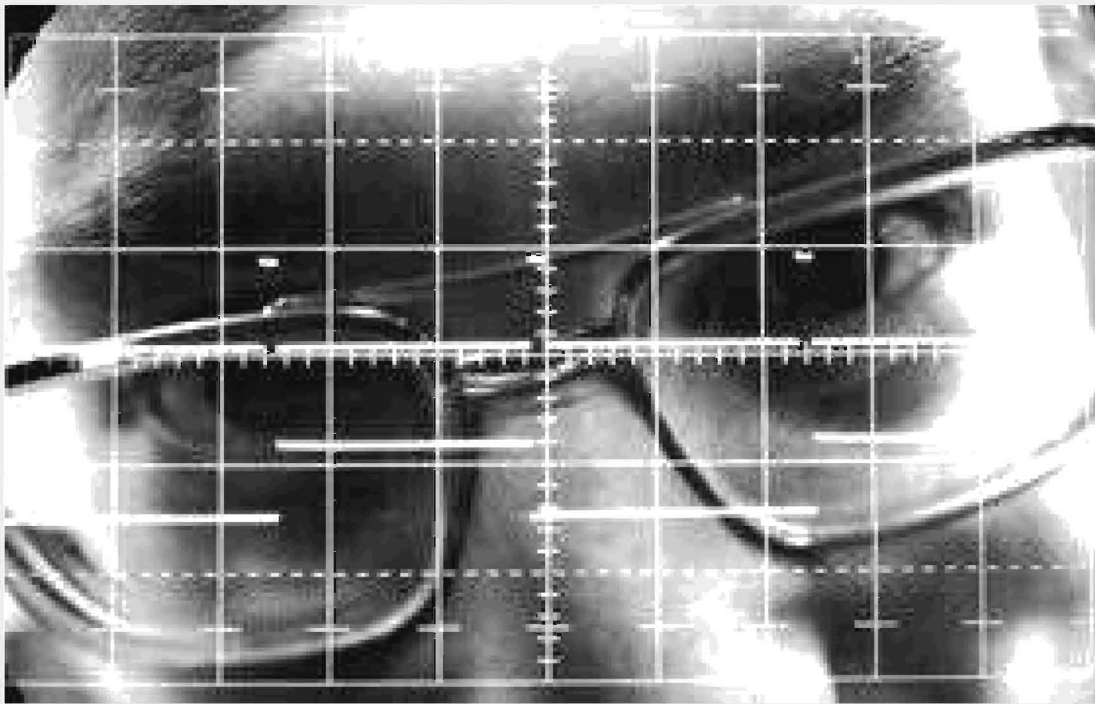


A Tribute to Jim Williams

**Linear Technology Corporation
Application and Design Notes**



Understanding and Applying the LT1005 Multifunction Regulator

Jim Williams

The number of voltage regulators currently available makes the introduction of another regulator seem almost unnecessary. However, a new device, the LT1005, offers auxiliary functions which help solve problems often associated with voltage regulation in circuits.

The LT1005 (Figure 1) consists of a 5V, 1A[†] regulator, which is controlled by a positive logic enable pin, and a 5V auxiliary regulator. The auxiliary regulator's output is

unaffected by the state of the main regulator. Thermal overload protection and current limiting round out the device. The enable pin is a high impedance input which floats in a high state. 10 μ A[†] of current pulled from the pin will force it below its 1.6V turn-off threshold, shutting down the main output. Figure 2A shows a simple but useful application. Here, the regulator's enable pin is controlled by the state of a toggling flip-flop which is triggered by a pushbutton on a computer keyboard. The

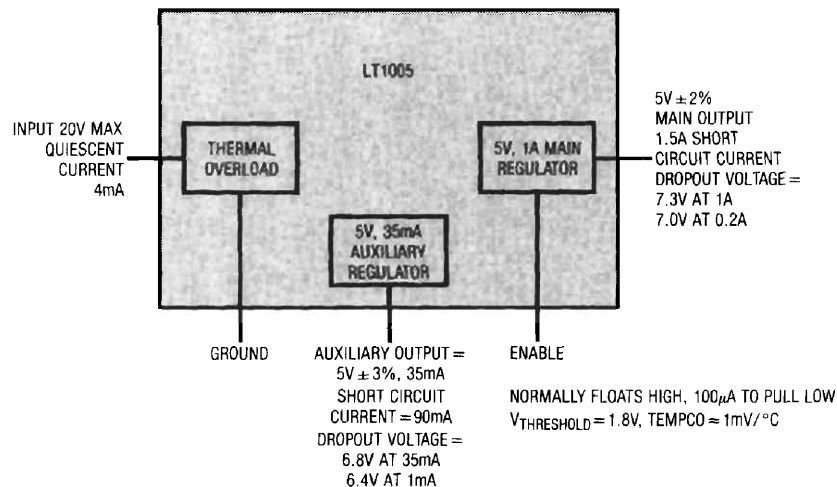


Figure 1

[†]A 3A version of the LT1005 is also available. See LT1035.

Application Note 1

auxiliary 5V output powers the flip-flop when the computer has been shut down. This arrangement allows the normal separate power switch to be eliminated. Although the enable pin interfaces directly to CMOS and TTL, its relatively high impedance allows it to implement a number of diverse functions.

Figure 2B is a power-on delay circuit. Upon application of power, the output is held low until the capacitor charges beyond the 1.6V threshold of the enable pin. In this case, the time required is about 100ms. The diode-1k combination drains the capacitor quickly when power is removed.

Figure 2C shows a simple arrangement which will latch down the main regulator output if a short circuit occurs in

the load. When power is applied to the regulator, the 5V auxiliary output comes up, transferring charge through the 10 μ F unit. This forces the enable pin high, allowing the main regulator to come up and power the load. If a load short occurs, the regulator goes into current limit and the main output falls to zero. This pulls the enable pin low, completing a positive feedback latch which disables the main regulator output. Under these conditions the output will remain at zero, even after the load short is removed. Also, the regulator will not have to dissipate power for the duration of the short circuit. The output may be reset by removing regulator input power or forcing the enable pin.

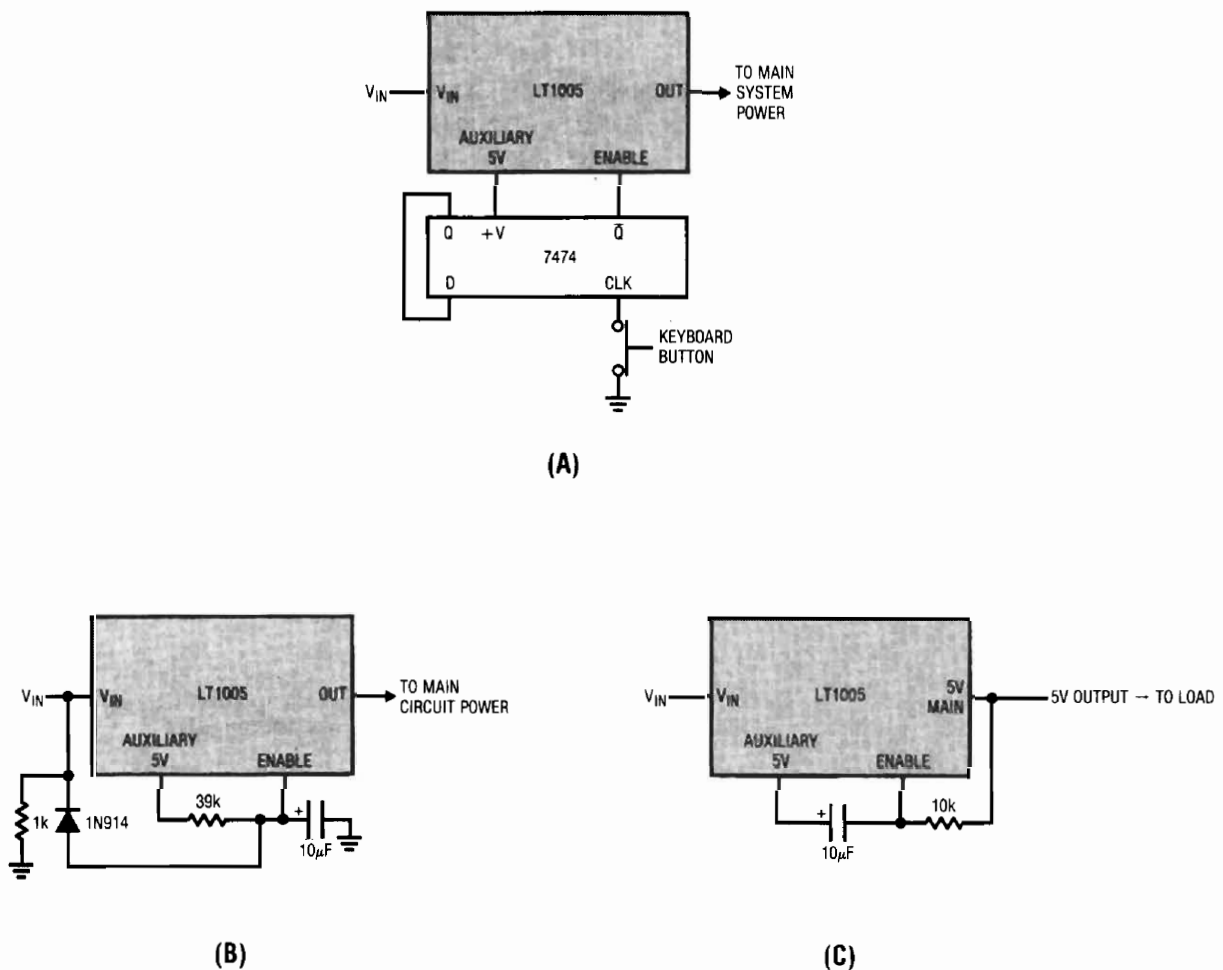


Figure 2

Figure 3 illustrates a circuit which takes advantage of this operation to achieve a cost-effective solid-state equivalent of a circuit breaker. This circuit will turn off the main regulator's output within 700ns of an over-load. The trip current and breaker delay times are settable over a wide range. Under normal conditions the current through the 1Ω shunt is insufficient to bias Q1 into conduction. Q2 is also off and the regulator functions. When an overload occurs (Trace A, Figure 4 is the regulator's output current), the potential across the 1Ω resistor rises, turning on Q1. Q1's collector drives Q2's base (Trace B, Figure 4) via the 1k resistor and the 100pF speed-up capacitor. This turns on Q2, pulling the enable pin (Trace C, Figure 4) to ground and shutting down the regulator output (Trace D, Figure 4). The 10k value from the main output to the enable pin latches the regulator down in a fashion similar to Figure 1 and the 4.7μF capacitor shown in dashed lines may be added (delete the 100pF unit) for applications where fast response is not desirable. The 1Ω value can be selected to accommodate any desired current trip point.

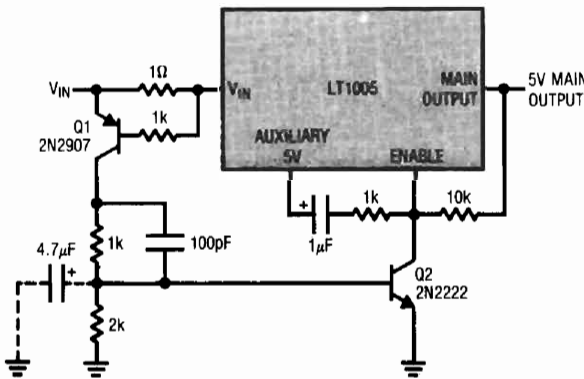


Figure 3

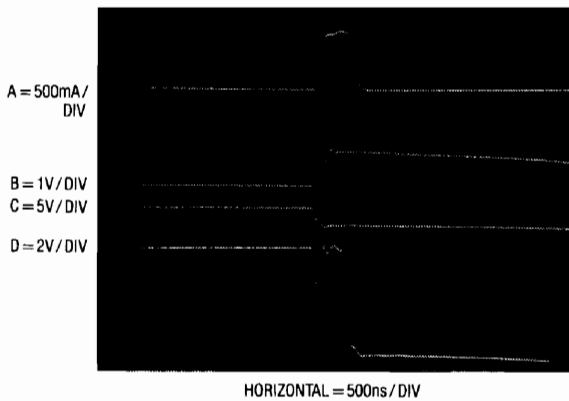


Figure 4

Figure 5 shows another circuit which uses the enable pin to shut down the regulator under abnormal conditions.

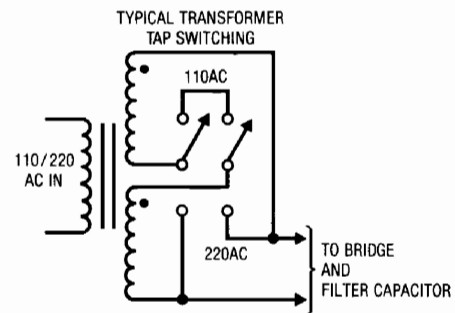
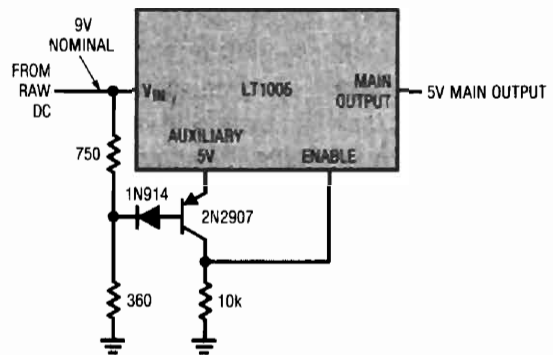


Figure 5

This configuration is useful in instruments or systems meant to be powered from 110VAC or 220VAC. Powering a regulator from a 220VAC primary when the secondary transformer tap switch is set for 110VAC forces excessive dissipation in the regulator, leading to thermal shutdown. The circuit shown prevents this by sensing the abnormally high input voltage and shutting down the regulator. Under normal operating conditions the input voltage is low enough to keep the transistor on, pulling the enable pin toward the auxiliary output and maintaining regulator output. If the circuit is inadvertently powered from 220VAC without moving the transformer tap switch, the regulator's input voltage rises. This cuts off the transistor and the 10k resistor pulls the enable pin to ground, shutting down the regulator. The diode in the transistor's base line prevents V_{BE} zenering during the reverse bias condition which exists during the shutdown. For the values given, this circuit will function properly over ranges of 88VAC–135VAC and 180VAC–260VAC (110VAC–220VAC \pm 20%).

Application Note 1

Figure 6 shows the LT1005 in another circuit where operation depends on input conditions. This circuit is useful in systems where it is necessary to bring up and power-down circuitry in a sequence. It is particularly applicable in situations where it is desirable to transfer and store data into nonvolatile memory during power outages. It functions by taking advantage of the differing dropout voltages between the main and auxiliary outputs. When power is first applied, the LT1005 input (Trace A, Figure 7) starts to ramp up. The auxiliary output (Trace D, Figure 7) follows this ramping action and clamps at its 5V regulated output. During this interval, C1 monitors the difference between the regulator input and the 5V auxiliary output. The resistor ratios at its inputs are scaled so that the enable pin (Trace B, Figure 7) will be clamped until the regulator input is high enough to support main output regulation. (The small ramp segments visible at the enable pin are

due to the comparator output's failure to clamp under very low supply voltage conditions. They do not influence overall circuit operation.) When this point is reached, the main output (Trace C, Figure 7) comes up quickly. Because the auxiliary output precedes the main output, it can be used to preset conditions in the circuitry being powered by the regulator. When power falls below the threshold point, C1 pulls the enable pin (Trace B, Figure 7) low, forcing the regulator's main output to go off rapidly. The auxiliary output, however, maintains regulation after the main output has gone off. This allows the main output to be used as a logic signal to alert auxiliary-powered nonvolatile memory to store data. The amount of time the auxiliary output will maintain regulation on power-down may be controlled by regulator filter capacitor size. The diode-4.7k combination provides regenerative action to assure a clean turn-off for the main output.

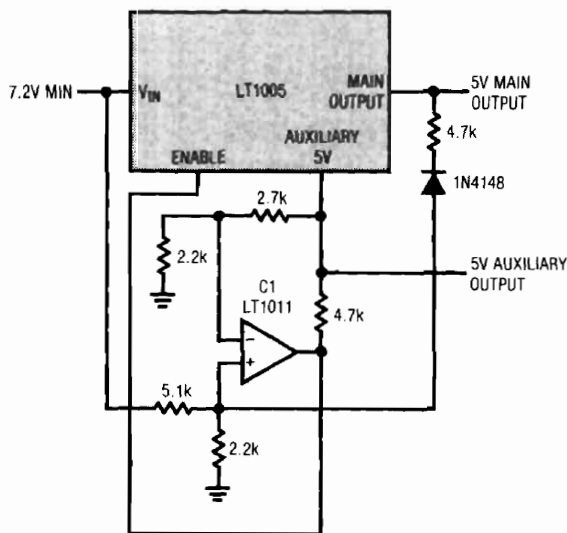


Figure 6

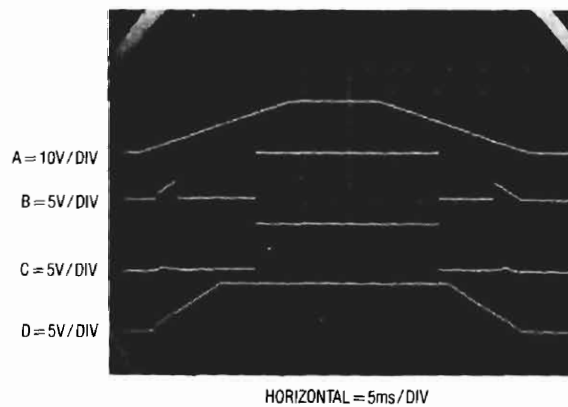


Figure 7

In some systems it is more convenient, or advantageous, to detect power outages by directly monitoring the AC line. Figure 8's circuit does this by connecting an optoisolator across the AC output of the power transformer. Normally, the AC line (Trace A, Figure 9) turns on the LED every 8ms ($1/2$ cycle of the line), causing the Darlington output transistor to reset the $0.01\mu\text{F}$ capacitor to $V_{CE(SAT)}$. When the line drops out (Trace B, Figure 9), the capacitor charges at a rate dependent upon the setting of the 20k potentiometer. This ramping voltage is compared by C1 to a refer-

ence derived from the auxiliary output. When C1 goes low, the regulator output goes low (Trace C, Figure 9). This occurrence can be used as a logic signal to flag circuitry which is powered by the auxiliary output. The "trip set" potentiometer and the value of the capacitor can be used to determine the number of missing line cycles required to shut down the regulator. When using this circuit it is important to recognize that the hold-up time of the raw supply must be taken into account to determine how long the auxiliary output will remain regulated.

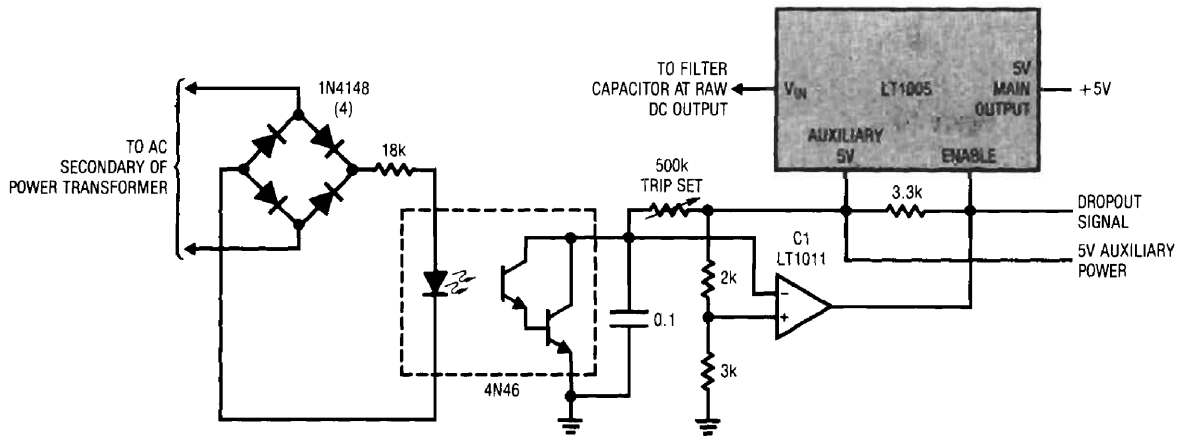


Figure 8

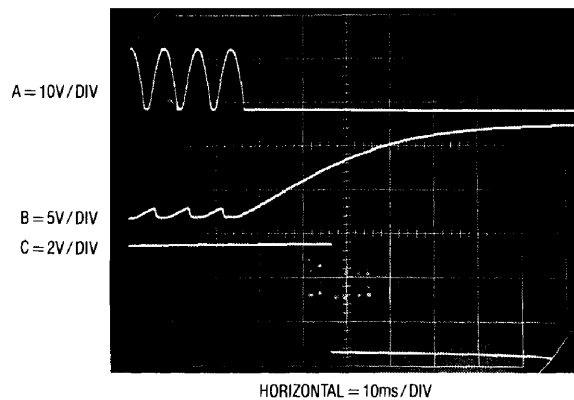


Figure 9

Application Note 1

Figure 10 shows a latching circuit similar to Figure 2, except that a negative temperature coefficient (NTC) sharp transition thermistor runs from the enable pin to ground.

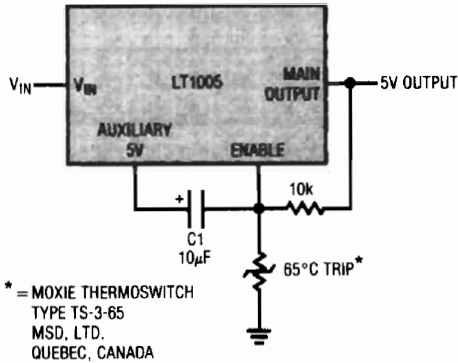


Figure 10

This circuit will provide latching protection for circuitry under thermal overloads due to blocked vents or fan failures. The NTC device resistance decreases from 200k at 60°C to 10k at 65°C, cutting off the regulator. The thermistor is biased from the output, so latch-off occurs when the trip temperature is reached. C1 ensures starting. Unfortunately, the transition and hysteresis points of NTC devices are fixed and cannot be user-varied. Figure 11 takes-advantage of the relatively high impedance of the enable input to circumvent this problem. A standard thermistor (negative temperature coefficient) allows the trip point and hysteresis band to be set at any desired point. For the example shown, the regulator will shut down at 58°C ambient (8k thermistor resistance) and come back up at 42°C (15.2k thermistor resistance). Other characteristics are obtainable by shifting resistor and thermistor values.

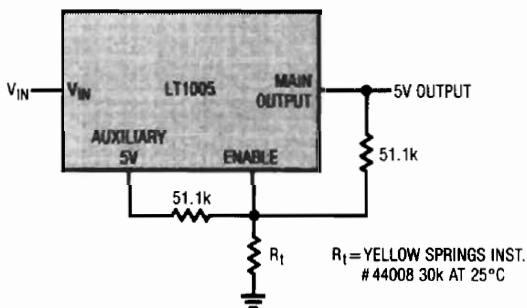


Figure 11

Figure 12 shows another thermally-related use of the regulator. The highest crystal oscillator stabilities are achieved by temperature-stabilizing the crystal. In frequency-measuring equipment and communications work it is often important that the crystal frequency be stabilized before the equipment is used. In this circuit, the LT1005 combines with a typical commercial crystal oven to prevent equipment use until oven temperature has stabilized. When power is applied, pin 6 of the crystal oven is high, biasing Q1. Simultaneously, the SCR gate is triggered by auxiliary-generated output current coming through the 4.7 μ F unit. This disables the main regulator output. When the oven reaches temperature, the thermoswitch opens, removing bias from Q1. This commutates the SCR and the regulator comes up, allowing its load to operate. The 4.7k resistor eliminates false SCR triggering and the diode suppresses reverse gate current when regulator input power is removed.

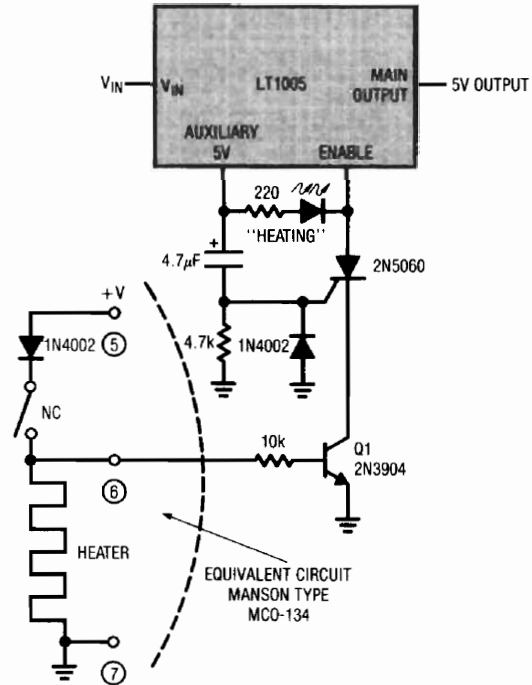
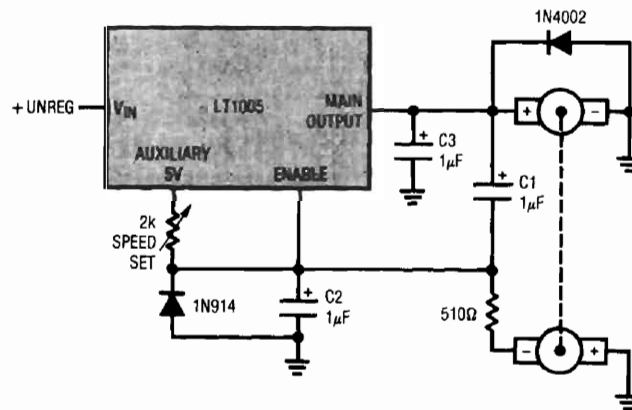


Figure 12

The latching action used in many of the preceding applications is one form of feedback. *Negative* feedback to the enable pin can be used to make closed loop servos. Figure 13 shows a way to make a simple switched-mode motor speed controller with the LT1005. This circuit uses a tachometer to generate a feedback signal which is compared to a reference supplied by the auxiliary output. When power is applied, the tachometer output is zero and the regulator output (Trace A, Figure 14) comes on, forcing current (Trace C, Figure 14) into the motor. As motor rotation increases, the negative tachometer output pulls the enable pin (Trace B, Figure 14) toward ground. When the enable pin's threshold voltage is reached, the regulator output goes down and the motor slows. C1 provides positive feedback, ensuring clean transitions. In this fashion, the motor's speed is servo-controlled at a point

determined by the 2k potentiometer setting. The regulator free-runs at whatever frequency and duty cycle are required to maintain the enable pin at its threshold. Loop bandwidth and stability are set by C2 and C3. The 1N914 diode prevents the negative output tachometer from pulling the enable pin below ground while the 1N4002 commutates the motor's negative flyback pulse. The servo-controlled pulse mode excitation allows the motor to furnish excellent torque characteristics, even when operating at 5% of its full speed rating. For example, the small motor listed, with a shaft torque rating of 20 gram-cMs at 3300RPM, is almost unstoppable by the unaided human hand at 150RPM. The thermal and current limiting in the regulator prevents either the motor or the regulator from burning up in the event of a shaft overload.



MOTOR-TACH = CANON #EF-26-R1-N1

Figure 13

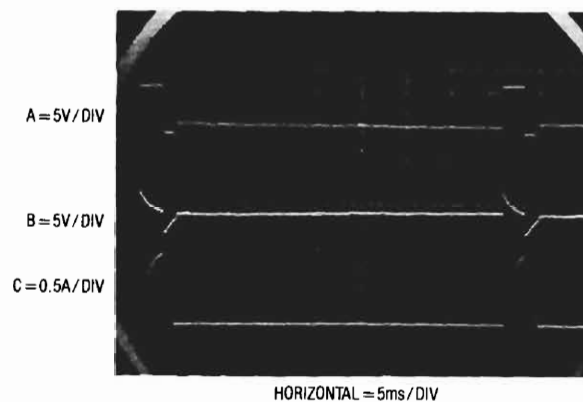


Figure 14

Application Note 1

Figure 15 shows a way to run higher voltage motors. In this mode the motor is placed in the regulator input line and the output is terminated into a 3.3Ω load. The servo loop operates in a similar fashion to the one in Figure 13. In this case, however, a large capacitor is placed at the regulator to filter the transients generated by motor switching. When the tachometer output (Trace A, Figure 16) calls for power, the regulator comes on, allowing current to flow through the motor. This forces the regulator input toward ground (Trace B, Figure 16) for the duration of the on-time. The

circuit's advantage is that it allows higher voltage motors (up to 20V) to be controlled. In common with the previous circuit, the regulator provides thermal and current overload protection for the motor. Its disadvantage is that for servo setpoints which require high motor power, the regulator's DC input will go below dropout and the auxiliary output will fall, destabilizing the servo setpoint. Each of these circuits offers a simple, cost-effective, one package solution to speed control of small motors at the expense of efficiency.

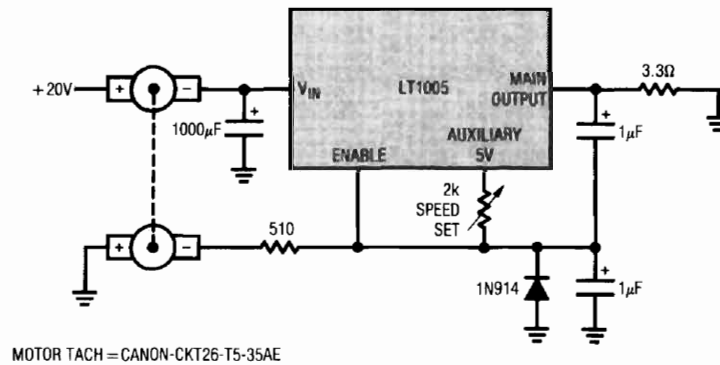


Figure 15

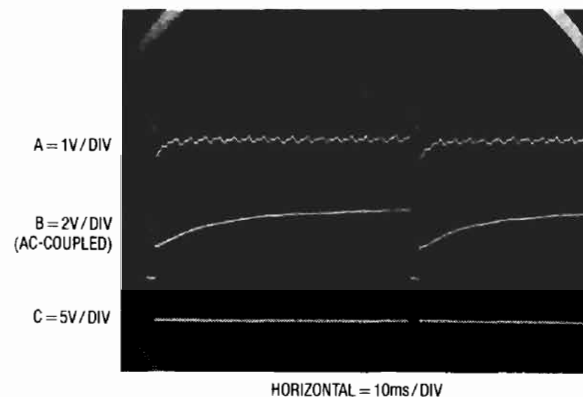


Figure 16

Performance Enhancement Techniques for Three-Terminal Regulators

Jim Williams

Three terminal regulators provide a simple, effective solution to voltage regulation requirements. In many situations the regulator can be used with no special considerations. Some applications, however, require special techniques to enhance the performance of the device.

Probably the most common modification involves extending the output current of regulators. Conceptually, the simplest way to do this is by paralleling devices. In practice, the voltage output tolerance of the regulators can cause problems. Figure 1 shows a way to use two regulators to achieve an output current equal to their sum. This circuit capitalizes on the 1% output tolerance of the specified regulators to achieve a simple paralleled configuration. Both regulators sense from the same divider string and the small value resistors provide ballast to account for the slightly differing output voltages. This added impedance degrades total circuit regulation to about 1%.

Figure 2 shows another way to extend current capability in a regulator. Although this circuit is more complex than Figure 1, it eliminates the ballasting resistor's effects and has a fast-acting logic-controlled shutdown feature. Additionally, the current limit may be set to any desired value. This circuit extends the 1A capacity of the LT1005 multi-function regulator to 12A, while retaining the LT1005's enable feature and auxiliary 5V output. Q1, a booster transistor, is servo-controlled by the LT1005, while Q2 senses the current dependent voltage across the 0.05Ω shunt. When the shunt voltage is large enough, Q2 comes on, biasing Q3 and shutting down the regulator via the LT1005's enable pin. The shunt's value can be selected for the desired current limit. The 100°C thermoswitch limits dissipation in Q1 during prolonged short circuits by disabling the LT1005. It should be mounted on Q1's heat sink.

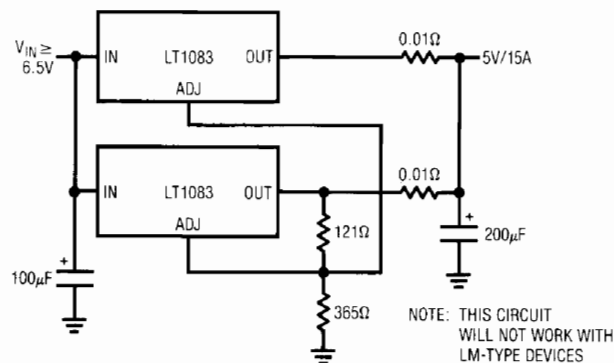


Figure 1

Application Note 2

Boosted regulator schemes of this type are often poorly dynamically damped. Such improper loop compensation results in large output transients for shifts in the load. In particular, because Q1's common emitter configuration has voltage gain, transients approaching the input voltage are possible when the load drops out. Here, the 100 μ F capacitor damps Q1's tendency to overshoot, while the 20 Ω value provides turn-off bias. The 250 μ F unit maintains Q1's emitter at DC. Figure 3 shows that this "brute force" compensation works quite well. Normally the regulator sees no load. When Trace A goes high, a 12A load (regulator output current is Trace C) is placed across the output terminals. The regulator output voltage recovers quickly, with minimal aberration.

While the 100 μ F output capacitor aids stability, it prevents the regulator output from dropping quickly when the enable command is given. Because Q1 cannot sink current, the 100 μ F unit's discharge time is load limited. Q4 corrects this problem, even when there is no load. When the enable command is given (Trace A, Figure 4) Q3 comes on, cutting off the LT1005 and forcing Q1 off. Simultaneously, Q4 comes on, pulling down the regulator output (Trace B), and sinks the 100 μ F capacitor's discharge current (Trace C). If fast turn-off is not needed, Q4 may be omitted.

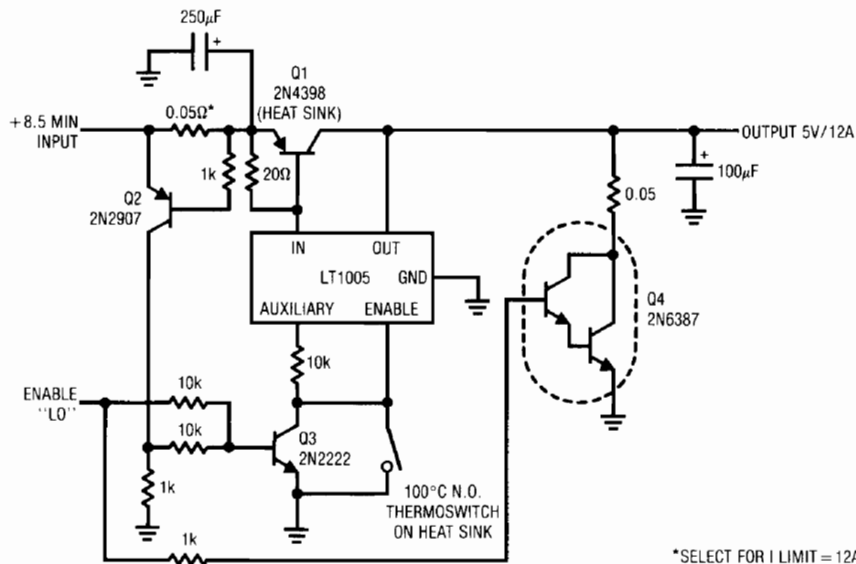


Figure 2

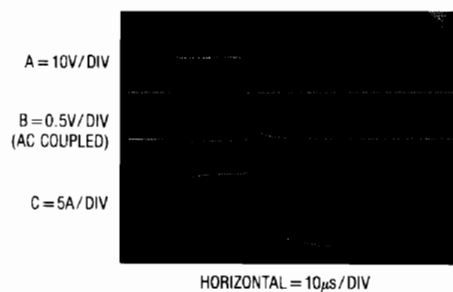


Figure 3

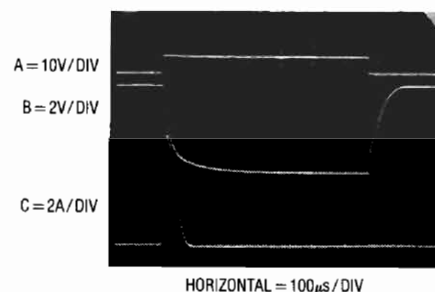


Figure 4

Power dissipation control is another area where regulators can be helped by additional circuitry. Increasing heat sink area can be used to offset dissipation problems, but is a wasteful and inefficient approach. Instead, the regulator can be placed within a switched-mode loop that servo-controls the voltage *across* the regulator. In this arrangement the regulator functions normally while the switched-mode control loop maintains the voltage across it at a minimal value, regardless of line or load changes. Although this approach is not quite as efficient as a classical switching regulator, it offers lower noise and the fast transient response of the linear regulator. Figure 5 details a DC driven version of the

circuit. The LT350A functions in the conventional fashion, supplying a regulated output at 3A capacity. The remaining components form the switched-mode dissipation limiting control. This loop forces the potential across the LT350A to equal the 3.7V value of V_Z . When the input of the regulator (Trace A, Figure 6) decays far enough, the LT1018 output (Trace B) switches low, turning on Q1 (Q1 collector is Trace D). This allows current flow (Trace C) from the circuit input into the 4500 μ F capacitor, raising the regulator's input voltage. When the regulator input rises far enough, the comparator goes high, Q1 cuts off and the capacitor ceases charging.

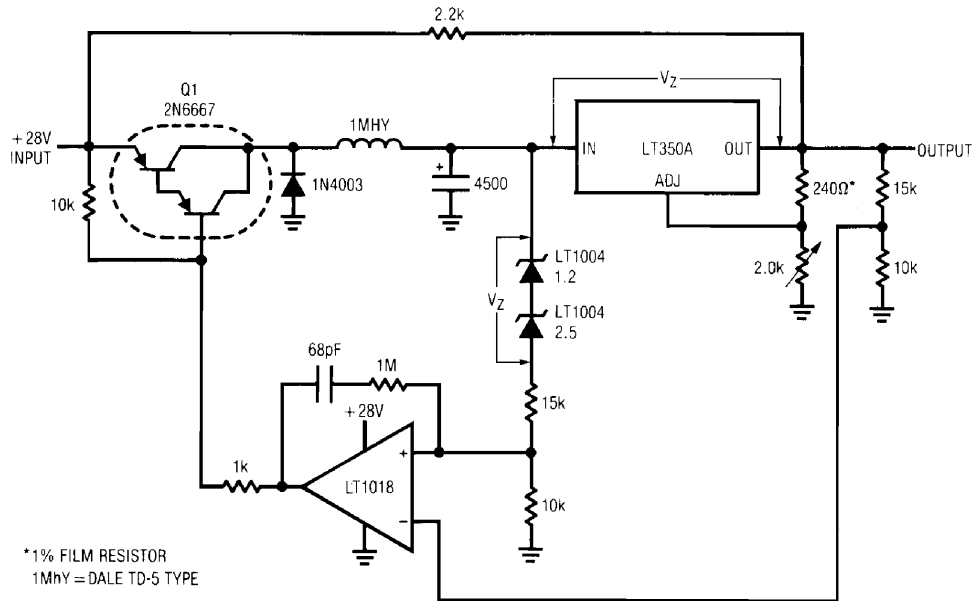


Figure 5

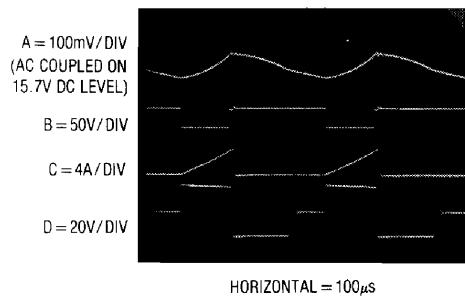


Figure 6

via C1. The resulting AC line synchronous ramp at C1's output is compared to A1's offset output by C2. A1's output represents the deviation from the V_z value that the loop is trying to force across the LT1038. When the ramp output exceeds C2's "+" input value, C2 pulls low, dumping current through T1's primary (Trace C). This fires the appropriate SCR and a path from the main transformer to the LC pair occurs (Trace D). The resultant current flow (Trace E) is limited by the inductor and charges the capacitor. When the AC line cycle drops low enough, the SCR commutates and charging ceases. On the next half-cycle the process repeats, except that the alternate SCR does the work. In this fashion, the loop controls the phase angle at which the SCRs fire to keep the voltage across the

LT1038 at V_z (3.7V). As a result, the circuit functions over all line, load and output voltage conditions with good efficiency. The 1.2V LT1004 at the LT1038 allows the output voltage to be set down to 0.00 and the 2N3904 clamp at A1 prevents loop "hangup". Figure 7A shows a way to trigger the SCRs without using a transformer.

Although A1's output is an analog voltage, the AC driven nature of the circuit makes it approximate a smoothed, sampled loop response. Conversely, the regulator constitutes a true linear system. Because these two feedback systems are interlocked, frequency compensation can be difficult.

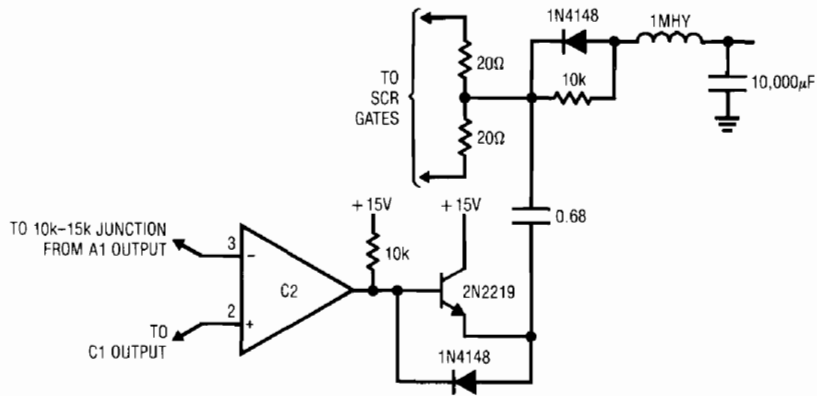


Figure 7A

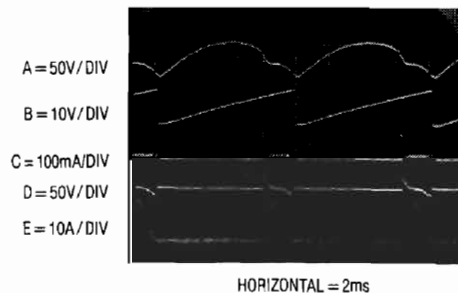


Figure 8

Application Note 2

In practice, A1's $1\mu\text{F}$ capacitor keeps dissipation loop gain at a low enough frequency for stable characteristics, without influencing the LT1038's transient response characteristic. Trace A, Figure 9 shows the output noise while the circuit is operating at 35V into a 10A load (350W). Note the absence of fast switching transients and harmonics. The output noise is made up of residual 120Hz ripple and regulator noise. Reflected noise into the AC power line is also negligible (Trace B) because the inductor limits current rise time to about 1ms, much slower than the normal switching supplies. Figure 10 shows a plot of efficiency versus output voltage for a 10A load. At low output voltages, where the static losses across the regulator and SCRs are significant, efficiency suffers, but 85% is attained at the upper extreme.

High voltage output is another area for regulator enhancement. In theory, because the regulator does not have a ground pin, it can regulate high voltages. In normal operation the regulator floats at the supply's upper level, and as long as the $V_{\text{IN}}-V_{\text{OUT}}$ maximum differential is not exceeded there are no problems. However, if the output is shorted, the $V_{\text{IN}}-V_{\text{OUT}}$ maximum is exceeded and device destruction will occur. The circuit of Figure 11 shows a complete high voltage regulator that delivers 100V at 100mA and withstands shorts to ground. Even at 100V output the LT317A functions in the normal mode, maintaining 1.2V between its output and adjustment pin.

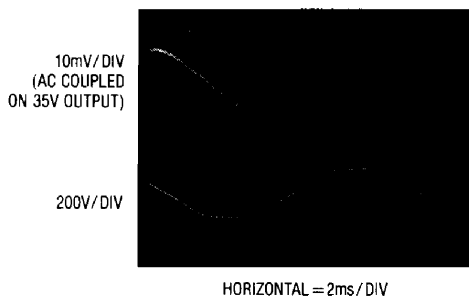


Figure 9

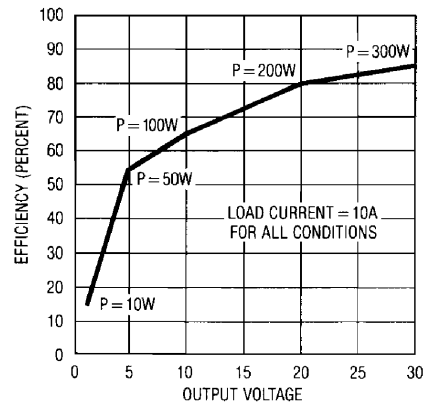


Figure 10

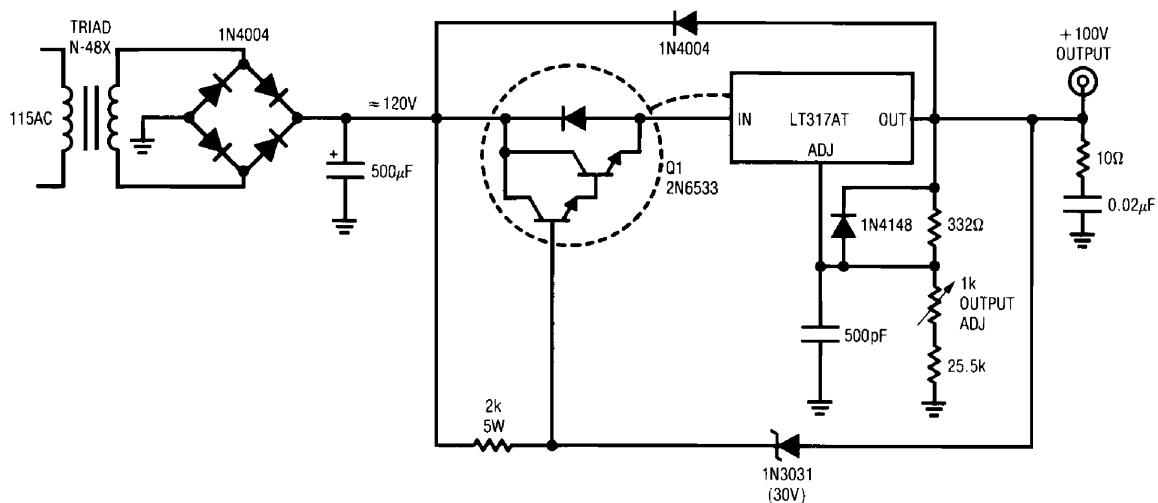


Figure 11

Under these conditions the 30V zener is off and Q1 conducts. When an output short occurs, the zener conducts, forcing Q1's base to 30V. This causes Q1's emitter to clamp $2 V_{BE}$ s below V_Z , well within the $V_{IN}-V_{OUT}$ rating of the regulator. Under these conditions, Q1, a high voltage device, sustains 90V V_{CE} at whatever current the transformer and the regulator's current limit will support. The transformer specified saturates at 130mA, keeping Q1 well within its safe area as it dissipates 12W. If Q1 and the LT317A are thermally coupled, the regulator will soon go into thermal shutdown and oscillation will commence. This action will continue, protecting the load and the regulator as long as the output remains shorted. The 500pF capacitor and the $10\Omega-0.02\mu F$ damper aid transient response and the diodes provide safe discharge paths for the capacitors.

This approach to high voltage regulation is primarily limited by the power dissipation capability of the device in series with the regulator. Figure 11A uses a vacuum tube (remember them?) to achieve very high short circuit dissipation capability. The tube allows high voltage operation and is extremely tolerant of overloads. This circuit allows the LT317A to control 600W at 2000V (V_1 's plate limit is 300mA) with full short circuit protection.

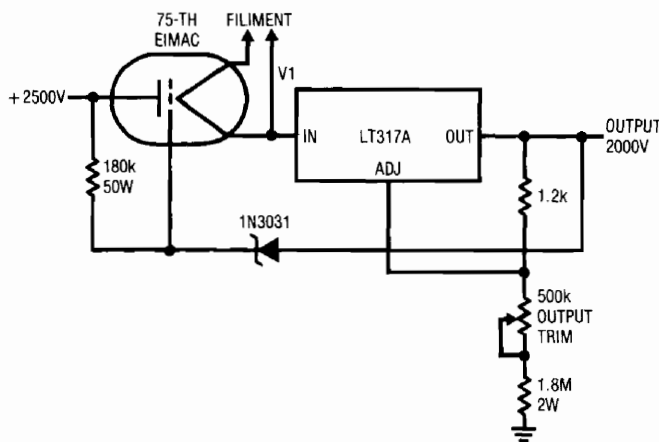


Figure 11A

Power is not the only area in which regulator performance can be augmented. Figure 12 shows a way to increase the stability of a regulator's output over time and temperature. This is particularly useful in powering strain gauge-based transducers. In this circuit the output voltage is divided down and compared to the 2.5V reference by A1, a precision amplifier. A1's output is used to force the LT317A's adjustment pin to whatever voltage is required to maintain the 10V output. A1 contributes negligible error. The resistors specified will track within 5ppm/ $^{\circ}C$ and the reference contributes about 20ppm/ $^{\circ}C$. The regulator's internal circuitry protects against short circuits and thermal overload.

Figure 13's circuit allows a regulator to remotely sense the feedback voltage, eliminating the effects of voltage drop in the supply lines. This is a concern where high currents must be transmitted over relatively long supply rails or PC traces. Figure 13's circuit uses A1 to sense the voltage at the point of load. A1's output, summed with the regulator's output, modifies the adjustment pin voltage to compensate for the voltage lost across R_{DROP} . The feedback divider is returned through a separate lead from the load, completing the remote sensing scheme. The $5\mu F$ capacitor filters noise and the 1k value limits bypass capacitor discharge when power is turned off.

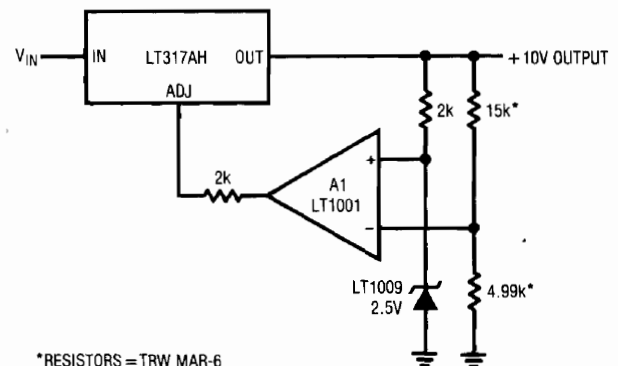


Figure 12

Applications for a Switched-Capacitor Instrumentation Building Block

Jim Williams

CMOS analog IC design is largely based on manipulation of charge. Switches and capacitors are the elements used to control and distribute the charge. Monolithic filters, data converters and voltage converters rely on the excellent characteristics of IC CMOS switches. Because of the importance of switches in their circuits, CMOS designers have developed techniques to minimize switch induced errors, particularly those associated with stray capacitance and switch timing. Until now, these techniques have been used only in the internal construction of monolithic devices. A new device, the LTC[®]1043, makes these switches available for board-level use. Multi-pole switching and a self-driven, non-overlapping clock allow the device to be used in circuits which are impractical with other switches.

Conceptually, the LTC1043 is simple. Figure 1 details its features. The oscillator, free-running at 200kHz, drives a non-overlapping clock. Placing a capacitor from Pin 16 to ground shifts the oscillator frequency downward to any desired point. The pin may also be driven from an external source, synchronizing the switches to external circuitry. A non-overlapping clock controls both DPDT switch sections. The non-overlapping drive prevents simultaneous conduction in the series connected switch sections.

Charge balancing circuitry cancels the effects of stray capacitance. Pins 1 and 10 may be used as guard points for Pins 3 and 12 in particularly sensitive applications.

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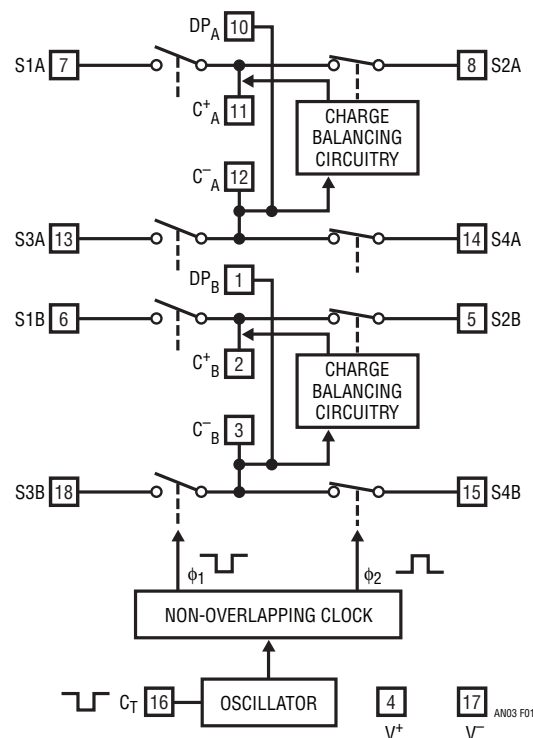


Figure 1. Block Diagram of LTC1043 Showing Individual Switches

Application Note 3

Although the device's operation is simple, it permits surprisingly sophisticated circuit functions. Additionally, the careful attention paid to switching characteristics makes implementing such functions relatively easy. Discrete timing and charge-balance compensation networks are eliminated, reducing component count and trimming requirements.

Classical analog circuits work by utilizing continuous functions. Their operation is usually described in terms of voltage and current. Switched-capacitor based circuits are sampled data systems which approximate continuous functions with bandwidth limited by the sampling frequency. Their operation is described in the distribution of charge over time. To best understand the circuits which follow, this distinction should be kept in mind. Analog sampled data and carrier-based systems are less common than true continuous approaches, and developing a working familiarity with them requires some thought.

Switched-capacitor approaches have greatly aided analog MOS IC design. The LTC1043 brings many of the freedoms and advantages of CMOS IC switched-capacitor circuits to the board level, providing a valuable addition to available design techniques.

Instrumentation Amplifier

Figure 2 uses the LTC1043 to build a simple, precise instrumentation amplifier. An LTC1043 and an LT[®]1013 dual op amp are used, allowing a dual instrumentation amplifier using just two packages. A single DPDT section converts the differential input to a ground referred single-ended signal at the LT1013's input. With the input switches closed, C1 acquires the input signal. When the input switches open, C2's switches close and C2 receives charge. Continuous clocking forces C2's voltage to equal the difference between the circuit's inputs. The 0.01 μ F capacitor at Pin 16 sets the switching frequency at 500Hz. Common mode voltages are rejected by over 120dB and drift is low.

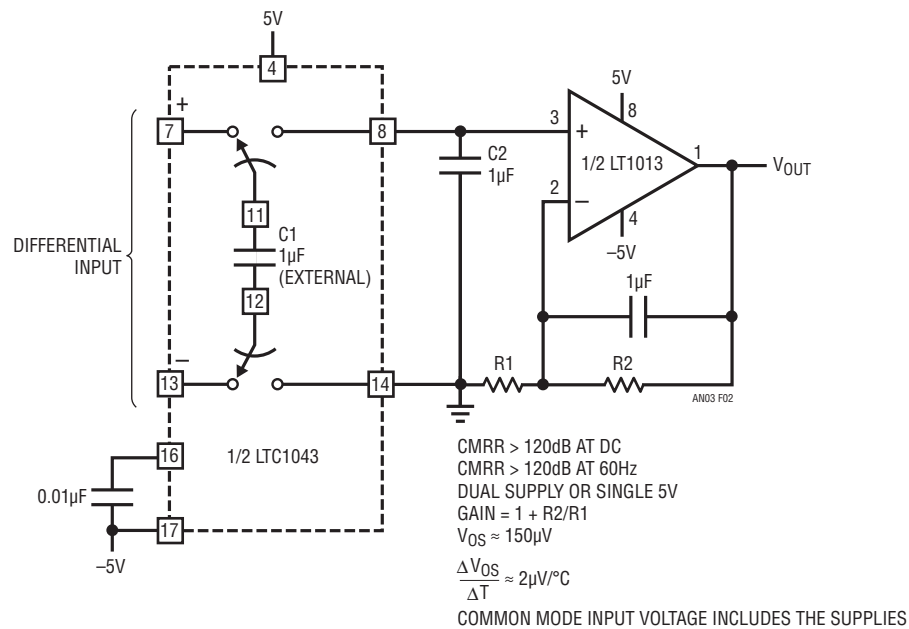


Figure 2. $\pm 5\text{V}$ Precision Instrumentation Amplifier

Amplifier gain is set in the conventional manner. This circuit is a simple, economical way to build a high performance instrumentation amplifier. Its DC characteristics rival any IC or hybrid unit and it can operate from a single 5V supply. The common mode range includes the supply rails, allowing the circuit to read across shunts in the supply lines. The performance of the instrumentation amplifier depends on the output amplifier used. Specifications for an LT1013 appear in the figure. Lower figures for offset, drift and bias current are achievable by employing type LT1001, LT1012, LT1056 or the chopper-stabilized LTC1052.

Ultrahigh Performance Instrumentation Amplifier

Figure 3 is similar to Figure 2, but utilizes the remaining LTC1043 section to construct a low drift chopper amplifier. This approach maintains the true differential inputs while achieving $0.1\mu\text{V}/^\circ\text{C}$ drift. The differential input is converted to a single-ended potential at Pin 7 of the LTC1043. This voltage is chopped into a 500Hz square wave by the switching action of Pins 7, 11 and 8. A1, AC-coupled, amplifies this signal. A1's square wave output, also AC-coupled, is synchronously demodulated by switches 12, 14 and 13. Because this switch section is synchronously driven with

the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage to provide the output. The output is divided down and fed back to Pin 8 of the input chopper where it serves as the zero signal reference. Because the main amplifier is AC-coupled, its DC terms do not affect overall circuit offset, resulting in the extremely low offset and drift noted in the specifications. This circuit offers lower offset and drift than any commercially available instrumentation amplifier.

Lock-In Amplifier

The AC carrier approach used in Figure 3 may be extended to form a "lock-in" amplifier. A lock-in amplifier works by synchronously detecting the carrier modulated output of the signal source. Because the desired signal information is contained within the carrier, the system constitutes an extremely narrow-band amplifier. Non-carrier related components are rejected and the amplifier passes only signals which are coherent with the carrier. In practice, lock-in amplifiers can extract a signal 120dB below the noise level.

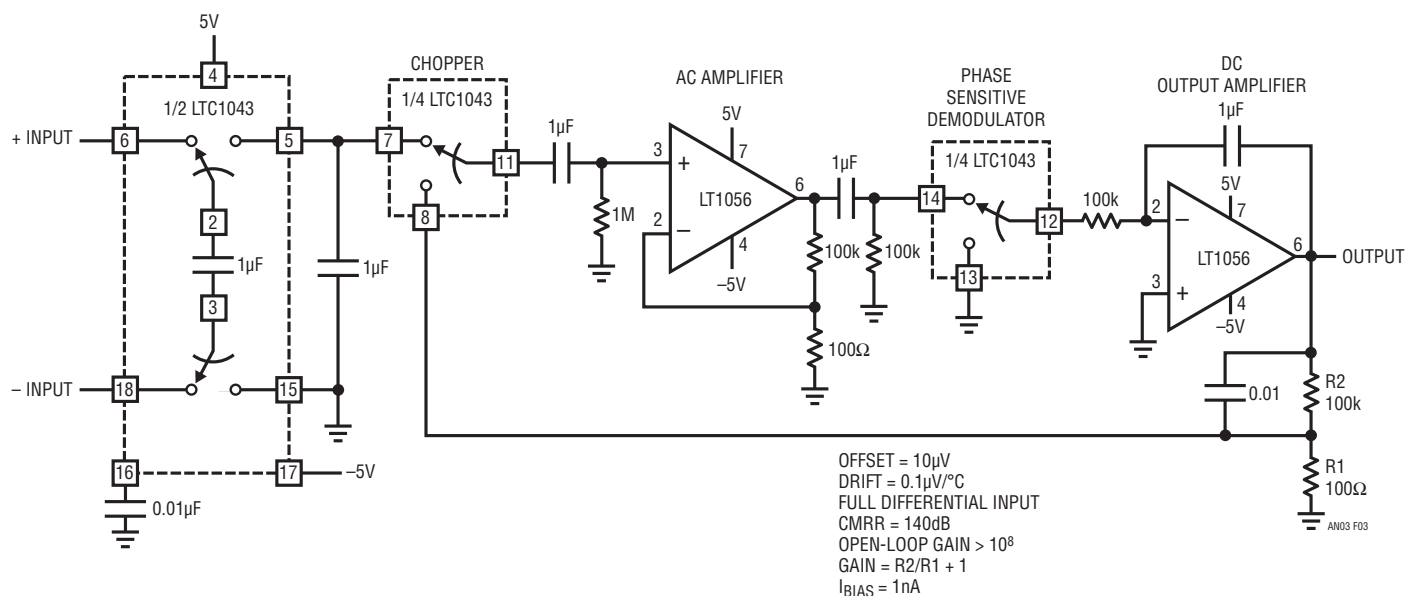


Figure 3. Chopper-Stabilized Instrumentation Amplifier

Application Note 3

Figure 4 shows a lock-in amplifier which uses a single LTC1043 section. In this application, the signal source is a thermistor bridge which detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber.

The 500Hz carrier is applied at T1's input (Trace A, Figure 5). T1's floating output drives the thermistor bridge, which presents a single-ended output to A1. A1 operates at an AC gain of 1000. A 60Hz broadband noise source is also deliberately injected into A1's input (Trace B). The carrier's zero crossings are detected by C1. C1's output clocks the LTC1043 (Trace C). A1's output (Trace D) shows

the desired 500Hz signal buried within the 60Hz noise source. The LTC1043's zero-cross-synchronized switching at A2's positive input (Trace E) causes A2's gain to alternate between plus and minus one. As a result, A1's output is synchronously demodulated by A2. A2's output (Trace F) consists of demodulated carrier signal and non-coherent components. The desired carrier amplitude and polarity information is discernible in A2's output and is extracted by filter averaging at A3. To trim this circuit, adjust the phase potentiometer so that C1 switches when the carrier crosses through zero.

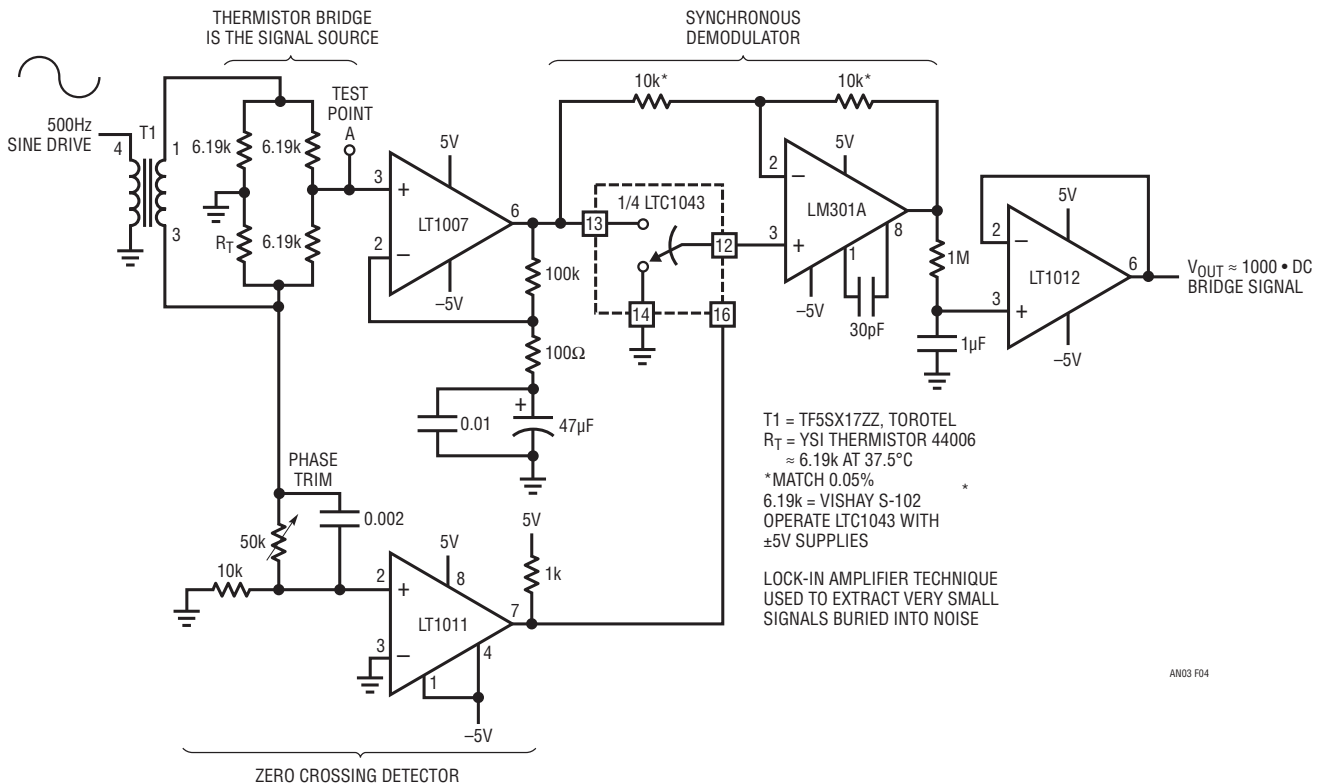


Figure 4. Lock-In Amplifier

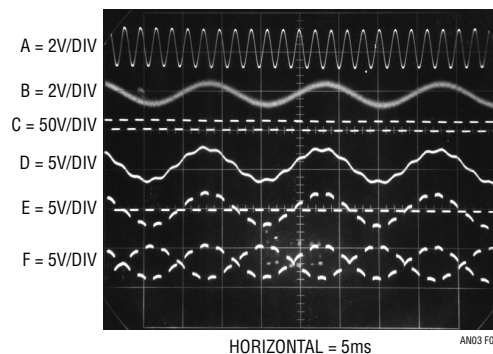


Figure 5

Wide Range, Digitally Controlled, Variable Gain Amplifier

Aside from low drift and noise rejection, another dimension in amplifier design is variable gain. Designing a wide range, digitally variable gain block with good DC stability is a difficult task. Such configurations usually involve relays or temperature compensated FET networks in expensive and complex arrangements. The circuit shown in Figure 6 uses the LTC1043 in a variable gain amplifier which features continuously variable gain from 0 to 1000, gain stability of 20ppm/°C and single-ended or differential input. The circuit uses two separate LTC1043s. Unit A is clocked by a frequency input which could be derived from a host processor. LTC1043B is continuously clocked by a 1kHz source which could also be processor supplied. Both LTC1043s function as the sampled data equivalent of a resistor within the bandwidth set by A1's 0.01μF value and the switched-capacitor equivalent feedback resistor. The time-averaged current delivered to the summing point by LTC1043A is a function of the 0.01μF capacitor's input-derived voltage and

the commutation frequency at Pin 16. Low commutation frequencies result in small time-averaged current values, approximating a large input resistor. Higher frequencies produce an equivalent small input resistor. LTC1043B, in A1's feedback path, acts in a similar fashion. For the circuit values given, the gain is simply:

$$G = \frac{f_{IN}}{10} \cdot \frac{0.01\mu F}{100pF}$$

Gain stability depends on the ratiometric stability between the 1kHz and variable clocks (which could be derived from a common source) and the ratio stability of the capacitors. For polystyrene types, this will typically be 20ppm/°C. The circuit input, determined by the pin connections shown in the figure, may be either single-ended or fully differential. Additionally, although A1 is connected as an inverter, the circuit's overall transfer function may be either positive or negative. As shown, with Pins 13A and 7A grounded and the input applied to 8A, it is negative.

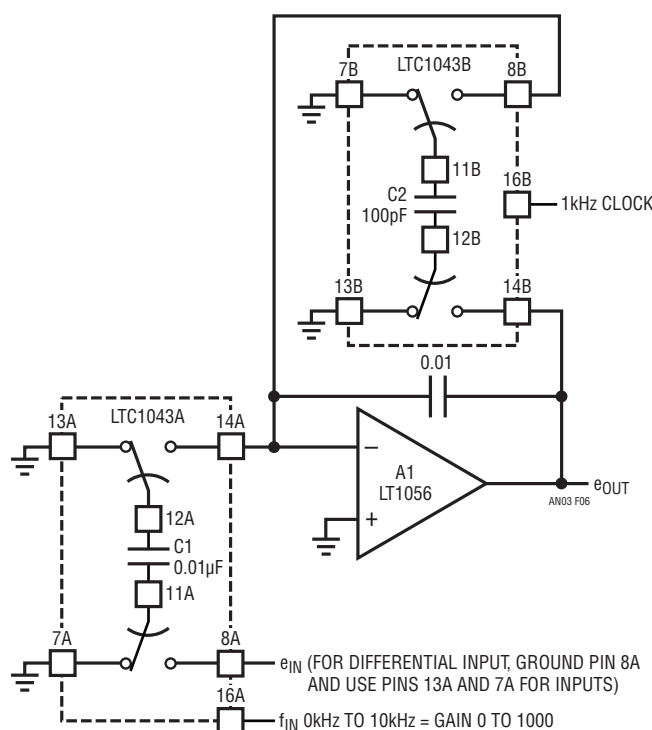


Figure 6. Variable-Gain Amplifier

Application Note 3

Precision, Linearized Platinum RTD Signal Conditioner

Figure 7 shows a circuit which provides complete, linearized signal conditioning for a platinum RTD. One side of the RTD sensor is grounded, often desirable for noise considerations. This LTC1043 based circuit is considerably simpler than instrumentation or multi-amplifier based designs and will operate from a single 5V supply. A1 serves as a voltage-controlled ground referred current source by differentially sensing the voltage across the 887Ω feedback resistor. The LTC1043 section which does this presents a single-ended signal to A1's negative input, closing a loop. The 2k-0.1μF combination sets amplifier roll-off well below the LTC1043's switching frequency and the configuration is stable. Because A1's loop forces a fixed voltage across the 887Ω resistor, the current through R_P is constant. A1's operating point is primarily fixed by the 2.5V LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The nonlinearity could cause several degrees of error over the circuit's 0°C to 400°C operating range. A2 amplifies R_P's output, while simultaneously supplying nonlinearity correction. The correction is implemented by feeding a portion of A2's output back to A1's input via the 10k to 250k divider. This causes the current supplied to R_P to slightly shift with its operating point, compensating sensor nonlinearity to within ±0.05°C. The remaining LTC1043 section furnishes A2 with a differential input. This allows an offsetting potential, derived from the LT1009 reference, to be subtracted from R_P's output. Scaling is arranged so 0°C equals 0V at A2's output. Circuit gain is set by A2's feedback values and linearity correction is derived from the output.

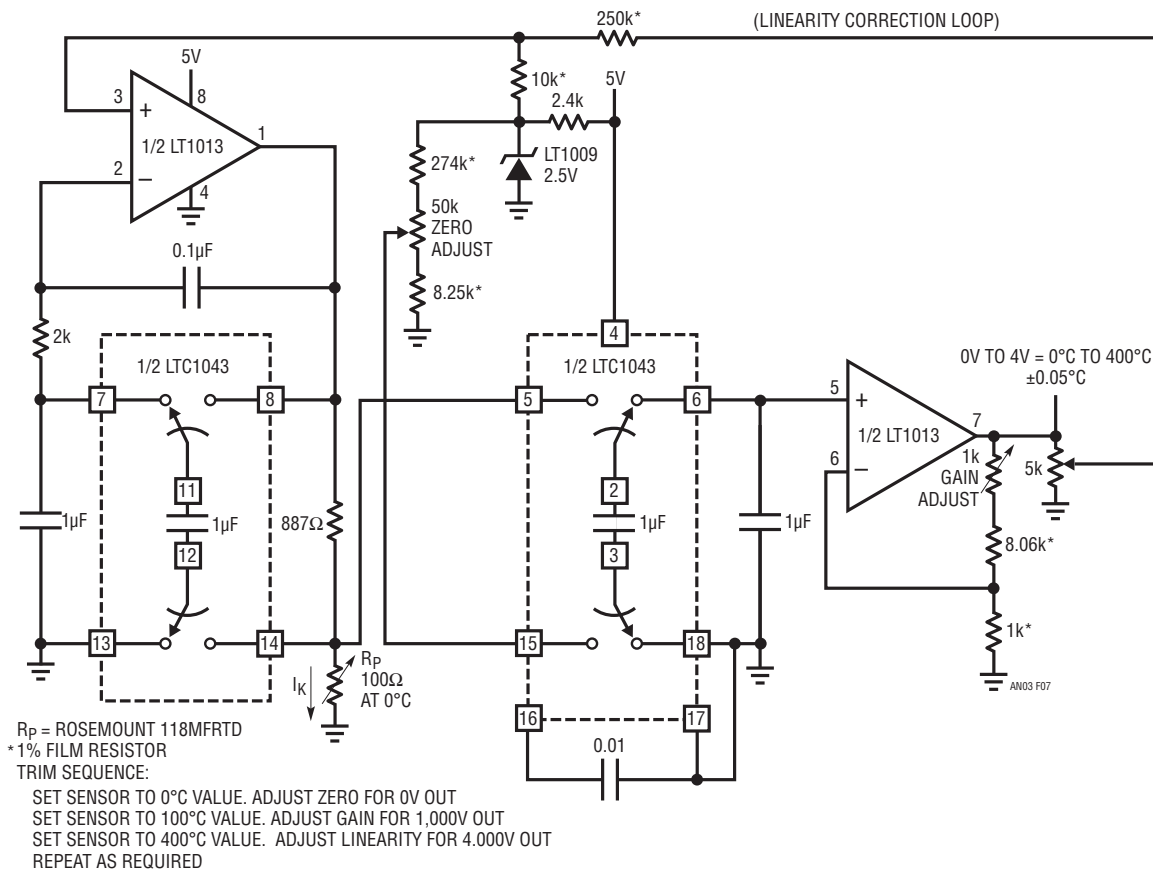


Figure 7. Linearized Platinum Signal Conditioner

Application Note 3

the average current into the summing point is determined by the sensor's humidity related value. The $1\mu\text{F}$ value AC couples the sensor to the charge-discharge path, maintaining the required zero average voltage across the device. The 22M resistor prevents accumulation of charge, which would stop current flow. The average current into A1's summing point is balanced by packets of charge delivered by the switched-capacitor network in A1's feedback loop. The $0.1\mu\text{F}$ capacitor gives A1 an integrator-like response, and its output is DC.

To allow 0% RH to equal 0V, offsetting is required. The signal and feedback terms biasing the summing point are expressed in charge form. Because of this, the offset must also be delivered to the summing point as charge, instead of a simple DC current. If this is not done, the circuit will be affected by frequency drift of LTC1034B's oscillator. Section 8B-11B-7B serves this function, delivering LT1009-referenced offsetting charge to A1.

Drift terms in this circuit include the LT1009 and the ratio stability of the sensor and the 100pF capacitors. These terms are well within the sensor's 2% accuracy specification and temperature compensation is not required. To calibrate this circuit, place the sensor in a known 5% RH environment and adjust the "5% RH trim" for 0.05V output. Next, place the sensor in a 90% RH environment and set the "90% RH trim" for 900mV output. Repeat this procedure until both points are fixed. Once calibrated, this circuit is accurate within 2% in the 5% to 90% RH range.

Figure 9 shows an alternate circuit which requires two op amps but needs only one LTC1043 package. This circuit retains insensitivity to clock frequency while permitting a DC offset trim. This is accomplished by summing in the offset current after A1.

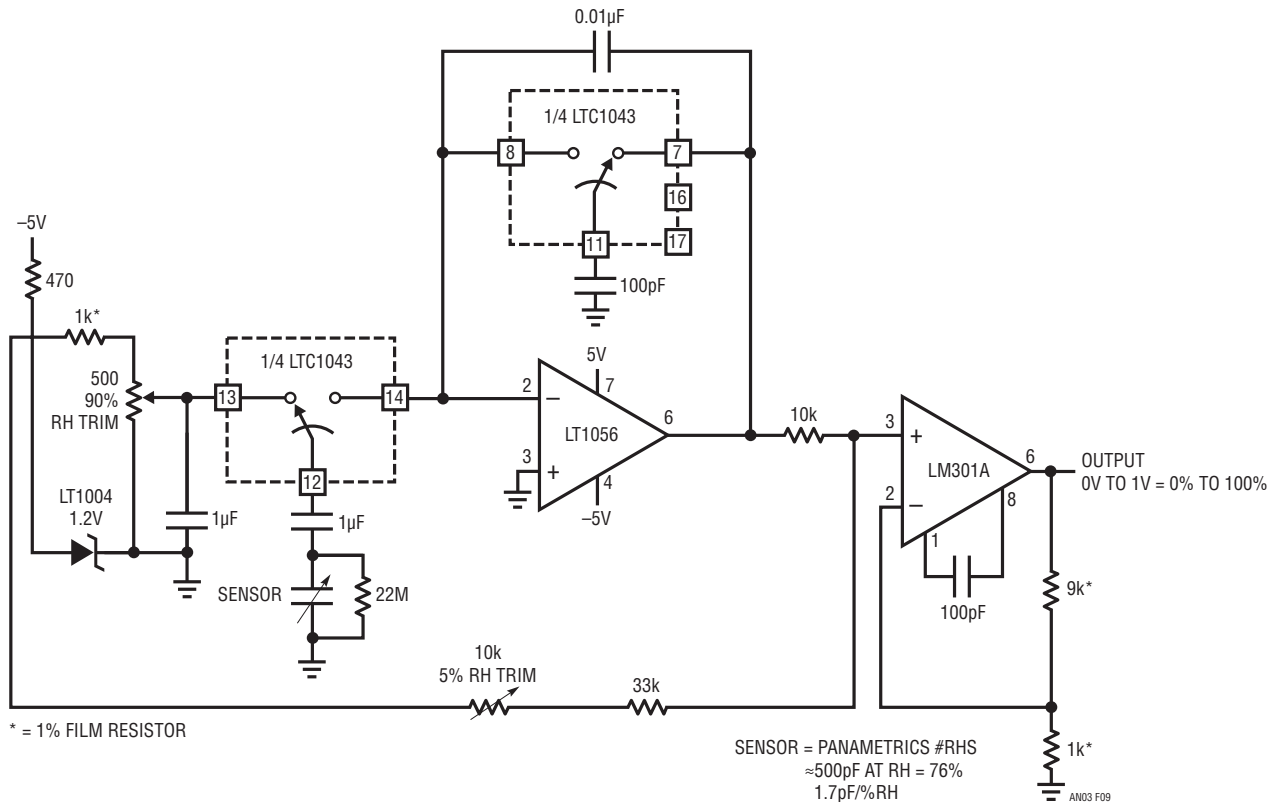


Figure 9. Relative Humidity Signal Conditioner

LVDT Signal Conditioner

LVDTs (linear variable differential transformers) are another example of a transducer which the LTC1043 can signal condition. An LVDT is a transformer with a mechanically actuated core. The primary is driven by a sine wave, usually amplitude stabilized. Sine drive eliminates error inducing harmonics in the transformer. The two secondaries are connected in opposed phase. When the core is positioned in the magnetic center of the transformer, the secondary outputs cancel and there is no output. Moving the core away from the center position unbalances the flux ratio between the secondaries, developing an output. Figure 10

shows an LTC1043 based LVDT signal conditioner. A1 and its associated components furnish the amplitude stable sine wave source. A1's positive feedback path is a Wein bridge, tuned for 1.5kHz. Q1, the LT1004 reference, and additional components in A1's negative loop unity-gain stabilize the amplifier. A1's output (Trace A, Figure 11), an amplitude stable sine wave, drives the LVDT. C1 detects zero crossings and feeds the LTC1043 clock pin (Trace B). A speed-up network at C1's input compensates LVDT phase shift, synchronizing the LTC1043's clock to the transformer's output zero crossings. The LTC1043 alternately connects each end of the transformer to ground,

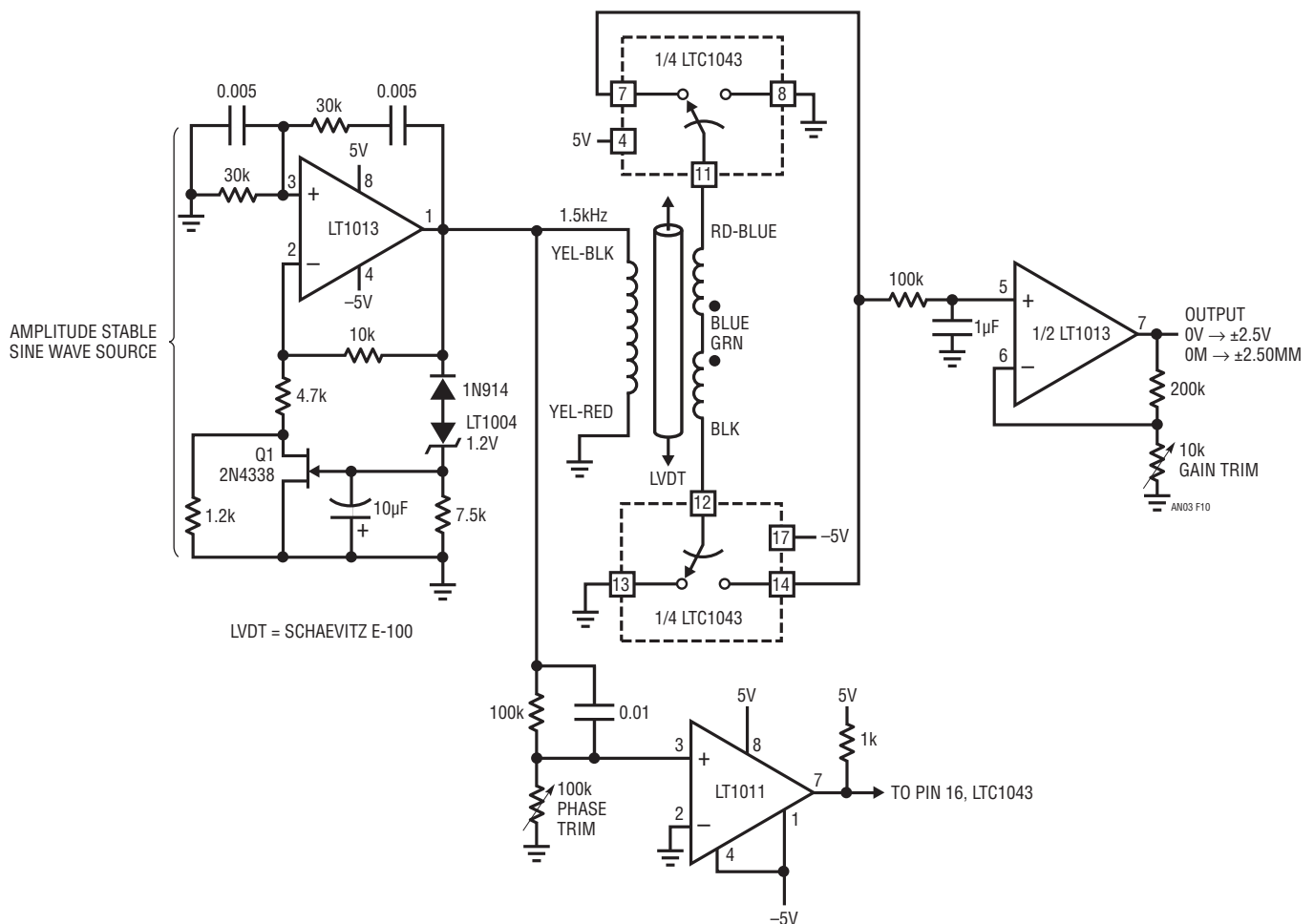


Figure 10. LVDT Signal Conditioner

Application Note 3

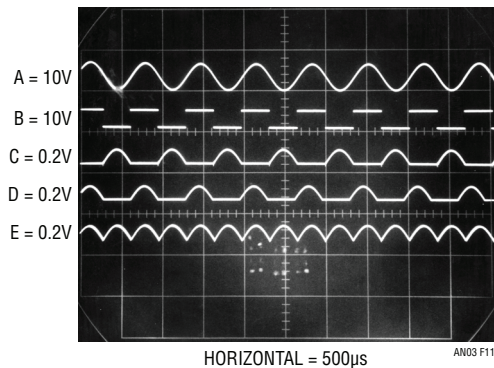


Figure 11

resulting in positive half-wave rectification at Pins 7 and 14 (Traces C and D, respectively). These points are summed (Trace E) at a lowpass filter which feeds A2. A2 furnishes gain scaling and the circuit's output.

The LTC1043's synchronized clocking means the information presented to the lowpass filter is amplitude and phase sensitive. The circuit output indicates how far the core is from center and on which side.

To calibrate this circuit, center the LVDT core in the transformer and adjust the phase trim for 0V output. Next, move the core to either extreme position and set the gain trim for 2.50V output.

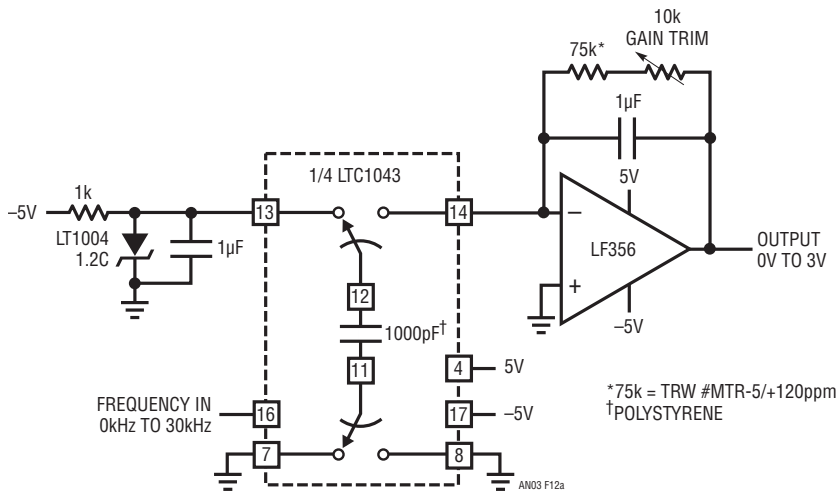
Charge Pump $F \rightarrow V$ and $V \rightarrow F$ Converters

Figure 12 shows two related circuits, both of which show how the LTC1043 can simplify a precision circuit function. Charge pump $F \rightarrow V$ and $V \rightarrow F$ converters usually require substantial compensation for non-ideal charge gating behavior. These examples equal the performance of such circuits, while requiring no compensations. These circuits are economical, component count is low, and the 0.005% transfer linearity equals that of more complex designs. Figure 12A is an $F \rightarrow V$ converter. The LTC1043's clock pin is driven from the input (Trace A, Figure 13). With the input high, Pins 12 and 13 are shorted and 14 is open. The 1000pF capacitor receives charge from the 1 μ F unit, which is biased by the LT1004. At the input's negative-going edge, Pins 12 and 13 open and 12 and 14 close. The 1000pF capacitor quickly removes current (Trace B) from A1's summing node. Initially, current is transferred through A1's feedback capacitor and the amplifier output

goes negative (Trace C). When A1 recovers, it slews positive to a level which resets the summing junction to zero. A1's 1 μ F feedback capacitor averages this action over many cycles and the circuit output is a DC level linearly related to frequency. A1's feedback resistors set the circuit's DC gain. To trim the circuit, apply 30kHz in and set the 10k Ω gain trim for exactly 3V output. The primary drift term in this circuit is the 120ppm/ $^{\circ}$ C tempco of the 1000pF capacitor, which should be polystyrene. This can be reduced to within 20ppm/ $^{\circ}$ C by using a feedback resistor with an opposing tempco (e.g., TRW #MTR-5/+120ppm). The input pulse width must be low for at least 100ns to allow complete discharge of the 1000pF capacitor.

In Figure 12B, the LTC1043 based charge pump is placed in A1's feedback loop, resulting in a $V \rightarrow F$ converter. The clock pin is driven from A1's output. Assume that A1's negative input is just below 0V. The amplifier output is positive. Under these conditions, LTC1043's Pins 12 and 13 are shorted and 14 is open, allowing the 0.01 μ F capacitor to charge toward the negative 1.2V LT1004. When the input-voltage-derived current forces A1's summing point (Trace A, Figure 13) positive, its output (Trace B) goes negative. This reverses the LTC1043's switch states, connecting Pins 12 and 14. Current flows from the summing point into the 0.01 μ F capacitor (Trace C). The 30pF-22k combination at A1's positive input (Trace D) ensures A1 will remain low long enough for the 0.01 μ F capacitor to completely reset to zero. When the 30pF-22k positive feedback path decays, A1's output returns positive and the entire cycle repeats. The oscillation frequency of this action is directly related to the input voltage with a transfer linearity of 0.005%.

Start-up or overdrive conditions could force A1 to go to the negative rail and stay there. Q1 prevents this by pulling the summing point negative if A1's output stays low long enough to charge the 1 μ F-330k RC. Two LTC1043 switch sections provide complementary sink-source outputs. Similar to the $F \rightarrow V$ circuit, the 0.01 μ F capacitor is the primary drift term, and the resistor type noted above will provide optimum tempco cancellation. To calibrate this circuit, apply 3V and adjust the gain trim for a 30kHz output.



12a. Frequency-to-Voltage Converter

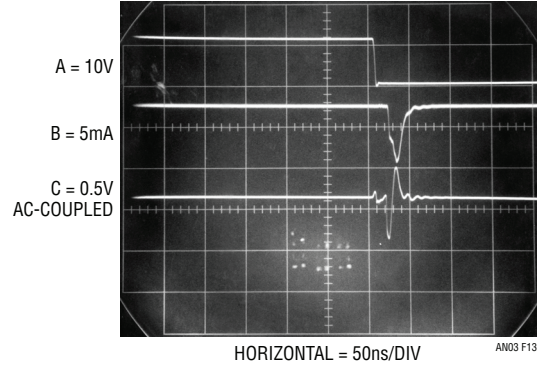
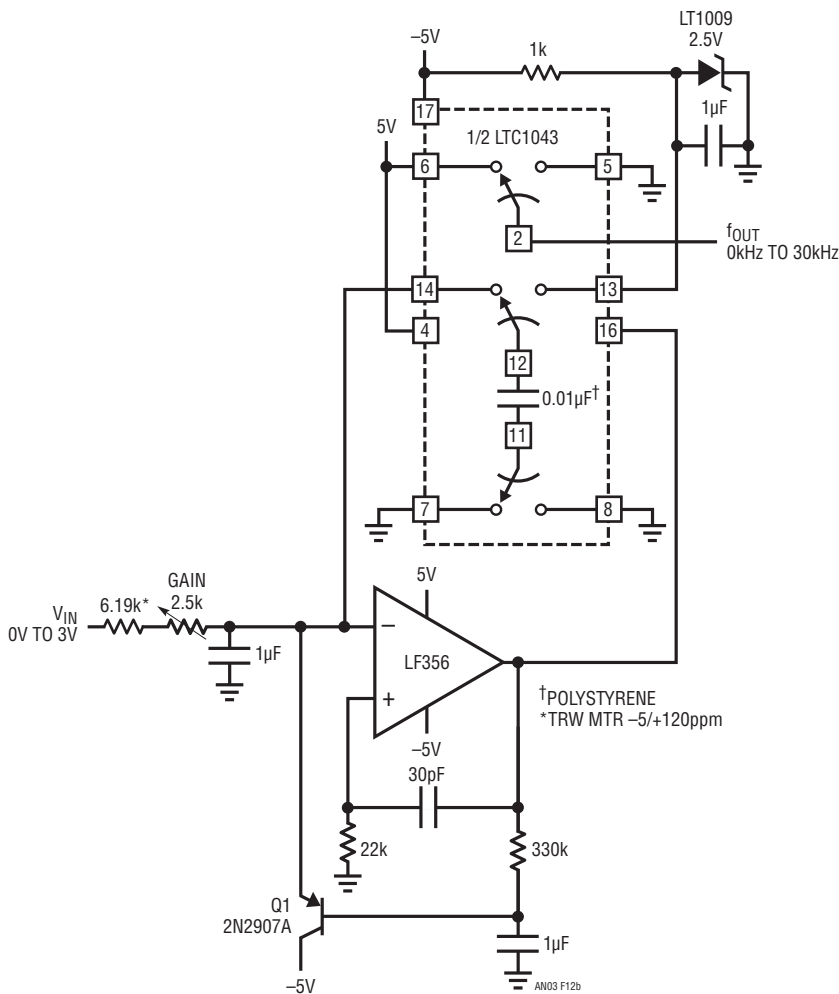


Figure 13



12b. Voltage-to-Frequency Converter

Figure 12

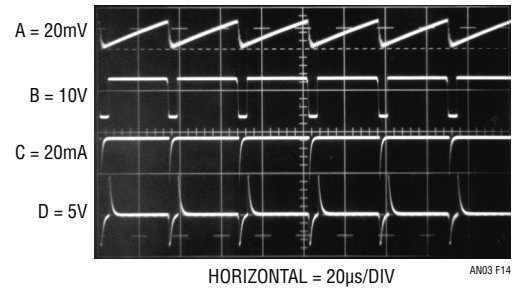


Figure 14

Application Note 3

12-Bit A→D Converter

Figure 15 shows the LTC1043 used to implement an economical 12-bit A→D converter. The circuit is self-clocking, has a serial output, and completes a full-scale conversion in 25ms.

Two LTC1043s are used in this design. Unit A free-runs, alternately charging the 100pF capacitor from the LT1004

reference source and then dumping it into A1's summing point. A1, connected as an integrator, responds with a linear ramp output (Trace B, Figure 16). This ramp is compared to the input voltage by C1B. When the crossing occurs, C1B's output goes low (Trace C, just faintly visible in the photograph), setting the flip-flop high (Trace D). This pulls LTC1043's Pin 16 high, resetting A1's integrator capacitor via the paralleled switches. Simultaneously, Pin 14B opens,

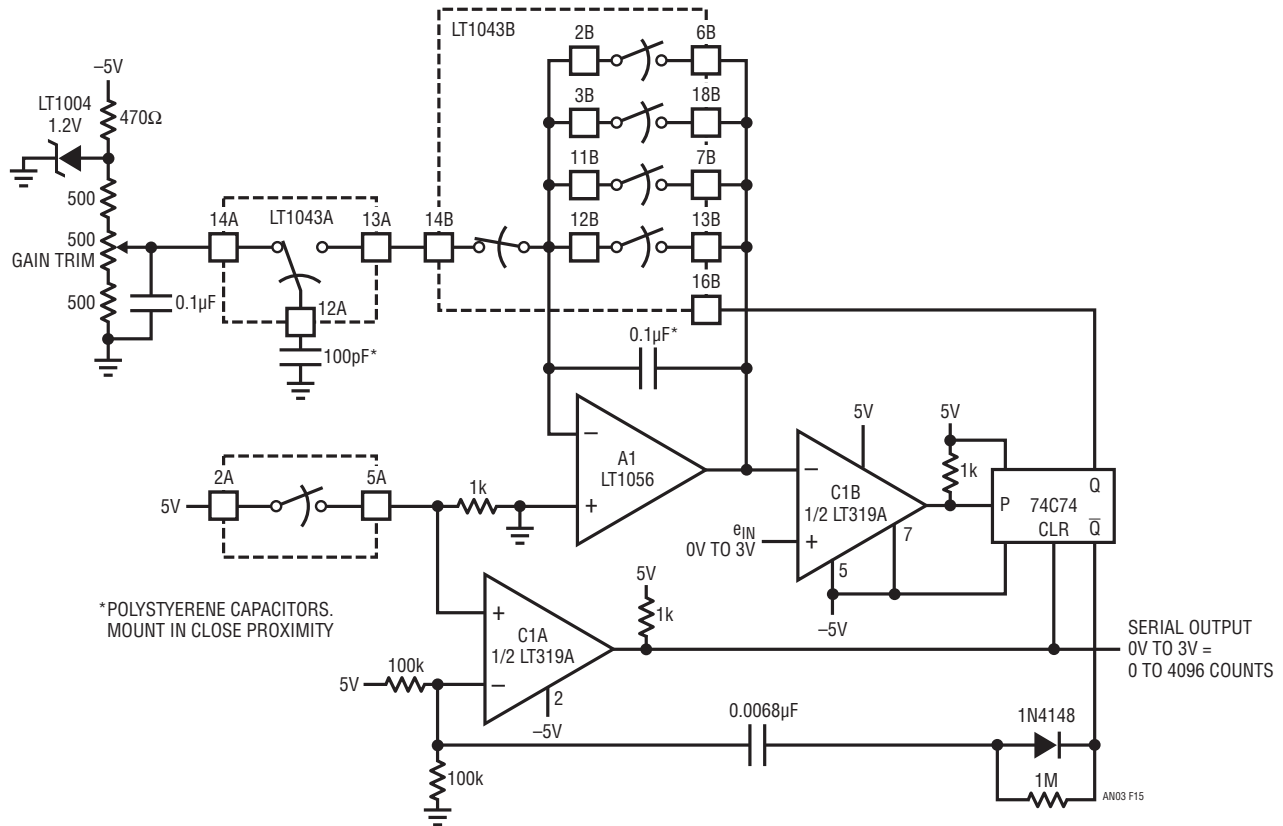


Figure 15. 12-Bit A→D Converter

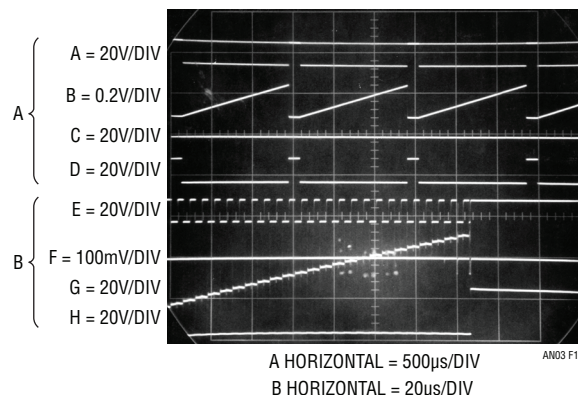


Figure 16

preventing charge from being delivered to A1's summing point during the reset. The flip-flop's Q output, low during this interval, causes an AC negative-going spike at C1A. This forces C1A's output high, inserting a gap in the output clock pulse stream (Trace A). The width of this gap, set by the components at C1A's negative input, is sufficient to allow a complete reset of A1's integrating capacitor. The number of pulses between gaps is directly related to the input voltage. The actual conversion begins at the gap's negative edge and ends at its positive edge. The flip-flop output may be used for resetting. Alternately, a processor driven "time-out" routine can determine the end of conversion. Traces E through H offer expanded scale versions of Traces A through D, respectively. The staircase detail of A1's ramp output reflects the charge pumping action at its summing point. Note that drift in the 100pF and 0.1µF capacitors, which should be polystyrene, ratiometrically cancels. Full-scale drift for this circuit is typically 20ppm/°C, allowing it to hold 12-bit accuracy over 25°C + 10°C. To calibrate the circuit, apply 3V in and trim the gain potentiometer for 4096 pulses out between data stream gaps.

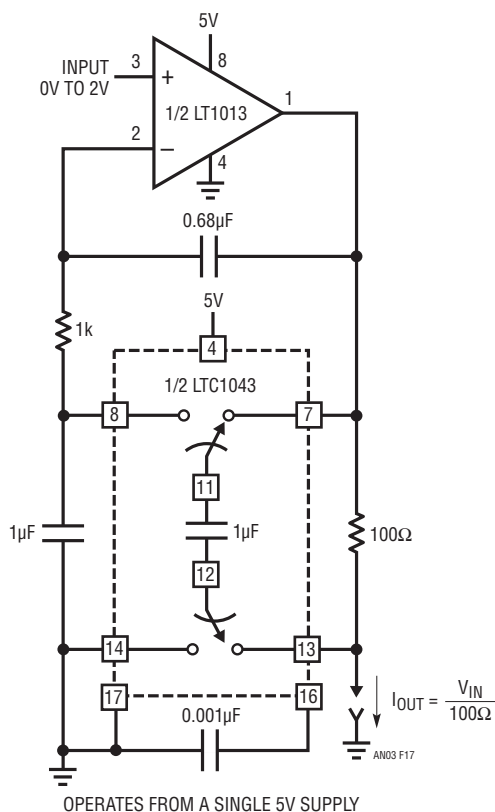


Figure 17. Voltage Controlled Current Source with Ground Referred Input and Output

Miscellaneous Circuits

Figures 17 to 22 show a group of miscellaneous circuits, most of which are derivations of applications covered in the text. As such, only brief comments are provided.

Voltage-Controlled Current Source—Grounded Source and Load

This is a simple, precise voltage-controlled current source. Bipolar supplies will permit bipolar output. Configurations featuring a grounded voltage control source and a grounded load are usually more complex and depend upon several components for stability. In this circuit, accuracy and stability are almost entirely dependent on the 100Ω shunt.

Current Sensing in Supply Rails

The LTC1043 can sense current through a shunt in either of its supply rails (Figure 18). This capability has wide application in battery and solar-powered systems. If the ground-referred voltage output is unloaded by an amplifier, the shunt can operate with very little voltage drop across it, minimizing losses.

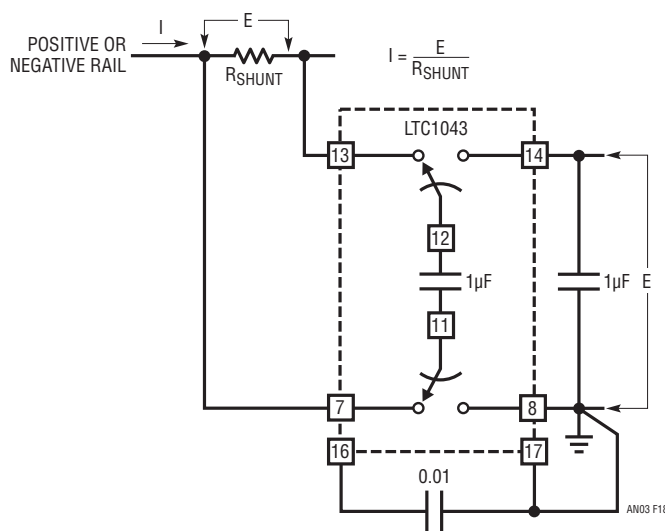


Figure 18. Precision Current Sensing in Supply Rails

Application Note 3

0.01% Analog Multiplier

Figure 19, using the $V \rightarrow F$ and $F \rightarrow V$ circuits previously described, forms a high precision analog multiplier. The $F \rightarrow V$ input frequency is locked to the $V \rightarrow F$ output because the LTC1043's clock is common to both sections. The $F \rightarrow V$ reference is used as one input of the multiplier, while the $V \rightarrow F$ furnishes the other. To calibrate, short the X and Y inputs to 1.7320V and trim for a 3V output.

Inverting a Reference

Figure 20 allows a reference to be inverted with 1ppm accuracy. This circuit features high input impedance and requires no trimming.

Low Power, 5V Driven, Temperature Compensated Crystal Oscillator

Figure 21 uses the LTC1043 to differentiate between a temperature sensing network and a DC reference. The single-ended output biases a varactor-tuned crystal oscillator to compensate drift. The varactor-crystal network has high DC impedance, eliminating the need for an LTC1043 output amplifier.

Simple Thermometer

Figure 22's circuit is conceptually similar to the platinum RTD example of Figure 7. The thermistor network specified eliminates the requirement for a linearity trim, at the expense of accuracy and range of operation.

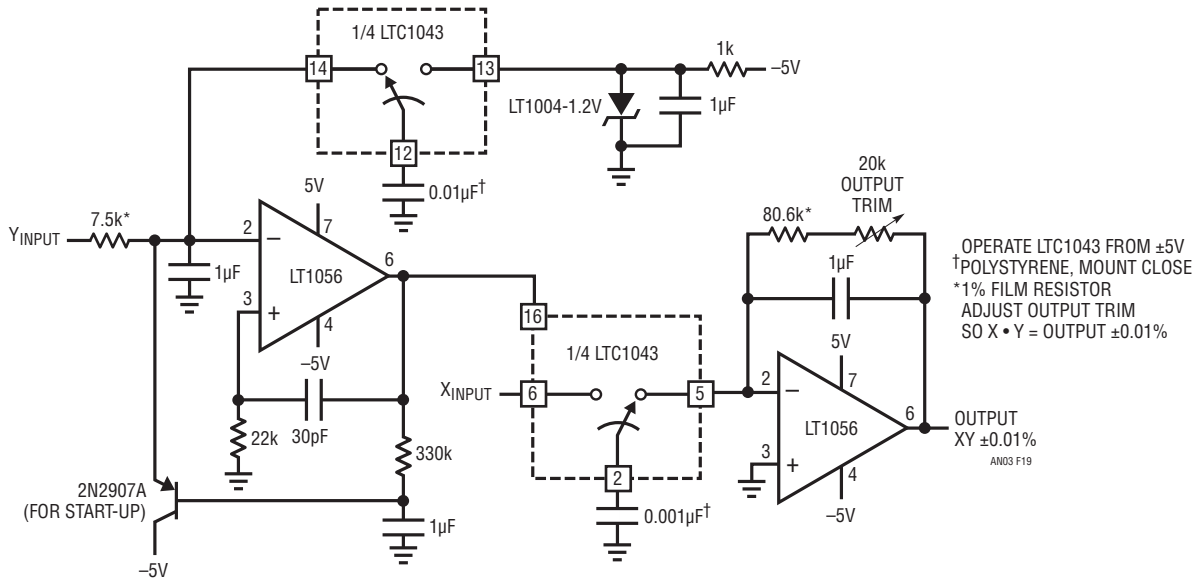


Figure 19. Analog Multiplier with 0.01% Accuracy

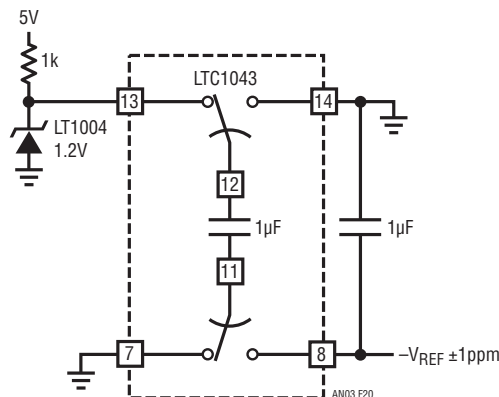


Figure 20. Precision Voltage Inverter

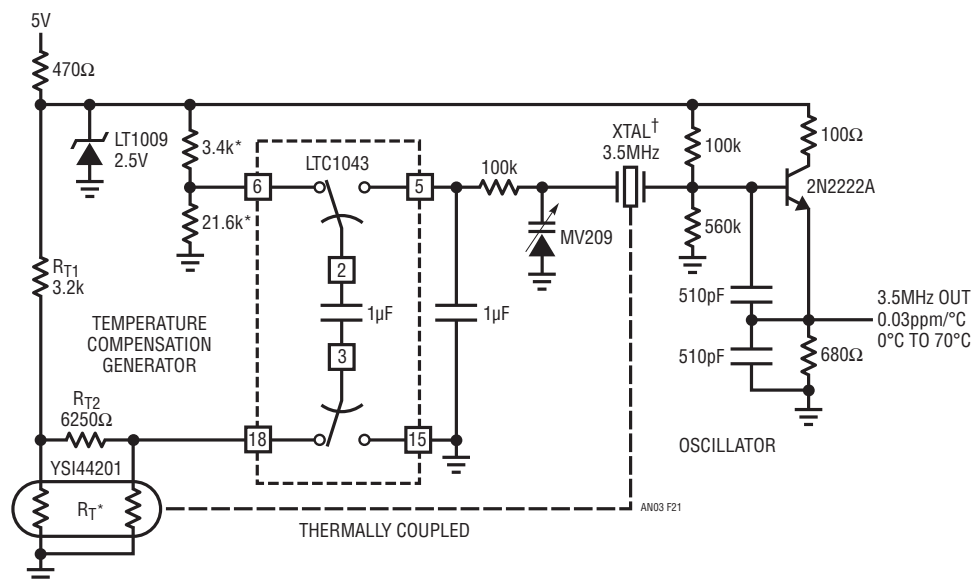


Figure 21. Temperature Compensated Crystal Oscillator

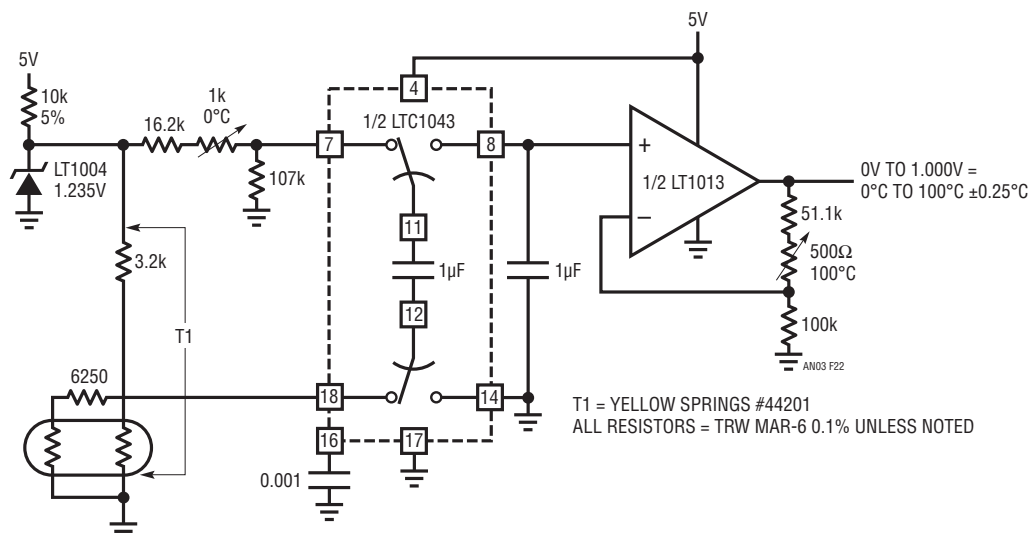


Figure 22. Linear Thermometer

High Current, “Inductorless,” Switching Regulator

Figure 23 shows a high efficiency battery driven regulator with a 1A output capacity. Additionally, it does not require an inductor, an unusual feature for a switching regulator operating at this current level.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the 12V battery’s current flows

through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 24, are the LTC1043-supplied drives to Q3 and Q4, respectively. Q1 and Q2 receive similar drive from Pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one-half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the

Application Note 3

output (Trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043 oscillator pin (Trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF capacitor

provides sharp transitions. The loop regulates the output to 5V by feedback controlling the turn-off point of the series MOSFET. The circuit constitutes a large-scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

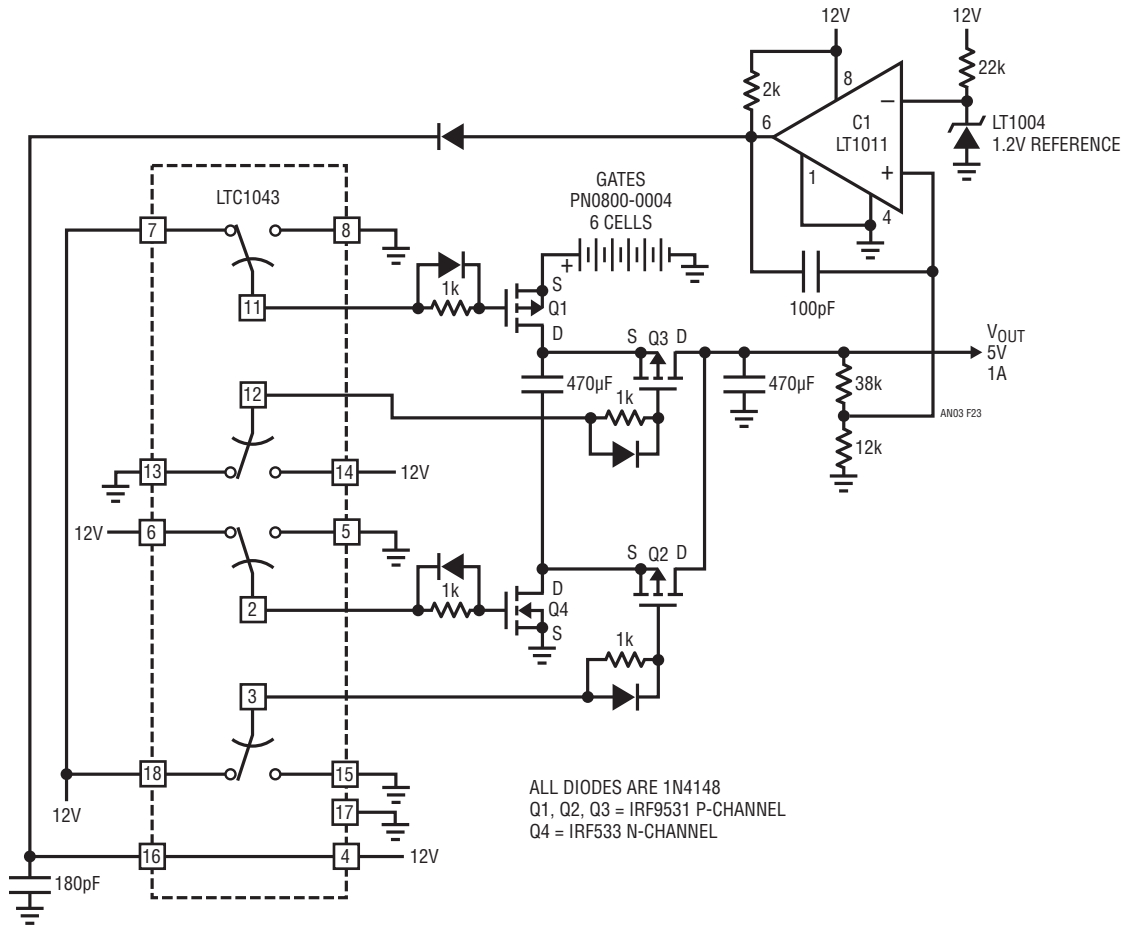


Figure 23. Inductorless Switching Regulator

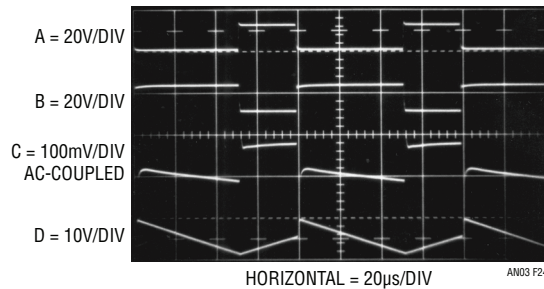


Figure 24

Applications for a New Power Buffer

Jim Williams

A frequent requirement in systems involves driving analog signals into non-linear or reactive loads. Cables, transformers, actuators, motors and sample-and-hold circuits are examples where the ability to drive difficult loads is required. Although several power buffer amplifiers are available, none have been optimized for driving difficult loads. The LT[®]1010 can isolate and drive almost any reactive load. It also offers current limiting and thermal overload protection which protect the device against output fault conditions. The combination of good speed, output protection, and reactive load driving capability (see box section, "The LT1010 at a Glance") make the device useful in a variety of practical situations.

Buffered Output Line Driver

Figure 1 shows the LT1010 placed within the feedback loop of an operational amplifier. At lower frequencies, the buffer is within the feedback loop and its offset voltage and gain error are negligible. At higher frequencies, feedback is through C_F so that phase shift from load capacitance acting against the buffer's output resistance does not cause loop instability.

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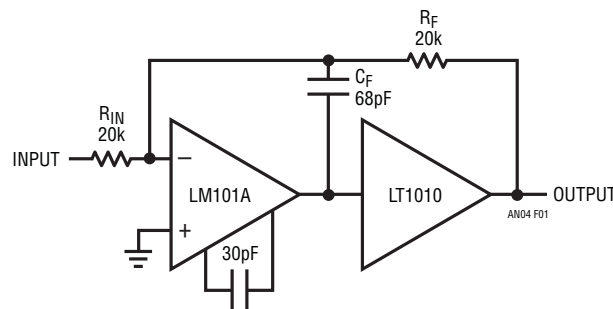


Figure 1. Practical LT1010 Based Boosted Op Amp

Application Note 4

Figure 2 shows this configuration driving a 50Ω - $0.33\mu\text{F}$ load. The waveform is clean, with controlled damping. With C load increased to a brutal $2\mu\text{F}$, the circuit is still stable (Trace A, Figure 3), even though the large capacitance requires substantial current (Trace B) from the LT1010. Adjustment of the R_F - C_F time constant would allow improved damping.

Although this circuit is useful, its speed is limited by the op amp.

Fast, Stabilized Buffer Amplifier

Figure 4 shows a way to eliminate this restriction, while maintaining good DC characteristics. Here, the LT1010 is combined with a wideband gain stage, Q1-Q3, to form a fast inverting configuration. The LT1008 op amp DC stabilizes this stage by biasing the Q2-Q3 emitters to force a zero DC potential at the circuit's summing junction. The roll-offs of the fast stage and the op amp are arranged to provide smooth overall circuit response.

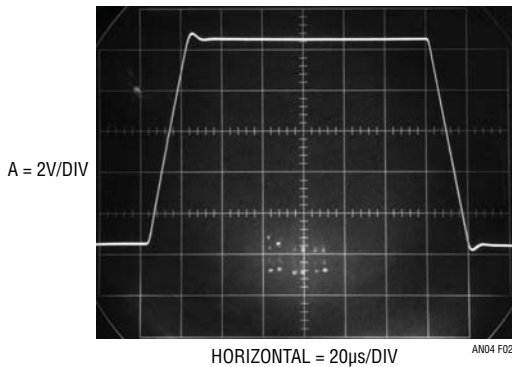


Figure 2

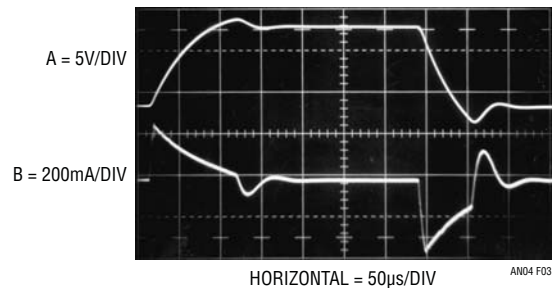


Figure 3

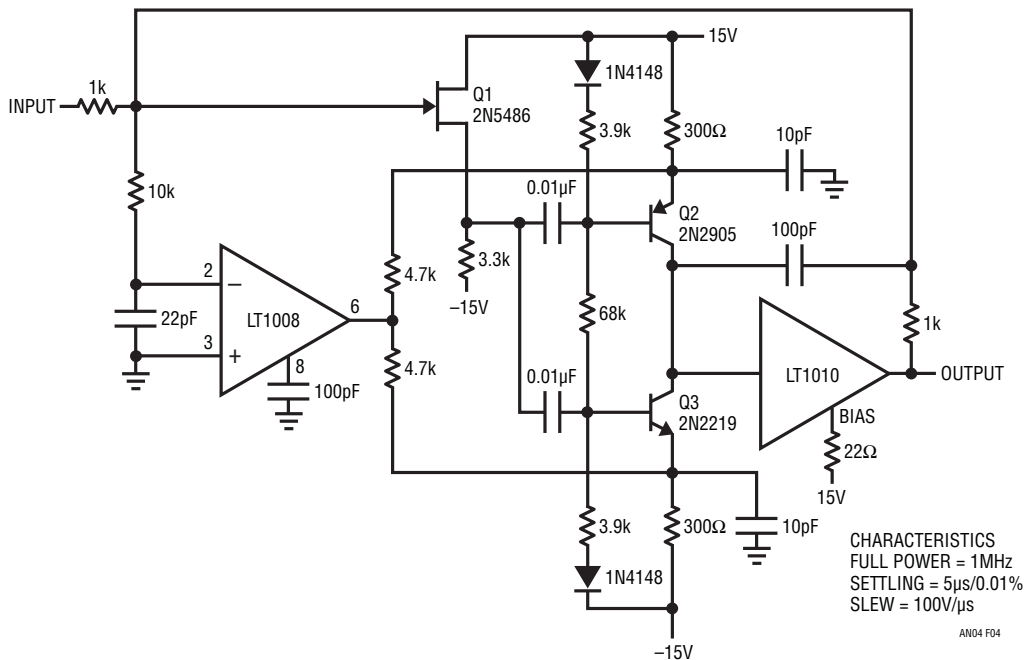


Figure 4. Fed Forward, Wideband DC-Stabilized Buffer

Because the circuit's DC stabilization path occurs in parallel with the buffer, higher speed is obtainable. Figure 5 shows the circuit driving a 600Ω - 2500pF load. Despite the heavy load, the output (Trace B) does a good job of following the input (Trace A) at a gain of -1 .

Video Line Driving Amplifier

In many applications, DC stability is unimportant and AC gain is required. Figure 6 shows how to combine the LT1010's load handling capability with a fast, discrete gain stage. Q1 and Q2 form a differential stage which single

ends into the LT1010. The capacitively terminated feedback divider gives the circuit a DC gain of 1, while allowing AC gains up to 10. Using a 20Ω bias resistor (see box section), the circuit delivers $1\text{V}_{\text{P-P}}$ into a typical 75Ω video load. For applications sensitive to NTSC requirements, dropping the bias resistor value will aid performance.

At $A = 2$, the gain is within 0.5dB to 10MHz with the -3dB point occurring at 16MHz . At $A = 10$, the gain is flat ($\pm 0.5\text{dB}$ to 4MHz) with a -3dB point at 8MHz . The peaking adjustment should be optimized under loaded output conditions.

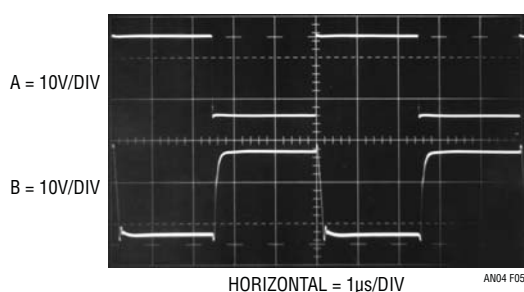


Figure 5

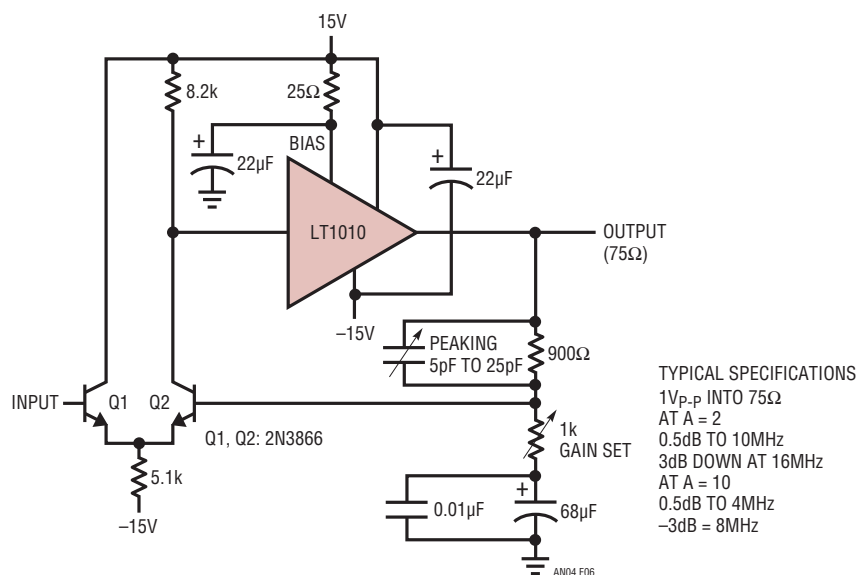


Figure 6. Video Line Driving Amplifier

Application Note 4

Figure 7 shows a video distribution amplifier. In this example, resistors are included in the output line to isolate reflections from unterminated lines. If the line characteristics are known, the resistors may be deleted. To meet NTSC gain-phase requirements, a small value boost resistor is used. Each $1V_{p-p}$ channel output is essentially flat through 6MHz into a 75Ω load.

Fast, Precision Sample-Hold Circuit

Sample-hold circuits require high capacitive load driving capability to achieve fast acquisition times. Additionally, other trade-offs must be considered to achieve a good design. The conceptual circuit of Figure 8 illustrates some of the issues encountered. Fast acquisition requires high charge currents and dynamic stability, which the LT1010 can

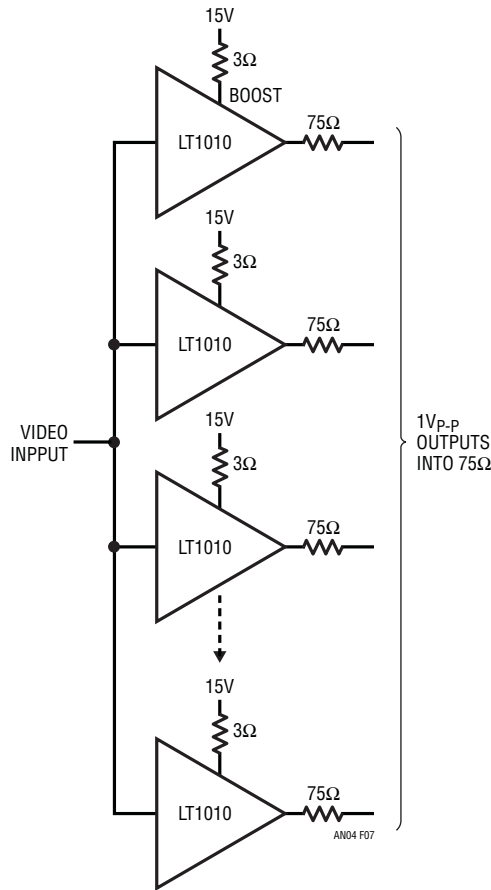


Figure 7. Video Distribution Amplifier

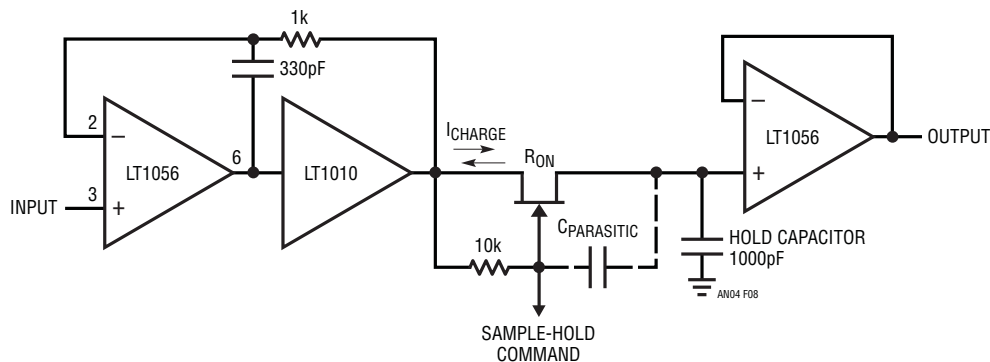


Figure 8. Conceptual Sample-Hold

an4f

Application Note 4

potentiometer—15pF network in Q5's emitter. The amount of charge is scaled to compensate for charge removal due to Q6's parasitic term. A3's inverting input is biased so that negative supply shifts, which alter the charge removed through C parasitic, are accounted for in the compensating charge. Compensation is set by grounding the signal input, clocking the S-H line and adjusting the potentiometer for minimum disturbance at the circuit's output.

Figure 10 shows the circuit at work. When the sample-hold input (Trace A, Figure 10) goes into hold, charge cancellation occurs and the output (Trace B) sees less than 250µV of hold step error within 100ns. Without compensation, the error would be 50mV (Trace B, Figure 11—Trace A is the sample-hold input).

Figure 12 shows the LT1010's contribution to fast acquisition. The circuit acquires a 10V signal in this photograph. Trace A is the sample-hold input. Trace B shows the LT1010 delivering over 100mA to the hold capacitor and Trace C depicts the output value slewing and settling to final value. Note that the acquisition time is limited by

amplifier settling time and not capacitor charge time. Pertinent specifications include:

Acquisition time: 2µs to 0.01%

Hold settling time: <100ns to 1mV

Aperture time: 16ns

Motor Speed Control

The LT1010's ability to drive difficult loads is exploited in Figure 13's circuit. Here, the buffer drives a motor-tachometer combination. The tachometer signal is fed back and compared to a reference current and the LM301A amplifier closes a control loop. The 0.47µF capacitor provides stable compensation. Because the tachometer output is bipolar, the speed is controllable in both directions, with clean transitions through zero. The LT1010's thermal protection is particularly useful in this application, preventing device destruction in the event of mechanical overload or malfunction.

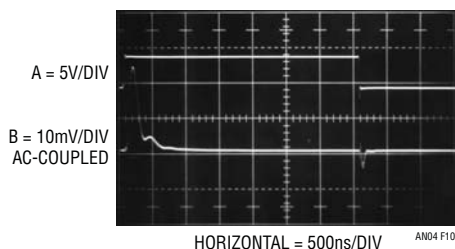


Figure 10

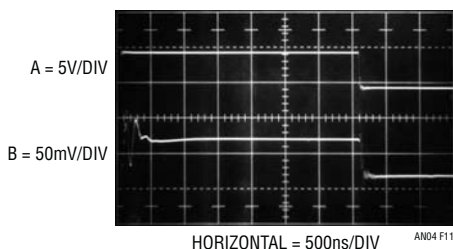


Figure 11

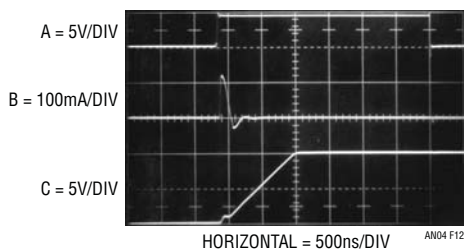


Figure 12

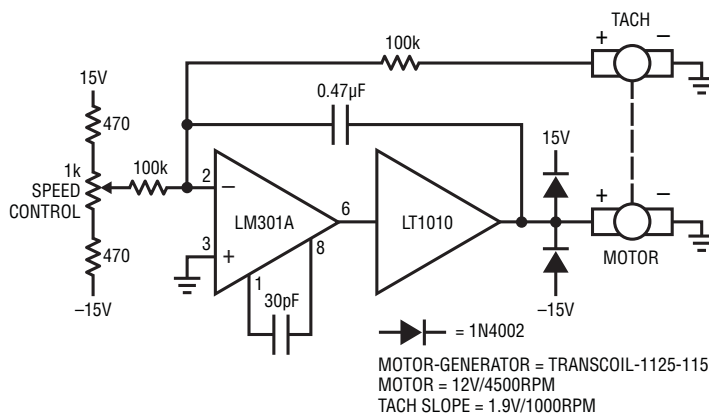


Figure 13. Overload Protected Motor Speed Controller

Fan-Based Temperature Controller

Figure 14 shows a way to use the LT1010 to control a fan motor's speed to regulate instrument temperature. The fan employed is one of the new electrostatic types which has very high reliability because it contains no wearing parts. These devices require high voltage drive. When power is applied, the thermistor (located in the fan's exhaust stream) is at a high value. This unbalances the A3 amplifier-driven bridge, A1 receives no power, and the fan does not run. As the instrument enclosure warms, the thermistor value

decreases until A3 begins to oscillate. A2 provides isolation and gain and A4 drives the transformer to generate high voltage for the fan. In this fashion, the loop acts to maintain a stable instrument temperature by controlling the fan's exhaust rate. The 100 μ F time constant across the error amplifier pins is typical of such configurations. Fast time constants will produce audibly annoying "hunting" in the servo. Optimal values for this time constant and gain depend upon the thermal and airflow characteristics of the enclosure being controlled.

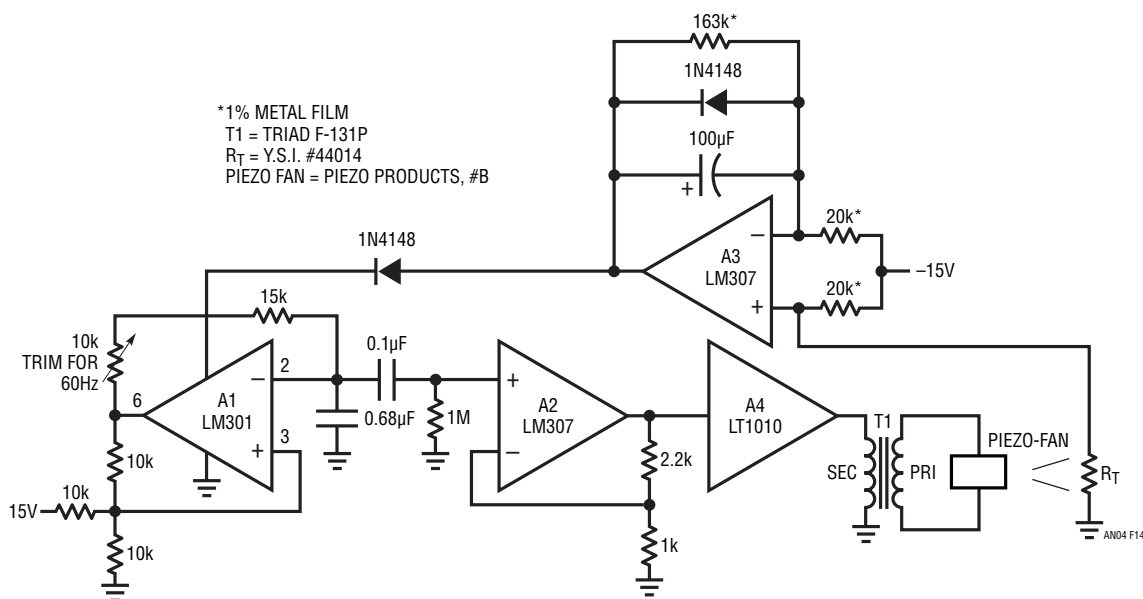


Figure 14. Piezo-Electric Fan Servo

The LT1010 at a Glance

by R. J. Widlar

The schematic describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower never drops below the quiescent value (determined by I and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower, even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading in the output lead.

The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal at V⁺, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single supply operation.

Application Note 4

The buffer is no more sensitive to supply bypassing than slower op amps as far as stability is concerned. The 0.1 μ F disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane are prudent, especially when operating at high frequencies.

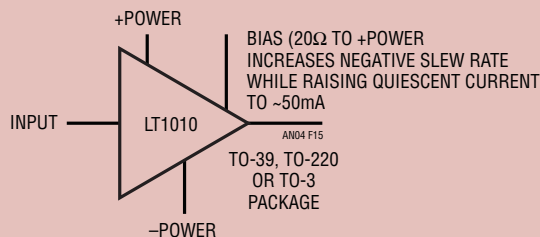
The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/ μ s, using 10 μ F solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp, causing stability problems with the overall loop. Adequate bypassing can usually be provided by 10 μ F solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air, is 150°C/W for the TO-39 package and 60°C/W for the TO-3 package. Circulating air, a heat sink or mounting the TO-3 package to a printed circuit board will reduce thermal resistance.

The LT1010 at a Glance



15MHz BANDWIDTH
100V/ μ s SLEW RATE
DRIVE \pm 10V INTO 75 Ω
5mA QUIESCENT CURRENT
DRIVE CAPACITIVE LOADS > 1 μ F
CURRENT/THERMAL LIMIT
4.5V \rightarrow 40V SUPPLY RANGE

In DC circuits, buffer dissipation is easily computed. In AC circuits, signal wave shape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

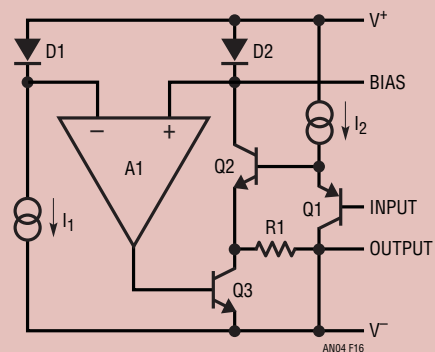
Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to ensure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Some low power op amps are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this can be done only on the TO-3 package.

The LT1010 Conceptual Schematic



Thermal Techniques in Measurement and Control Circuitry

Jim Williams

Designers spend much time combating thermal effects in circuitry. The close relationship between temperature and electronic devices is the source of more design headaches than any other consideration.

In fact, instead of eliminating or compensating for thermal parasitics in circuits, it is possible to utilize them. In particular, applying thermal techniques to measurement and control circuits allows novel solutions to difficult problems. The most obvious example is temperature control. Familiarity with thermal considerations in temperature control loops permits less obvious, but very useful, thermally-based circuits to be built.

Temperature Controller

Figure 1 shows a precision temperature controller for a small components oven. When power is applied, the thermistor, a negative TC device, is at a high value. A1 saturates positive. This forces the LT[®]3525A switching

regulator's output low, biasing Q1. As the heater warms, the thermistor's value decreases. When its inputs finally balance, A1 comes out of saturation and the LT3525A pulse width modulates the heater via Q1, completing a feedback path. A1 provides gain and the LT3523A furnishes high efficiency. The 2kHz pulse width modulated heater power is much faster than the thermal loop's response and the oven sees an even, continuous heat flow.

The key to high performance control is matching the gain bandwidth of A1 to the thermal feedback path. Theoretically, it is a simple matter to do this using conventional servo-feedback techniques. Practically, the long time constants and uncertain delays inherent in thermal systems present a challenge. The unfortunate relationship between servo systems and oscillators is very apparent in thermal control systems.

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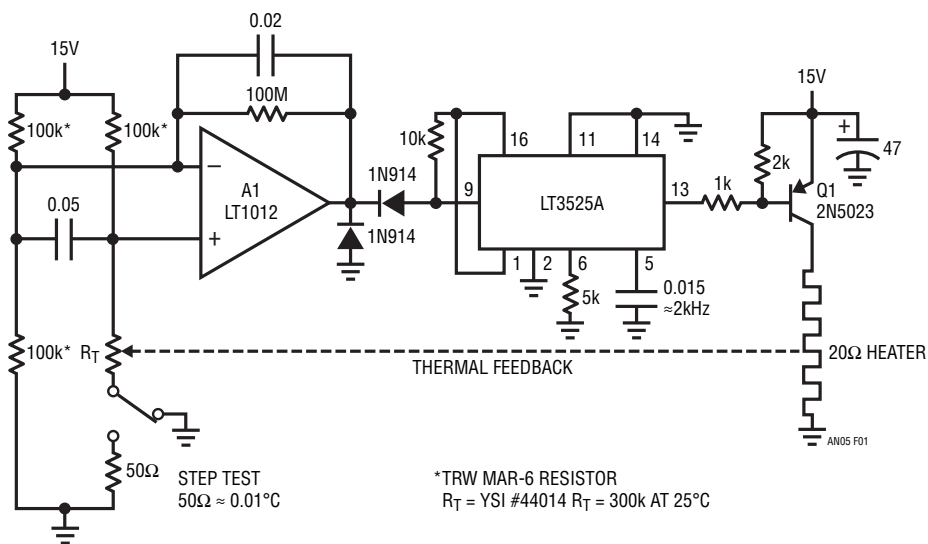


Figure 1. Precision Temperature Controller

Application Note 5

The thermal control loop can be very simply modeled as a network of resistors and capacitors. The resistors are equivalent to the thermal resistance and the capacitors equivalent to thermal capacity. In Figure 2 the heater, heater-sensor interface, and sensor all have RC factors that contribute to a lumped delay in the ability of a thermal system to respond. To prevent oscillation, A1's gain bandwidth must be limited to account for this delay. Since high gain bandwidth is desirable for good control, the delays must be minimized. The physical size and electrical resistivity of the heater selected give some element of control over the heater's time constant. The heater-sensor interface time constant can be minimized by placing the sensor in intimate contact with the heater.

The sensor's RC product can be minimized by selecting a sensor of small size relative to the capacity of its thermal environment. Clearly, if the wall of an oven is 6" thick aluminum, the tiniest sensor available is not an absolute

necessity. Conversely, if one is controlling the temperature of 1/16" thick glass microscope slide, a very small sensor (i.e., fast) is in order.

After the thermal time constants relating to the heater and sensor have been minimized, some form of insulation for the system must be chosen. The function of insulation is to keep the loss rate down so the temperature control device can keep up with the losses. For any given system, the higher the ratio between the heater-sensor time constants and the insulation time constants, the better the performance of the control loop.

After these thermal considerations have been attended to, the control loop's gain bandwidth can be optimized. Figures 3A, 3B and 3C show the effects of different compensation values at A1. Compensation is trimmed by applying small steps in temperature setpoint and observing the loop response at A1's output. The 50Ω resistor and

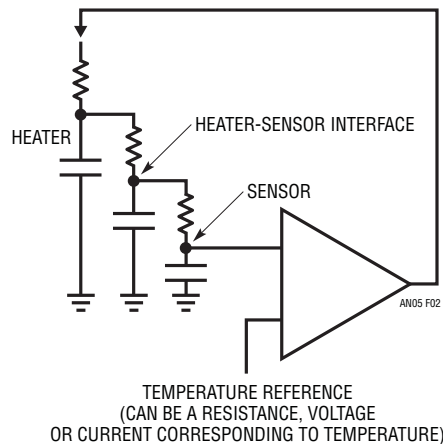


Figure 2. Thermal Control Loop Model

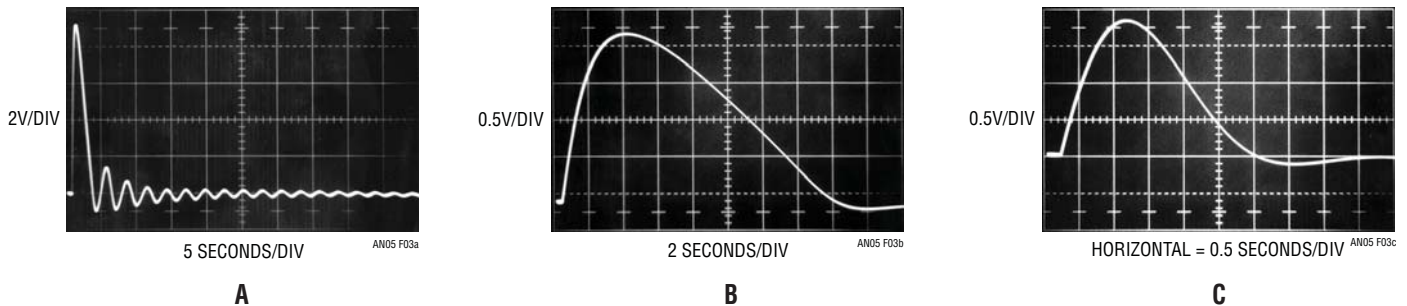


Figure 3. Loop Response for Various Gain Bandwidths

switch in the thermistor leg of the bridge furnish a 0.01°C step generator. Figure 3A shows the effects of too much gain bandwidth. The step change forces a damped, ringing response over 50 seconds in duration! The loop is marginally stable. Increasing A1's gain bandwidth (GBW) will force oscillation. Figure 3B shows what happens when GBW is reduced. Settling is much quicker and more controlled. The waveform is overdamped, indicating that higher GBW is achievable without stability compromises. Figure 3C shows the response for the compensation values given and is a nearly ideal critically damped recovery. Settling occurs within 4 seconds. An oven optimized in this fashion will easily attenuate external temperature shifts by a factor of thousands without overshoots or excessive lags.

Thermally Stabilized PIN Photodiode Signal Conditioner

PIN photodiodes are frequently employed in wide range photometric measurements. The photodiode specified in Figure 4 responds linearly to light intensity over a 100dB range. Digitizing the diode's linearly amplified output

would require an A/D converter with 17 bits of range. This requirement can be eliminated by logarithmically compressing the diode's output in the signal conditioning circuitry. Logarithmic amplifiers utilize the logarithmic relationship between V_{BE} and collector current in transistors. This characteristic is very temperature sensitive and requires special components and layout considerations to achieve good results. Figure 4's circuit logarithmically signal conditions the photodiode's output with no special components or layout.

A1 and Q4 convert the diode's photocurrent to a voltage output with a logarithmic transfer function. A2 provides offsetting and additional gain. A3 and its associated components form a temperature control loop which maintains Q4 at constant temperature (all transistors in this circuit are part of a CA3096 monolithic array). The 0.033μF value at A3's compensation pins gives good loop damping if the circuit is built using the array's transistors in the locations shown. These locations have been selected for optimal control at Q4, the logging transistor. Because of the array

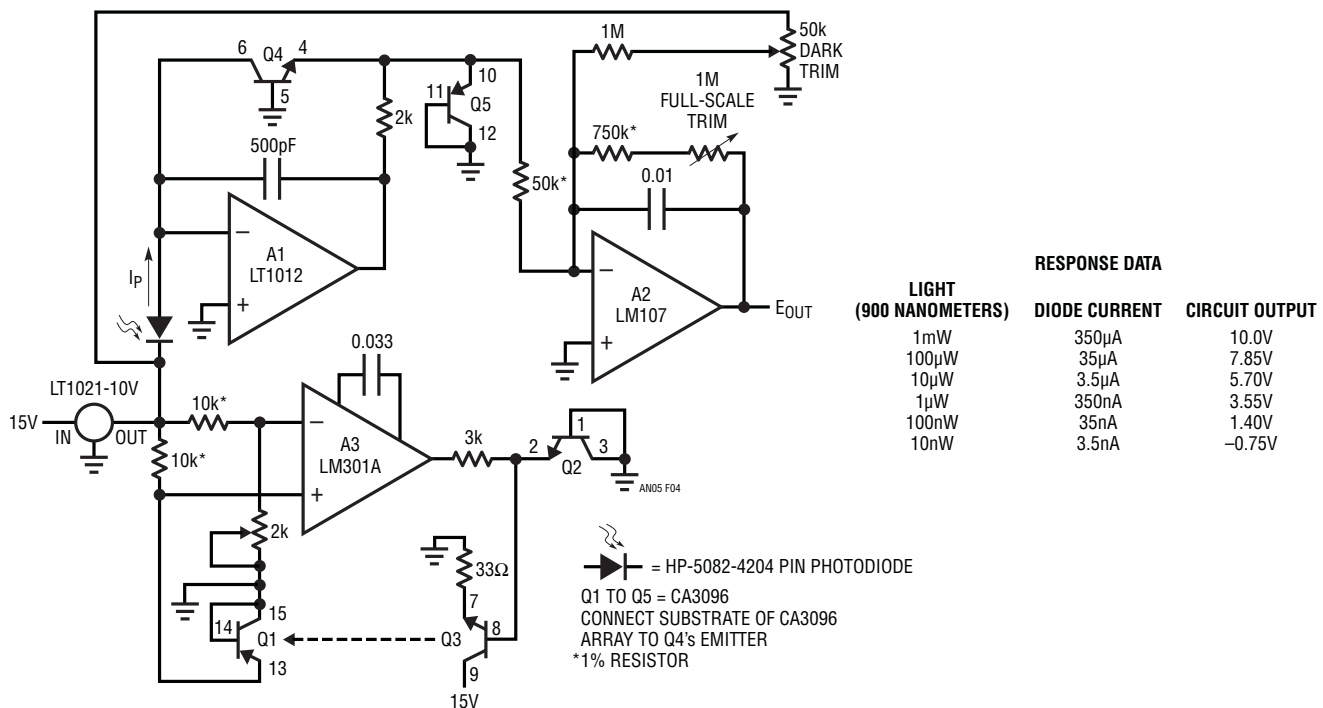


Figure 4. 100dB Range Logarithmic Photodiode Amplifier

Application Note 5

die's small size, response is quick and clean. A full-scale step requires only 250ms to settle (photo, Figure 5) to final value. To use this circuit, first set the thermal control loop. To do this, ground Q3's base and set the 2k pot so A3's negative input voltage is 55mV below its positive input. This places the servo's setpoint at about 50°C (25°C ambient + 2.2mV/°C • 25°C rise = 55mV = 50°C). Unground Q3's base and the array will come to temperature. Next, place the photodiode in a completely dark environment and adjust the "dark trim" so A2's output is 0V. Finally, apply or electrically simulate (see chart, Figure 4) 1mW of light and set the "full-scale" trim to 10V out. Once adjusted, this circuit responds logarithmically to light inputs from 10nW to 1mW with an accuracy limited by the diode's 1% error.

50MHz Bandwidth Thermal RMS→DC Converter

Conversion of AC waveforms to their equivalent DC power value is usually accomplished by either rectifying and averaging or using analog computing methods. Rectification averaging works only for sinusoidal inputs. Analog computing methods are limited to use below 500kHz. Above this frequency, accuracy degrades beyond the point of usefulness in instrumentation applications. Additionally, crest factors greater than 10 cause significant reading errors.

A way to achieve wide bandwidth and high crest factor performance is to measure the true power value of the waveform directly. The circuit of Figure 6 does this by measuring the DC heating power of the input waveform.

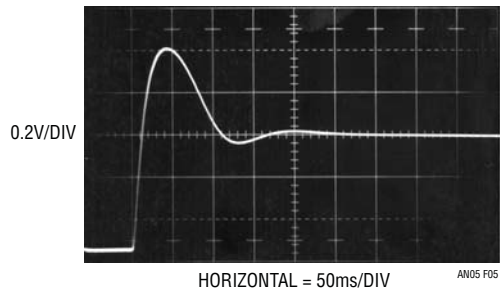


Figure 5. Figure 4's Thermal Loop Response

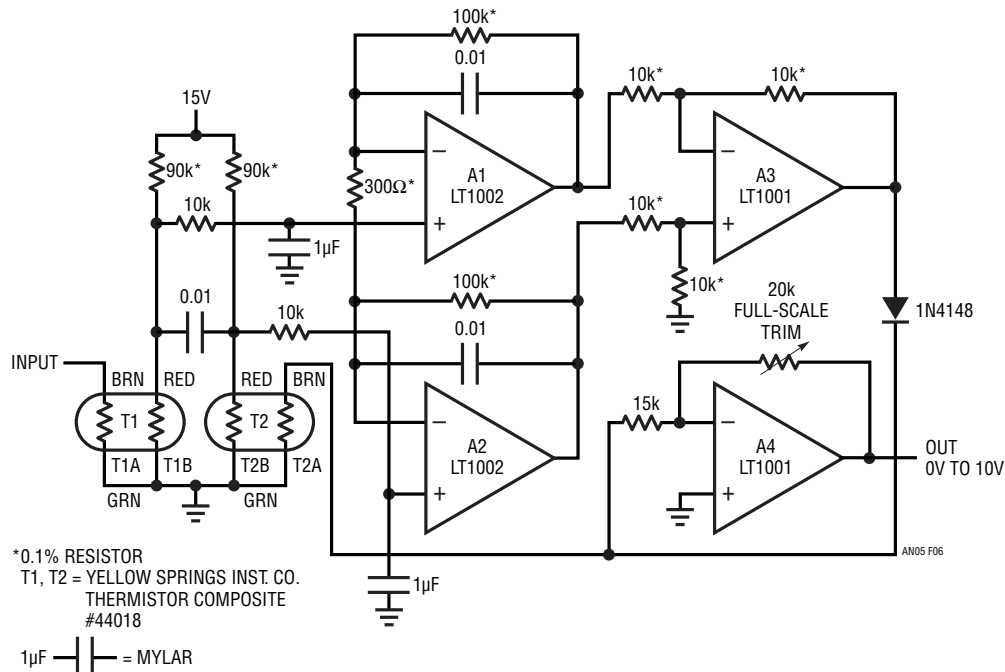


Figure 6. 50MHz Thermal RMS→DC Converter

By using thermal techniques to integrate the input waveform, 50MHz bandwidth is easily achieved with 2% accuracy. Additionally, because the thermal integrator's output is at low frequency, no wideband circuitry is required. The circuit uses standard components and requires no special trimming techniques. It is based on measuring the amount of power required to maintain two similar but thermally decoupled masses at the same temperature. The input is applied to T1, a dual thermistor bead. The power dissipated in one leg (T1A) of this bead forces the other section (T1B) to shift down in value, unbalancing the bridge formed by the other bead and the 90k resistors. This imbalance is amplified by the A1-A2-A3 combination. A3's output is applied to a second thermistor bead, T2. T2A heats, causing T2B to decay in value. As T2B's resistance drops, the bridge balances. A3's output adjusts drive to T2A until T1B and T2B have equal values. Under these conditions, the voltage at T2A is equal to the RMS value of the circuit's input. In fact, slight mass imbalances between T1 and T2 contribute a gain error, which is corrected at A4. RC filters at A1 and A2 and the 0.01 μ F capacitor eliminate possible high frequency error due to capacitive coupling between T1A and T1B. The diode in A3's output line prevents circuit latch-up.

Figure 7 details the recommended thermal arrangement for the thermistors. The Styrofoam block provides an isothermal environment and coiling the thermistor leads attenuates heat pipe effects to the outside ambient. The 2-inch distance between the devices allows them to see identical thermal conditions without interaction. To calibrate this circuit, apply 10V_{DC} to the input and adjust the full-scale trim for 10V out at A4. Accuracy remains within 2% from DC to 50MHz for inputs of 300mV to 10V. Crest factors of 100:1 contribute less than 0.1% additional error and response time to rated accuracy is five seconds.

Low Flow Rate Thermal Flowmeter

Measuring low flow rates in fluids presents difficulties. "Paddle wheel" and hinged vane type transducers have low and inaccurate outputs at low flow rates. If small diameter tubing is required, as in medical or biochemical work, such transduction techniques also become mechanically impractical. Figure 8 shows a thermally-based flowmeter which features high accuracy at rates as low as 1mL/minute and has a frequency output which is a linear function of flow rate. This design measures the differential temperature between two sensors (Figure 9). One sensor, T1, located before the heater resistor, assumes the fluid's temperature before it is heated by the resistor. The second sensor, T2, picks up the temperature rise induced into the fluid by the resistor's heating. The sensor's difference signal appears at A1's output. A2 amplifies this difference with a time constant set by the 10M Ω adjustment. Figure 10 shows A2's output versus flow rate. The function has an inverse relationship. A3 and A4 linearize this relationship, while simultaneously providing a frequency output (Figure 10). A3 functions as an integrator which is biased from the LT1004 and the 383k input resistor. Its output is compared to A2's output at A4. Large inputs from A2 force the integrator to run for a long time before A4 can go high, turning on Q1 and resetting A3. For small inputs from A2, A3 does not have to integrate very long before resetting action occurs. Thus, the configuration oscillates at a frequency which is inversely proportional to A2's output voltage. Since this voltage is inversely related to flow rate, the oscillation frequency linearly corresponds to flow rate.

Several thermal considerations are important in this circuit. The amount of power dissipated into the stream should be constant to maintain calibration. Ideally, the best way to do this is to measure the VI product at the heater resistor and construct a control loop to maintain constant wattage

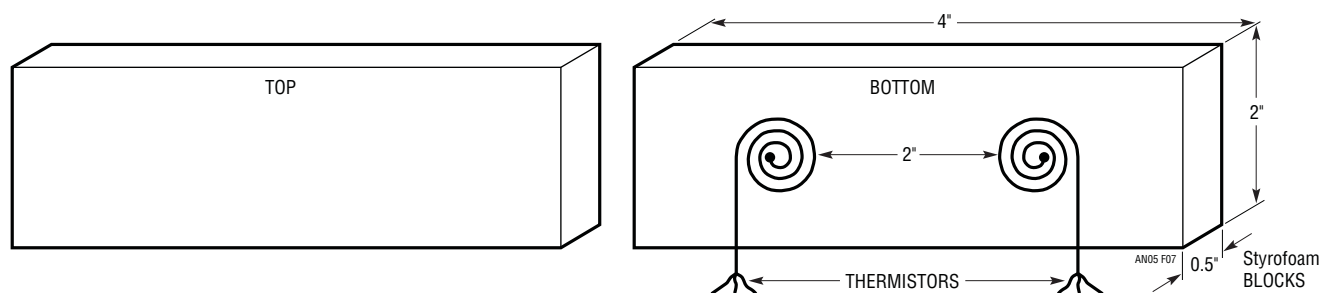


Figure 7. Thermal Arrangement for RMS→DC Converter

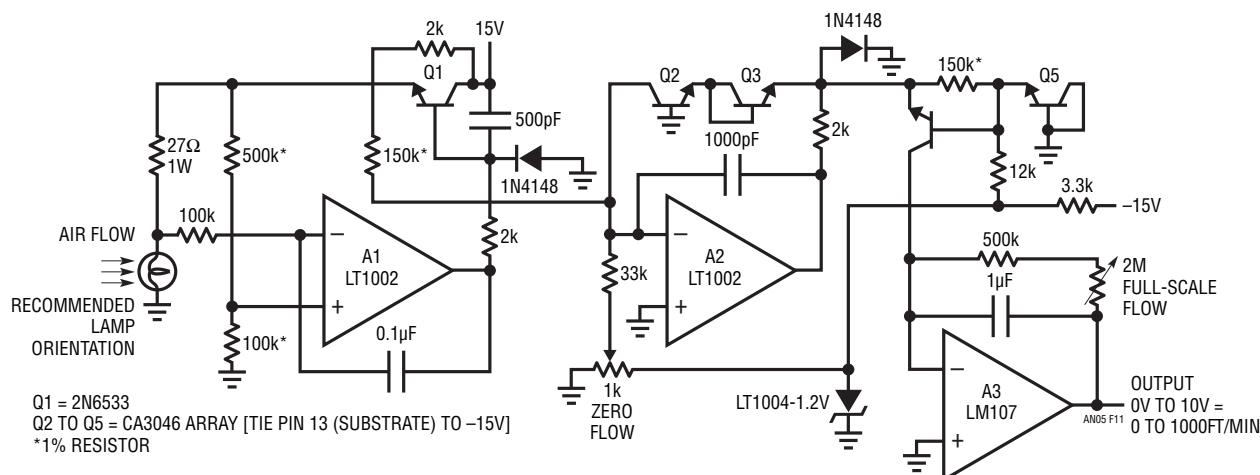


Figure 11. Thermal Anemometer

328 lamp is modified for this circuit by removing its glass envelope. The lamp is placed in a bridge which is monitored by A1. A1's output is current amplified by Q1 and fed back to drive the bridge. The capacitors and 220 Ω resistor ensure stability. The 2k resistor furnishes start-up. When power is applied, the lamp is at a low resistance and Q1's emitter tries to come full on. As current flows through the lamp, its temperature quickly rises, forcing its resistance to increase. This action increases A1's negative input potential. Q1's emitter voltage decreases and the circuit finds a stable operating point. To keep the bridge balanced, A1 acts to force the lamp's resistance, hence its temperature, constant. The 10k-2k bridge values have been chosen so that the lamp operates just below the incandescence point. This high temperature minimizes the effects of ambient temperature shifts on circuit operation. Under these conditions, the only physical parameter which can significantly influence the lamp's temperature is a change in dissipation characteristic. Air flow moving by the lamp provides this change. Moving air by the lamp tends to cool it and A1 increases Q1's output to maintain the lamp's temperature. The voltage at Q1's emitter is nonlinearly, but predictably, related to air flow by the lamp. A2, A3 and the array transistors form a circuit which squares and amplifies Q1's emitter voltage to give a linear, calibrated output versus air flow rate. To use this circuit, place the lamp in the air flow so that its filament is a 90° angle to the flow. Next, either shut off the air flow or shield the lamp from it and adjust the zero flow potentiometer for a circuit output of 0V. Then, expose the lamp to air flow of 1000 feet/minute and trim the full flow potentiometer for 10V output. Repeat

these adjustments until both points are fixed. With this procedure completed, the air flowmeter is accurate within 3% over the entire 0 to 1000 foot/minute range.

Low Distortion, Thermally Stabilized Wien Bridge Oscillator

The positive temperature coefficient of lamp filaments is employed in a modern adaptation of a classic circuit in Figure 12. In any oscillator it is necessary to control the gain as well as the phase shift at the frequency of interest. If gain is too low, oscillation will not occur. Conversely, too much gain will cause saturation limiting. Figure 12 uses a variable Wien Bridge to provide frequency tuning from 20Hz to 20kHz. Gain control comes from the positive temperature coefficient of the lamp. When power is applied, the lamp is at a low resistance value, gain is high and oscillation amplitude builds. As amplitude builds, the lamp current increases, heating occurs and its resistance goes up. This causes a reduction in amplifier gain and the circuit finds a stable operating point. The lamp's gain-regulating behavior is flat within 0.25dB over the 20Hz-20kHz range of the circuit. The smooth, limiting nature of the lamp's operation, in combination with its simplicity, gives good results. Trace A, Figure 13 shows circuit output at 10kHz. Harmonic distortion is shown in Trace B and is below 0.003%. The trace shows that most of the distortion is due to second harmonic content and some crossover disturbance is noticeable. The low resistance values in the Wein network and the 3.8nV $\sqrt{\text{Hz}}$ noise specification of the LT1037 eliminate amplifier noise as an error term.

Application Note 5

At low frequencies, the thermal time constant of the small normal mode lamp begins to introduce distortion levels above 0.01%. This is due to "hunting" as the oscillator's frequency approaches the lamp thermal time constant. This effect can be eliminated, at the expense of reduced output amplitude and longer amplitude settling time, by switching to the low frequency, low distortion mode. The four large lamps give a longer thermal time constant and distortion is reduced. Figure 14 plots distortion versus frequency for the circuit.

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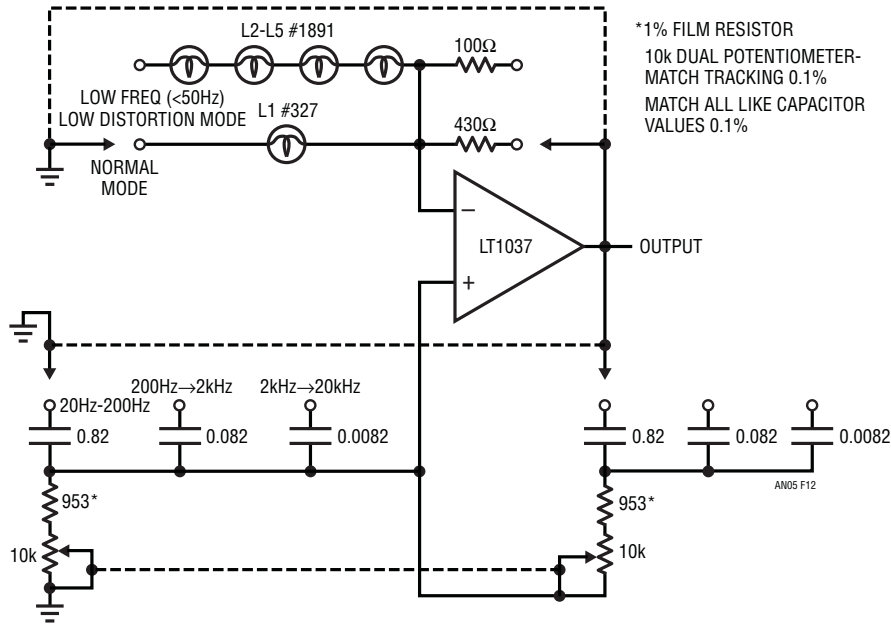


Figure 12. Low Distortion Sinewave Oscillator

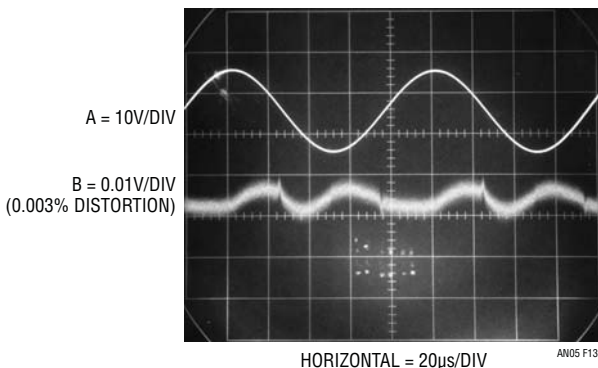


Figure 13. Oscillator Waveforms

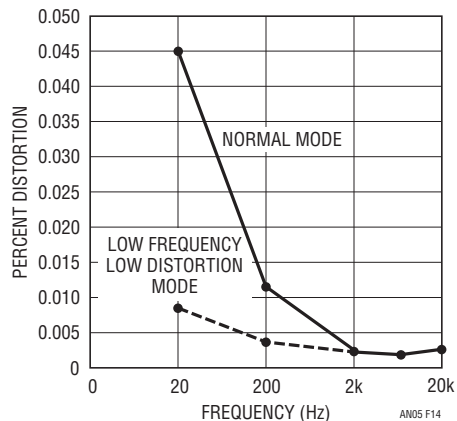


Figure 14. Oscillator Distortion vs Frequency

Applications of New Precision Op Amps

Jim Williams

Two new precision bipolar op amps, the LT1001 and a dual version, the LT1002, expand applications possibilities for designers of measurement and control circuits. These devices will find use where high accuracy and/or microvolt level capability are required. A summary of the new op-amp specifications appears in Table A. The high performance of these devices makes them useful as building blocks in precision circuitry. Figure 1 furnishes an excellent example.

Table A. LT1001A Specifications

OFFSET VOLTAGE	
Initial	25 μ V Max
vs Temperature	1 μ V/ $^{\circ}$ C Max
vs Time	1 μ V/Month Max
BIAS CURRENT	
Initial	2nA Max
Offset	2nA Max
OPEN LOOP GAIN	400,000 Min
COMMON-MODE REJECTION (+13V)	114dB Min
POWER SUPPLY REJECTION	110dB Min
SLEW RATE	0.15V/ μ s Min
GAIN-BANDWIDTH PRODUCT	0.5MHz Min
NOISE (Voltage)	
0.1Hz-10Hz	0.5 μ V/p-p
10Hz	18nV/ \sqrt Hz Max
100Hz	13nV/ \sqrt Hz Max
1000Hz	11nV/ \sqrt Hz Max
NOISE (Current)	
0.1Hz-10Hz	30pAp-p Max
10Hz	0.8pAp-p Max
100Hz	0.23pAp-p Max
1000Hz	0.17pAp-p Max

Instrumentation Amplifier with $V_{CM} = 300V$ and $CMRR > 160dB$

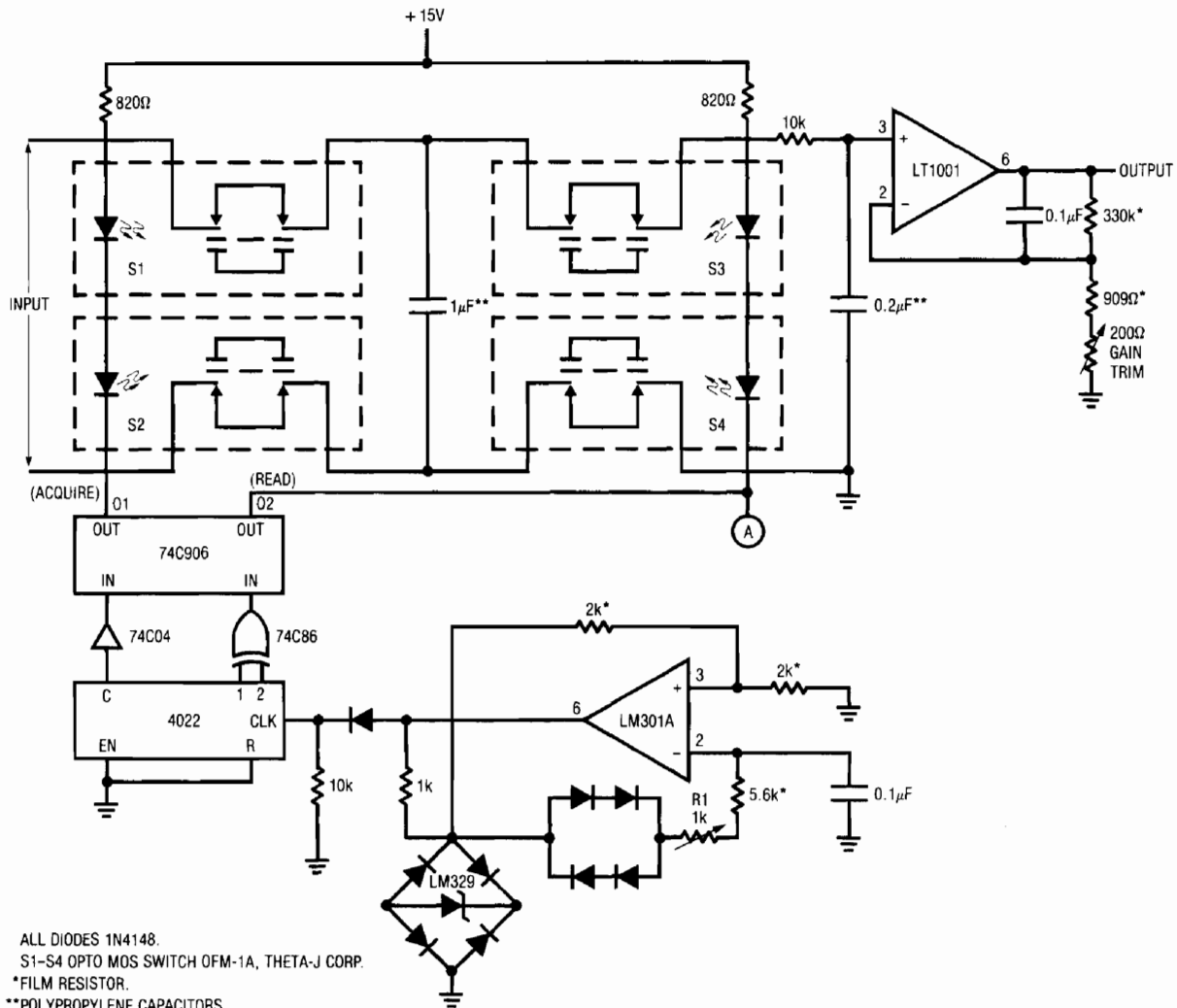
The circuit of Figure 1 may be used wherever differential inputs are required. It is particularly applicable to transducer signal conditioning where high common-mode voltages may exist. The circuit has the low offset and drift of the LT1002, but also incorporates a novel switched-capacitor "front end" to achieve some specifications not available in an instrumentation amplifier.

Common-mode rejection ratio at DC for the front end exceeds 160dB. The amplifier will operate over a $\pm 300V$ common-mode range and gain accuracy and stability are limited only by external resistors. The high common-mode voltage capability of the design allows it to withstand transient and fault conditions often encountered in industrial environments.

The circuit's inputs are fed to LED-driven optically-coupled MOSFET switches, S1 and S2. Two similar switches, S3 and S4, are in series with S1 and S2. A2, a precision oscillator, and its associated CMOS logic functions generate non-overlapping clock outputs which drive the switch's LEDs. When the "acquire pulse" is low, S1 and S2 are on and the 1 μ F capacitor acquires the differential voltage at the bridge's output. During this interval, S3 and S4 are off. When the acquire pulse rises, S1 and S2 begin to go off. After a delay to allow S1 and S2 to fully open, the "read pulse" goes low, turning on S3 and S4. Now, the 1 μ F capacitor appears as a ground-referred voltage source which is read by the main amplifier, A3. The 10k-0.2 μ F network allows A3's input to retain the 1 μ F unit's value when the circuit returns to the acquire mode. A3 provides the circuit's output. Its gain is set in normal fashion by feedback resistors. The 0.1 μ F feedback capacitor sets a rolloff of 5Hz. Several features aid circuit operation. A2 is trimmed for a 93Hz clock output. This frequency inhibits power line-originated noise from interacting with the switching action because it is not harmonically related to 60Hz. Such interaction may cause DC errors.

The differential-to-single-ended transition performed by the switches and capacitors means that A3 never sees the input's common-mode signal. The 300V breakdown specification of the optically-driven MOSFET switch allows the circuit to withstand and operate at common-mode levels of $\pm 300V$ (switch leakage typically rises above 1nA over 100V, causing some circuit performance degradation). In addition, the optical drive to the

Application Note 6



ALL DIODES 1N4148.
 S1-S4 OPTO MOS SWITCH OFM-1A, THETA-J CORP.
 *FILM RESISTOR.
 **POLYPROPYLENE CAPACITORS.
 ADJUST R1 FOR 93Hz AT TEST POINT A.
 A FLYING CAPACITOR CHARGED BY CLOCKED PHOTO-DRIVEN FET SWITCHES CONVERTS A DIFFERENTIAL SIGNAL AT A HIGH COMMON-MODE VOLTAGE TO A SINGLE-ENDED SIGNAL AT THE LT1001 OUTPUT.

Figure 1. Instrumentation Amplifier with 300V Common-Mode Range

MOSFETs eliminates the charge injection problems common to FET switched capacitive networks. The 750µs switching speed of the optical switch limits the circuit carrier to low frequencies, but most transducer circuits do not require any substantial bandwidth.

Linearized Platinum RTD Signal Conditioner

Platinum resistance temperature detectors (RTD) are generally accepted as the best choice for high accuracy and stability in temperature measurements. Unfortunately, they exhibit a non-linear temperature versus

resistance characteristic which complicates signal conditioning. Over a 0°C to 100°C range this non-linearity amounts to 0.4°C. Figure 2 shows a thermometer circuit which corrects for this error and achieves ± 0.025°C absolute accuracy over the 0°C-100°C range.

A1 functions as a negative gain inverter to drive a constant current through the platinum sensor. The LT1009 and the 10k resistor provide the current reference. Because A1 operates at negative gain, the voltage across the RTD is low and self-heating induced errors are reduced. A1's output potential, which varies with the

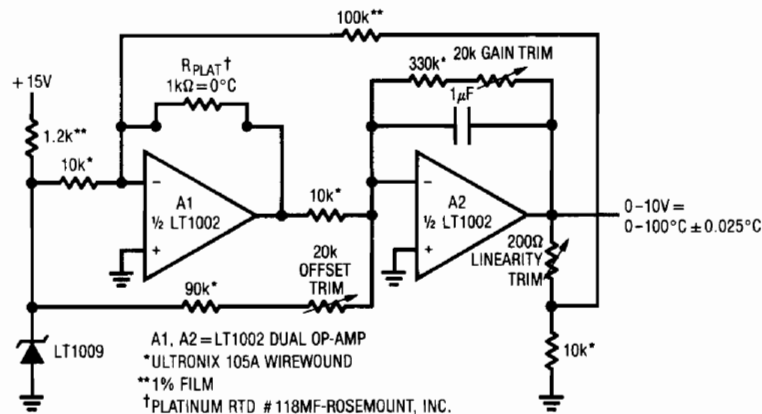


Figure 2. Linear Thermometer

platinum sensor's temperature, feeds A2. A2 provides scaled gain and offsetting so that its output will swing from 0.00V to 10.000V for a 0.00°C to 100.00°C temperature swing at the RTD. The 1μF capacitor limits noise pick-up. Normally, this circuit would exhibit a 0.4°C non-linearity error due to the RTD's imperfect response. This term is corrected by returning a small portion of the circuit's output to A1's negative input. This varies the reference current, causing compensatory changes in the circuit's gain slope. To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432-K) for the sensor. Set the box to the 0°C value (1000.0Ω) and adjust the offset trim for a 0.000V output. Next, set the decade box for a 35°C output (1138.7Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 1392.6Ω (100.00°C) and trim the linearity adjustment. Repeat this sequence until all three points are fixed. Total error over the entire range will be within $\pm 0.025^\circ\text{C}$. The resistance values given are for a nominal 1000.0Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 1000.0Ω. This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Thermally Controlled Ni Cad Charger

Charging Ni Cad batteries at high current rates is desirable because it allows short charge time. The difficulty with such operations is that excessive internal heating degrades the batteries and can cause gas venting to the outside atmosphere. Schemes based on monitoring cell voltage during charge suffer because cell voltage is not necessarily indicative of the charge state of the battery. Open loop techniques involving high charge rates for a fixed time do not account for battery characteristic shifts over life and ambient temperature.

One way to charge batteries rapidly without abuse is to measure cell temperature and taper the charge accordingly. Figure 3 uses a thermocouple for this function. A second thermocouple nulls out the effects of ambient temperature. The LT1001 amplifier furnishes the low level capability necessary to work with the microvolt level thermocouple signals. To understand the circuit's operation, assume a discharged battery pack in the Darlington collector line. The battery and ambient thermocouples are at the same temperature. The battery thermocouple is directly mounted to one of the cells in the pack. The ambient thermocouple is exposed to ambient temperature and mounted to a thermal mass which approximates that

Application Note 6

of the battery pack. Under these conditions, the thermocouple voltages cancel and the positive input is at zero volts. The negative current through the 620kΩ resistor to the summing junction causes the amplifier to swing positive, turning on the Darlington pair. Current flows from the +15V supply, through the battery pack and to ground via the 0.6Ω shunt. The voltage across the shunt rises to 1V, balancing the summing junction, and the amplifier servo controls about 1.6A through the battery pack. As the battery charges, it heats. This heat is picked up by the battery-mounted thermocouple. The temperature difference between the two thermocouples determines the voltage which appears at the amplifier's positive input. As battery temperature rises, this small negative voltage (1°C difference between the thermocouples equals 40μV) becomes larger. The amplifier, operating at a gain of 4300, gradually reduces the current through the bat-

tery to maintain its inputs at balance. The effect of this action is shown in Figure 4. The battery charges at a high rate until heating occurs and the circuit then tapers the charge. The values given in the circuit limit the battery surface temperature rise over ambient to about 5°C.

Precision Adjustable Dead Zone Circuit

Figure 5 details a precision adjustable dead zone circuit. This is particularly useful in motor driven position servo circuits. In such applications it is desirable to generate an adjustable, symmetrical dead band so that the servo motor's degree of stiffness and hunting characteristics around null may be controlled. In addition, because stages of this type are usually followed by very high gain servo amplifiers, it is necessary that low voltage offsets be maintained when inside the dead band zone.

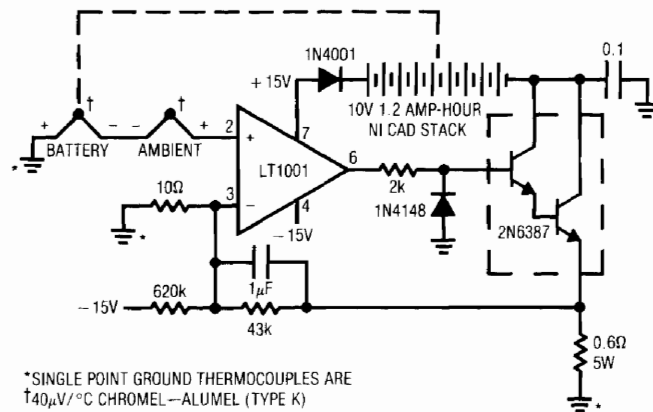


Figure 3. Thermally Controlled Ni Cad Battery Charger

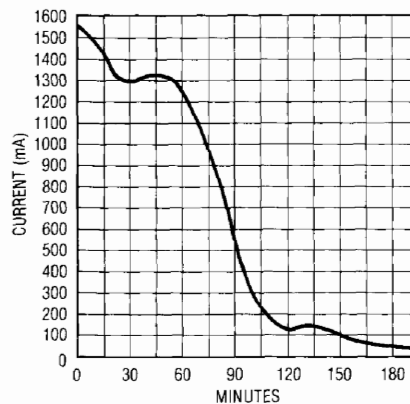


Figure 4. Charging Current vs Time for a 1.2A-Hour Cell

The circuit is made up of a synchronous rectifier (A1, C1), a variable unipolar dead zone cell composed of A2A and Q2-Q4, and a demodulator (A2B). When a circuit input (Trace A, Figure 6), in this case a triangle wave, is applied, the C1 crossing detector determines its polarity. C1's output (Trace B, Figure 6) drives Q1. When the input is negative, C1 goes high and Q1 conducts, grounding A1's positive input (Trace C, Figure 6). This turns A1 into a unity-gain inverter and its output (Trace D, Figure 6) inverts the input signal. For negative inputs, C1's output is low, cutting Q1 off and A1 unity-gain follows the input. This synchronous rectification presents the dead zone cell with a unipolar signal. Q2 forms a voltage adjustable current control at A2A's summing junction. Q3 provides V_{BE} temperature compensation and Q4 protects Q2's V_{BE} against reverse bias. When the dead zone command input is above A1's output, Q2 (Q2 emitter is Trace E, Figure 6) is off and A2A's output (Trace F, Figure 6) goes

to zero. When A1's output rises above the dead zone input, Q2 conducts, A2A functions as a current-to-voltage converter, and an inverted version of A1's output appears at A2A's output. This signal feeds synchronous demodulator A2B, which recovers the bipolar input signal. Q6 is switched by Q5's phase inverted version of C1's output. When the circuit signal input is positive, Q6 is on, grounding A2B's positive input (Trace G, Figure 6) and A2B's output inverts. The opposite action occurs for negative signal inputs. In this fashion, A2B's output recovers the bipolar input signal while preserving the adjustable dead zone. Because the same device (Q2) is used for positive and negative signals, dead zone symmetry is nearly ideal. Q2's V_{BE} drop limits the minimum dead zone to 600mV. Thus, A1's offsets will never be seen when the circuit is in dead band and the effects of delay time and offset in C1 are similarly eliminated. Only A2A and A2B need to be low offset devices.

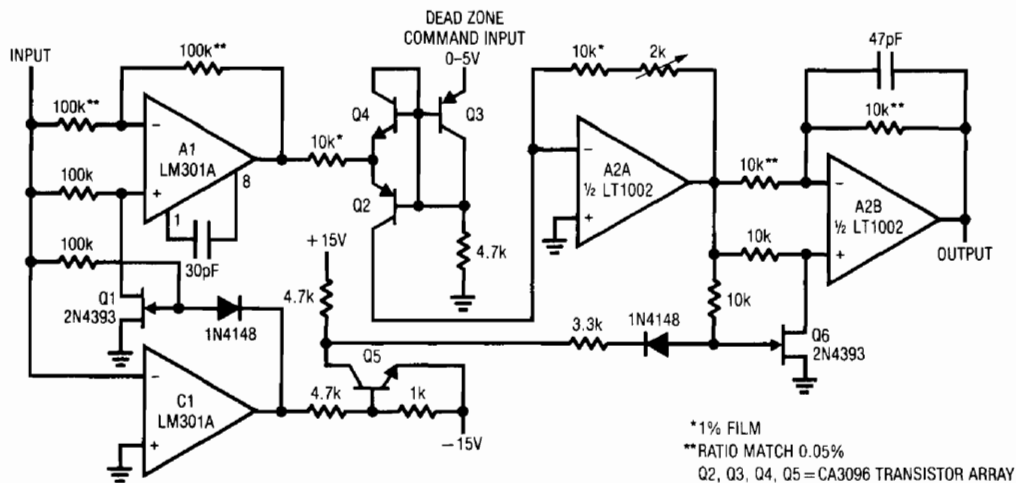


Figure 5. Precision Adjustable Dead Zone Generator

A = 10V/DIV
 B = 50V/DIV
 C = 5V/DIV
 D = 5V/DIV
 E = 2V/DIV
 F = 5V/DIV
 G = 5V/DIV
 H = 5V/DIV

HORIZONTAL = 500 μ S/DIV

Figure 6

Application Note 6

Ultra-Precision Variable Voltage Reference

Figure 7 combines an LT1002 with a MOSFET switched toroid to create a precision variable voltage reference with a wide dynamic range of outputs. The reference has two outputs. The low voltage range spans 0V to 10V and is settable in 100 μ V (10ppm at full scale) increments. The high voltage range runs from 0V to 100V in 1mV steps (also 10ppm at full scale). The low voltage range is derived from A1, the LM199A voltage reference, and the panel mounted Kelvin-Varley Divider (KVD). A1 is a follower with gain, with the 2N2219 used for a boosted output. The selected value, typically in the 43k Ω range, and the 100 Ω potentiometer are used to trim the output to 10.0000V with the KVD dials set to full scale. The low offset of the LT1002 op amp eliminates the need for an offset trim. The non-inverting configuration used permits the 100k Ω KVD to be unloaded by the amplifier. The low bias current and high CMRR of the LT1002 are required to read the KVD without introducing error. The 100 Ω resistor is a short circuit limit and the low range output is taken at the 2N2219 emitter.

The circuit achieves its high voltage output without resorting to separate high voltage power supplies. Instead, the DC input to a chopped step-up toroidal transformer is servo-controlled by an op amp. The C1 multivibrator generates a 40kHz clock, which is divided into a complementary 20kHz square wave by the 74C74 flip-flop. These waveforms bias the VMOS FETs. A2 compares the divided down output of the transformer's rectifier-filter against the low voltage output. The amplified difference voltage biases the power Darlington, which drives the transformer's primary center tap, completing a feedback loop around the transformer. The 0.1 μ F unit is used for loop stability. A2 servos whatever voltage is required to balance its inputs. The loop is calibrated so a precise 0V–100.00V output corresponds to the setting of the KVD dials. The VMOS choppers are the key to maintaining the wide dynamic range of settings on the high voltage scale. Their resistive saturation characteristic allows the control range to extend to within an LSB (1mV) of 0V. The 2N2907 serves as a simple coarse voltage clamp on the high voltage range. The potentiometer allows a voltage ceiling to

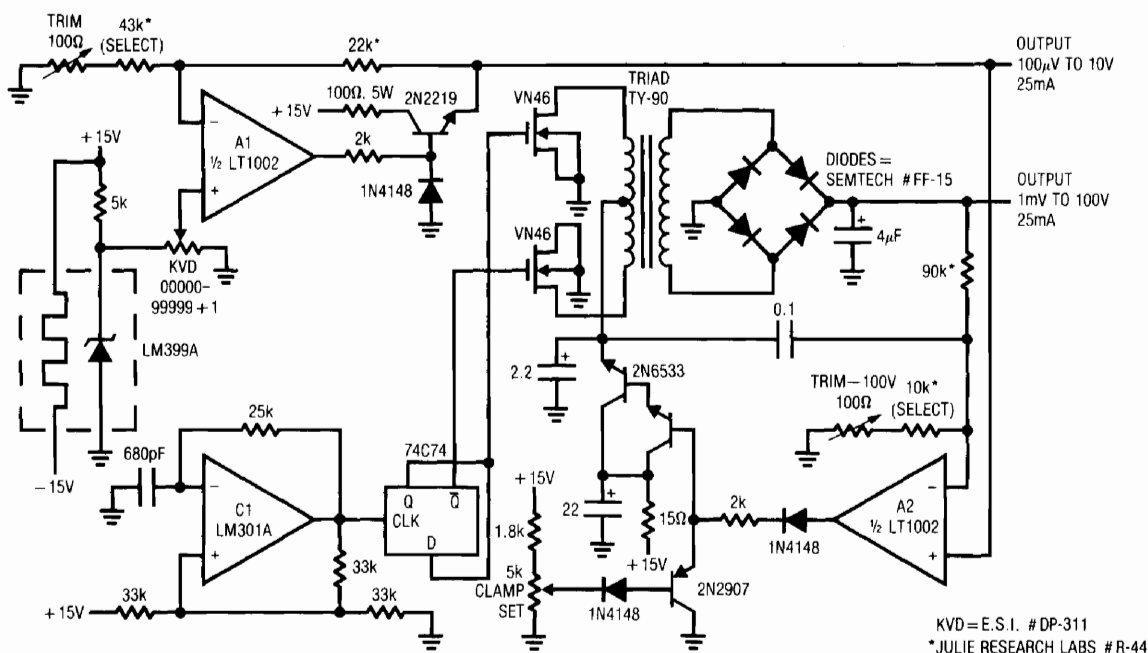


Figure 7. Ultra-Precision Variable Voltage Reference

be set for safety or other reasons when using the reference. To calibrate this circuit, select the 43kΩ value and adjust the 100Ω trim for a precise 10.0000V output at the low voltage output. Next, select the 10kΩ value and trim the 100Ω unit in the high voltage divider string. The typical stability of this circuit under laboratory conditions ($25^{\circ}\text{C} \pm 5^{\circ}\text{C}$) may be estimated from the following data:

10V Range

Zener drift—		
temperature $5^{\circ}\text{C} \times 0.2\text{ppm}/^{\circ}\text{C}$	=	1ppm
Zener drift—time (per year)	=	25ppm
A1 op amp E_{OS} drift		
$0.5\mu\text{V}/^{\circ}\text{C} \times 5^{\circ}\text{C} \times A = 1.4 = 2.5\mu\text{V}$	=	0.25ppm
A1 op amp E_{OS} drift—		
1 year = $10\mu\text{V}/\text{year}$	=	1ppm
KVD— $2\text{ppm}/^{\circ}\text{C}$ ratio shift $\times 5^{\circ}\text{C}$	=	10ppm

37.25ppm over $\pm 5^{\circ}\text{C}$ and
1 year at full scale

100V Range

All above errors	=	37.25ppm
A2 time and temperature	=	0.5ppm
		<hr/>
		37.75ppm at full scale

Precision High Speed Op Amp

The design requirements to achieve high DC accuracy in an amplifier such as the LT1001/1002 preclude high speed performance. Additionally, it is difficult to design a precision monolithic amplifier which will drive large currents because of internal die heating problems. Some applications do call for speed, accuracy and output drive capability. Figure 8 shows a circuit which can be used to meet these conflicting requirements. In this arrangement, the LT1001 is used to stabilize a broadband stage to build an op amp with the DC precision of the LT1001 and high speed capability. This composite amplifier

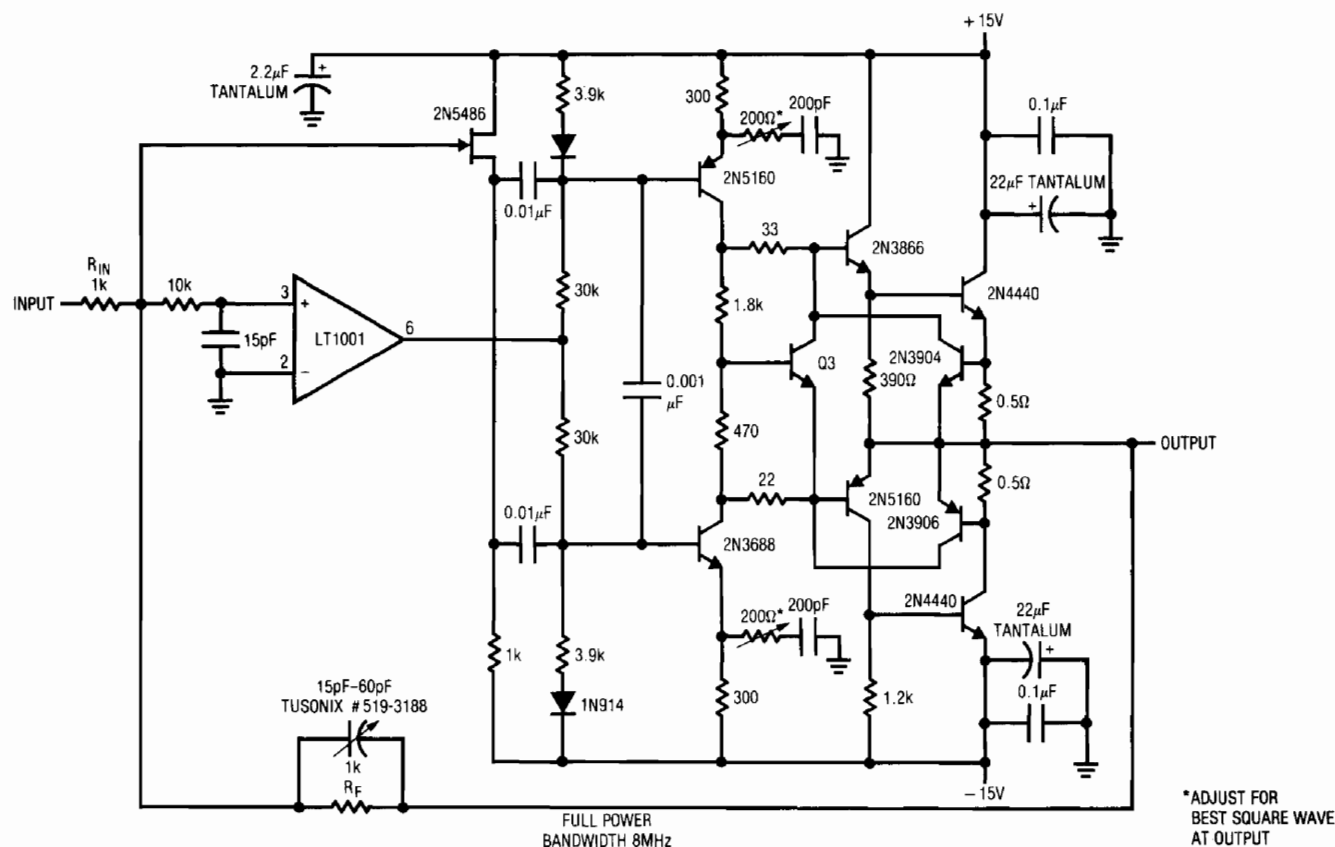


Figure 8. 1000V/ μs 1A Op Amp

Application Note 6

features a $1500\text{V}/\mu\text{s}$ slew rate, full output to 8MHz and will drive $\pm 10\text{V}$ into a 10Ω load. It is short circuit protected at $\pm 1\text{A}$. The offset and drift specifications are controlled by the LT1001. High speed signals are fed forward around the LT1001 through Q10 and directly drive the wideband stage. The LT1001 operates at low frequency to DC stabilize the fast stage. The high frequency rolloff of the LT1001 is matched to the low frequency rolloff of the discrete stage.

The high speed stage is composed of transistors with F_t 's approaching 1GHz. The output devices are NPN RF power transistors in a quasi-complementary arrangement. This is necessary because PNP RF power transistors are not available. Q8 and Q9 limit short circuit

current by sensing across 0.5Ω shunts. They apply degenerative feedback around the output stage when turned on, thereby limiting current. The 200Ω potentiometers and the variable feedback capacitor should be adjusted for a compromise between slew rate and output waveform clarity. Typically, the highest slew rate will sacrifice clean transitions. Figure 9 shows the response of the amplifier (Trace B) to a fast input pulse (Trace A), with the adjustments optimized for clean transitions. Slew rate is still $1000\text{V}/\mu\text{s}$ and the output appears clean within the 275MHz bandpass of the monitoring oscilloscope. In setting up and using this circuit, RF layout techniques and a ground plane are mandatory and the 2N4440s must be heat sunk.

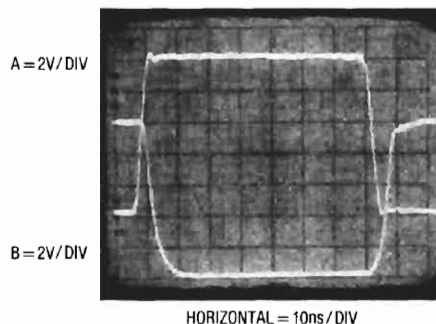


Figure 9. Op Amp Response

Some Techniques for Direct Digitization of Transducer Outputs

Jim Williams

Almost all transducers produce low level signals. Normally, high accuracy signal conditioning amplifiers are used to boost these outputs to levels which can easily drive cables, additional circuitry, or data converters. This practice raises the signal processing range well above the error floor, permitting high resolution over a wide dynamic range.

Some emerging trends in transducer-based systems are causing the use of signal conditioning amplifiers to be reevaluated. While these amplifiers will always be useful, their utilization may not be as universal as it once was. In particular, many industrial transducer-fed systems are employing digital transmission of signals to eliminate noise-induced inaccuracies in long cable runs. Additionally, the increasing digital content of systems, along with pressures on board space and cost, make it desirable to digitize transducer outputs as far forward in the signal chain as possible. These trends point toward direct digitization of transducer outputs—a difficult task.

Classical A/D conversion techniques emphasize high level input ranges. This allows LSB step size to be as large as possible, minimizing offset and noise-caused errors. For this reason, A/D LSB size is almost always above a millivolt, with 100 μ V to 200 μ V per LSB available in a few 10V full-scale devices. The requirements to directly A/D convert the output of a typical strain gauge transducer are illuminating. The transducer's full-scale output is 30mV,

meaning a 10-bit A/D converter must have an LSB increment of only 30 μ V. Performing a 10-bit conversion on a type K thermocouple monitoring a 0°C to 60°C environment proves even more stringent. The type K thermocouple puts out 41.4 μ V/°C over the 0°C to 60°C range. The LSB increment is found by:

$$\frac{60^{\circ}\text{C} \cdot 41.4\mu\text{V}/^{\circ}\text{C}}{1024} = 2.42\mu\text{V}/\text{LSB}$$

These examples furnish extraordinarily small step sizes, far below commercially available A/D units and seemingly impossible to digitize without DC preamplification. In fact, both transducers' outputs may be directly digitized to stable 10-bit resolution using circuitry specifically designed for the function.

This application note details circuit techniques which directly digitize the low level outputs of a variety of transducers. The approaches described are unique in that they do not utilize any DC gain stage. The transducer outputs receive no DC signal conditioning; A/D conversion is directly performed at low level. The circuits produce a serial data output which may be transmitted over a single wire with the characteristic noise immunity of digital systems. By eliminating the traditional DC gain stage, these circuits furnish a direct, economical way to digitize low level transducer outputs without sacrificing performance.

Application Note 7

Figure 1 shows a simple way to convert the current output of an LM334 temperature sensor to a corresponding output frequency. The sensor pulls a temperature-dependent current ($0.33\%/^{\circ}\text{C}$) from A1's positive input node. This point, biased from the LM329-driven resistor string, responds with a varying, temperature-dependent voltage. The voltage varies the operating point of A1, configured as a self-resetting integrator. A1 integrates the LM329-referenced current into its summing point, producing a negative-going ramp at its output. When the ramp amplitude becomes large enough, the transistors turn on, resetting the feedback capacitor and forcing A1's output to zero. When the capacitor's reset current goes to zero, the transistors go off and A1 begins to integrate negatively again. The frequency of this oscillation action is dependent on A1's DC operating point, which varies with the LM334's temperature. The circuit's DC biasing values are arranged so that a 0°C to 100°C sensor temperature excursion produces 0kHz to 1kHz at the output. Additionally, only 2V appear across the LM334, minimizing sensor power dissipation related errors. The differentiator-transistor network at A1's output provides a TTL compatible output. To calibrate this circuit, place the LM334 in a 0°C environment and trim the "0°C adjust" for 0Hz. Next, put the LM334 in a 100°C environment and set the "100°C adjust" for 1kHz output.

Repeat this procedure until both points are fixed. This circuit has a stable 0.1°C resolution with $\pm 1.0^{\circ}\text{C}$ accuracy.

Figure 2 shows another temperature-to-frequency converter, but this circuit uses the popular type K thermocouple as a sensor. The design includes cold junction compensation for the thermocouple over a 0°C to 60°C range. Accuracy is $\pm 1^{\circ}\text{C}$ and resolution is 0.1°C .

The thermocouple's extremely low output ($41.4\mu\text{V}/^{\circ}\text{C}$) and the requirement for cold junction compensation make it one of the most difficult transducers to directly digitize. The approach used is based on the $50\text{nV}/^{\circ}\text{C}$ input offset drift performance of the LTC[®]1052 chopper-stabilized amplifier.

In this circuit, A1's positive input is biased by the thermocouple. A1's output drives a crude $V \rightarrow F$ converter, comprised of the 74C04 inverters and associated components. Each $V \rightarrow F$ output pulse causes a fixed quantity of charge to be dispensed into a $1\mu\text{F}$ capacitor from the 100pF capacitor via the LTC1043 switch. The larger capacitor integrates the packets of charge, producing a DC voltage at A1's negative input. A1's output forces the $V \rightarrow F$ converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action eliminates drift and nonlinearities in the $V \rightarrow F$ converter as an error

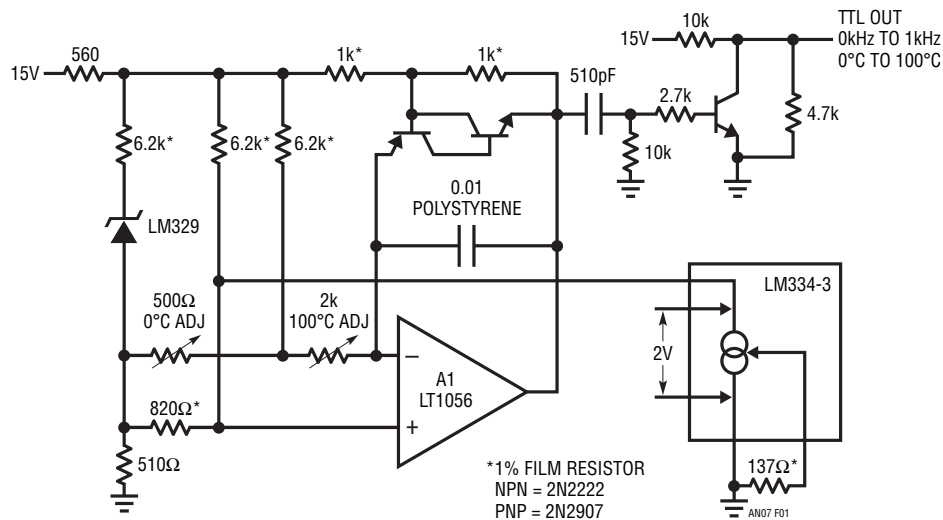


Figure 1. Temperature-to-Frequency Converter

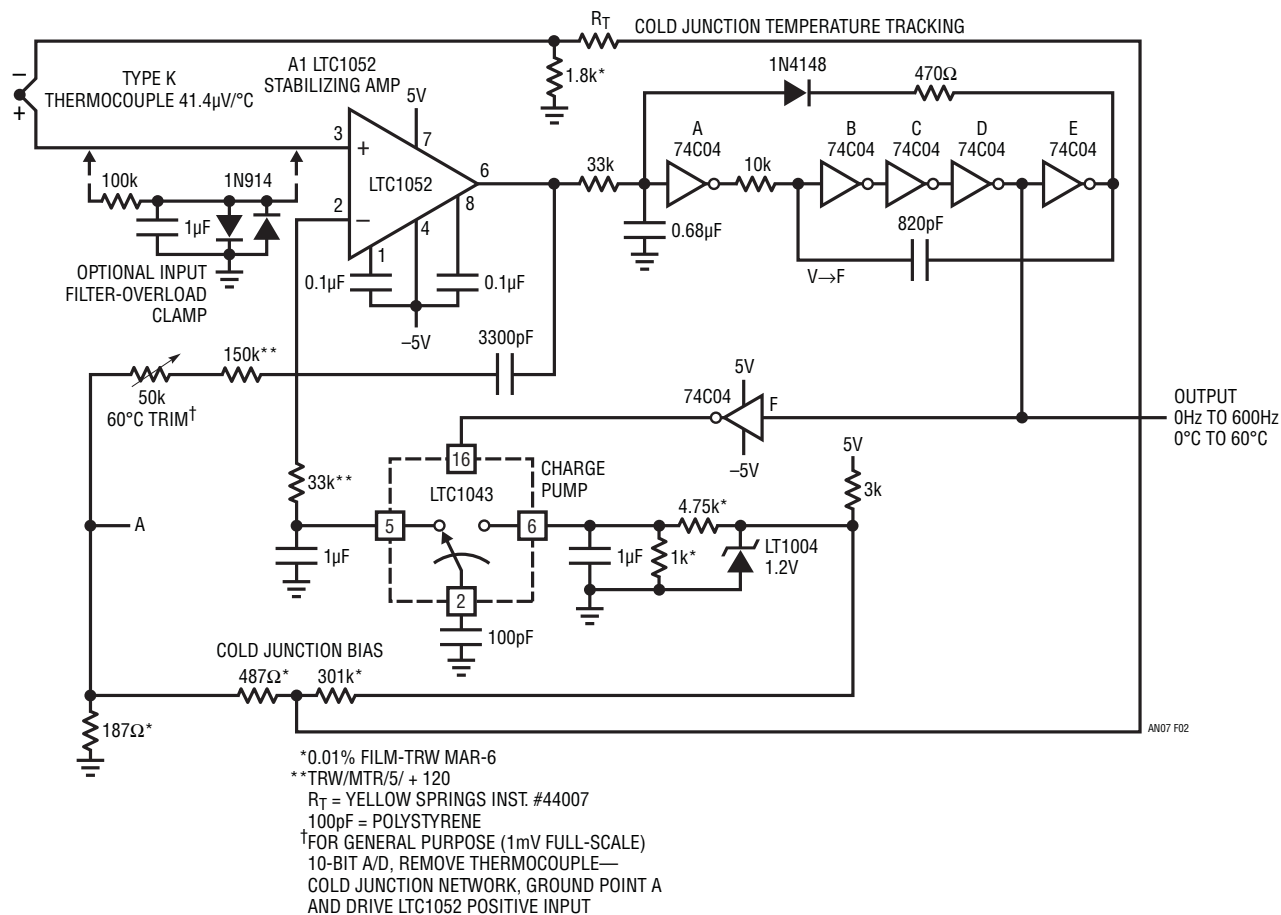


Figure 2. Thermocouple-to-Frequency Converter

term and the output frequency is solely a function of the DC conditions at A1's inputs. The 3300pF capacitor forms a dominant response pole at A1, stabilizing the loop.

A1's low drift eliminates offset errors in the circuit, despite an LSB value of only $4.14\mu\text{V}$ (0.1°C)!

R_T , a thermistor, and the 1.8k, 187 Ω , 487 Ω and 301k values form a cold junction compensation network which is biased from the LT[®]1004 1.2V reference. In addition to cold junction compensation, the network provides offsetting, permitting a 0°C sensor temperature to yield 0Hz at the output.

Figure 3 details circuit operation. A1's output drives the 33k-0.68 μF combination, producing a ramp (Trace A, Figure 3) across the capacitor. When the ramp crosses inverter A's threshold, the cascaded inverter chain switches, producing a low output at E (Trace B). This causes the 0.68 μF capacitor to discharge through the diode, resetting the capacitor to 0V. The 820pF unit provides positive AC feedback to inverter B's input (Trace C), assuring a clean reset. The frequency of this ramp-and-reset sequence varies with A1's output. Inverter F's output controls the LTC1043 switch. When the inverter output is high, Pins 2 and 6 are connected, allowing the 100pF capacitor to charge to a

Application Note 7

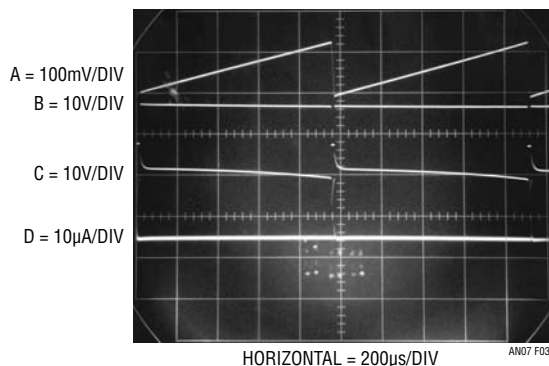


Figure 3. Thermocouple Digitizer Waveforms

potential derived from the LT1004 1.2V reference. When the inverter goes low, Pin 2 is connected to Pin 5. During this interval, the 100pF capacitor completely discharges (Trace D) into the 1µF unit. The amount of charge delivered is constant over each cycle ($Q = CV$), so the voltage the 1µF capacitor charges to is a function of frequency and discharge path resistance. This voltage is summed with the LT1004-derived offsetting potential at A1's negative input, closing a loop around A1. The $-120\text{ppm}/^\circ\text{C}$ drift of the 100pF charge-dispersing polystyrene capacitor is compensated by the opposing tempco of the specified resistors used in the 1µF's discharge path. Typical circuit gain is $20\text{ppm}/^\circ\text{C}$, allowing less than 1LSB (0.1°C) output drift over a 0°C to 70°C ambient operating range.

The thermocouple's known characteristics, combined with A1's low offset and the cold junction/offsetting network components specified, eliminate zero trimming. Calibration is accomplished by placing the thermocouple in a 60°C environment and adjusting the $50\text{k}\Omega$ potentiometer for a 600Hz output. Beyond 60°C the cold junction network departs from the thermocouple's response and output error increases rapidly. Although the digital output will be a function of the thermocouple's temperature over hundreds of degrees, linearization by a monitoring processor is required.

It is worth noting that this circuit can directly convert any low level, single-ended signal. If the offsetting/cold junction network is removed and the $50\text{k}\Omega$ potentiometer returned directly to ground, inputs may be applied to A1's positive terminal. The circuit produces a 10-bit accurate output with a full-scale range of only 1mV ($1\mu\text{V}$ per LSB)! The high impedance of A1's input allows filtering or overload clamping of the input signal without introducing error.

Figure 4 is another temperature measuring circuit, but the transducer used is unusual. The circuit measures temperature by utilizing the relationship between the speed of sound and temperature in a medium. In dry air the relationship is governed by:

$$C = 331, 5 \sqrt{\frac{T}{273}} \text{ meters/second}$$

where C = speed of sound.

Acoustic thermometry is used where extremes in operating temperature are encountered, such as cryogenics and nuclear reactors. Additionally, acoustic temperature standards have been built by operating the acoustic transducer inside a sealed, known medium.

The inherent time domain operation of acoustic thermometers allows a direct conversion into a digital output. Figure 4 shows a circuit that does this. A1, the inductor, and their associated components for a simple flyback type regulated 200V supply which biases the transducer. The transducer is composed of the Polaroid ultrasonic element noted, mounted at one end of a sealed, 6-inch long Invar tube. The Invar material minimizes mechanical tube deformation with temperature. The medium inside the tube is dry air. The transducer may be thought of as a capacitor, composed of an insulating disc with a conductive coating on each side.

Each time the TTL clock (Trace A, Figure 5) goes high, the transducer receives AC drive via the $0.22\mu\text{F}$ capacitor. This drive causes mechanical movement of the disc and ultrasonic energy is emitted. The clock input simultaneously sets the 74C74 flip-flop output (Trace E) low and pulls the $0.01\mu\text{F}$ capacitor to ground. This cuts off drive to C1's 3k output pull-up resistor (Trace C), forcing C1's output (Trace D) to zero. During the clock pulse's period, A2's output (Trace B) is saturated due to excessive signal at its input. When the clock pulse ceases, A2 comes out of bound and amplifies in its linear region. The ultrasonic transducer now acts like a capacitance microphone, with the 200V supply providing bias. Residual disc ringing is picked up and appears at A2's output. This signal cannot trigger C1, however, because the $0.01\mu\text{F}$ capacitor has not charged high enough to allow the inverter to chain output to bias C1's output pull-up resistor.

The ultrasonic energy emitted by the transducer travels down the tube, bounces off the far end and heads toward the transducer. Before it returns, the $0.01\mu\text{F}$ capacitor crosses the inverter's threshold and C1's $3\text{k}\Omega$ resistor (Trace C) receives bias. Upon returning, the sonic energy causes a mechanical displacement of the transducer, forcing a shift in capacitance. This capacitance shift causes charge to be displaced into C2's summing point, and the

output responds with an amplified version of this signal (Trace B). C1's output (Trace D) triggers, resetting the flip-flop. The flip-flop's output pulse (Trace E) represents the transit time down the tube and will vary with temperature according to the equation given. A monitoring processor can convert this pulse width into the desired temperature information.

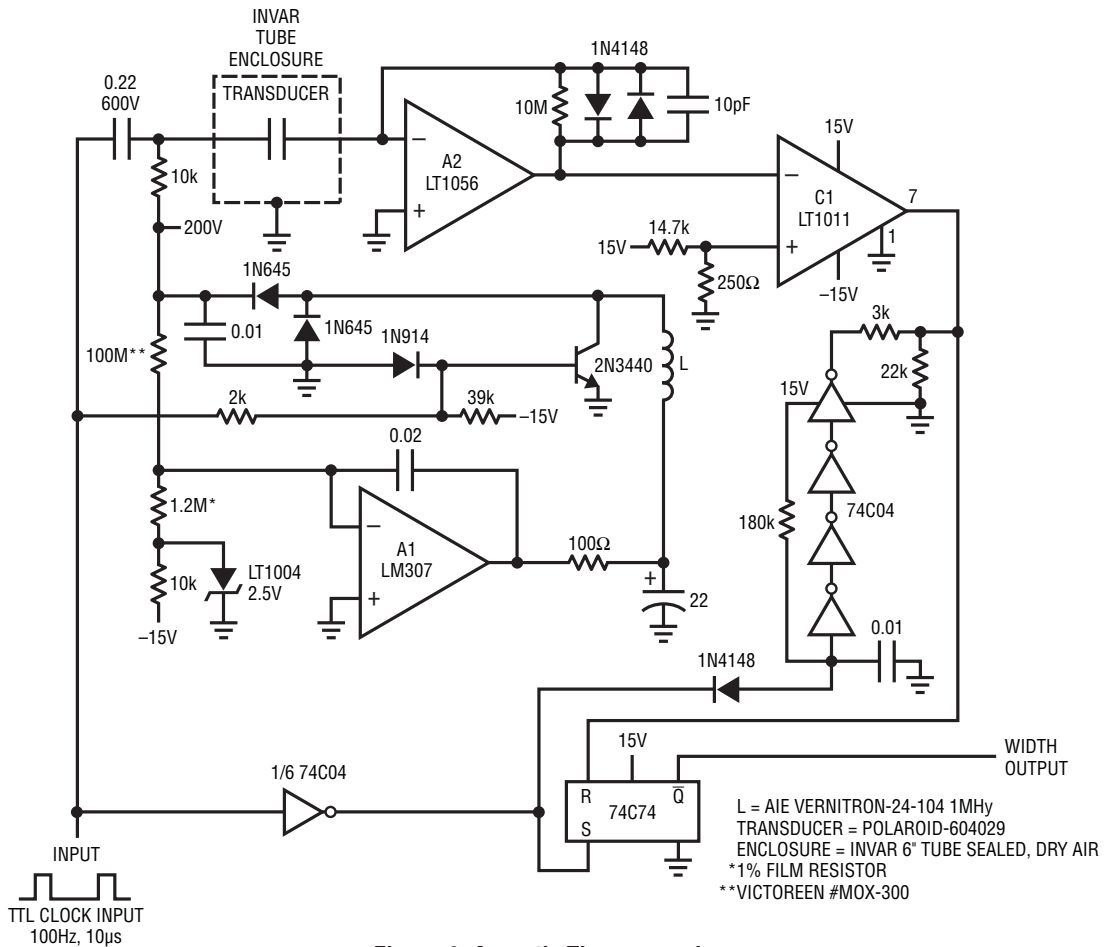


Figure 4. Acoustic Thermocouple

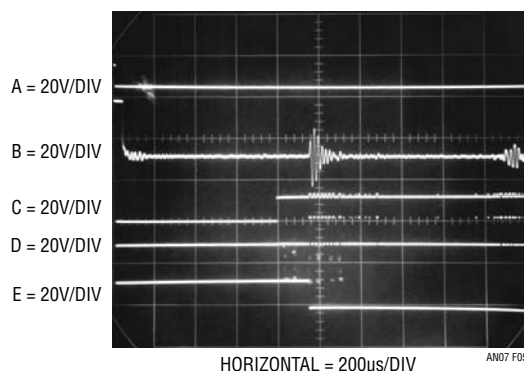


Figure 5. Acoustic Thermocouple Waveforms

Application Note 7

In the photograph another received signal, lower in amplitude, is visible at the extreme right-hand side of Trace B. Its position in time identifies it as a second bounce return from the tube's far end. Also, note the increased detected noise level after the return of the first bounce. This is due to sonic energy dispersion inside the tube. The transducer picks up energy deflected from the tube walls, which is phase shifted from the desired signal. C1 is seen to respond to these unwanted signal sources, but the circuit's final pulse output is unaffected. Additionally, the time window gating supplied to C1's pull-up resistor greatly reduces the likelihood of false triggering due to noise coming from outside the tube.

Temperature sensors are not the only transducers which can be directly digitized. Strain gauge transducers account for a large class of pressure and force measurements. Typically, a strain gauge bridge-based transducer produces 3mV of full-scale output per volt of bridge drive. Figure 6 shows a way to directly digitize a strain gauge bridge's output to 10-bit accuracy. For a 7.5V bridge drive, an LSB increment is 25 μ V, considerably larger than the thermocouple example but still far below conventional A/D converters. The bridge's differential output complicates the required converter input structure, but is accommodated.

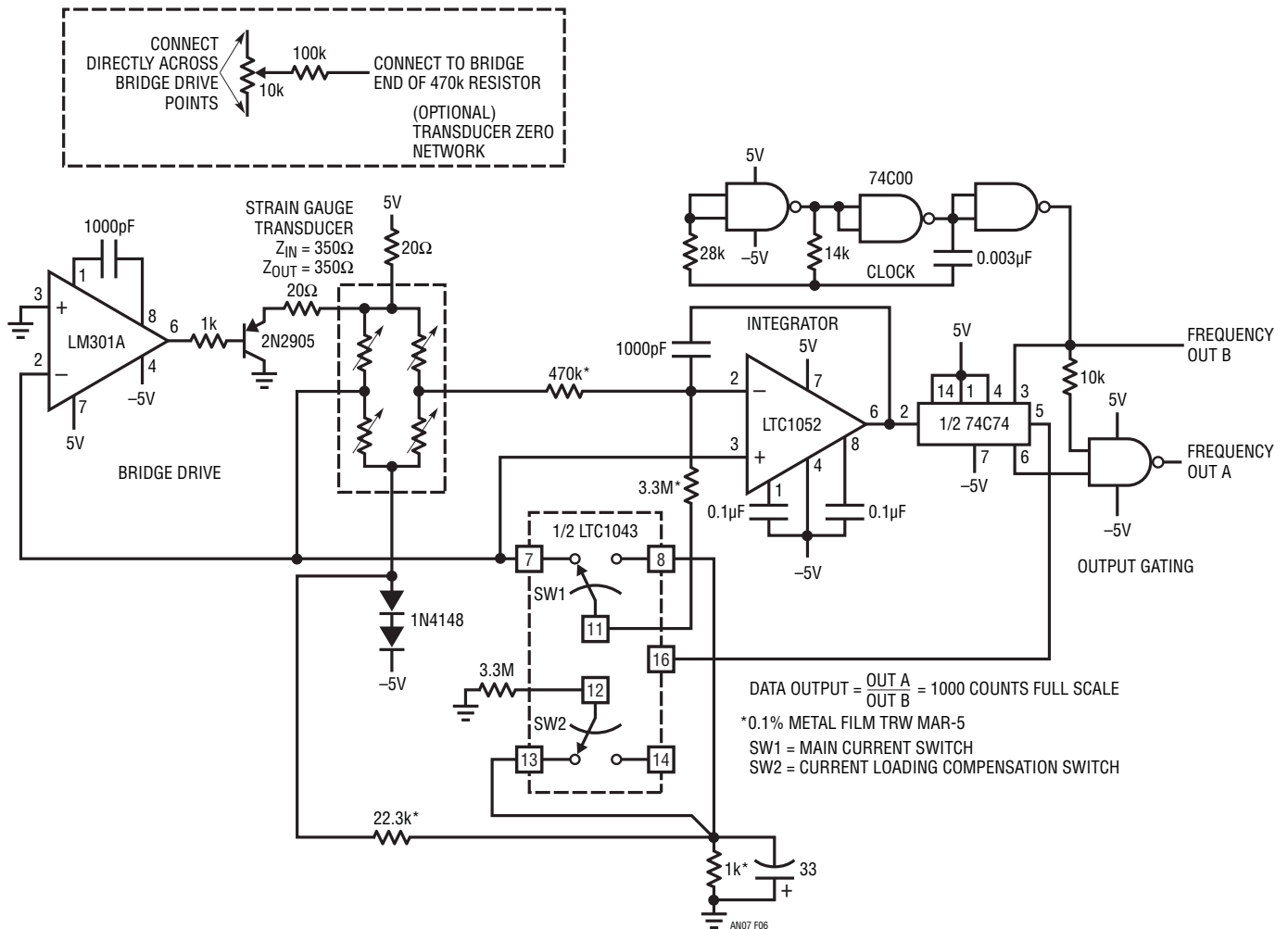


Figure 6. Strain Gauge Digitizer

A1 and the transistor provide bridge excitation. One signal output of the bridge is connected to A1's negative input. A1's positive input is at ground. A1 drives the transistor to bias the bridge at whatever voltage is required to bring its negative input to ground potential. The diode drops in the bridge's $-5V$ return line allow the transistor to force the bridge's positive end far enough to servo A1's inputs. This arrangement allows the bridge's other output to be sensed in a single-ended, ground-referred fashion. In practice, a slight error exists due to A1's offset voltage. This error is eliminated by referring the A/D converter input to A1's negative input instead of ground.

The A/D converter is made up of A2, a flip-flop and some gates. It is based on a current balancing technique. Once again, the chopper-stabilized LTC7652's $50nV/^\circ C$ input drift is required to implement the low level input A/D. Figure 7 details key A/D waveforms. Assume the flip-flop's Q output (Trace B) is low, connecting LTC1043 Pins 11 and 12 to Pins 7 and 13, respectively. The main current switch passes no current, as the $3.3M$ resistor is placed across A2's inputs. The current loading compensation switch puts a $3.3M$ value across the $1k$ divider resistor, lowering the voltage across it by 0.03% .

Under these conditions the only current into A2's summing point is from the bridge via the $470k$ resistor. This positive current forces A2's output (Trace A, Figure 7) to integrate in a negative direction. The negative ramp continues and finally passes the 74C74 flip-flop's switching threshold. At the next clock pulse (clock is Trace C), the flip-flop changes state (Trace B), causing the LTC1043 switch positions to

reverse. Pin 12 connects to Pin 14 and Pin 11 to Pin 8. In this case, the $3.3M$ resistor, controlled by the current loading compensation switch, is disconnected from the $1k$ unit, but the $3.3M$ value, controlled by the main current switch, replaces it. The 0.03% loading of the $3.3M$ resistor, combined with this switching scheme, eliminate any sag or loading effects across the $1k$ resistor during switching. The result is a quickly rising, precise current flow out of A2's summing point.

This current, scaled to be greater than the bridge's maximum output, forces A2's output movement to reverse and integrate in the positive direction. At the first clock pulse after A2's output has crossed the flip-flop's triggering threshold, switching occurs and the entire cycle repeats. Because the reference current is fixed, the flip-flop's duty cycle is solely a function of the bridge signal current into A2's summing point. Additionally, the reference current is supplied from the $22.3k-1k$ divider, which is derived from the bridge drive. Thus, the A/D's reference current varies ratiometrically with the bridge output, eliminating bridge drive variations as an error source. The flip-flop's output gates the clock, producing the "frequency output A" waveform (Trace D). The $10k$ resistor combines with the output gate's input capacitance to slightly delay the clock signal, eliminating spurious output pulses due to flip-flop delay. The circuit's data output, the ratio of output A to the clock frequency, may be extracted with counters. Because the output is expressed as a ratio, clock frequency stability is unimportant.

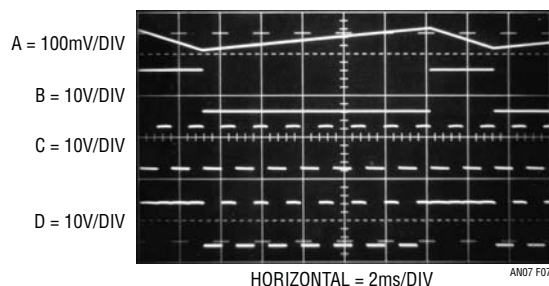


Figure 7. Strain Gauge Digitizer Waveforms

Application Note 7

Several subtle factors are critical in setting up and using this circuit. The 470k input resistor at A2 has been selected to produce less than 1LSB loading error on the strain gauge bridge. The bridge receives only about 7.5V of drive due to the deliberate resistor and diode drops in its supply lines. At 3mV output per volt of bridge drive, full-scale signal is 22.5mV. This produces a signal current of only:

$$I = \frac{0.0225V}{470k} = 48nA$$

To maintain 10-bit accuracy, leakage and amplifier bias current into A2's summing point must be less than 0.1% of this figure or:

$$I = \frac{48nV}{1000} = 48pA$$

Although A2's bias current is much lower than this, board leakage can cause trouble. At a minimum, careful layout and a clean PC board are required. The best practice is to use a Teflon stand-off for all summing point connections. The 470k and 3.3M resistors associated with A2's negative input should be placed as close as possible to the IC pin. Note also that the 3.3M current summing resistor is switched to A2's positive input when it is not sourcing current to the summing point. This seemingly unnecessary connection prevents minute stray 60Hz and noise currents from being coupled to A2's summing point when the current reference is off. Failure to utilize this connection will cause jitter in the LSB. Gain trimming of this circuit may be accomplished by varying the 22.3k value. If the particular strain gauge transducer used requires zero trimming, use the optional network shown. Over a 0°C to 70°C range the circuit will typically maintain its 10-bit output within 1LSB accuracy. The tracking errors of the starred resistors are the primary contributors to this small error.

Because of their extremely wide dynamic range, photo diodes present a difficult challenge for signal conditioning circuitry. A high quality device furnishes a linear current output over a 100dB range, requiring a 17-bit A/D converter as well as a current-to-voltage input amplifier. A common approach

employs a logarithmically responding current-to-voltage input amplifier to nonlinearly compress the photodiode's output, allowing a much lower resolution A/D converter to be used. Although this scheme saves the cost of the 17-bit A/D, it has the inconvenience of a nonlinear output. Also, logarithmic amplifiers respond relatively slowly, which may be detrimental in some photometric measurements. Figure 8's circuit directly converts a photodiode's current output into an output frequency with 100dB of dynamic range. Optical input power of 20nW to 2mW produces a linear, calibrated 20Hz-to-2MHz output. Output response to input light steps is fast and cost is low.

The photodiode's output current feeds a highly modified, high frequency version of a Pease type charge pump $I \rightarrow F$ converter. Diode output current biases A1's negative input, causing its output (Trace A, Figure 9) to ramp in a negative direction. When A1's output crosses zero, C1's output (Trace B) goes low, causing the LT1009 diode bridge to bound at -3.7V. The 200pF-1.8k lead network at C1's positive input aids comparator high frequency response. C1's output going low also provides AC positive feedback to its positive input (Trace D). Additional AC positive feedback is supplied by output transistor Q3's collector (Trace C). During this interval, charge is pulled from A1's summing point via the 47pF-5pF capacitors (Trace E). This causes A1's output to move quickly positive, switching C1 after the positive feedback around it has decayed. The LT1009 diode bridge now bounds at 3.7V. The 47pF-5pF pair receives charge, A2's summing junction recovers and the entire cycle repeats at a frequency linearly related to photodiode output current. D1 and D2 compensate the bridge diodes. Diode connected Q1 compensates steering diode Q2. The diode connected transistors provide lower leakage than simple diodes. C2 provides circuit latch-up protection, necessary because of the circuit's AC-coupled feedback loop. If latch-up occurs, A1's output saturates low, causing C2's emitter-follower connected output to go high. This forces A1's output positive, initiating normal circuit action.

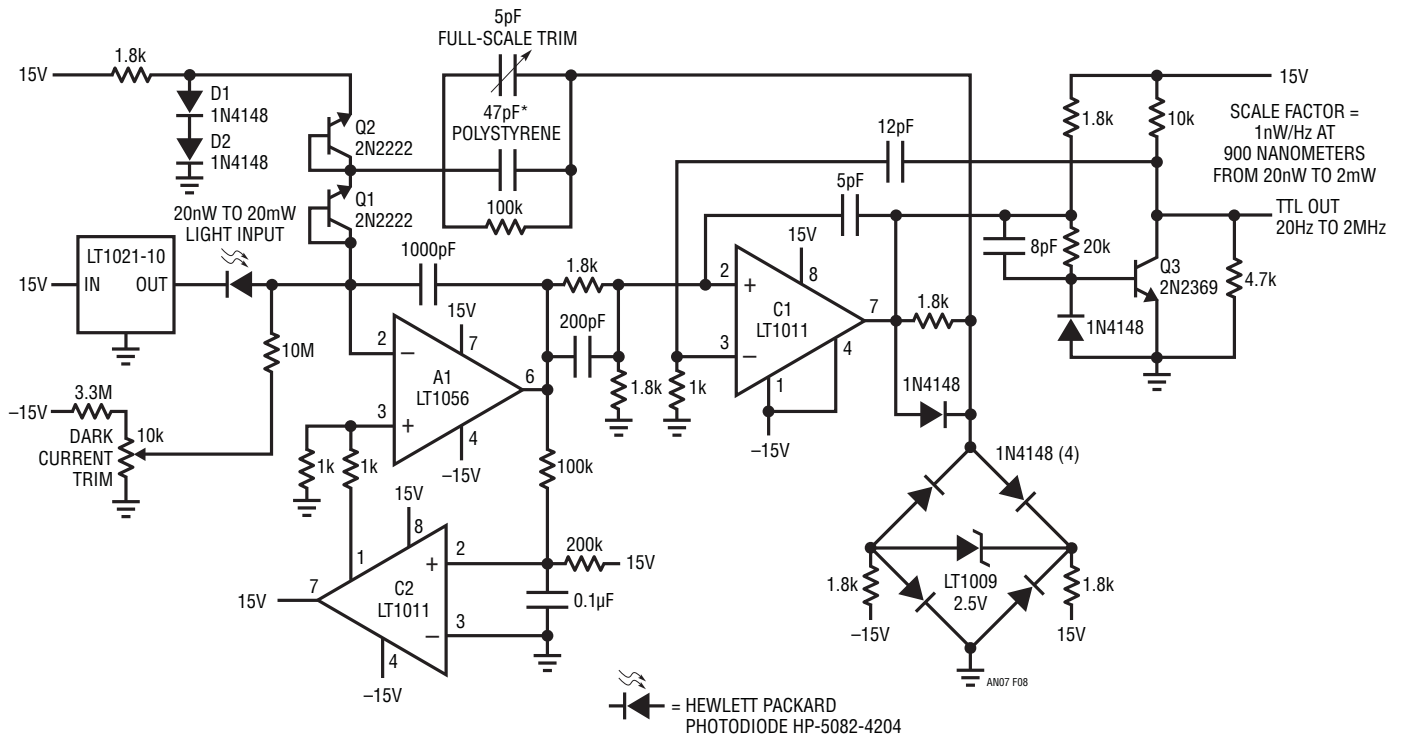


Figure 8. Photodiode Digitizer

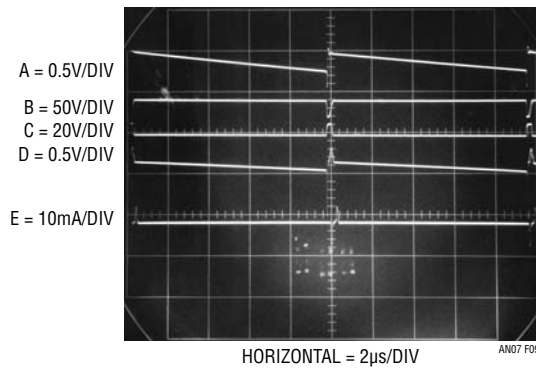


Figure 9. Photodiode Digitizer Waveforms

Application Note 7

The LT1021-10 reference biases the photodiode, providing optimum optical current response characteristics. To trim this circuit, place the photodiode in a *completely* dark environment. Trim the “dark current” adjustment so the circuit oscillates at the lowest possible frequency, typically 1Hz to 2Hz. Next, apply or electrically simulate (see manufacturer’s data sheet for light input versus output current data) a 2mW optical input. Trim the 5pF adjustment for an output frequency of 2MHz. If the adjustment is outside the range of the trimmer, alter the 47pF capacitor’s value appropriately. Once calibrated, this circuit will maintain 1% accuracy over the photodiodes’s entire 100dB range. The accuracy obtained is limited by photodiode characteristics and not the circuit. Figure 10 shows dynamic response of the circuit to a fast light pulse (Trace A, Figure 10). The frequency output settles within 1 μ s on both edges.

One of the most difficult physical parameters to transduce is relative humidity. A recently introduced humidity transducer, based on a capacitance shift versus relative humidity (RH), offers good accuracy, fast response, wide range and linear response. The transducer features a nominal 1.7pF per percent RH capacitance shift with a 500pF value at RH = 76%. It does not require temperature compensation. A significant consideration in signal conditioning this transducer is that the average voltage across the device must be zero. No net DC may pass through the transducer. Figure 11’s circuit converts the RH transducer’s capacitive shifts directly into a calibrated frequency output. The LTC1043 switched-capacitor instrumentation building block IC free runs at 150kHz. Pin 2 (Figure 12, Trace A) is alternately connected between the LT1004 negative reference and A1’s summing junction. The 1 μ F-22M Ω combination associated with the RH transducer ensures the device’s required pure AC biasing.

When Pin 2 is connected to Pin 6, the transducer receives a negative charge. When the LTC1043’s internal clock switches, Pin 2 is tied to Pin 5, depositing all of the transducer’s charge into A1’s summing point. A1’s input (Trace B), just faintly visible, shows transducer current, while Trace C is A1’s output. A1, an integrator, ramps up in stepped fashion as successive discrete packets of charge are deposited into its summing point. Concurrent with this action, a second set of LTC1043 switches (Pins 7, 8, 11, 12, 13 and 14) works to synchronously transfer a fixed amount of charge of opposing polarity into A1’s summing junction. The amount of fixed charge is set to cancel the sensor offset (e.g., 0% RH does not extrapolate to 0pF sensor capacitance). Thus, the slope of the stepped ramp at A1’s output is a function of the sensor’s value minus its offset term. A1 continues to ramp positive until it equals the voltage at C1’s negative input. This triggers C1’s output high (Trace D). AC positive feedback holds C1’s output high long enough for the 2N4393 FET to completely discharge A1’s feedback capacitor. A1’s output drops to zero and the entire cycle repeats. The frequency of repetition is a function of the RH transducer’s capacitance. C1’s input voltage is derived from the LT1004 reference. LTC1044 Pins 3, 18 and 15 and the 330pF value form a simple charge pump which biases A2’s summing point. A2’s output assumes whatever value is required to maintain its summing point at zero. The 0.22 μ F capacitor integrates A2’s response to DC, while the feedback resistors establish the operating point. Because A2’s output voltage determines ramp height, its feedback resistor’s value sets the circuit’s gain slope. Traces E, F and G, time and amplitude expansions of Traces A, B and C, permit a detailed look at the effects of the transducer’s charge dumping on A1’s output ramp.

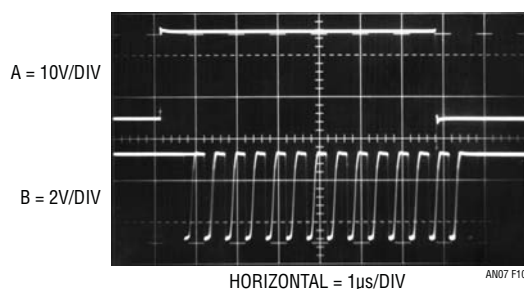


Figure 10. Step Response of Photodiode Digitizer

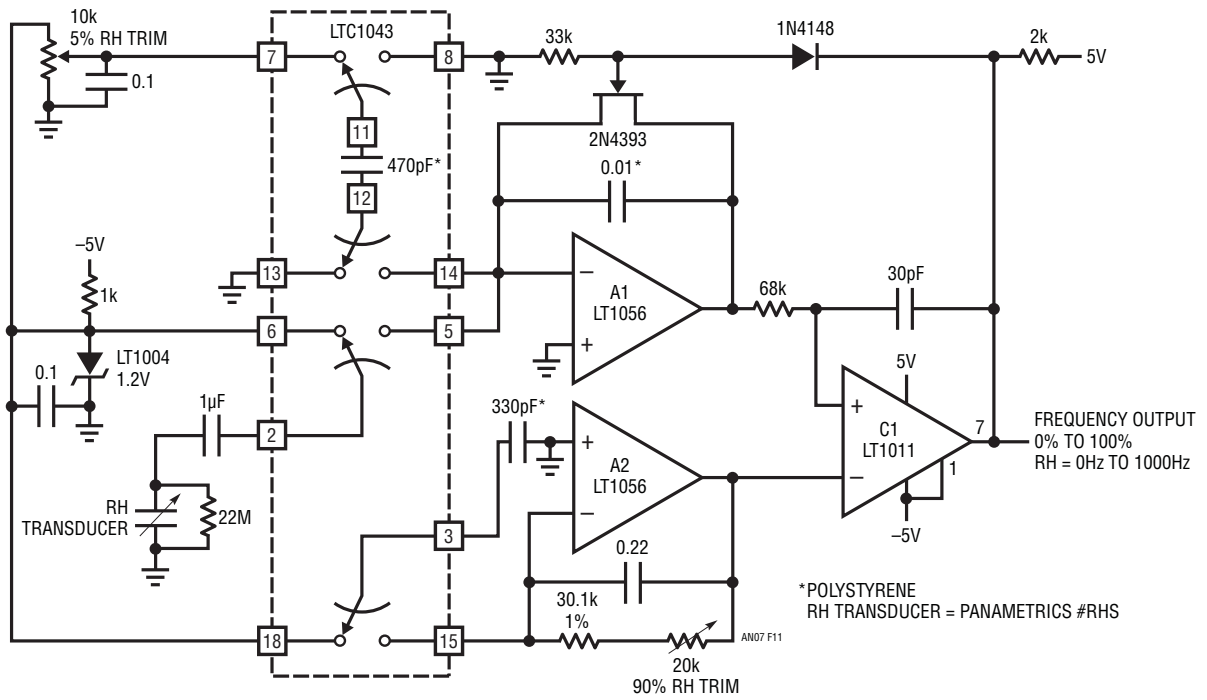


Figure 11. Humidity-to-Frequency Converter

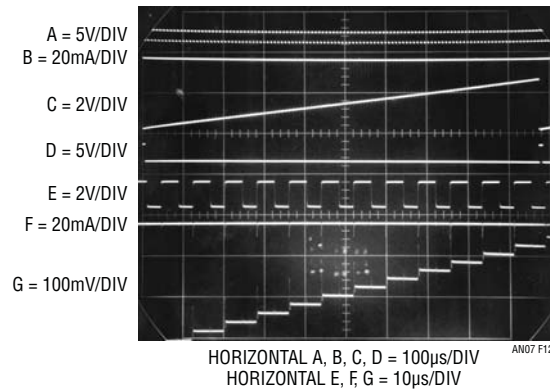


Figure 12. Humidity-to-Frequency Converter Waveforms

Application Note 7

Circuit temperature dependence is low because the 330pF and 0.01 μ F polystyrene capacitors' (both gain terms) -120 ppm drifts ratiometrically cancel. Further ratiometric error cancellation occurs because the transducer's charge source and A2's output voltage are both derived from the LT1004 reference. The sole uncompensated term in the circuit is the 470pF capacitor which supplies the offsetting charge. Its -120 ppm/ $^{\circ}$ C drift is well below the transducer's 2% accuracy specification, and circuit temperature independence is assured.

To calibrate this circuit, place the transducer in a 5% RH environment and adjust the 5% trim for 50Hz output. Next place the transducer in a 90% RH environment and adjust the 90% trim for a 900Hz output. Repeat this procedure until both points are fixed. Relative humidity accuracy will be 2% over the 5% to 90% RH range. If RH standards are not available, the circuit may be approximately calibrated against using fixed capacitors in place of the sensor. Ideal values are 5% RH = 379.3pF and 90% = 523.8pF. Note that these values assume an ideal sensor. An actual device may depart from them by as much as 10%.

Another frequently required physical parameter is level. Level transducers which measure angle from ideal level are employed in road construction, machine tools, inertial navigation systems and other applications requiring a gravity reference. One of the most elegantly simple level transducers is a small tube nearly filled with a partially conductive liquid. Figure 13 shows such a device. If the tube is level with respect to gravity, the bubble resides in the tube's center and the electrode resistances to common are identical. As the tube shifts away from level, the resistances increase and decrease proportionally. By controlling the tube's shape at manufacture, it is possible to obtain a linear output signal when the transducer is incorporated into a bridge circuit.

Transducers of this type must be excited with an AC waveform to avoid damage to the partially conductive liquid inside the tube. Signal conditioning involves generating this excitation as well as extracting angle information and polarity determination (e.g., which side of level the tube is on). Figure 14 shows a circuit which does this, directly producing a calibrated frequency output corresponding to level. A sign bit, also supplied at the output, gives polarity information.

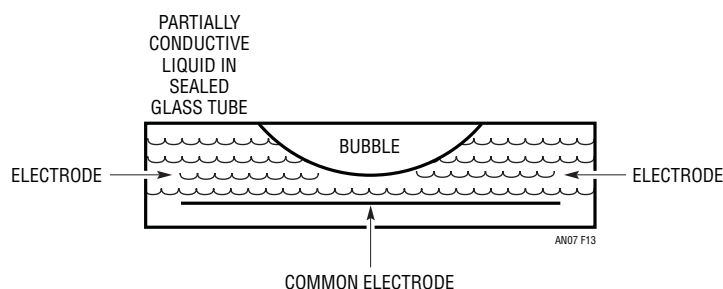


Figure 13. Bubble-Based Level Transducer

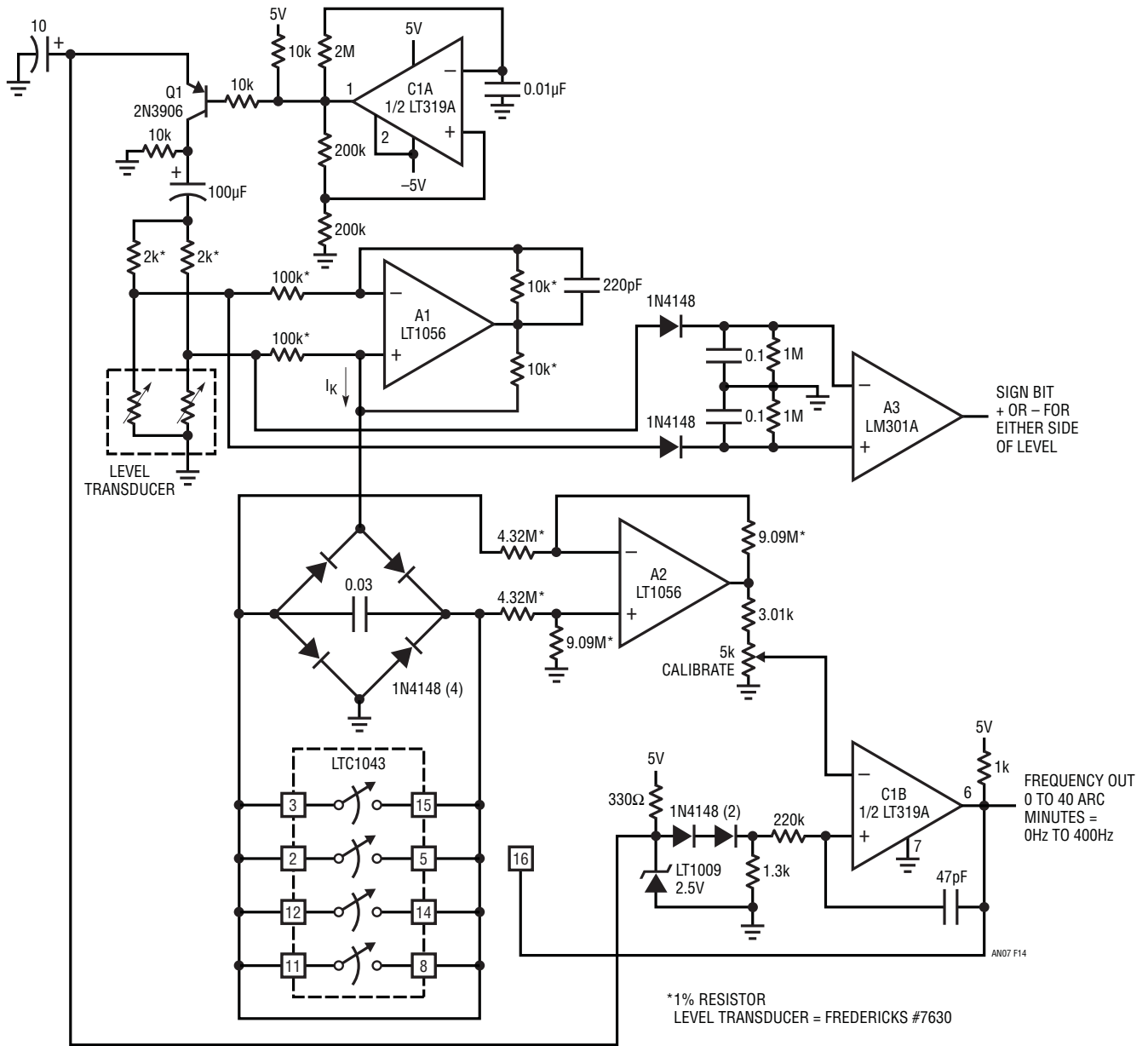


Figure 14. Level Transducer Digitizer

Application Note 7

The level transducer is configured with a pair of 2k resistors to form a bridge. The required AC bridge excitation is developed at C1A, which is configured as a multivibrator. C1 biases Q1, which switches the LT1009's 2.5V potential through the 100 μ F capacitor to provide the AC bridge drive. The bridge differential output AC signal is converted to a current by A1, operating as a Howland current pump. This current, whose polarity reverses as bridge drive polarity switches, is rectified by the diode bridge. Thus, the 0.03 μ F capacitor receives unipolar charge. A2, running at a differential gain of 2, senses the voltage across the capacitor and presents its single-ended output to C1B. When the voltage across the 0.03 μ F capacitor becomes high enough, C1B's output goes high, turning on the paralleled sections of the LTC1043 switch. This discharges the capacitor. The 47pF capacitor provides enough AC feedback around C1B to allow a complete zero reset for the capacitor. When the AC feedback ceases, C1B's output goes low and the LTC1043 switch goes off. The 0.03 μ F unit again receives constant-current charging and the entire cycle repeats. The frequency of this oscillation is determined by the magnitude of the constant current delivered to the bridge-capacitor configuration. This current's magnitude is determined by the transducer bridge's offset, which is level related.

Figure 15 shows circuit waveforms. Trace A is the AC bridge drive, while Trace B is A1's output. Observe that when the bridge drive changes polarity, A1's output flips sign rapidly to maintain a constant current into the bridge-capacitor configuration. A2's output (Trace C) is a unipolar, ground-referred ramp. Trace D is C1B's output pulse and the circuit's output. The diodes at C1B's positive input

provide temperature compensation for the sensor's positive tempco, allowing C1B's trip voltage to ratiometrically track bridge output over temperature.

A3, operating open loop, determines polarity by comparing the rectified and filtered bridge output signals with respect to ground.

To calibrate this circuit, place the level transducer at a known 40 arc-minute angle and adjust the 5k trimmer at C1B for a 400Hz output. Circuit accuracy is limited by the transducer to about 2.5%.

The final example concerns direct digitization of a piezoelectric accelerometer. These transducers rely on the property of ceramic materials to produce charge when mechanically excited. In this device a mass is coupled to the ceramic element. An acceleration acting on the mass causes charge to be dispensed from the ceramic element. Sensitivity and frequency response are related to the characteristics of the ceramic used and the mechanical design of the transducer. The best way to signal condition a piezoelectric output is to unload it directly into the virtual ground of an op amp's summing point. This method provides no voltage difference between the center conductor and the shield of the coaxial cable connecting the accelerometer and the single conditioning amplifier. This eliminates cable capacitance as a parasitic term, an important consideration in any charge output transducer. Because the accelerometer produces AC outputs, a direct digitization of its output must produce a sign bit as well as amplitude data.

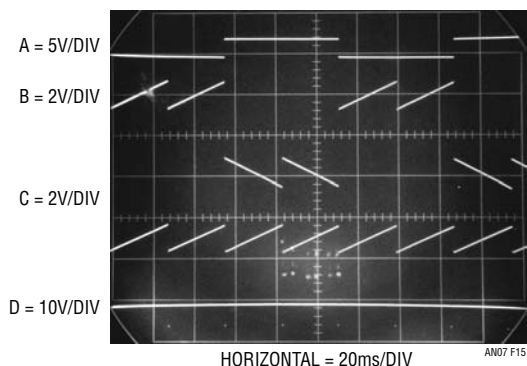


Figure 15. Level Transducer Digitizer Waveforms

Application Note 7

This circuit constitutes an I→F converter which responds to AC inputs. If the square wave source is replaced with a piezoelectric accelerometer, direct digitization results. Figure 18 shows circuit response when an acceleration (Trace A), in this case a damped sinusoid, is applied to the transducer. The sign bit (Trace B) keeps track of acceleration polarity, while the frequency output supplies amplitude data. Observe the drop in output frequency

as the input waveform damps. A monitoring processor, sampling the sign and frequency waveforms faster than twice the highest acceleration frequency of interest, can extract desired acceleration waveform data. To trim the circuit, apply a known amplitude acceleration and adjust the 1MΩ gain trim at C2. Alternately, the accelerometer may be electrically simulated (see manufacturer's data sheet for scale factors).

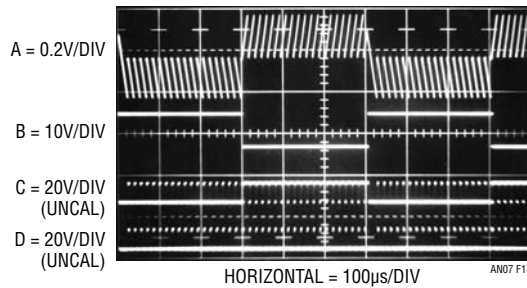


Figure 17. Accelerometer Digitizer Waveforms with Square Wave Test Drive

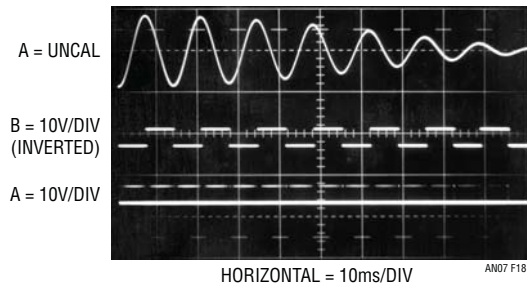


Figure 18. Accelerometer Digitizer Response

Power Conditioning Techniques for Batteries

Jim Williams

Declining power requirements for circuitry have made battery operation desirable and common. In many circumstances the battery voltage may be applied directly to circuitry with no special considerations. Other situations require some form of battery power conditioning to supply necessary voltages. At present, most IC regulators are not suitable for battery regulation because of high quiescent current and/or inability to operate at low input voltages. In particular, some switching regulators consume 20mA, many times the total power drain of some low power systems.

Designing battery regulator circuitry involves numerous considerations including efficiency, power output, battery life, circuit complexity, PC board space and cost.

Various linear and switching regulation techniques are applicable, with the best approach determined by specific requirements. Most circuit types provide DC outputs, although AC is sometimes required. General classes of regulators include voltage inverters, step-down circuits and step-up converters.

Negative Voltage Generators

Generating a negative voltage is a common requirement. Figure 1 shows a simple way to do this. The LTC1044 switched-capacitor voltage converter's internal switches synchronously transfer charge from C1 to C2, the output capacitor. When SW1 is closed, C1 charges to 9V. When SW1 opens, SW2 closes, charging C2, which assumes a negative potential with respect to ground. Continuous clocking

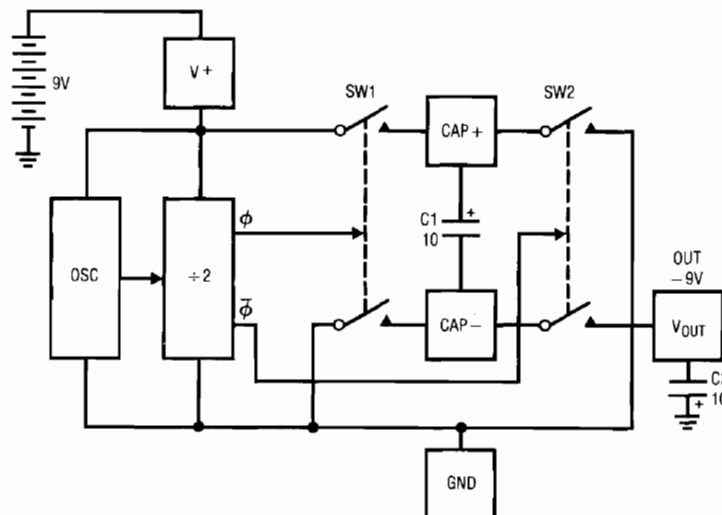


Figure 1. Negative Voltage Generator

Application Note 8

keeps V_{OUT} at DC. Due to finite output impedance, loading the output causes a drop in voltage. Figure 2 plots output voltage deviation versus load current. In low current applications or where regulation is not critical, this circuit is adequate. To improve regulation, it is necessary to decrease output impedance. Figure 3 encloses the LTC1044 within the LM10's feedback loop. Because of the LTC1044's voltage inversion, the loop is closed at the op amp's positive input. The voltage converter's losses are compensated by increased drive from the LM10. The $0.1\mu\text{F}$ capacitor stabilizes the loop and the $47\mu\text{F}$ unit keeps LM10 output impedance low at the LTC1044's switching frequency. LM10 output swing restrictions limit circuit output to 8.5V. Output regulation, plotted in Figure 2, improves upon Figure 1's basic circuit.

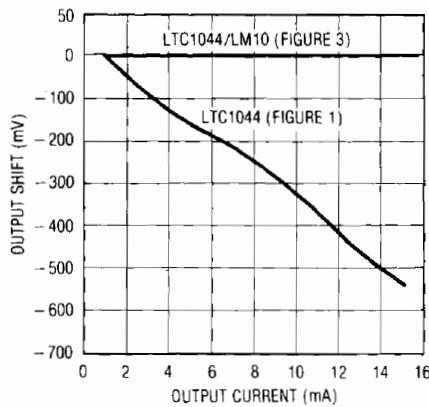


Figure 2

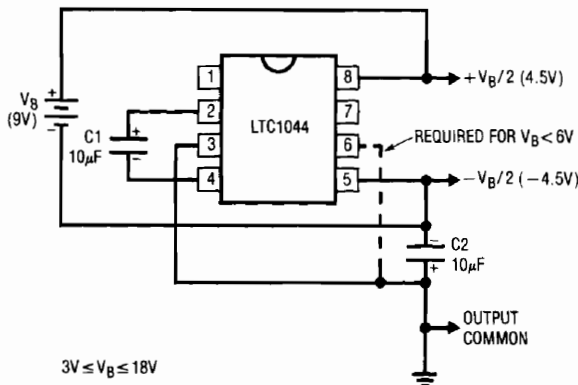


Figure 4. Battery Splitter

Battery Splitter

A common need in many systems is to obtain positive and negative supplies from a single battery. Where current requirements are small, the circuit shown in Figure 4 is a simple solution. It provides symmetrical \pm output voltages, both equal to one half the input voltage. The output voltages are referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 exceeds 6V, pin 6 should also be connected to pin 3, as shown by the dashed line. Higher current requirements are served by an LT1010 buffer. The splitter circuit shown in Figure 5 can source or sink up to $\pm 150\text{mA}$ with only 5mA quiescent current. The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

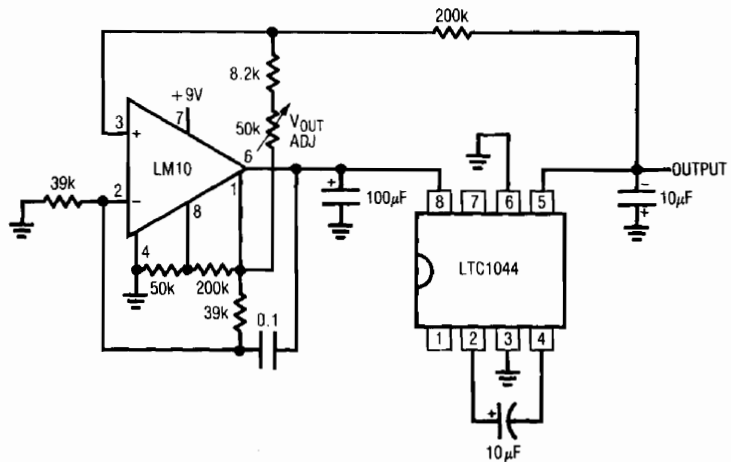


Figure 3. Regulated Negative Voltage Converter

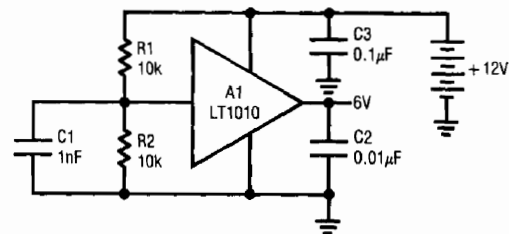


Figure 5. High Current Battery Splitter

Low Dropout Regulator

Linear regulators for batteries are a good way to get low noise, fast transient response regulation. It is desirable to achieve this performance with a very low regulator dropout voltage to maximize battery life. This can be done with PNP pass elements, but their base current never arrives at the load, decreasing efficiency. Additionally, the PNP's voltage gain complicates loop dynamics, often resulting in relatively poor transient response.

The circuit illustrated in Figure 6 offers extremely low dropout and the fast transient response of an NPN pass element. Quiescent current is $760\mu\text{A}$ and the 100mA capacity output is short circuit protected. Normally, NPN pass-based regulators have high dropout voltages because of voltage drops in the emitter-follower connected pass transistor. This 6V powered design drives the NPN pass base from a 12V source generated by the LTC1044

voltage doubler. The transistor operates as a voltage overdriven emitter-follower. The emitter's ability to follow the collector is limited only by $V_{CE\text{SAT}}$. The voltage overdriven base removes V_{BE} drop, normally the dominant loss, as a consideration. The LTC1044 doubles the battery voltage and powers the LT1013 dual op amp. A1, with 12V output capability, feedback controls the 6V collector-biased transistor. The 100Ω resistor prevents parasitic high frequency oscillation and the LT1004 serves as a reference. The output is trimmed by varying A1's feedback divider and the $0.003\mu\text{F}$ capacitor compensates the loop. A2 provides short circuit protection by forcing A1's output low if battery current exceeds 150mA. A2's low offset and high open loop gain allow using the 0.01Ω current sense resistor, reducing voltage drop losses. At 100mA output, the shunt has only 1mV across it.

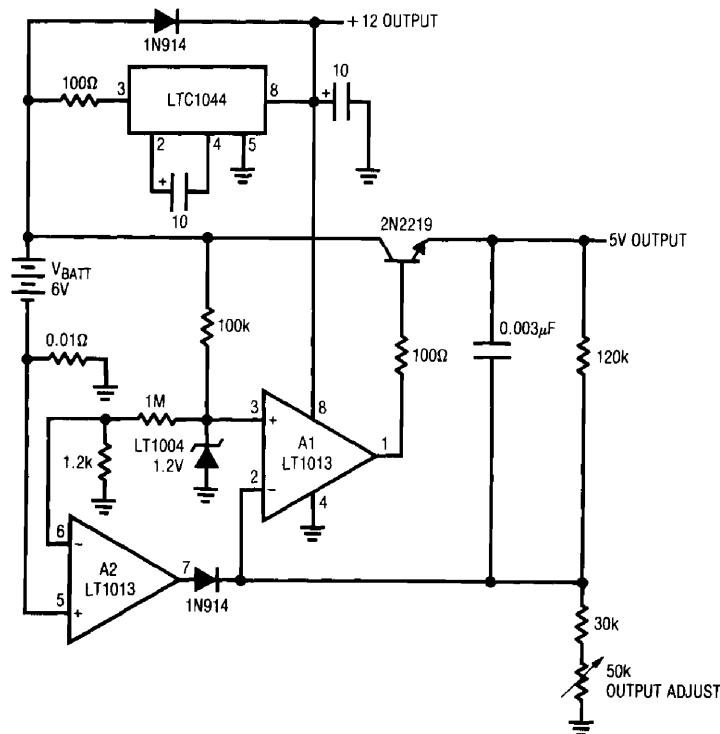


Figure 6. Low Dropout 5V Regulator

Application Note 8

Figure 7 illustrates dropout data for the regulator. At 10mA load, dropout is only 0.016V, with 0.94V occurring at 100mA loading. Transient response is shown in Figure 8. Waveform A controls an output load which is either zero or 100mA. Waveform B is the regulator's AC-coupled output. Transient response is clean and quick, with little tailing or aberration.

Low Power Switching Regulator

The low dropout linear regulator is efficient only when its input and output voltages are close. Situations requiring substantial voltage drop to achieve the desired regulated output need switching techniques to maintain good efficiency. Figure 9 shows a simple battery-powered switching regulator. It provides 5V out from a 9V source with 80%

efficiency and 50mA output capability. Assume Q1 is on. Its collector (Trace A, Figure 10) voltage rises, forcing current (Trace B) through the inductor. The output voltage (Trace C) rises, causing A1's output to rise. Q1 cuts off and the output decays through the load. The 100pF capacitor ensures clean switching. The cycle repeats when the output drops low enough for A1 to turn on Q1. The 1μF capacitor ensures low battery impedance at high frequencies, preventing "sag" during switching. Short circuit protection is as shown in Figure 6's circuit. In some applications the switching-induced noise on the regulated output may be troublesome. Figure 11 eliminates the noise by adding a low-dropout series regulator at the switching circuit's output. The switching loop's operation is similar to Figure 9 except that the voltage across the 2N5434 FET series pass element is controlled. The switching loop

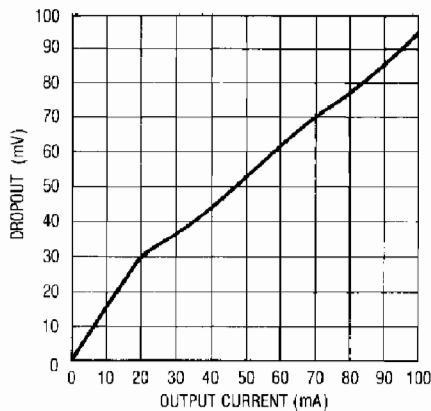


Figure 7. Dropout vs Load for Figure 6

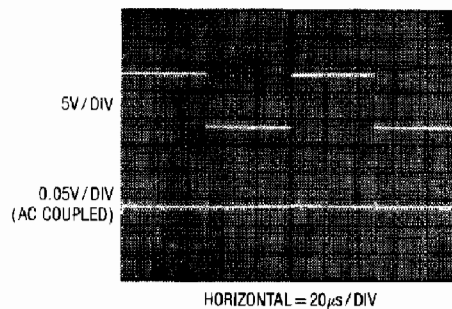


Figure 8. Transient Response of Figure 6's Circuit

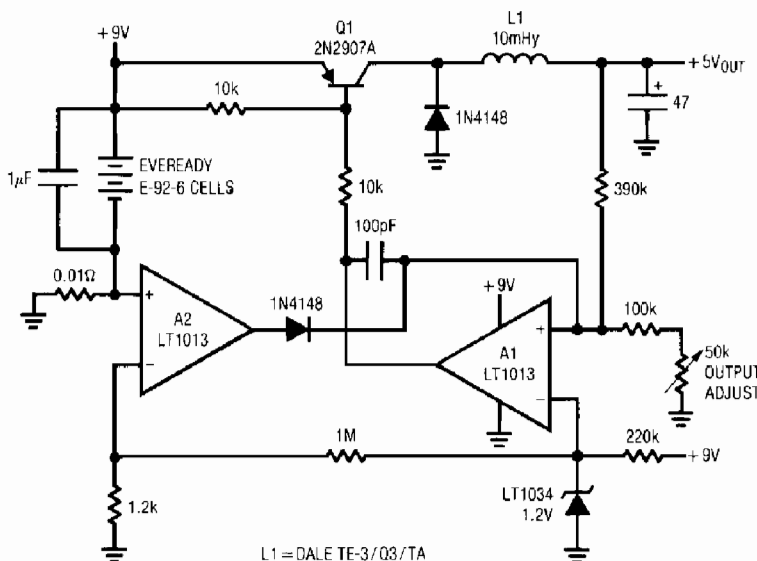


Figure 9. Low Power Switching Regulator

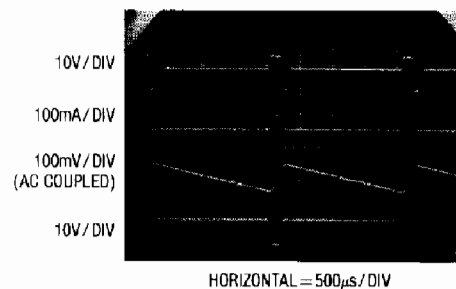


Figure 10. Figure 9's Operating Waveforms

forces this voltage to equal V_D , regardless of input or loading conditions. The FET, a low R_{ON} , low pinch-off unit, combines with A2 to form a simple, low dropout series pass regulator. The LT1004 is the reference and the 1000pF capacitor provides roll-off. This circuit will supply 25mA of noise-free, regulated power with short circuit current set by the FET's 30mA I_{DSS} . The overall 75% efficiency is not quite as good as the basic switching circuit due to the 6mW ($0.250V \times 0.025A$) dissipated in the FET.

ciency is not quite as good as the basic switching circuit due to the 6mW ($0.250V \times 0.025A$) dissipated in the FET.

High Current, "Inductorless," Switching Regulator

Figure 12 shows another high efficiency battery-driven regulator, but this circuit features a 1A output capacity.

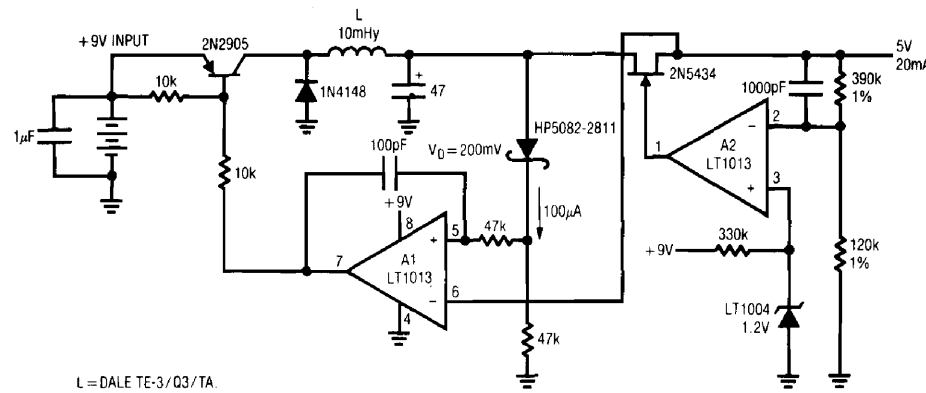


Figure 11. Switching Preregulated Linear Regulator

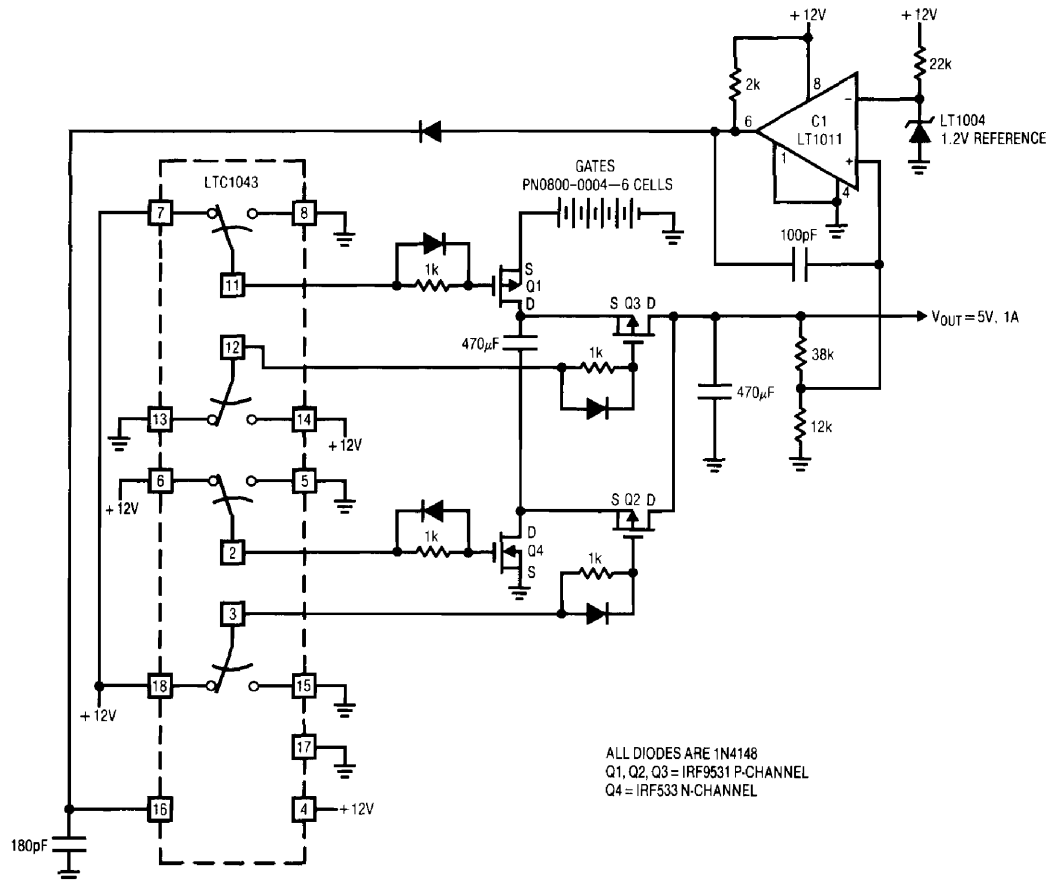


Figure 12. "Inductorless" High Current Switching Regulator

Application Note 8

Additionally, it does not require an inductor, an unusual feature for a switching regulator operating at this current level.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the +12V battery's current flows through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 13, are the LTC1043-supplied drives to Q3 and Q4 respectively. Q1 and Q2 receive similar drive from pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the output (Trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043 oscillator pin (Trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel

phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF capacitor provides sharp transitions. The loop regulates the output to 5V by feedback-controlling the turn-off point of the series phase. The circuit constitutes a large scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

Voltage Step-Up Circuits—Simple Voltage Doubler

All of the previous circuits condition battery output to a lower voltage. Many applications call for a voltage above the battery output. Figure 14 shows a simple way to double available battery voltage using the LTC1044 switched-capacitor voltage converter. As shown, the IC functions in similar fashion to Figure 12's circuit, at greatly reduced power levels. This circuit will drive low power 74-CMOS loads (V_{SUPPLY} 3V-15V) for extended periods of time from two small cells. Efficiency exceeds 90% for load currents below 1.75mA. Figure 15 plots output voltage versus loading.

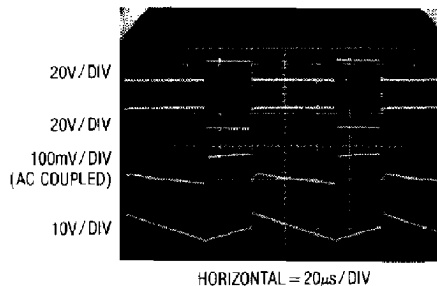


Figure 13. "Inductorless" Regulator's Waveforms

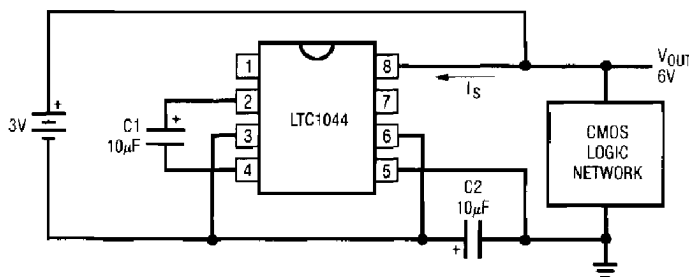


Figure 14. Voltage Doubler

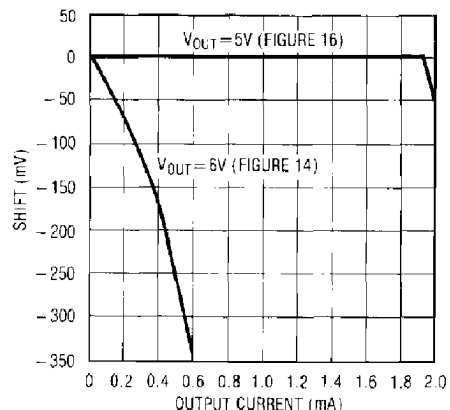


Figure 15

Figure 16 addresses Figure 14's regulation fall-off with increasing current. As in Figure 12, feedback techniques are used to compensate for the voltage converter's output impedance. The LTC1044 is connected in a voltage doubler mode, with the $10\mu\text{F}$ value used to pump up the $100\mu\text{F}$ capacitor. Q1 and Q2 serve as a bidirectional switch, allowing the pump up action to be interrupted. The circuit regulates by using an LM10 op amp reference to control the switch. When output voltage decays low enough (Figure 17, Trace A), the LM10's reference ampli-

fier swings high (Trace B), driving the op amp negative (Trace C) and both transistors come on. This allows the LTC1044 to pump charge to the $100\mu\text{F}$ capacitor. For each charge cycle, the output takes a voltage step. When the output steps high enough, the LM10 switches and the cycle repeats. Repetition rate is load dependent, with typical values of 1Hz-400Hz. Response hysteresis is set by the loop's gain-bandwidth to 40mV. The feedback network fixes the 5V output within 0.025V for loads up to 2mA (plotted in Figure 15).

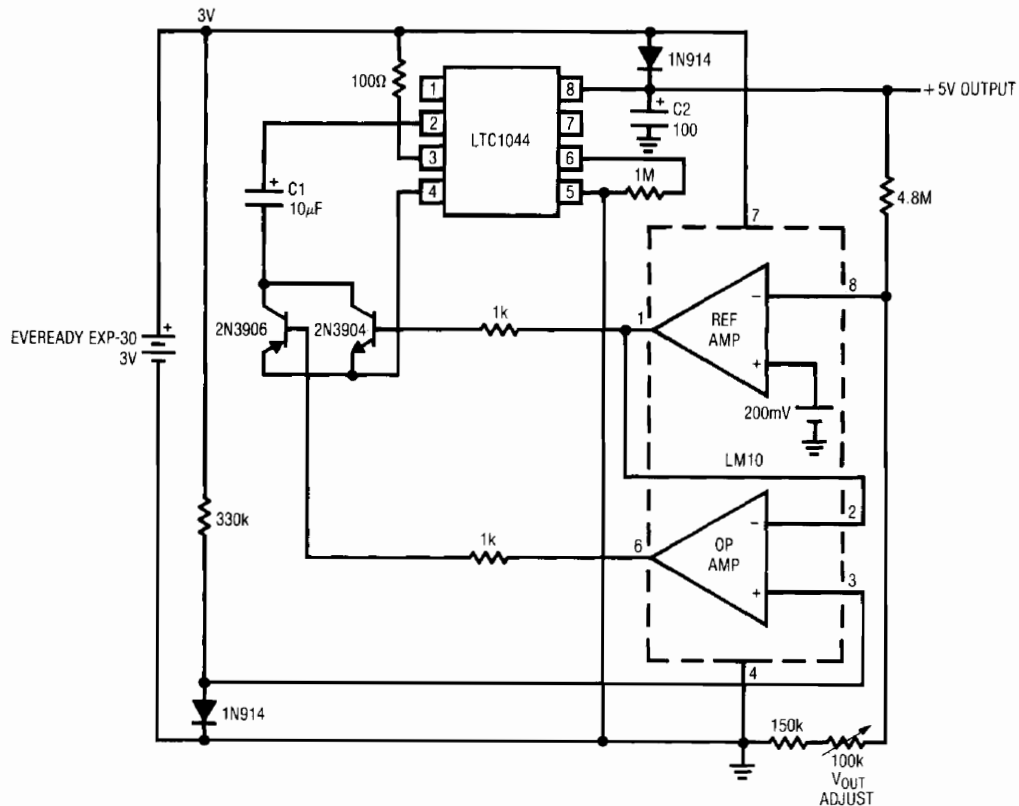


Figure 16. Regulated Voltage Up Converter

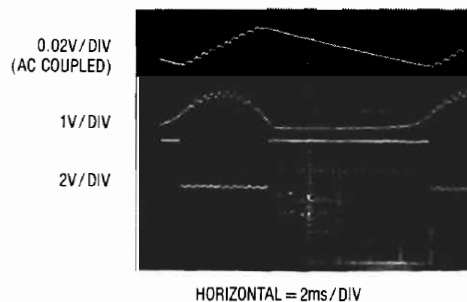


Figure 17. Up Converter's Waveforms

Application Note 8

The circuit in Figure 18 is conceptually similar, but uses a transformer to get greater voltage gain. This allows a 5V output from a single 1.5V cell. Q2, Q3 and T1 form a self-oscillating DC-DC converter, controlled by the Q1 switch. As in Figure 16, an LM10 closes feedback around this battery step-up converter. With only 1.5V at the input, particular attention must be paid to switch saturation losses. The Germanium transistors specified have under 50mV drop, less than silicon types. Germanium output diodes also contribute low forward drop losses. The 0.004 μ F capacitor sets hysteresis at 20mV, preventing erratic loop dynamics. An RC damper in T1's primary

eliminates parasitic high frequency oscillation modes. Figure 19 shows operation, with Q1's collector (Trace A) going high when circuit output voltage (Trace D) falls below the loop setpoint. Traces B and C are the LM10 output and Q2's collector, respectively. Note that the output's ramp steps up in similar fashion to Figure 16's capacitively-driven circuit. As with Figure 16, loop oscillation frequency is directly load dependent, with typical values of 1Hz-250Hz. This circuit will supply a 5V, 150 μ A load (about 25 CMOS SSI ICs) for 3000 hours from a single 1.5V "D" battery.

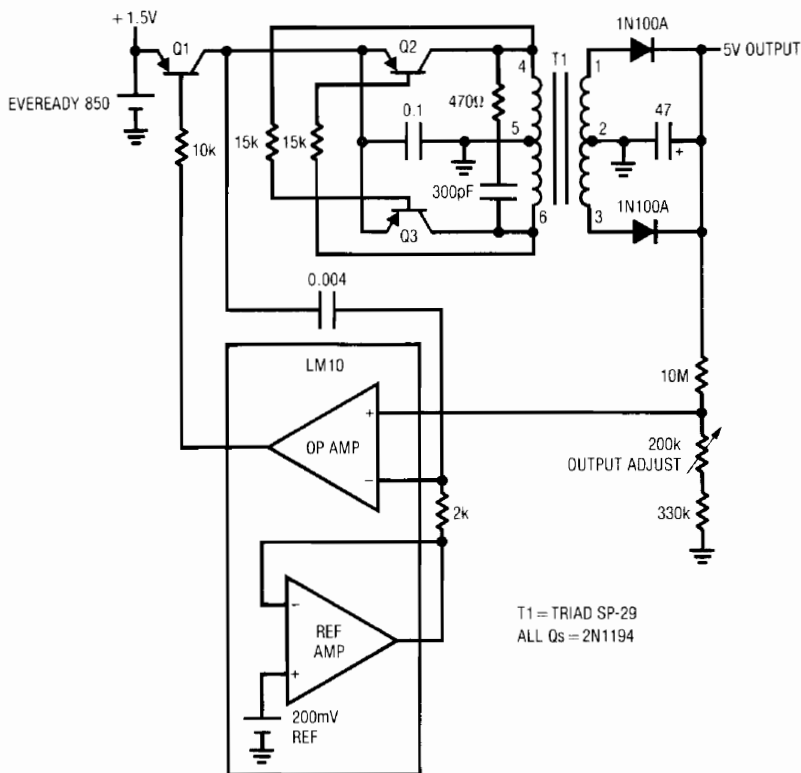


Figure 18. Single Cell Up Converter

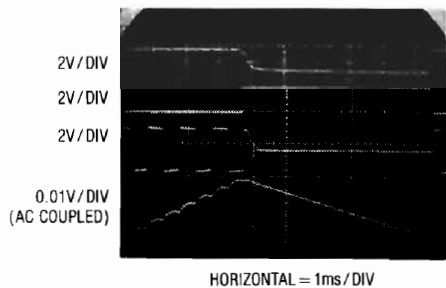


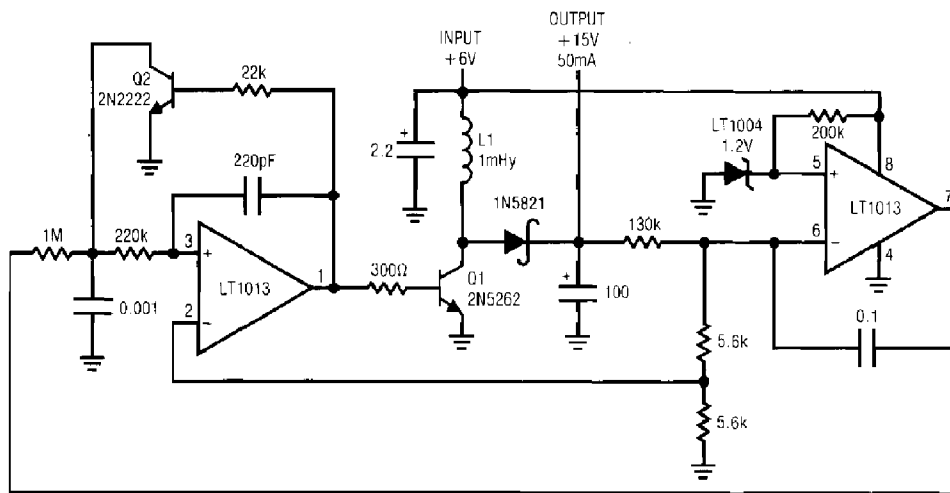
Figure 19. Figure 18's Waveforms

Regulated, 15V_{OUT}, 6V Driven Converter

Figure 20 shows a 15V output converter which delivers up to 50mA from a 6V battery. Efficiency is 78%. This flyback class converter functions by feedback-controlling the frequency of inductive flyback events. The inductor's output, rectified and filtered to DC, biases the feedback loop to establish a stable output. If the converter's output is below the loop setpoint, A2's inputs unbalance and current is fed through the 1MΩ resistor at A1. This ramps the 1000pF value positive (Trace A, Figure 21). When this ramp exceeds the 0.5V potential at A1's positive input, the amplifier switches high (Trace B). Q2 comes on, discharging the capacitor to ground. Simultaneously, regenerative feedback through the 220pF value causes a positive-going pulse at A1's positive input (Trace C), sustaining A1's positive output. Q1 comes on, allowing inductor (L1) current (Trace D) to flow. When A1's feedback pulse

decays, its output goes low, turning off Q1. Q1's collector (Trace E) is pulled high by the inductor's flyback and the energy is stored in the 100μF capacitor. The capacitor's voltage, which is the circuit output, is sampled by A2 to close a loop around the A1-Q1 combination. This loop forces A1 to oscillate at whatever frequency is required to maintain the 15V output. A1's fixed width output pulse prevents L1 from ever saturating, preventing destructive Q1 currents. The 0.1μF capacitor at A2 furnishes stable loop compensation, with the LT1004 serving as a reference. Regulation is within 0.05% over a wide range of output loads and temperature coefficient is typically 50ppm/°C.

The relatively high voltage-high power output of this circuit suits mixed linear-digital systems requirements well.



L1 = AIE-VERNITRON 24-104
78% EFFICIENCY

Figure 20. +6V-to-+15V Converter

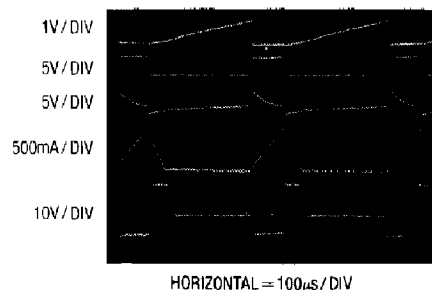


Figure 21. Figure 20's Waveforms

Application Note 8

Bipolar Output Flyback Converter

Figure 22 shows a way to obtain positive and negative 15V outputs from a single inductor. The circuit works by alternately determining which end of the inductor is allowed to flyback. The resultant positive and negative peaks are rectified, stored and regulated to produce a bipolar output. The 30kHz clock drives the 74C74 flip-flop, producing a square wave at Q1 (Trace A, Figure 23).

This waveform is fed to the 74C00 gate network. The RC networks prevent unwanted pulses due to flip-flop delay. G2 and G3's outputs appear as Traces B and C, respectively, and bias Q1 and Q2. The logic alternately turns Q1

and Q2 off when the inductor flies back. Although inductor drive current (Trace D) always flows in the same direction, the alternate switching allows positive and negative flyback action at the transistor's collectors. Trace E shows Q1's collector and Trace F is Q2's output. The ringing, due to incomplete damping, is common at low power converter outputs and is not deleterious to circuit operation. The LT1013 dual op amp and the FETs form a dual low dropout $\pm 15V$ regulator with 30mA output capability. These mirror image circuits function similarly to the one shown in Figure 11.

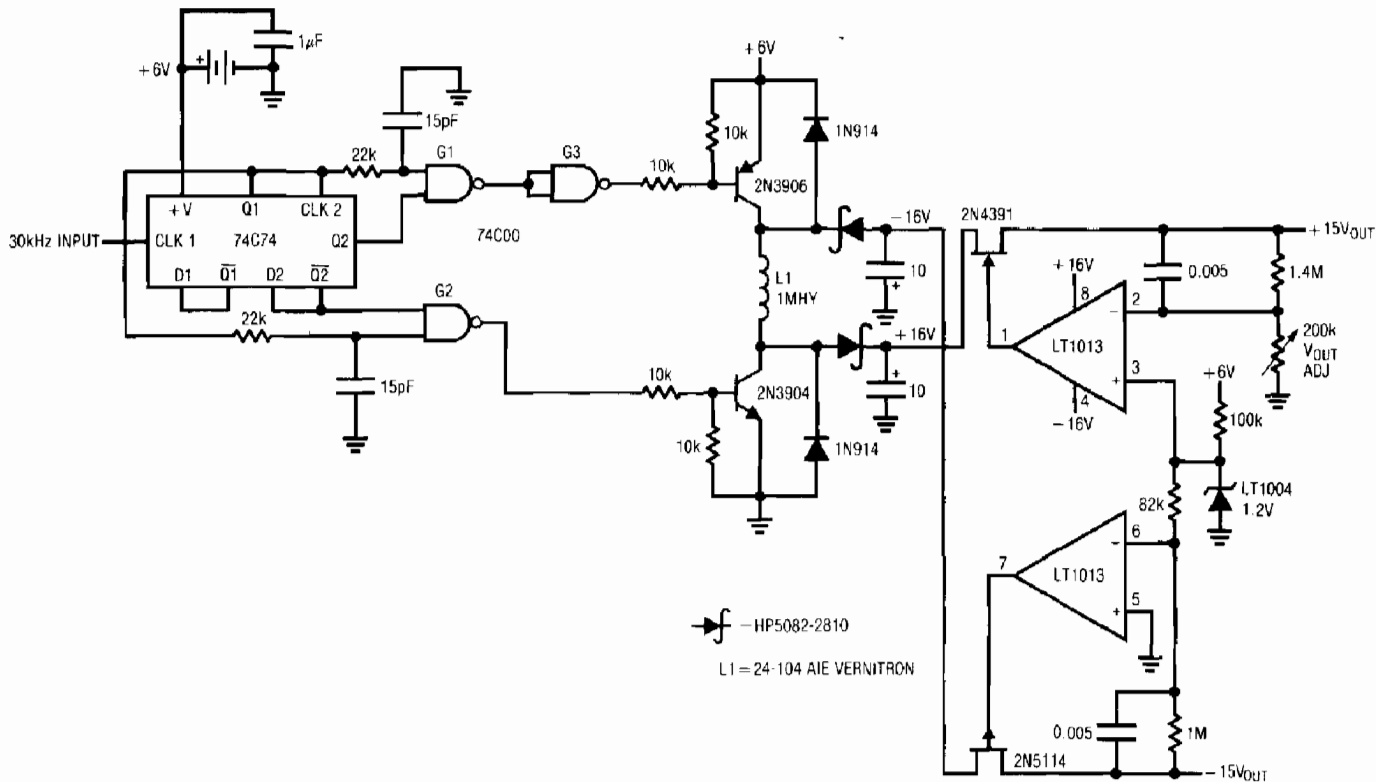


Figure 22. Single Inductor, Dual Polarity Regulator

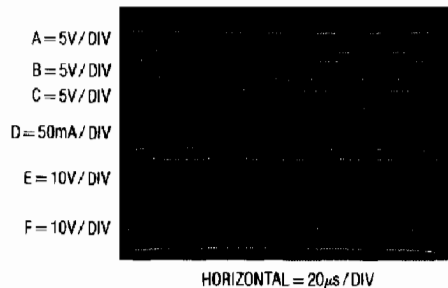


Figure 23. Figure 22's Waveforms

Application Considerations and Circuits for a New Chopper-Stabilized Op Amp

Jim Williams

A great deal of progress has been made in op amp DC characteristics. Carefully executed designs currently available provide sub-microvolt $V_{OS} \Delta T$ drift, low bias currents and open-loop gains exceeding one million. Considerable design and processing advances were required to achieve these specifications. Because of this, it is interesting to note that amplifiers with even better DC specification were available in 1963 (Philbrick Researches Model SP656). Although these modular amplifiers were large and expensive ($\approx 3" \times 2" \times 1.5"$ at \$195.00 1963 dollars) by modern standards, their DC performance anticipated today's best monolithic amplifiers while using relatively primitive components. This was accomplished by employing chopper-stabilization techniques (see Box "Choppers, Chopper-Stabilization and the LTC[®]1052") instead of the more common DC-differential stage approach.

The chopper-stabilized approach, developed by E. A. Goldberg in 1948, uses the amplifier's input to amplitude modulate an AC carrier. This carrier, amplified and synchronously demodulated back to DC, furnishes the amplifier's

output. Because the DC input is translated to and amplified as an AC signal, the amplifier's DC terms have no effect on overall drift. This is the reason chopper-stabilized amplifiers are able to achieve significantly lower time and temperature drifts than classic differential types. Additionally, the AC processing of the signal aids low frequency amplifier noise performance and eliminates many of the careful design and layout procedures necessary in a classic differential approach. The most significant trade-off is increased complexity. The chopping circuitry and sampled data operation of these amplifiers require significant attention for good results. Additionally, the AC dynamics of chopper-stabilized amplifiers are complex if bandwidths greater than the chopping carrier frequency are required.

The LTC1052 is a third generation monolithic chopper-stabilized amplifier. As the table in Figure 1 shows, it is significantly better than previous monolithic chopper-stabilized amplifiers in several areas. For comparison purposes,

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PARAMETER	LTC1052 CHOPPER- STABILIZED	ICL7652 CHOPPER- STABILIZED	HA2904/5 CHOPPER- STABILIZED	AD547 FET	LM11 LOW I_B BIPOLAR	LT1012 LOW I_B BIPOLAR
$E_{OS} - 25^\circ C$	$\pm 5\mu V$	$\pm 5\mu V$	$\pm 50\mu V$	$\pm 250\mu V$	$\pm 300\mu V$	$\pm 35\mu V$
$E_{OS} \Delta T/^\circ C$	$0.05\mu V/^\circ C$	$0.05\mu V/^\circ C$	$0.4\mu V/^\circ C$	$1\mu V/^\circ C$	$3\mu V/^\circ C$	$1.5\mu V/^\circ C$
Noise (1Hz BW)	$0.5\mu V_{p-p}$ Typ	$0.2\mu V_{p-p}$ Typ*	Specified as $900nV/\sqrt{Hz}$ at $10Hz^{**}$	$4\mu V_{p-p}$	$6\mu V_{p-p}$	$0.5\mu V_{p-p}$
Open-Loop Gain	120dB	120dB (25°C)	5×10^8 Typ	2.5×10^5	2.5×10^5	3×10^5
Bias Current—25°C	30pA	30pA	150pA Typ	25pA	50pA	100pA
CMRR	120dB	110dB (25°C)	120dB	80dB	110dB	114dB
PSRR	120dB	110dB (25°C)	120dB	100dB	100dB	114dB
Input Common Mode Range	$V^+/-2.3V$ $V^-/+0V$	$V^+/-1.5V$ $V^-/+0.7V$	$\pm 10V$ at $\pm 15V$ Supply	$V^+/-2V$ $V^-/+3V$	$V^+/-0.5V$ $V^-/+1.5V$	$V^+/-1.5V$ $V^-/+1.5V$
Slew Rate	$4V/\mu s$	$0.5V/\mu s$	$2.5V/\mu s$	$3V/\mu s$	$0.3V/\mu s$	$0.1V/\mu s$
GBW	1MHz	0.45MHz	3MHz	1MHz	0.8MHz	0.8MHz

*Unable to verify by laboratory testing. Measured at $0.7\mu V_{p-p}$

**Measured at $5\mu V_{p-p}$ in a 1Hz bandwidth

Figure 1

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Application Note 9

conventional FET input and bias current compensated bipolar types are also listed. Noise has been a particular concern with previous monolithic chopper designs and Figure 2 is a strip chart of the LTC1052's performance at two measurement bandwidths. Additionally, the LTC1052's input common mode range includes V^- , making single supply operation more practical.

Considerable attention to DC parasitics, particularly thermal EMFs, is required if the LTC1052's ultralow drift is to be fully utilized. Any connection of dissimilar metals produces a potential which varies with the junction's temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is probably the primary source of error. Connectors, switches, relay con-

tacts, sockets, wire and even solder are all candidates for thermal EMF generation. It is relatively clear that connectors and sockets can form thermal junctions. However, it is not at all obvious that junctions of wire from different manufacturers can easily generate $200\text{nV}/^\circ\text{C}$ —four times the LTC1052's drift specification! Figure 3 shows a plot obtained for such a wire junction. Even solder can become an error term at low levels, creating a junction with copper or Kovar wires or PC traces (see Figure 4).

Minimizing thermal EMF induced errors is possible if judicious attention is given to circuit board layout. In general, it is good practice to limit the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and other potential error sources to the extent possible. In some cases this will not be possible. In these

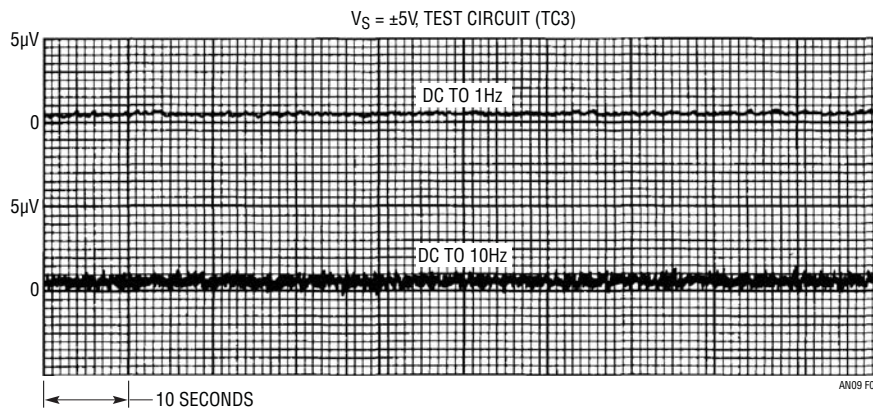


Figure 2. LTC1052 Input Noise Voltage

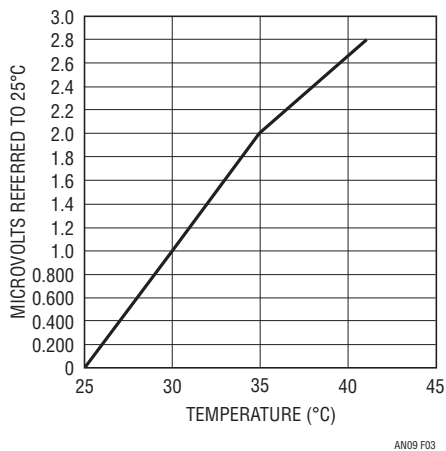


Figure 3. Thermal EMF Generated by Two Wires

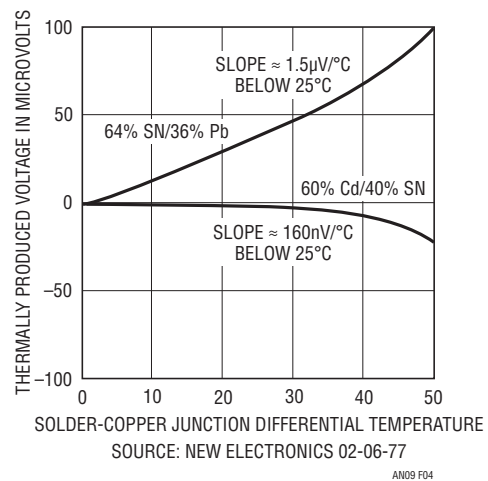


Figure 4. Solder-Copper Thermal EMFs

instances, attempt to balance the number and type of junctions in the amplifier inputs so that differential cancellation occurs. Doing this may involve deliberately creating and introducing junctions to offset unavoidable junctions. This practice, borrowed from standard lab procedures, can be quite effective in reducing thermal EMF originated drifts. Figure 5 shows a simple example where a nominally unnecessary resistor is included to promote such thermal balancing. For remote signal sources such as transducers, connectors may be unavoidable. In these cases choose a connector specified for relatively low thermal EMF activity and ensure a similarly balanced approach in routing signals through the connector, along the circuit board and to the amplifier. If some imbalance is unavoidable, deliberately introduce an intentional counterbalancing junction. In all cases maintain the junctions in close physical proximity, which will keep them at the same temperature. Avoid drafts and temperature gradients, which can introduce thermal imbalances and cause problems. Figure 6 shows the LTC1052 set up in a test circuit to measure its temperature stability. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity each input sees is also balanced because of the symmetrical connection of the resistors and their identical size. Thus, thermal EMF induced shifts are equal in phase and amplitude and cancellation occurs. Very slight air currents can still affect even this arrangement. Figure 7 shows strip

charts of output noise with the circuit covered by a small Styrofoam cup (HANDI-KUP Company Model H8-S) and with no cover in "still" air. This data illustrates why it is often prudent to enclose the LTC1052 and its attendant components inside some form of thermal baffle.

Thermal EMFs are the most likely, but not the only, potential low level error source. Electrostatic and electromagnetic shielding may be required. Power supply transformer fields are notorious sources of errors often mistakenly attributed to amplifier DC drift and noise. A transformer's magnetic field impinging on a PC trace can easily generate microvolts across that conductor in accordance with well-known magnetic theory. The amplifier cannot distinguish between this spurious signal and the desired input. Attempts to eliminate the problem by rolling off amplifier gain with a feedback capacitor may work, but often the filtered version of the undesired pickup masquerades as an unstable DC term in the output. The most direct approach is to use shielded transformers, but careful layout may be equally effective and less costly. A circuit which requires the transformer to be close by to achieve a good quality grounding scheme may be distributed by the transformer's magnetic field. An RF choke connected across a scope probe can determine the presence and relative intensity of transformer fields, aiding layout experimentation.

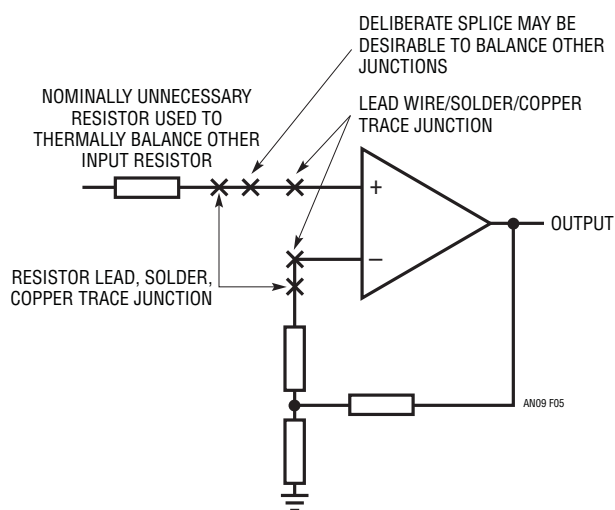


Figure 5. Typical Thermal Layout Considerations

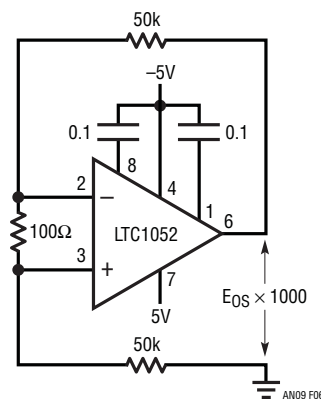


Figure 6. Recommended Drift Test Circuit

Application Note 9

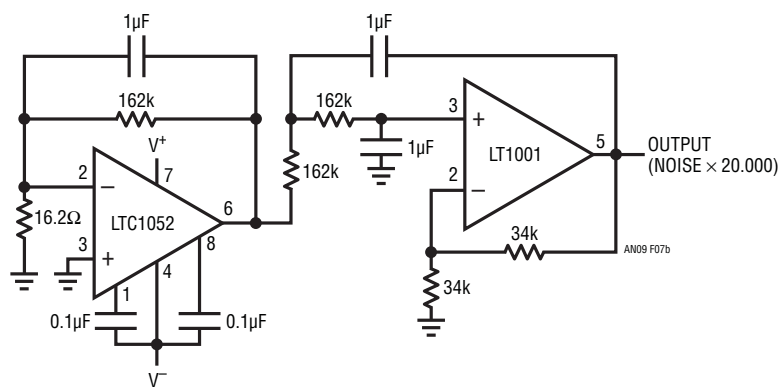
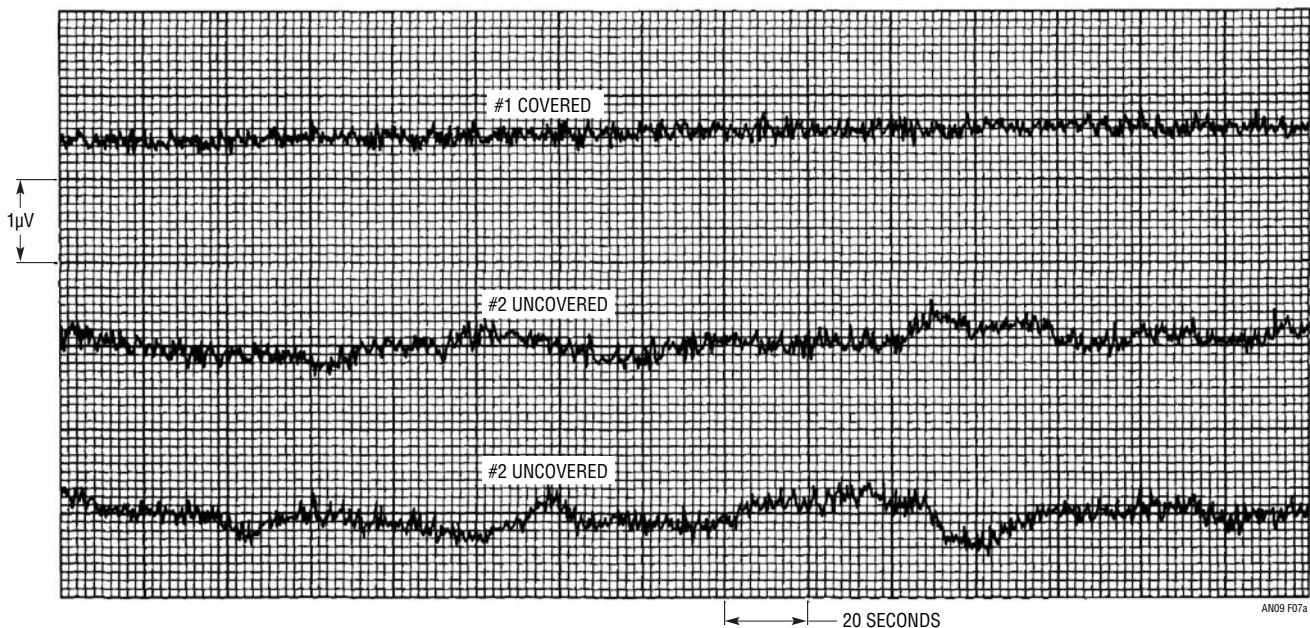


Figure 7. DC-to-1Hz Noise Test Circuit

Another source of parasitic error is stray leakage current. The LTC1052's 30pA bias current allows operation from very high source impedances. In such cases it is desirable to prevent stray leakage currents from reaching the inputs. The simplest way to do this is to connect the amplifier inputs directly to the signal source via a Teflon standoff. Because the amplifier inputs never contact the PC board, stray leakage currents do not affect them. Although this approach is effective, its implementation may not be acceptable in production. Guarding is another technique to minimize board leakage effects. The guard is a PC trace completely encircling the input. This trace is driven (see Figure 8) at a potential equal to that of the input, preventing leakage to the amplifier input terminal. On PC boards, the guard should enclose the input(s) to be protected, with signal connections made directly to the amplifier input.

A final form of parasitic is on particular to all carrier-based amplifiers. If the amplifier is operating in a circuit which contains clocking or oscillation with substantial harmonic content at or near its carrier frequency (e.g., from another LTC1052), erratic operation is possible. This is particularly the case if inductors or transformers radiate magnetic fields related to the clocking or oscillation. The undesired interaction between the amplifier's chopping sequence and the externally generated AC signals may cause mixing the beat frequencies to occur, resulting in errors in the output. The LTC1052 is not particularly sensitive in this regard, but synchronizing its internal oscillator with external circuit clocking precludes this problem. The 14-pin version of the LTC1052 features a pin which allows the internal clock to be synchronized to an external signal. Input signals containing substantial AC content may also cause this

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problem if the AC signal has strong spectral components related to the chopping frequency. In applications where such AC input components exist, it may be necessary to drive the LTC1052 from an external clock source at a frequency which has no harmonic relationship with the input signal. For example, a 372Hz clock frequency will prevent 60Hz input components from affecting amplifier operation.

Applications

Once alerted to the potential problems previously outlined, the engineer is prepared to design circuits around the LTC1052. The most obvious applications are at low level DC, where the low drift will improve performance over other amplifiers. More subtly, it is possible to exploit the LTC1052's low offset uncertainties to extend

the dynamic range of circuit operation. The circuits which follow demonstrate these points, using relatively straightforward examples of improvements in low level, precision performance. Additional, less obvious, circuits use the LTC1052 to stabilize and enhance the performance of a variety of functions including data converters, buffers and comparators.

Standard Grade Variable Voltage Reference

Figure 9 diagrams a standard lab grade variable voltage reference. This circuit combines a pair of LTC1052s with high grade saturated standard cells and other components to produce an extremely stable reference source. The circuit may be used to calibrate 6 1/2 digit voltmeters, ultrahigh resolution data converters and other apparatus requiring high order traceability to primary standards.

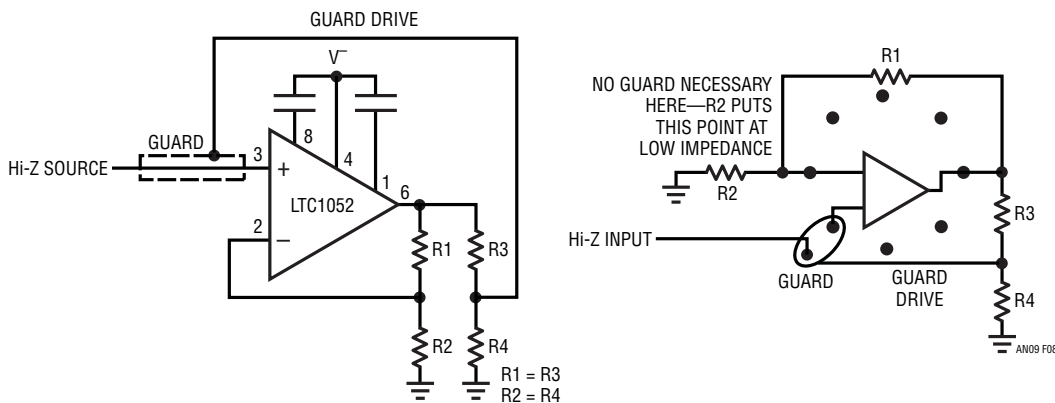


Figure 8. Guarding Technique and Typical Layout

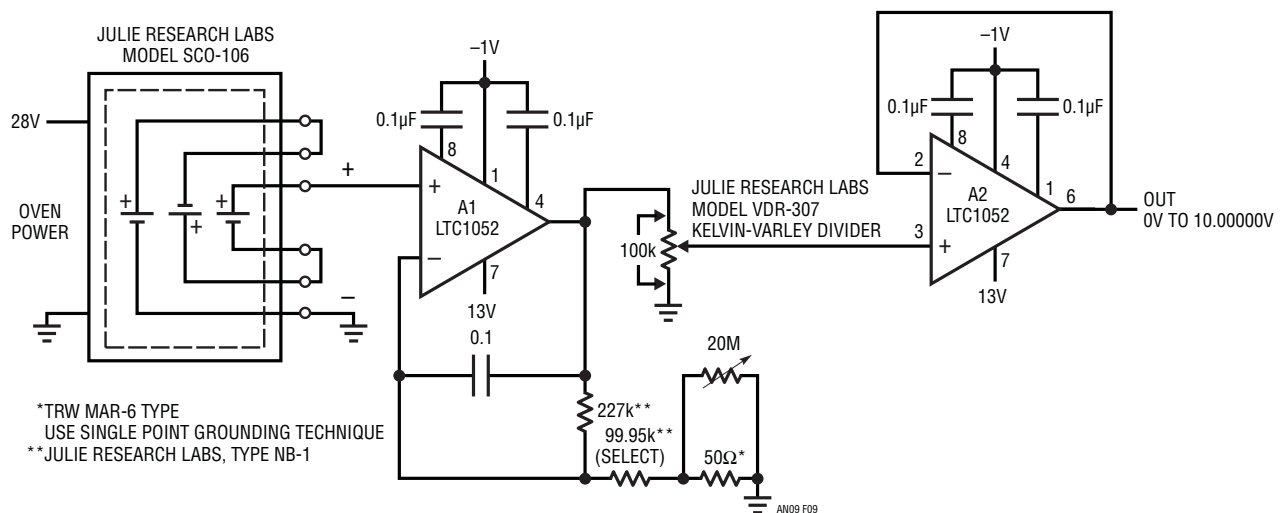


Figure 9. Standard Grade Variable Voltage Reference

Application Note 9

The SCO-106 saturated cells furnish a reference voltage which is buffered and amplified to precisely 10V by A1. A1's output drives a seven place settable Kelvin-Varley divider with 1ppm accuracy. A2's low bias current and high CMRR allow it to unload the divider without introducing significant error. To calibrate this circuit, adjust A1's output for exactly 10V by selecting the feedback resistor and fine trimming the 20MΩ potentiometer. A1's output should be measured with equipment having order traceability to primary NBS standards. Once calibrated, this circuit will

provide *worst-case* 0.0014% accuracy over one year's time and ±5°C temperature excursions. Figure 10 details error sources. Note that the amplifiers contribute only about 1.3ppm (0.00013%) of the total.

Ultra-Precision Instrumentation Amplifier

An ultra-precision instrumentation amplifier appears in Figure 11. This circuit offers greater accuracy and lower drift than any commercially available IC, hybrid or module.

SCO-106 Reference/2ppm/Year	= 2ppm
A1 - 0.05μV/°C × A = 3 × 5°C = 0.75μV	= 0.075ppm
A2 - 0.05μV/°C × A = 1 × 5°C = 0.25μV	= 0.025ppm
A1 + A2 Time Drift/Year = 2μV	= 0.02ppm
KVD - 0.5ppm/°C × 5°C + 1ppm/Year = 3.5ppm	= 3.5ppm
Resistors - 0.1ppm/°C Ratio 5°C + 2ppm/Year = 2.5ppm	= 2.5ppm
A2 CMRR Error = 1ppm 1.2ppm	= 1.2ppm
A2 Loading Error = 0.2ppm	<u>9.32ppm</u>

Figure 10. Error Sources for Ultra-Precision Voltage Reference

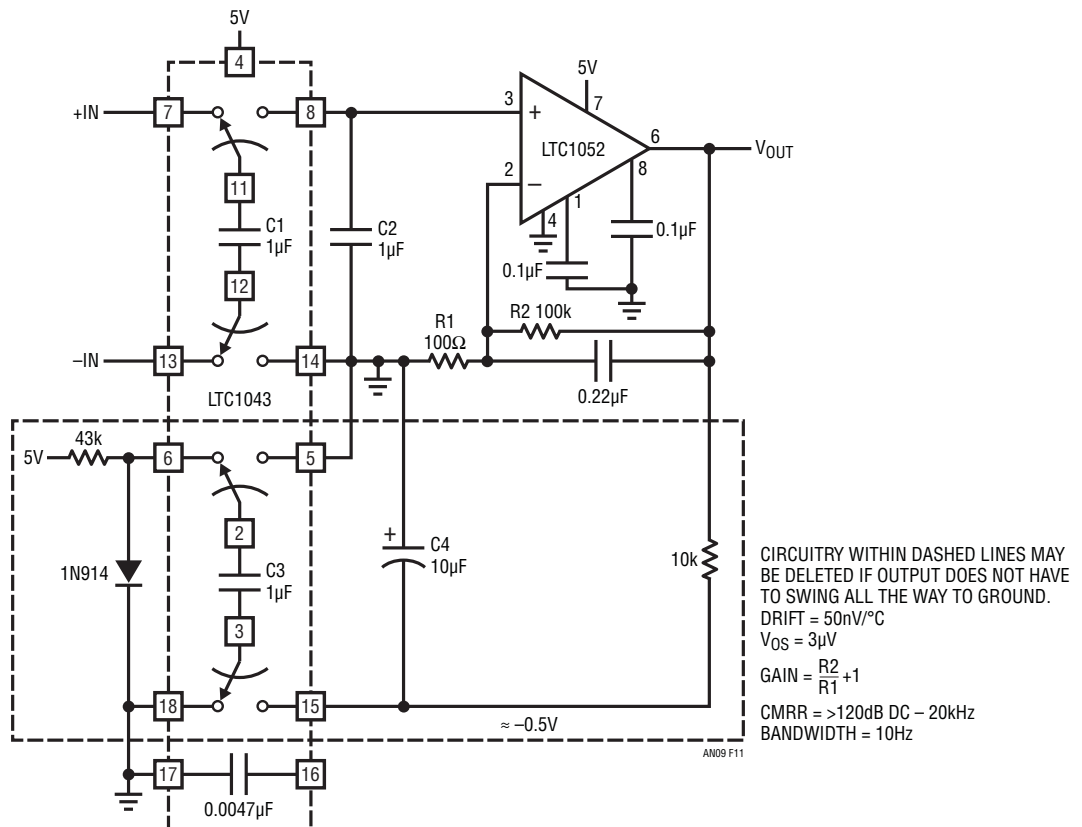


Figure 11. Ultra-Precision Instrumentation Amp

Additionally, it will run from a single 5V power supply. The LTC1043 switched-capacitor instrumentation building block provides a differential-to-single-ended transition using a flying capacitor technique. C1 alternately samples the differential input signal and charges ground referred C2 with this information. The LTC1052 measures the voltage across C2 and provides the circuit's output. Gain is set by the ratio of the amplifier's feedback resistors. Normally, the LTC1052's output stage can swing within 15mV of ground. If operation all the way to zero is required, the circuit shown in dashed lines may be employed. This configuration uses the remaining LTC1043 section to generate a small negative voltage by inverting the diode drop. This potential drives the 10k pull-down resistor, forcing the LTC1052's output into class A operation for voltages near zero. Note that the circuit's switched-capacitor front end forms a sampled data filter allowing common mode rejection ratio to remain high, even with increasing frequency. The 0.0047 μ F unit sets front-end switching frequency at a few hundred hertz. The chart details circuit performance.

High Performance Isolation Amplifier

Instrumentation amplifiers cannot be used to signal condition all differential signals. In factory and process control environments, severe grounding and common mode voltages often mandate the requirement for isolation amplifiers. Isolation amplifiers feature inputs which are galvanically isolated from their output and power connections. This allows the amplifier to ignore the effects of ground loops and operate at input common mode voltages many times the power supply voltage. Implementing a precise, low drift isolation amplifier is not easy, and commercial units are quite expensive. Figure 12 shows a circuit with 0.03% transfer accuracy and the 50nV/ $^{\circ}$ C input drift of the LTC1052. As shown, the circuit provides a gain of 1000 and will operate at 250V input common mode levels.

The circuit works by amplitude modulating the output of a signal conditioning amplifier through a transformer. A synchronous demodulator filter reconstructs the amplifier's original output and furnishes the circuit's output. A separate oscillator and transformer provide power to the amplifier, preserving galvanic isolation between the circuit's input and output ports.

Three 74C04 gates and their associated components form an oscillator which provides complementary drive to Q5

and Q6. These devices energize L1, which generates floating power on the input side of the dashed barrier shown. Simultaneously, the oscillator provides slightly delayed complementary drive to the Q1-Q2 FET switches via the 330 Ω -100pF network and the additional inverters. The floating power produced by L1 is rectified and filtered and drives the LTC1052 (A1) via the Zener drops of the transistors. The \pm 15V floating power is brought out so it can be used to power transducers or other loads. Interaction between the transformer's chopping carrier and A1's internal oscillator is avoided by synchronizing the amplifier to the carrier via the two decade counters. Q3 and Q4, driven by opposing phase carrier signals derived from L1, chop A1's output into L2. This modulated signal information is received at L2's other winding. Because Q1 and Q2 are driven synchronously with Q3 and Q4, they demodulate the amplitude and phase (e.g., plus or minus polarity) information in the carrier. The 330 Ω -100pF network compensates for the slight skew in switch drive signals on opposing sides of L2, minimizing gain error. L2's output (Pin 2) is RC filtered at A2, which also provides the circuit's output. Slight switching errors in the modulator-demodulator result in very small gain differences between positive and negative outputs at Pin 2 of L2. This effect is compensated by the diode-resistor network in A2's output, which provides a small decrease in gain for negative outputs.

Figure 13 shows the response of the isolation amplifier to a sine wave input. For this test, the floating common and circuit grounds are tied together. Trace A is the input applied to A1. Trace B, taken at Pin 4 of L2, shows A1's amplified output being modulated into the transformer. Trace C, obtained at Pin 1 of L2, depicts the received modulated waveform as it is synchronously demodulated. The filtered and final output of A2 appears in Trace D. The 25kHz carrier limits full-power bandwidth of this circuit to about 500Hz, adequate for process control and transducer applications. The transformers used set a voltage breakdown specification of 250V, although higher levels are achievable with different devices. As shown, circuit gain is 1000, allowing amplification of a \pm 5mV signal riding on 250V of common mode to a \pm 5V output. Gain accuracy is 0.03% with a gain drift of typically 50ppm/ $^{\circ}$ C. Input referred drift is set by the LTC1052's 50nV/ $^{\circ}$ C specification.

To trim this circuit, tie A1's input to floating common and adjust the zero trim for 0V output. Next, connect A1's input to a 5mV source and adjust the gain trim at A2 for exactly $5.000V_{OUT}$. Finally, connect A1's input to a $-5mV$ source and select the $10M\Omega$ value in A2's feedback path for a $-5.000V$ output reading. Repeat this procedure until all three points are fixed.

Stabilized, Low Input Capacitance Buffer (FET Probe)

A recurring requirement in automatic semiconductor testing and probing equipment is for a highly stable unity-gain buffer amplifier with low input capacitance. Such an amplifier is also useful for other circuit chores where it is desirable to accurately monitor a point without introducing any significant AC or DC loading terms. Figure 14 shows such a circuit. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel

current. The LT[®]1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open-loop configuration would be quite drifty because there is no DC feedback. The LTC1052 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The diode in Q1's source line ensures that the gate never forward biases and the 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

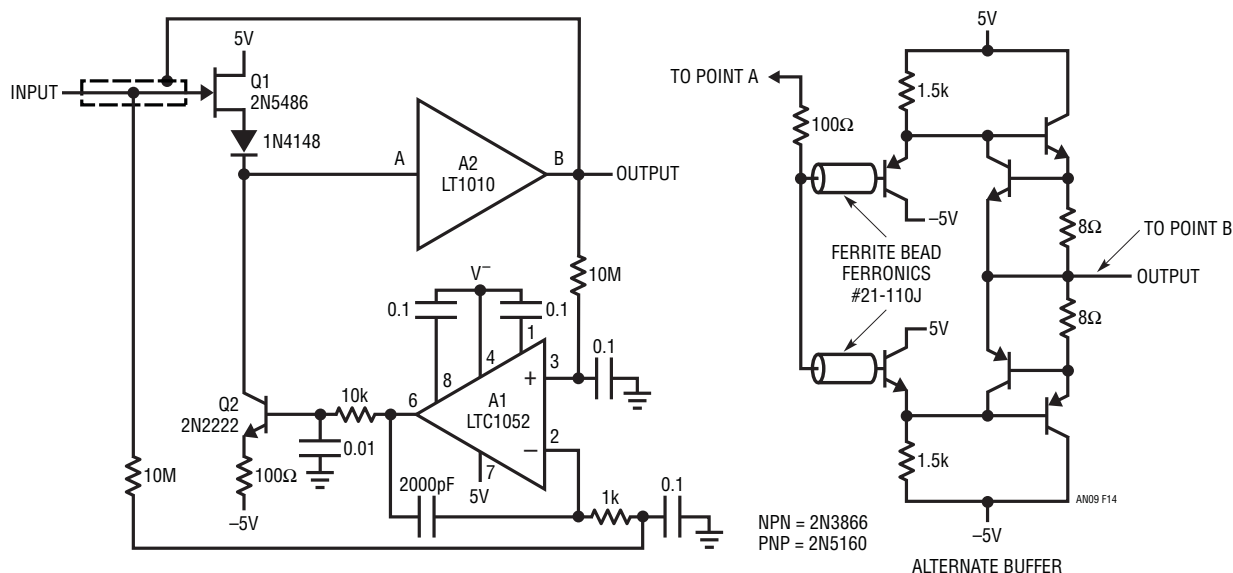


Figure 14. Fast, Stabilized FET Buffer

Application Note 9

The LT1010's 15MHz bandwidth and 100V/ μ s slew rate, combined with its 150mA output, are fast enough for most circuits. For very fast requirements, the alternate discrete component buffer shown will be useful. Although its output is current limited at 75mA, the GHz range transistors employed provide exceptionally wide bandwidth, fast slewing and very little delay. Figure 15 shows the LTC1052 stabilized buffer circuit's response using the discrete stage. Response is clean and quick, with delay inside 4ns. Note that rise time is limited by the pulse generator and not the circuit. For either stage, offset is set by the LTC1052 at 3 μ V, with gain about 0.95. It is worth noting that this circuit performs the same function as commercial FET probes in the \$1,000.00 range.

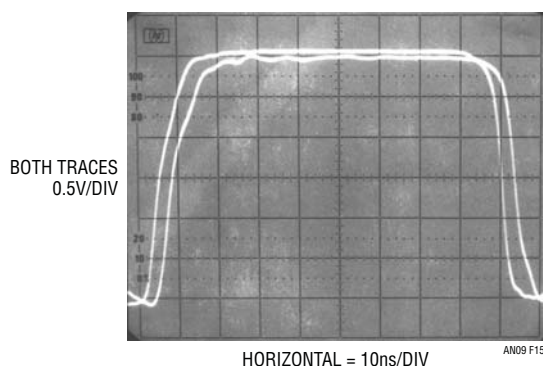


Figure 15. Stabilized Buffer Delay

Chopper-Stabilized Comparator

It is often desirable to use a reasonably fast voltage comparator with low input offset drift. Such a device is useful in high resolution A/D converters, crossing detectors and anywhere else a precise, stable, high speed comparison must be made. Unfortunately, obtaining reasonable comparator speed and low input drift in a design is difficult and monolithic comparators must be constructed around this trade-off. Figure 16 shows a way to use the LTC1052 to eliminate the offset and drift in a comparator without sacrificing speed or differential input versatility. This circuit is applicable only in situations where some dead time is available for zeroing action to occur.

The circuit functions by periodically shorting the comparator inputs together and forcing the comparator into its linear region via its offset pins. The voltage at the offset

pins required to do this is stored. When the comparator inputs are returned to their normal states, the stored voltage is maintained at the comparator's offset pins, effectively controlling the device's offset. Periodic updating ensures long-term stability of the correction. In this circuit, A1 is the stabilizing amplifier for C1. C1's inputs are controlled by a dual DPDT switch section furnished by the LTC1043. When LTC1043 Pin 16 is high, Pins 12 and 11 are connected to Pins 13 and 7, respectively. Pin 3 at C1's output, is connected to Pin 18. Under these conditions, A1 is effectively connected in a negative feedback loop between C1's output and its offset Pin 5 (see detail of LT1011 input stage in Figure 16). This forces C1 into its linear region and its output oscillates at a high frequency between the rail voltages. A1, connected as a low frequency integrator, filters this action, compares its DC equivalent value to ground (its positive input potential) and drives C1's offsets to zero. When Pin 16 of the LTC1043 goes low, all switch states reverse and C1's inputs are free to compare the signals present at LTC1043 Pins 14 and 8 in the normal fashion. During this interval, A1's output remains fixed at the voltage stored in its feedback capacitor. A1's low bias current allows long durations between correction cycles—periods of seconds are practical—while maintaining effective comparator offset well within 5 μ V with negligible temperature drift.

Figure 17 shows the circuit's response to a sine wave (Trace A) applied to C1's positive input at LTC1043 Pin 14. C1's negative input, LTC1043 Pin 8, is grounded. With the circuit's zero command low (Trace B), C1's output (Trace C) responds in the normal fashion. During this period, the status output (Trace D) is low, indicating C1 is in its normal mode. When the zero command occurs (Trace B, just to the right-center of the screen), C1 is forced into its linear region, where it oscillates. During this time, A1 updates the correction voltage stored in its feedback capacitor. When the zero command pulse falls, normal comparator action is seen to resume. Note that the circuit's status output reflects the true operating mode of the circuit, because its timing includes the 50ns delay of the LTC1043 switch. For this reason the status output, and not the zero command, should be used to indicate the circuit's actual operating state.

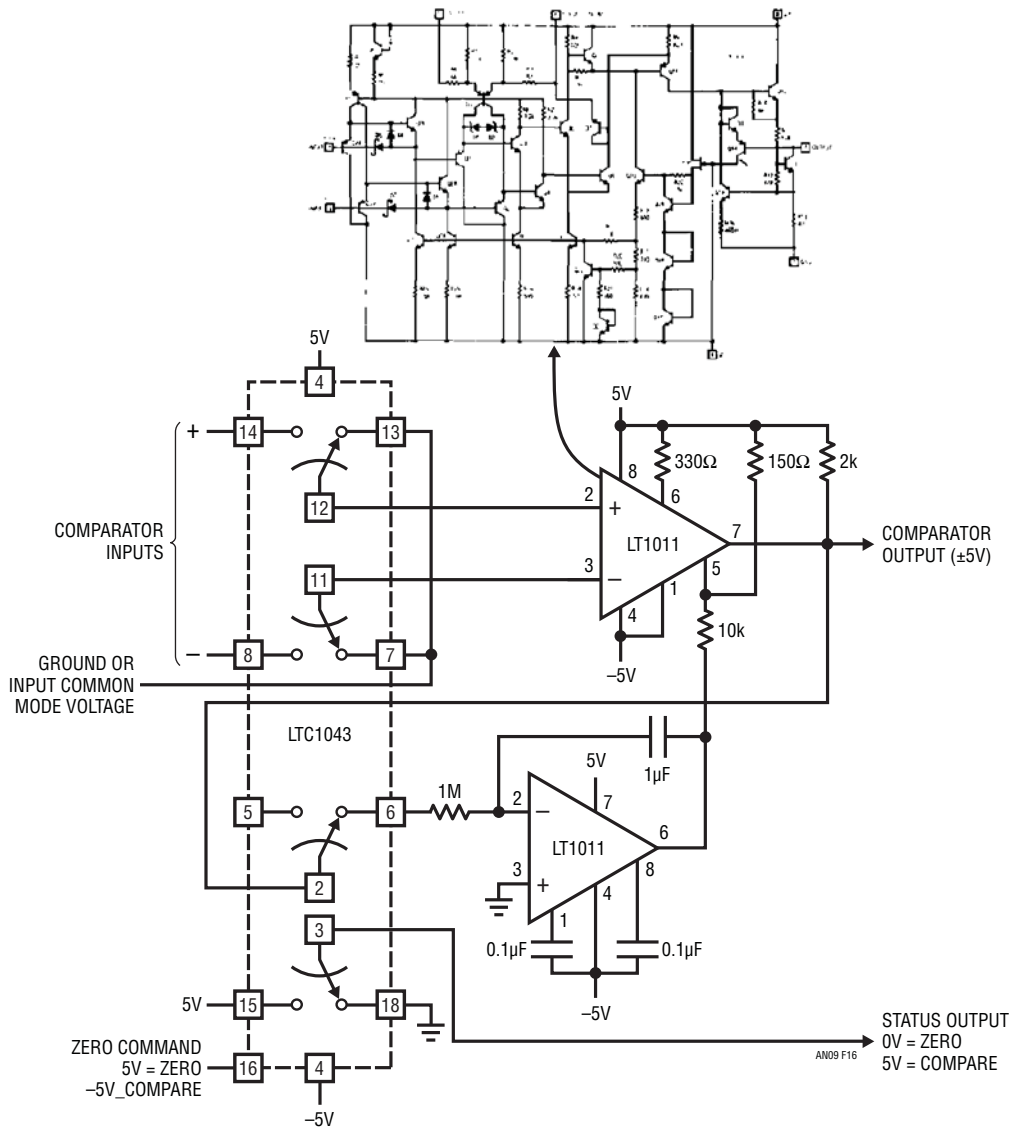


Figure 16. Offset Stabilized Comparator

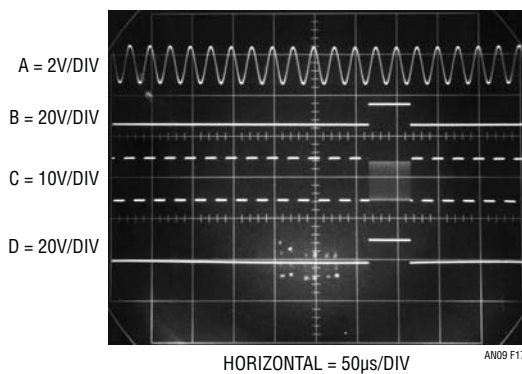


Figure 17. Stabilized Comparator Waveforms

Application Note 9

Stabilized Data Converter

Amplifiers and comparators are not the only elements which can benefit from chopper-stabilization by the LTC1052. Figure 18 shows a way to offset-stabilize a data converter, thereby doubling its dynamic range of operation, eliminating the necessity for an offset trim and reducing zero drift to negligible levels. In this circuit, the LTC1052 corrects for offset deficiencies in the AD650 V→F converter. Although specified for 1MHz full-scale operation, this device's 4mV input offset limits untrimmed dynamic range of operation to only 3 1/2 decades of output frequency. Under normal operating conditions, the AD650's positive input is grounded and its negative input is driven via the resistor string shown. Obtaining more than 3 1/2 decades of operation requires an offset trim at Pins 13 and 14. Even after trimming, the input amplifier's 30 μ V/°C

drift contributes a 3Hz/°C zero point error. The LTC1052 corrects these problems by measuring the offset voltage at the circuit's summing node, comparing it to ground and driving the AD650 positive input (normally grounded in the manufacturer's recommended circuit configuration) with the appropriate stabilizing correction voltage. The dual FETs eliminate bias current caused errors. The LTC1052's integrator configuration keeps its gain at low frequency and DC, preserving the AD650's fast dynamic response while eliminating its offset errors. The divider network in the LTC1052's output is scaled to allow enough correction range to zero the AD650's offsets without causing overdrive during start-up and transients. With this scheme in use, the circuit does not require any zero trim to achieve full 6 decade operation. To calibrate, apply 10V and trim the output for exactly 1MHz.

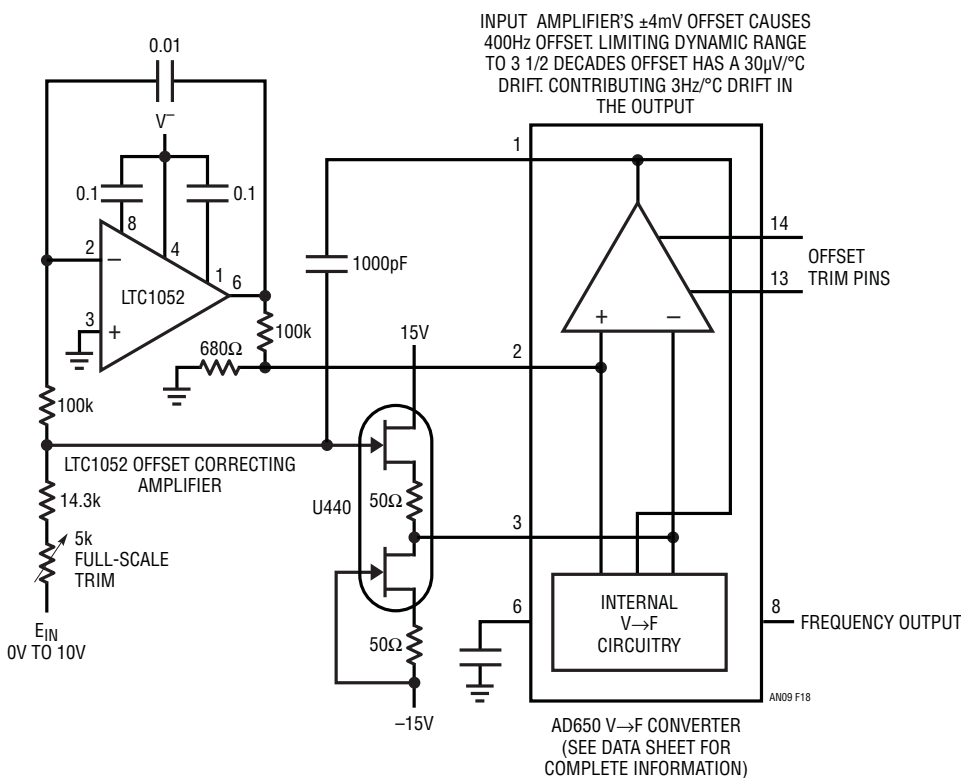


Figure 18. Offset Stabilizing a V→F Converter

Wide Range V→F Converter

Figure 19 shows another stabilized V→F converter. It features 1Hz to 1.25MHz operation, 0.05% linearity, and a temperature coefficient of typically 20ppm/°C, all substantially better than Figure 18's circuit. Additionally, it is less expensive and runs from a single 5V supply. Trade-offs include slower step response and a larger

component count. This circuit uses a charge feedback scheme to allow the LTC1052 to close a loop around the entire V→F converter, instead of simply controlling offset. This approach enhances linearity and stability but introduces the loop's settling time into the overall V→F step response characteristic. Figure 20 shows waveforms of operation.

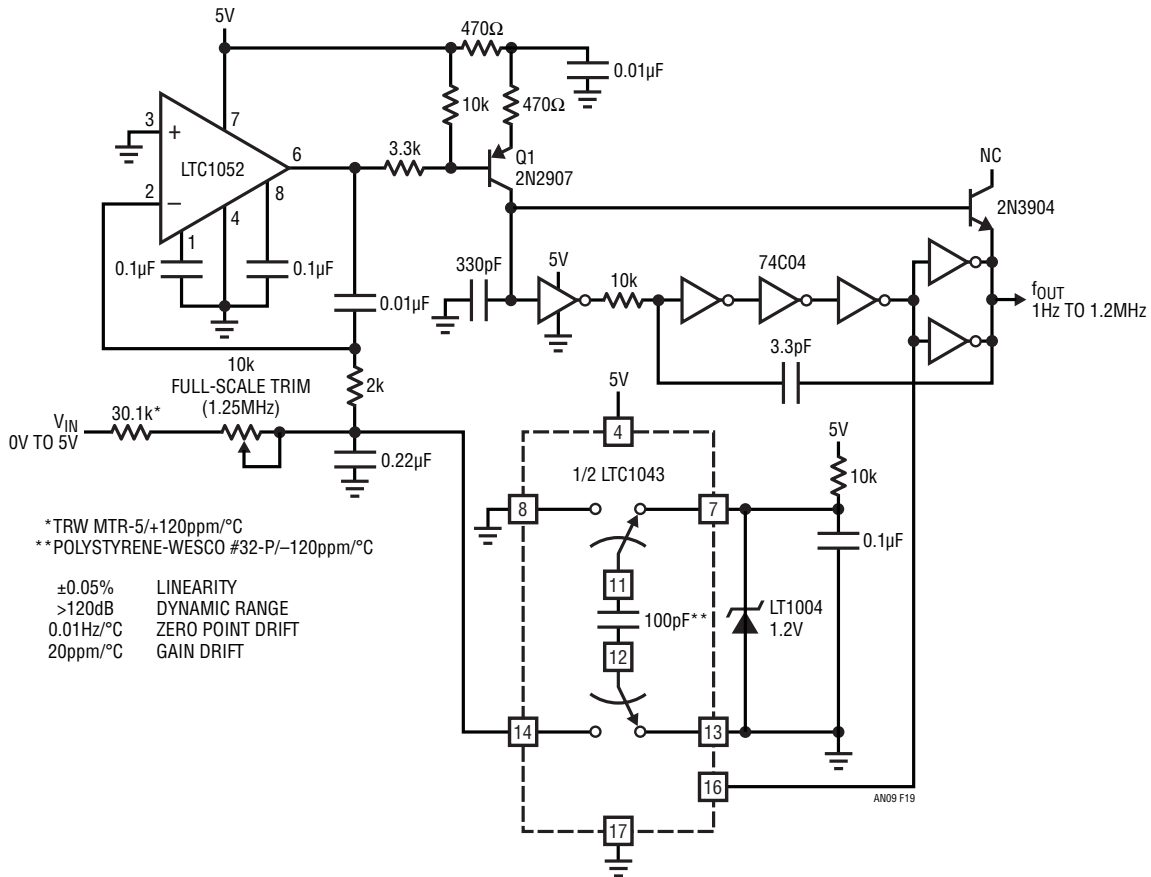


Figure 19. 1Hz to 1.25MHz Voltage-to-Frequency Converter

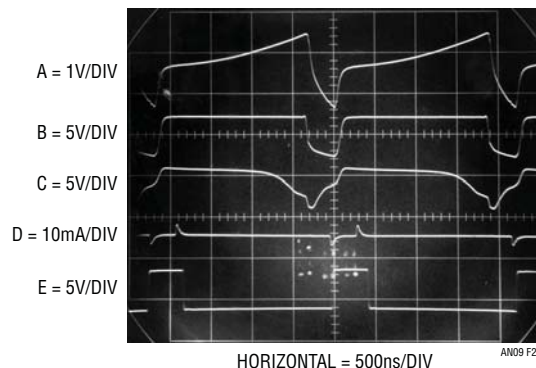


Figure 20. V→F Waveforms

Application Note 9

A positive input voltage directs A1's output to go negative, biasing the Q1 current source. Q1's collector puts current into the 330pF capacitor, causing it to rise in voltage (Trace A, Figure 20). The low input current CMOS inverter changes state when the ramp crosses 1/2 of the supply voltage. This causes all of the inverters to switch. The two paralleled inverters at the end of the chain go low (Trace B), simultaneously supplying positive feedback at the 10k-3.3pF junction (Trace C) and forcing the 330pF capacitor to a lower voltage by removing current from it (Trace D) via the diode connected 2N3904. During the ramping interval, LTC1043 switch Pins 11 and 12 are connected to Pins 8 and 14 discharging the 100pF capacitor into Pin 14. When the output inverters go low, the LTC1043's control pin (Pin 16) also switches, placing the charged 100pF capacitor across Pins 7 and 13. Thus, each time the inverters switch, a fixed quantity of charge is dispensed into the 2k-0.22 μ F-10k potentiometer junction ($Q = CV$). The LTC1043's switching is arranged so that this charge is of opposite polarity to the positive input current. The 0.22 μ F capacitor integrates the discrete charge dumps to DC. A1 servo controls the Q1 inverter oscillator to run at whatever frequency is required to force its negative input to 0V. In this manner, drift and nonlinear response in the Q1 inverter oscillator are compensated by A1's closed-loop control. The circuit's frequency output is delivered by another LTC1043 section (Trace E).

Several factors contribute to this circuit's performance. The low input current to the CMOS inverter, combined with the low leakage of the 2N3904 base-emitter diode and the circuit's servo action, allows operation to well below 1Hz, despite the small 330pF integrating capacitor. In the lower frequency ranges, currents at this junction are small and board leakage can cause jitter. A clean board will work well, but the best approach is to mount the capacitor, Q1's collector, the inverter input and the transistor base connection on a Teflon stand-off, using short connections. The resistor and capacitor specified in the figure, both gain terms, have opposing temperature coefficients, aiding gain drift performance. The LTC1052's low offset eliminates the need for a zero trim while preserving the circuit's >120dB dynamic range of operation. To trim the circuit, apply 5.000V and adjust the 1.25MHz trim for 1.2500MHz out.

1Hz to 30MHz V→F Converter

Although Figure 19's circuit is impressive, it still does not tax the LTC1052's dynamic range of operation. Figure 21 shows a highly modified version of Figure 19. It has a 1Hz to 30MHz output (150dB dynamic range) for a 0V to 3V input. This is by far the widest dynamic range and highest operating frequency of any V→F discussed in the literature at the time of writing*. It is a good application of the extremely wide signal processing range afforded by the LTC1052. The circuit maintains 0.08% linearity over its entire 7 1/3 decade range with a full-scale drift of about 20ppm/°C. Zero point error is 0.3Hz/°C and is directly related to the LTC1052's 50nV/°C drift specification.

To get the additional bandwidth, Figure 19's CMOS inverters are replaced with a fast JFET buffer driving a Schottky TTL Schmitt trigger. The Schottky diode prevents the Schmitt trigger from ever seeing negative voltage at its input. The diode connected 2N3904 is retained for resetting the capacitor, which has a smaller value. Figure 19's positive AC feedback, with its attendant recovery time constant, is avoided in this circuit. Instead, the Schmitt's input voltage hysteresis provides the limits which the oscillator runs between. The 30MHz full-scale output is much faster than the LTC1043 can accept, so the digital divider stages are used to reduce the feedback frequency signal by a factor of 20. Remaining Schmitt sections furnish complementary outputs. Good high frequency wiring techniques should be used when constructing the current source-buffer-Schmitt trigger sections.

Figure 22 shows the key waveforms with the circuit loafing at 20MHz. Trace A is the Schmitt trigger input, which is seen to ramp between two voltage limits, while Trace B is the Schmitt output. The closed-loop approach results in very low output jitter and noise over the entire 150dB operating range. Figure 23 plots this, showing frequency jitter versus output frequency. Jitter does not rise above 0.01% until 20kHz, which is only 0.05% of scale. Even at 1ppm of scale (30Hz), jitter is still about 1%, finally rising to 10% at 1Hz (0.000003% of full scale). As V→F operating frequency decreases toward the LTC1052's feedback loop roll-off, the loop dominates the jitter characteristic. In the high frequency ranges the loop poles are not a

* 1Hz to 100MHz circuit is under development and will be discussed in AN14, "Designs for High Performance V→F Converters."

factor and current source and Schmitt trigger switching noise dominate. As with Figure 19's circuit, the feedback loop slows step response. Figure 24 shows this, with a full-scale input step requiring almost 50ms to settle. To

trim this circuit, ground the input and adjust the 1Hz trim until oscillation just starts. Next, apply 3.000V and set the 30MHz trim for a 30.00MHz output. Repeat this procedure until both points are fixed.

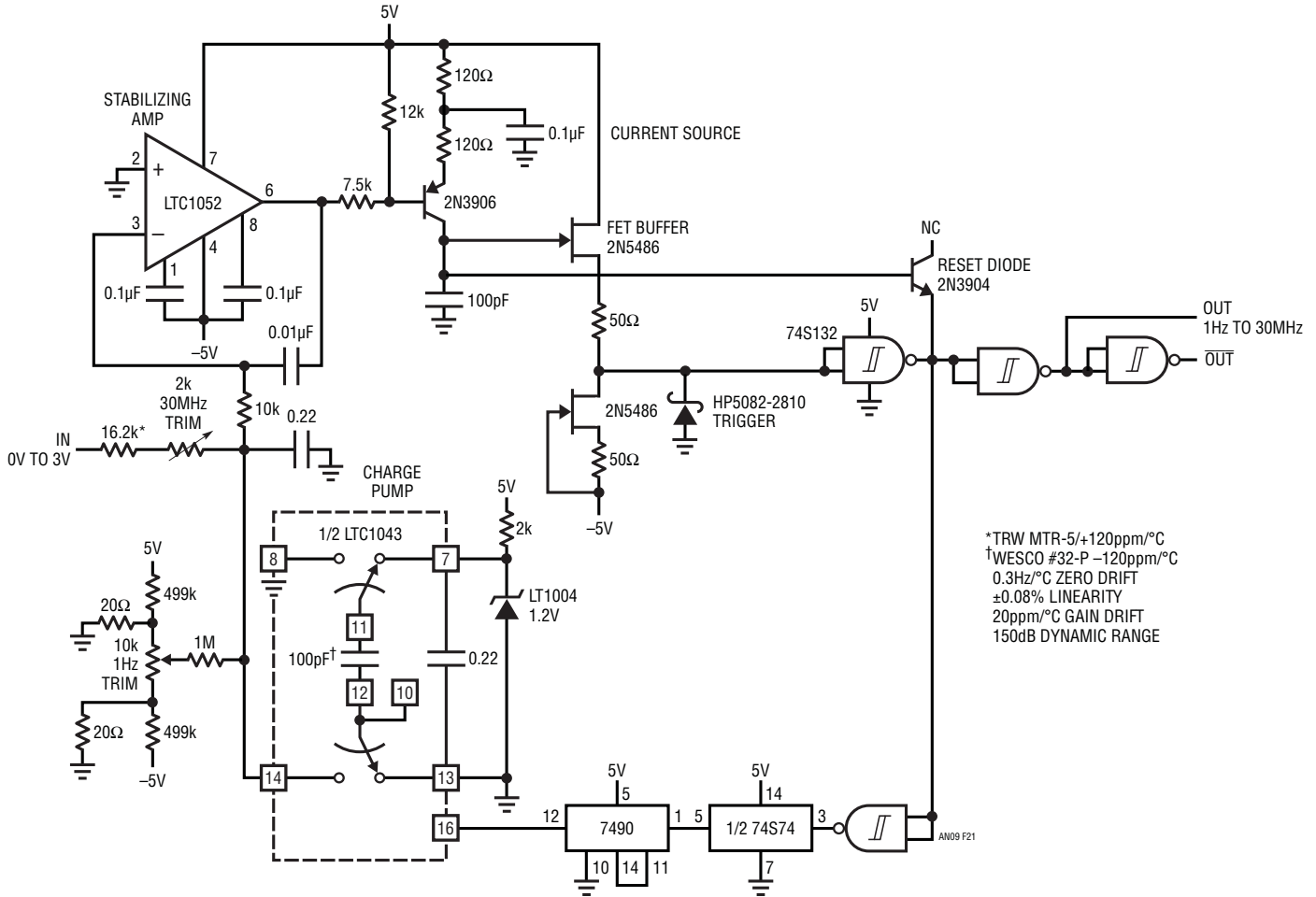


Figure 21. 1Hz to 30MHz V→F Converter

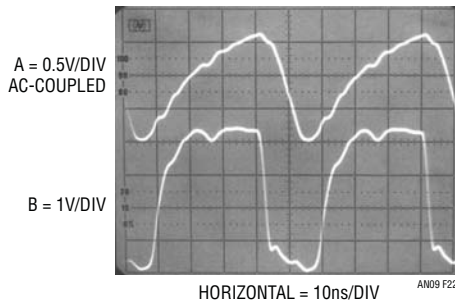


Figure 22. Fast V→F Ramp-Reset Detail

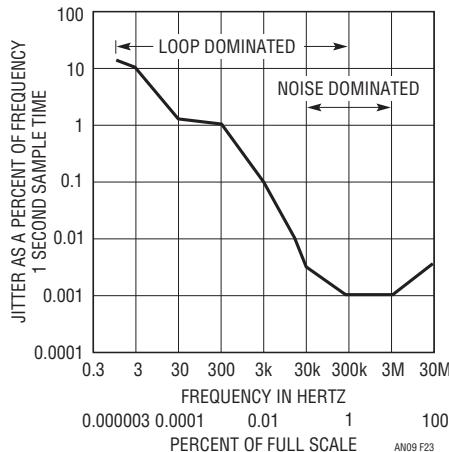


Figure 23

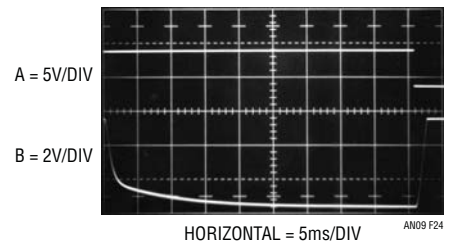


Figure 24. Fast V→F Step Response

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Application Note 9

16-Bit A/D Converter

V→F converters are not the only types of data converters which can benefit from the LTC1052's performance. Figure 25 shows a 16-bit A/D converter (overrange to 100,000 counts is provided).

The A/D converter, made up of A2, a flip-flop, some gates and a current sink, is based on a current balancing technique. Once again, the chopper-stabilized LTC1052's 50nV/°C input drift is required to eliminate offset errors in the A/D. Figure 26 details key A/D waveforms. Assume the flip-flop's Q output (Trace B) is low, connecting LTC1043 Pins 3 and 18. The current sink switch directs its output to ground.

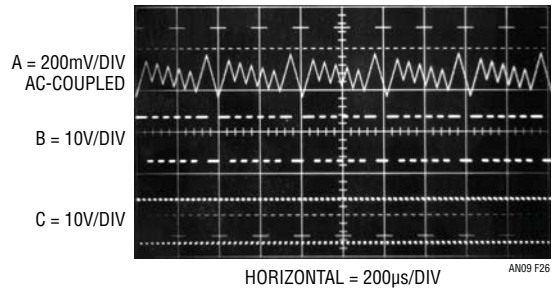


Figure 26. 16-Bit A/D Waveforms

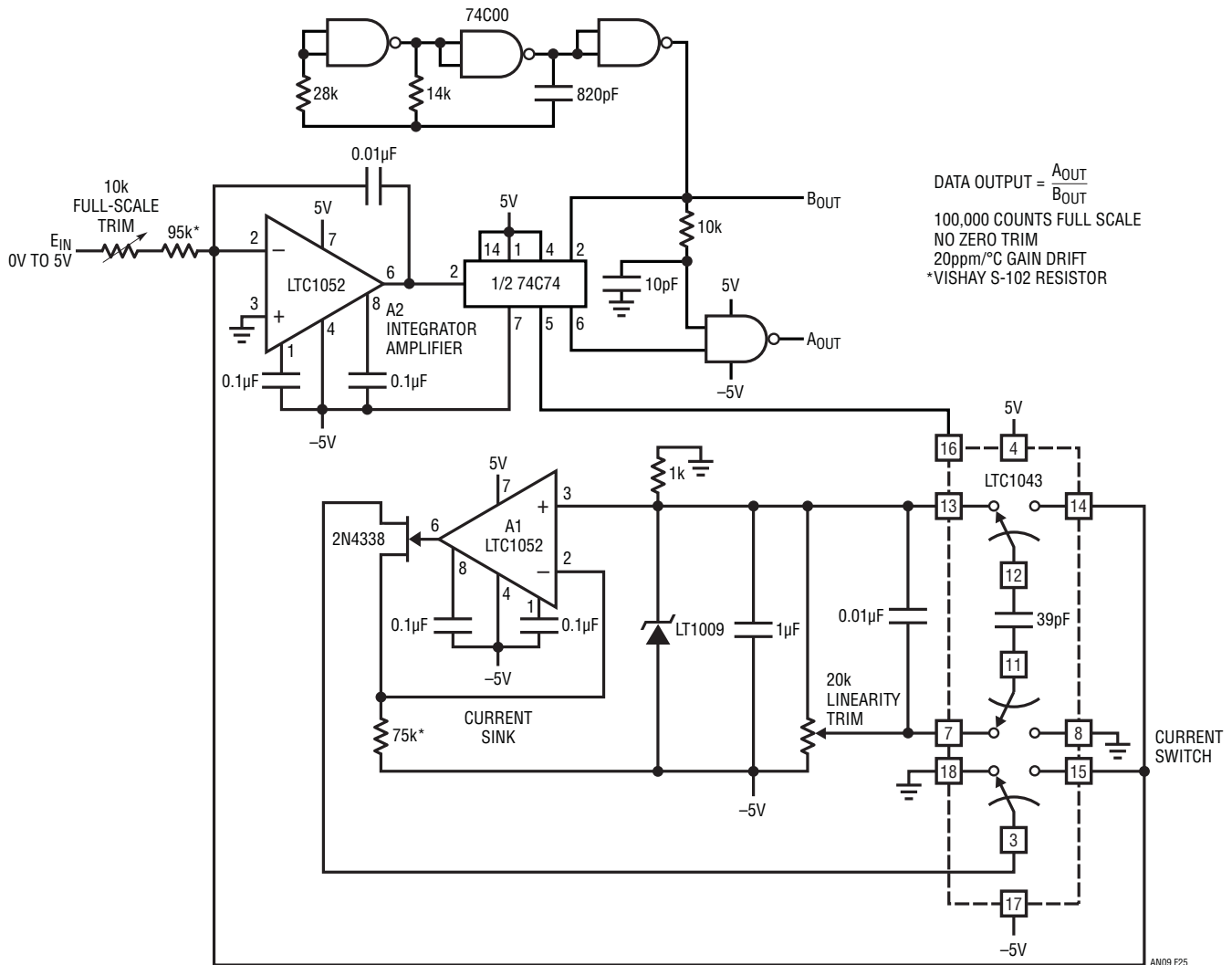


Figure 25. 16-Bit A/D Converter

Application Note 9

The op amp's offset drift is amplified to drive the meter by the LTC1052. The diode bridge connection allows either positive or negative op amp temperature sensor offsets to interface directly with the circuit. In this case, the circuit is arranged for a 10°C to 40°C output, although other ranges are easily accommodated. To calibrate this circuit, subject the op amp sensor to a 10°C environment and adjust the 10°C trim for an appropriate meter indication. Next, place the op amp sensor in a 40°C environment and trim the 40°C adjustment for the proper reading. Repeat this procedure until both points are fixed. Once calibrated, this circuit will typically provide accuracy within $\pm 2^\circ\text{C}$, even in high noise environments.

Output Stages

In some circumstances it may be required to obtain more output current or swing from the LTC1052 than it can provide. The CMOS output stage cannot provide the current levels of bipolar op amps. Additionally, it may be necessary to run the device off $\pm 15\text{V}$ supplies and to

obtain increased voltage and current outputs. Figure 28 parallels a package of CMOS inverters to obtain 10mA to 20mA output current capability. The inversion in the loop requires the feedback connection to go to the amplifier's positive input. The RC damper eliminates oscillation in the inverter stage, which is running in its linear region. The local capacitive feedback at the amplifier gives loop compensation. Figure 29 shows a way to run the LTC1052 from 15V supplies while obtaining the increased current and voltage output capabilities of the LT318A amplifier. The transistors run in Zener mode, dropping the supply to about $\pm 7\text{V}$ at the LTC1052. The LT318A serves as an output stage with a voltage gain of 4. The output swing is that of the LT318A, typically, $\pm 13\text{V}$ into $2\text{k}\Omega$ with a short-circuit current of 20mA. This circuit is dynamically stable at any gain in either the inverting or noninverting configuration, although the LTC1052's input common mode range (-7V to 5V with the $\pm 15\text{V}$ power supply used) must not be exceeded.

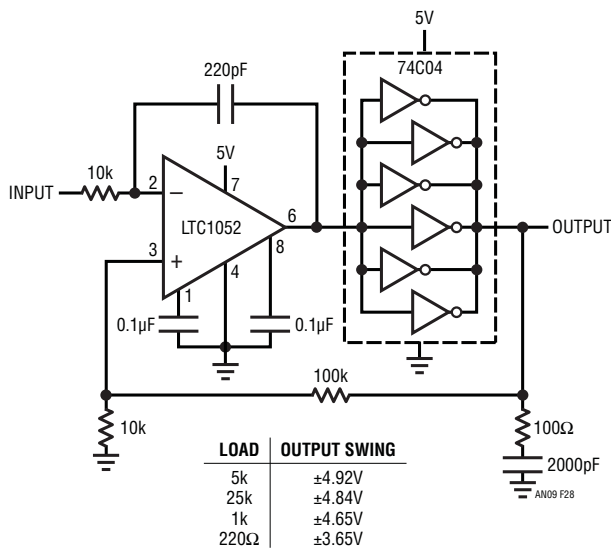


Figure 28. Increasing Output Current

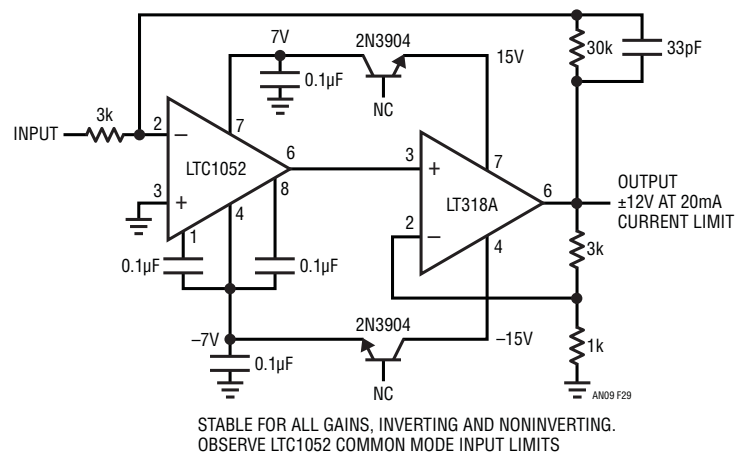


Figure 29. Increasing Output Current and Voltage ($V_{\text{SUPPLY}} = \pm 15\text{V}$)

Box Section—Choppers, Chopper-Stabilization and the LTC1052

All chopper-stabilized amplifiers achieve high DC stability by converting the DC input into an AC signal. An AC gain stage amplifies this signal. After amplification it is converted back to DC and presented as the amplifier's output. Figure B1 shows a conceptual chopper amplifier.

The AC amplifier's input is alternately switched between the signal input and feedback divider network. The AC amplifier's output amplitude represents the difference between the feedback signal and the circuit's input. This output is converted back to DC by a phase sensitive demodulator composed of a second switch, synchronously driven with the input switch. The output integrator stage smooths the switch output to DC and presents the final output. Drifts in the output integrator stage are of little consequence because they are preceded by the AC gain stage. The DC drifts in the AC stage are also irrelevant because they are isolated from the rest of the amplifier by the coupling capacitors. Overall DC gain is extremely high, being the product of the gains of the AC stage and the DC gain of the integrator. Although this approach easily yields drifts of $100\text{nV}/^\circ\text{C}$ and open-loop gains of 100 million, there are some drawbacks. The amplifier has a single-ended, noninverting input and cannot accept differential signals without additional circuitry added at the front end. Also, the carrier-based approach constitutes a sampled data system and overall amplifier bandwidth is limited to a small fraction of the carrier frequency. Carrier frequency, in turn, is restricted by AC

amplifier gain-phase limitations and errors induced by switch response time. Maintaining good DC performance involves keeping the effects of these considerations small and carrier frequencies are usually in the low kilohertz range, dictating low overall bandwidth.

The classic chopper-stabilized amplifier solves the chopper amplifier's low bandwidth problem. It uses a parallel path approach (Figure B2) to provide wider bandwidth while maintaining good DC characteristics. The stabilizing amplifier, a chopper type, biases the fast amplifier's positive terminal to force the summing point to zero. Fast signals directly drive the AC amplifier, while slow ones are handled by the stabilizing chopper amplifier. The low frequency cut-off of the fast amplifier must coincide with the high frequency roll-off of the stabilizing amplifier to achieve smooth overall gain-frequency characteristics. With proper design, the chopper-stabilized approach yields bandwidths of several megahertz with the low drift characteristic of the chopper amplifier. Unfortunately, because the stabilizing amplifier controls the fast amplifier's positive terminal, the classic chopper-stabilized approach is restricted to inverting operation only.

The LTC1052 uses a different approach which permits full differential input operation, good bandwidth and retains ultralow drift. It relies on an autozero technique.

During the LTC1052's autozero cycle, the inputs are shorted together and a feedback path is closed around

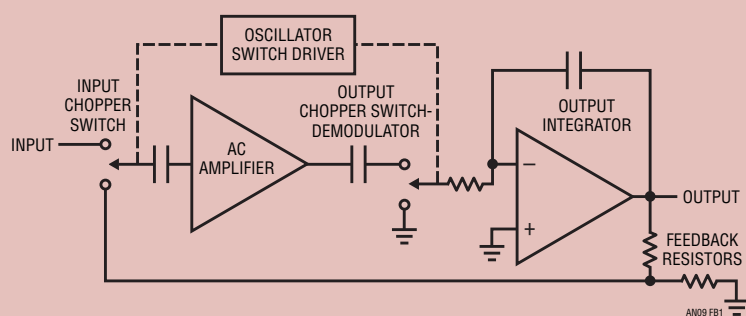


Figure B1. Chopper Amplifier

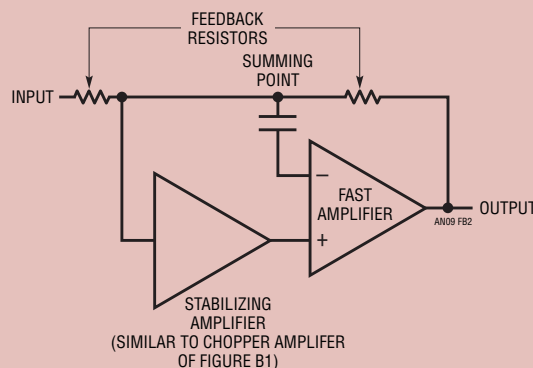


Figure B2. Classic Chopper-Stabilized Amplifier

Application Note 9

the input stage to null its offset. Switch S2 (Figure B3) and capacitor C_{EXTA} act as a sample and hold to store the nulling voltage during the sampling cycle.

In the sampling cycle, the now almost ideal amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S2 act as a sample and hold to store the amplified input signal during the autozero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the autozero cycle the inputs are not only shorted together, but are also shorted to the negative input. This forces nulling with the common mode voltage present. The same argument applies to power supply variations and accounts for the extremely good CMRR and PSRR specifications on the LTC1052.

The complete amplifier contains stabilizing elements, feedforward for high frequency signals, and antialiasing circuitry, but the superior DC performance is completely described by this simple loop.

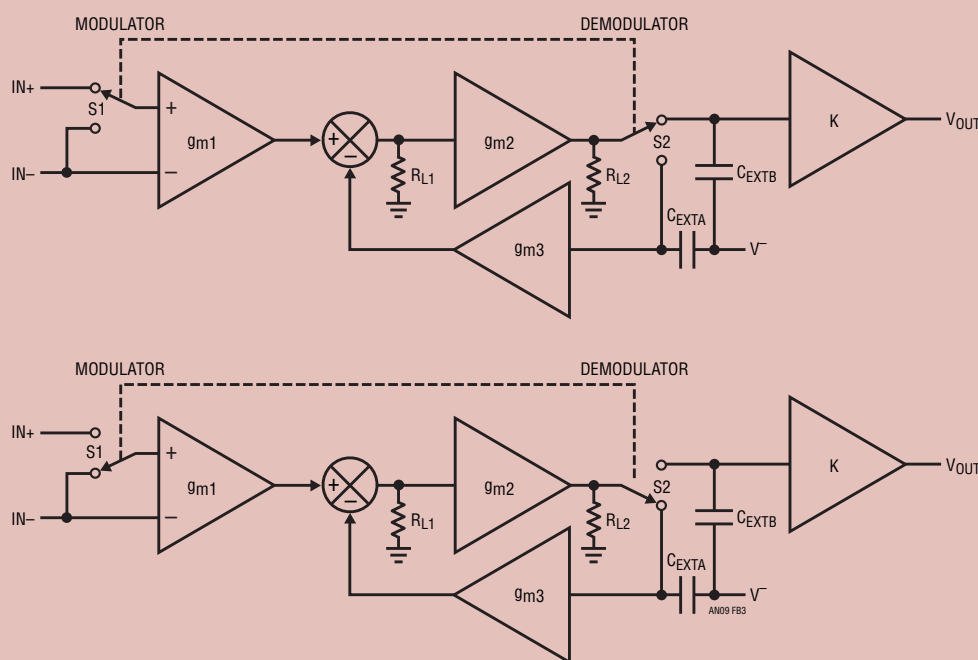


Figure B3. LTC1052 Conceptual Amplifier (Simplified)

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Methods for Measuring Op Amp Settling Time

Jim Williams

Servo, DAC and data acquisition amplifiers all require good dynamic response. In particular, the time required for an amplifier to settle to final value after an input step is especially important. This specification allows setting a circuit's timing margins with confidence that the data produced is accurate. The settling time is the total length of time from input step application until the amplifier remains within a specified error band around the final value.

Figure 1 shows one way to measure amplifier settling time (see References 1, 2, and 3). The circuit uses the "false sum node" technique. The resistors and amplifier form a bridge-type network. Assuming ideal resistors, the amplifier output will step to $-V_{IN}$ when an input pulse is applied. During slew, the oscilloscope probe is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. Several flaws exist. The circuit requires the input pulse to have a flat top within the

required measurement limits. Typically, settling within 10mV or less for a 10V step is of interest. No general purpose pulse generator is meant to hold output amplitude and noise within these limits. Generator output-caused aberrations appearing at the oscilloscope probe will be indistinguishable from amplifier output movement, producing unreliable results. The oscilloscope connection presents additional problems. As probe capacitance rises, AC loading of the resistor junction will influence observed settling waveforms. The 20pF probe shown alleviates this problem but its 10X attenuation sacrifices oscilloscope gain. 1X probes are not suitable because of their excessive input capacitance. An active 1X FET probe will work, but another issue remains.

The clamp diodes at the probe point are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The diodes' 600mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question (for a discussion of oscilloscope overdrive considerations, see Box Section A, "Evaluating Oscilloscope Overload Response").

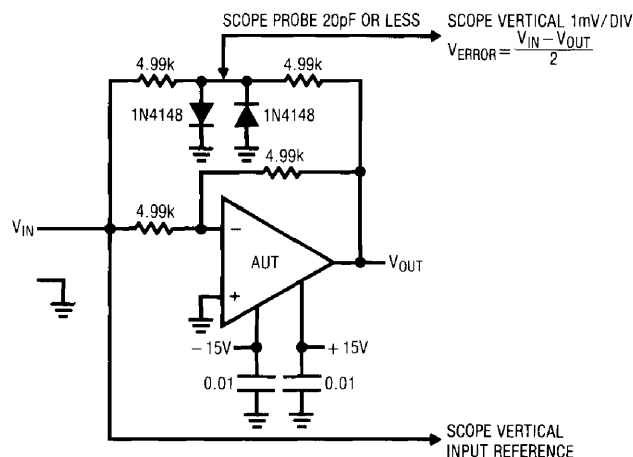


Figure 1. Typical Settling Time Test Circuit

Application Note 10

Figure 2 shows a practical settling time test circuit which addresses the problems discussed. Combined with a careful evaluation of the test oscilloscope used, it permits reliable settling time measurements in the 0.1% to 0.01% region. The input pulse does not drive the amplifier, but switches a Schottky bridge via a clamp. The bridge is biased from two low noise LT1021-10V references. Depending on input pulse polarity, current flows through the appropriate 10k resistor to bias the amplifier's summing point. The bridge switches cleanly and quickly, producing a flat-topped current pulse into the AUT. The circuit's input pulse characteristics do not influence the measurement. A second clamp-bridge arrangement supplies an opposite polarity signal which is nulled against the amplifier's output at point B. Schottky

clamp diodes limit this point's voltage excursion to $\pm 300\text{mV}$.

The Q1-Q5 configuration forms a low input capacitance, high speed buffer to drive the oscilloscope. Q1A's 1-2pF input capacitance provides very light AC loading, eliminating probe-caused problems. Q1B, running as a current sink, compensates Q1A's V_{GS} drop. Q2-Q5 form a complementary emitter-follower which can drive substantial cable capacitance without distortion.

The circuit should be built on a ground planed board with particular care taken to ensure low stray capacitance at points A and B. The AUT socket should be selected for short pin lengths. Very high speed amplifiers ($t_{SETTLE} < 200\text{ns}$) should be directly soldered into the circuit.

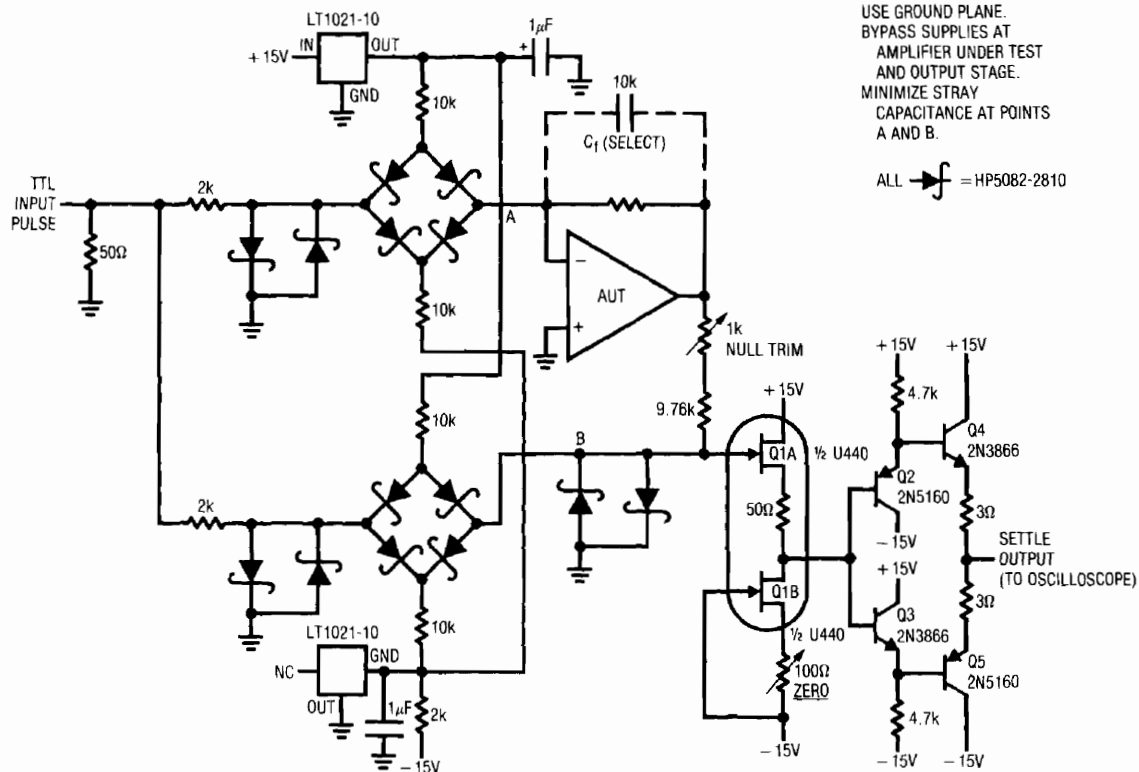


Figure 2. Improved Settling Time Test Circuit

This circuit, combined with a judiciously chosen oscilloscope, allows observation of amplifier settling to a millivolt (0.01%) for a 10V step. A good way to gain confidence in the circuit is to test a very fast UHF amplifier. Figure 3 shows response for an amplifier (Teledyne Philbrick 1435) specified to settle in 70ns within a millivolt for a 10V step. Trace A is the input pulse, Trace B is the amplifier output and Trace C is the settle signal. Settling occurs inside 70ns, indicating good agreement between the circuit and the AUT specification. Since most amplifiers are not nearly this fast, it is reasonable to assume that the circuit will always provide reliable results.

Because this circuit works by nulling opposite polarity sources, it seems unable to test followers—but it can. The AUT is battery-powered and completely floated from the circuit's power supply (Figure 4). The AUT output is connected to circuit ground and the battery center tap becomes the output. The positive input is driven from the Schottky bridge. The floating power supply lets the follower fool the circuit into thinking it is testing an inverter. The AUT's output appears inverted, but this is not a significant penalty.

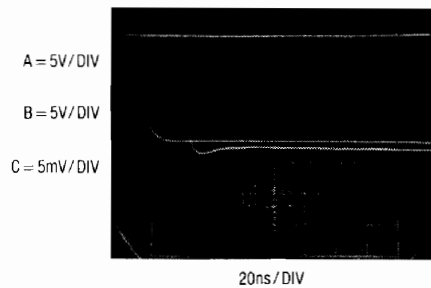


Figure 3. Settling Detail for a Fast Amplifier

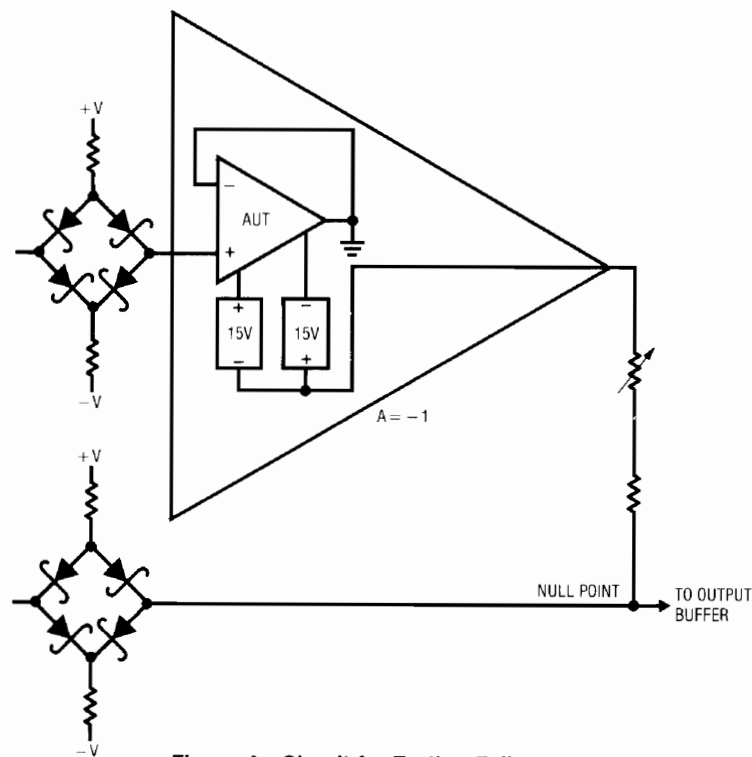


Figure 4. Circuit for Testing Followers

Application Note 10

To calibrate this circuit, ground point B and adjust the "zero trim" for 0V output. Next, temporarily tie the pulse input to +15V through 680Ω and adjust the "null trim" for 0V output. Remove the 680Ω resistor and the circuit is ready for use. When measuring settling times remember to experiment with the value of C_F to obtain best performance (see Box Section B, "Amplifier Compensation").

In the past, amplifier settling measurements below 1mV were not required. Recently, 16-bit and 18-bit D→A converters have become relatively common, requiring users to consider sub-millivolt settling time performance. Also, the offset specifications of current generation monolithic amplifiers are good enough to make very high precision settling time data worthwhile. Previously, being able to see an amplifier settle within 50μV wasn't interesting because its thermal drift swamped this figure.

The newer amplifier's substantially lower drift means very high precision settling time measurement data is useful. Figure 2's circuit is limited to 0.01% (1mV out of 10V) resolution by the 300mV Schottky clamp potential at point B. Simply increasing oscilloscope gain to get higher resolution will not work because of severe overload problems. With the oscilloscope set at 50μV/division, the

Schottky bound allows a 6000:1 overdrive. This is much more than any vertical amplifier is designed to accommodate. The oscilloscope's overload recovery will completely dominate the observed waveform and all measurements will be meaningless.

One way to obtain higher precision settling time measurements is to clip the incoming waveform in *time*, as well as amplitude. If the oscilloscope is prevented from seeing the waveform until settling is nearly complete, overload is avoided. Doing this requires placing a switch at the settle circuit's output and controlling it with an input-triggered, variable delay. FET switches are not suitable because of their gate-source capacitance. This capacitance will allow gate drive artifacts to corrupt the oscilloscope display, producing confusing readings. In the worst case, gate drive transients will be large enough to induce overload, defeating the switch's purpose.

Figure 5 shows a way to implement the switch which largely eliminates these problems. This circuit, connected to the basic settle circuit of Figure 2, allows settling within 10μV to be observed. The Schottky sampling bridge is the actual switch. The bridge's inherent balance, combined with matched diodes and very high

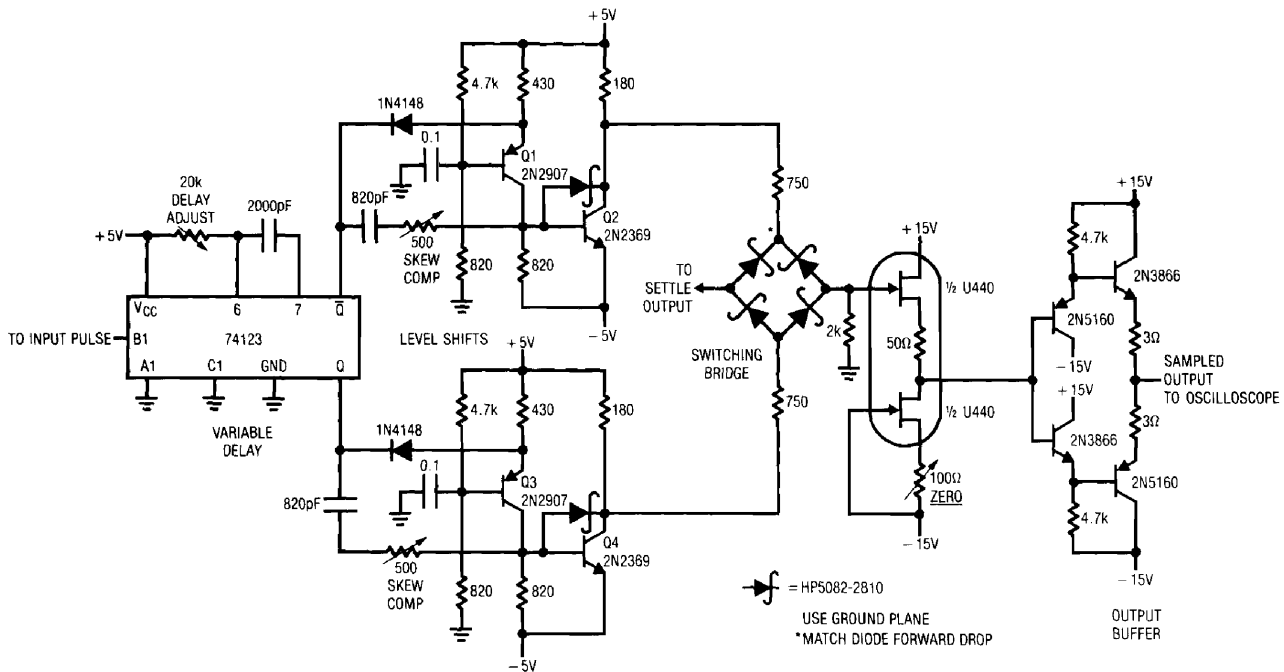


Figure 5. Sampling Switch for Ultra Precision Settling Time Measurement

speed complementary bridge switching, yields a clean, switched output. An output buffer stage, identical to the one used in Figure 2, unloads the bridge and drives the oscilloscope.

The complementary bridge switching drive is supplied from the Q1–Q2 and Q3–Q4 level shifters. Each circuit converts the delay one-shot's TTL output to $\pm 5V$ levels. The identical stages are comprised of an emitter-switched current source feeding a Baker-clamped common emitter output. Feedforward capacitance to the output transistor aids speed and overall delays are about 3ns. The level shifters must switch simultaneously to minimize drive-induced disturbances in the bridge's output. The "skew compensation" trims permit very small phasing adjustments in each level shifter, compensating skew in the 74123 one-shot's outputs. To trim this circuit, ground the bridge input and pulse the 74123's C1 input. Next, set the oscilloscope to $100\mu V$ /division and adjust the skew trims for minimum indication on the screen. Connect the bridge input back to the settle circuit's output and the circuit is ready for use.

Construction of this circuit requires care. A ground plane is mandatory and all bridge connections should be as

short and symmetrical as possible. To maintain low noise, the bridge's output ground return should be routed away from high current returns such as the 74123's ground pin.

This switch circuit, carefully constructed and used with the basic settle circuit, provides good results. Figure 6 shows an LT1001 precision op amp as the AUT. Trace A is the input pulse, while Trace B is the AUT output. During the AUT's slewing period the 74123 is fired (Trace C is Q), turning off the bridge. The bridge input appears in Trace D. The 74123 delay is adjusted so the bridge is switched when settling is nearly complete. Trace E is the circuit's final output, showing settling details at $100\mu V$ /division. The narrow peaking at the waveform's leading edge is due to switching residue. Figure 7 lists measured settling times to $50\mu V$ (0.0005% of a 10V step) for a group of precision amplifiers.

Some poorly designed amplifiers exhibit a substantial "thermal tail" after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking settling at high speed it

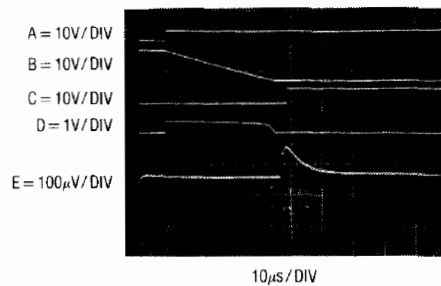


Figure 6. Sampling Switch Waveforms

Amplifier	Settling Time	Remarks
LT1001	65 μ s	
LT1007	18 μ s	
LT1008	65 μ s	Standard Compensation
LT1008	35 μ s	Feedforward Compensation
LT1012	70 μ s	
LT1055	6 μ s	
LT1056	5 μ s	

Figure 7. Measured Settling Times to 0.0005%

Application Note 10

is always a good idea to slow the oscilloscope sweep down and look for thermal tails. Often the thermal tail's effect can be accentuated by loading the amplifier's out-

put. Figure 8 shows the thermal tail of an amplifier which appears to have settled in a much shorter time than it actually has.

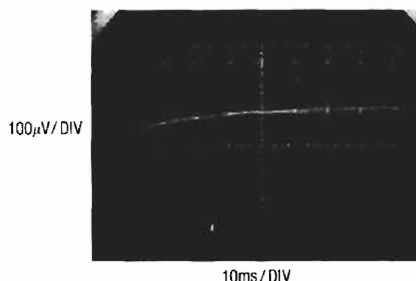


Figure 8. Typical Thermal Tail

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National Semiconductor, LF355/356/357 Data Sheet, "Settling Time Test Circuit."

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R. Demrow, "Settling Time of Operational Amplifiers," *Analog Dialogue*, volume 4-1, 1970 (Analog Devices).

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BOX SECTION A

Evaluating Oscilloscope Overload Performance

Settling time measurement relies heavily on the oscilloscope used. In many cases the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overload before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overload varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100X overload at 0.005V/division may be very different than at 0.1V/division. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overload must be

approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

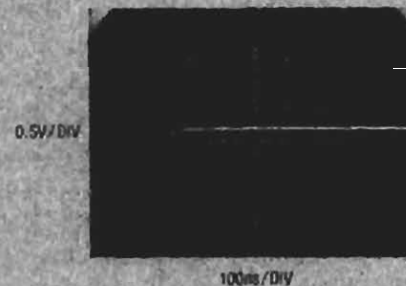
The waveform to be expanded is placed on the screen at a vertical sensitivity which eliminates all off-screen activity. Figure A1 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure A2) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure A3, gain has

been further increased, and all the features of Figure A2 are amplified accordingly. The basic wavelshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure A4 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure A3. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can

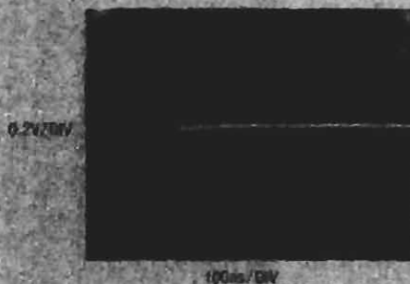
confirm that this waveform is being influenced by overloading. In Figure A5 the gain remains the same but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure A6). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.



A1



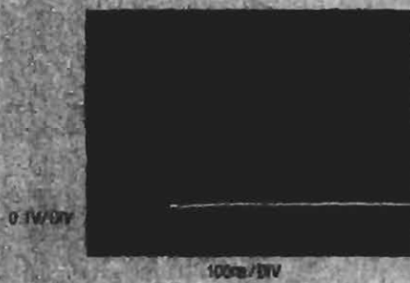
A2



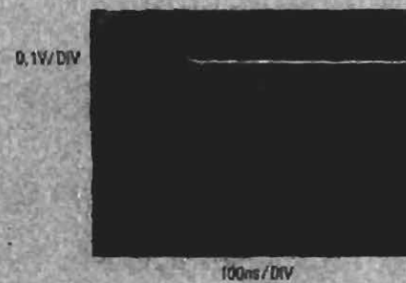
A3



A4



A5



A6

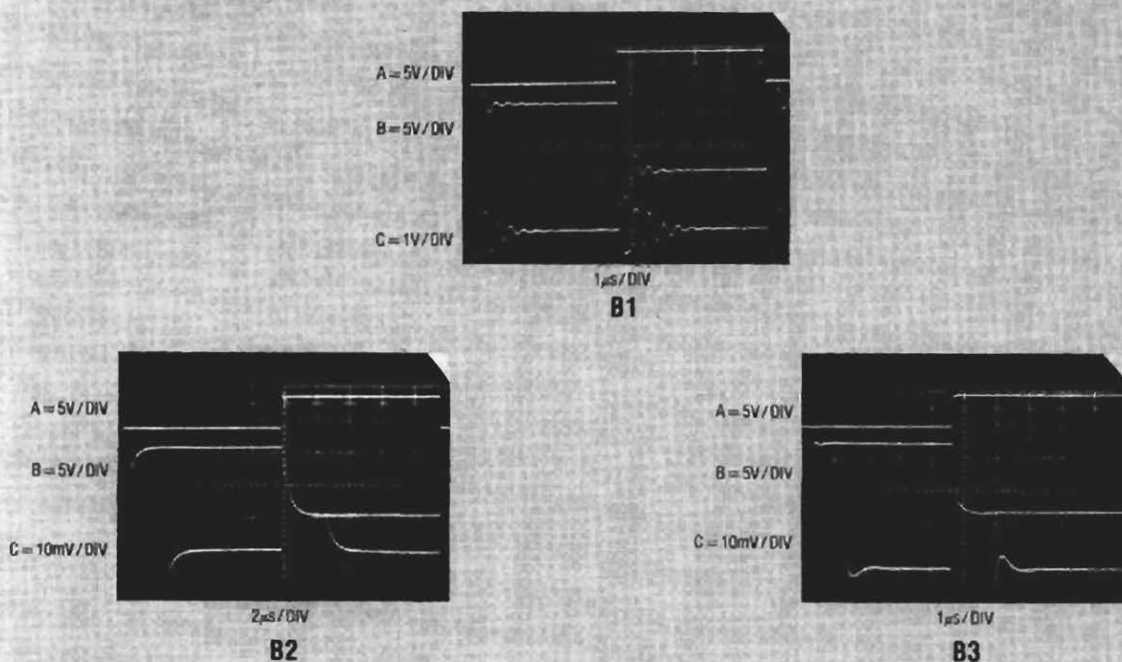
Figures A1-A6. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

BOX SECTION B

Amplifier Compensation

To get the best possible settling time from any amplifier, the feedback capacitor, C_F , should be carefully chosen. C_F 's purpose is to roll off amplifier gain at the frequency which permits best dynamic response. The optimum value for C_F will depend on the feedback resistor's value and the characteristics of the source. One of the most common sources is also one of the most difficult. Digital-to-analog converters' current outputs must often be converted to a voltage. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to "hunt" and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output

capacitance and it varies with code. Bipolar DACs typically have 20pF–30pF of capacitance, stable over all codes. Because of their output capacitance, DACs furnish an instructive example in amplifier compensation. In practice, the Schottky bridge which feeds the AUT in the settle circuit is replaced with the DAC to be used. Depending on DAC input coding, it may be necessary to use inverters in the DAC input lines to maintain circuit nulling action. Figure B1 shows the response of an industry standard DAC-80 type and an LT1023 op amp which is optimized for inverting applications. Trace A is the input, while Traces B and C are the amplifier and settle outputs, respectively. In this example no compensation capacitor is used and the amplifier rings badly before settling. In B2, an 82pF unit stops the ringing and settling time goes down to 4 μ s. The overdamped response means that C_F dominates the capacitance at the AUT's input and stability is assured. If fastest response is desired, C_F must be reduced. B3 shows critically damped behavior obtained with a 22pF unit. The settling time of 2 μ s is the best obtainable for this DAC-amplifier combination.



Figures B1-B3. Effects of Different Feedback Capacitors on a DAC-Op Amp Combination

Designing Linear Circuits for 5V Single Supply Operation

Jim Williams

In predominantly digital systems it is often necessary to include linear circuit functions. Traditionally, separate power supplies have been used to run the linear components (see Box, "Linear Power Supplies—Past, Present, and Future").

Recently, there has been increasing interest in powering linear circuits directly from the 5V logic rail. The logic rail is a difficult place for analog components to function. The high amplitude broadband current and voltage noise generated by logic clocking makes analog circuit operation difficult. (See Box, "Using Logic Supplies for Linear Functions".)

Generally speaking, analog circuitry which must achieve very high performance levels should be driven from dedicated supplies. The difficulties encountered in maintaining the lowest possible levels of noise and drift in an analog system are challenging enough without contending with a digitally corrupted power supply.

Many analog applications, however, can be successfully implemented using the logic supply. Combining components intended to provide high performance from the

logic rail with good design can give excellent results (see Box, "High Performance, Single Supply Analog Building Blocks"). The examples which follow show this in a variety of precision measurement and control circuits which function from a 5V supply.

Linearized RTD Signal Conditioner

Figure 1 shows a circuit which provides complete, linearized signal conditioning for a platinum RTD. One side of the RTD sensor is grounded, often desirable for noise considerations. The Q1-Q2 current source is referenced to A1's output. A1's operating point is primarily fixed by the 2.5V LT[®]1009 voltage reference. The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The nonlinearity causes several degrees of error over the circuit's 0°C to 400°C operating range. A2 amplifies R_P's output, while simultaneously supplying nonlinearity correction. The correction is implemented by feeding a portion of A2's output back to A1's input via the 10k-250k divider. This causes the Q1-Q2 current source

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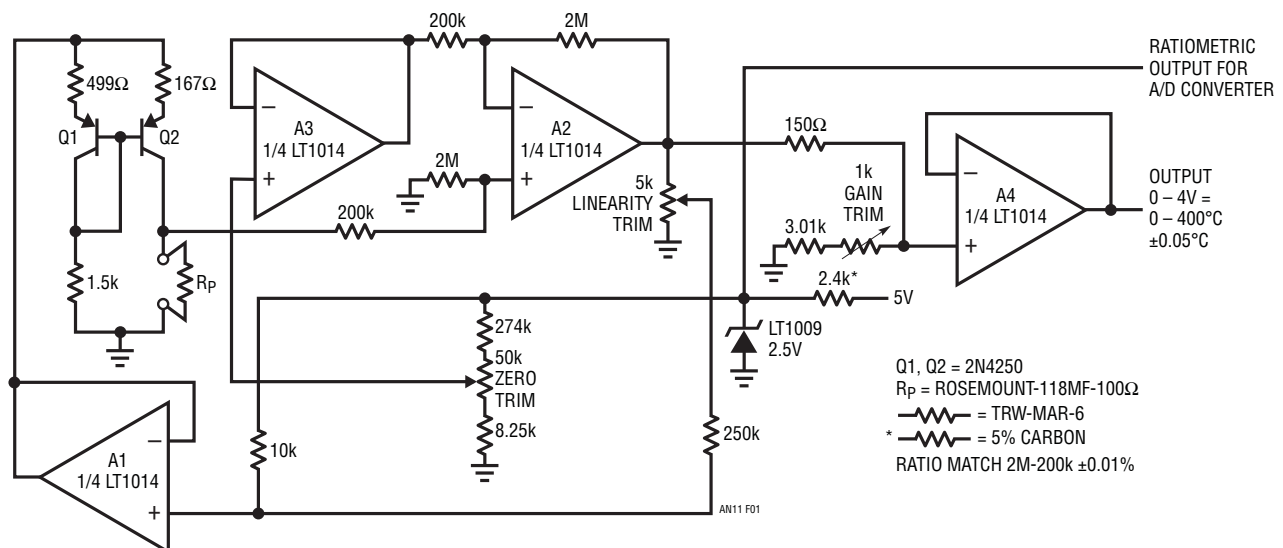


Figure 1. Linearized Platinum RTD Signal Conditioner

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Application Note 11

output to shift with R_p 's operating point, compensating sensor nonlinearity to within $\pm 0.05^\circ\text{C}$. A3, also referenced to the LT1004, voltage sums an offsetting signal at A2's negative input, allowing 0°C to equal 0V at A2's output. The resistive divider in A4's input line sets circuit gain, and the circuit's output is taken at A4.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432K) for R_p . Set the box to 0°C value (100.00Ω) and adjust the zero trim for a 0.0V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 1.400V output reading. Finally, set the box to 400°C (249.0Ω) and trim the linearity adjustment for a 4.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within $\pm 0.05^\circ\text{C}$. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω . This deviation, which is manufacturer-specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Linearized Output Methane Detector

Figure 2 is another 5V powered transducer circuit. Like the platinum RTD example, this circuit linearizes the transducer's output, but it performs a more complex mathematical operation. The circuit's frequency output is directly proportional to the methane concentration detected by the transducer specified. Figure 3 shows that the transducer output varies as:

$$\approx \frac{1}{\sqrt{\text{Concentration}}}$$

The circuit linearizes this function and its frequency output is also plotted.

The sensor's resistance vs methane concentration is converted to a voltage by A1. The LT1034 serves as a reference. A1's output feeds A2. The exponential relationship

between V_{BE} and collector current in transistors is utilized to generate a current in Q3's collector proportional to the square of A2's input current. This operation compensates the sensor's square root term. Q3's collector current sets the operating point of the A3-A4 oscillator. A3, an integrator, generates a positive going linear ramp (Trace A, Figure 4). The ramp is compared with Q3's current at A4's summing point (Trace B). A4 is configured as a current summing comparator. The feedback diode-bound network minimizes delay due to output slew time. When the ramp forces the summing point positive, A4's output (Trace C) swings negative. CMOS inverter A (Trace D) goes high, turning on the CD4016 switch to reset the A3 integrator. Simultaneously, inverter B goes low (Trace E), supplying AC positive feedback to A4's "+" input (Trace F). When the positive feedback decays, A4's output goes high, A3 begins to integrate, and the entire cycle repeats. Q3's collector current determines how long A3's ramp runs before A4 resets it. The ramp time is directly proportional to Q3's collector current, meaning that oscillation frequency is inversely ($1/X$) related to the current. The overall circuit transfer function is:

$$\frac{1}{X^2}$$

This linearizes the sensor's output. In practice, the sensor's response slightly deviates from the equation shown, actually being:

$$\frac{1}{1.9\sqrt{\text{Concentration}}}$$

The reset time constants at A4's input introduce enough oscillator "dead time" to partially compensate for the deviation. The dead time's frequency retarding characteristic effects the oscillator's high frequency range, providing a first order correction. The overall linearization achieved is within the sensor's manufacturing tolerances. The slight "bump" in the circuit's response curve is due to the mismatch between the sensor's term and the circuit's X^2 function.

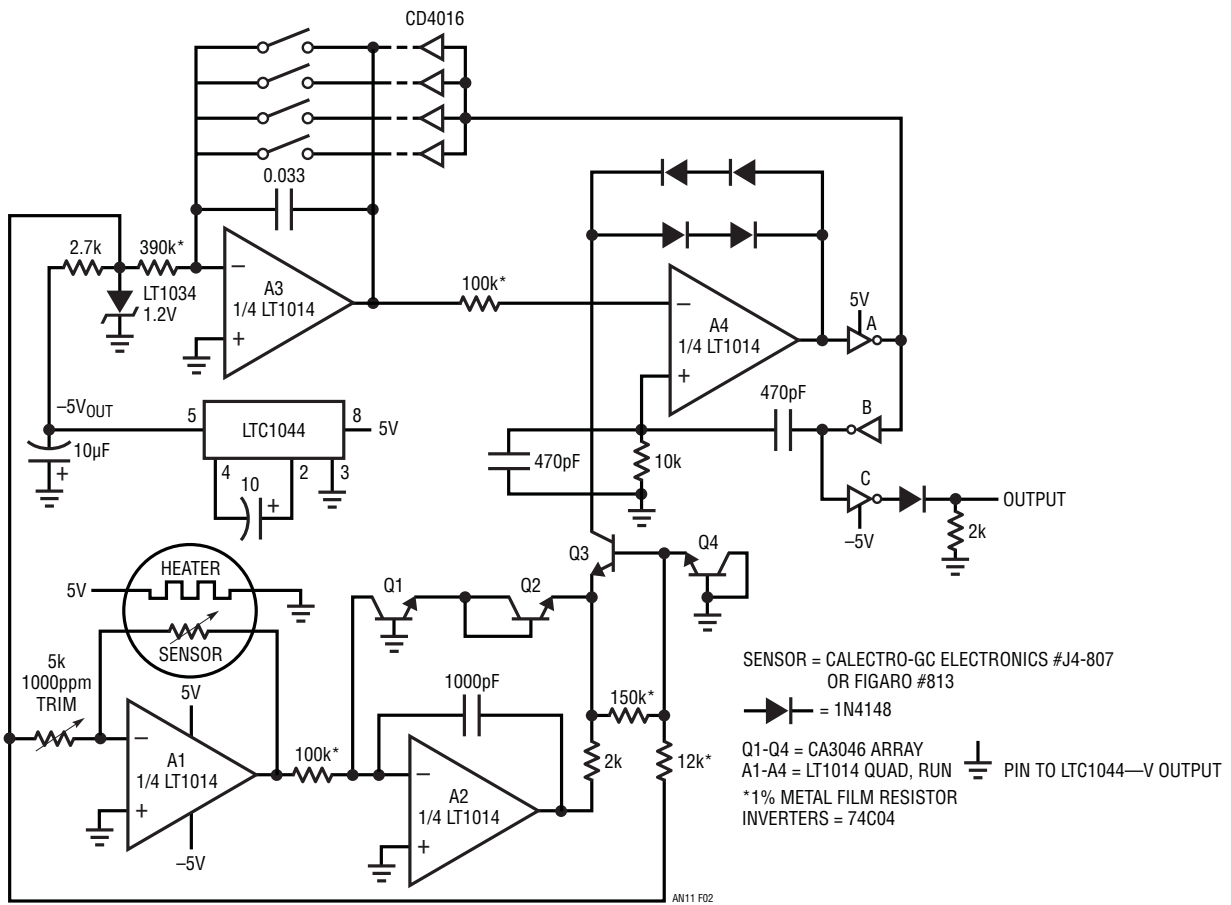


Figure 2. Linearized Methane Transducer Signal Conditioner

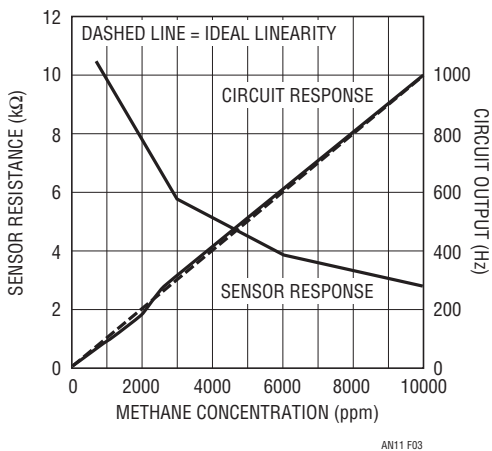


Figure 3. Transducer vs Circuit Response

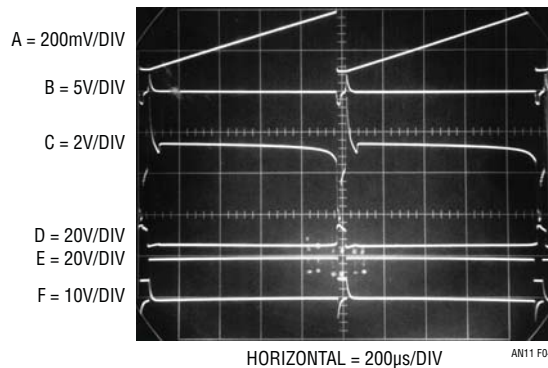


Figure 4. Linearized Methane Detector Waveforms

Application Note 11

The dead time correction in the oscillator smooths this error out above 4000ppm. The LTC[®]1044 voltage converter generates a negative supply directly from the 5V rail. This approach provides necessary negative circuit potentials while maintaining compatibility with 5V supply only operation. The sensor's heater is powered directly from the 5V rail, as specified by the manufacturer. To calibrate the circuit, place the sensor in a 1000ppm methane environment and adjust the 5k trim for a 100Hz output. Accuracy from 500ppm to 10,000ppm is limited by the sensor's 10% specification.

Cold Junction Compensated Thermocouple Signal Conditioner

Figure 5 shows a 5V powered, complete thermocouple signal conditioner. Cold junction compensation is included, and the circuit allows one leg of the thermocouple to be grounded, desirable for noise considerations. The LTC1043 combines the cold junction network differential output with the grounded thermocouple's signal at the LTC1052. The LTC1052 provides stable, low drift gain. To enable swing all the way to ground, the LTC1043's other switch section generates a small negative potential. This allows the LTC1052 output stage to run Class A for small outputs, permitting swing to 0V. The table gives proper values for R1 for various thermocouples. Output scaling may be set by R_F/R_I to whatever slope is desirable. Cold junction compensation holds within $\pm 1^\circ\text{C}$ over 0°C to 60°C .

5V Powered Precision Instrumentation Amplifier

Many transducer outputs require a true differential input "instrumentation" type amplifier. Transducers with single-ended outputs do not, in theory, require a differential input amplifier but common mode noise often exceeds the signal of interest. For these reasons, transducer systems often employ these type amplifiers.

No commercially manufactured instrumentation amplifier will function from a 5V supply and achieving good precision in a design is difficult. The circuits in Figure 6 meet these requirements. They also feature input protection, filtering capability and a shield driving output.

In Figure 6a, A1, A2 and A3 accomplish the differential input-to-single-ended output conversion, with R_G setting gain. The LT1014's high open-loop gain permits accurate circuit gain. Offset and drift performance allows use with low level transducers such as thermocouples and strain gauges. The $100\text{k}\Omega$ - $1\mu\text{F}$ combination filters noise and 60Hz pickup; the amplifier is never exposed to high frequency common mode noise. The transistor-diode clamps combine with the 100k resistors to prevent high voltage spikes or faults (common in industrial environments) from damaging the amplifiers. A4 is used as a shield driver to reduce the effects of input cable capacitance. It drives the shield at the input common mode voltage, which is derived from the input amplifier's output. Performance characteristics are summarized in the table.

Figure 6B achieves greater DC precision at the expense of bandwidth. Here, the LTC1043 switched-capacitor building block alternately commutates a $1\mu\text{F}$ capacitor between the circuit input and the LTC1052's input. This stage, accomplishing a differential-to-single-ended transition, allows the chopper-stabilized LTC1052 to take a ground referred measurement. The LTC1043's other switch stage generates a small negative potential, allowing the LTC1052 output to swing all the way to 0V. DC precision is excellent, surpassing all monolithic $\pm 15\text{V}$ instrumentation amps, although bandwidth is limited to 10Hz. The LTC1043's switching action, set at about 400Hz by the $0.01\mu\text{F}$ value, forms a lowpass filter. This permits extremely high rejection of noise, allowing the CMRR to remain above 120dB at 20kHz. Overall performance is summarized in the table.

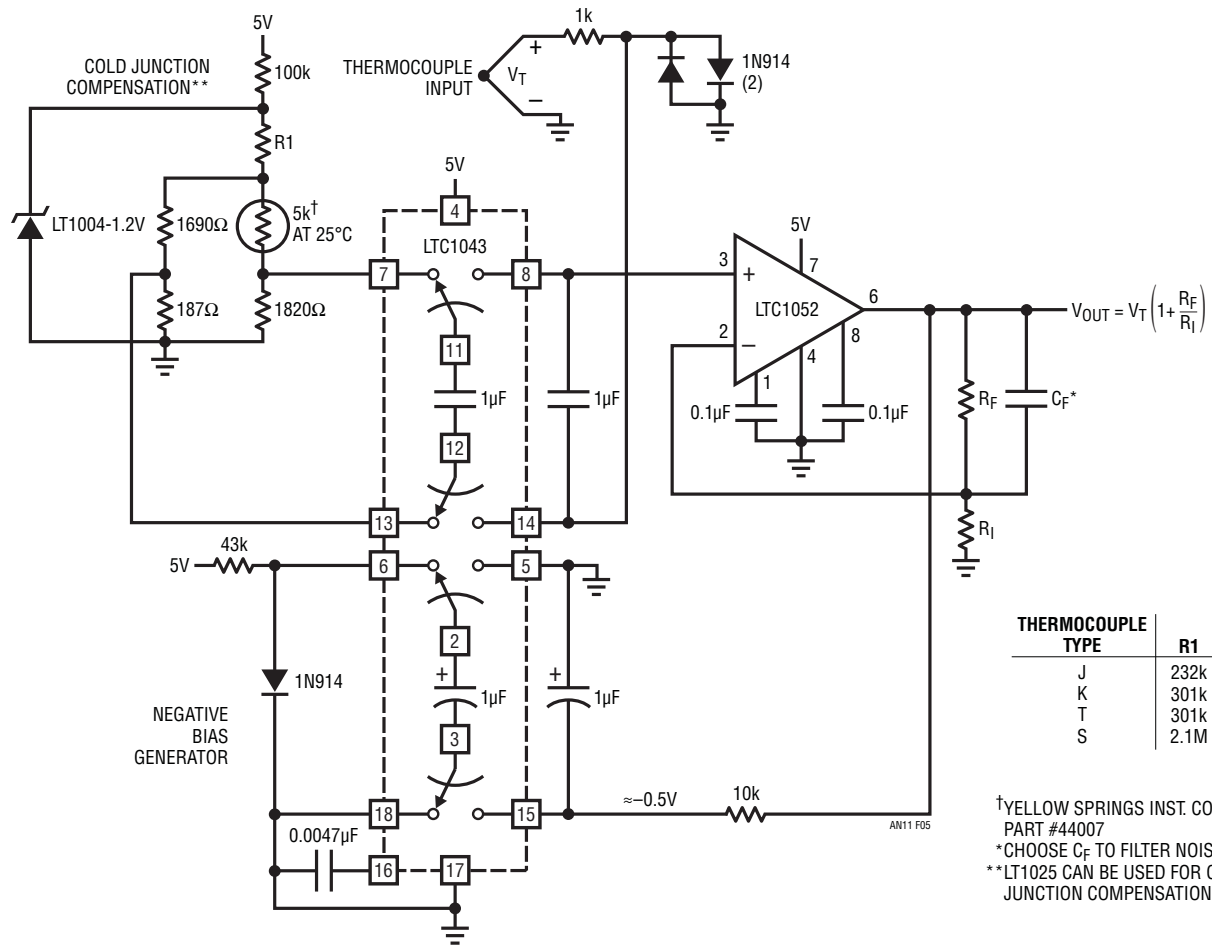


Figure 5. Cold Junction Compensated Thermocouple Signal Conditioner

Application Note 11

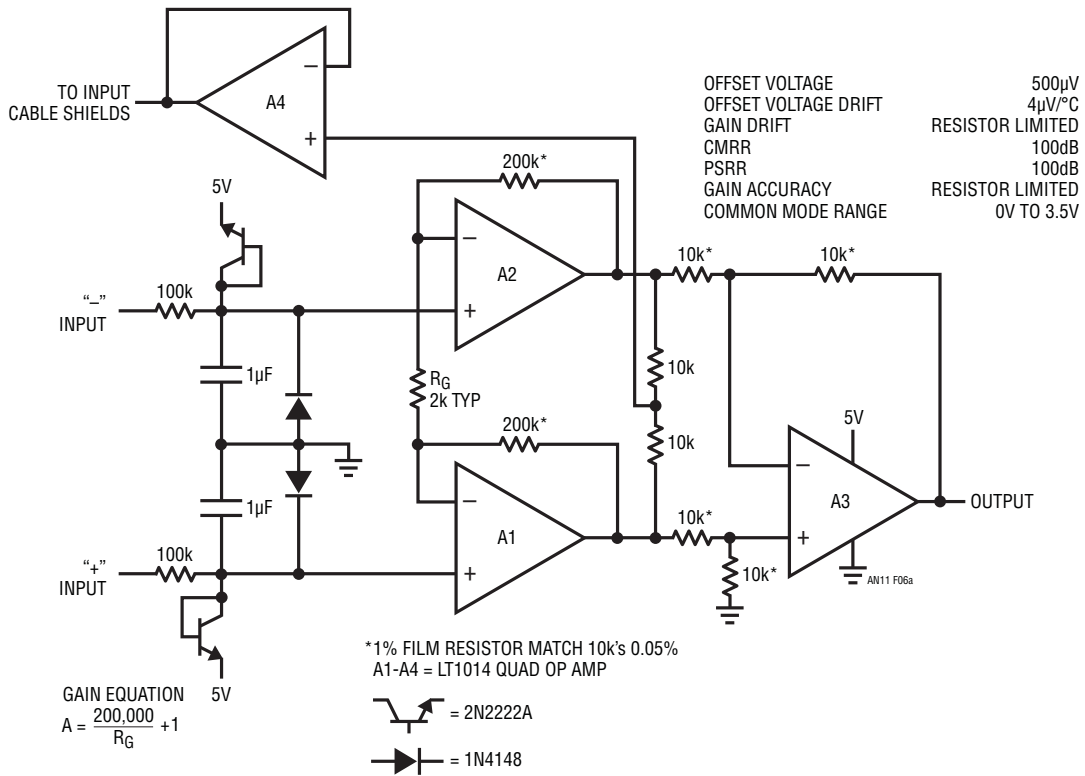


Figure 6a. Precision Instrumentation Amplifier

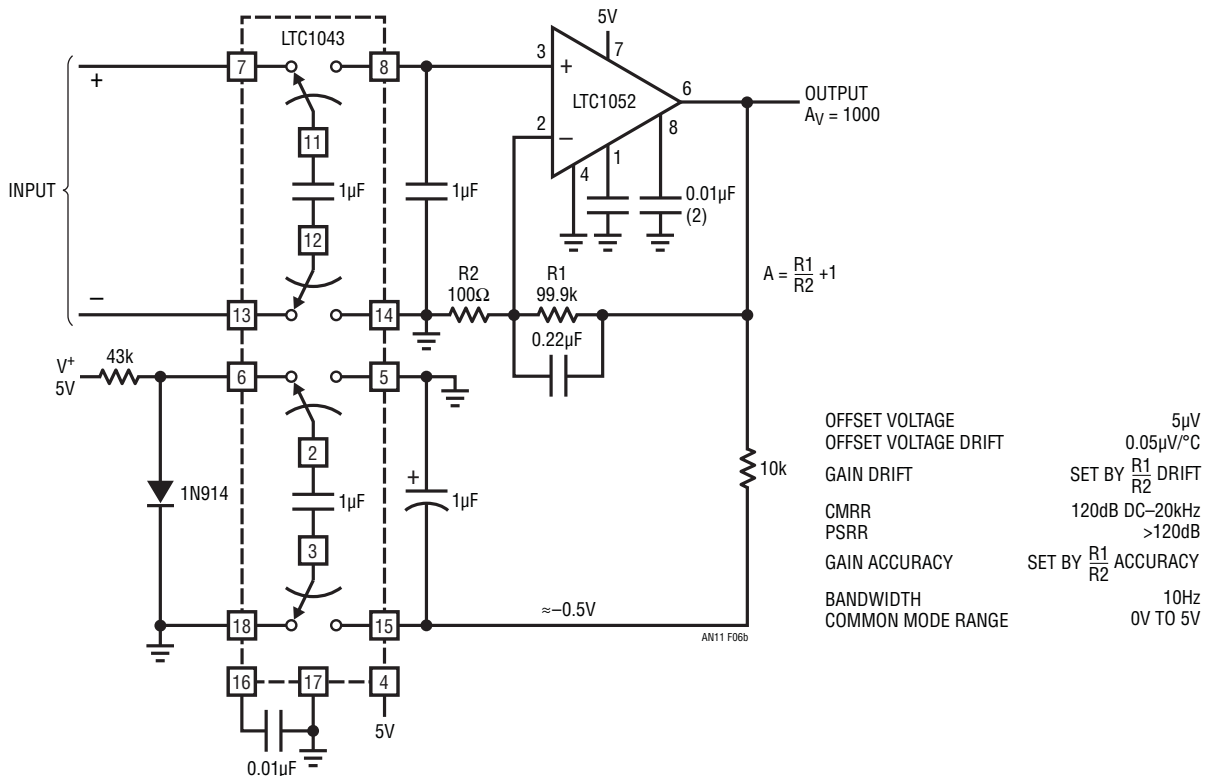


Figure 6b. Ultra-Precision Instrumentation Amplifier

5V Powered Strain Gauge Signal Conditioner

Figure 7 shows an unusual approach to signal conditioning the bridge output of a strain gauge pressure transducer. The 5V circuit needs only two amplifiers and provides an auxiliary ratio output for a monitoring A/D converter. The design functions by converting the bridge's differential output into a ground-referred single-ended signal which is then amplified. This approach eliminates common mode errors by eliminating the bridge's common mode output component. Additionally, the number of precision resistors required is minimized and no matching is required.

A1 biases the LTC1044 positive-to-negative converter. The LTC1044's output pulls the bridge's output negative, causing A1's input to balance at 0V. This local loop permits a single-ended amplifier (A2) to extract the bridge's output signal. The 100k-0.33μF RC filter's noise and A2's gain is set to provide the desired output scale factor. Because bridge drive is derived from the LT1034 reference, A2's output is not affected by supply shifts. The LT1034's output is

available for ratio operation. To calibrate this circuit, apply or electrically simulate 0psi and trim the zero adjustment for 0V output. Next, apply or electrically simulate 350psi and trim gain for 3.500V out. Repeat these adjustments until both points are fixed.

“Tachless” Motor Speed Controller

Figure 8 shows a way to servo control the speed of a DC motor. This circuit is particularly applicable to digitally controlled systems in robotic and X-Y positioning applications. By functioning from the 5V logic supply it eliminates additional motor drive supplies. The “tachless” feedback saves additional space and cost. The circuit senses the motor's back EMF to determine its speed. The difference between the speed and a setpoint is used to close a sampled loop around the motor. Because no commercially available sample-and-hold circuit will run from a 5V supply, special techniques are required.

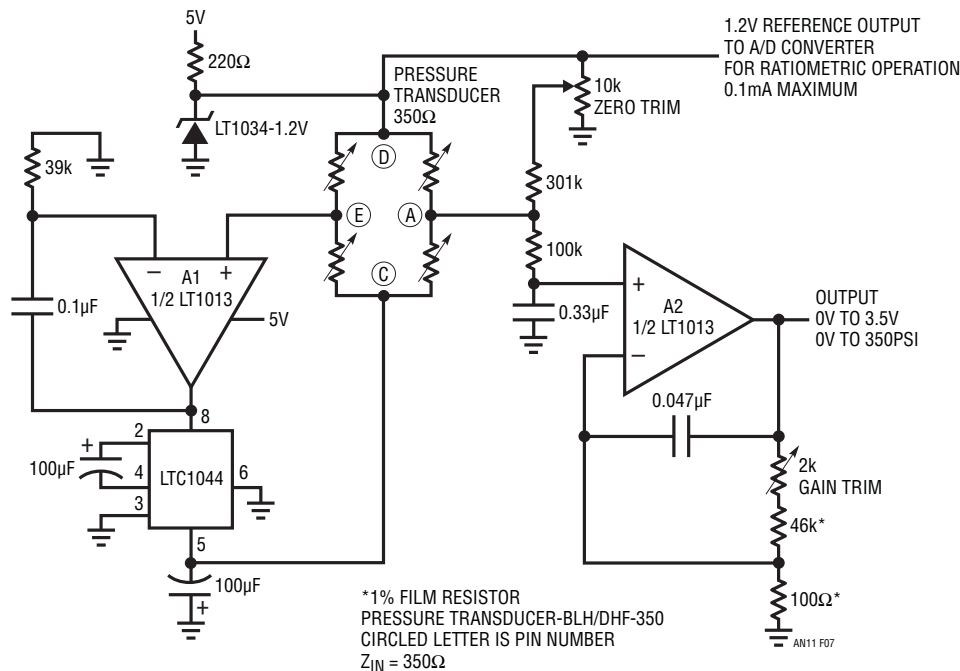


Figure 7. Strain Gauge Signal Conditioner

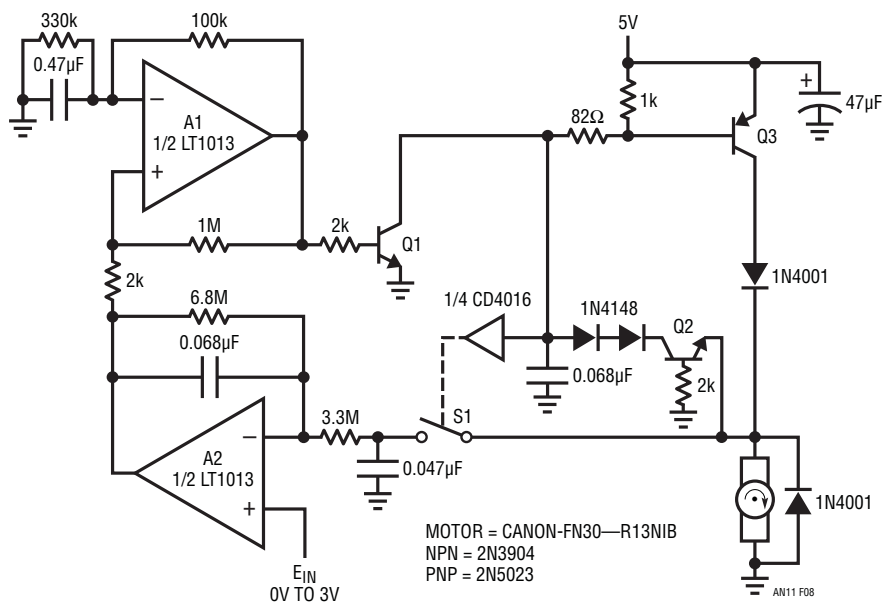


Figure 8. "Tachless" Motor Speed Controller

A1 generates a pulse train (Trace A, Figure 9). When A1's output is high, Q1 is biased and Q3 drives the motor's ungrounded terminal (Trace B). When A1 goes low, Q3 turns off and the motor's back EMF appears after the inductive flyback ceases. During this period, S1's input (Trace C) is turned on, and the 0.047 capacitor acquires the back EMF's value. A2 compares this value with the setpoint and the amplified difference (Trace D) changes A1's duty cycle, controlling motor speed. A2 has the desirable characteristic of assuming unity gain in the absence of a feedback signal. Start-up or input overdrive cannot force servo lock-up due to loss of sampling action. The loop is self-restoring and will establish control when abnormal conditions cease.

Drive to S1's control input must be carefully controlled for proper operation. Q2 prevents the switch from closing until the negative going flyback interval is over and the 0.068µF capacitor slows the switches turn-on edge. These measures ensure clean back EMF acquisition in the 0.047µF unit. Q2's collector line diodes compensate the motor's clamp diode drop, preventing destructive negative voltages at S1. The circuit controls from 20rpm to full speed with good transient response under all shaft loads. The gain and roll-off terms in A2's feedback loop are optimal for the motor listed, and should be reestablished for other types.

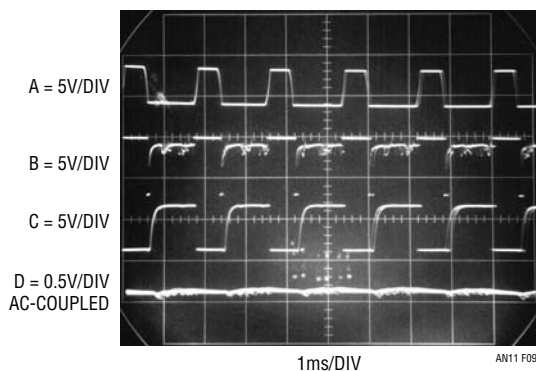


Figure 9. Motor Speed Controller Waveforms

Application Note 11

Figure 11 details modifications which permit the circuit's output current to galvanically float. This is often useful in industrial situations where the output lines may be exposed to common mode voltages or high voltage fault conditions. The transformer's primary current, which theoretically reflects current delivered by the secondary, is sensed across a shunt and fed back via A2. In practice,

current control precision is limited by non-ideal transformer behavior to about 1%. Common mode voltage is limited by T1's 300V breakdown.

Fully Isolated Limit Comparator

Figure 12's 5V powered circuit performs a fully isolated limit comparison on low level signals. It produces a digital

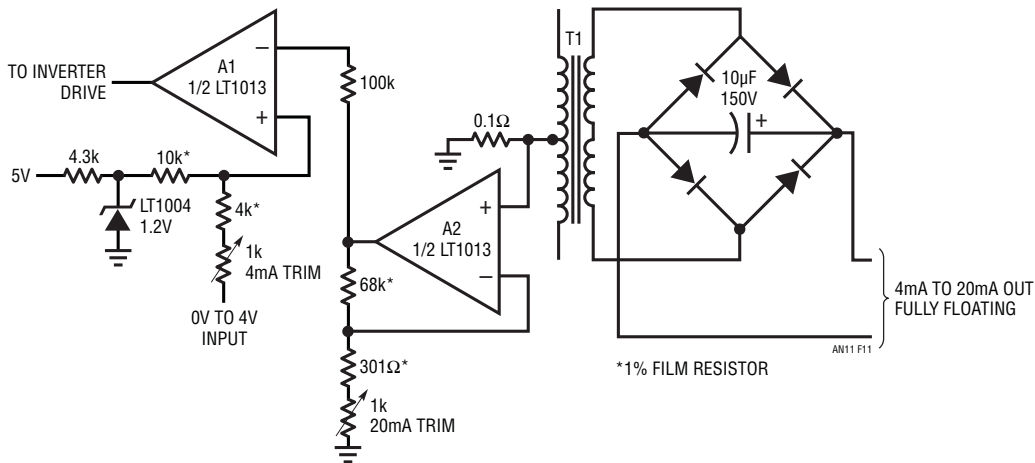


Figure 11. Floating Output Option for Current Loop Transmitter

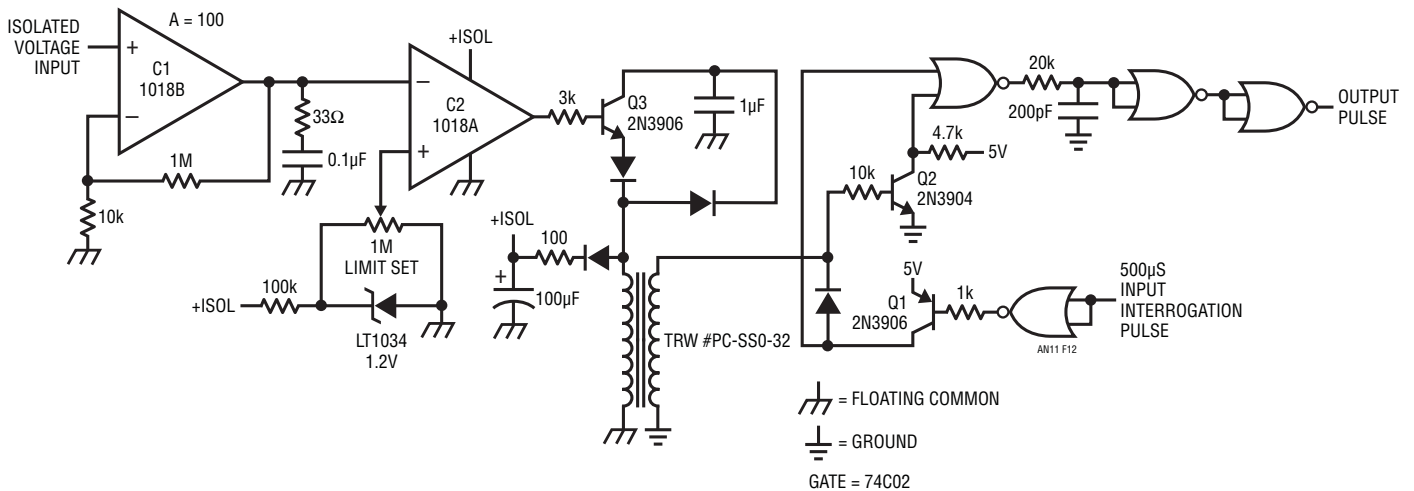


Figure 12. Fully Isolated Limit Comparator with Gain of 100

output indicating if the input is above or below a preset limit. This circuit is ideal for process control applications where transducers operate at high common mode voltages or where large ground loops exist. An uncommitted gain of 100 amplifier allow thermocouples and other low level sources to be used with the circuit. The circuit functions by echoing an interrogation pulse if the input is above a preset level. If the input is below this level, no echo pulse occurs. A transformer is used to allow a 2-way, galvanically isolated signal path and the energy contained in the interrogation pulse powers the circuit's floating elements. Figure 13 shows operating waveforms for the "above limit" case. When an input interrogation pulse is applied, Q1's collector drives the transformer primary (Figure 13, Trace A). Energy is transferred to the transformer's secondary and stored in the 100 μ F capacitor. The charge in the capacitor powers the isolated circuitry (" +ISOL" potential indicated

in Figure 12). If low power dual comparator C2's output is low, Q3 biases and drives current into the transformer secondary (Trace B). This is reflected in the transformer's primary (Trace C). Q2 and the associated gate circuitry form a demodulator which produces an output pulse (Trace D). If C2's output had been high (below limit set), the transformer would have received no secondary drive and there would be no output pulse. The demodulator is designed so that nothing appears on the output line unless the circuit is above the preset limit.

Comparator C1's output damper network allows it to function as an op amp for low level signals. This circuit easily extracts millivolt signals buried in high common mode voltage or ground noise and delivers its limit decision to the output. The maximum common mode voltage is limited by the transformer's 500V breakdown.

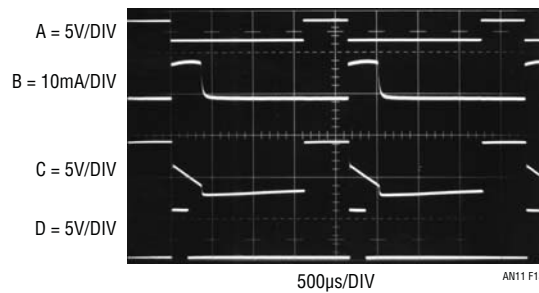


Figure 13. Isolated Limit Comparator Waveforms

Application Note 11

Fully Isolated 10-Bit A/D Converter

Figure 14's 5V powered circuit is a complete 10-bit A/D converter which is fully floating from system ground. It is ideal for performing 10-bit A/D conversions in the face of the high common mode noise characteristics of

predominantly digital systems. It is also useful in industrial environments, where noise and high common mode voltages are present in transducer fed systems.

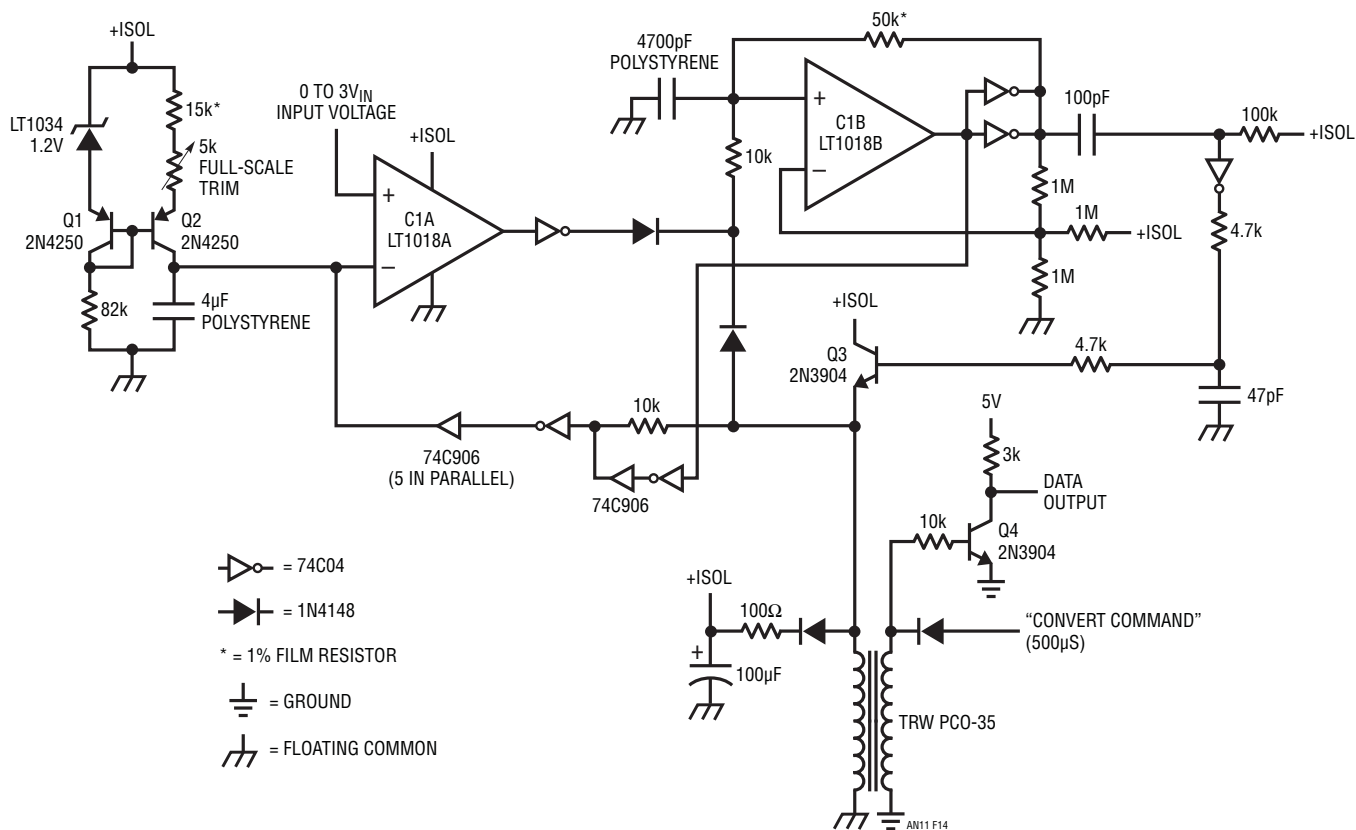


Figure 14. Fully Isolated A/D Converter

Circuit operation is initiated by applying a pulse to the “convert command” input (Trace A, Figure 15). This pulse appears at the transformer secondary and charges the 100 μ F capacitor. This potential is used to supply power to the floating A/D conversion circuitry. The transformer’s secondary pulse biases the inverter-open drain buffer combination to discharge the 4 μ F capacitor (Trace B). The secondary pulse also biases a diode to stop the C1B 3kHz oscillator output (Trace D). Concurrently, C1A goes high, forcing the inverter in its output line low (Trace C). When the convert command pulse ceases, the Q1-Q2 current source charges the 4 μ F capacitor with a linear ramp. The C1B oscillator now runs. When the ramp crosses the input voltage’s value, C1A’s output switches and its output line inverter (Trace C) goes high, cutting off the oscillator. The number of oscillator pulses occurring during this interval

is proportional to the input voltage value. These pulses are differentiated and fed to Q3, which drives the transformer. The differentiation causes narrow spikes to be fed to the transformer, easing power drain on the 100 μ F energy storage capacitor. Q3’s RC base delay and inverter-buffer combination at C1B’s output prevent Q3’s emitter pulses from triggering a ramp reset. The waveforms appearing at the transformer’s input do not reflect the circuit’s complex operation, and easily interface to a digital system. Figure 16, Trace A shows the “convert command” pulse. Trace B is the transformer primary. The differentiated oscillator pulses coming from the transformer secondary appear as small amplitude spikes. In this case, a small voltage is being converted and the number of pulses is small. Trace C, the “data output”, is taken at Q4’s collector, and the pulses are TTL compatible.

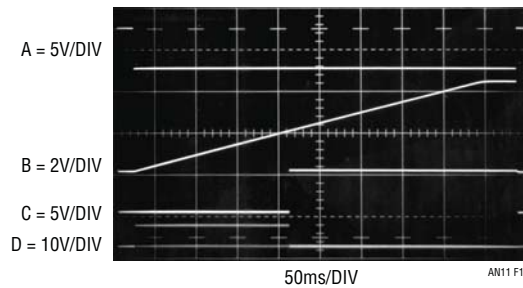


Figure 15. A/D Waveforms—Isolated Section

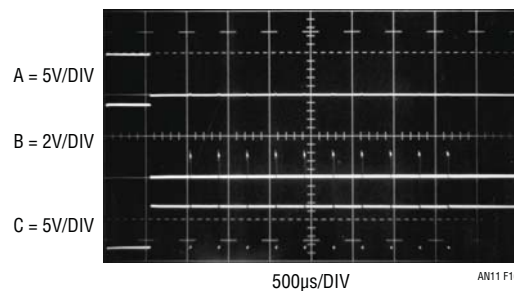


Figure 16. Detail of A/D Waveforms—Grounded Section

Linear Power Supplies—Past, Present, and Future

The amplitude of linear circuitry's power supplies has been determined by the available technology used for linear functions.

Probably the first standard linear supply was $\pm 300\text{V}$, used in analog computers. The operating characteristics of vacuum tubes necessitated high voltages. Additionally, because analog computers (from which operational amplifiers descended) were mathematical machines, bipolar supplies were desirable for computational purposes. With the arrival of solid state linear components in the early 1960s, new supply voltages were necessary and desirable. $\pm 15\text{V}$ was adapted because of transistor breakdown limits, as well as the availability of low voltage references (Zener and avalanche diodes). Power and size advantages afforded by the new supply standard were also obviously attractive. It is significant that while the supply drop decreased available dynamic range of operation by over 20dB, the usable signal processing range did not decrease. This was due to the lower noise and drift of the solid state components.

The arrival of monolithic linear circuits in the late 1960s and subsequent design refinements expanded the available territory at the lower end of the signal processing range.

Currently available precision linear components and technology shifts are causing reevaluation of the power supply issue. In particular, several trends argue for linear functions to be able to operate from the low voltage digital rail. The increasing digital content of systems makes 5V compatible linear components attractive. Cost and space considerations in these systems often make separate linear supplies undesirable. This situation is not universal, and never will be, but is increasingly common.

A move to lower voltages for digital circuits, which must occur, underscores the need for low voltage, high performance linear ICs. Drops in digital supply value will be forced by increasing density requirements, which will lower IC breakdown limits.

Lower power consumption in systems goes along with supply voltage and density issues. Increasingly

complex systems are being put into smaller physical spaces, necessitating attention to dissipation. In many instances, portable operation is desirable, so circuitry must be directly compatible with battery potentials, as well as lower power. Linear components must not give up performance to function in this low voltage, digitally driven environment. Demands for precision remain high, and low voltage linear circuits, despite their narrowed dynamic operating range, must meet these requirements. This is not easy, considering that a 12-bit $\pm 15\text{V}$ system typically has a 2.5mV/LSB error budget. At 5V, this number shrinks to 1mV. To deal with this, design techniques developed for $\pm 15\text{V}$ components are being used in new, low voltage ICs and new approaches will also be employed.

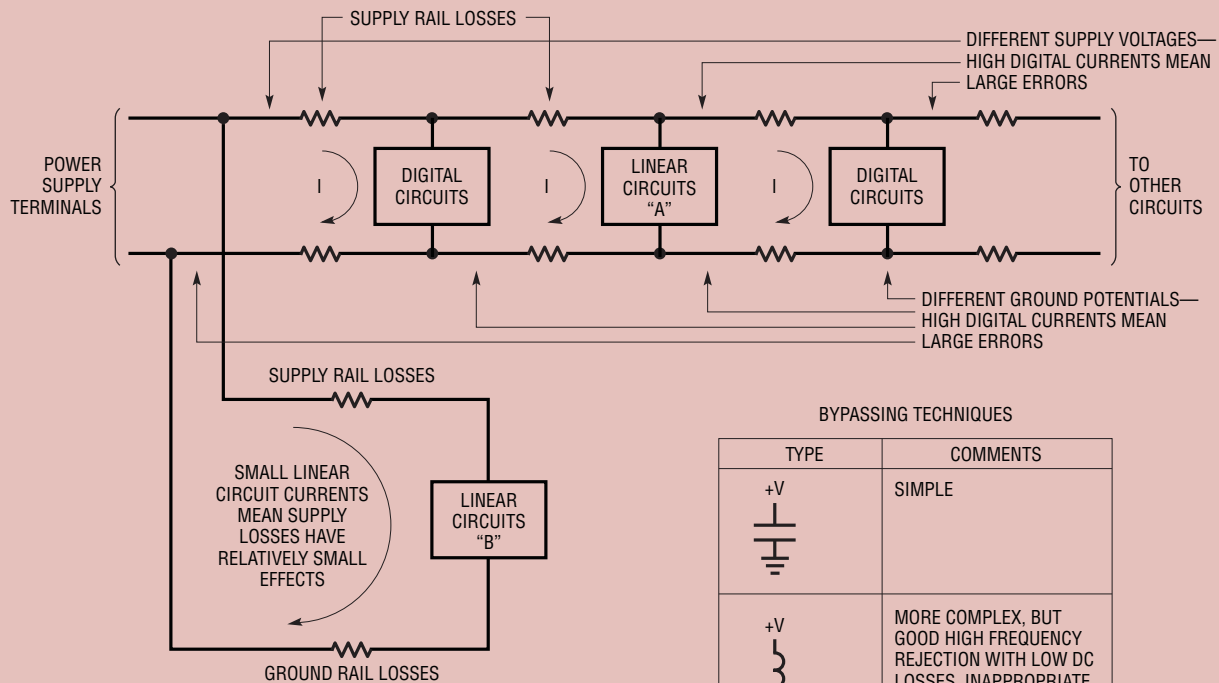
Using Logic Supplies for Linear Functions

The fast clocking and transient high currents characteristic of digital systems make logic supplies an unfriendly place for linear components to operate. A key to achieving good results is considering power bus routing as an integral part of the signal processing chain. The figure shows that supply rail impedances will cause both DC and AC errors at various points in a system. This is true of any power distribution scheme, but is especially troublesome in digitally oriented systems, where fast current spiking and clock harmonics are present. Circuitry located at position "A" will see appreciable positive rail noise and ground potential will be corrupted by fast, relatively high currents returning through conductor impedances. Supply bypassing can reduce positive rail noise, but ground potential uncertainty can cause unacceptable errors. Locating linear circuits as shown in "B" reduces both positive and ground rail problems by eliminating the digitally derived currents. The linear devices lower operating currents allow lower errors due to supply distribution impedances. Appropriate bypassing techniques are also shown. LC filters can be substantially more effective than simple capacitors, especially in cases where it is not practical to route the positive rail directly from the supply. RC filtering forces voltage drop across the resistor, but is often acceptable due to the linear components low power requirements.

Application Note 11

In many cases it is not possible to arrange a “clean” supply for the linear components. In such circumstances it may be possible to synchronize noise sensitive linear circuit operations to occur between system clock pulses. This approach utilizes the synchronous nature of most digital systems and the fact that supply bus disturbances are often minimized between clock pulses.

Probably the most effective technique for dealing with digital supply noise is to galvanically isolate the linear circuits from the supply. The most obvious way to do this is provision of separate power supplies for the linear circuits, but this is often unacceptable. Instead, transformer and optical isolation circuit techniques allow logic rail driven, galvanically isolated circuits (see Figures 11, 12 and 14).



BYPASSING TECHNIQUES

TYPE	COMMENTS
	SIMPLE
	MORE COMPLEX, BUT GOOD HIGH FREQUENCY REJECTION WITH LOW DC LOSSES. INAPPROPRIATE FOR USE WITH FAST LINEAR CIRCUITRY
	RC FILTER EFFECTIVE FOR HIGH FREQUENCY REJECTION BUT HAS DC LOSSES. LOW CURRENT LINEAR CIRCUITS CAN ALLOW THIS APPROACH. DO NOT USE WITH FAST LINEAR

AN11 F17

Circuit Techniques for Clock Sources

Jim Williams

Almost all digital or communication systems require some form of clock source. Generating accurate and stable clock signals is often a difficult design problem.

Quartz crystals are the basis for most clock sources. The combination of high Q, stability vs time and temperature, and wide available frequency range make crystals a price-performance bargain. Unfortunately, relatively little information has appeared on circuitry for crystals and engineers often view crystal circuitry as a black art, best left to a few skilled practitioners (see box, "About Quartz Crystals").

In fact, the highest performance crystal clock circuitry does demand a variety of complex considerations and subtle implementation techniques. Most applications, however, don't require this level of attention and are relatively easy to serve. Figure 1 shows five (5) forms of simple crystal clocks. Types 1a through 1d are commonly referred to as gate oscillators. Although these types are popular, they are often associated with temperamental operation, spurious modes or outright failure to oscillate. The primary reason for this is the inability to reliably identify the analog characteristics of the gates used as gain elements. It is not uncommon in circuits of this type for gates from different manufacturers to produce markedly different circuit operation. In other cases, the circuit works, but is influenced by the status of other gates in the same package. Other circuits seem to prefer certain gate locations within the package. In consideration of these difficulties, gate oscillators are generally not the best possible choice in a production design; nevertheless, they offer low discrete component count, are used in a variety of situations, and bear mention. Figure 1a shows a CMOS Schmitt trigger biased into its linear region. The capacitor adds phase shift and the circuit oscillates at the crystal resonant frequency. Figure 1b shows a similar version for higher frequencies. The gate gives inverting gain, with the capacitors providing additional phase shift to produce oscillation. In Figure 1c, a TTL gate is used to allow the 10MHz operating frequency. The low input resistance of TTL elements does not allow the high value, single resistor biasing method. The R-C-R network shown is a

replacement for this function. Figure 1d is a version using two gates. Such circuits are particularly vulnerable to spurious operation but are attractive from a component count standpoint. The two linearly biased gates provide 360 degrees of phase shift with the feedback path coming through the crystal. The capacitor simply blocks DC in the gain path. Figure 1e shows a circuit based on discrete components. Contrasted against the other circuits, it provides a good example of the design flexibility and certainty available with components specified in the linear domain. This circuit will oscillate over a wide range of crystal frequencies, typically 2MHz to 20MHz.

The 2.2k and 33k resistors and the diodes compose a pseudo current source which supplies base drive.

At 25°C the base current is:

$$\frac{1.2V - 1V_{BE}}{33k} = 18\mu A$$

To saturate the transistor, which would stop the oscillator, requires V_{CE} to go to near zero. The collector current necessary to do this is:

$$I_C(\text{sat}) = \frac{5V}{1k} (\text{delete } V_{CE} \text{ sat}) \\ = 5mA$$

with 18μA of base drive a beta of:

$$\frac{5mA}{18\mu A} = 278 \text{ is required.}$$

At 1mA the DC beta spread of 2N3904's is 70 to ≈210.

The transistor should not saturate...even at supply voltages below 3V.

In similar fashion, the effects of temperature may also be determined.

V_{BE} vs temperature over 25°C – 70°C is:

$$-2.2mV/^\circ C \cdot 45^\circ = -99mV.$$

Application Note 12

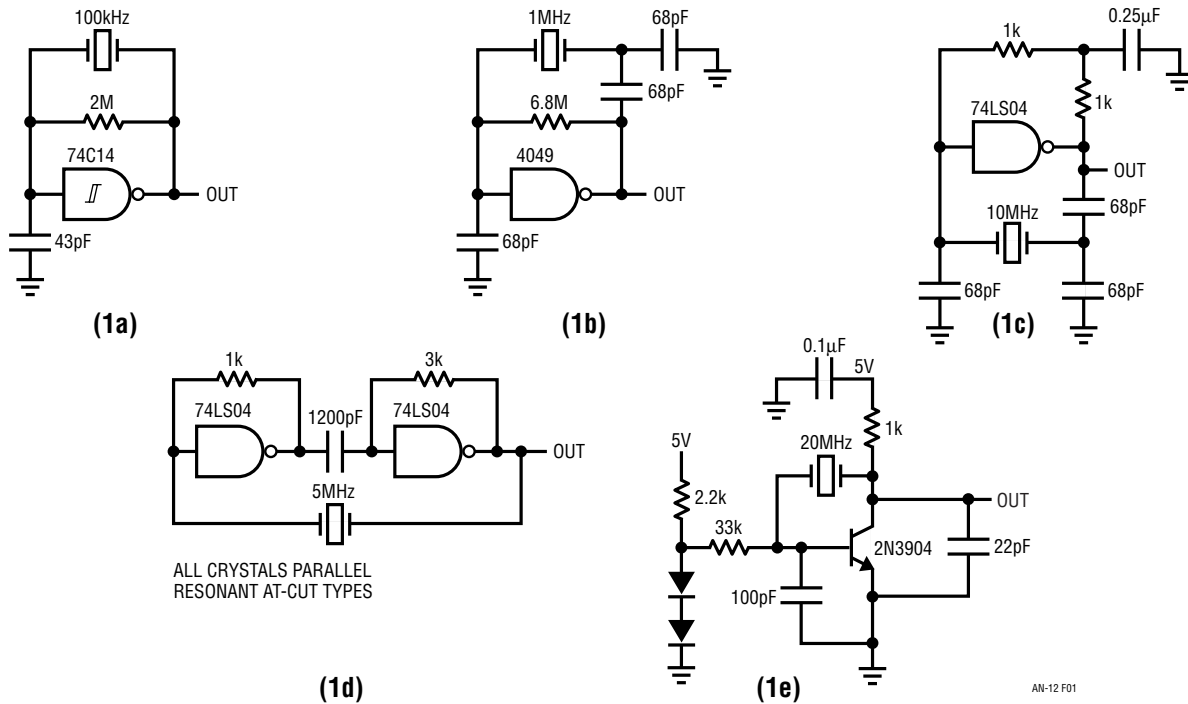


Figure 1. Typical Gate Oscillators and the Preferred Discrete Unit

The compliance voltage of the current source will move:

$$2 \cdot -2.2\text{mV}/^\circ\text{C} \cdot 45^\circ\text{C} = -198\text{mV}.$$

Hence, a first order compensation occurs:

$$-198\text{mV} - 99\text{mV} = -99\text{mV total shift}.$$

This remaining -99mV over temperature causes a shift in base current:

$$25^\circ\text{C current} = \frac{0.6\text{V}}{33\text{k}} = 18\mu\text{A}$$

$$70^\circ\text{C current} = \frac{0.5\text{V}}{33\text{k}} = 15\mu\text{A}$$

$$18\mu\text{A} - 15\mu\text{A} = 3\mu\text{A}$$

This $3\mu\text{A}$ shift (about 16%) provides a compensation for transistor h_{FE} shift with temperature, which moves about 20% from 25°C to 70°C . Thus the circuit's behavior over temperature is quite predictable. The resistor, diode and V_{BE} tolerances mean that only first order compensations for V_{BE} and h_{FE} over temperature are appropriate.

Figure 2 shows another approach. This circuit uses a standard RC-comparator multivibrator circuit with the crystal connected directly across the timing capacitor.

Because the free running frequency of the circuit is close to the crystal's resonance, the crystal "steals" energy from the RC, forcing it to run at the crystal's frequency. The crystal activity is readily apparent in Trace A of Figure 3, which is the LT[®]1011's "-" input. Trace B is the LT1011's output. In circuits of this type, it is important to ensure that enough current is available to quickly start the crystal resonating while simultaneously maintaining an RC time constant of appropriate frequency. Typically, the free running frequency should be set 5% to 10% above crystal resonance with a resistor feedback value calculated to allow about $100\mu\text{A}$ into the capacitor-crystal network. This type of circuit is not recommended for use above a few hundred kHz because of comparator delays.

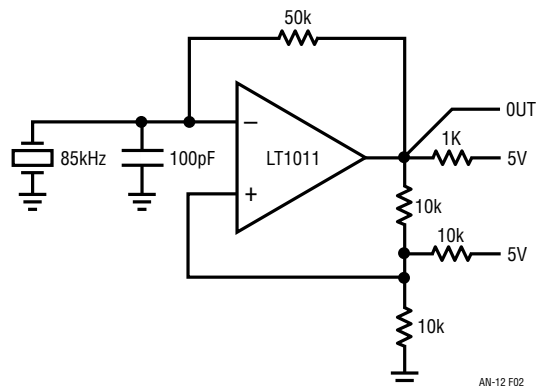


Figure 2. Crystal Stabilized Relaxation Oscillator

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Figures 4a and 4b use another comparator based approach. In Figure 4a, the LT1016 comparator is set up with DC negative feedback. The 2k resistors set the common mode level at the device's positive input. Without the crystal, the circuit may be considered as a very wideband (50GHz GBW) unity gain follower biased at 2.5V. With the crystal inserted, positive feedback occurs and oscillation commences. Figure 4a is useful with AT-cut fundamental mode crystals up to 10MHz. Figure 4b is similar, but supports oscillation frequencies to 25MHz. Above 10MHz,

AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, insuring proper operation.

All of the preceding circuits will typically provide temperature coefficients of 1ppm/°C with long term (1 year) stability of 5ppm to 10ppm. Higher stability is achievable with more attention to circuit design and control of temperature. Figure 5 shows a Pierce class circuit with fine frequency trimming provided by the paralleled fixed and

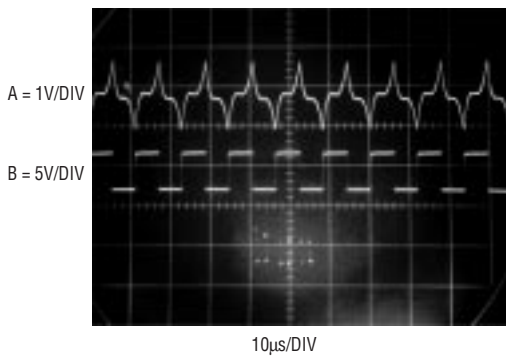


Figure 3. Figure 2's Waveforms

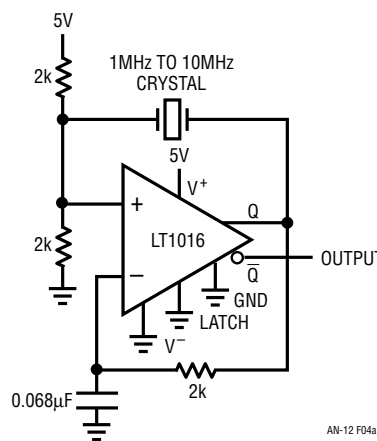


Figure 4a. 1MHz to 10MHz Crystal Oscillator

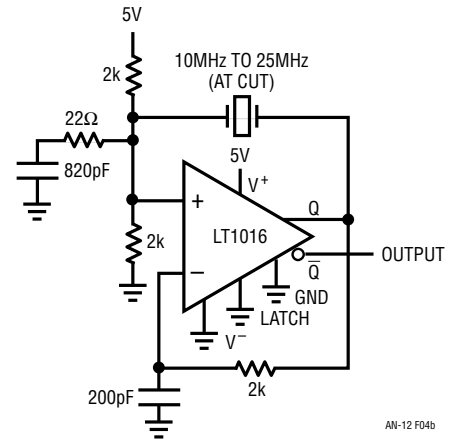
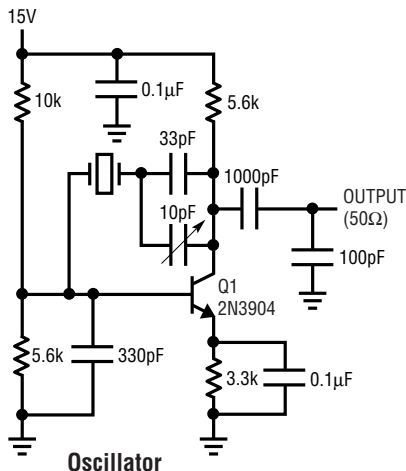


Figure 4b. 10MHz to 25MHz Crystal Oscillator



* TRW MAR-6 RESISTOR
 R_T = YELLOW SPRINGS INST. #44014 75°C = 35.39k
 = BLILEY #BG61AH-55, 75°C TURNING POINT. 5MHz FREQUENCY

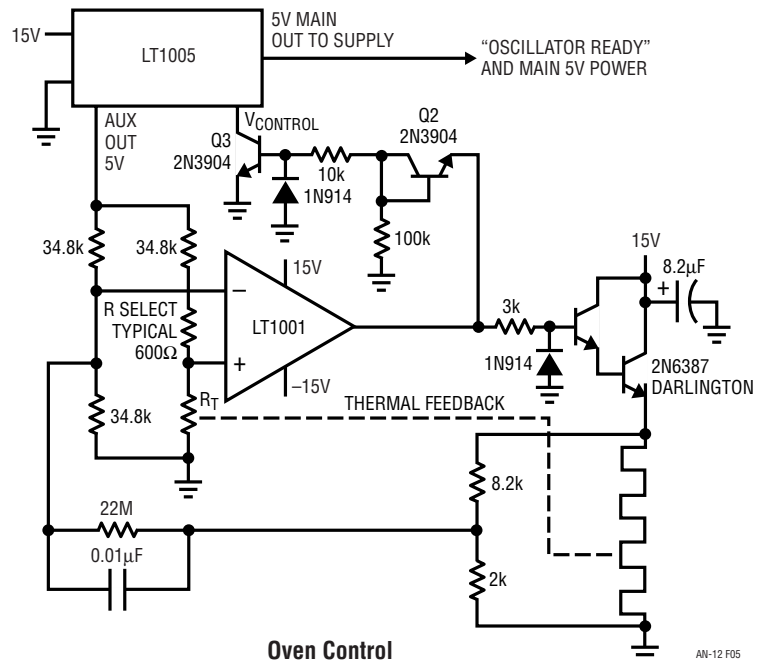


Figure 5. Ovenized Oscillator

Application Note 12

variable capacitors. The transistor provides 180° of phase shift with the loop components adding another 180°, resulting in oscillation. The LT1005 voltage regulator and the LT1001 op amp are used in a precision temperature servo to control crystal temperature. The LT1001 extracts the differential bridge signal and drives the Darlington stage to power the heater, which is monitored by the thermistor. In practice, the sensor is tightly coupled to the heater. The RC feedback values should be optimized for the thermal characteristics of the oven. In this case, the oven was constructed of aluminum tube stock 3" long × 1" wide × 1/8" thick. The heater windings were distributed around the cylinder and the assembly placed within a small insulating Dewar flask. This allows 75°C setpoint (the zero TC or "turnover" temperature of the crystal specified) control of 0.05°C over 0°C to 70°C. The LT1005 regulator sources bridge drive from its auxiliary output and also keeps system power off until the crystal's temperature (hence, its frequency) is stabilized. When power is applied the negative TC thermistor is high in value, causing the LT1001 to saturate positive. This turns on zener-connected Q2, biasing Q3. Q3's collector current pulls the regulator's control pin low, disabling its output. When the oven arrives at its control point, the LT1001's output comes out of saturation and servo controls the oven at a point well below Q2's zener value. This turns off Q3, enabling the regulator to source power to whatever

system the clock is associated with. For the crystal and circuit values specified, this clock will drift less than 1×10^{-9} over 0°C to 70°C with a time drift of 1 part 10^{-9} week.

The oven approach to removing temperature effects of crystal clock frequency is the most effective and in wide use. Ovens do, however, require substantial power and warm-up time. In some situations, this is unacceptable. Another approach to offsetting temperature effects is to measure ambient temperature and insert a scaled compensation factor into the crystal clock's frequency trimming network. This open loop correction technique relies on matching the clock frequency vs temperature characteristic, which is quite repeatable. Figure 6 shows a temperature compensated crystal oscillator (TXCO) which uses a first order linear fit to correct for temperature. The oscillator is a Colpitts type, with a capacitive tapped tank network. The LT319A picks off the output and the RC network at the LT319's "-" input provides a signal adaptive trip threshold. The LT1005 regulator's auxiliary output buffers supply variations and the main regulator output control pin allows the system to be shut down without removing power from the oscillator, aiding overall stability. The ambient temperature is sensed by the linear thermistor network in A1's feedback loop with A2 used for scaling and offsetting. A2's voltage output expresses the

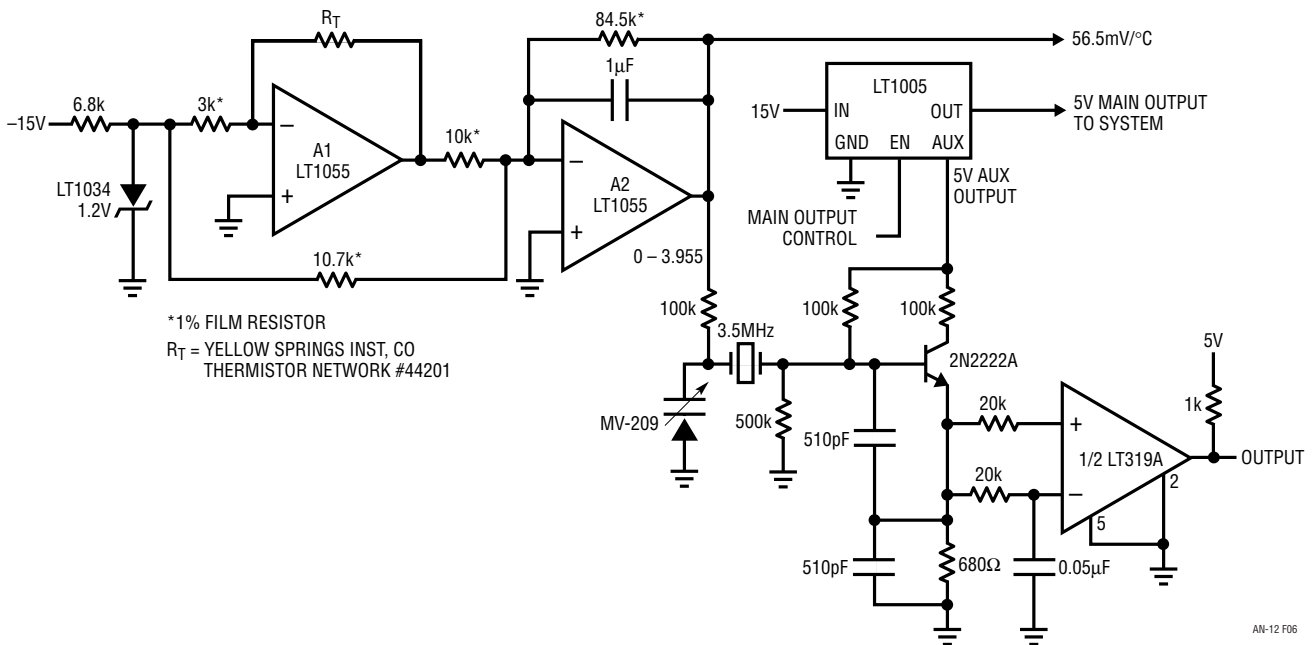


Figure 6. Temperature Compensated Crystal Oscillator (TXCO)

AN-12 F06

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ambient temperature information required to compensate the clock. The correction is implemented by biasing the varactor diode (a varactor diode's capacitance varies with reverse bias) which is in series with the crystal. The varactor's shift in capacitance is used to pull the crystal's frequency in a complementary fashion to the circuit's temperature error. If the thermistor is maintained isothermally with the circuit, compensation is very effective. Figure 7 shows the results. The -40ppm frequency shift over 0°C to 70°C is corrected to within 2ppm . Better compensation is achievable by including 2nd and 3rd order terms in the temperature to voltage conversion to more accurately complement the nonlinear frequency drift characteristic.

Figure 8 is another voltage-varactor tuned circuit but is configured to allow frequency shift instead of opposing it. This voltage controlled crystal oscillator (VXCO) has a

clean 20MHz sine wave output (Figure 9) suitable for communications applications. The curve of Figure 10 shows a 7kHz shift from 20MHz over the 10V tuning range. The 25pF trimmer sets the 20MHz zero bias frequency. In many applications, such as phase-locking and narrow bandwidth FM secure communications, the nonlinear response is irrelevant. Improved linearity will require conditioning the tuning voltage or the varactor network's response. In circuits of this type it is important to remember that the limit on pulling frequency is set by the crystals Q , which is high. Achieving wide dynamic "pull" range without stopping the oscillator or forcing it into abnormal modes is difficult. Typical circuits, such as this one, offer pull ranges of several hundred ppm. Larger shifts (e.g., 2000ppm to 3000ppm) are possible without losing crystal lock, although clock output frequency stability suffers somewhat.

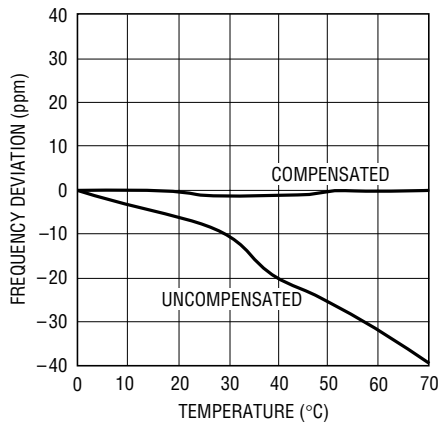


Figure 7. TXCO Drift Performance

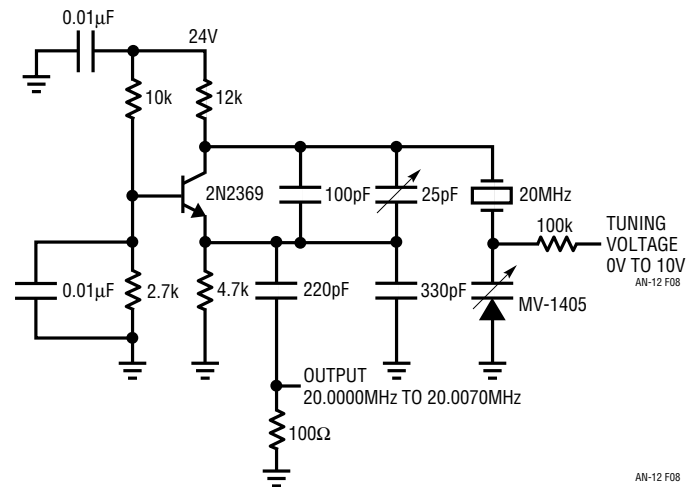


Figure 8. Voltage Controlled Crystal Oscillator (VXCO)

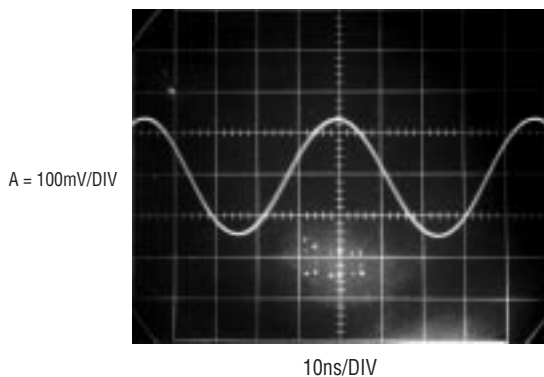


Figure 9. Figure 8's Output

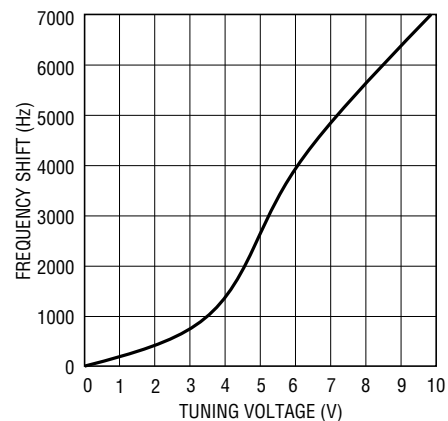


Figure 10. Figure 8's Tuning Characteristics

Application Note 12

Noncrystal Clock Circuits

Although crystal based circuits are universally applied, they cannot serve all clock requirements. As an example, many systems require a reliable 60Hz line synchronous clock. Zero crossing detectors or simple voltage level detectors are often employed, but have poor noise rejection characteristics. The key to achieving a good line clock under adverse conditions is to design a circuit which takes advantage of the narrow bandwidth of the 60Hz fundamental. Approaches utilizing wide gain bandwidth, even if hysteresis is applied, invite trouble with noise. Figure 11 shows a line synchronous clock which will not lose lock under noisy line conditions. The basic RC multivibrator is tuned to free run near 60Hz, but the AC-line derived synchronizing input forces the oscillator to lock to the line. The circuit derives its noise rejection from the integrator characteristics of the RC network. As Figure 12 shows, noise and fast spiking on the 60Hz input (Trace A, Figure 12) has little effect on the capacitor's charging characteristics (Trace B, Figure 12) and the circuit's output (Trace C, Figure 12) is stable.

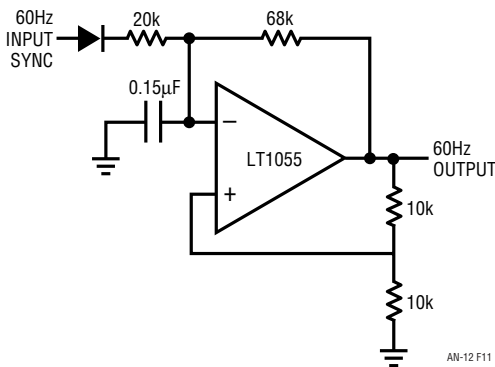


Figure 11. Synchronized Oscillator

Figure 13 is another synchronous clock circuit. In this instance, the circuit output locks at a higher frequency than the synchronizing input. Circuit operation is the time domain equivalent of a reset stabilized DC amplifier. The LT1055 and its associated components form a stable oscillator. The LM329 diode bridge and compensating diodes provide a stable bipolar charging source for the RC located at the amplifier's negative input. The synchronizing pulse (Trace A, Figure 14) is level shifted by the LT1011 comparator to drive the FET. When the synchronizing pulse appears, the FET turns on, grounding the capacitor (Trace B, Figure 14). This interrupts normal oscillator action, but only for a small fraction of a cycle. When the sync pulse falls, the capacitor's charge cycle, which has been reset to 0V, starts again. This resetting action forces the frequency of the RC charging to be synchronous and stabilized by the sync pulse. The only evidence of this operation at the output is an occasional, slightly enlarged pulse width (Trace C, Figure 14), which is caused by the synchronizing interval. The sync adjust potentiometer

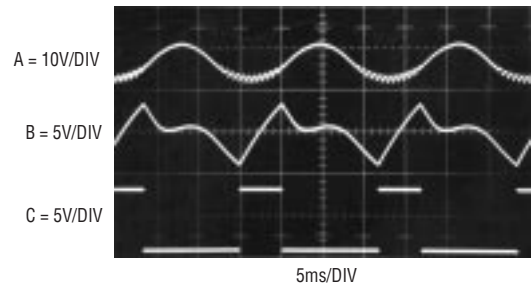


Figure 12. Figure 11's Waveforms

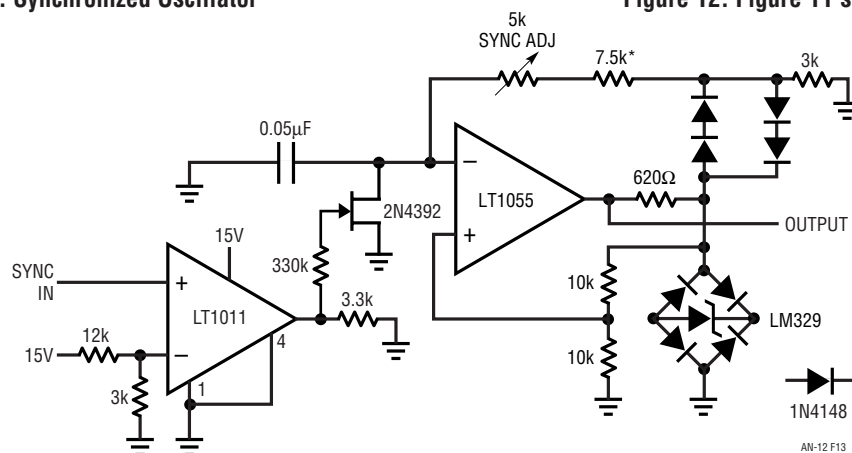


Figure 13. Reset Stabilized Oscillator

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should be trimmed so the sync pulse appears when the capacitor is near 0V. This minimizes output waveform width deviation and allows maximum protection against losing lock due to RC drift over time and temperature. The maximum practical output frequency to sync frequency ratio is about 50x.

Pure RC oscillators are a final form of clock circuit. Although this class of circuit cannot achieve the stability of a synchronized or crystal based approach, it offers simplicity, economy and direct low frequency output. As such they are used in baud rate generators and other low frequency applications. The key to designing a stable RC oscillator is to make output frequency insensitive to drift in as many circuit elements as possible. Figure 15 shows an RC clock circuit which depends primarily on the RC elements for stability. All other components contribute very low order error terms, even for substantial shifts. In addition, the RC components have been chosen for opposing temperature coefficients, further aiding stability. The circuit is a standard comparator-multivibrator with parallel CMOS inverters interposed between the comparator output and the feedback resistors. This replaces the relatively large and unstable bipolar V_{CE} saturation losses of the LT1011 output with the superior ON characteristics

of MOS. Not only are the MOS switching losses to the rails low and resistive, but they tend to cancel. The paralleling of inverters further reduces errors to insignificant levels. With this arrangement, the charge and discharge time constant of the capacitor is almost totally immune from supply and temperature shifts. The 10k units need not be precision types, because shifts in them will cancel. In addition, the effect of the comparator's DC input errors is also negated because of the symmetrical nature of the oscillator. This leaves only the RC network as a significant error term. The nominal—120ppm/°C temperature coefficient of the polystyrene capacitor is partially offset by the opposing positive temperature coefficient designed into the specified resistor. In practice, only a first order compensation is achievable because of the uncertainty of the capacitor's exact TC. For the test circuit, 0°C to 70°C temperature excursion showed a 15ppm/°C TC with a power supply rejection factor of less than 20ppm/V. In contrast, a clock constructed from the popular 555 timer, using the compensating RC network, showed 95ppm/°C and 1050ppm/V of supply shift. Because of comparator propagation delays, circuits of this type are less stable above a 5kHz to 10kHz operating frequency.

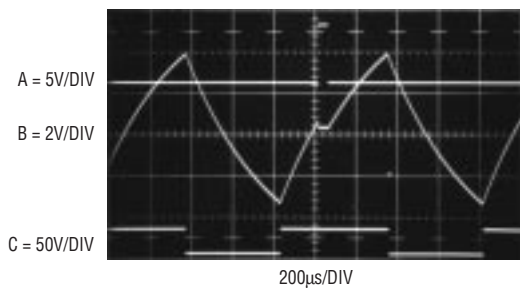


Figure 14. Figure13's Waveforms

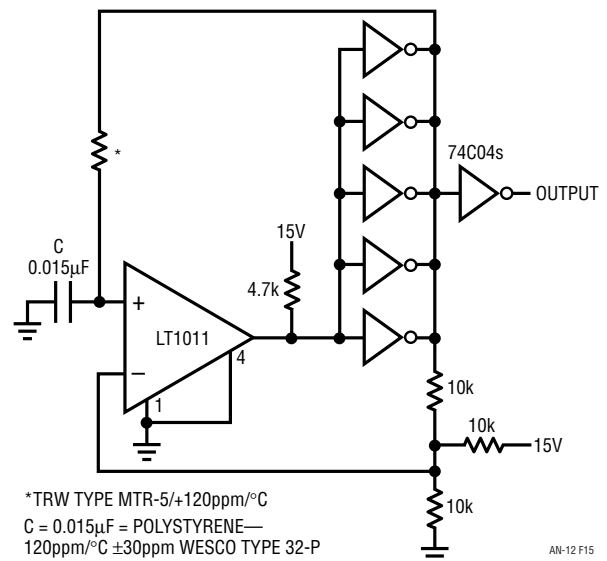
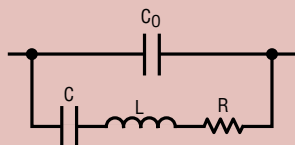


Figure 15. Stable RC Oscillator

Application Note 12

ABOUT QUARTZ CRYSTALS

The frequency stability and repeatability of quartz crystals represent one of nature's best bargains for the circuit designer. The equivalent circuit of a crystal looks like a series-parallel combination of elements.



Typical Values:

$$R = 100\Omega$$

$$L = 500\mu\text{H}$$

$$C = 0.01\text{pF}$$

$$C_0 = 5\text{pF}$$

$$Q = 50,000$$

C_0 is the static capacitance produced by the contact wires, crystal electrodes and the crystal holder. The RLC term is called the motional arm. C is the mechanical mass. R includes all electrical losses in the crystal and L is the reactive component of the quartz. Different angles of cut from the mother crystal produce different electrical characteristics in individual crystals. Cuts can be optimized for temperature coefficient, frequency range and other parameters. The basic "AT" cut used in most crystals in the 1MHz to 150MHz range is a good compromise between temperature coefficient, frequency range, ease of manufacture and other considerations. Other

factors affecting resonator performance include the method of lead attachment, package sealing method and internal environment (e.g., vacuum, partial pressure, etc.). Some circuit considerations when using crystals include:

Load Capacitance—The reactance the crystal must present to the circuit. Some circuits use the crystal in the parallel resonant mode (e.g., the crystal looks inductive). Other circuits are specified as series resonant and the crystal appears resistive. In this mode, the circuit's load capacitance, including all parasitics, must be specified. A typical number is around 30pF.

Resistance—The impedance the crystal presents when it is resonating.

Drive Level—How much power may be dissipated in the crystal and still maintain all specifications. 10mW is typical. Excessive levels can fracture the crystal.

Temperature Coefficient/Turning Point—The tempco of the crystal is usually specified near the "turning point." This is the temperature at which the crystal tempco is zero. Typically the tempco will be below 1ppm/°C over the operating range and the turning point around 75°C, although different cuts can considerably alter these numbers.

Frequency Tolerance—The deviation from ideal frequency when used under specified circuit conditions at a defined temperature. Tolerances vary from 50ppm to less than 1ppm.

High Speed Comparator Techniques

Jim Williams

INTRODUCTION

Comparators may be the most underrated and underutilized monolithic linear component. This is unfortunate because comparators are one of the most flexible and universally applicable components available. In large measure the lack of recognition is due to the IC op amp, whose versatility allows it to dominate the analog design world. Comparators are frequently perceived as devices which crudely express analog signals in digital form—a 1-bit A-D converter. Strictly speaking, this viewpoint is correct. It is also wastefully constrictive in its outlook. Comparators don't "just compare" in the same way that op amps don't "just amplify".

Comparators, in particular high speed comparators, can be used to implement linear circuit functions which are as sophisticated as any op amp-based circuit. Judiciously combining a fast comparator with op amps is a key to achieving high performance results. In general, op amp-based circuits capitalize on their ability to close a feedback loop with precision. Ideally, such loops are maintained continuously over time. Conversely, comparator circuits are often based on speed and have a discontinuous output over time. While each approach has its merits, a fusion of both yields the best circuits.

This effort's initial sections are devoted to familiarizing the reader with the realities and difficulties of high speed comparator circuit work. The mechanics and subtleties of

achieving precision circuit operation at DC and low frequency have been well documented. Relatively little has appeared which discusses, in practical terms, how to get fast circuitry to work. In developing such circuits, even the most veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high speed circuits can only work if negotiated compromises with nature are arranged. Ignorance of, or contempt for, physical law is a direct route to frustration. In this regard, much of the text and appendices are directed at developing awareness of and respect for circuit parasitics and fundamental limitations. This approach is maintained in the applications section, where the notion of "negotiated compromises" is expressed in terms of resistor values and compensation techniques. Many of the application circuits use the LT1016's speed to improve on a standard circuit. Some utilize the speed to implement a traditional function in a non-traditional way, with attendant advantages. A (very) few operate at or near the state-of-the-art for a given circuit type, regardless of approach. Substantial effort has been expended in developing these examples and documenting their operation. The resultant level of detail is justified in the hope that it will be catalytic. The circuits should stimulate new ideas to suit particular needs, while demonstrating the LT1016's capabilities in an instructive manner.

TABLE OF CONTENTS

Introduction	AN13-1
The LT1016 — An Overview	AN13-3
The Rogue's Gallery of High Speed Comparator Problems	
Bypassing	AN13-4
Probe Compensation	AN13-4
Probe Bandwidth	AN13-4
Probe Grounding	AN13-5
FET Probe Considerations	AN13-5
Comparator Grounding	AN13-6
Ground Planes	AN13-6
Source Impedance Considerations	AN13-6
Stray Capacitance at Inputs	AN13-7
Output Loading	AN13-7
Output Termination	AN13-7
Input Common-Mode Level	AN13-7
Oscilloscopes	AN13-8
Applications	
1Hz–10MHz V → F Converter	AN13-8
Quartz-Stabilized 1Hz–30MHz V → F Converter	AN13-10
1Hz–1MHz Voltage-Controlled Sine Wave Oscillator	AN13-12
200ns–0.01% Sample-and-Hold Circuit	AN13-14
Fast Track-and-Hold Circuit	AN13-16
10ns Sample-and-Hold	AN13-17
2.5 μ s, 12-Bit A–D Converter	AN13-18
Inexpensive, Fast 10-Bit Serial Output A–D	AN13-20
2.5MHz Precision Rectifier / AC Voltmeter	AN13-21
10MHz Fiber Optic Receiver	AN13-22
12ns Circuit Breaker	AN13-23
50MHz Trigger	AN13-24
References	AN13-25
Appendices	
A — About Bypass Capacitors	AN13-25
B — About Probes and Oscilloscopes	AN13-27
C — About Ground Planes	AN13-29
D — Measuring Equipment Response	AN13-30
E — About Level Shifts	AN13-31

THE LT1016 — AN OVERVIEW

A new ultra high speed comparator, the LT1016, features TTL-compatible complementary outputs and 10ns response time. Other capabilities include a latch pin and good DC input characteristics (see Figure 1). The LT1016's outputs directly drive all TTL families, including the new higher speed ASTTL and FAST parts. Additionally, TTL outputs make the device easier to use in linear circuit applications where ECL output levels are often inconvenient.

A substantial amount of design effort has made the LT1016 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1016 is stable in its linear region, a feature no other high speed comparator has. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. These features make the application of the 200GHz gain-bandwidth LT1016 considerably easier than other fast comparators. Unfortunately, laws of physics dictate that the circuit environment the LT1016 works in must be properly prepared. The performance limits of high speed circuitry

are often determined by parasitics such as stray capacitance, ground impedance, and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1016 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1016's (Trace B) response to the pulse generator (Trace A) is faster than a TTL inverter (Trace C)! In fact, the inverter's output never gets to a TTL "0" level. Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used

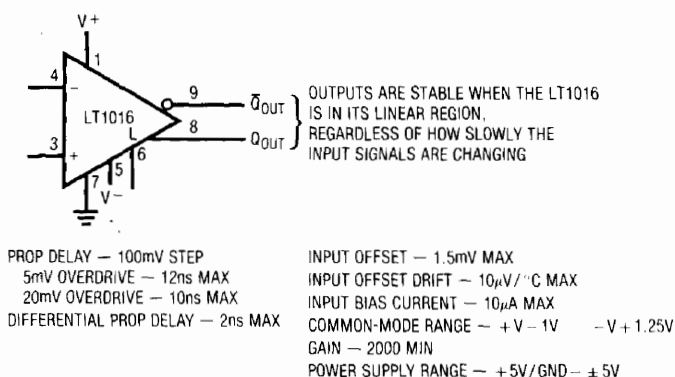


Figure 1. The LT1016 at a Glance

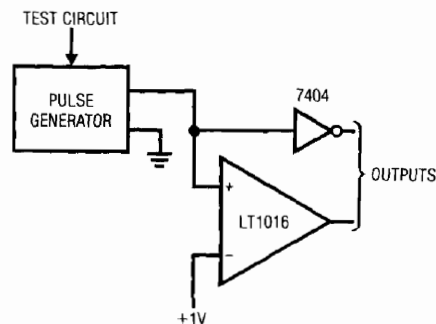
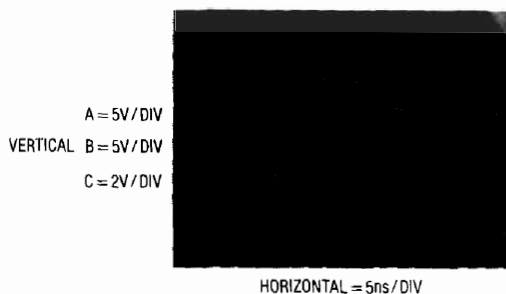


Figure 2. LT1016 vs a TTL Gate

Application Note 13

in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

The Rogue's Gallery of High Speed Comparator Problems

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully (see Appendix A, "About Bypass Capacitors"). An unbypassed LT1016 is shown responding to a pulse input in Figure 3. The power supply the LT1016 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1016, allowing the supply to move as internal conditions in the comparator change. This causes local

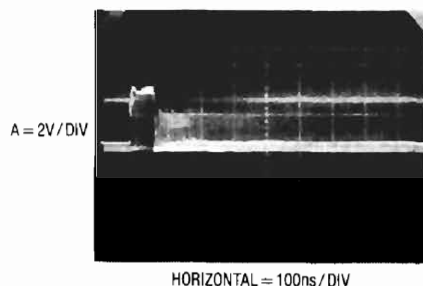


Figure 3. Unbypassed LT1016 Response

feedback and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

In Figure 4 the LT1016's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount them as close as possible to the LT1016. An inch of wire between the capacitor and the LT1016 can cause problems.*

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V — quite a trick for a device running from a +5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly* (for a discussion on probes, see Appendix B, "About Probes and Scopes"). Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 10ns response time LT1016 appears to have 50ns edges! In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

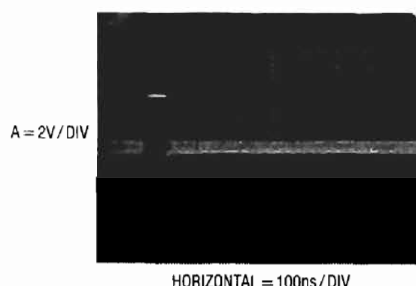


Figure 4. LT1016 Response with Poor Bypassing

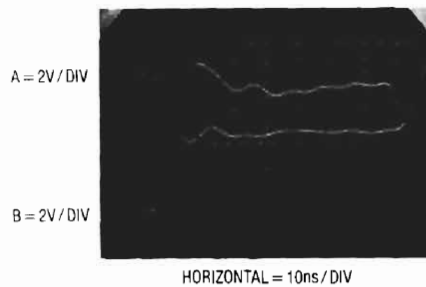


Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

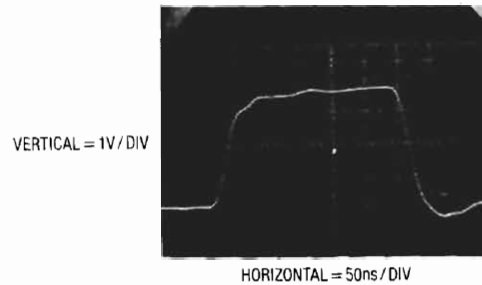


Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

In Figure 7 the probes are properly selected and applied but the LT1016's output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. *Keep the probe ground connection as short as possible.*

The difficulty in Figure 8 is delay and inadequate amplitude (Trace B). A small delay on the leading edge is followed by a large delay before the falling edge begins.

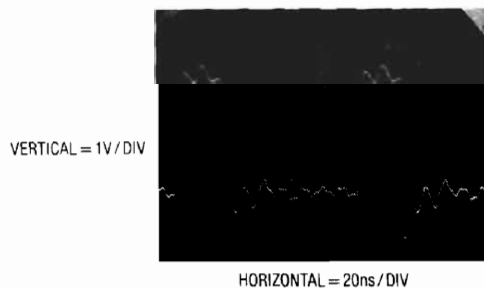


Figure 7. Typical Results Due to Poor Probe Grounding

Additionally, a lengthy, tailing response stretches 70ns before finally settling out. The amplitude only rises to 1.5V. A common oversight is responsible for these conditions.

A FET probe monitors the LT1016 output in this example. The probe's common-mode input range has been exceeded, causing it to overload and clip the output badly. The small delay on the rising edge is characteristic of active probes and is legitimate. During the time the output is high, the probe is driven deeply into saturation. When the output falls, the probe's overload recovery is lengthy and uneven, causing the delay and tailing.

Know your FET probe. Account for the delay of its active circuitry. Avoid saturation effects due to common-mode input limitations (typically $\pm 1V$). Use 10X and 100X attenuator heads when required.

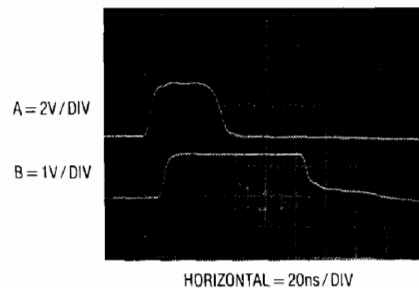


Figure 8. Overdriven FET Probe Causes Delayed, Tailing Response

Application Note 13

Figure 9 shows the LT1016's output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1016's ground pin connection is 1 inch long. The ground lead of the LT1016 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1016's ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1016's ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

Figure 10 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1016 without a "ground plane." A ground plane is formed by using

a continuous conductive plane over the surface of the circuit board (the theory behind ground planes is discussed in Appendix C). The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1016.*

"Fuzz" on the edges is the difficulty in Figure 11. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3k Ω input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedances as low as possible, preferably 1k Ω or less. Route output and input pins and components away from each other.*

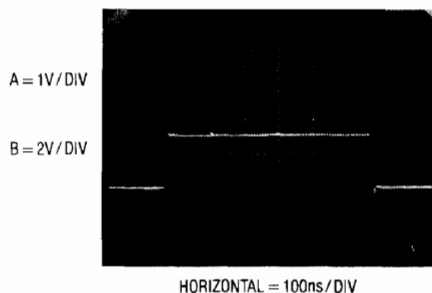


Figure 9. Excessive LT1016 Ground Path Resistance Causes Oscillation

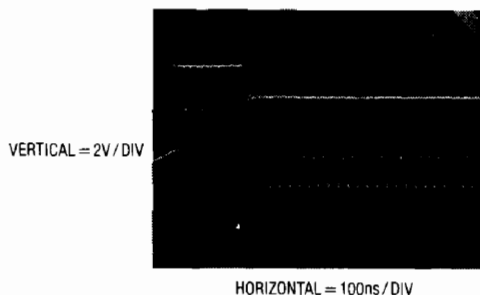


Figure 10. Transition Instabilities Due to No Ground Plane

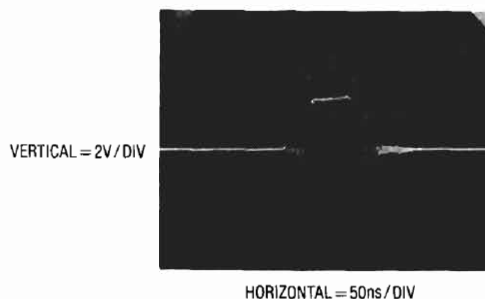


Figure 11. 3pF Stray Capacitive Feedback with 3k Ω Source Can Cause Oscillation

The opposite of stray-caused oscillations appears in Figure 12. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input and output delay occurs. An RC combination of $2k\Omega$ source resistance and $10pF$ to ground gives a $20ns$ time constant — significantly longer than the LT1016's response time. *Keep source impedances low and minimize stray input capacitance to ground.*

Figure 13 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few circumstances it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.*

Another output-caused fault is shown in Figure 14. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead which is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω – 400Ω).*

A final malady is presented in Figure 15. These waveforms are reminiscent of the input RC-induced delay of Figure 12. The output waveform initially responds to the input's leading edge, but then returns to zero before going high again. When it does go high, it slews slowly. Additional odd characteristics include pronounced overshoot and pulse top aberration. The fall time is also slow and well delayed from the input. This is certainly strange

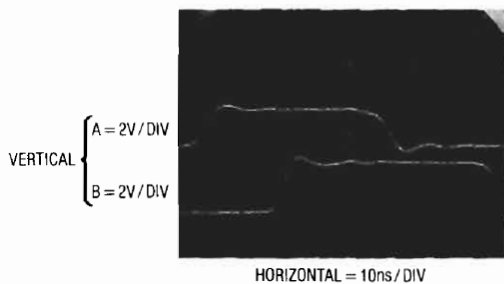


Figure 12. Stray 5pF Capacitance from Input to Ground Causes Delay

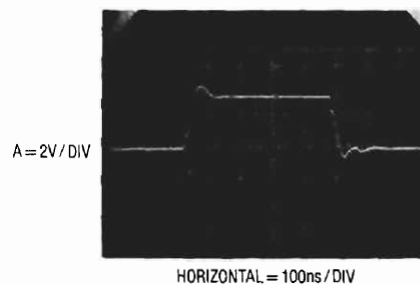


Figure 13. Excessive Load Capacitance Forces Edge Distortion

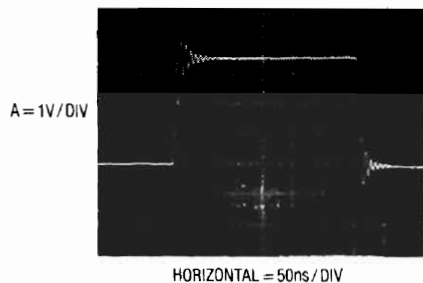


Figure 14. Lengthy, Unterminated Output Lines Ring from Reflections

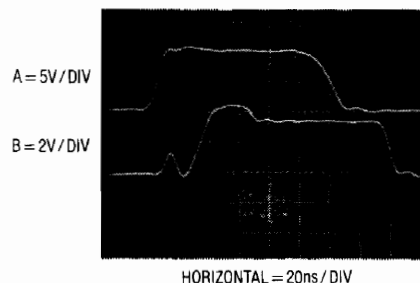


Figure 15. Input Common-Mode Overdrive Generates Odd Outputs

Application Note 13

behavior from a TTL output. What is going on here? The input pulse is responsible for all these anomalies. Its 10V amplitude is well outside the +5V powered LT1016's common-mode input range. Internal input clamps prevent this pulse from damaging the LT1016, but an overdrive of this magnitude results in poor response. *Keep input signals inside the LT1016's common-mode range at all times.*

Oscilloscopes

A few of the examples illustrated dealt with probe-caused problems. Although it should be obvious, it is worth mentioning that the choice of oscilloscope employed is crucial. Be certain of the characteristic of the probe-oscilloscope combination you are using. Rise time, bandwidth, resistive and capacitive loading, delay, overdrive recovery and other limitations must be kept in mind. High speed linear circuitry demands a great deal from test equipment and countless hours can be saved if the characteristics of the instruments used are well known (see Appendix C, "Measuring Equipment Response"). In fact, it is possible to use seemingly inadequate equipment to get good results if the equipment's limitations are well known and respected. All of the applications which follow involve rise times and delays well above the

100MHz–200MHz region, but 90% of the development work was done with a 50MHz oscilloscope. Familiarity with equipment and thoughtful measurement technique permit useful measurements seemingly beyond instrument specifications. A 50MHz oscilloscope cannot track a 5ns rise time pulse, but it can measure a 2ns delay between two such events. Using such techniques, it is often possible to deduce the desired information. There are situations where no amount of cleverness will work and the right equipment, e.g., a faster oscilloscope, must be used.

In general, use equipment you trust and measurement techniques you understand. Keep asking questions and don't be satisfied until everything you see on the oscilloscope is accounted for and makes sense.

The LT1016, combined with the precautionary notes listed above, permits fast linear circuit functions which are difficult or impossible using other approaches. Many of the applications presented represent the state-of-the-art for a particular circuit function. Some show new and improved ways to implement standard functions by utilizing the LT1016's speed. All have been carefully (and painfully) worked out and should serve as good idea sources for potential users of the device.

APPLICATIONS SECTION

1Hz–10MHz V → F Converter

The LT1016 and the LT1012 low drift amplifier combine to form a high speed V → F converter in Figure 16. A variety of circuit techniques is used to achieve a 1Hz to 10MHz output. Overrange to 12 MHz ($V_{IN} = 12V$) is provided. This circuit has a wider dynamic range (140dB, or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V → Fs. The theory of operation is based on the identity $Q = CV$.

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor.

The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

For low bias, high speed operation, a pair of discrete FETs directly drives A1's output stages, replacing A1's monolithic input circuitry. A1's input stage is turned off by connecting the input pins to the negative 15V rail. The FET gates become the "+" and "-" inputs of the amplifier. $0.2\mu V/^\circ C$ offset drift performance is obtained by stabilizing the A1-FET combination with A2, a precision op amp. A2 measures the DC value of the negative

input, compares it to ground, and forces the positive input to maintain offset balance in the A1-FET combination. Note that A2 is configured as an integrator and cannot see high frequency signals. It functions only at DC and low frequency. The A1-FET combination is arranged as an integrator with a 100pF feedback capacitor. When a positive voltage is applied to the input, A1's output integrates in a negative direction (Trace A, Figure 17). Dur-

ing this period, C1's inverting output is low. A very high speed level shifter, Q1-Q2 (see Appendix D, "About Level Shifters"), inverts this output and drives the zener reference bridge. The bridge's positive output is used to charge the 33pF capacitor. The 1.2V diode string provides cancellation and temperature compensation for the diode drops in the bridge so that the 33pF unit charges to $V_Z + V_{BE} Q3$.

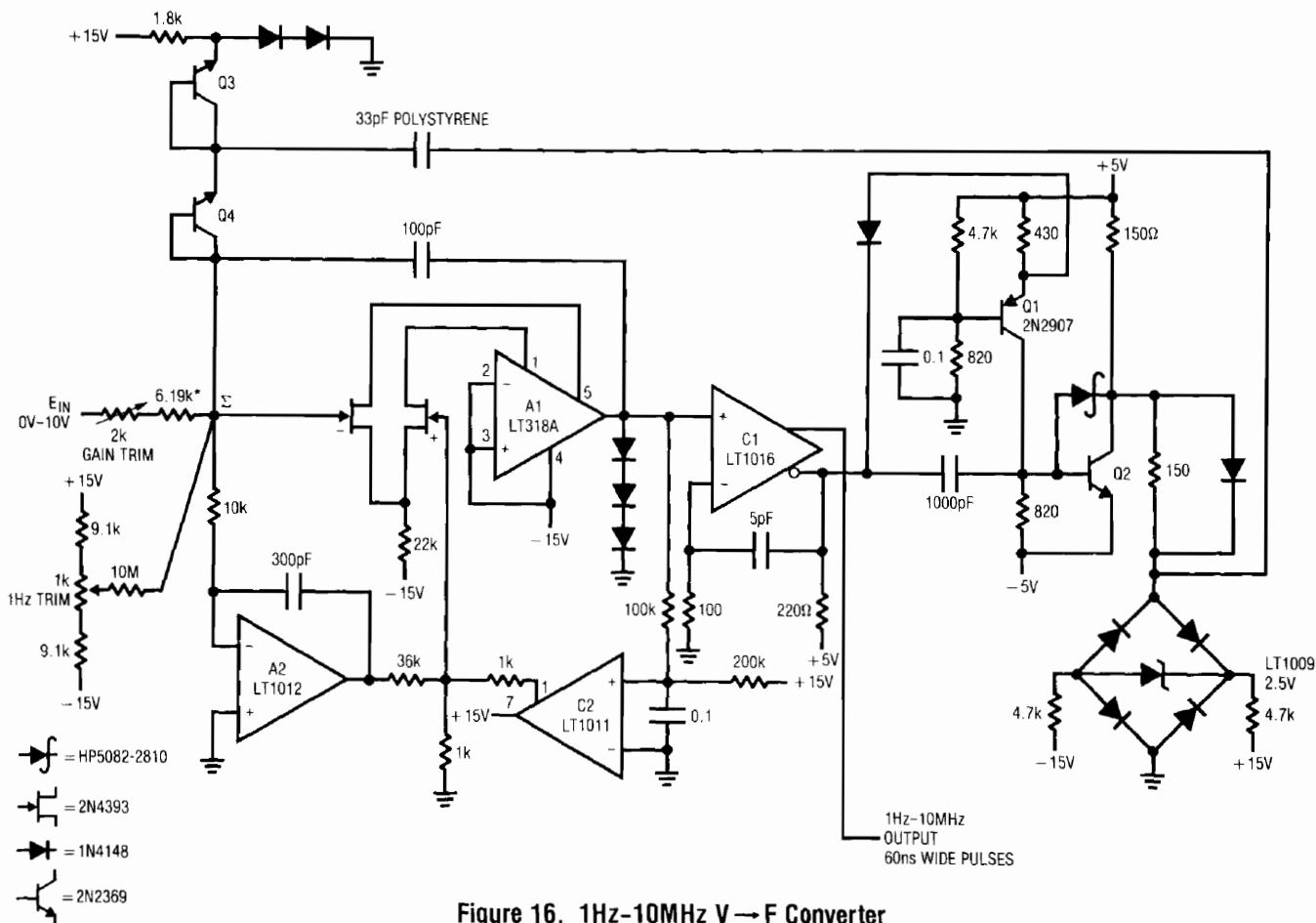


Figure 16. 1Hz-10MHz V → F Converter

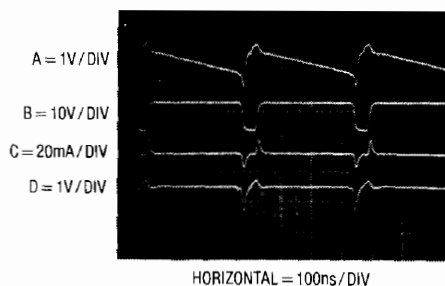


Figure 17. 10MHz V → Fs Operating Waveforms

Application Note 13

When A1's output crosses zero, C1's inverting output goes high and Q2's (Trace B) collector goes to $-5V$. This causes the 33pF unit to dispense charge into the summing node via Q4's V_{BE} . The amount of charge dispensed is a direct function of the voltage that the 33pF unit was charged to ($Q = CV$). Q4's V_{BE} compensates the Q3 V_{BE} term in the capacitor's charge equation. The current which flows through the 33pF unit (Trace C) reflects this charge pumping action. The removal of current from A1's summing junction (Trace D) causes the junction to be driven very quickly negative. The initial negative-going 20ns transient at A1's output is due to amplifier delay. The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (Trace A) slews limits as it attempts to regain control of the summing node. The amount of time Q2's collector (Trace B) remains at $-5V$ depends on how long it takes A1 to recover and the 5pF-100 Ω hysteresis network at C1. This 60ns interval is long enough for the 33pF unit to fully discharge. After this, C1 changes state and Q2's collector swings positive. The capacitor is recharged and the entire cycle repeats. The frequency at which this oscillation occurs is directly related to the voltage-input-derived current into the summing junction. Any input current will require a corresponding oscillation frequency to hold the summing point at an average value of 0V.

Maintaining this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to achieving 10MHz full-scale operating frequency is the ability to transmit information around the loop as quickly as possible. The discharge-reset sequence is particularly critical and is detailed in Figure 18. Trace A is the A1 integrator output. Its ramp output crosses 0V at the first left vertical graticule division. A few nanoseconds later, C1's inverting output begins to rise (Trace B), driving the Q1-Q2 level shifter output negative (Trace C). Q2's collector begins to head negative about 12ns after A1's output crosses 0V. 4ns later, the summing point (Trace D) begins to go negative as current is pulled from it through the 33pF capacitor. At 25ns, C1's inverting output is fully up, Q2's collector is at $-5V$, and the summing point has been pulled to its negative extreme. Now, A1 begins to take control. Its output (Trace A) slews rapidly in the

positive direction, restoring the summing point. At 60ns, A1 is in control of the summing node and the integration ramp begins again.

Start-up and overdrive conditions could force A1's output to go to the negative rail and stay there. The AC-coupled nature of the charge dispensing loop can preclude normal operation and the circuit may latch. C2 provides a "watchdog" function for this condition. If A1's output tries to go too far below zero, C2 switches, forcing the "+" input FET gate positive. This causes A1's output to slew positive, initiating normal circuit action. The diode chain at C1's input prevents common-mode overdrive at the LT1016. To trim this circuit, ground the input and adjust the 1k pot for 1Hz output. Next, apply 10.000V and set the 2k Ω unit for 10.000MHz output. The transfer linearity of the circuit is 0.06%. Full-scale drift is typically 50ppm/ $^{\circ}C$ and zero point error about 0.2 $\mu V/^{\circ}C$ (0.2Hz/ $^{\circ}C$).

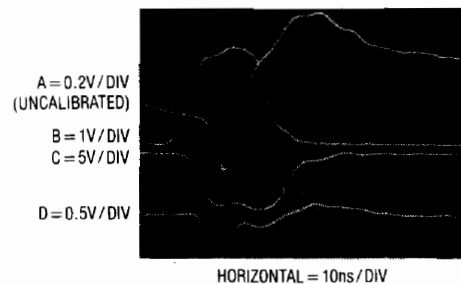


Figure 18. Detail of 60ns Reset Sequence (Whoosh!)

Quartz-Stabilized 1Hz-30MHz V \rightarrow F Converter

Figure 16's upper limit on operating frequency is imposed by delays in the active elements in the LT1016's feedback path. Higher speed is possible by minimizing these delays. Figure 19 shows a way to do this while retaining good drift and linearity characteristics. The circuit's untrimmed 150dB dynamic range is 1000 times greater than commercially available V \rightarrow F converters, whether monolithic, hybrid, or modular.

The technique employed allows the LT1016 to roar along at a 30MHz full-scale output frequency, substantially faster than any commercially available V \rightarrow F. The actual V \rightarrow F conversion is performed by the circuit shown inside the dashed lines. This circuit functions similarly to Figure 16.

The level shift and zener bridge are eliminated. Q1 charges the 200pF capacitor, which is unloaded by the Q2-Q3 buffer. When the LT1016's negative input rises above its positive input, its output goes low, pulling charge out of the capacitor via Q4, which serves as a low leakage diode. The 2.7pF capacitor provides positive feedback. If the left end of the 100k input resistor is driven from a voltage source, the LT1016 oscillates over a 1Hz to 30MHz range. Although this simple circuit is fast, its linearity is poor and drift exceeds 5000ppm/°C.

The remaining components in Figure 19 form a quartz-locked sampled-data loop to correct these terms without sacrificing speed. The loop works by counting the number of pulses at the LT1016's output during a fixed interval and converting this information to a voltage. The voltage is compared to the circuit's input by an amplifier which drives the LT1016 V → F circuit. This closed loop technique relies on the stability of the time interval and the digital-to-voltage conversion to achieve circuit stability. Frequent updating of the loop ensures long term stability. Figure 20 shows how the circuit functions.

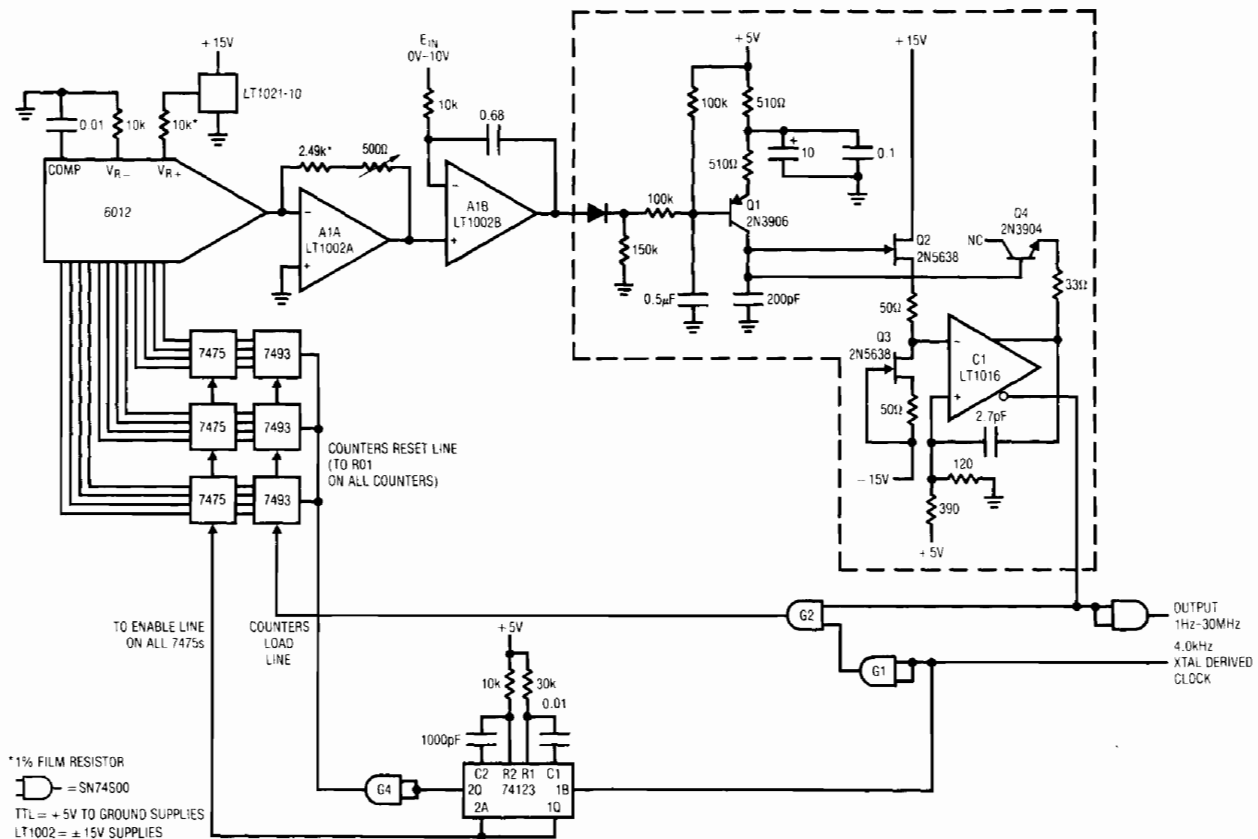


Figure 19. 30MHz V → F Utilizes Sampled Loop for High Stability and Linearity

Application Note 13

Waveforms A, B and C are the LT1016's negative input, output and positive input, respectively. Their similarity to Figure 17 (Traces A, B and C) reflects the two circuits' commonality of operation. Trace D shows the quartz-crystal-derived 4kHz clock. During the clock's low portion, the LT1016's gated output appears at G2's output (Trace E). This data is loaded into counters which drive a 12-bit DAC via the 7475 latches. When the clock goes high, one section of the 74123 one-shot generates a pulse (Trace F), allowing the latches to acquire the counter's data. After this pulse goes low, the one-shot's second half pulses (Trace G) the counter's reset line. At the clock's next falling edge the entire cycle repeats. The DAC and its associated output amplifier (A1A) provide a voltage representation of the digital word at the 7475 outputs. This voltage is compared to the circuit's input by A1B, whose output drives the LT1016-based V→F. Any drift or nonlinearity in the V→F will be corrected by the feedback action of this stabilizing loop. The 10k-0.68μF time constant at A1B provides loop compensation.

Although it is not obvious, the frequency setting resolution is much greater than the 12-bit quantization limit of the DAC. This is because the DAC's output dithering around the LSB is integrated to a pure DC level by loop time constants. Once the DAC has settled within an LSB, its output acts like a 4kHz clocked pulse width modulator. The slow loop time constants integrate the width-modulated information to DC, affording smooth, continuous frequency setting capability. The practical limit on resolution is due to the LT1016 oscillator's short term jitter and is about 25ppm of reading.

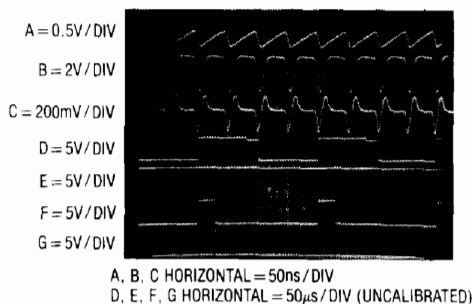


Figure 20. Waveforms for Figure 19. Sampled Data Loop (Traces D-G) Stabilizes Basic V→F (Traces A-C)

Although this approach allows higher speeds than Figure 16, there are some trade-offs. The loop's sampled nature, combined with its long time constants, limit settling time to about 100ms. Thus, although its output is faster than Figure 16's, it cannot track quickly varying inputs. Circuit linearity is DAC limited to 0.025% with full-scale drift of 50ppm/°C. Zero point drift of 1Hz/°C is due to A1B's 0.3μV/°C offset drift.

1Hz–1MHz Voltage-Controlled Sine Wave Oscillator

Both V→F converters described have pulse outputs. Many applications such as audio, shaker table driving, and automatic test equipment require voltage-controlled oscillators (VCO) with a sine wave output. The circuit of Figure 21 meets this need, spanning a 1Hz–1MHz range (120dB, or 6 decades) for a 0V to 10V input. It is over 10 times faster than previously published circuits, while maintaining 0.25% frequency linearity and 0.40% distortion specifications.

To understand the circuit, assume Q5 is on and its collector (Trace A, Figure 22) is at –15V, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 3.6k resistor and the self-biased FETs. A current, –I, is pulled from the summing point. A2, a precision op amp, DC stabilizes A1. A1's output (Trace B, Figure 22) integrates positive until C1's input (Trace C) crosses 0V. When this happens, C1's inverting output goes negative, the Q4–Q5 level shifter turns off, and Q5's collector goes to +15V. This allows Q1 to come on. The resistors in Q1's path are scaled to produce a current, +2I, exactly twice the absolute magnitude of the current, –I, being removed from the summing node. As a result, the net current into the junction becomes +I and A1 integrates negatively at the same rate its positive excursion took.

When A1 integrates far enough in the negative direction, C1's "+" input crosses zero and its outputs reverse. This switches the Q4–Q5 level shifter's state, Q1 goes off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 1MHz with a 0V–10V input.

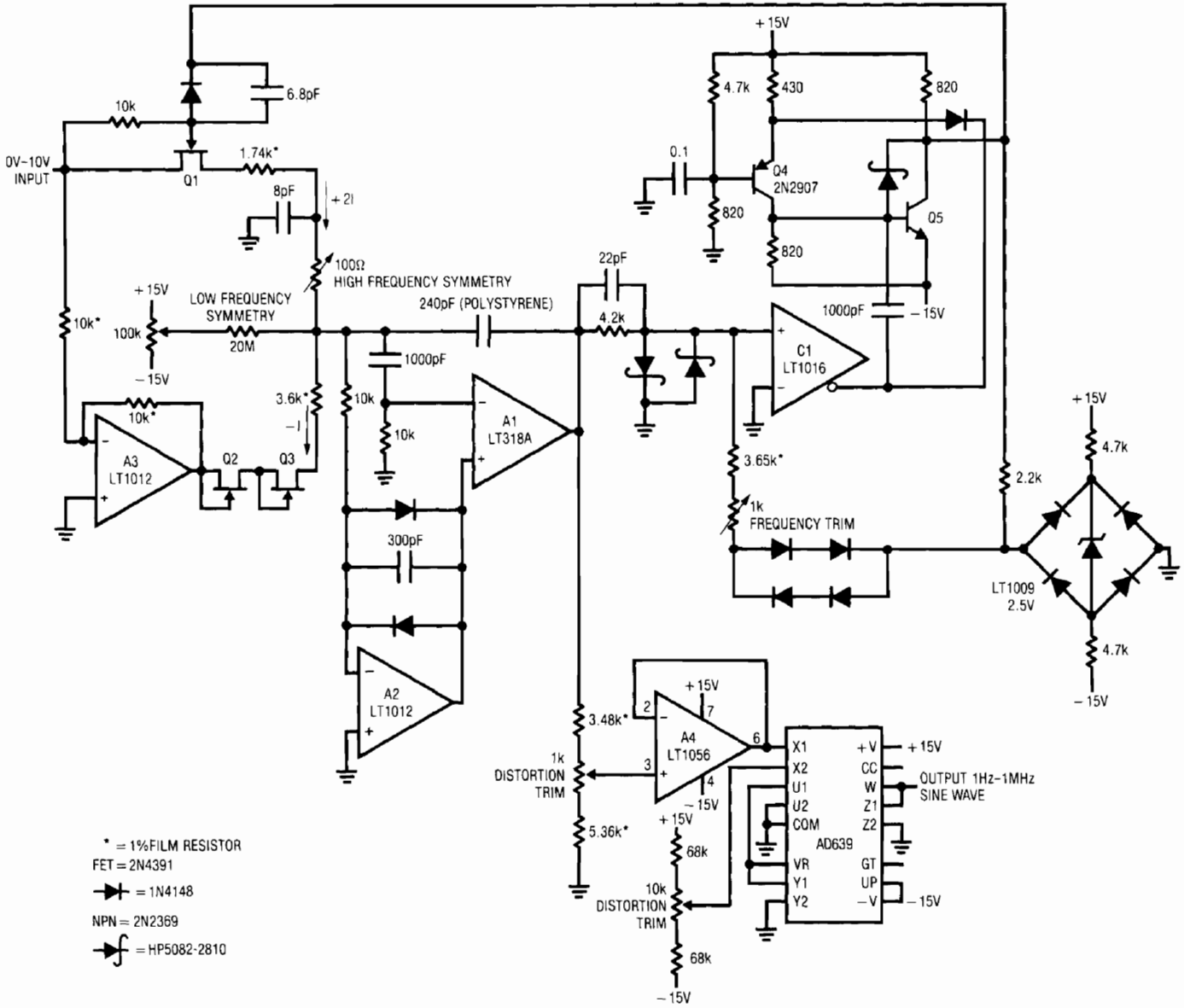


Figure 21. 1Hz-1MHz Sine Wave Output VCO

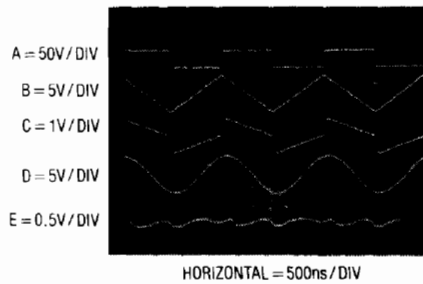


Figure 22. Sine Wave VCO Waveforms

Application Note 13

The LT1009 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's "+" input, assuring it clean recovery from overdrive.

The AD639 trigonometric function generator, biased via A4, converts A1's triangle output into a sine wave (Trace D).

The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At higher frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If these delays are not minimized, triangle amplitude will increase with frequency, causing distortion level to also increase with frequency. The total delay generated by the LT1016, the Q4-Q5 level shifter, and Q1 is 14ns. This small delay, combined with the 22pF feedforward network at the LT1016's input, keeps distortion to just 0.40% over the entire 1MHz range. At 100kHz, distortion is typically inside 0.2%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 8pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature-dependent on-resistance of Q1, keeping the $+2I/-I$ relationship constant with temperature.

To adjust this circuit, put in 10.00V and trim the 100 Ω pot for a symmetrical triangle output at A1. Next, put in 100 μ V and trim the 100k pot for triangle symmetry. Then, put in 10.00V again and trim the 1k "frequency trim" adjustment for a 1MHz output frequency. Finally, adjust the "distortion trim" potentiometers for minimum distortion as measured on a distortion analyzer (Trace E). Slight readjustment of the other potentiometers may be required to get lowest possible distortion.

200ns-0.01% Sample-and-Hold Circuit

Figure 23's circuit uses the LT1016's high speed to improve upon a standard circuit function. The 200ns acquisition time is well beyond monolithic sample-and-hold capabilities and is matched only by hybrid and modular units selling in the \$200 range. Other specifications exceed the best commercial unit's performance. This circuit also gets around many of the problems associated

with standard sample-and-hold approaches, including FET switch errors and amplifier settling time. To achieve this, the LT1016's high speed is used in a circuit which completely abandons traditional sample-and-hold methods. When the sample-and-hold command line (Trace A, Figure 24) is high, Q2 conducts current, biasing Q3 on and forcing the 1000pF capacitor (Trace B) to discharge toward Q4's emitter potential. Q4's emitter, in turn, sits at a potential slightly below Q3's collector voltage. Q5 and the LT1009, biased from the input voltage, drive Q4. Concurrently, the TTL gate at the LT1016 grounds the latch pin (enabling the comparator) and the comparator's inverting output (Trace C) goes high. When the sample-and-hold command line (Trace A) falls, Q2 and Q3 go off and the Q1 current source charges the 1000pF unit (Trace B) with a fast linear ramp. This capacitor is buffered by Q7, a current sink loaded source follower. When Q7's output reaches the circuit's input value, the LT1016's inverting output (Trace C) switches low. The Q1 current source cuts off in about 2ns and capacitor charging ceases. The LT1016's low state also means the NOR gate's output is high, latching the comparator's output. This prevents input line noise or a change in signal from affecting the stored value in the 1000pF hold capacitor.

Ideally, Q7's output now sits at exactly the sampled value of the input voltage. In practice, a slight error exists because of the LT1016's delay and the turn-off time of Q1 (total 12ns). Because of these delays, the capacitor is able to charge to a higher voltage than the input before current stops. This error term is compensated by removing a small quantity of charge from the 1000pF capacitor when the LT1016's inverting output goes low. The charge is removed through the 8pF-1k Ω potentiometer network. Because the charging ramp's slope is fixed, the error term is constant and the compensation works over the circuit's $\pm 3V$ input common-mode range. The lower four traces are expanded to show detail of the compensation and the circuit's critical ramp turn-off sequence. When the LT1016 goes off (Trace D), the ramp is seen to slightly overshoot its final value (Trace E).

The 1k Ω -8pF combination pulls enough charge (Trace F) out of the 1000pF hold capacitor to bring it back to the correct value. Trace G is the \overline{NOW} line. It falls low 2 gate delays after the LT1016 inverting output goes low. When

Application Note 13

Figure 25 the circuit is shown sampling a bipolar triangle wave. Trace A is the input and Trace B is the circuit output. Trace C is an expansion of Trace B (the "smearing" of the sampled pedestals in Trace C is due to the repetitive asynchronous sampling of the triangle). The action of the tracking amplifier is readily apparent. It always resets the ramp to the same point below the input voltage, regardless of the common-mode level. To calibrate the circuit, ground the input, repetitively pulse the sample-and-hold command line, and adjust the 1kΩ pot for 0V output.

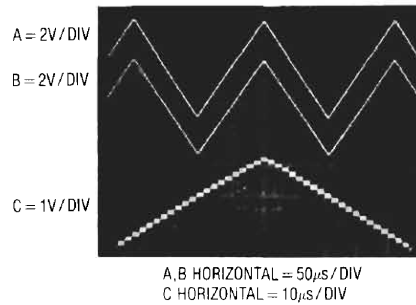


Figure 25. Fast Sample-and-Hold Tracking a Triangle Wave. Trace C is Expanded to Show the Ramping of the Circuit's Output.

Important specifications for this circuit include:

Acquisition Time	< 200ns
Common-Mode Input Range	± 3V
Droop	1µV/µs
Hold Step	2mV
Hold Settling Time	15ns
Feedthrough Rejection	>> 100dB

Fast Track-and-Hold Circuit

The track-and-hold circuit shown in Figure 26 is generically related to the sample-and-hold circuit of Figure 23.

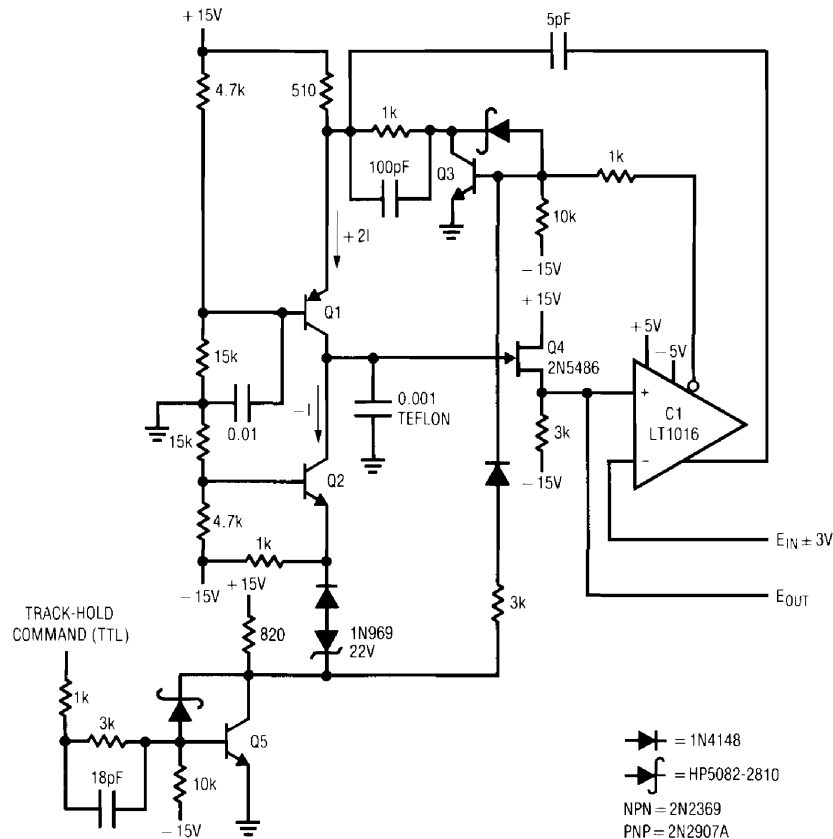


Figure 26. Comparator-Based Track-and-Hold

It also forsakes standard techniques in favor of an approach based on the LT1016's speed. This circuit's main blocks are a switched current source (Q1-Q3), a current sink (Q2), a FET follower (Q4), and the LT1016. To understand the circuit, assume the voltage stored in the 0.001 μ F hold capacitor is below the input potential and the track-and-hold command line (Trace A, Figure 27) is at a TTL "1" (track mode). Under these conditions Q5 is on and C1's output is positive. C1's inverting output is low and Q3 is off, allowing the Q1 current source to charge the hold capacitor. The Q2 current sink is also operating, but at 1/2 the current density of Q1. The hold capacitor charges positively. When Q4's source (Trace B, Figure 27) ramps to the input voltage's value, C1's outputs reverse state. Q3 comes on, quickly turning off the Q1 current source. The 5pF feedforward capacitor speeds up Q1's turnoff by bypassing Q3. With Q1 off, Q2's sink current discharges the hold capacitor. This causes C1's output to change state and oscillation commences (Trace B, Figure 27). This controlled, 10mV-25MHz oscillation centers itself around the input voltage's value. When the track-and-hold line (Trace A) goes low, Q5 ceases conducting, Q1 and Q2 immediately go off, oscillations cease and the circuit's output sits within ± 5 mV of the input value at the time of turn-off. This 5mV uncertainty, caused by the nature of the circuit's operation, limits accuracy to 8 bits.

Figure 28 shows what happens when a square wave is fed into the circuit. Trace A is the input. Trace B is the output. Trace C is the track-and-hold command line and Trace D is the LT1016's output. Note that the controlled oscillation stops cleanly when the track-and-hold line goes low. If the source-sink transistors were run at

higher currents, the circuit's output would slew much faster to keep up with the input's transitions. The oscillation's error band would also proportionately enlarge. The 25MHz update rate allows this circuit to track a relatively slow signal very closely with settling time under 10ns when switched into hold.

10ns Sample-and-Hold

Figure 29 shows a 10ns acquisition time sample-and-hold which can be used with repetitive signals only. Here, the LT1016 (C1) drives a differential integrator's (A1) input. Feedback from the integrator back to the LT1016 closes a loop around the circuit. Figure 30 shows what happens when a 1MHz sine wave (Trace A, Figure 30) is applied to the input. C2 generates a zero crossing signal (Trace B) and one-shot "A" (Trace C) provides an adjustable width. One-shot B's Q output produces a 30ns pulse (Trace D) which is fed into a logic network with the \bar{Q} signal. The two inverter delays in Q's path give its associated gate a shorter duration output (Trace F) than \bar{Q} 's gate (Trace E). The last gate subtracts these two signals and generates a 10ns spike. This is inverted (Trace G) and fed to C1's latch pin. Each time the latch is enabled the comparator responds to the condition of the summing junction at its "+" input. If summing error is positive, A1 pulls current. If the error is negative, A1 sources current to the junction. After a number of input cycles, A1's output settles at a DC value which is the same as the level sampled during the time the latch is enabled. The "delay adjust" allows the 10ns sampling "window" to be positioned anywhere on the input sine wave.

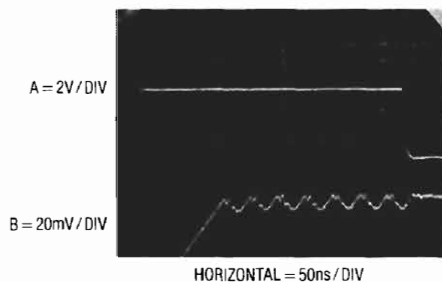


Figure 27. Track-and-Hold Circuit Acquiring an Input

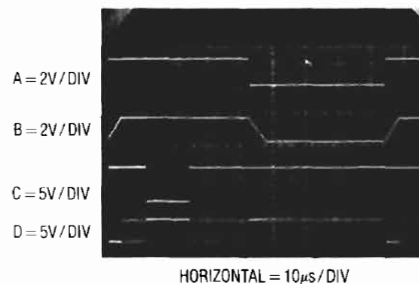


Figure 28. Track-and-Hold Responding to a Square Wave Input

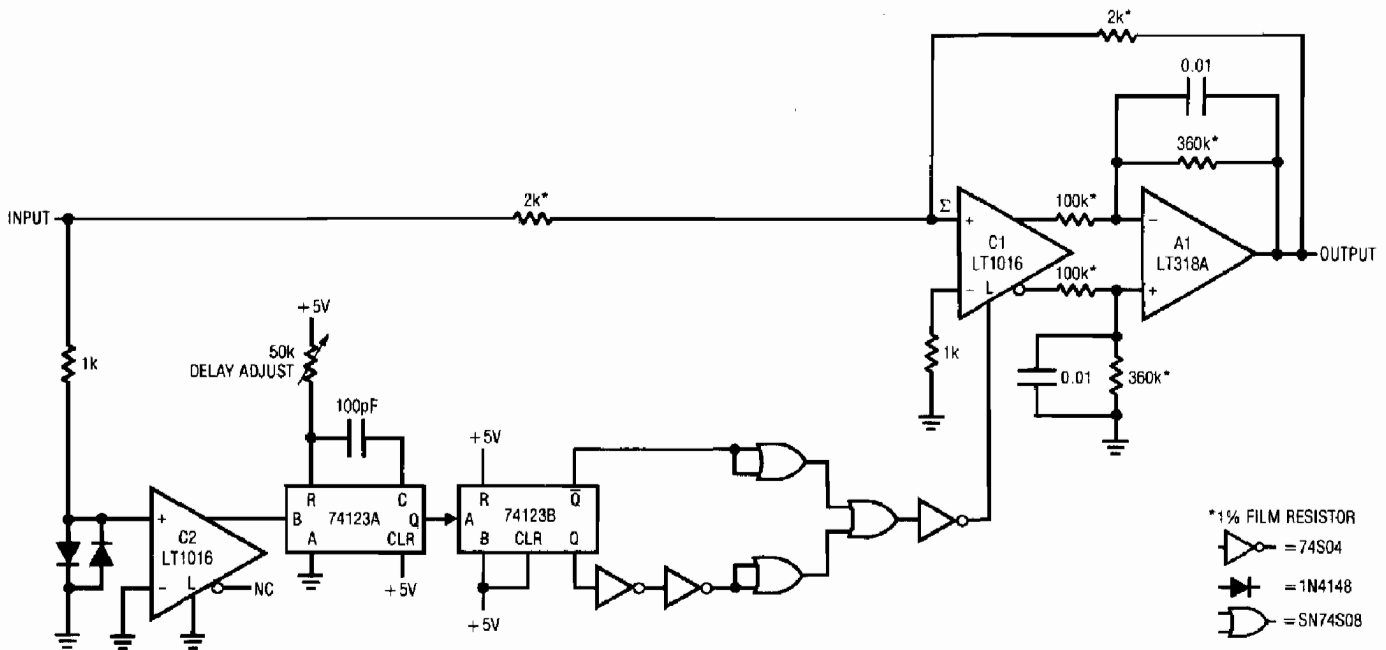


Figure 29. 10ns Sample-and-Hold for Repetitive Signals

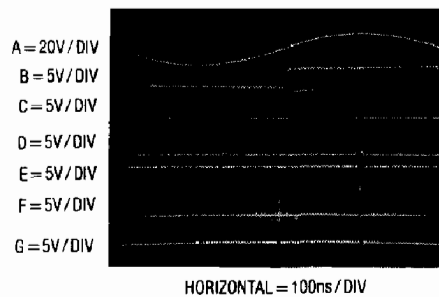


Figure 30. Waveforms for 10ns Sample-and-Hold. 10ns Sampling Window (Trace G) May be Positioned Anywhere on Input (Trace A)

5 μ s, 12-Bit A-D Converter

The LT1016's high speed is used to implement a fast 12-bit A-D converter in Figure 31. The circuit is a modified form of the standard successive approximation approach and is faster than most commercial SAR 12-bit units. In this arrangement the 2504 successive approximation register (SAR), A1 and C1 test each bit, beginning with the MSB, and produce a digital word representing V_N 's value. To get faster conversion time, the clock (C2) is sped up after the third MSB is converted. This takes advantage of

the segmented DAC used, which has significantly faster settling time for the lower 9 bits.

A1 provides preamplification for C1 while adding only 7ns delay. The preamplification allows clean response to $\frac{1}{2}$ LSB (1.22mV) overdrives at A1's input. Figure 32 shows the converter at work. To aid in observing operation, A1 has been eliminated and the DAC-input node drives the LT1016 "+" input directly. A1 should be employed in normal use.

Application Note 13

Inexpensive, Fast 10-Bit Serial Output A-D

Figure 33 shows a simple way to build a fast, inexpensive 10-bit A-D converter. This circuit is especially useful where a large number of converters is required and all of them can be serviced by one clock. The design consists of a current source, an integrating capacitor, a comparator and some gates.

Every time a pulse is applied to the convert command input (Trace A, Figure 34), Q1 resets the 1000pF capacitor to 0V (Trace B). This resetting action takes 200ns — the minimum acceptable convert command pulse width. On the falling edge of the convert command pulse, the capacitor begins to charge linearly. In precisely 10 μ s, it charges to 2.5V (over range to 3.0V is provided). Normally, Q1 would not be able to reset the capacitor to zero due to its V_{CE} saturation voltage. This effect is compensated by Q4. This device switches in inverting mode,

resulting in a reset within 1mV of ground. Q1 absorbs most of the capacitor's charge and Q4 completes the discharge.

The 10 μ s ramp is applied to the LT1016's positive input. The LT1016 compares the ramp to Ex, the unknown, at its negative input. For a 0V–2.5V range, Ex is applied to the 2.5k Ω resistor. For a 0V–10V range, the 2.5k Ω resistor is grounded and Ex is applied to the 7.5k Ω resistor. The 2.0k resistor at the positive input provides balanced source impedance for C1. The output of the LT1016 is a pulse (Trace C) whose width is directly dependent on the value of Ex. This pulse width is used to gate a 100MHz clock. The 74AS00 gate achieves this function and also gates out the portion of the LT1016 output pulse due to the convert command pulse. Thus, the 100MHz clock pulse bursts that appear at the output

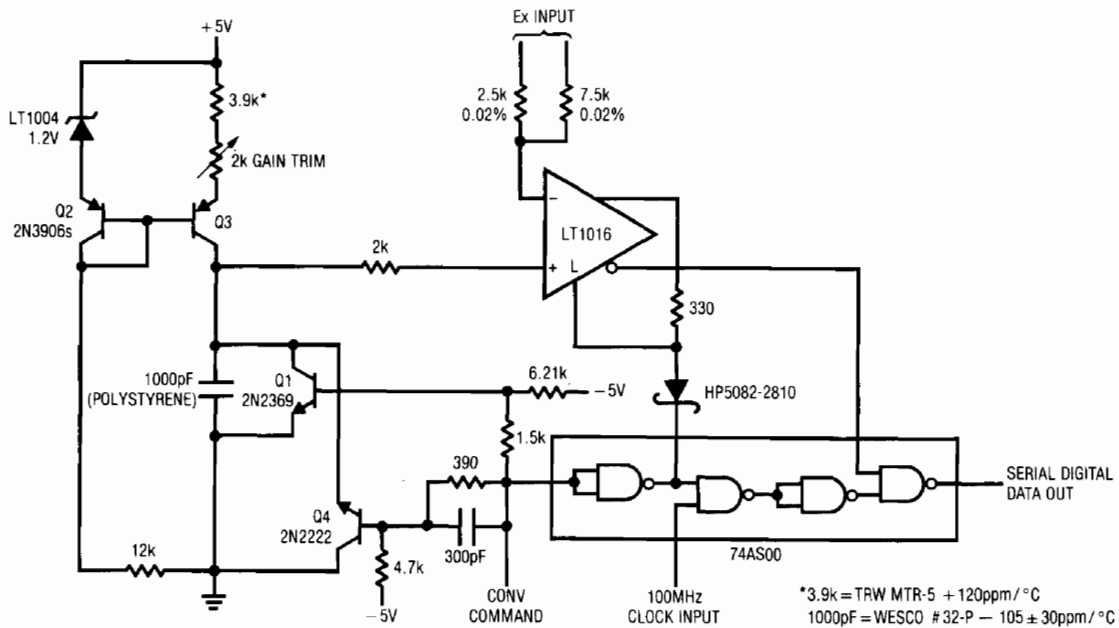


Figure 33. Simple, Fast 10-Bit A → D

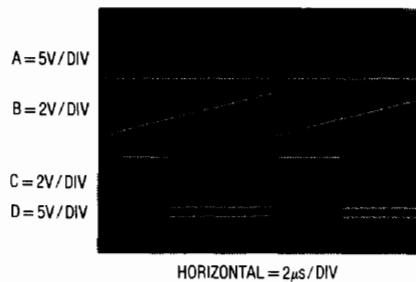


Figure 34. Waveforms for 10-Bit A → D

(Trace D) are proportional to Ex. For a 0V–10V input, 1024 pulses appear at full-scale, 512 at 5.00V, etc. The resistor-diode network at the LT1016's latch pin ensures clean comparator transitions by locking the LT1016 outputs after the conversion is completed. This latch is broken by the next convert command pulse.

The current source scaling resistor and ramp capacitor specified provide good temperature compensation because of their opposing thermal coefficients. The circuit will typically hold ± 1 LSB accuracy over 0°C–70°C with an additional ± 1 LSB uncertainty due to the asynchronous relationship between the clock and the conversion sequence.

Figure 35 details the most critical part of the converter's operation, the reset phase. Trace A is the convert command. Trace B is the capacitor (greatly magnified) resetting to zero. The comparator output appears in Trace C and Trace D is the gated serial output. Observe that the output pulses do not appear until the capacitor has started to ramp (just past mid-screen), even though the comparator is high.

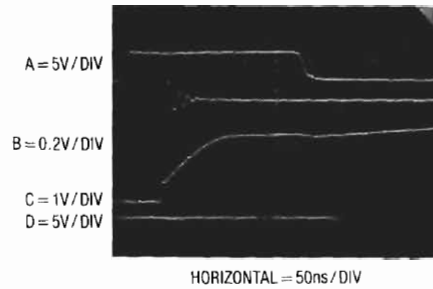


Figure 35. Figure 33's Reset Sequence. Q1-Q4 Combination Gives Quick, Low Offset Zero Reset

2.5MHz Precision Rectifier/AC Voltmeter

Most precision rectifier circuits rely on operational amplifiers to correct for diode drops. Although this scheme works well, bandwidth limitations usually restrict these circuits to operation below 100kHz. Figure 36 shows the LT1016 in an open-loop, synchronous rectifier configuration which has high accuracy out to 2.5MHz. An input

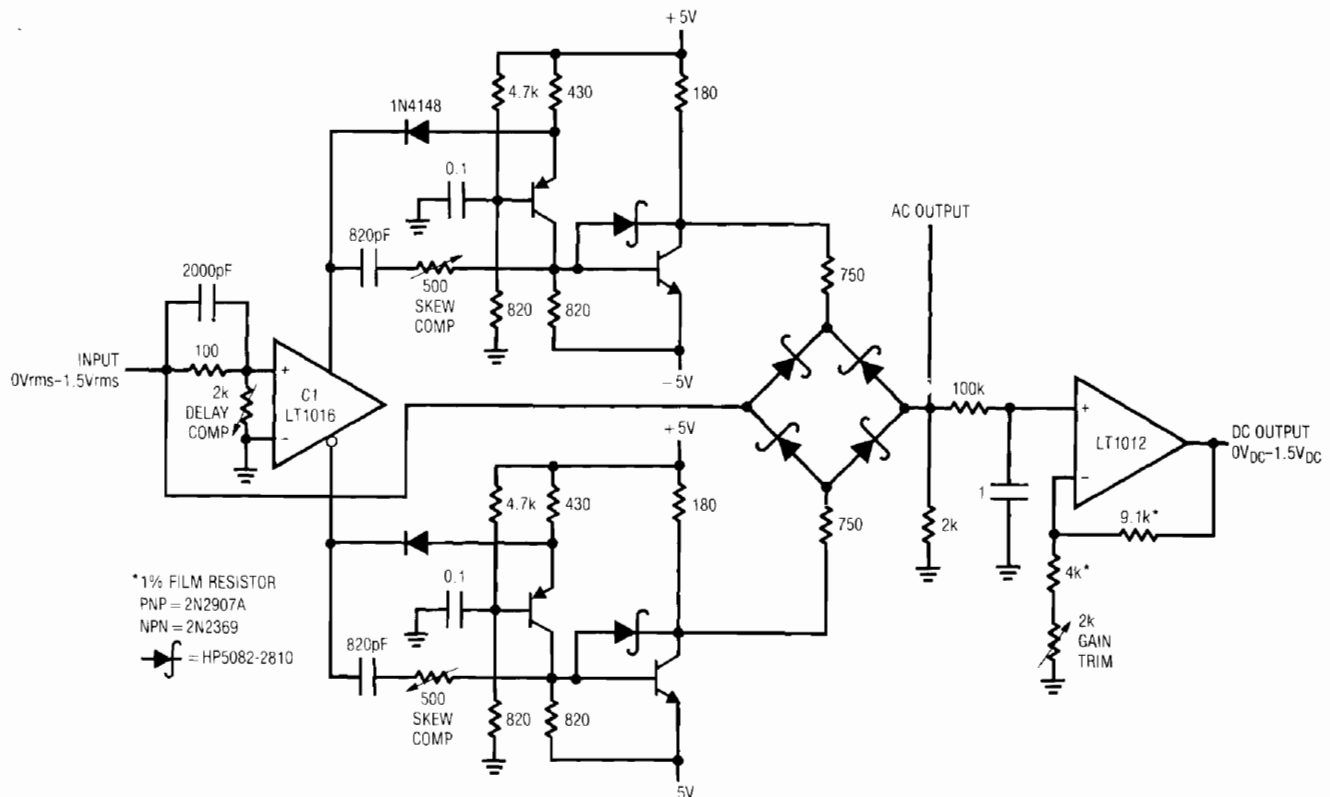


Figure 36. Fast, Synchronous Rectifier-Based AC-DC Converter

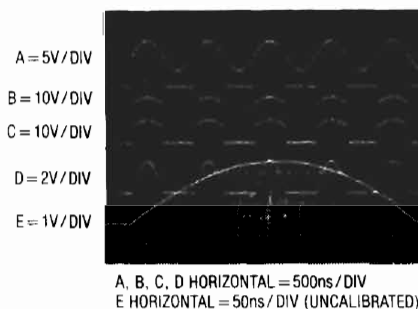
Application Note 13

1MHz sine wave (Trace A, Figure 37) is zero cross detected by C1. Both of C1's outputs drive identical level shifters with fast (delay = 2ns–3ns), $\pm 5V$ outputs. These outputs bias a Schottky switching bridge (Traces B and C are the switched corners of the bridge). The input signal is fed to the left-midsection of the bridge. Because C1 drives the bridge synchronously with the input signal, a half-wave rectified sine appears at the AC output (Trace D). The DC RMS value appears at the DC output. The Schottky bridge gives fast switching and eliminates the charge pump-through that a FET switch would contribute. This is evident in Trace E, which is an expanded version of Trace D. The waveform is clean with the exception of very small disturbances where bridge switching occurs. To calibrate this circuit, apply a 1MHz–2MHz 1Vp-p. Sine wave and adjust the delay compensation so bridge switching occurs when the sine crosses zero. This adjustment corrects for the small delays through the LT1016 and the level shifters. Next, adjust the skew compensation potentiometers for minimum aberrations in the AC output signal. These trims slightly shift the phase of the rising output edge of their respective level shifter. This allows skew in the complementary bridge drive signals to be kept within 1ns–2ns, minimizing output disturbances when switching occurs. A 100mV sine input will produce a clean output with a DC output accuracy of better than 0.25%.

10MHz Fiber Optic Receiver

Reception of high data rate fiber optic data is not easy. The high speed data and uncertain intensity of the light level

can cause erroneous results unless the receiver is carefully designed. The fiber optic receiver shown in Figure 38 will accurately condition a wide range of light inputs at up to 10MHz data rates. Its digital output features an adaptive threshold trigger which accommodates varying signal intensities due to component aging and other causes. An analog output is also available to monitor the detector output. The optical signal is detected by the PIN photodiode and amplified by a broadband fed-back stage, Q1–Q3. A second, similar, stage gives further amplification. The output of this stage (Q5's collector) biases a 2-way peak detector (Q6–Q7). The maximum peak is stored in Q6's emitter capacitor, while the minimum excursion is retained in Q7's emitter capacitor. The DC value of Q5's output signal's mid-point appears at the junction of the 500pF capacitor and the 22Meg units. This point will always sit midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by the low bias LT1012 to set the trigger voltage at the LT1016's positive input. The LT1016's negative input is biased directly from Q5's collector. Figure 39 shows the results using the test circuit indicated in Figure 38. The pulse generator's output is Trace A, while Q5's collector (analog output monitor) appears in Trace B. The LT1016 output is Trace C. The wideband amplifier responds within 5ns and rises in 25ns. Note that the LT1016's output transitions line up with the mid-point of Trace B, in accordance with the adaptive trigger's operation.



**Figure 37. Fast AC-DC Converter Operating at 1MHz.
Clean Switching is Due to LT1016's Speed and
Compensations for Delay and Switching Skew**

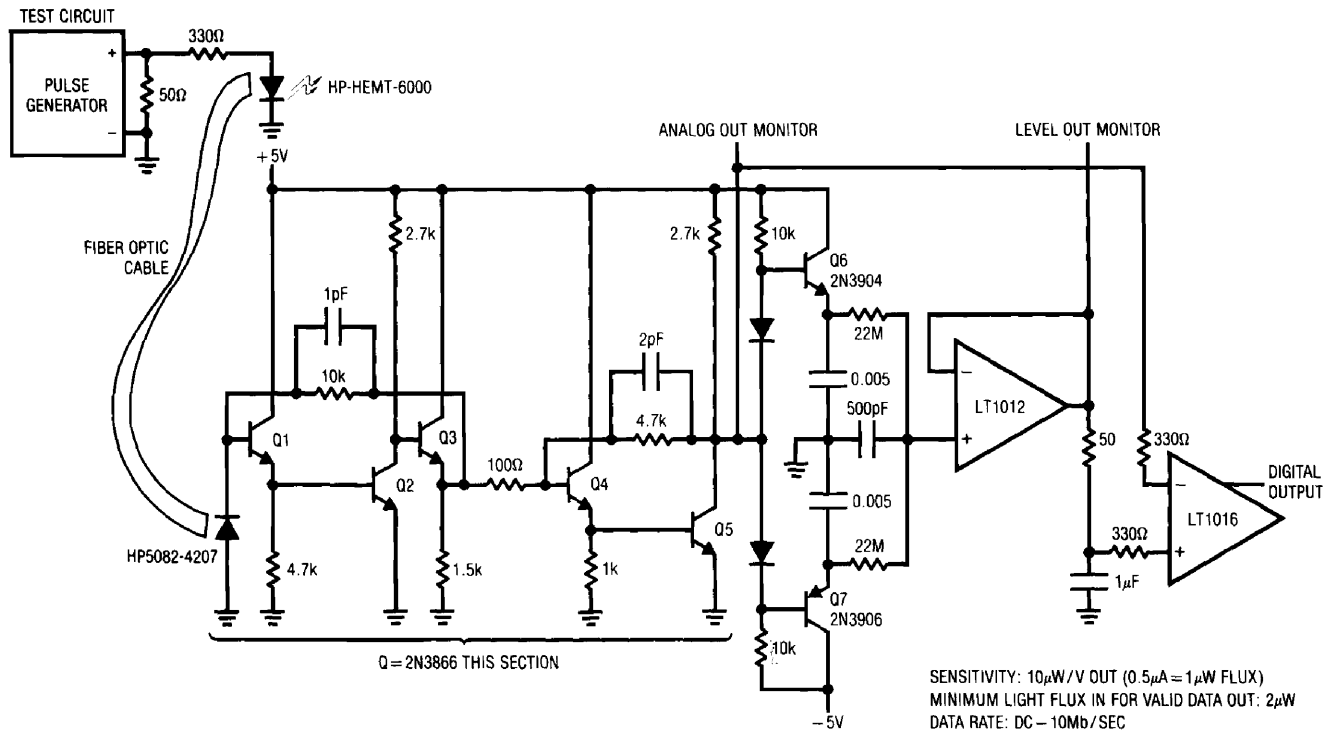


Figure 38. Fast Fiber Optic Receiver is Immune to Shifts in Operating Point

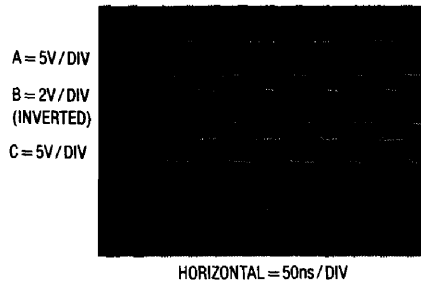


Figure 39. Fiber Optic Receiver Waveforms

12ns Circuit Breaker

Figure 40 shows a simple circuit which will turn off current in a load 12ns after it exceeds a preset value. This circuit has been used to protect integrated circuits during developmental probing and is also useful for protecting expensive loads during trimming and calibration. It is 3 times faster and less complex than previously published circuits. Under normal conditions the voltage across the 10Ω shunt is smaller than the potential at the LT1016's negative input. This keeps Q1 off and Q2 receives bias, driving the load. When an overload occurs (in this case via a test circuit, whose output is Trace A, Figure 41),

the current through the 10Ω sense resistor begins to increase (Trace B, Figure 41). When this current exceeds the preset value, the LT1016's outputs (non-inverting output shown in Trace C) reverse. This provides ideal turn-on drive for Q1 and it cuts off Q2 (Q2 emitter is Trace D) in 5ns. The delay from the onset of excessive load current to complete shutdown is just 13ns. Once the circuit has triggered, the LT1016 is held in its latched state by feedback from the non-inverting output. When the load fault has been cleared the pushbutton can be used to reset the circuit.

Application Note 13

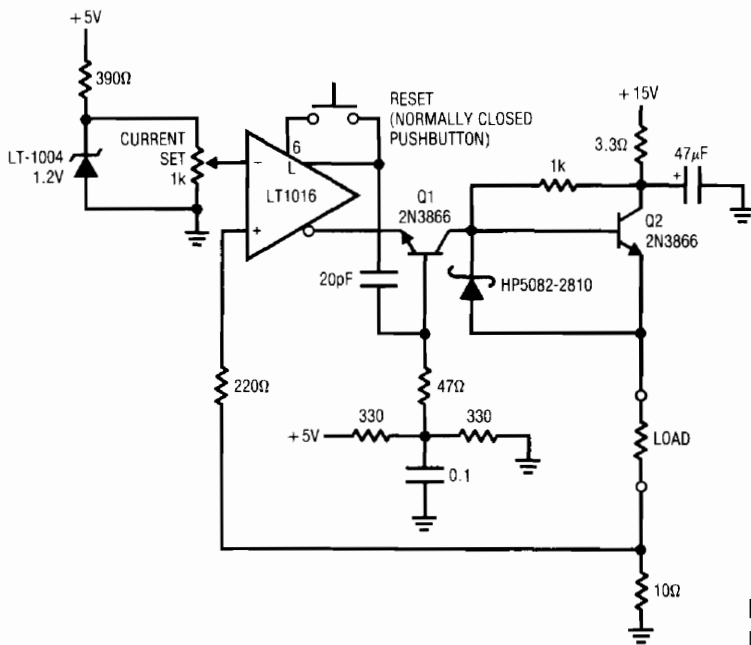


Figure 40. 12ns Circuit Breaker

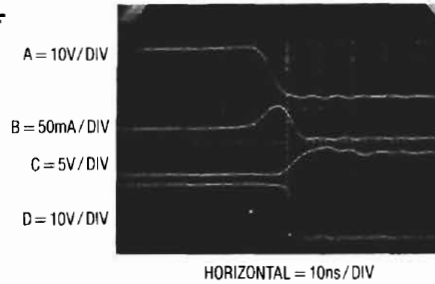


Figure 41. Operating Waveforms for the 12ns Circuit Breaker. Circuit Output (Trace D) Starts to Shut Down 12ns after Output Current (Trace B) Begins to Rise

50MHz Trigger

Counters and other instruments require a trigger circuit. Designing a fast, stable trigger is not easy, and often entails a considerable amount of discrete circuitry. Figure 42 shows a simple trigger with 100mV sensitivity at 50MHz. The FETs comprise a simple high speed buffer and the LT1016 compares the buffer's output to the potential at the "trigger level" potentiometer, which may be either

polarity. The 10k resistor provides hysteresis, eliminating "chattering" caused by noisy input signals. Figure 43 shows the trigger's response (Trace B) to a 50MHz sine wave (Trace A). To calibrate this circuit, ground the input and adjust the "input zero" control for 0V at Q2's drain terminal.

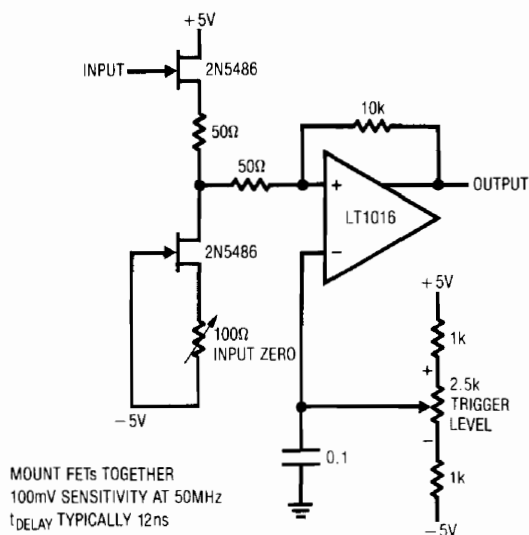


Figure 42. 50MHz Trigger

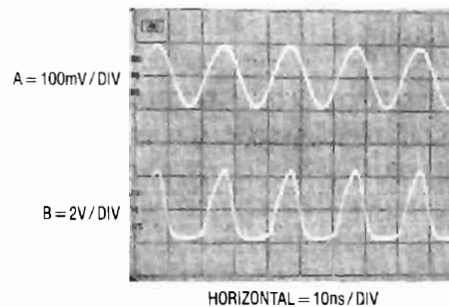


Figure 43. Trigger Responding to a 50MHz Sine Input

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APPENDIX A

About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure A1. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values

so they can absorb long transients, necessitating electrolytic types which have large series R and L.

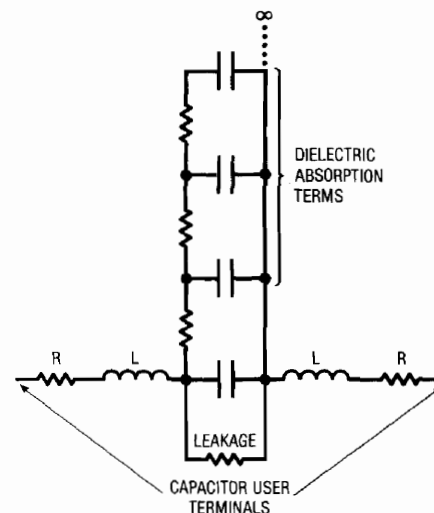


Figure A1. Parasitic Terms of a Capacitor

Application Note 13

Different types of electrolytics and electrolytic-non-polar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure A2) and accompanying photos are useful. The photos show the response of 5 bypassing methods to the transient generated by the test circuit. Figure A3 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure A4 uses an aluminum 10 μ F electrolytic to considerably cut the dis-

turbance, but there is still plenty of potential trouble. A tantalum 10 μ F unit offers cleaner response in A5 and the 10 μ F aluminum combined with a 0.01 μ F ceramic type is even better in A6. Combining electrolytics with non-polarized capacitors is a popular way to get good response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in A7. Caveat!

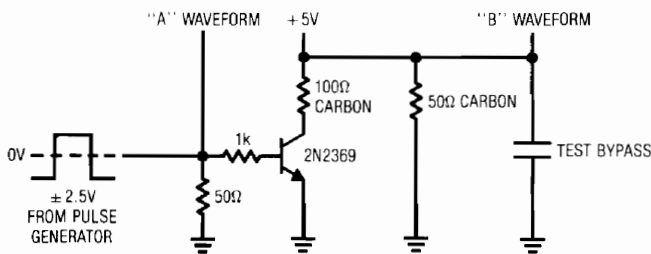


Figure A2. Bypass Capacitor Test Circuit

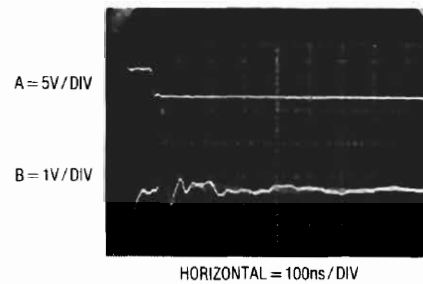


Figure A3. Response of Unbypassed Line

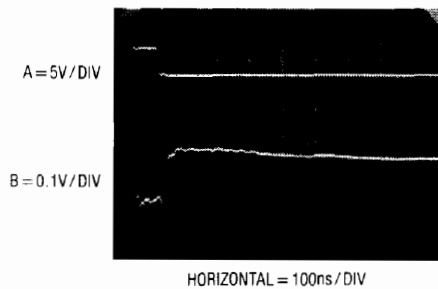


Figure A4. Response of 10 μ F Aluminum Capacitor

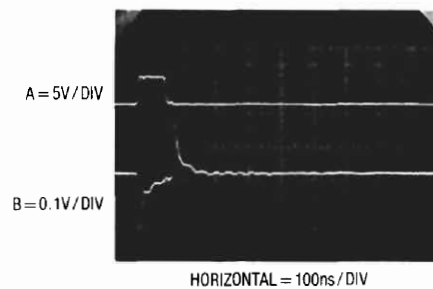


Figure A5. Response of 10 μ F Tantalum Capacitor

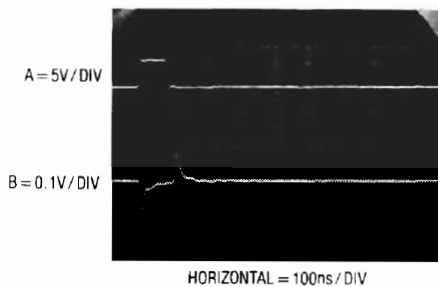


Figure A6. Response of 10 μ F Aluminum Paralleled by 0.01 μ F Ceramic

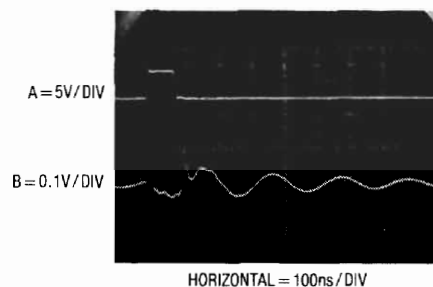


Figure A7. Some Paralleled Combinations can Ring. Try before Specifying!

APPENDIX B

About Probes and Oscilloscopes

The oscilloscope-probe combination used in high speed work is the most important equipment decision the designer must make. Ideally, the oscilloscope should have at least 150MHz bandwidth for work with the LT1016, but slower instruments are acceptable if their limitations are well understood. Be aware of your scope's behavior with respect to input impedance, noise, overdrive recovery, sweep nonlinearity, triggering, channel-to-channel feedthrough and other characteristics.

Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the point they are measuring. The most obvious is input resistance, but input capacitance usually dominates in a high speed measurement. Much time can be lost chasing circuit events which are actually due to improperly selected or applied probes. An 8pF probe looking at a 1k Ω source impedance will form an 8ns lag — close to the LT1016's response time! Low impedance probes, designed for 50 Ω inputs, (with 500 Ω to 1k Ω resistance) usually have input capacitance of 1pF or 2pF. They are a very good choice if you can stand the low resistance. FET probes maintain high input resistance and keep capacitance at the 1pF level but have substantially more delay than passive probes. FET probes also have limitations on input common-mode range which must be adhered to or serious measurement errors will result. Contrary to popular belief, FET probes *do not* have extremely high input resistance — some types are as low as 100k Ω .

Current probes are useful and convenient. The passive transformer-based types are fast and have less delay than the Hall effect-based versions. The Hall types, however, respond at DC and low frequency and the transformer types typically roll off around 100Hz to 1kHz. Both types have saturation limitations which, when exceeded, cause odd results on the CRT which will confuse the unwary.

When using different probes remember that they all have different delay times, meaning that apparent timing errors will occur on the CRT. Know what the individual probe delays are and account for them in interpreting the CRT display.

By far the greatest source of error in probe use is grounding. Poor probe grounding can cause ripples and discontinuities in the waveform observed. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is due to parasitic inductance in the probe's ground connection. In most oscilloscope measurements this is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in making the lowest possible inductive connection to ground. Most of these attachments assume a ground plane is in use, which it should be. Always try to make the shortest possible connection to ground — anything longer than 1 inch may cause trouble.

The simple network of Figure B1 shows just how easy it is for poorly chosen or used probes to cause bad results. A 9pF input capacitance probe with a 4 inch long ground-strap monitors the output (Trace B, Figure B2). Although the input (Trace A) is clean, the output contains ringing. Using the same probe with a ¼ inch spring tip ground connection accessory seemingly cleans up everything (Figure B3). However, substituting a 1pF FET probe (Figure B4) reveals a 50% output amplitude error in measurement B3! The FET probe's low input capacitance allows a more accurate version of circuit action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5ns due to delay in its active circuitry. Hence, separate measurements with each probe are required to determine amplitude and timing parameters of the output.

Application Note 13

A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can be used to introduce stray capacitance to a suspected circuit node while observing results on the CRT. Two fingers, lightly moistened, can be used to provide an experimental resistance path. Some high speed engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

Examples of the probes discussed, along with different forms of grounding implements, are shown in Figure B5.

Probes A, B, E, and F are standard types equipped with various forms of low impedance grounding attachments.

The conventional ground lead used on G is more convenient to work with but will cause ringing and other effects at high frequencies, rendering it useless. H has a very short ground lead. This is better, but can still cause trouble at high speeds. D is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. C is a separated FET probe attenuator head. Such heads allow the probe to be used at higher voltage levels (e.g., $\pm 10V$ or $\pm 100V$). The miniature coaxial connector shown can be mounted on the circuit board and the probe mated with it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended.

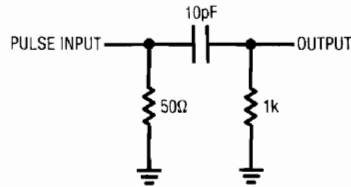


Figure B1. Probe Test Circuit

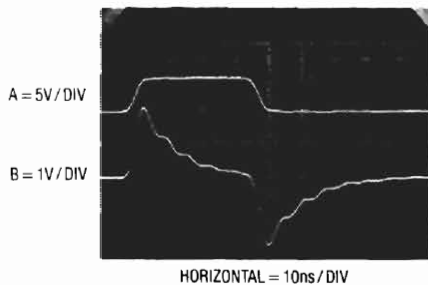


Figure B2. Test Circuit Output with 9pF Probe and 4 Inch Ground Strap

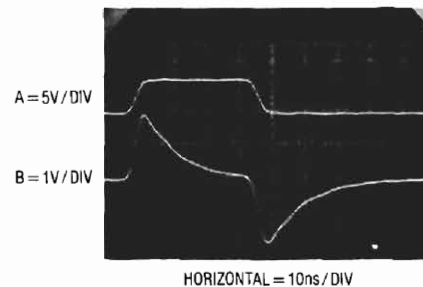


Figure B3. Test Circuit Output with 9pF Probe and 0.25 Inch Ground Strap

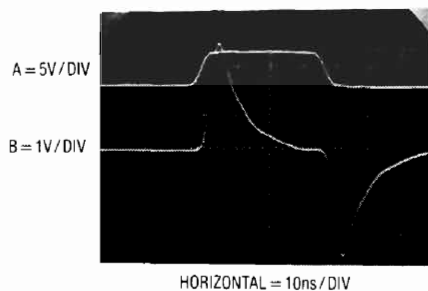


Figure B4. Test Circuit Output with FET Probe

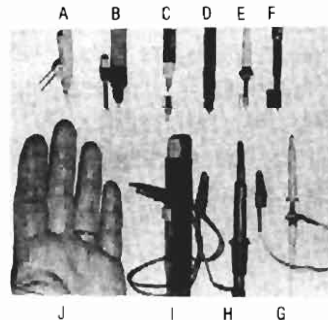


Figure B5. Various Probe-Ground Strap Configurations

I is a current probe. A ground connection is not usually required. However, at high speeds the ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible. J is typical of the finger probes described in the text. Note the ground strap on the third finger.

The low inductance ground connectors shown are available from probe manufacturers and are always supplied with good quality, high frequency probes. Because most oscilloscope measurements do not require them, they invariably become lost. There is no substitute for these devices when they are needed, so it is prudent to take care of them. This is especially applicable to the ground strap on the finger probe.

APPENDIX C

About Ground Planes

Many times in high frequency circuit layout the term "ground plane" is used, most often as a mystical and ill-defined cure to spurious circuit operation. In fact, there is little mystery to the usefulness and operation of ground planes, and like many phenomena, their fundamental operational principle is surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a wire carrying current (Figure C1) surrounded by radii of magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the wire's current. To compute the wire's inductance requires integrating the field over the wire's length

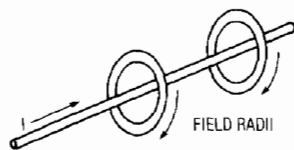


Figure C1. Single Wire Case

and the total radial area of the field. This implies integrating on the radius from $R=R_w$ to infinity, a very large number. However, consider the case where we have two wires in space carrying the same current in either direction (Figure C2). The fields produced cancel.

In this case, the inductance is much smaller than in the sample wire case and can be made arbitrarily small by reducing the distance between the two wires. This reduction of inductance between current carrying conductors is the underlying reason for ground planes. In a normal circuit, the path current takes from the signal source, through its conductor and back to ground includes a large loop area. This produces a large inductance for this conductor which can cause ringing due to LRC effects. It is worth noting that 10nH at 100MHz has an impedance of 6Ω. At 10mA a 60mV drop results.

A ground plane provides a return path directly under the signal carrying conductor through which return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents will always flow through the return path of lowest impedance. In a properly designed ground plane this path is directly under the signal conductor. In a practical circuit it is desirable to "ground plane" one whole side of the PC card (usually the component side for wave solder considerations) and run the signal conductors on the other side. This will give a low inductance path for all the return currents.

PN Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to AC "skin effect" (AC currents travel along a conductor's surface). Additionally, they aid the circuit's high frequency stability by referring stray capacitances to ground.

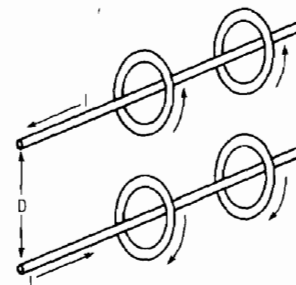


Figure C2. Two Wire Case

Application Note 13

Some practical hints for ground planes are:

1. Ground plane as much area as possible on the component side of the board, especially under traces that operate at high frequency.
2. Mount components that conduct substantial fast rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
3. Where common ground potential is important (i.e., at comparator inputs), try to single point the critical components into the ground plane to avoid voltage drops.

For example, in Figure C3's common A/D circuit, good practice would dictate that grounds 2, 3, 4 and 6 be as close to single point as possible.

Fast, large currents must flow through R1, R2, D1 and D2 during the DAC settle time. Therefore, D1, D2, R1 and R2 should be mounted close to the ground plane to minimize their inductance. R3 and C1 don't carry any current, so their inductance is less important; they could be vertically inserted to save space and to allow point 4 to be single point common with 2, 3 and 6. In critical circuits the designer must often trade off the beneficial effects of lowered inductance versus the loss of single point ground.

4. Keep trace length short. Inductance varies directly with length and no ground plane will achieve perfect cancellation.

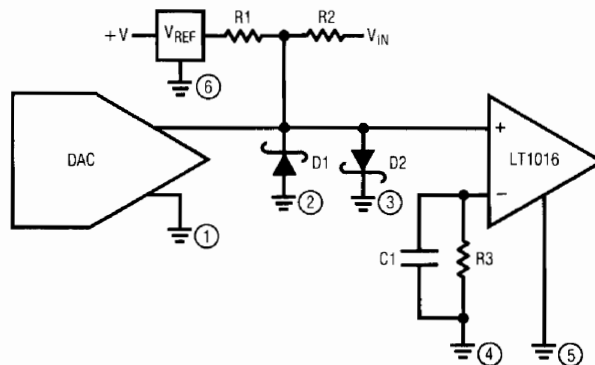


Figure C3. Typical Grounding Scheme

APPENDIX D

Measuring Equipment Response

The 10ns response time of the LT1016 and the circuitry it is used in will challenge the best test equipment. Many of the measurements made utilize equipment near the limit of its capabilities. It is a good idea to verify parameters such as probe and scope rise time and differences in

delays between probes and even oscilloscope channels. To do this, a source of very fast, clean pulses is necessary. The circuit shown in Figure D1 uses a tunnel diode to generate a pulse with a rise time well under 1ns.

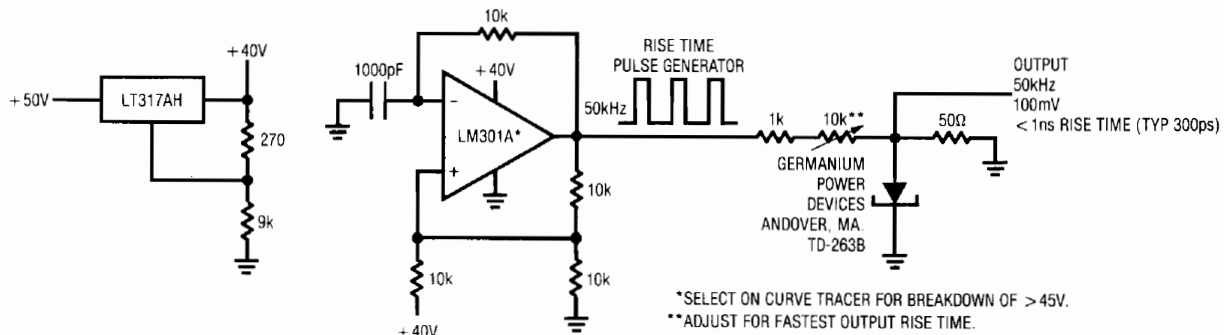


Figure D1. Tunnel Diode-Based 1ns Rise Time Pulse Generator

Figure C2 shows that the pulse is also very clean, with no attendant ringing or noise. In this photo the pulse is used to check a probe-scope combination with a specified 1.4ns rise time. The display shows that the equipment is being properly used and is in specification. Using the

tunnel diode generator to perform tests such as this can save countless hours pursuing "circuit problems," which in reality are caused by misapplied or out of spec equipment.

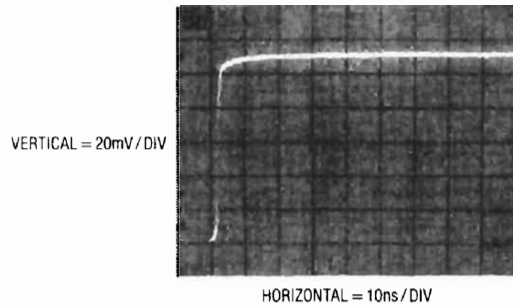


Figure D2. Figure D1's Output Monitored on a 275MHz Oscilloscope

APPENDIX E

About Level Shifts

The TTL output of the LT1016 will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1016-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1016 is a sink-source pair (Figure E1) with good ability to drive capacitance (such as feedforward capacitors).

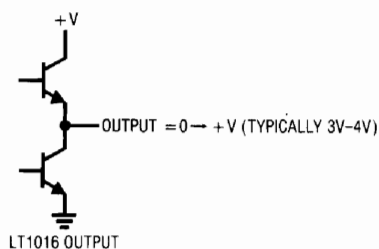


Figure E1

Figure E2 shows a non-inverting voltage gain stage with a 15V output. When the LT1016 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

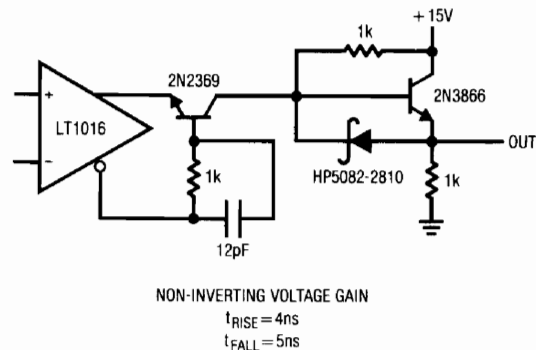


Figure E2

Application Note 13

Figure E3 is a very versatile stage. It features a bipolar swing which may be programmed by varying the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1016 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1016's output transition (Trace A, Figure E5), but Q2's switching is clean (Trace B, Figure E5) with 3ns delay on the rise and fall of the pulse.

Figure E4 is similar to E2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET which switches 1A at 15V. Most of the 7ns–9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T 's. To get the kind of results shown, switching times in the ns range and f_T 's approaching 1GHz are required.

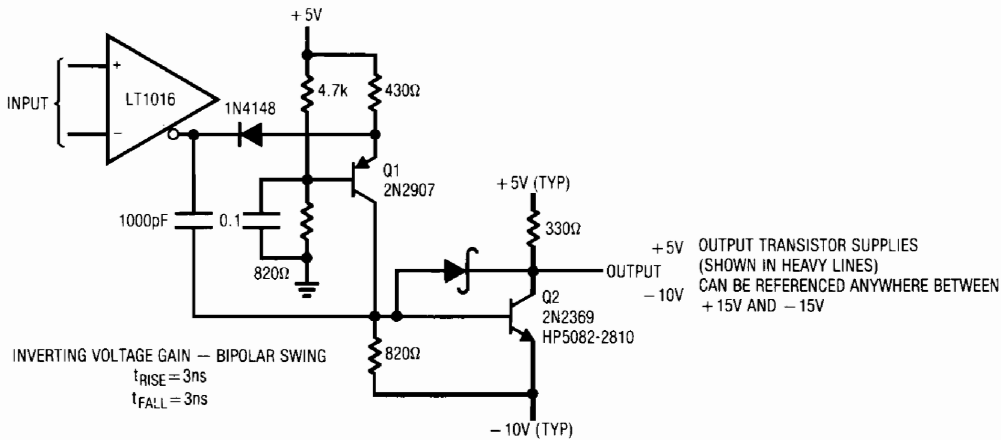


Figure E3

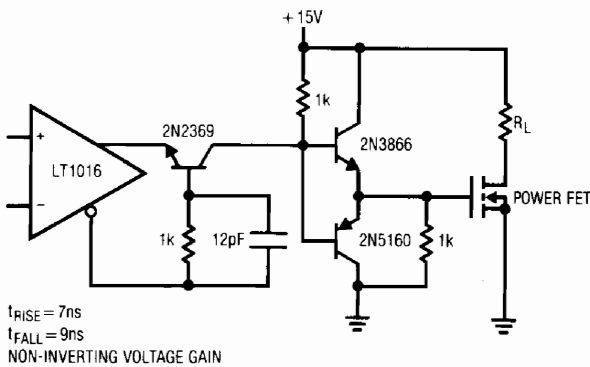


Figure E4

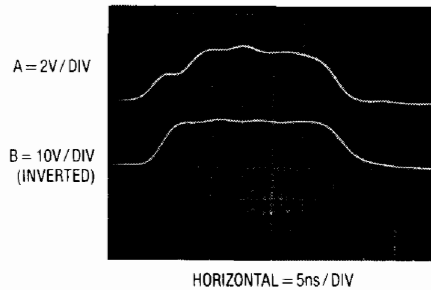


Figure E5. Figure E3's Waveforms

Designs for High Performance Voltage-to-Frequency Converters

Jim Williams

Monolithic, modular and hybrid technologies have been used to implement voltage-to-frequency converters. A number of types are commercially available and overall performance is adequate to meet many requirements. In many cases, however, very high performance or special characteristics are required and available units will not work. In these instances $V \rightarrow F$ circuits specifically optimized for the desired parameter(s) are required. This application note presents examples of circuits which offer substantially improved performance over commercially available $V \rightarrow F$ s. Various approaches (see Box Section, " $V \rightarrow F$ Design Techniques") permit improvements in speed, dynamic range, stability and linearity. Other circuits feature low voltage operation, sine wave output and deliberate nonlinear transfer functions.

Ultra-High Speed 1Hz to 100MHz $V \rightarrow F$ Converter

Figure 1's circuit uses a variety of circuit methods to achieve wider dynamic range and higher speed than any commercial $V \rightarrow F$. Rocketing along at 100MHz full-scale (10% overrange to 110MHz is provided), it leaves all other $V \rightarrow F$ s far behind. The circuit's 160dB dynamic range (8 decades) allows continuous operation down to 1Hz. Additional specifications include 0.06% linearity, 25ppm/ $^{\circ}C$ gain temperature coefficient, 50nV/ $^{\circ}C$ (0.5Hz/ $^{\circ}C$) zero shift and a 0V to 10V input range.

In this circuit an LTC[®]1052 chopper-stabilized amplifier servo-biases a crude by wide range $V \rightarrow F$ converter. The $V \rightarrow F$ output drives a charge pump. The averaged difference between the charge pump's output and the circuit's input biases the servo amplifier, closing a control loop around the wide range $V \rightarrow F$. The circuit's wide dynamic range and high speed are derived from the basic $V \rightarrow F$ s characteristics. The chopper-stabilized amplifier and charge pump stabilize the circuit's operating point, contributing high linearity and low drift. The LTC1052's 50nV/ $^{\circ}C$ offset drift allows the circuit's 100nV/Hz gain slope, permitting operation down to 1Hz.

The positive input voltage causes A1, the servo amplifier, to swing positive. The 2N3904 current sink pulls current (Trace A, Figure 2) from the varactor diode, serving as an integrated capacitor. A3 unloads the varactor and biases a trigger made up of the ECL gate and its associated components. This circuit, similar to those employed in oscilloscope triggering applications, features voltage threshold hysteresis and 1ns response time. When A3 ramps to the trigger's lower trip point, its outputs reverse state. The inverting output, operating as an unterminated emitter-follower, deposits a fast positive current spike (Trace B) into the varactor diode integrator. The trigger-gate's complementary output goes low (Trace C), clocking the ECL $\div 16$ counter. This counter's output (Trace D), level shifted by the differential pair of 2N5160s, feeds the 4013 flip-flop. The 4013's square wave drive (Trace E) to the LTC1043 provides charge pump action. The switch-capacitor pairs in the LTC1043 run out of phase and charge is pumped (Trace F) from A1's positive input on each edge of the LTC1043's square wave input. The amount of charge delivered per cycle is primarily dependent on the LT[®]1009 voltage reference and the 100pF value of the capacitors ($Q = CV$). The slight difference between the charge delivered on the clock's rising and falling edge is due to capacitor tolerances and does not influence circuit operation. The charge pump's overall accuracy is determined by the stability of the LT1009 and the capacitors and the low charge injection of the LTC1043. The ECL counter and the flip-flop divide the trigger's output by 32, setting the LTC1043's maximum switching frequency at about 3MHz (100MHz \div 32); within its specified operating range. The 0.22 μ F capacitor integrates the pumping action to DC. The averaged difference between the positive input-derived current and the charge pump feedback signal is amplified by A1, which servo-controls the circuit's operating point. The compensation capacitor at A1 provides stable loop compensation. Nonlinearity and drift in the basic $V \rightarrow F$

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Application Note 14

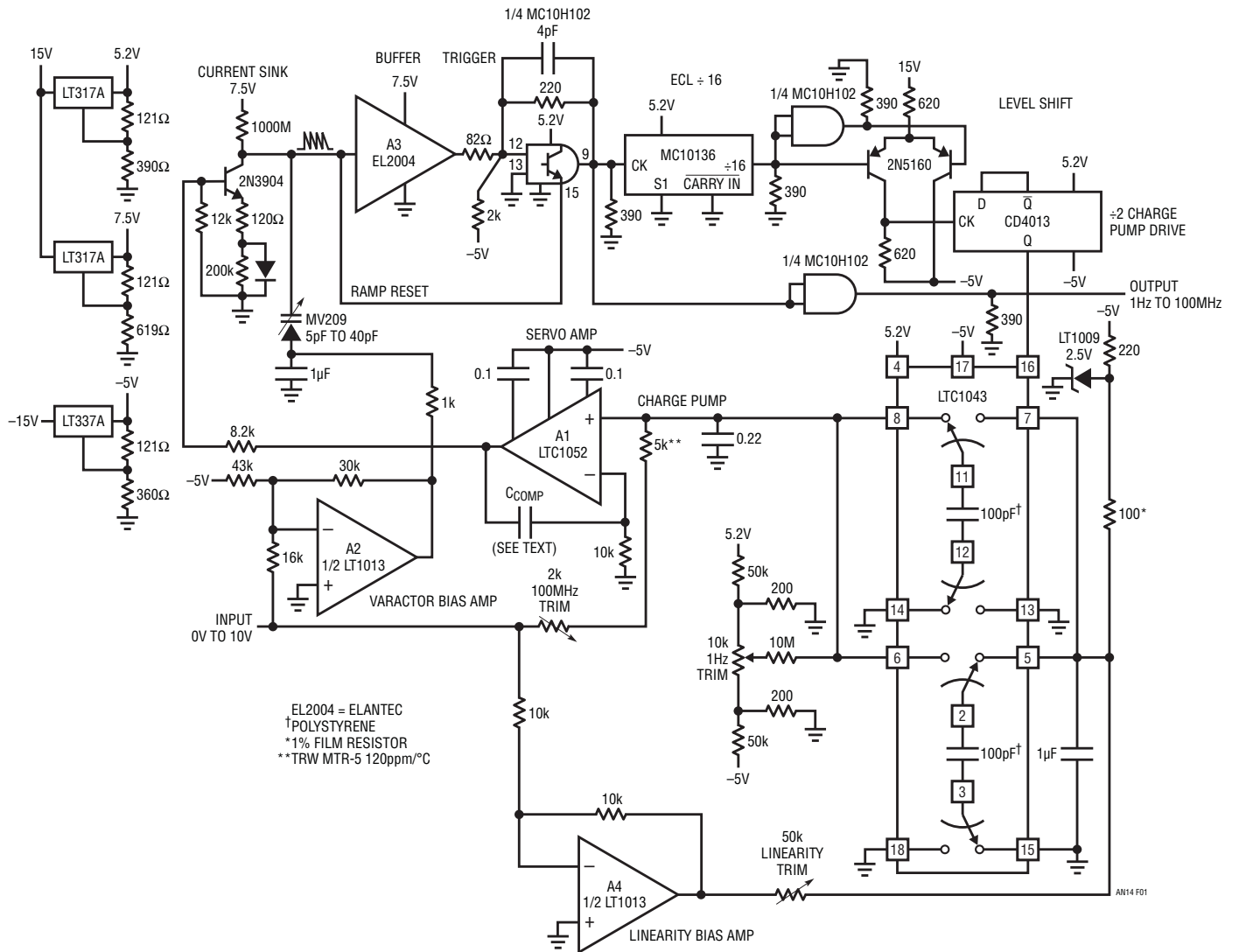


Figure 1. 1Hz to 100MHz Voltage-to-Frequency Converter (King Kong V→F)

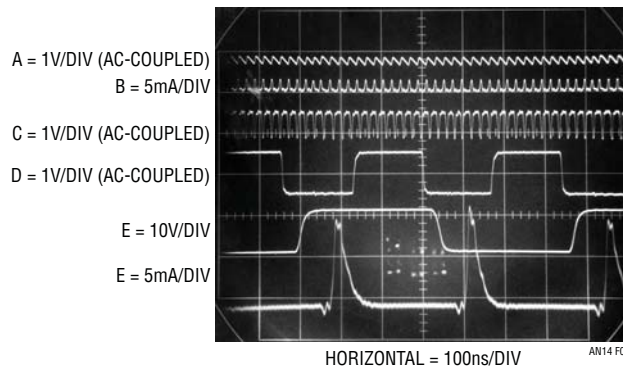


Figure 2. 1Hz to 100MHz V→F Waveforms

circuit are compensated by A1's servo action, resulting in the high linearity and low drift previously noted.

Some special techniques are required for this circuit to achieve its specifications. A2, driven from the input voltage, provides DC bias for the varactor diode-integrating capacitor. This DC bias causes the varactor's capacitance to vary inversely with input, helping the circuit achieve its 8-decade dynamic range. The $1\mu\text{F}$ capacitor, in series with the varactor, gives the relatively large ramp currents a low impedance path to ground. The 1000M resistor in the current sink sources enough current to swamp the effects of all leakages from the 2N3904 collector. This ensures that current must always be sunk from the varactor-integrator to sustain oscillation, even at the very lowest frequencies.

The 200k diode combination in the 2N3904's emitter reduces low frequency jitter. It does this by reducing current sink noise at low frequencies by increasing emitter resistance at low base bias voltages.

The 2k pull-down resistor at the trigger input ensures clean, quick transitions at low ramp slew rates, aiding low frequency jitter performance.

The 5k input resistor specified has a temperature coefficient which opposes that of the polystyrene capacitors in the charge pump. This reduces the effect of their tempco, lowering overall circuit gain drift.

A4 supplies a small, input-related current to the charge pump's voltage reference, correcting nonlinear terms due to residual charge imbalance in the LTC1043. The input-derived correction is effective because the effect of this imbalance varies directly with frequency.

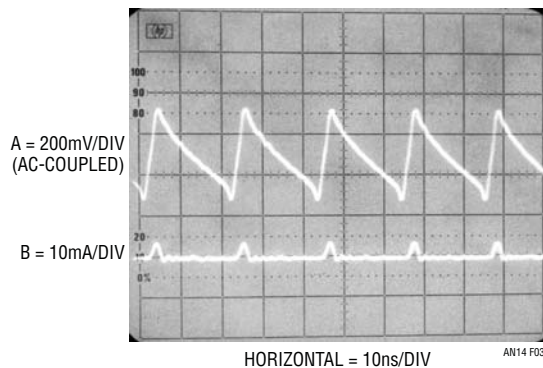


Figure 3. Ramp and Reset Current Detail at 50MHz

The 100MHz full-scale frequency sets stringent restrictions on oscillator cycle time. At this frequency only 10ns is available for a complete ramp-and-reset sequence. The ultimate limitation on speed in the circuit is the time required to reset the varactor integrator. Figure 3 shows high speed details. The combination of a small amplitude ramp and fast ECL switching yields the necessary high speed operation. Trace A is the ramp and Trace B is the reset current from the ECL gate's open emitter. Note that reset occurs in 3.5ns , with little aberration or overshoot.

Figure 4 plots output frequency jitter as a function of frequency. At 100MHz , jitter is 0.01% , falling to about 0.002% at 1MHz . In this range the jitter is dominated by noise in the current source and ECL inputs. Below this, jitter slowly rises as operating frequency approaches the servo amplifier's roll off. At 1kHz (10ppm of full scale) jitter is still below 1% , with about 10% jitter at 1Hz (0.01ppm) for $C_{\text{COMP}} = 1\mu\text{F}$. With $C_{\text{COMP}} = 0.1\mu\text{F}$, jitter increases below 1kHz and operation below 10Hz is not possible due to loop instability and A1's noise floor. The trade-off is loop settling time. With the larger compensation capacitor the loop settles in 600ms . The $0.1\mu\text{F}$ value permits 60ms settling.

To calibrate this circuit, apply 10.000V and trim the 100MHz adjustment for 100.00MHz at the output. If a fast enough counter is not available, the $\div 32$ signal at Pin 16 of the LTC1043 will read 3.1250MHz . Next, ground the input, install $C_{\text{COMP}} = 1\mu\text{F}$ and adjust the "1Hz trim" until the circuit oscillates at 1Hz . Finally, set the "linearity trim" to 50.00MHz for a 5.000V input. Repeat these adjustments until all three points are fixed.

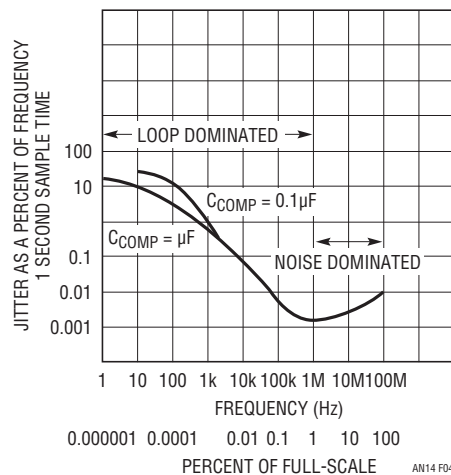


Figure 4. Jitter vs Output Frequency

Application Note 14

Fast Response 1Hz to 2.5MHz V→F Converter

Figure 5's circuit is not nearly as fast as Figure 1's, but its 2.5MHz output settles from a full-scale input step in only 3μs. This makes the circuit a good candidate for FM applications or any area where fast response to input movement is required. Linearity is 0.05% with a 50ppm/°C gain tempco. A chopper-stabilized correction network holds zero-point error to 0.025Hz/°C. This circuit, a high speed charge-dispersing type (see Box Section) also

uses charge feedback. The charge feedback scheme used is a highly modified, high speed variant of the approach originally described by R. A. Pease (see References). A servo amplifier is not used, permitting fast response to input steps. Instead, the charge is fed back directly to the oscillator, which can respond immediately. Although this approach permits fast response, it also requires attention to parasitics to achieve high linearity and low drift.

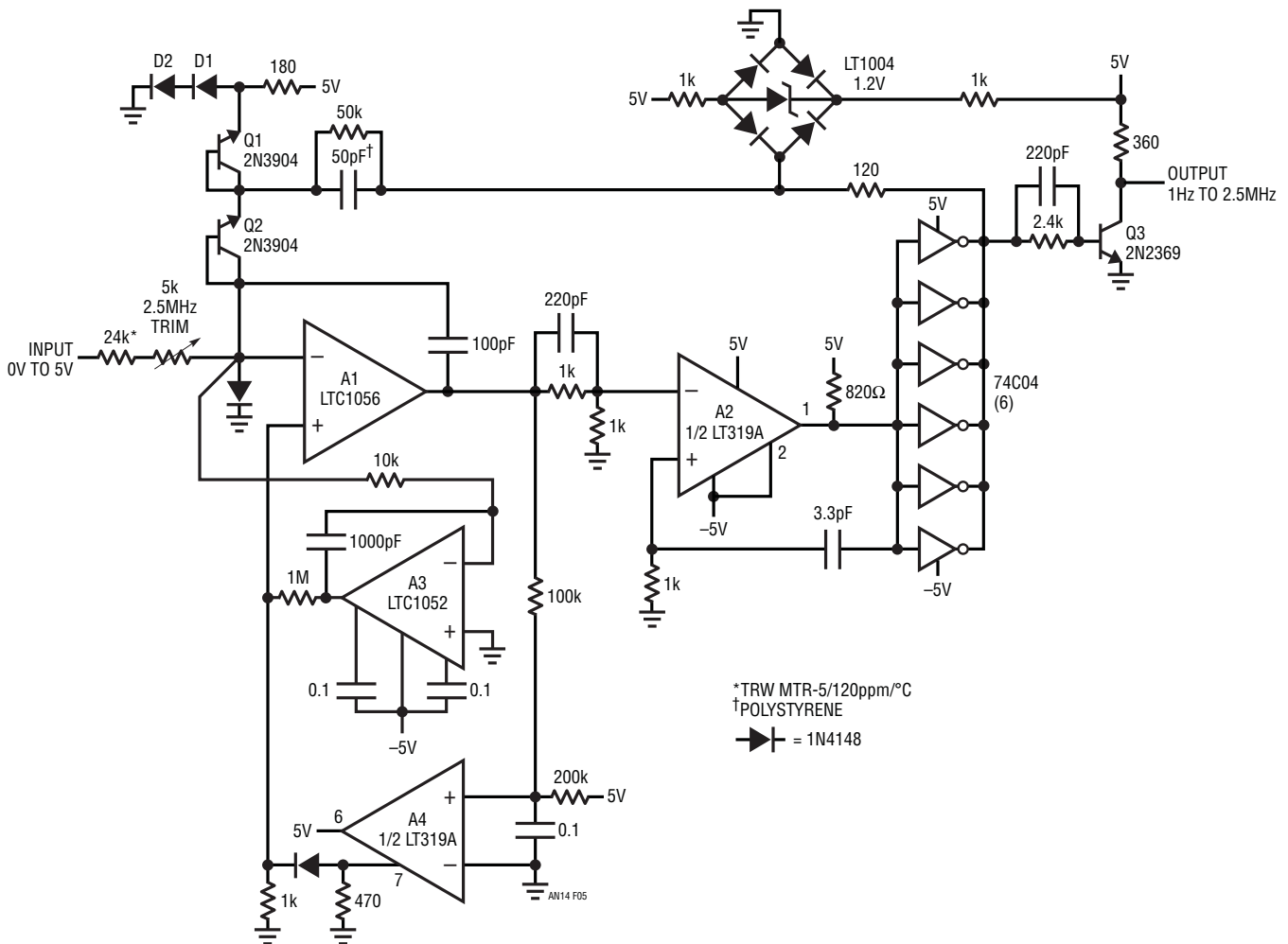


Figure 5. 1Hz to 2.5MHz Fast Response V→F

When an input voltage is applied, A1 integrates in a negative direction (Trace A, Figure 6). When its output crosses zero, A2's output switches, causing the paralleled inverters to go low (Trace B). The feedforward network in A2's negative input aids response. This causes the LT1004 diode bridge to bound at $-2.4V (-V_Z \text{ LT1004}) + (-2V_{FWD})$. Local positive feedback at A2's positive input (Trace C) reinforces this action. During this interval, charge is pulled (Trace D) from A1's summing junction via the 50pF-50k combination, forcing A1's output to move quickly positive. This causes the A2 inverter combination to switch positive (Trace B), bounding the LT1004 diode bridge at 2.4V. Now the 50pF capacitor receives charge, while A1 again integrates negative, and the entire cycle repeats. The frequency of this action is a linear function of the input voltage.

D1 and D2 compensate the diodes in the bridge. Diode-connected Q1 compensates steering diode Q2. (The diode-connected transistors provide lower leakage from the summing junction than conventional diodes.) A3, a chopper-stabilized op amp, offset stabilizes A1, eliminating the necessity for zero trimming.

A4 guards against circuit latch-up, which can occur due to the AC-coupled feedback loop. If the circuit latches, A1's output goes to the negative rail and stays there. This causes A4's output (A4 is used in emitter-follower output mode) to go high. A1's output now heads positive, initiating normal circuit behavior. The diode at A1's

negative input ensures that the start-up loop will dominate over any input condition.

The 50k resistor across the 50pF charge-dispensing capacitor improves linearity by permitting complete discharge on each cycle, despite junction tailing effects in Q2. The input resistor specified has a temperature coefficient opposite that of the capacitor's enhancing circuit gain tempo.

Figure 7 shows circuit step response. Trace A is the input, while Trace B is the output. Frequency shift is quick and clean, with no evidence of poor dynamics or time constants.

To trim the circuit, apply 5.000V and adjust the 5k potentiometer for a 2.500MHz output. A3's low offset eliminates the requirement for a zero trim. The circuit maintains 0.05% linearity with 50ppm/°C drift from 1Hz to 2.5MHz. The TTL-compatible output is available at Q3's collector (Trace E). A 10MHz full-scale circuit of this type appears in AN13.

High Stability Quartz Stabilized V→F Converter

The gain temperature coefficient of the previous circuits is affected by drift in the charge pumping capacitors. Although compensation schemes were employed in both cases to minimize the effect of this drift, another approach is required to get significantly lower gain drift.

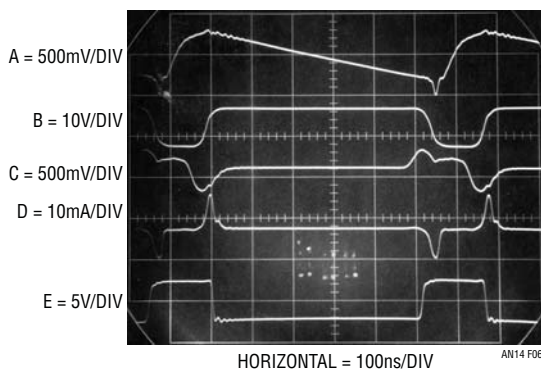


Figure 6. Fast Response V→F Waveforms

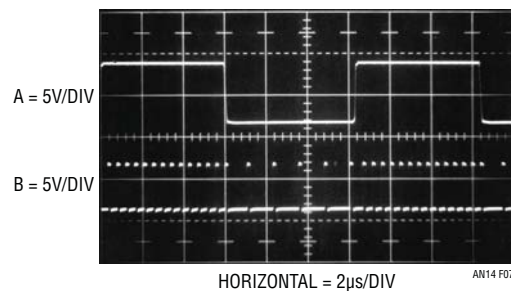


Figure 7. Step Response of 2.5MHz V→F

Application Note 14

Figure 8's circuit reduces gain TC to 5ppm/°C by replacing the capacitor with a quartz-stabilized clock.

In charge pump-based circuits the feedback is based on $Q = CV$. In a quartz-stabilized circuit the feedback is based on $Q = IT$, where I is a stable current source and T is an interval of time derived from the clock.

Figure 9 details Figure 8's waveforms of operation. A positive input voltage causes A1 to integrate in the negative direction (Trace A, Figure 9). The flip-flop's Q1 output (Trace B) changes state at the first positive-going clock edge after A1's output has crossed the D input's switching

threshold. The 50kHz clock (Trace C) comes from the flip-flop's other half, which is driven by A2, a quartz-stabilized relaxation oscillator. The flip-flop's Q1 output controls the gating of a precision current sink composed of A3, the LM199 voltage reference, a FET and the LTC1043 switch. When A1 is integrating negative, the Q1 output is high and the LTC1043 directs the current sink's output to ground via Pins 11 and 7. When A1's output crosses the D input's switching threshold, Q1 goes low at the first positive clock edge. LTC1043 Pins 11 and 8 close and a precise, quickly rising current flows out of A1's summing point (Trace D).

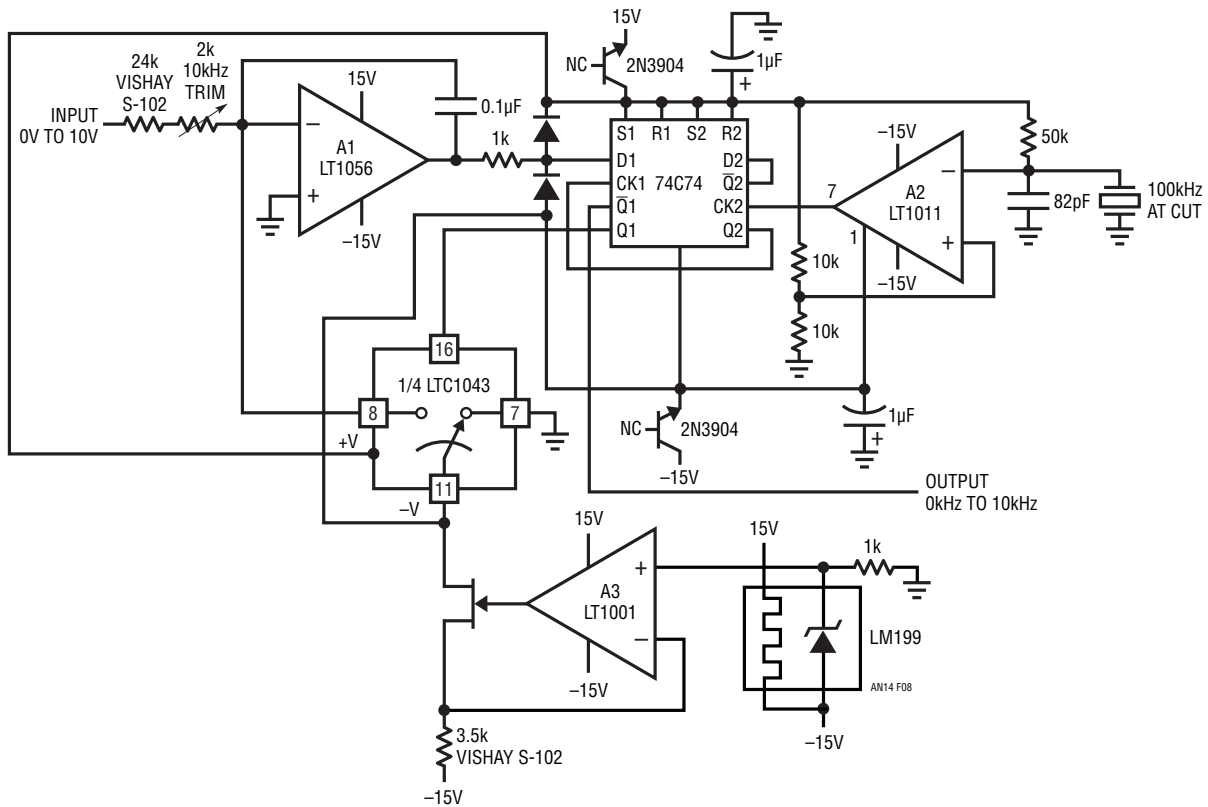


Figure 8. Quartz-Stabilized V→F

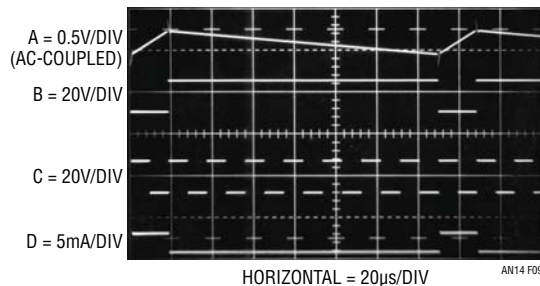


Figure 9. Waveforms for Quartz-Stabilized V→F

This current, scaled to be greater than the maximum signal-derived input current, causes A1's output to reverse direction. At the first positive clock pulse after A1's output crosses the D input's trip point, switching again occurs and the entire process repeats. The repetition frequency depends on the input-derived current, hence the frequency of oscillation is directly related to the input voltage. The circuit's output may be taken from the flip-flop's Q1 or $\bar{Q}1$ outputs. Because this circuit replaces the capacitor with a quartz-locked clock, temperature drift is low, typically 5ppm/°C. The quartz crystal contributes about 0.5ppm/°C, with the remaining drift a function of the current source components, switching time variations and the input resistor.

The reverse-biased 2N3904s serve as Zener diodes, providing about 15V across the CMOS flip-flop. The diodes at the D1 input prevent transient overdrive from A1 during circuit start-up.

A V→F of this type is usually restricted to relatively low full-scale frequencies, e.g., 10kHz to 100kHz, because of speed limitations in accurately switching the current sink.

Additionally, short-term frequency jitter may occur because of the uncertain timing relationship between A1's output switching the flip-flop and the clock phase. This is normally not a problem because the circuit's output is usually read over many cycles, e.g., 0.1 to 1 second.

As shown circuit linearity is 0.005%, gain temperature coefficient is 5ppm/°C and full-scale frequency is 10kHz. The LT1056's low input offset reduces zero point error to 0.005Hz/°C. To trim this circuit, apply exactly 10V in and adjust the 2k potentiometer for 10.000kHz output.

Ultra-Linear V→F Converter

Figure 10 shows a V→F circuit optimized for very high linearity. Although it may be used in a "stand-alone" mode it is specifically intended for processor-driven applications which require 17-bit accuracy, such as weighing scales. This V→F has a resolution of 1ppm, with linearity inside 7ppm (0.0007%). When combined with a processor-driven gain/zero calibration loop it has negligible zero and gain drift. To further ease interface with processor-based systems, the circuit functions from a single 5V power supply.

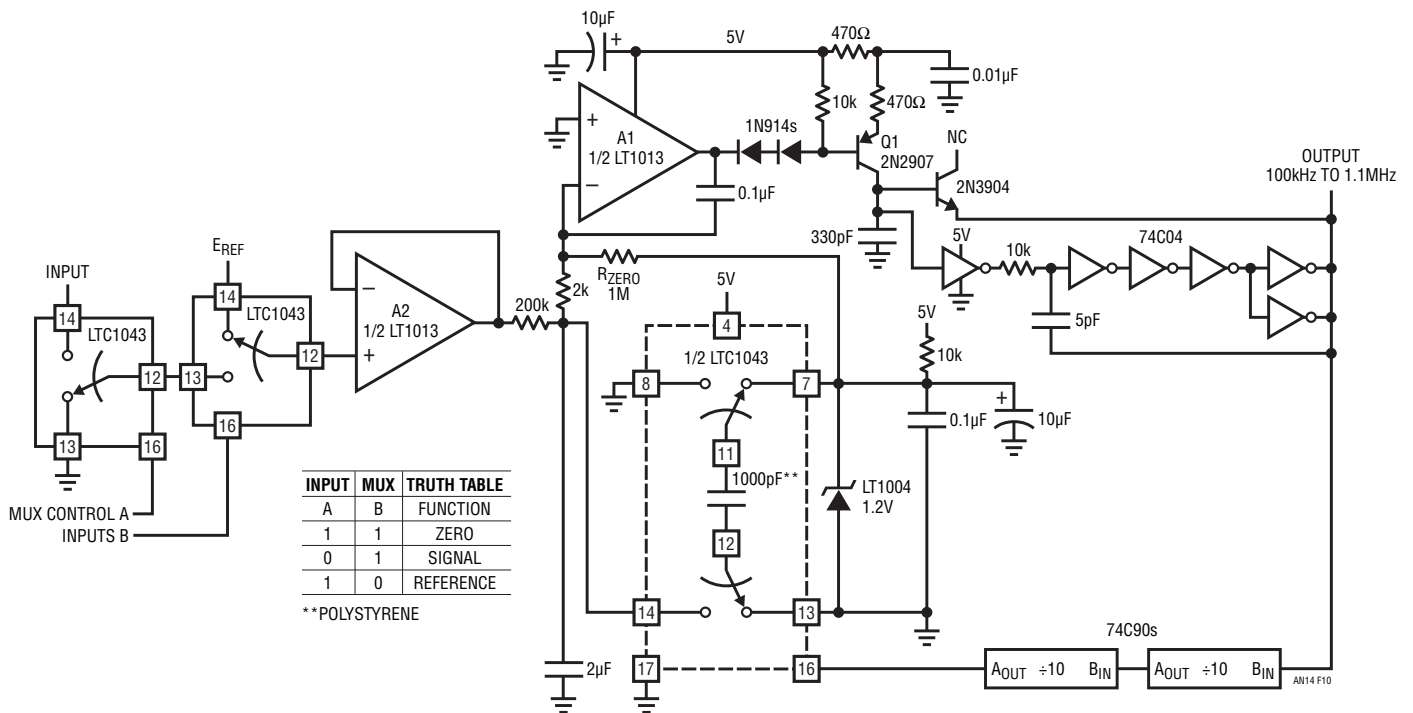


Figure 10. Ultra-Linear V→F

Application Note 14

The circuit is conceptually similar to the 100MHz $V \rightarrow F$ of Figure 1. A1 servo-controls a crude $V \rightarrow F$ converter composed of Q1, in this case a current source, and the 74C04 gates. The $V \rightarrow F$'s output is divided digitally and drives a charge pump whose output closes a loop back at A1. In Figure 1's case, the crude $V \rightarrow F$'s output was divided down to permit the LTC1043 to function; it cannot operate at 100MHz toggle rates. Here, the divider's purpose is to lower the toggle frequency, allowing the charge pump to achieve much higher precision than with direct feedback.

Before discussing processor-driven operation it is necessary to understand basic circuit operation. To do this, delete A2 and R_{ZERO} . Assume a positive voltage is applied to the left end of the 200k resistor which was previously connected to A2. This forces A1's output to move negatively, turning on Q1. A1's collector (Trace A, Figure 11) ramps the 330pF capacitor positively. When this ramp crosses the 74C04 inverter's threshold, its output moves toward ground, causing the entire chain to switch. AC positive feedback from the paralleled outputs enhances switching. The output inverter's signal (Trace B), the circuit's output, also drives the $\div 100$ counter chain. The counter's output (Trace C) clocks the LTC1043 which is configured to pump negative charge (Trace D) into the 200k-2k-2 μ F junction. The 2 μ F capacitor integrates the discrete charge events to DC, closing a loop around A1. Thus, A1 biases Q1 at whatever point is required to maintain its inputs at balance. This forces the crude $V \rightarrow F$'s output frequency to be a direct function of the input voltage over a 0MHz

to 1MHz output range. The relatively low LTC1043 clock frequency furnished by the dividers permits 0.0007% $V \rightarrow F$ linearity.

For processor-driven auto-zero/gain loop operation, the input multiplexer and R_{ZERO} must be added. With the multiplexer set to the "zero" function (see Truth Table), A2's input is grounded and the 200k resistor receives no drive. A1 receives bias via R_{ZERO} , however, and the circuit oscillates around 100kHz. After the processor has read this frequency it shifts the multiplexer to the "signal" function. Here, A2's output is a buffered version of the signal input. The circuit's output frequency is now determined by this input and the current through R_{ZERO} . Typical outputs will range from 100kHz to 1MHz. After reading this frequency the processor selects the "reference" multiplexer state and determines the frequency produced. The reference voltage must be greater than the largest signal input. It may be either a stable potential or one ratiometrically related to the signal input, as is the case in many transducer-based systems. Typically, it will produce a 1.1MHz output. Once this measurement sequence is completed the processor has enough information to determine the value of the signal input by mathematical manipulation. Additionally, because the multiplexing sequence occurs relatively quickly, drifts in the $V \rightarrow F$ are cancelled. No precision components are required, although the polystyrene capacitor is needed for high linearity. The circuit's 7ppm linearity and 1ppm resolution will suit almost all applications, although processor techniques could be used to obtain even better linearity.

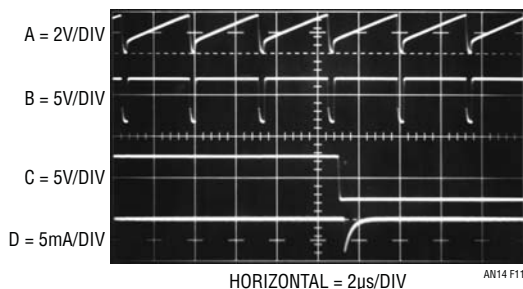


Figure 11. Ultra-Linear $V \rightarrow F$ Waveforms

Single Cell V→F Converter

High speed and precision are not the only areas where special V→F circuits are needed. Figure 12 shows a circuit which runs from a single 1.5V cell with only 125μA current drain. The circuit uses an LT1017 dual micropower comparator in a servo-controlled charge pump configuration. The input is applied to C1, which is compensated by the 10μF and 1μF capacitors to act as an op amp. C1's output drives the 110k-0.02μF RC, causing the capacitor to ramp (Trace A, Figure 13).

During the ramp, C2's output is high, turning off Q1 and biasing Q2 on. The potential across the Q3-Q4 V_{BE} voltage reference (Trace B) is zero. The 0.01μF capacitor receives no charge. When the ramp equals the potential at C2's positive input, switching occurs. C2's output goes low, and the 0.02μF unit discharges. AC positive feedback (Trace C) "hangs up" C2 long enough for a ramp reset of about 80mV. Concurrently, Q1 comes on and Q2 goes off. The Q3-Q4 reference comes on (Trace B) and charges the 0.01μF capacitor via Q6.

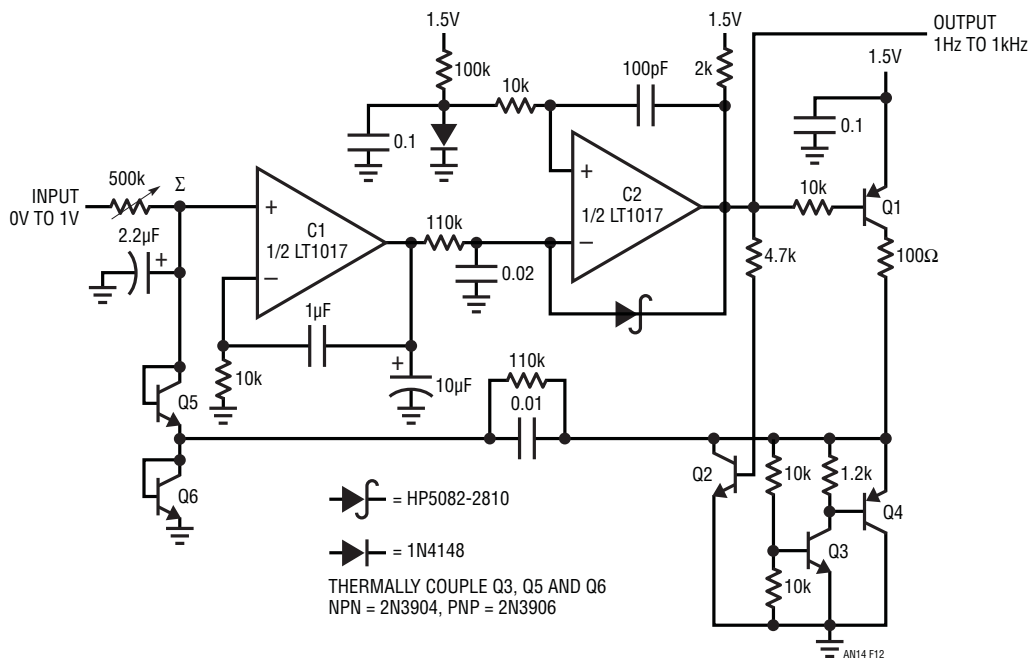


Figure 12. Single Cell V→F

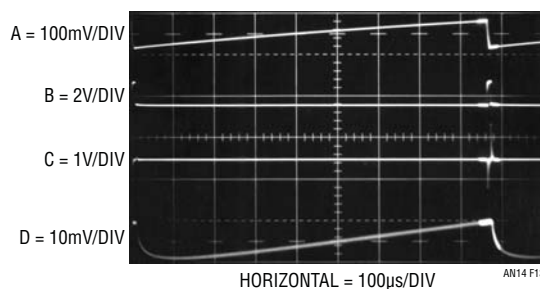


Figure 13. Single Cell V→F Waveforms

Application Note 14

When the positive feedback at C2 ceases, its output returns high, cutting off Q1 and biasing Q2. Now, the 0.01 μ F capacitor discharges, forcing current to flow from C1's 2.2 μ F summing point capacitor (Trace D) via Q5 and Q2. C1 servo-controls this oscillator to whatever frequency is required to maintain C1's summing point near zero. Since the current into C1's input is a linear function of the input voltage, oscillator frequency is also linear. The 1 μ F-10k combination at C1 provides loop stability. The 100k resistor across the 0.01 μ F capacitor influences its discharge characteristic, aiding overall circuit linearity.

The temperature coefficient of the 1.2V Q3-Q4 reference is largely compensated by the junction tempcos of Q5

and Q6, giving the circuit a 250ppm/ $^{\circ}$ C gain drift. Battery discharge introduces less than 1% error over 1000 hours operation.

Sine Wave Output V \rightarrow F Converter

Almost all V \rightarrow F converters have a pulse or square wave output. Many applications such as audio, filter testing and automatic test equipment require a sine wave output. The circuit of Figure 14 meets this need, spanning a 1Hz to 100kHz range (100dB or 5 decades) for a 0V to 10V input. It is significantly faster than previously published circuits while maintaining 0.1% frequency linearity and 0.2% distortion specifications.

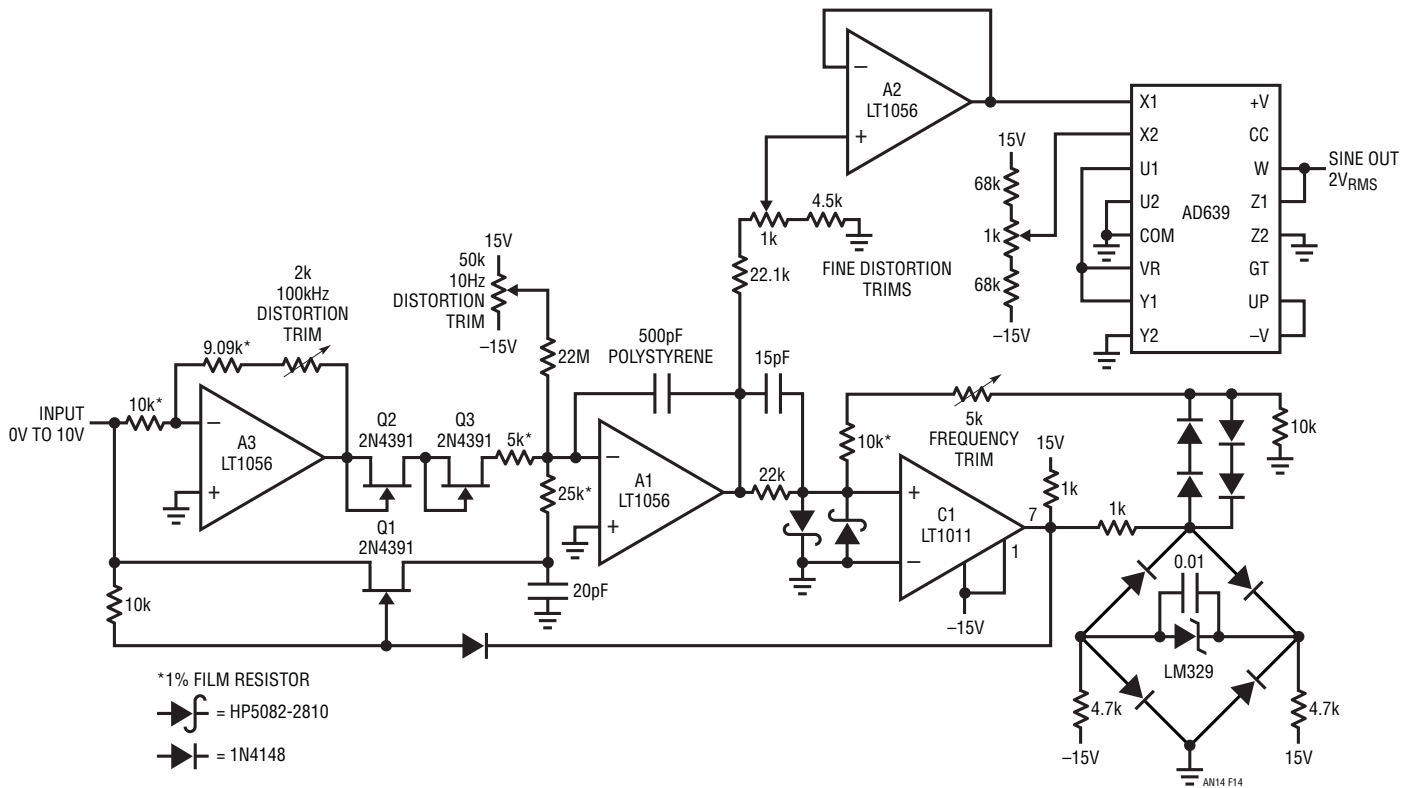


Figure 14. Sine Wave Output 1Hz to 100kHz V \rightarrow F (VCO)

To understand the circuit, assume C1 is low, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 5k resistor and the self-biased FETs. A current, $-I$, is pulled from the summing point. A1's output (Trace A, Figure 15) integrates positive until C1's input crosses 0V. When this happens, C1's output goes positive (Trace B), allowing Q1 to come on. The resistor in Q1's path is scaled to produce a current, $+2I$, exactly twice the absolute magnitude of the current, $-I$, being removed from the summing node. As a result, the net current into the junction becomes $+I$ and A1 integrates negatively at the same rate its positive excursion took. When A1 integrates far enough in the negative direction, C1's positive input crosses zero and it again switches. This turns Q1 off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 100kHz with a 0V to 10V input. The LM329 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's positive input, assuring it clean recovery from overdrive. The AD639 trigonometric function generator, biased via A2, converts A1's triangle output into a sine wave (Trace C). The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At high frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If the effects of the delays are not minimized, triangle amplitude will

increase with frequency, causing distortion level to also increase with frequency. The 15pF feedforward network at C1's input compensates the delay, keeping distortion to just 0.2% over the entire 100kHz range. At 10kHz, distortion is inside 0.07%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 20pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature dependent on-resistance of Q1, keeping the $+2I/-I$ relationship constant with temperature. Circuit gain TC is 150ppm and zero point drift is 0.1Hz/°C.

This circuit features extremely fast response to input changes, something most sine wave circuits cannot do. Figure 16 shows what happens when the input switches between two levels (Trace A). The circuit's output (Trace B) shifts frequency immediately, with no glitching or poor dynamics.

To adjust this circuit, put in 10.00V and trim the 2k pot for a symmetrical triangle output at A1. Next, put in 100 μ V and trim the 50k pot for triangle symmetry. Then, put in 10.00V again and trim the 5k "frequency trim" adjustment for a 100.0kHz output frequency. Finally, adjust the "distortion trim" potentiometers for minimum distortion as measured on a distortion analyzer (Trace D). Slight readjustment of the other potentiometers may be required to get lowest possible distortion.

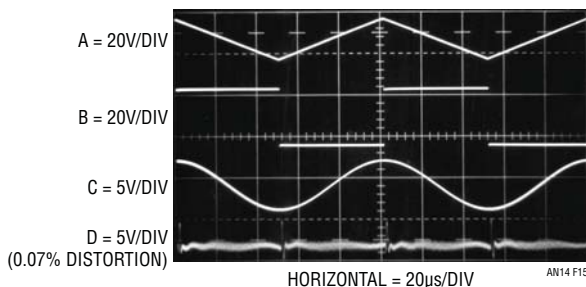


Figure 15. Sine Wave Output V→F Converter Waveforms

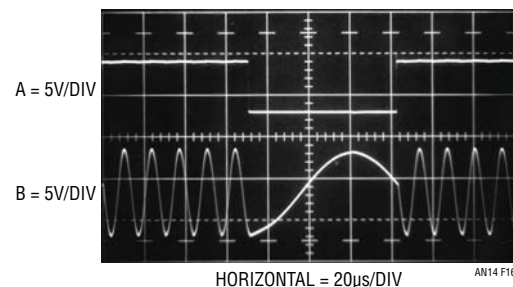


Figure 16. Sine Wave Output V→F Input Step Response

Application Note 14

1/X Transfer Function V→F Converters

Another dimension in V→F design is converters which have a deliberate nonlinear transfer function. Such converters are useful in linearizing outputs from transducers such as gas sensors and flow meters. Figure 17's circuit converts input voltages of 0V to 10V to an output frequency of 1kHz to 2Hz with a 0.05% accurate 1/X conformity.

A1 integrates current from the LT1009 2.5V reference. A1's negative output ramp (Trace A, Figure 18) is compared at C1 to the input voltage via a current summing network. When C1's input goes negative, its output (Trace B) falls, triggering the flip-flop (Trace C) Q output high. This turns on Q1, resetting the ramp. When the ramp reset gets very

near ground, C2 triggers low (Trace D), resetting the Q output low. This turns off Q1, allowing the ramp to begin again and the entire cycle repeats. Waveforms E, F, G and H are expanded versions of A through D, respectively, and show detail of the ramp resetting sequence.

In most V→F converters the input signal controls the integrator slope. Here the integrator runs at a fixed slope. The length of time the integrator requires to cross the input voltage is inversely proportional to the input's amplitude and loop oscillation is related by 1/X to the input. The ramp reset time is a first order error term because it is lost in the integration. At low frequencies the ramp reset time

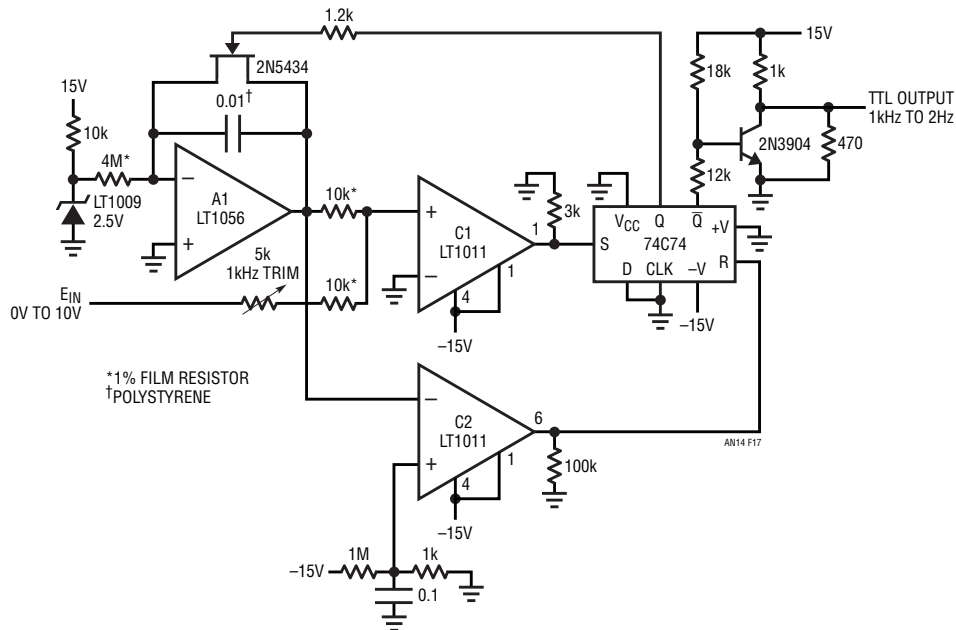


Figure 17. $\frac{1}{E_{IN}} \rightarrow$ Frequency Converter

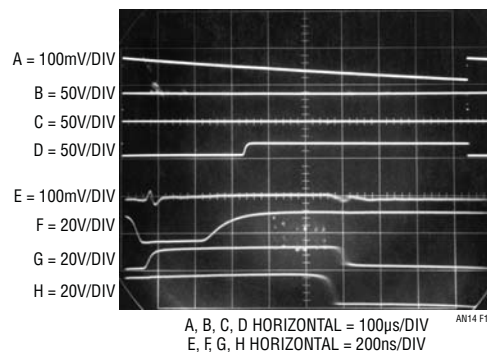


Figure 18. $\frac{1}{E_{IN}} \rightarrow$ Frequency Converter Waveforms

is a small term, even though reset takes longer (because the ramp had to run to a higher amplitude to cross the input). At higher frequencies, even though it is shorter, the reset period becomes significant because its "dead time" is a substantial percentage of the oscillation frequency. The 2-comparator flip-flop reset scheme reduces this error by adaptively controlling and minimizing the ramp reset time, regardless of peak ramp amplitude. A simple fixed AC feedback scheme would not do this because its time constant would have to be long enough to reset the ramp from large peak amplitudes (e.g., at low frequency). Even with this reset arrangement, the circuit's 0.05% 1/X

conformity can only be achieved by limiting maximum frequency to about 1kHz. It is worth noting that this circuit has almost ten times the accuracy of analog multipliers and other analog 1/X computing techniques. Circuit drift is about 150ppm/°C. To trim the circuit, put in 50mV and adjust the 5k potentiometer for 1kHz output.

Figure 19's 1/X V→F, developed by R. Essaff, provides better performance, although it is somewhat more complex. This charge pump class design gives 0.005% 1/X conformity, 50ppm/°C drift and 10kHz to 50Hz outputs for 0V to 5V in.

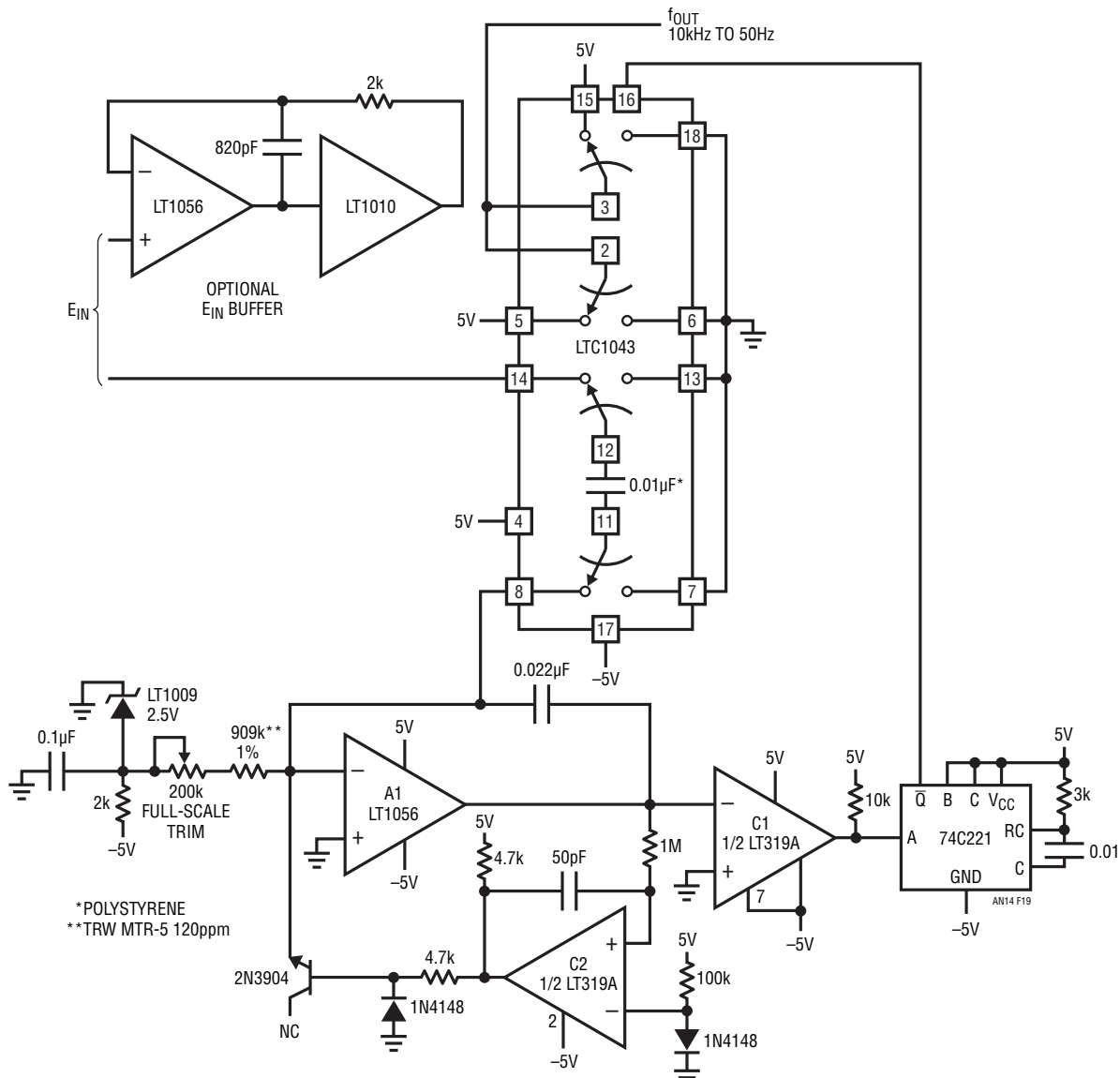


Figure 19. Charge Pump $\frac{1}{E_{IN}} \rightarrow$ Frequency Converter

an14f

Application Note 14

A1 and its associated components form an integrator which ramps positive (Trace A, Figure 20). When A1's output crosses zero, C1 goes negative (Trace B), triggering the one-shot. The one-shot output (Trace C) toggles the LTC1043 switch, transferring charge from E_{IN} to A1's summing point via the $0.01\mu\text{F}$ capacitor (Trace D). This forces A1's output negative by an amount related to the charge transferred. When charge transfer ceases, A1 again ramps positively. The depth of A1's negative excursion is directly proportional to E_{IN} , hence loop oscillation frequency is inversely (1/X) related to E_{IN} .

The circuit's output is taken from the paralleled LTC1043 switch sections.

Because this circuit relies on charge feedback, integrator reset time does not influence accuracy. The loop runs at whatever frequency is required to maintain A1's summing point at zero.

If A1's output ever overruns 0V, the oscillator loop will latch. This condition is detected by C2, which goes high, driving current into A1's summing point via the low leakage 2N3904 BE junction. A1's output is forced negative, and normal circuit operation commences.

This circuit's primary disadvantage is that the input signal must be capable of supplying substantial current each time the LTC1043 commutates the $0.01\mu\text{F}$ capacitor to A1's summing point. The current required varies directly with input voltage, with 25mA drawn at $E_{IN} = 5\text{V}$. The optional input buffer shown will provide the necessary drive, although input voltage range must fall within the buffer's common mode limits.

To calibrate this circuit, apply exactly 5V and trim the $200\text{k}\Omega$ potentiometer for 50Hz output.

E^X Transfer Function V→F Converter

Figure 21's V→F circuit responds exponentially to its input voltage. It is ideally suited to electronic music synthesizers and, as shown, has a 1V in/octave of frequency out scale factor. Exponential conformity is within 0.13% over a 10Hz to 20kHz range and drift is 150ppm/°C. The circuit has a pulse output and also provides a ramp output for applications which require substantial power at the fundamental frequency.

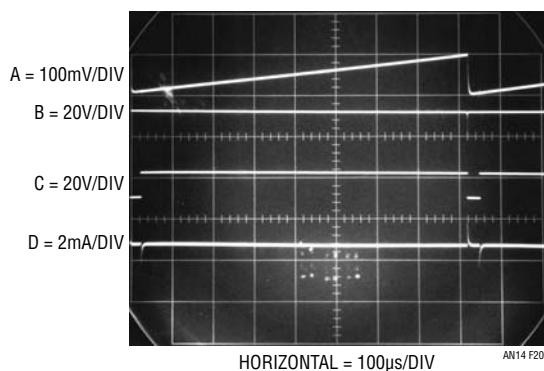


Figure 20. Charge Pump-Based $\frac{I}{E_{IN}} \rightarrow$ Frequency Converter Waveforms

A1's 1 μ F input capacitor integrates current from Q4's emitter, forming a ramp at A1's input (Trace A, Figure 22). When the ramp crosses zero, A1's output flips (Trace B, Figure 22), causing the LTC1043 to change states. The 0.0012 μ F capacitor, charged to the LT1021's 10V potential, is switched to pull current from A1's summing point (Trace C). The 30pF capacitor provides A1's positive input with positive AC feedback (Trace D), insuring enough time for a complete discharge of the 0.0012 μ F unit. This

action forces A1's input ramp to go in a negative direction, resetting it toward zero. When the positive AC feedback around A1 decays, the cycle repeats. Q5 and its associated components form a start-up loop, insuring proper circuit start sequence. Start-up conditions or input overdrive could force A1's output to go to the negative rail and stay there. If this occurs, Q5 comes on, pulling A1's negative input toward -15V and initializing normal circuit operation.

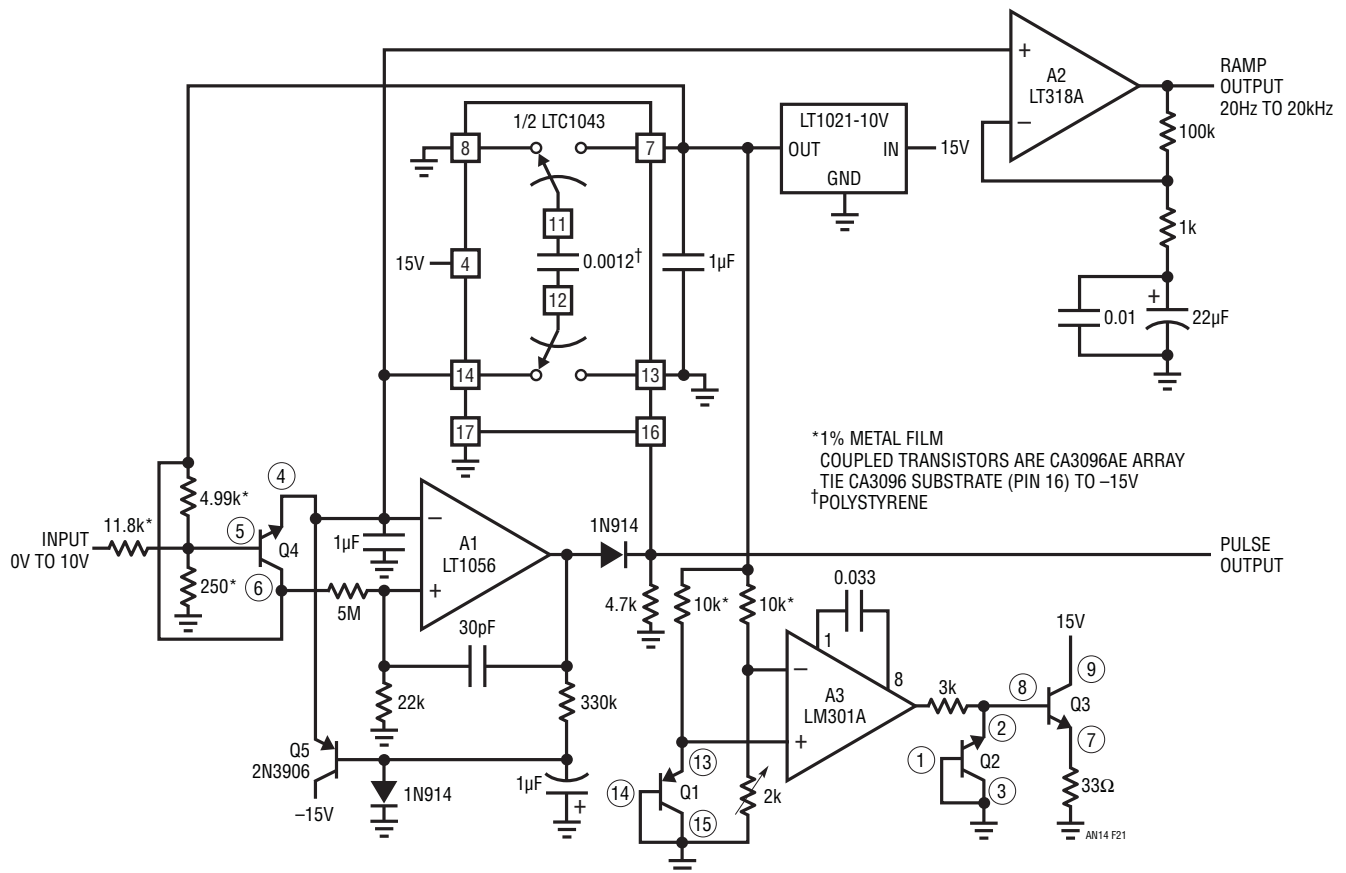


Figure 21. $E_{IN}^X \rightarrow$ Frequency Converter

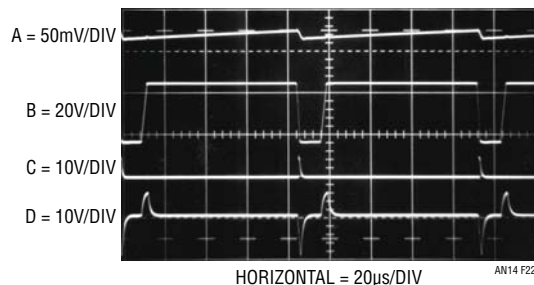


Figure 22. $E_{IN}^X \rightarrow$ Frequency Converter Waveforms

Application Note 14

The oscillation frequency of this charge pump class current-to-frequency converter is linearly related to Q4's emitter current. Q4's emitter current, in turn, is exponentially related to its V_{BE} , which is determined by the resistors connected to it and the input voltage. This is in accordance with the well-known relationship between collector current and V_{BE} in transistors. Normally Q4's operating point would be quite sensitive to temperature, but it is part of an array which is temperature-stabilized by the A3 configuration. Q1, also part of the array, senses temperature. A3 compares Q1's V_{BE} with a bridge potential and drives array transistor Q3 to close a thermal control loop. This stabilizes the array, preventing ambient temperature shifts from influencing Q4's operation. Q2, serving as a clamp, ensures against loop lock-up conditions and prevents Q3 from ever becoming reverse biased.

With the thermal loop controlling Q4, the circuit's exponential behavior is stable and repeatable. The $5M\Omega$ value from Q4's collector to A1's positive input introduces a slight shift in A1's operating point at high frequencies (e.g., high Q4 collector currents). This compensates Q4's bulk emitter resistance term, maintaining good exponential performance up to 20kHz. The 4.99k resistor sets the 0V input frequency at about 10Hz, while the 250Ω value establishes circuit k factor, nominally 1V/octave output, as shown.

To use this circuit, adjust the 2k potentiometer so that A3's negative input is 100mV below its positive input with Q3's base grounded. Next, underground Q3's base and the circuit is ready for use.

$$\frac{R1}{R2} = \frac{V1}{V2} \rightarrow \text{Frequency Converter}$$

Figure 23's circuit produces an output frequency proportional to the ratio of the voltages across two externally supplied resistors. This circuit has wide application in transducer signal conditioning. Both R1 and R2 are ground referred, preferable for noise considerations. In this case, R1 is a Platinum resistance sensor, with R2 being set at the sensor's 0°C value. The grounded end of R2 allows fine trimming with decade boxes without excessive noise problems. R1's grounded side allows it to be located at the end of a cable run, with similar noise rejection properties.

The 6012 DAC serves as a simple source of two identical currents. The DAC's MSB is set high and all other bits are low. This sets the DAC's output currents equal. With constant, equal, currents through them, R1 and R2 produce a differential voltage which is sampled by the LTC1043 switch-capacitor configuration. The LTC1043's internal clock continuously switches the 3900pF capacitor across the R1-R2 pair and then dumps the charge into A1's summing point. The quantity of charge delivered per cycle is a direct function of the voltage difference across R1 and R2 ($Q = CV$). A1's output ramps (Trace A, Figure 24) negative. The ramp is compared to A2's output at C1. A2's DC output is a function of the 330pF charge pump capacitor at the LTC1043, A2's feedback resistor and the LTC1043 clock frequency. Because A1 and A2 are receiving charge at the same rate, LTC1043 oscillator drift affects each equally and does not contribute error.

When A1's ramp crosses A2's output value, C1 goes high (Trace B), turning on the FET. AC positive feedback to C1's positive input (Trace C) ensures a complete discharge for A1's feedback capacitor. When the feedback ceases, the cycle repeats. The oscillation frequency is a linear function of the R1-R2 ratio.

The two polystyrene capacitors at the LTC1043 provide temperature coefficient cancellation. A2's specified feedback resistor compensates A1's polystyrene feedback capacitor. Overall circuit tempco is about 35ppm/°C. As shown, a 0°C to 100°C excursion at the R1 sensor gives a 0kHz to 1kHz output with an accuracy, limited by the sensor, of 0.35°C. This is well outside the dead time error produced by A1's reset time and the circuit contributes no appreciable measurement error. In practice, slight trimming of R2's value may be required to compensate for individual R1 tolerances at 0°. The 5k potentiometer trims for 1kHz out at a 100°C R1 temperature. This circuit may be used with any resistive based transducer. For negative tempco devices, reverse the positions of R1 and R2.

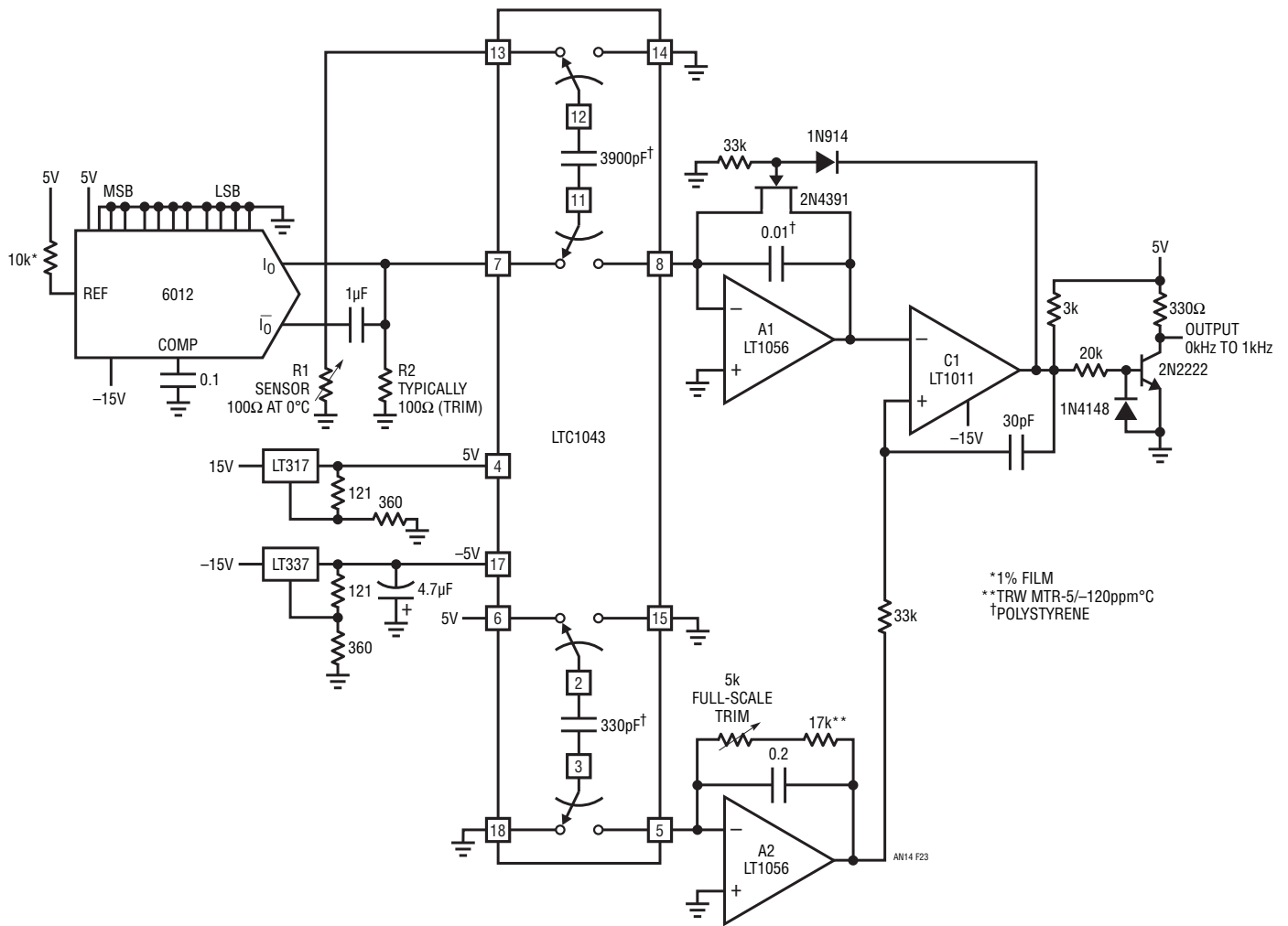


Figure 23. $\frac{R1}{R2} = \frac{V1}{V2}$ → Frequency Converter

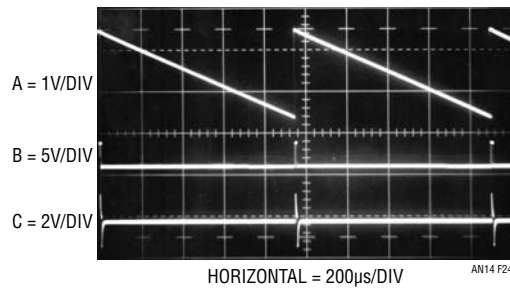


Figure 24. $\frac{R1}{R2} = \frac{V1}{V2}$ → Frequency Converter Waveforms

Application Note 14

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3. Pease R. A., assignee to Teledyne, "Amplitude to Frequency Converter," U.S. patent 3,746,968, filed September 1972.
4. Williams, J., "Low Cost A→D Conversion Uses Single-Slope Techniques," *EDN*, August 5, 1978, pages 101-104.
5. Gilbert B., "A Versatile Monolithic Voltage-to-Frequency Converter," *IEEE J. Solid State Circuits*, Volume SC-11, pages 852-864, December 1976.
6. Williams, J., "Applications Considerations and Circuits for a New Chopper Stabilized Op Amp," 1Hz-30MHz V→F, pages 14-15, Linear Technology Corporation, Application Note 9.

BOX SECTION

V→F Techniques

There are many ways to convert a voltage to a frequency. The best approach in an application varies with desired precision, speed, response time, dynamic range and other considerations. Figure B1 shows one of the most obvious. The input drives an integrator. The integrator's ramp slope varies with the input-derived current. When the ramp crosses V_{REF} , the comparator turns on the switch, discharging the capacitor and reinitializing the cycle. The frequency of this action directly relates to input voltage. With careful design, one op amp can serve as both integrator and comparator, providing circuit economy.

A serious drawback to this approach is the capacitor's discharge-reset time. This time, "lost" in the integration,

results in significant linearity error as operating frequency approaches it. For example, a 1 μ s reset interval introduces 0.1% error at 1kHz, rising to 1% at 10kHz. Also, variations in reset time contribute additional errors. Because of this, circuit operation is restricted to relatively low frequencies if good linearity and stability are required. Although various compensation methods can reduce these errors, performance is still limited.

Figure B2 gets around B1's problems by enclosing the integrator in a charge-dispensing loop. In this approach C1 charges to V_{REF} during the integrator's ramping time. When the comparator trips, C1 is discharged into A1's summing point, forcing its output high. After C1's discharge, A1 begins to ramp and the cycle repeats.

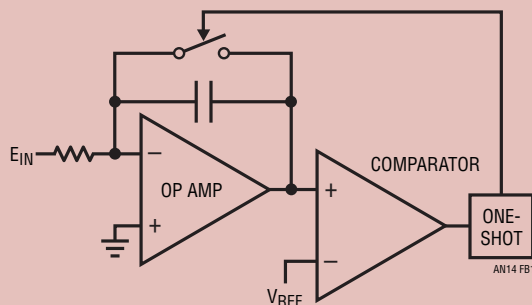


Figure B1. Ramp-Comparator V→F

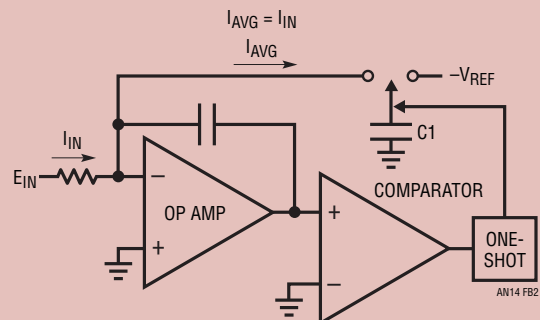


Figure B2. Charge Pump V→F

Because the loop acts to force the average summing currents to zero, integrator time constant and reset time do not affect frequency. This approach yields high linearity (typically 0.01%) up to high frequencies. With attention to design, converters of this type can be constructed with a single op amp.

Figure B3 is conceptually similar, except that it uses feedback current instead of charge to maintain the op amp's summing point. Each time the op amp's output trips the comparator, the current sink pulls current from the summing point. Current is pulled from the summing point for the timing reference's duration, forcing the integrator positive. At the end of the current sink's

period, the integrators output again heads negative. The frequency of this action is input-related.

Figure B4 uses DC loop correction. This arrangement offers all the advantages of charge and current balancing except that response time is slower. Additionally, it can achieve exceptionally high linearity (0.001%), output speeds exceeding 100MHz and very wide dynamic range (160dB). The DC amplifier controls a relatively crude V→F. This V→F is designed for high speed and wide dynamic range at the expense of linearity and thermal stability. The circuit's output switches a charge pump whose output, integrated to DC, is compared to the input voltage.

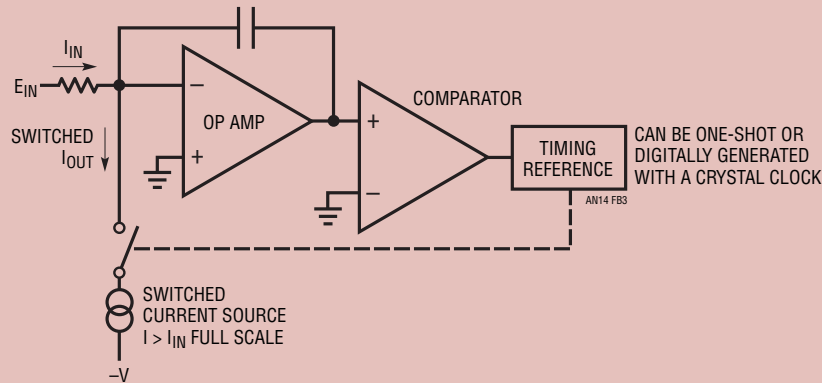


Figure B3. Current Balance V→F

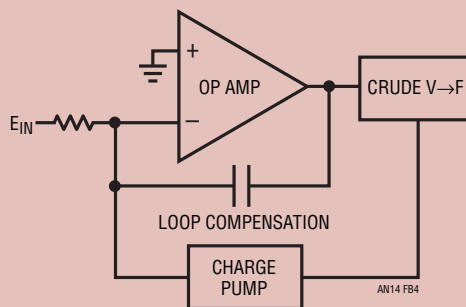


Figure B4. Loop-Charge Pump V→F

Application Note 14

The DC amplifier forces $V \rightarrow F$ operating frequency to be a direct function of input voltage. The DC amplifier's frequency compensation capacitor, required because of loop delays, limits loop response time. Figure B5 is similar, except that the charge pump is replaced by digital counters, a quartz time base and a DAC. Although it is not immediately obvious, this circuit's resolution is not restricted by the DAC's quantizing limitations. The

loop forces the DAC's LSB to oscillate around the ideal value. These oscillations are integrated to DC in the loop compensation capacitor. Hence, the circuit will track input shifts much smaller than a DAC LSB. Typically, a 12-bit DAC (4096 steps) will yield 1 part in 50,000 resolution. Circuit linearity, however, is set by the DAC's specification. An example of this approach appears in AN-13, "High Speed Comparator Techniques".

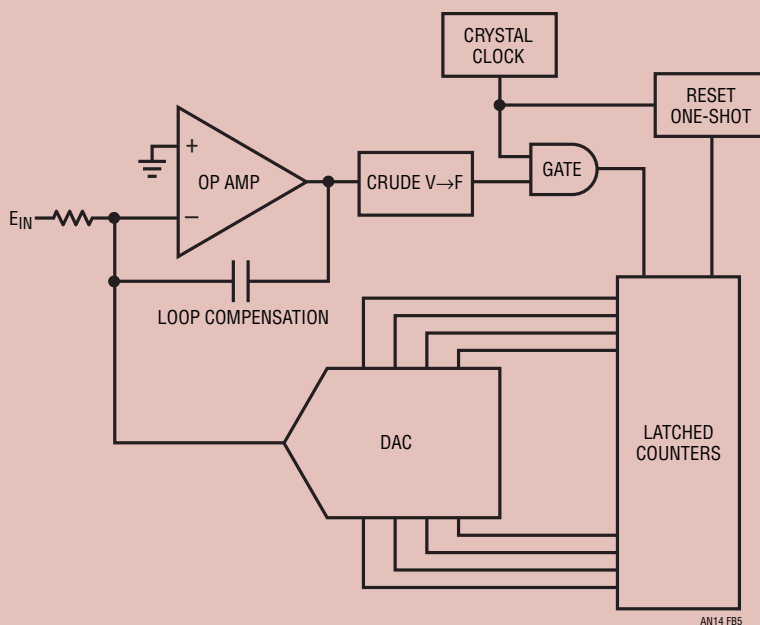


Figure B5. Loop-DAC $V \rightarrow F$

Application Note 15

The input voltage causes a positive going ramp at C1's positive input (Trace A, Figure 2). C1's output (Trace B) is low, biasing Q1 on. Q1's collector current drives the Q2-Q3 combination, forcing Q2's emitter (Trace C) to clamp at 1V. The 0.001 μ F capacitor charges to ground (0.001 μ F unit's current waveform is Trace D) via Q5. When the ramp at C1's positive input goes high enough, C1's output goes high, cutting off Q1, Q2 and Q3. Q4 conducts, pulling current from C1's positive input capacitor via Q6. This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output low. The 100pF capacitor at Q1's collector furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 0.001 μ F capacitor.

of Q5 and Q6, minimizing overall temperature drift. The 270k resistor path provides an input voltage derived trip point for C1, enhancing circuit linearity performance. This resistor should be selected to achieve the quoted linearity.

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback loop to latch. If this occurs, C1's output goes high. C2 detects this, via the 820k-0.22 μ F lag, and also goes high, lifting C1's negative input towards 1.5V. Because C1's positive input is diode clamped at 600mV, its output switches low, initiating normal circuit behavior.

To calibrate this circuit, select the 100k value for $V_{CLAMP} = 1V$. Next, apply 2.5mV at the input and select the resistor value indicated at C1's input for a 25Hz output. Then, put in exactly 1V and trim the 500k Ω potentiometer for 10kHz output.

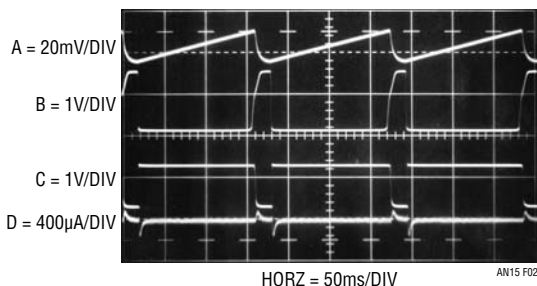


Figure 2. V \rightarrow F Operating Waveforms

The Schottky diode prevents C1's input from being driven outside its negative common mode limit. This action cuts off Q4, Q1-Q3 come on and the entire cycle repeats. The oscillation frequency directly depends on the input voltage derived current. The temperature coefficient of the Q2-Q3 1V clamp is largely compensated by the junction tempcos

10-Bit A/D Converter

Figure 3 is another data converter circuit. This integrating A/D converter has a 60ms conversion time, consumes 460 μ A from its 1.5V supply and maintains 10-bit accuracy over a 15 $^{\circ}$ C to 35 $^{\circ}$ C temperature range.

A pulse applied to the convert command line (Trace A, Figure 4) causes Q3, operating in inverted mode, to discharge the 1 μ F capacitor (Trace B). Simultaneously, Q4 is biased through the 10k diode path, forcing its collector (Trace D) low. Q3's inverted mode switching results in a capacitor discharge within 1mV of ground. When the convert command falls low, Q3 goes off, Q4's collector lifts, and the LT1004 stabilized Q1-Q2 current source

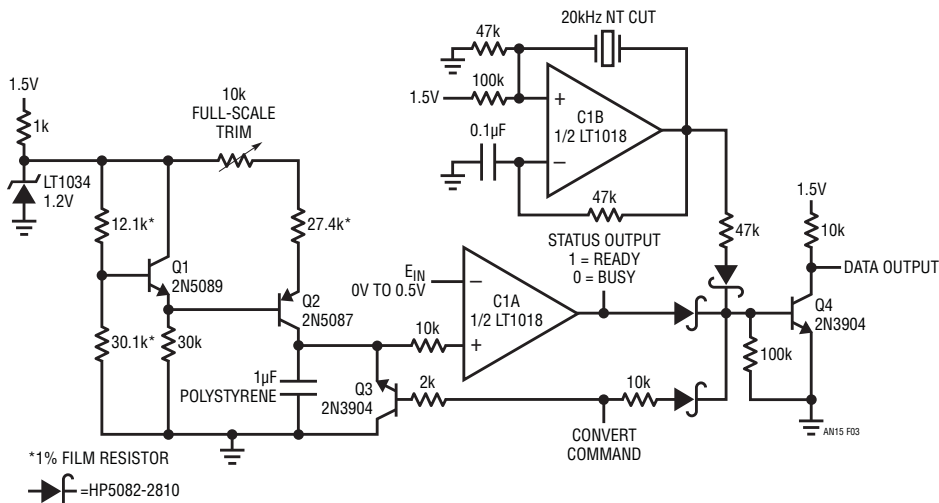


Figure 3. 10-Bit A/D Converter

charges the $1\mu\text{F}$ unit with a linear ramp. During the time the ramps value is below the input voltage, C1A's output is low (Trace C). This allows pulses from C1B, a quartz stabilized oscillator, to modulate Q4. Output data appears at Q4's collector (Trace D). When the ramp crosses the input voltages value C1A's output goes high, biasing Q4 and output data ceases. The number of pulses appearing at the output is directly proportional to the input voltage. To calibrate this circuit, apply 0.5000V to the input and trim the 10k potentiometer for exactly 1000 pulses out each time the convert command line is pulsed. No zero trim is required, although Q3's inverted 1mV saturation voltage limits zero resolution to 2 LSBs.

Sample-Hold Amplifier

A logical companion to the A/D converter described is a sample-and-hold amplifier. A sample-and-hold is one of the most difficult circuits to design for 1.5V operation, primarily because FET switches with low enough pinch-off voltages are not available. Two methods are presented

here. The first circuit gets around the switch problem with an approach that eliminates the switch. Although an unusual way to implement a sample-and-hold, it requires no special components or trimming, is easy to build and has a 4ms acquisition time to 0.1% . The second circuit, a more conventional design, requires specially selected and matched components and is more complex, but offers $125\mu\text{s}$ (0.1%) acquisition time—a $30\times$ improvement over the other design.

When a sample command (Figure 5, Trace A) is applied to the circuit of Figure 6, Q1, operating in inverting mode, discharges the $1\mu\text{F}$ capacitor (Trace C). When the sample command falls, Q1 goes off and C1A's internal output pull-up current source (Trace B) charges the capacitor via Q2, connected as a low leakage diode. The capacitor's charging ramp is followed by the LM10, which biases C1B's positive input. When the ramp potential crosses the circuit's input voltage, applied to C1B's negative input, C1B's output goes high (Trace D).

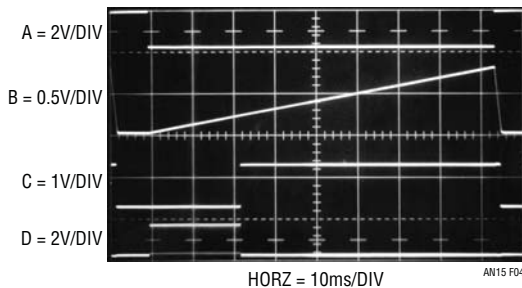


Figure 4. A/D Converter Waveforms

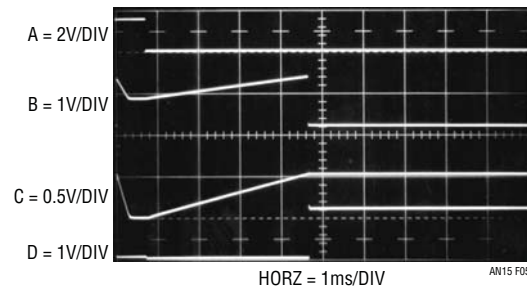


Figure 5. Sample-Hold Waveforms

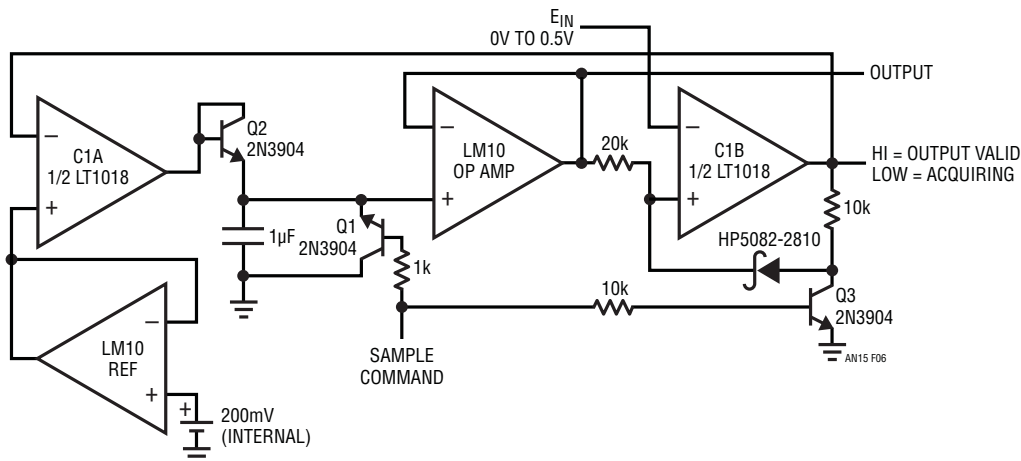


Figure 6. Sample-Hold Circuit

Application Note 15

This forces C1A's output low, and the 1 μ F capacitor stops charging. Under these conditions, the circuit is in the "hold" mode. The voltage the capacitor sits at is the same as the input voltage, and the circuit output is taken at the LM10. The 10k diode path at C1B provides a latch, preventing input voltage changes or noise from affecting the value stored in the 1 μ F capacitor. When the next sample command is received, Q3 breaks the latch and circuit action repeats.

Acquisition time is directly proportional to input value, with 4ms required for full-scale (0.5V). Although faster acquisition is possible, the delay in shutting off C1A's output will degrade accuracy. The circuit's primary advantages are elimination of the FET switch requirement and relative simplicity. Accuracy is 0.1%, droop rate specs at 10 μ V/ms and current consumption is 350 μ A.

Fast Sample-Hold Amplifier

Figure 7, a more conventional approach to sample-and-hold, is significantly faster, but also more complex and has special construction requirements. Q1 serves as the sample-and-hold switch, with Q6 and Q7 providing a level shift to drive the gate. To minimize power consumption, a 1500pF feedforward path is used for fast gate switching without resorting to high operating currents in Q6 and Q7. C1A, a simple

square wave oscillator, drives Q4. C1B inverts C1A's output and biases Q5. The transistors serve as synchronous switches and charge is pumped to the 2.2 μ F capacitor at Q5's collector, resulting in a negative potential there.

Q1's low pinch-off voltage is obtained at the expense of on-resistance. The typical R_{ON} of 1.5k to 2k means the circuit's hold capacitor must be small if fast acquisition is desired. This mandates a low bias current output amplifier, or droop rate will suffer. Q2, Q3 and A2 meet this need. Q2 and Q3 are set up as source followers, with the resistors used as level shifters to keep A2's inputs inside the LM10's common mode range. A2's output diode ensures clean dynamic performance for voltages close to zero by setting the LM10's output bias point well above ground. The 180pF capacitor compensates the composite amplifier.

Several special considerations are required to use this circuit. Q1, an extremely low pinch-off device, must be further selected for a pinch-off below 500mV to enable proper turn-off. Also, any V_{GS} mismatch between Q2 and Q3 will contribute offset error, and these devices must be selected for V_{GS} matching within 500 μ V. Additionally, the Q2-Q3 V_{GS} absolute value must be inside 500mV or A2 may encounter common mode limitations for circuit inputs near full-scale.

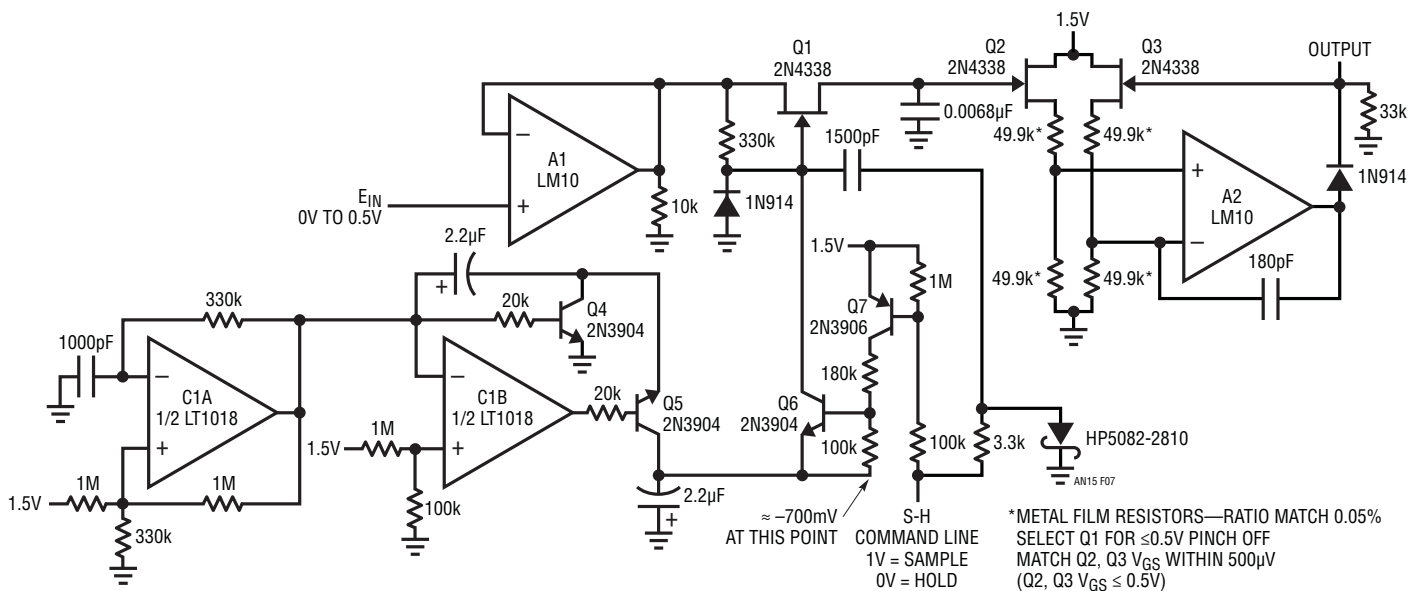


Figure 7. Fast Sample-Hold

Finally, mismatches in the resistor level shift contribute a gain error. To hold 0.1% circuit accuracy, the resistors should be ratio matched with 0.05%.

Once these special provisions have been attended to, the circuit delivers excellent specifications for a 1.5V powered sample-and-hold. Acquisition time is 125 μ s to 0.1% with a droop rate of 10 μ V/ms. Current consumption is inside 700 μ A.

Figure 8 shows the circuit acquiring a full-scale input. Trace A is the sample-and-hold command, while Trace B is the circuit's output. Trace C, an amplitude expanded version of B, shows acquisition detail. The input is acquired within 125 μ s and sample-to-hold offset is within a millivolt.

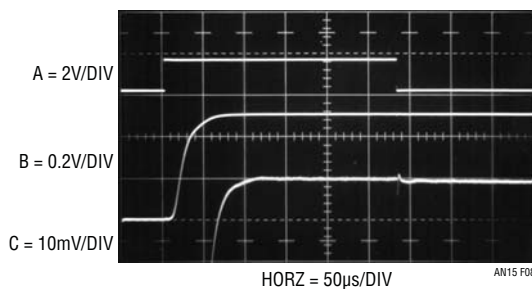


Figure 8. Fast Sample-and-Hold Waveforms

Temperature Compensated Crystal Clock

Many systems require a stable clock source and crystal oscillators which run from 1.5V are relatively easy to construct. However, if good stability over temperature is required, things become more difficult. Ovenizing the crystal is one approach, but power consumption is excessive. An alternate method provides open loop, frequency correcting bias to the oscillator. The bias value is determined by absolute temperature. In this fashion, the oscillator's thermal drift, which is repeatable, is corrected. The simplest way to do this is by slightly varying the crystal's resonance point with a variable shunt or series impedance. Varactor diodes, the capacitance of which varies with reverse voltage, are commonly employed for this purpose. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shift, making direct 1.5V powered operation impossible.

Figure 9's circuit accomplishes the temperature compensation function. The transistor and associated components form a Colpitts class oscillator which runs directly from the 1.5V supply. The varactor diode, in series with the crystal, tunes oscillator frequency as its DC bias varies. An ambient temperature dependent DC bias is generated by the remaining circuitry.

The thermistor network and the LM10 amplifier are arranged to produce a temperature dependent signal which corrects the thermal drift of the crystal type specified. Normally, the 1.5V powered LM10 could not provide the output levels required to bias the varactor. Here, however, a self-exciting switching up-converter (T1 and associated components) is included in the LM10's feedback loop. The LM10 drives the switching converter's input to generate whatever output voltage is required to close the loop. The thermistor-bridge network and amplifier feedback resistor values are scaled to produce appropriate temperature dependent varactor bias. The LM10's reference portion stabilizes the temperature network against 1.5V supply variations. The 100pF positive feedback forces the LM10's output into switched mode operation, conserving power.

Figure 10 plots compensated versus uncompensated oscillator drift. The compensation improves drift performance by more than a factor of ten. The residual aberrance in the compensated curve is due to the first-order linear correction used. Current consumption is inside 850 μ A.

Voltage Boosted Output Amplifier

In many circumstances, it is desirable to have 1.5V powered circuitry interface to higher voltage systems. The most obvious example is 1.5V driven, remote data acquisition apparatus which feeds a line-powered data gathering point. Although the battery-powered portion may locally process signals with 1.5V circuitry, it is useful to address the monitoring high level instrumentation at high voltage.

Figure 11's design borrows from the method used in Figure 9 to generate high voltage outputs. This 1.5V powered amplifier provides 0V to 10V outputs at up to 75 μ A capacity. The LM10 drives the self-exciting up-converter

Application Note 15

with whatever energy is required to close the feedback loop. In this case, the amplifier is set up with a gain of 101, although other gains are easily realized. The sole restriction is that the 1.5V powered LM10's common mode input range not be exceeded. The Schottky diode bypasses the up-converter for low voltage outputs, aiding output

noise performance. Overlap between the up-converter's turn-on threshold and the diode forward breakdown ensures clean dynamic behavior at the transition point. To increase efficiency the 0.033 μ F capacitor provides AC positive feedback, forcing the LM10 output to pulse-width modulate the up-converter.

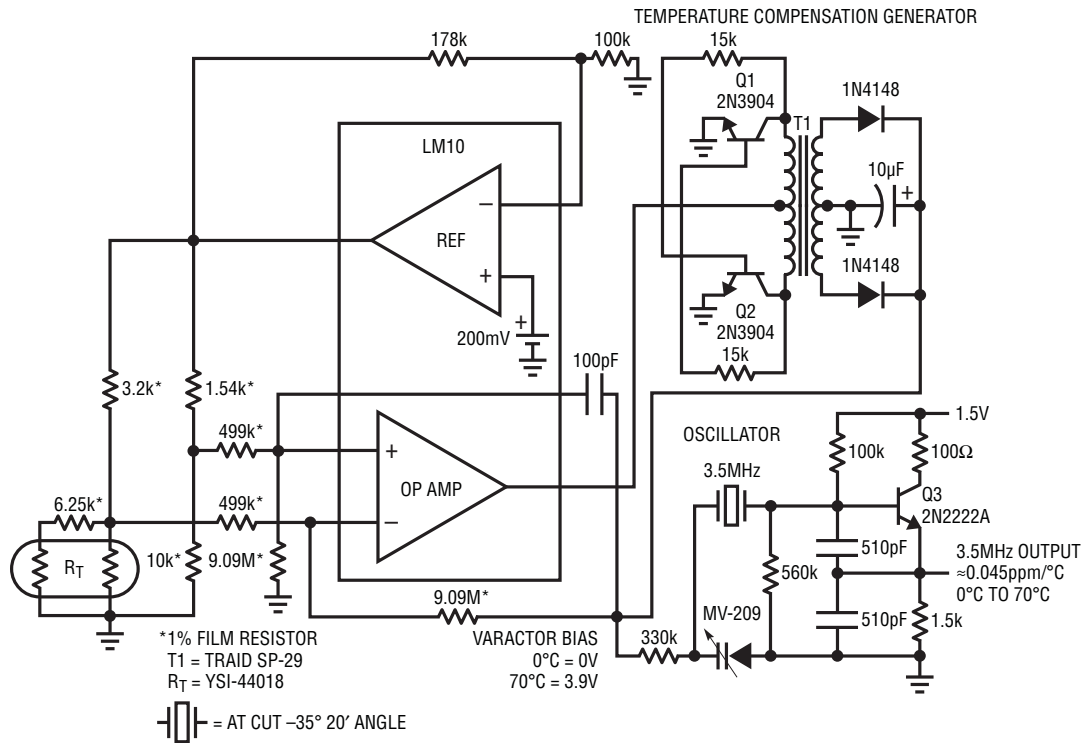


Figure 9. Temperature Compensated Crystal Oscillator

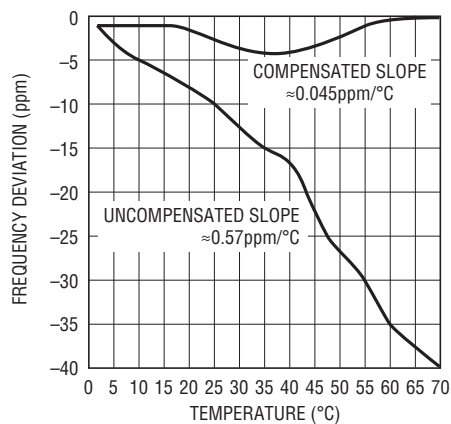


Figure 10. Compensated vs Uncompensated Oscillator Results

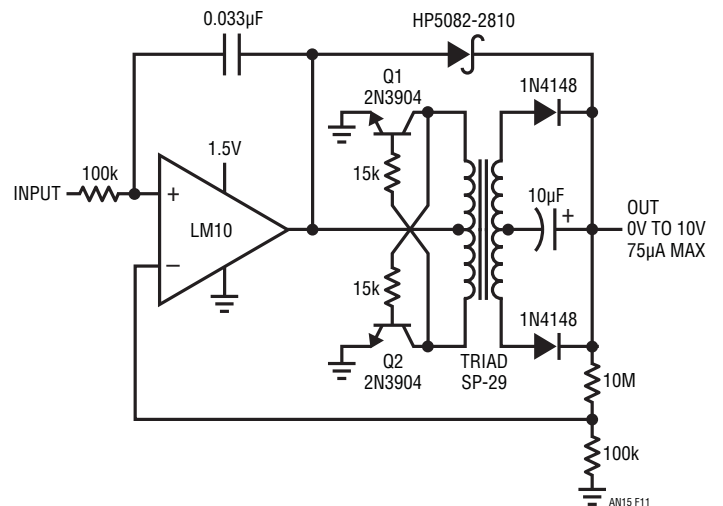


Figure 11. Voltage-Boosted Output Op Amp

Figure 12 details operation. The circuit's output (Trace A) decays until the LM10 switches (Trace B), starting the up converter. The two transistors alternately drive the transformer (transistor collectors are Traces C and D) until the output voltage rises high enough to shut off the LM10 output. This sequence repeats, with repetition rate dependent upon output voltage and loading conditions.

5V Output Switching Regulator

No commercially available logic, processor or memory family will operate from 1.5V. Many of the circuits described previously normally work in logic-driven systems. Because of this, a way to permit use of standard logic functions

from a 1.5V battery is necessary. The simplest way to do this is a switching regulator specifically designed for 1.5V input operation. Figure 13's flyback configuration, a variant of a design by R. J. Widlar, gives a 5V output. C1A serves as an oscillator, providing a ramp (Trace A, Figure 14) at C1B's DC-biased negative input. C1B compares a divided version of the output to a reference point derived from the LT1034. The ramp signal, summed with the reference point, causes C1B's output to width modulate (Trace B). During the time C1B is low, current builds in its output inductor (Trace C). When the ramp at C1B goes low enough, C1B's output goes high, and the inductor discharges into the 47 μ F capacitor. The diode

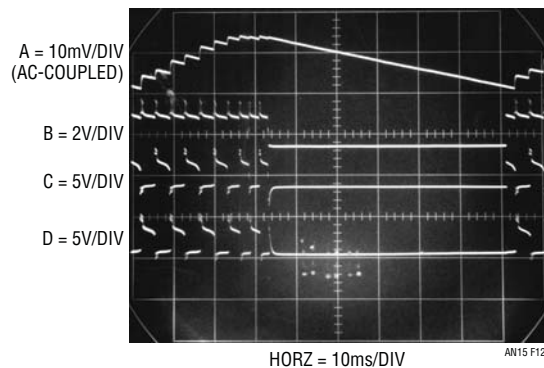


Figure 12. Boosted Op Amp Waveforms

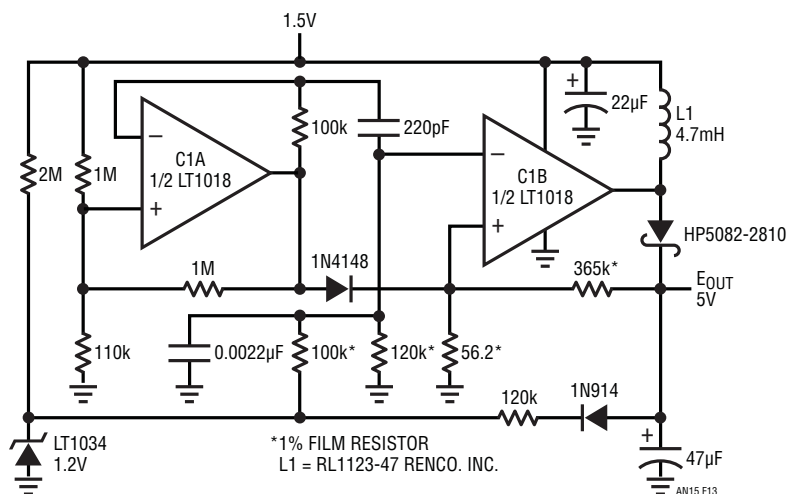


Figure 13. Flyback Regulator

Application Note 15

from C1A's output to C1B's positive input supplies a pulse (Trace D) on each oscillator cycle, ensuring loop start-up. The 120kΩ diode path from the output bootstraps LT1034 bias, aiding overall regulation.

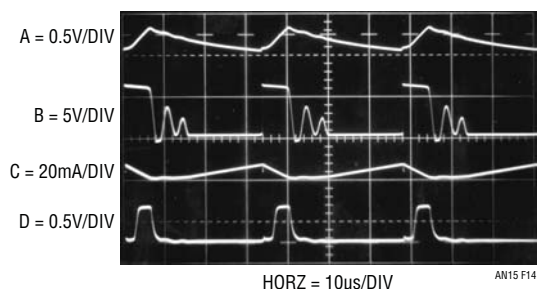


Figure 14. Flyback Regulator Waveforms

Figure 15 plots regulator efficiency. Small loads produce lowest efficiency because of fixed losses in the regulator, although 80% efficiency is achieved above 150µA.

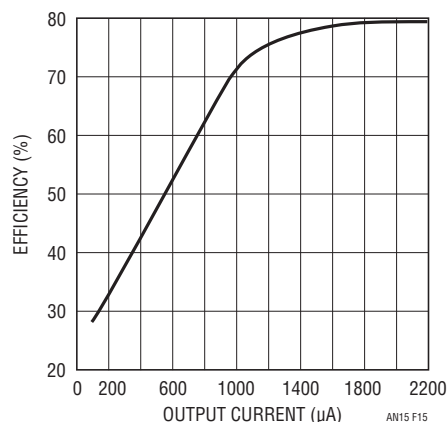


Figure 15. Flyback Regulator Efficiency

Components for 1.5V Operation

Almost all commercially available linear ICs are not capable of 1.5V operation. Two that are capable include the LM10 and LT1017/LT1018. The LM10 op amp-reference runs as low as 1.1V; the LT1017/LT1018 comparator goes down to 1.2V. The LM10 provides good DC input characteristics, although speed is limited to 0.1V/µs. The LT1017/LT1018 comparator series features microsecond range response time, high gain and good DC characteristics. Both devices feature low power consumption. The LT1004 and LT1034 voltage references feature 20µA operating currents and 1.2V operation.

Standard PN junction diodes have a 600mV drop, a substantial percentage of available supply range. At currents below 10µA to 20µA, this figure reduces to about 450mV. Schottky diodes typically exhibit only 300mV drop, although reverse leakage is higher than standard diodes. Germanium diodes are lowest, with 150mV to 200mV drop, even at relatively high currents. Often, though, the significant reverse leakage of Germanium precludes its use.

Standard silicon transistors have a 600mV V_{BE} , although this figure comes down somewhat at very low base currents. The V_{CE} saturation of silicon transistors is well below 100mV at reasonable currents, and judicious device selection and use can reduce this figure below 25mV. Inverted mode operation allows V_{CE} saturation losses

below 1mV, although beta is often below 0.1, necessitating substantial base drive. Germanium transistors have 2 to 3 times lower V_{BE} and V_{CE} losses, although speed, leakage and beta are generally not as good as silicon types.

Perhaps the most important component is the battery. Many types of cells are available, and the best choice varies with the application. Two common types are Carbon-Zinc and Mercury. Carbon-Zinc offers higher initial voltage, but Mercury units have a much flatter discharge curve (e.g., better supply regulation) if currents are controlled (see Figure 16).

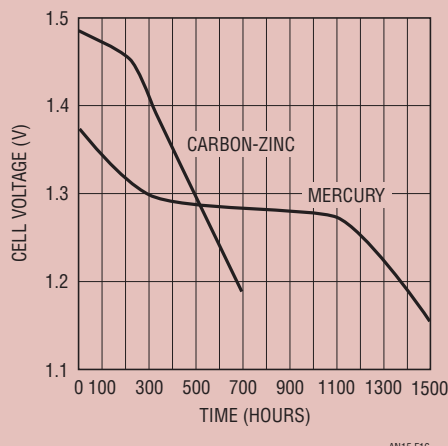


Figure 16. Typical Discharge Curves of Similar Size (AA) Mercury and Carbon Zinc Cells (1mA Load)

Considerations for Successive Approximation A → D Converters

Jim Williams

The most popular A → D method employed today is the successive approximation register (SAR) converter (see Box, "The Successive Approximation Technique"). Numerous monolithic, hybrid and modular devices embodying the successive approximation technique are available, and monolithic devices are slowly gaining in performance. Nevertheless, hybrid and modular SAR types feature the best performance. In particular, at the 12-bit level, the fastest monolithic devices currently available require about 10 μ s to convert. Modular and hybrid units achieve

conversion speeds below 2 μ s, although they are quite expensive. Because of these factors, it is often desirable to build, rather than buy, a high speed 12-bit SAR converter. Even in cases where high speed is not required, lower cost may still mandate building the circuit instead of using a monolithic device.

Figure 1 shows a simple 12-bit, 12 μ s SAR converter. Understanding this circuit's performance limitations is useful in

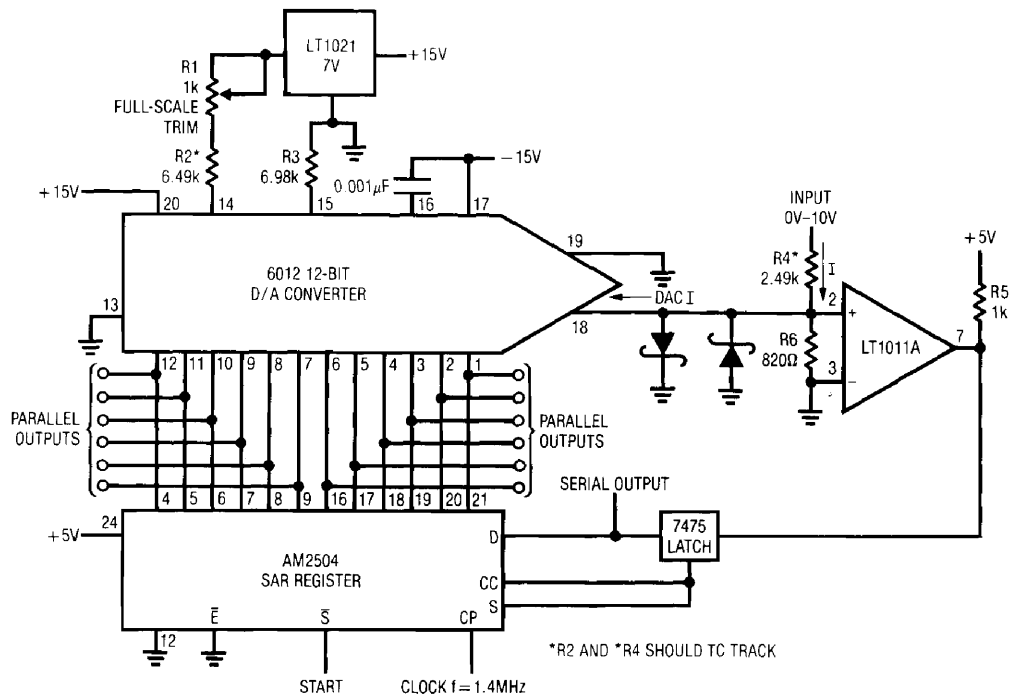


Figure 1. Basic 12-Bit, 12 μ s Successive Approximation A → D Converter

Application Note 17

designing faster converters. Figure 2 shows waveforms of operation. Trace A is the clock, which is applied to the 2504 IC successive approximation register (SAR), while Trace B is the start pulse. On the rising edge of the start pulse, the SAR-DAC combination begins to test each bit, beginning with the MSB. This action is reflected in conditions at the LT1011's positive input (Trace C). This waveform is seen to sequentially converge towards zero as the SAR, DAC and comparator servo the node. After the LSB has been converted the "conversion complete" (CC) line (Trace D) goes high, signaling the end of the sequence. The 7475 latch prevents the comparator from responding to input noise or shifts after the conversion is complete. It is reset at the next "conversion command". The major limitations on speed in this circuit are the DAC and the comparator. Most bipolar DACs require 150–200ns to settle for a worst-case (full-scale) step and the comparator's delay time must also be accounted for. The clamp diodes limit overdrive, aiding comparator response. Additionally, the 820 Ω resistor to ground shunts the DAC's output capacitance, helping the comparator-DAC node settle more quickly. The shunt degrades the voltage per-LSB available to the comparator, but the LT1011's high gain makes up for this.

In general, this is a fairly typical 12-bit SAR converter with good speed and low cost. To get higher conversion speed requires more sophisticated circuitry.

Figure 3 shows a circuit which uses a clock modulation scheme to decrease conversion time. The A \rightarrow D is identical to Figure 1's circuit, but the clock terminal (CP) is driven by a 2 speed oscillator. Figure 4 shows operating details. A convert command pulse (Trace A) initiates the SAR routine. Simultaneously, the 7474 flip-flop's Q output is set high (Trace C), biasing Q1. This causes the 47pF capacitor to be paralleled with the 33pF unit. These capacitors are part of the timing network of C1, which is configured as an oscillator. C1's output pulses (Trace B) drive the SAR's clock terminal ("CP" in the schematic). After the third MSB has been converted, the flip-flop is reset (Trace C). Q1 goes off and the clock oscillator (Trace B) speeds up. The increase in clock speed results in less dwell time per bit at the DAC-comparator junction (Trace D), allowing faster total conversion time. Trace E, the conversion complete pulse ("CC"), drops low 7.5 μ s after the conversion started.

This clock modulation approach buys significantly improved speed, but does nothing to get around the comparator's contribution to delay. Minimizing comparator delay would seem to be as simple as using a faster device. At the 8 or even 10-bit level this usually works, but 12-bit performance raises problems. Replacing the LT1011, a 150ns device, with a 10ns LT1016 increases speed, but decreases available gain. The LT1011 has a minimum gain of

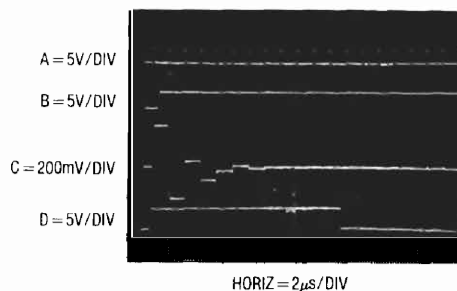


Figure 2. 12 μ s A \rightarrow D Waveforms

200,000. The LT1016's high speed sacrifices gain. Minimum gain for this device is 1400. For a 10V full-scale A → D, the LSB size is given by:

$$\frac{10V}{4096 \text{ steps}} = 2.44\text{mV/LSB}$$

To switch a full TTL output level with 1/2 LSB overdrive (1.22mV), the comparator must have a minimum gain of:

$$\frac{5V}{1.22\text{mV}} = 4,098.$$

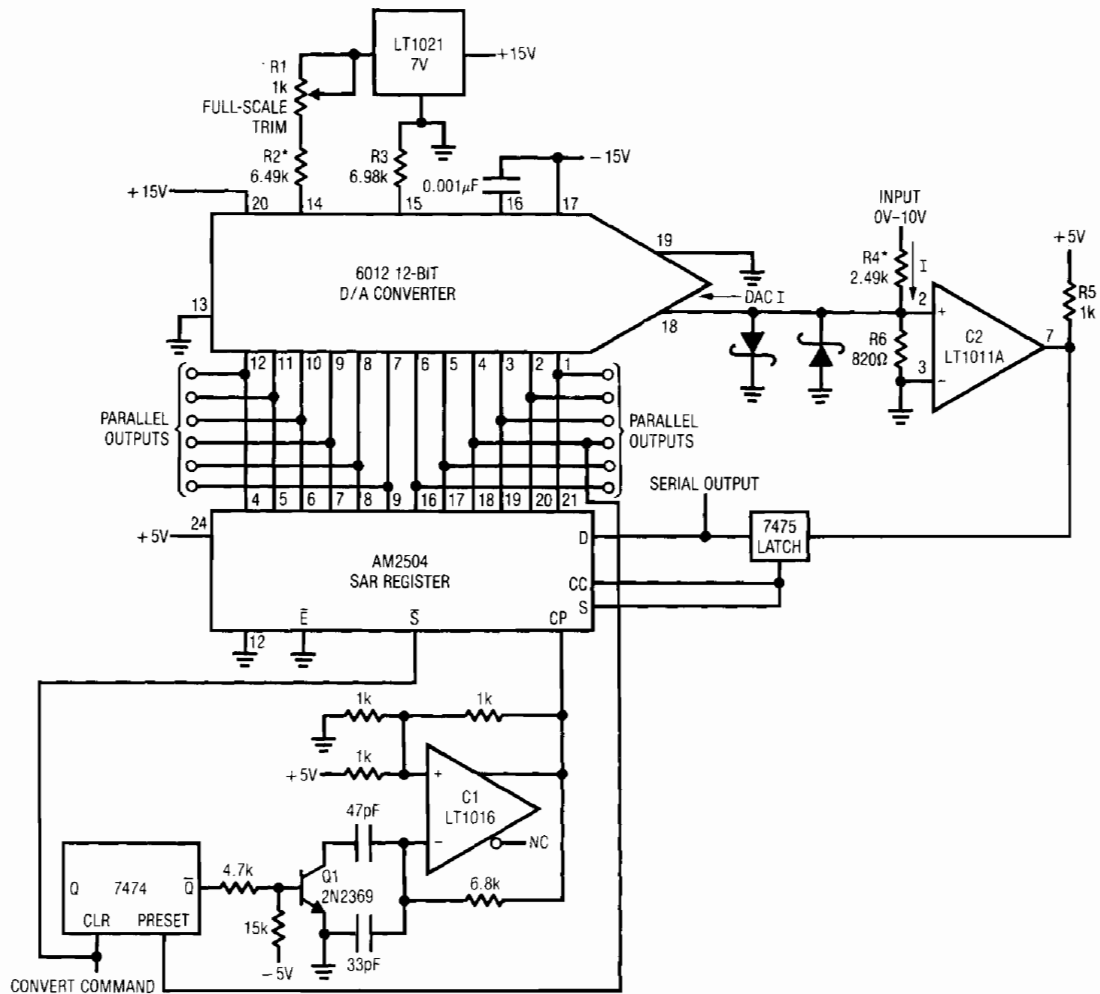
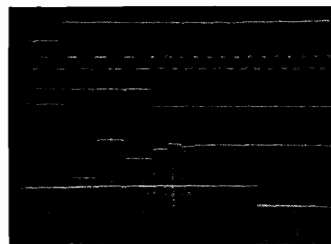


Figure 3. 7.5µs A-D Using a 2 Speed Clock

A = 5V/DIV
 B = 10V/DIV
 C = 10V/DIV
 D = 200mV/DIV
 E = 5V/DIV



HORIZ = 1µs/DIV

Figure 4. Figure 3's Waveforms

Application Note 17

This figure clearly means the comparator cannot do the job without some help. The input signal reduction caused by the shunt resistor at the DAC output worsens the problem. Finally, the comparator's speed degrades for such low level overdrives.

The solution to the aforementioned difficulties is to place a gain stage ahead of the comparator. While the gain stage adds some delay, it also increases gain, providing the needed overdrive to the comparator.

Figure 5 shows a simple pre-amplifier. This pre-amp-comparator combination gives adequate gain and an overall response time of 40-50ns. A1 is set up as a Schottky bounded amplifier. The bound diodes prevent A1 from saturating due to excessive summing point overdrive, aid-

ing response time. The 10pF capacitor, a typical value, compensates DAC output capacitance and is selected for best amplifier damping. The 10k feedback resistor, also typical, is chosen for best gain-bandwidth performance. Voltage gains of 4 to 10 are common. Figure 6 shows performance. Trace A, a test input pulse, causes A1's output (Trace B) to slew through zero (screen center horizontal line). When A1 crosses zero, C1's input biases negative and it responds (C1's output is Trace C) 10ns later with a TTL output.

A simple circuit like this results in faster comparisons. Substituted for the LT1011 in Figure 3's circuit, it permits conversion times in the 3-5 μ s range. Further reduction in conversion time is possible with a faster discrete preamplifier.

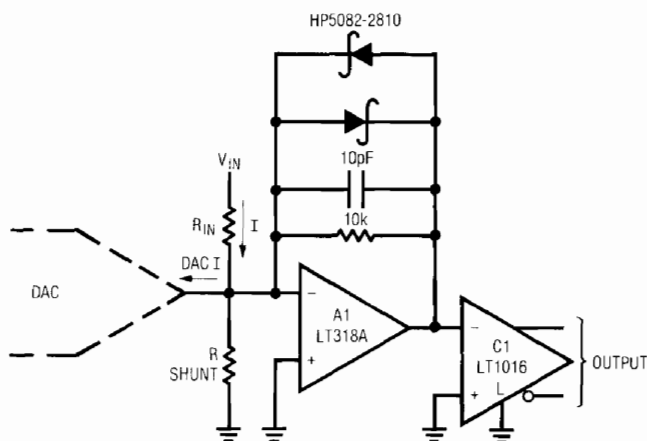


Figure 5. Simple Pre-Amplifier for the Comparator

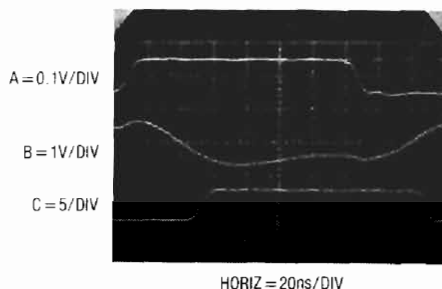


Figure 6. Pre-Amplified Comparator Waveforms

Figure 7 shows a very fast pre-amplifier built with GHz range transistors. This cascoded differential amplifier is placed ahead of C1, an LT1016. Q4 and Q5 provide bias current compensation for Q1's base current. Figure 8

shows results for a test input signal (Trace A). C1's output (Trace B) switches in 15-20ns. About 10ns of this delay is due to C1, with the pre-amplifier contributing the rest.

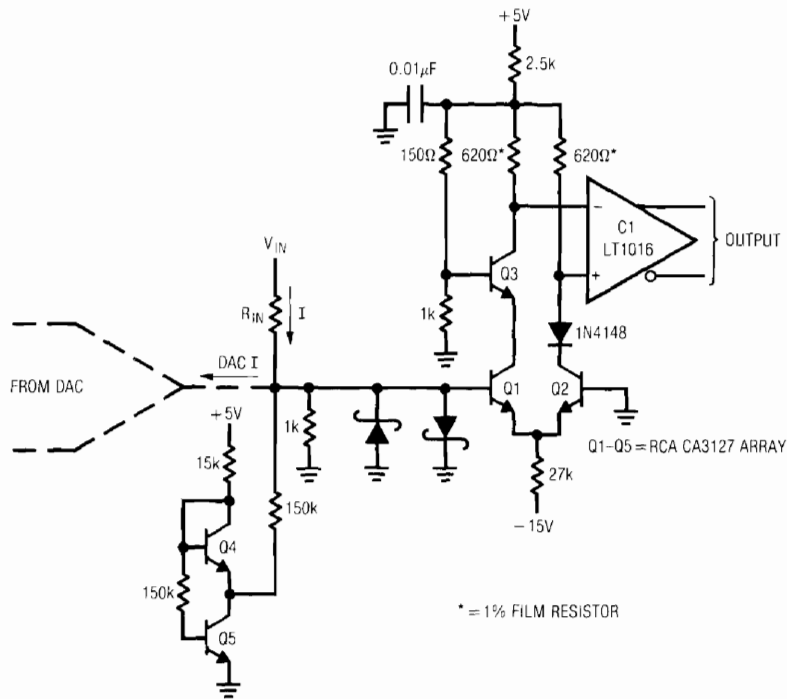


Figure 7. Fast Pre-Amplifier-Comparator

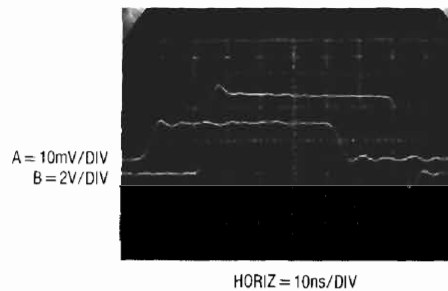


Figure 8. Fast Pre-Amp-Comparator Waveforms

Application Note 17

Figure 9 shows the discrete pre-amplifier used in a very fast 12-bit SAR converter. The design utilizes a variety of techniques to attain extremely high speed. Primary speed enhancing features include a closed loop clock control

method and active summing node clamping. The circuit achieves a full 12-bit conversion in 1.8 μ s, about the practical limit with off-the-shelf components.

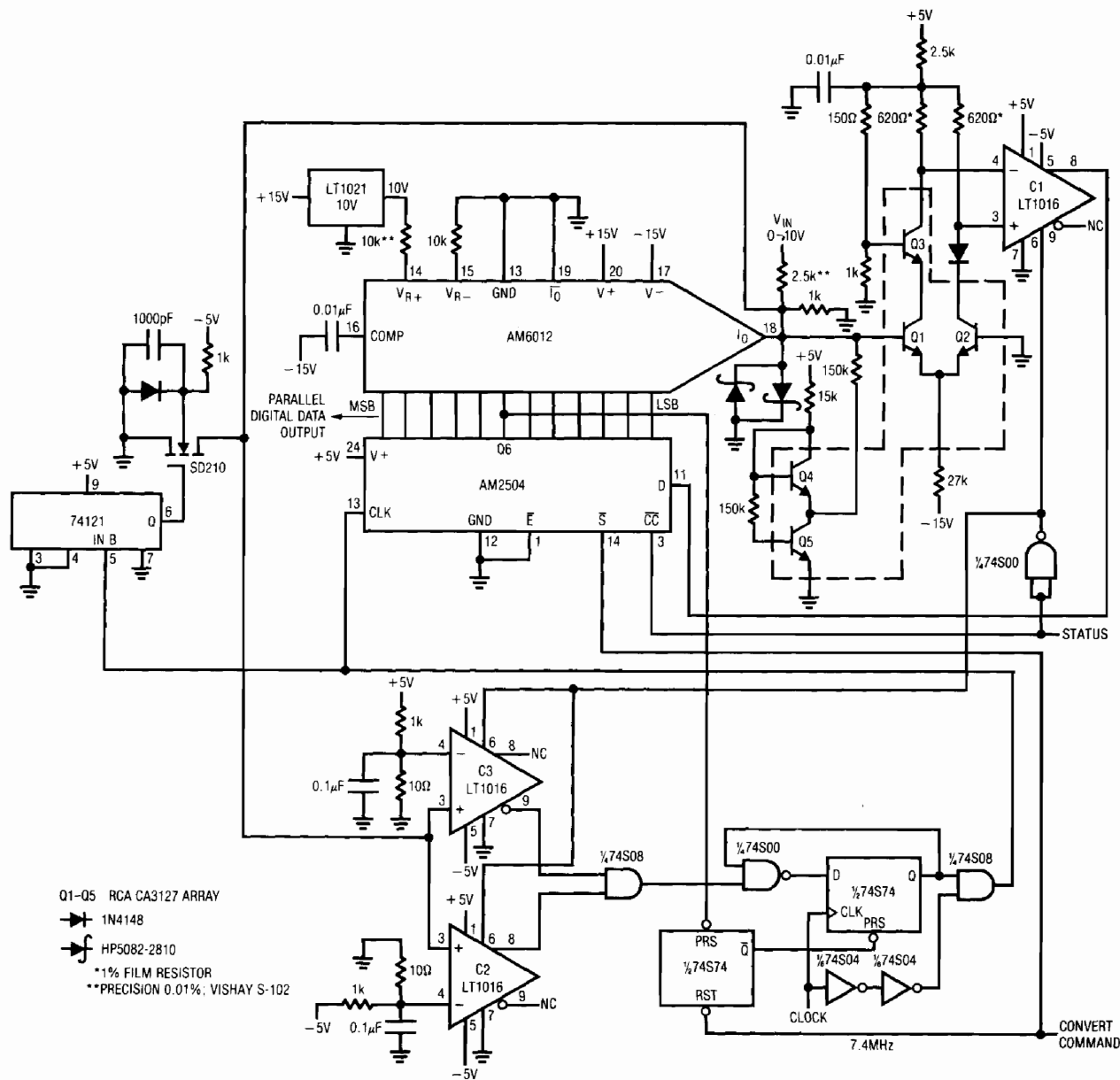


Figure 9. 12-Bit 1.8 μ s SAR A→D

The design is similar in concept to Figure 3, except that the fast pre-amplifier replaces the LT1011. Additionally, the clock speed change is implemented with the digital logic shown. Unlike before, the clock rate is accelerated after the fifth MSB is converted. During conversion of the upper four bits, the clock rate is controlled by a closed loop to maximize overall speed. The loop monitors conditions at the DAC-comparator summing node. If the node is outside $\pm 50\text{mV}$, the SAR is clocked at the maximum rate. For node responses inside $\pm 50\text{mV}$, the clock rate is retarded, giving adequate time for settling. The clock loop speeds conversion by not waiting for bits which aren't going to settle within $\pm 50\text{mV}$. C2 and C3 form a high speed window comparator which delivers summing node information in digital form to the clock logic.

Figure 10 shows the effects of the closed loop clocking scheme. Trace A is the convert command. Trace B is the gated output of the C2-C3 window comparator. Trace B's state controls the clock line, which is Trace C. Trace D is the summing point, and the dwell time-per-bit is controlled by the window comparator's decision. Beyond the fifth bit, the SAR's Q6 line instructs the clock logic to run at maximum speed. As described to this point, the circuit achieves a $1.9\mu\text{s}$ conversion time.

If the 74121 one-shot and associated circuitry are included, conversion time is reduced to $1.8\mu\text{s}$. These

components form an active clamp at the DAC-comparator summing node. Each time the SAR clock is pulsed (Trace A, Figure 11), the 74121 puts out a 30ns FET gate pulse (Trace B). The FET comes on, shunting the summing node (Trace C) to ground. The FET's low on resistance aids DAC settling by discharging the DACs 30pF output capacitance for 30ns . The summing node (Trace C) is reset to zero by this action at each SAR-directed step. When the one shot times out, the node settles to its final value. This active clamping results in about a 10ns -per-bit time savings.

This circuit's $1.8\mu\text{s}$ conversion time is very close to what is practically achievable for a 12-bit SAR A \rightarrow D converter. The special techniques used result in an effective DAC settling time of about 100ns per bit. Comparator-pre-amp delay is about 20ns per bit and SAR chip delays are in the 25ns per bit range. Adding these together gives; $(100\text{ns} + 20\text{ns} + 25\text{ns} \times 12 = 1.74\mu\text{s})$. The comparator and SAR delays, about 31% of the total, are not easily reduced. A discrete Schottky SAR design and a faster pre-amp can cut this figure somewhat, but the DAC settling time, 69% of the total, remains. The effective $100\text{ns}/\text{bit}$ DAC settling time compares favorably with published specifications for monolithic DACs, and is not readily reducible. Beyond this speed, other conversion methods are required.

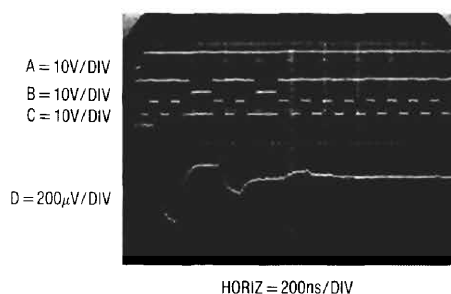


Figure 10. Figure 9's Waveforms

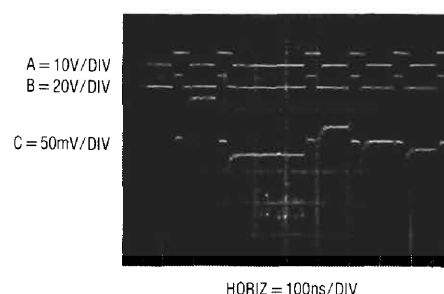


Figure 11. Figure 9's Waveforms Using Active Clamping

The Successive Approximation Technique

The successive approximation technique is probably as old as the first crude weighing scale ever constructed. It is most easily visualized when considering the operation of a beam balance. The unknown weight, in one pan, is determined by successive trials with standard weights placed in the other pan. Overweight-underweight decisions are made by the balance as standard weights (and combinations of them) are successively tried in a logical sequence which converges towards balancing the scale.

Successive approximation A → D converters start with the MSB and proceed toward the LSB as each under-over decision is made. The figure shows the summing node response (Trace A) as the DAC, instructed by the clock driven (Trace B) successive approximation register (SAR) logic, tries different bit weights. The comparator's decisions are also shown (Trace C). Note how the summing point sequentially converges towards zero, the analog of null in a beam balance.

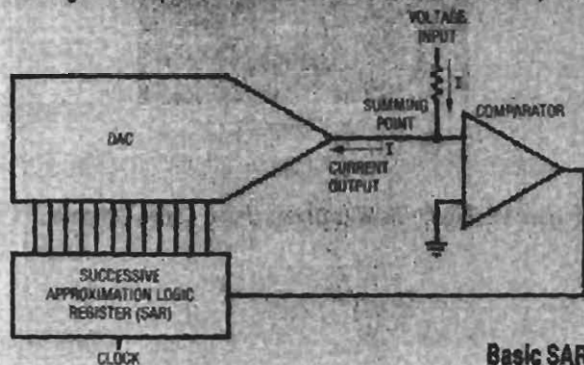
Digital to Analog Converters in SAR Applications

Selecting a DAC for use in an SAR-based A → D requires some thought. Most often, bipolar current mode DACs are employed because of their higher speed. CMOS DACs output capacitance, in the 100-150pF range, causes excessive summing node settling times. Monolithic bipolar types, in the 30pF region, settle more quickly. Voltage mode output DACs are almost never used because they are not necessary to achieve summing action and they are substantially slower than current output types.

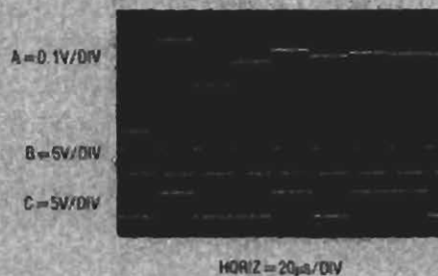
Speed is often important, and since the DAC is the slowest part of the converter, it should be carefully considered. Settling time specifications for DACs are usually stated

for full-scale transitions. Smaller bit changes take less time, so some interpretation of the full-scale settling time number can be made when considering the DACs effective settling time-per-bit in an A → D application. Unfortunately, the complex dynamics of DAC internals prevent simple straight line calculations (e.g., 1 LSB will not settle in 1/12 the time of full-scale for a 12-bit unit). At moderate speeds, the simplest course is to allow the specified full-scale settling time for each bit decision. This conservative method will never get you into trouble, but almost certainly guarantees slower than necessary DAC performance. The best way to find out just how far you can push the DACs settling time specifications in an SAR application is to consult the manufacturer. Additionally, it is worthwhile to actually measure the settling time under conditions appropriate to the intended use (see LTC Application Note 10, "Methods for Measuring Op Amp Settling Time", for circuits readily adaptable to DAC settling time measurements). The wide variety of DACs and individual output termination requirements make obtainable results vary considerably. However, some guidelines on what to expect are possible. For example, the popular 565A type, specified at 250ns full-scale settling time into 0Ω, can achieve 110-150ns effective settling time-per-bit in SAR applications with careful design. It is also worth noting that the dynamics of DAC types can vary considerably between manufacturers of what is nominally the same part.

Speed is not the only concern. The DACs DC specifications translate directly into A → D error terms. Linearity, drift, accuracy and other DC terms contribute on a 1:1 basis to the A → D's error characteristics. One specification, monotonicity, can contribute a particularly nasty term. The effect of a non-monotonic DAC is an inability of the A → D to produce some output codes ("missing codes") under any input condition.



Basic SAR Circuit and Waveforms



Power Gain Stages for Monolithic Amplifiers

Jim Williams

Most monolithic amplifiers cannot supply more than a few hundred milliwatts of output power. Standard IC processing techniques set device supply levels at 36V, limiting available output swing. Additionally, supplying currents beyond tens of milliamperes requires large output transistors and causes undesirable IC power dissipation.

Many applications, however, require greater output power than most monolithic amplifiers will deliver. When voltage or current gain (or both) is needed, a separate output stage is necessary. The power gain stage, sometimes called a “booster”, is usually placed within the monolithic amplifier’s feedback loop, preserving the IC’s low drift and stable gain characteristics.

Because the output stage resides in the amplifier’s feedback path, loop stability is a concern. The output stage’s gain and AC characteristics must be considered if good dynamic performance is to be achieved. Overall circuit phase shift, frequency response and dynamic load handling capabilities are issues that cannot be ignored when designing a power gain stage for a monolithic amplifier. The output stage’s added gain and phase shift can cause poor AC response or outright oscillation. Judicious application of frequency compensation methods is needed for good results (see box section, “The Oscillation Problem”).

The type of circuitry used in an output stage varies with the application, which can be quite diverse. Current and voltage boosting are common requirements, although both are often simultaneously required. Voltage gain stages are usually associated with the need for high voltage power supplies, but output stages which inherently generate such high voltages are an alternative.

A simple, easily used current booster is a good place to begin a study of power gain stages.

150mA Output Stage

Figure 1a shows the LT[®]1010 monolithic 150mA current booster placed within the feedback loop of a fast FET amplifier. At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_f , so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

Small-signal bandwidth is reduced by C_f , but considerable load isolation can be obtained without reducing it below the power bandwidth. Often a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

The LT1010 is particularly adept at driving large capacitive loads, such as cables.

The follower configuration (Figure 1b) is unique in that capacitive load isolation is obtained without a reduction in small-signal bandwidth, although the output impedance of the buffer has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over 0.3 μ F.

Figure 1c shows LT1010s used in a bridge type differential output stage. This permits increased voltage swing across the load, although the load must float.

All of these circuits will deliver 150mA of output current. The LT1010 supplies short-circuit and thermal overload protection. Slew limit is set by the op amp used.

High Current Booster

Figure 2 uses a discrete stage to get 3A output capacity. The configuration shown provides a clean, quick way to increase LT1010 output power. It is useful for high current loads, such as linear actuator coils in disk drives.

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Application Note 18

The 33Ω resistors sense the LT1010's supply current, with the grounded 100Ω resistor supplying a load for the LT1010. The voltage drop across the 33Ω resistors biases Q1 and Q2. Another 100Ω value closes a local feedback

loop, stabilizing the output stage. Feedback to the LT1056 control amplifier is via the 10k value. Q3 and Q4, sensing across the 0.18Ω units, furnish current limiting at about 3.3A.

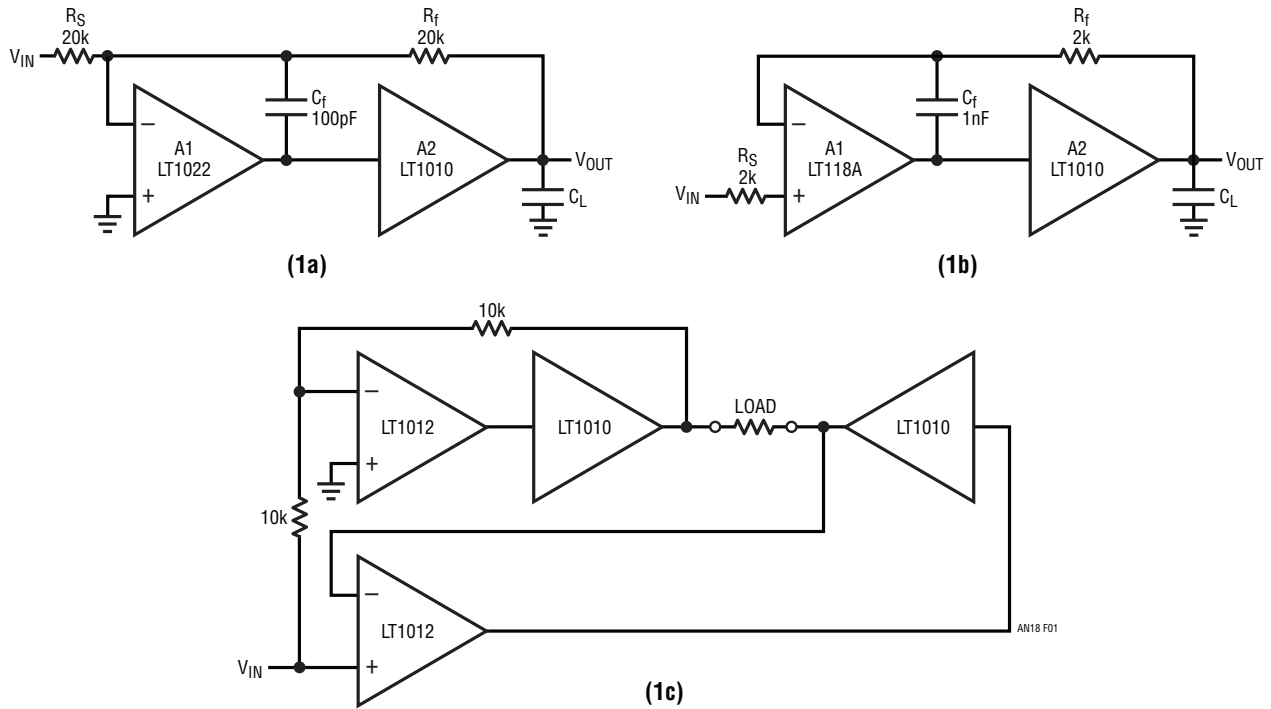


Figure 1. LT1010 Output Stages

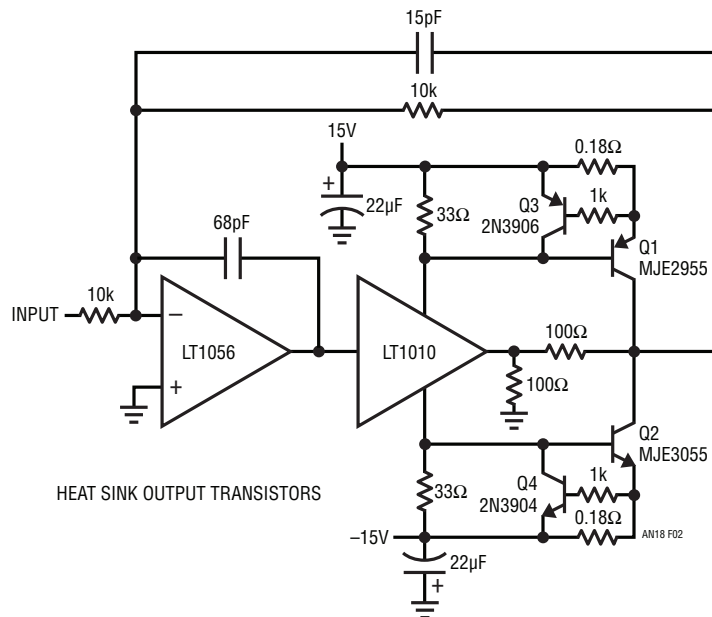


Figure 2. LT1010 Based Output Stage

The output transistors have low F_T , and no special frequency compensation considerations are required. The LT1056 is rolled off by the 68pF capacitor for dynamic stability, and the 15pF feedback capacitor trims edge response. At full power ($\pm 10V$, 3A peaks), bandwidth is 100kHz and slew rate about 10V/ μs .

Ultrafast™ Fed—Forward Current Booster

The previous circuits place the output stage booster within the op amp's feedback loop. Although this ensures low drift and gain stability, the op amp's response limits speed. Figure 3 shows a very wideband current boost stage. The LT1012 corrects DC errors in the booster stage, and does not see high frequency signals. Fast signals are fed directly to the stage via Q5 and the 0.01 μF coupling capacitors. DC and low frequency signals drive the stage via the op amp's output. This parallel path approach allows very broadband performance without sacrificing the DC stability of the op amp. Thus, the LT1012's output is effectively current and speed boosted. The output stage consists of current sources Q1 and Q2 driving the Q3-Q5 and Q4-Q7

complementary emitter followers. The transistors specified have F_T 's approaching 1GHz, resulting in a very fast stage. The diode network at the output steers drive away from the transistor bases when output current exceeds 250mA, providing fast short-circuit protection. Net inversion in the stage means the feedback must return to the LT1012's positive input. The circuit's high frequency summing node is the junction of the 1k and 10k resistors at the LT1012. The 10k-39pF pair filters high frequencies, permitting accurate DC summation at the LT1012's positive input. The low frequency roll-off of the fast stage is matched to the high frequency characteristics of the LT1012 section, minimizing aberration in the circuit's AC response. The 8pF feedback capacitor is selected to optimize settling characteristics at the highest speeds.

This current boosted amplifier features a slew rate in excess of 1000V/ μs , a full-power bandwidth of 7.5MHz and a 3dB point of 14MHz. Figure 4 shows the circuit driving a 10V pulse into a 50 Ω load. Trace A is the input and Trace B is the output.

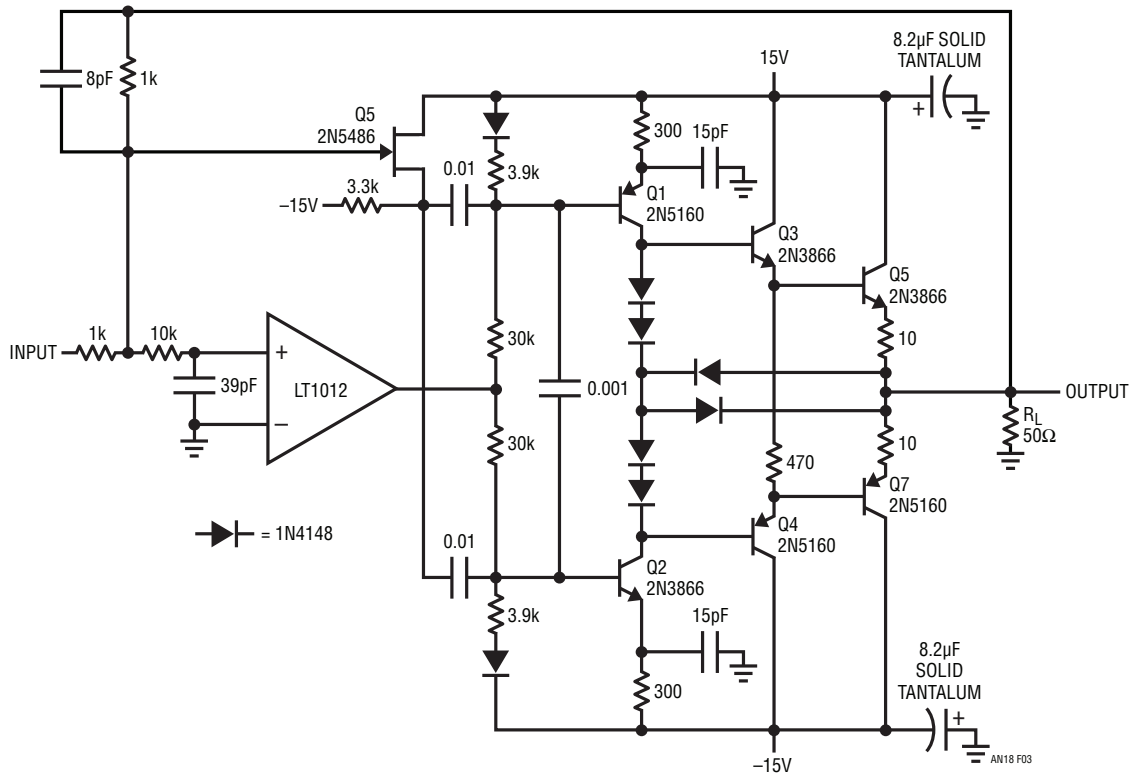


Figure 3. Fed-Forward Wideband Current Booster

Application Note 18

Slew and settling characteristics are quick and clean, with pulse fidelity approaching the quality of the input pulse generator. Note that this circuit relies on summing action, and cannot be used in the noninverting mode.

Simple Voltage Gain Stages

Voltage gain is another type of output stage. A form of voltage gain stage is one that allows output swing very near the supply rails. Figure 5a utilizes the resistive nature of the complementary outputs of a CMOS logic inverter to make such a stage. Although this is an unusual application for a logic inverter, it is a simple, inexpensive way to extend an amplifier's output swing to the supply rails. This circuit is

particularly useful in 5V powered analog systems, where improvements in available output swing are desirable to maximize signal processing range.

The paralleled logic inverters are placed within the LT1013's feedback loop. The paralleling drops output resistance, aiding swing capability. The inversion in the loop requires the feedback connection to go to the amplifier's positive input. An RC damper eliminates oscillation in the inverter stage, which has high gain bandwidth when running in its linear region. Local capacitive feedback at the amplifier gives loop compensation. The table provided shows that output swing is quite close to the positive rail, particularly at loads below several milliamperes.

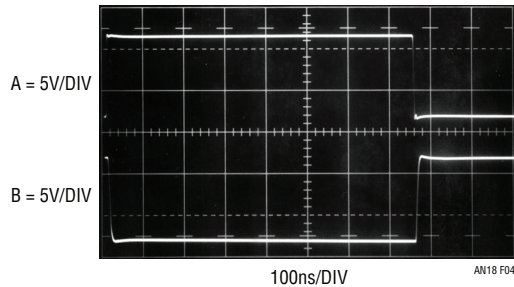


Figure 4. Figure 3's Response. Slew Rate Exceeds 1000V/ μ s at 10V Into 50 Ω

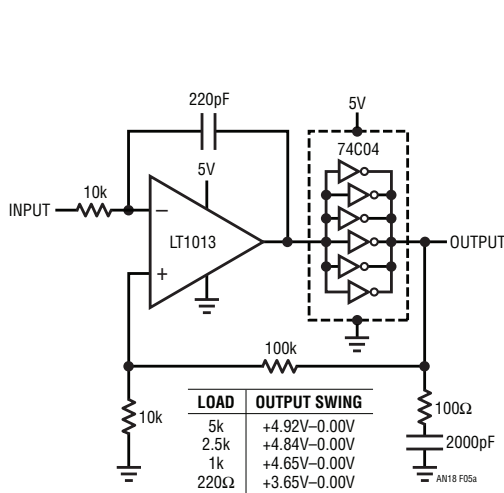


Figure 5a. CMOS Inverter-Based Output Stage with Voltage Gain

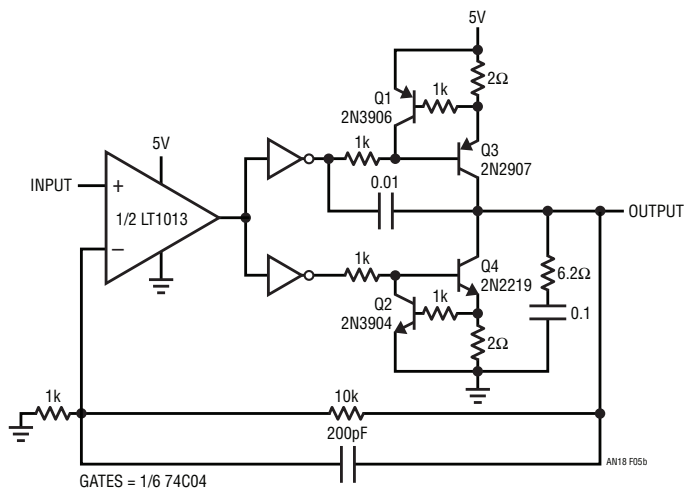


Figure 5b. Common Emitter Output Stage with Voltage Gain

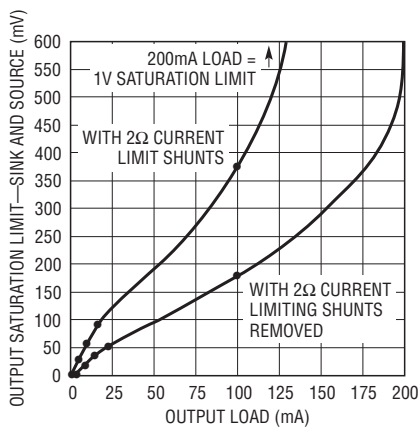
Figure 5b is similar, except that the CMOS inverters drive bipolar transistors to reduce saturation losses, even at relatively high currents. Figure 6a shows Figure 5b's output saturation characteristics. Note the extremely low saturation limits below 25mA. Removing the current limit circuitry permits even better performance, particularly at high output currents.

Figure 6b shows waveforms of operation for circuit Figure 5a. The LT1013's output (Trace B) servos around the 74C04's switching threshold (about 1/2 supply voltage) as it controls the circuit's output (Trace A). This allows

the amplifier to operate well within its output swing range while controlling a circuit output with nearly rail-to-rail capability.

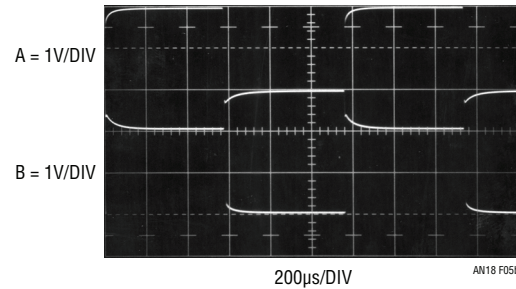
High Current Rail-to-Rail Output Stage

Figure 7 is another rail-to-rail output stage, but features higher output current and voltage capability. The stage's voltage gain and low saturation losses allow it to swing nearly to the rails while simultaneously supplying current gain.



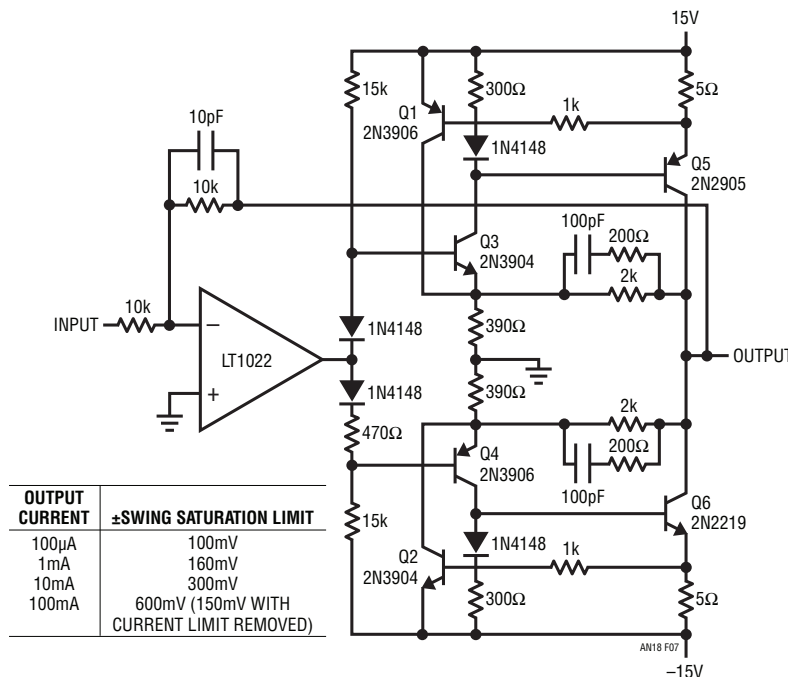
AN18 F06a

Figure 6a. Figure 5b's Saturation Characteristics



AN18 F05b

Figure 6b. Figure 5a's Waveforms



AN18 F07

Figure 7. Complementary Closed-Loop Common Emitter Stages Provide High Current and Good Saturation Performance

Application Note 18

Q3 and Q4, driven from the op amp, provide complementary voltage gain to output transistors Q5-Q6. In most amplifiers, the output transistors run as emitter followers, furnishing current gain. Their V_{BE} drop, combined with voltage swing limitations of the driving stage, introduces the swing restrictions characteristic of such stages. Here, Q5 and Q6 run common emitter, providing additional voltage gain and eliminating V_{BE} drops as a concern. The voltage inversion of these devices combines with the drive stage inversion to yield overall noninverting operation. Feedback is to the LT1022's negative input. The 2k-390 Ω local feedback loop associated with each side of the booster limits stage gain to about 5. This is necessary for stability. The gain bandwidth available through the Q3-Q5 and Q4-Q6 connections is quite high, and not readily controllable. The local feedback reduces the gain bandwidth, prompting stage stability. The 100pF-200 Ω damper across each 2k feedback resistor provides heavy gain attenuation at very high frequencies, eliminating parasitic local loop oscillations in the 50MHz to 100MHz range. Q1 and Q2, sensing across the 5 Ω shunts, furnish 125mA current limiting. Current flow above 125mA causes the appropriate transistor to come on, shutting off the Q3-Q4 driver stage.

Even with the feedback enforced gain-bandwidth limiting, the stage is quite fast. AC performance is close to the amplifier used to control the stage. Using the LT1022, full-power bandwidth is 600kHz and slew rate exceeds 23V/ μ s under 100mA output loading. The chart in the figure shows output swing versus loading. Note that, at high current, output swing is primarily limited by the 5 Ω current sense resistors, which may be removed. Figure 8 shows response to a bipolar input pulse for 25mA loading. The output swings nearly to the rails, with clean dynamics and good speed.

$\pm 120V$ Output Stage

Figure 9 is another voltage gain output stage. Instead of minimizing saturation losses, it provides high voltage outputs from a $\pm 15V$ powered amplifier. Q1 and Q2 furnish voltage gain, and feed the Q3-Q4 emitter follower outputs. $\pm 15V$ power for the LT1055 control amplifier is derived from the high voltage supplies via the Zener diodes. Q5 and Q6 set current limit at 25mA by diverting output drive when voltages across the 27 Ω shunts become too high. The local 1M-50k feedback pairs set stage gain at 20, allowing $\pm 10V$ LT1055 drives to cause full $\pm 120V$ output swing. As in Figure 7, the local feedback reduces stage gain bandwidth, making dynamic control easier. This stage is relatively simple to frequency compensate because only Q1 and Q2 contribute voltage gain. Additionally, the high voltage transistors have large junctions, resulting in low F_t 's, and no special high frequency roll-off precautions are needed. Because the stage inverts, feedback is returned to the LT1055's positive input. Frequency compensation is achieved by rolling off the LT1055 with the local 100pF-10k pair. The 33pF capacitor in the feedback peaks edge response and is not required for stability. Full power bandwidth is 15kHz with a slew limit of about 20V/ μ s. As shown, the circuit operates in inverting mode, although noninverting operation is possible by exchanging the input and ground assignments at the LT1055's input. Under noninverting conditions, the LT1055's input common mode voltage limits must be observed, setting the minimum noninverting gain at 11. If over compensation is required, it is preferable to increase the 100pF value, instead of increasing the 33pF loop feedback capacitor. This prevents excessive high voltage energy from coupling to the LT1055's inputs during slew. If it is necessary to increase the feedback capacitor, the summing point should

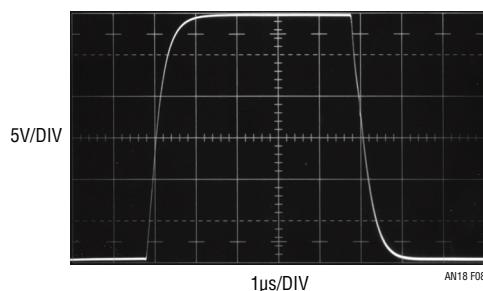


Figure 8. Figure 7 Drives $\pm 14.85V$ Into a 100mA Load

be diode clamped to ground or to the LT1055 supply terminals. Figure 10 shows results with a $\pm 12\text{V}$ input pulse

(Trace A). The output (Trace B) responds with a cleanly damped 240V peak-to-peak pulse.

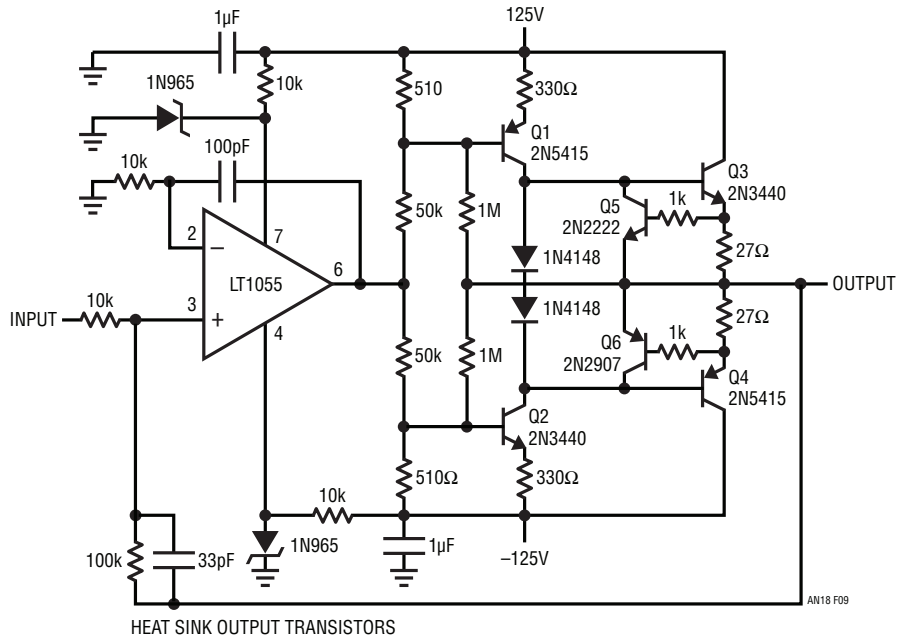


Figure 9. $\pm 120\text{V}$ Output Stage. DANGER! High Voltages Present. Use Caution

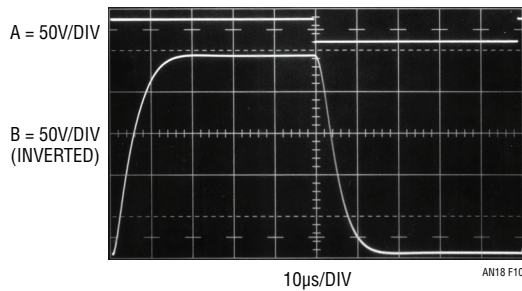


Figure 10. Figure 9 Swinging $\pm 120\text{V}$ Into $6\text{k}\Omega$. DANGER! High Voltages Present. Use Caution

Application Note 18

Figure 11 is a similar stage, except that Figure 9's output transistors are replaced with vacuum tubes. Most of this stage is conceptually identical to Figure 9, but major changes are needed to get the vacuum tube output to swing negatively. Positive swing is readily achieved by simply replacing Figure 9's NPN emitter follower with a cathode follower (V1A). Negative outputs require PNP Q3 to drive a Zener biased common cathode configuration. The transistor inverter is necessitated because our thermionic friends have no equivalent to PNP transistors. Zener biasing of V1B's cathode allows Q3's swing to cut off the tube, a depletion mode device.

Without correction, the DC biasing asymmetry caused by the Q3-V1B configuration will force the LT1055 to bias well away from zero. Tolerance stack-up could cause saturation

limiting in the LT1055's output, reducing overall available swing. This is avoided by skewing the stage's bias string with the potentiometer adjustment. To make this adjustment, ground the input and trim the potentiometer for 0V out at the LT1055.

Figure 11's full-power bandwidth is 12kHz, with a slew rate of about 12V/ μ s. Figure 12 shows response to a bipolar input (Trace A). The output responds cleanly, although the slew and settling characteristics reflect the stage's asymmetric gain bandwidth. This stage's output is extremely rugged, due to the inherent forgiving nature of vacuum tubes. No special short-circuit protection is needed, and the output will survive shorts to voltages many times the value of the \pm 150V supplies.

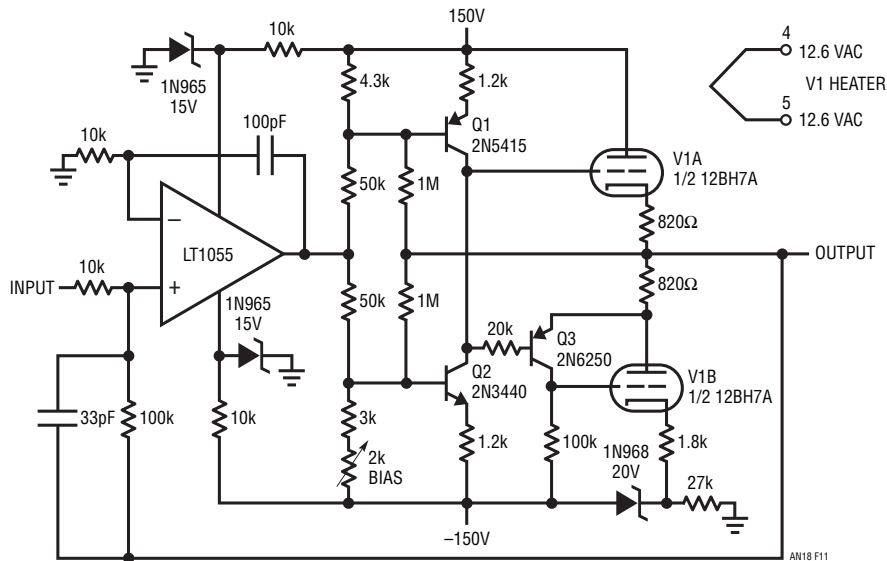


Figure 11. Rugged \pm 120V Output Stage Employing Mr. De Forest's Descendants. DANGER! High Voltages Present. Use Caution

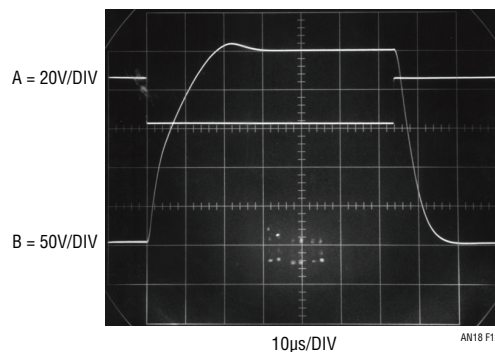


Figure 12. Figure 11's Response. Asymmetric Slew and Settling Are Due to Q3-V1B Connection. DANGER! High Voltages Present. Use Caution

Unipolar Output, 1000V Gain Stage

Figure 13 shows a unipolar output gain stage which swings 1000V and supplies 15W. This boost stage has the highly desirable property of operating from a single, low voltage supply. It does not require a separate high voltage supply. Instead, the high voltage is directly generated by a switching converter which is an integral part of the gain stage.

A2's output drives Q3, forcing current into T1. T1's primary is chopped by MOSFETs Q1 and Q2, which receive complementary drive from the 74C04 based square wave oscillator. A1 supplies power to the oscillator. T1 provides voltage step-up. Its rectified and filtered output is the boost stage's output. The 1M-10k divider furnishes feedback to A2, closing a loop around it. The 0.01 μ F capacitor from Q3's emitter to A2's negative input gives loop stability

and the 0.002 μ F unit trims step response damping. C1 is used for short-circuit limiting. Current from Q1 and Q2 passes through the 0.1 Ω shunt. Abnormal output currents cause shunt voltage to rise, tripping C1's output low. This simultaneously removes drive from Q3, Q1 and Q2's gates and the oscillator, resulting in output shutdown. The 1k-1000pF filter ensures that C1 does not trip due to current spikes or noise during normal operation.

A2 supplies whatever drive is required to close the loop, regardless of the output voltage called for. The low, resistive saturation losses of the VMOS FETs combined with A2's servo action allows controlled outputs all the way down to 0V.

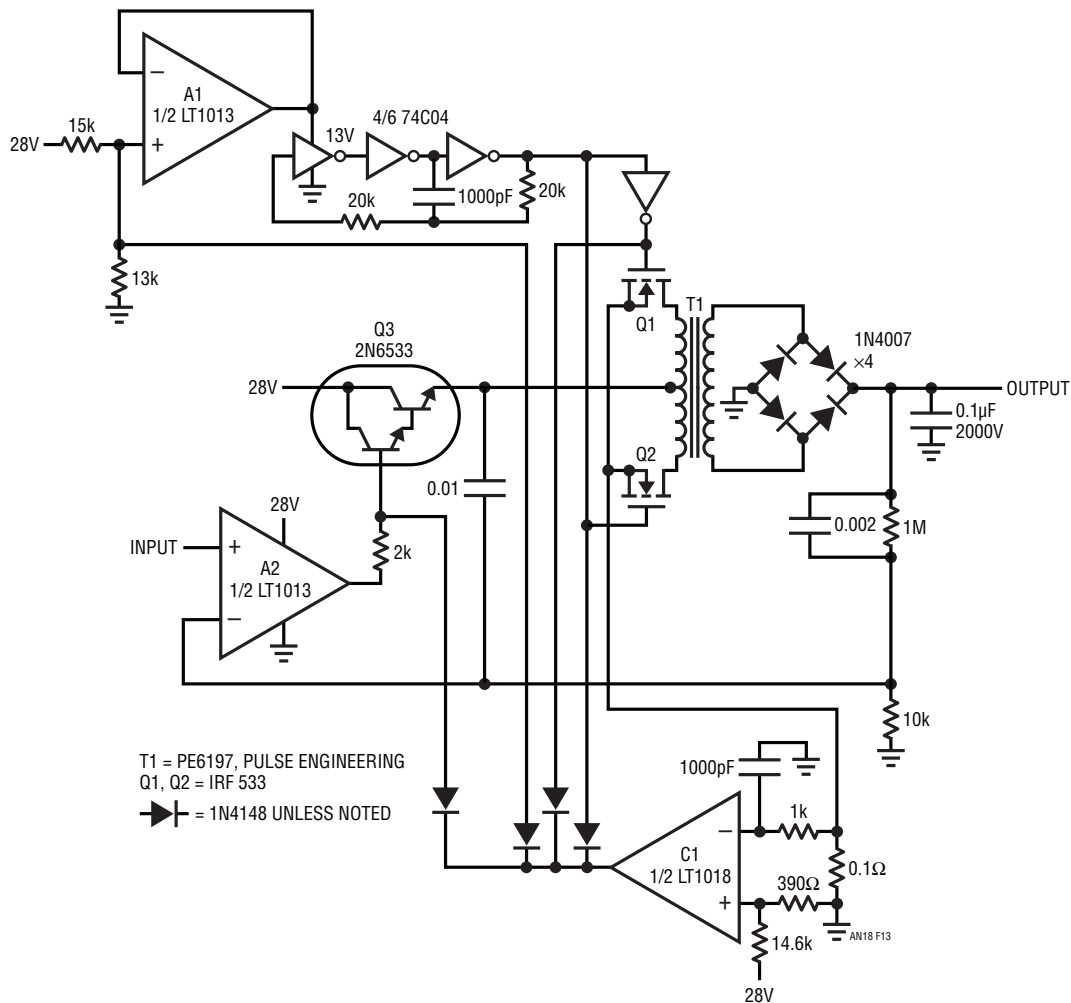


Figure 13. 15 Watt, 1000V Unipolar Output Stage. **DANGER! High Voltages Present. Use Caution**

Application Note 18

Substituting higher power devices for Q1 and Q2 along with a larger transformer allows more output power, although dissipation in Q3 will become excessive. If higher power is desired, a switched mode stage should be substituted for Q3 to maintain efficiency.

The 0.1 μ F filter capacitor at the output limits full-power bandwidth to about 60Hz. Figure 14 shows dynamic response at full load. Trace A, a 10V input, produces a 1000V output in Trace B. Note that slew is faster on the leading edge, because the stage cannot sink current. The falling edge slew rate is determined by the load resistance.

\pm 15V Powered, Bipolar Output, Voltage Gain Stage

Figure 13's output is limited to unipolar operation because the step-up transformer cannot pass DC polarity information.

Obtaining bipolar output from a transformer based voltage booster requires some form of DC polarity restoration at the output. Figure 15's \pm 15V powered circuit does this, using synchronous demodulation to preserve polarity in its \pm 100V output. This booster features 150mA current output, 150Hz full-power output and a slew rate of 0.1V/ μ s.

The high voltage output is generated in similar fashion to Figure 13's circuit. The 74C04 based oscillator furnishes complementary gate drive to VMOS devices Q1 and Q2, which chop Q3's output into T1, a step-up transformer. In this design, however, a synchronously switched absolute value amplifier is placed between servo amplifier A1 and Q3's drive point. Input signal polarity information, derived from A1's output, causes C1 to switch the LTC1043 section located at A2's positive input. This circuitry is arranged so that A2's output is the positive absolute value of A1's input signal. A second, synchronously switched LTC1043 section gates oscillator pulses to the appropriate SCR

trigger transformer at the output. For positive inputs LTC1043 Pins 2 and 6 are connected, as well as Pins 3 and 18. A2, acting as a unity gain follower, passes A1's output directly and drives Q3. Simultaneously, oscillator pulses are conducted through an inverter via LTC1043 Pin 18. The inverter drives trigger transformer T2, turning Q4 on. Q4, biased from the full wave bridge's positive point, supplies positive polarity voltage to the output.

Negative inputs cause the LTC1043 switch positions to reverse. A2, functioning as an inverter, again supplies Q3 with positive voltage drive. The Schottky diode at A2 prevents the LTC1043 from seeing transient negative voltages. Oscillator pulses are directed to SCR Q5 via LTC1043 Pin 15, its associated inverter and T3. This SCR connects the full wave bridge's negative point to the output. Both SCR cathodes are tied together to form the circuit's output. The 100k-10k divider supplies feedback to A1 in the conventional manner. The synchronous switching allows polarity information to be preserved in the stage's output, permitting full bipolar operation. Figure 16 shows waveforms for a sine wave input. Trace A is A1's input. Traces B and C are Q1 and Q2's drain waveforms. Traces D and E are the full wave bridge's negative and positive outputs, respectively. Trace F, the circuit output, is an amplified, reconstructed version of A1's input. Phase skewing between the SCR switching and the carrier borne signal causes some distortion at the zero crossover. The amount of skew is both load and signal frequency dependent, and is not readily compensated. Figure 17 shows distortion products (Trace B) at a 10Hz output (Trace A) at full load (\pm 100V at 150mA peak). Residual high frequency carrier components are clearly present, and the zero point SCR switching causes the sharp peaks. RMS distortion measured 1% at 10Hz, rising to 6% at 100Hz.

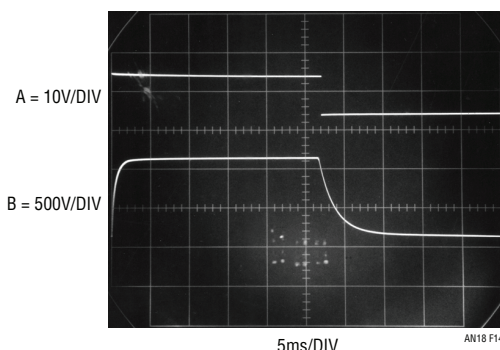


Figure 14. Figure 13's Pulse Response. **DANGER! High Voltage Present. Use Caution**

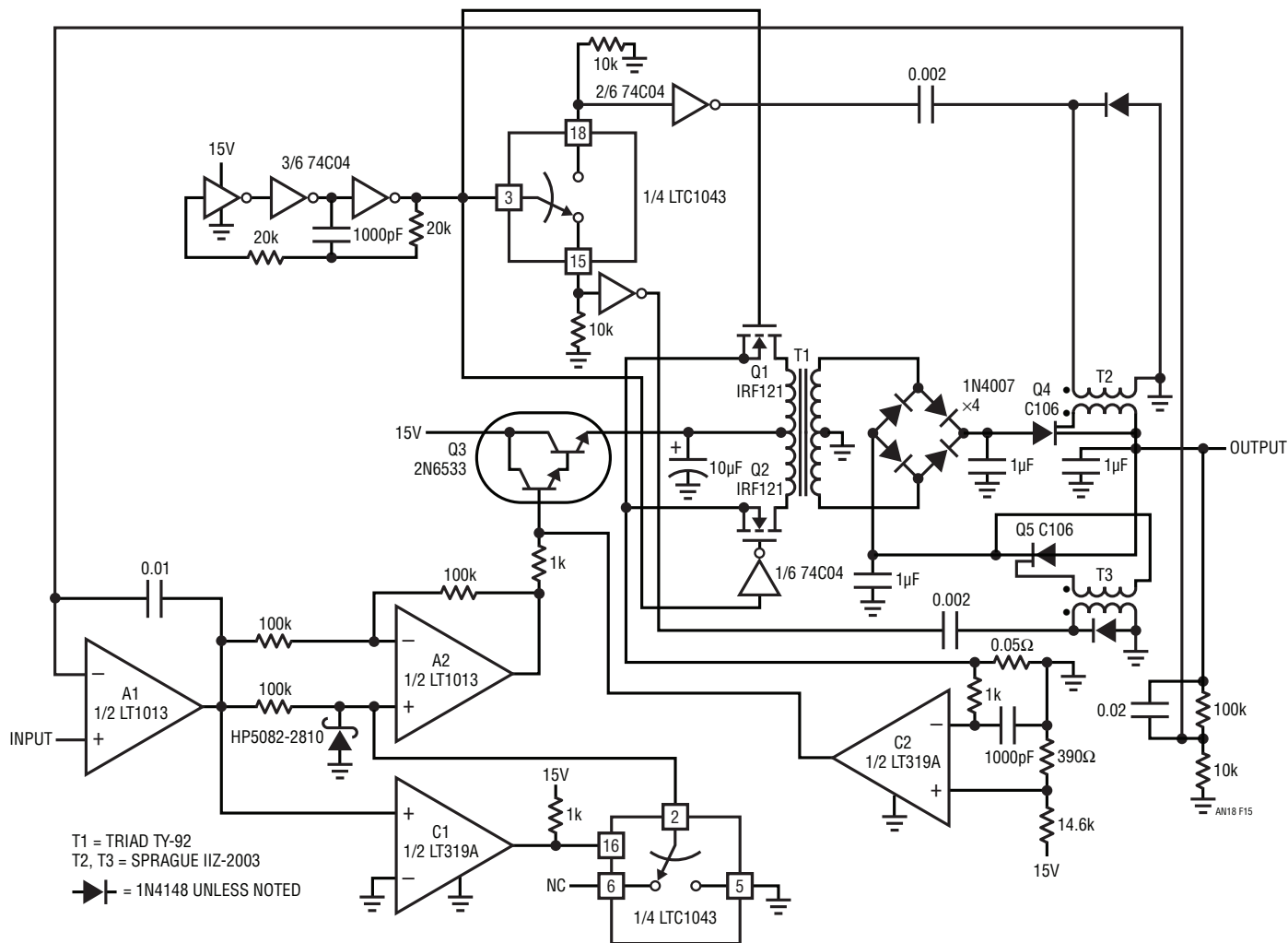


Figure 15. ±100V Output Stage Runs from ±15V Supply. DANGER! High Voltage Present. Use Caution

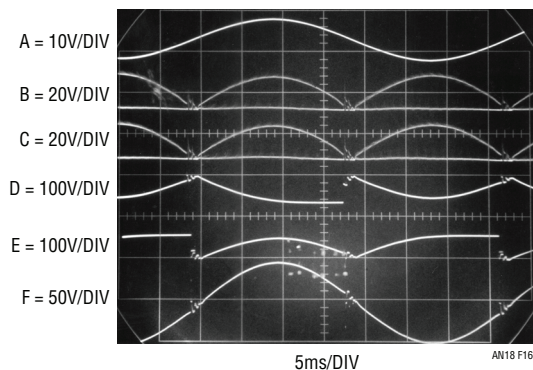


Figure 16. Figure 15's Operating Details. DANGER! High Voltages Present. Use Caution

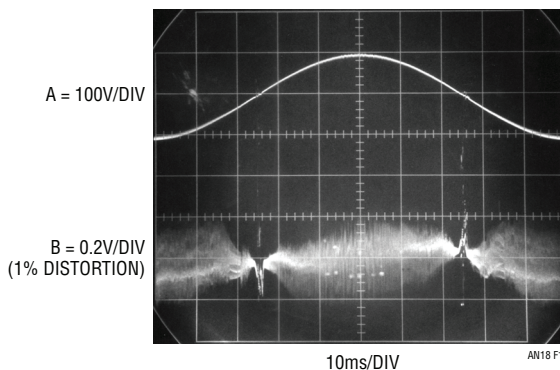


Figure 17. Crossover Residue Reflects Chopping and Zero Cross Switching. DANGER! High Voltages Present. Use Caution

Application Note 18

C2 supplies current limiting in identical fashion to Figure 13's scheme. Frequency compensation is also similar. A 0.01 μ F capacitor at A1 gives loop stability, while the 0.02 μ F feedback unit sets damping. Figure 18

summarizes the capabilities of the power gain stages presented, and should be useful in selecting an approach for a given application.

FIGURE	VOLTAGE GAIN	CURRENT GAIN	FULL-POWER BANDWIDTH	COMMENTS
1a	No	Yes, 150mA Output	600kHz	Simple, Easy
1b	No	Yes, 150mA Output	1.5MHz	Simple, Easy
2	No	Yes, 3A	100kHz	
3	No	Yes, 200mA	7.5MHz	Feedforward Technique Gives High Bandwidth >1000V/ μ s Slew. Inverting Operation Only
5a, 5b	Yes	No	Depends On Op Amp	Simple Stages Allow Wide Swing, Almost to Rails
7	Yes	Yes, 125mA	600kHz	High Current, Nearly Rail-to-Rail Swing Capability
9	Yes, \pm 120V	Yes, 25mA	15kHz	Good, General Purpose High Voltage Stage
11	Yes, \pm 120V	Yes, 25mA	12kHz	Almost Indestructible Output
13	Yes, 1000V	No	60Hz	High Voltage Output with No External High Voltage Supplies Required. Limited Bandwidth with Asymmetrical Slewing. Positive Outputs Only
15	Yes, \pm 100V	Yes, 150mA	150Hz	High Voltage Outputs with No External High Voltage Supplies. Limited Bandwidth. Full Bipolar Output.

Figure 18. Summary of Circuit Characteristics

The Oscillation Problem (Frequency Compensation without Tears)

All feedback systems have the propensity to oscillate. Basic theory tells us that gain and phase shift are required to build an oscillator. Unfortunately, feedback systems, such as operational amplifiers, have gain and phase shift. The close relationship between oscillators and feedback amplifiers requires careful attention when an op amp is designed. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when feedback is applied. Further, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This is why feedback loop enclosed power gain stages can cause oscillation.

A large body of complex mathematics is available which describes stability criteria, and can be used to predict

stability characteristics of feedback amplifiers. For the most sophisticated applications, this approach is required to achieve optimum performance.

However, little has appeared which discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. Specifically, a practical approach to stabilizing amplifier-power gain stage combinations is discussed here, although the considerations can be generalized to other feedback systems.

Oscillation problems in amplifier-power booster stage combinations fall into two broad categories; *local* and *loop* oscillations. *Local* oscillations can occur in the boost stage, but should not appear in the IC op amp,

which presumably was debugged prior to sale. These oscillations are due to transistor parasitics, layout and circuit configuration caused instabilities. They are usually relatively high in frequency, typically in the 0.5MHz to 100MHz range. Usually, local booster stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation. Text Figure 7 furnishes an instructive example. The Q3-Q5 and Q4-Q6 pairs have high gain bandwidth. The intended resistive feedback loops allow them to oscillate in the 50MHz to 100MHz region without the 100pF-200Ω network shunting the DC feedback. This network rolls off gain bandwidth, preventing oscillation. It is worth noting that a ferrite bead in series with the 2k resistor will give similar results. In this case, the bead raises the inductance of the wire, attenuating high frequencies.

The photo in Figure B1 shows text Figure 7 following a bipolar square wave input with the local high frequency RC compensation networks removed. The resultant high frequency oscillation is typical of locally caused disturbances. Note that the major loop is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high F_T transistors unless they are needed. When high frequency devices are in use, plan layout carefully. In very stubborn cases, it may be necessary to lightly bypass transistor junctions with small capacitors or RC networks. Circuits which use local feedback can sometimes require careful transistor selection and use. For example, transistors operating in a local loop may require different F_T 's to achieve stability. Emitter followers are notorious sources of oscillation, and should never be directly driven from low impedance sources.

Text Figure 5 uses an RC damper network from the 74C04 inverters to ground to eliminate local oscillations. In that circuit the 74C04s are forced to run in their linear region. Although their DC gain is low, bandwidth is high. Very small parasitic feedback terms result in high frequency oscillations. The damper network provides a low impedance to ground at high frequency, breaking up the unwanted feedback path.

Loop oscillations are caused when the added gain stage supplies enough delay to force substantial phase shift. This causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain combined with the added delay causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10Hz to 1MHz.

A good way to eliminate loop caused oscillations is to limit the gain bandwidth of the control amplifier. If the booster stage has higher gain bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When control amplifier gain bandwidth dominates, oscillation is assured. Under these conditions, the control amplifier hopelessly tries to servo a feedback signal which consistently arrives "too late." The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations it is preferable to "brute force" compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling off control amplifier gain bandwidth. The feedback capacitor serves to trim step response only and should not be relied on to stop outright oscillation.

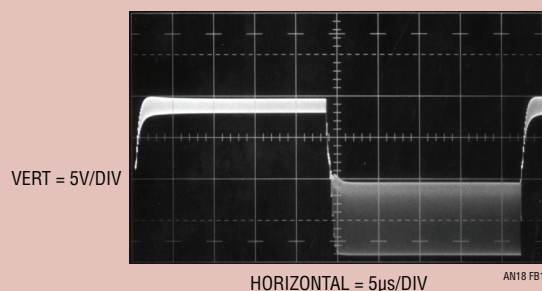


Figure B1. Typical Local Output Stage Oscillation

Application Note 18

Figures B2 and B3 illustrate these issues. The 600kHz gain bandwidth LT1012 amplifier used with the LT1010 current buffer produces the output shown in Figure B2. The LT1010's 20MHz gain bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1012's internal roll-off is well below that of the output stage, and stability is achieved with no external compensation components. Figure B3 uses a 15MHz LT318A as the control amplifier. The associated photo shows the results. Here, the control amplifier's roll-off, close to the output stages, causes problems. The phase shift through the LT1010 is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the LT318A's gain bandwidth (see text Figure 1).

The fact that the slower op amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is "free". The faster amplifier makes the AC characteristics of the output stage become significant and requires roll-off components for stability.

Text Figure 9's high voltage stage is an interesting case. The high voltage transistors are very slow devices, and the LT1055 amplifier has a much higher gain bandwidth than the output stage. The LT1055 is locally compensated by the 10k-100pF network, giving it an integrator-like response. This compensation, combined with the damping provided by the 33pF feedback capacitor, gives good loop response. The procedure used to compensate this circuit is typical of what is done to stabilize boosted amplifier loops and is worth reviewing.

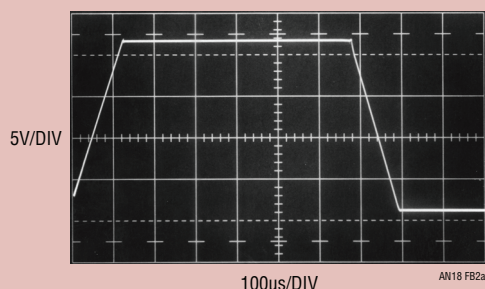


Figure B2. A Slow Control Amplifier Gives "Free" Loop Compensation

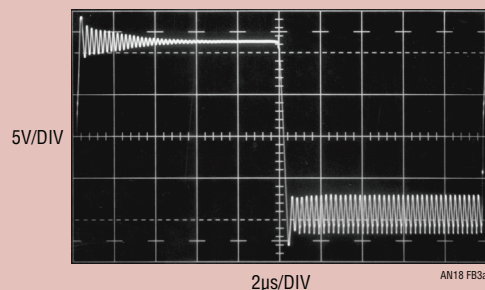
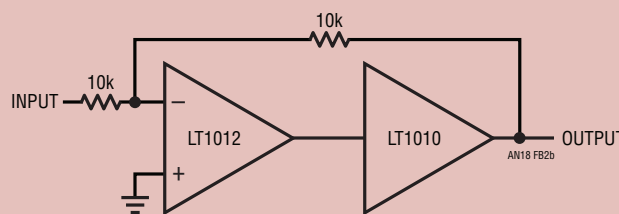
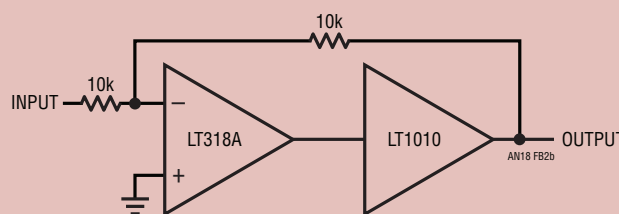


Figure B3. A Fast Control Amplifier Gives "Free" Loop Oscillation



With no compensation components installed, the circuit is turned on and oscillations are observed (photo, Figure B4). The relatively slow oscillation frequency suggests a loop oscillation problem. The LT1055 gain bandwidth is degenerated with the RC components around the amplifier. The RC time constant is chosen to eliminate oscillations and give the best possible response (photo, Figure B5) with no loop feedback capacitor in place. Observe that the $1\mu\text{s}$ time constant selected offers significant attenuation at the oscillation frequency

noted in the photo, Figure B4. Finally, the loop feedback capacitor (33pF) is selected to give the optimum damping shown in text Figure 10.

When making tests like these, remember to investigate the effects of various loads and output operating voltages. Sometimes a compensation scheme which appears fine gives bad results for some output conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

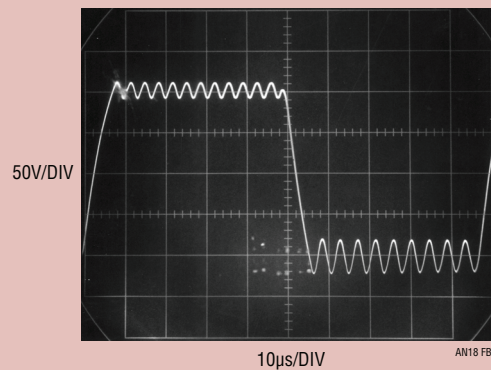


Figure B4. Oscillations After Slewing Suggest a Loop Problem

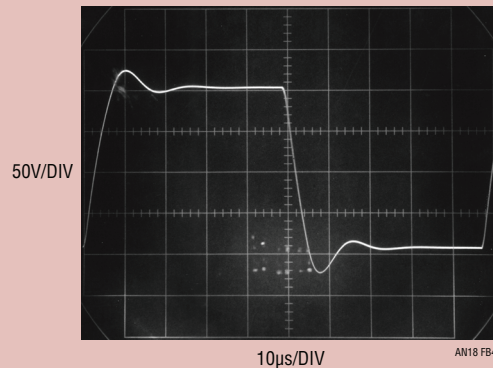


Figure B5. Control Amplifier Roll-Off Stabilizes B4's Problems

Application Note 18

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Composite Amplifiers

Jim Williams

Amplifier design, regardless of the technology utilized, is a study in compromise. Device limitations make it difficult for a particular amplifier to achieve optimal speed, drift, bias current, noise and power output specifications. As such, various amplifier families emphasizing one or more of these areas have evolved. Some amplifiers are very good attempts at doing everything well, but the best achievable performance figures are limited to dedicated designs.

Practical applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. Composite designs combine the best features of two or more amplifiers to achieve performance unobtainable in a single device. More subtly, composite designs permit circuit approaches which are normally impractical. This is particularly true of high speed stages which may be

designed with little attention to DC biasing considerations if a separate stabilizing stage is employed.

Figure 1 shows a composite made up of an LT[®]1012 low drift device and an LT1022 high speed amplifier. The overall circuit is a unity-gain inverter, with the summing node located at the junction of three 10k resistors. The LT1012 monitors this summing node, compares it to ground and drives the LT1022's positive input, completing a DC stabilizing loop around the LT1022. The 10k-300pF time constant at the LT1012 limits its response to low frequency signals. The LT1022 handles high frequency inputs while the LT1012 stabilizes the DC operating point. The 4.7k-220Ω divider at the LT1022 prevents excessive input overdrive during start-up. This circuit combines the LT1012's 35μV offset and 1.5V/°C drift with the LT1022's 23V/μs slew rate and 300kHz full-power bandwidth. Bias current, dominated by the LT1012, is about 100pA.

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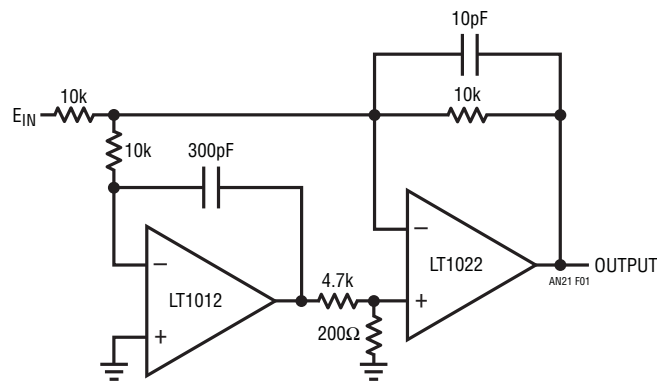


Figure 1. Basic DC-Stabilized Fast Amplifier

Application Note 21

Figure 2 is similar, but uses discrete FETs to more than triple the speed. Here A1's input stage is turned off by connecting its inputs to the negative rail. The differentially connected FETs bias the second state via A1's offset pins. This connection replaces A1's input stage, reducing bias current and increasing speed. FET mismatch would normally result in excessive offset and drift. A2 corrects this by monitoring the summing point (the junction of the two 4.7k resistors) and forcing Q2's gate to eliminate overall offset. The 10k-1000pF pair limits A2's response to low frequency, and the 1k divider chain prevents overdrive to Q2 on start-up. The 1k-10pF damper at the summing node aids high frequency stability. Figure 3 shows pulse response. Trace A is the input and Trace B the output. Slew rate exceeds 100V/ μ s, with clean damping. Full-power bandwidth is about 1MHz, and the input bias current is in the 100pA range. DC offset and drift are similar to Figure 1.

Figure 4 shows a highly stable unity-gain buffer with good speed and high input impedance. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open-loop configuration would be quite drift because there is no DC feedback. The LTC[®]1052 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through

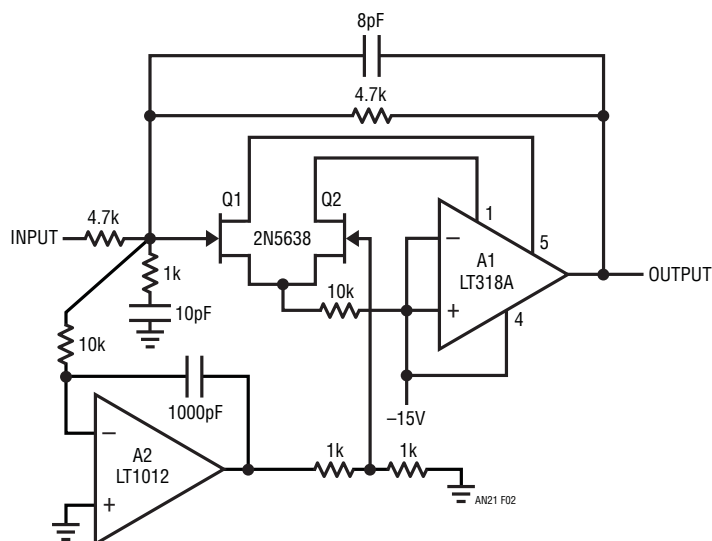


Figure 2. Fast DC-Stabilized FET Amplifier

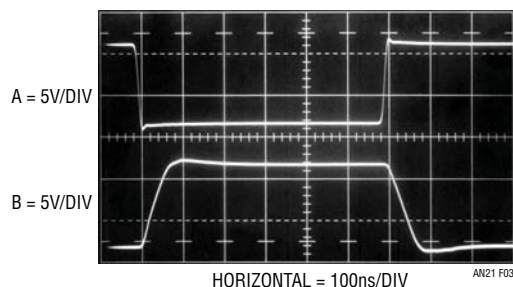


Figure 3. Figure 2's Waveforms

Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

The LT1010's 15MHz bandwidth and 100V/ μ s slew rate, combined with its 150mA output, are fast enough for most circuits. For very fast requirements, the alternate discrete component buffer shown will be useful. Although its output is current limited at 75mA, the GHz range transistors

employed provide exceptionally wide bandwidth, fast slewing and very little delay. Figure 5 shows the LTC1052 stabilized buffer circuit's response using the discrete stage. Response is clean and quick, with delay inside 4ns. Slew exceeds 2000V/ μ s with full-power bandwidth approaching 50MHz. Note that rise time is limited by the pulse generator and not the circuit. For either stage, offset is set by the LTC1052 at 5 μ V, with gain about 0.95.

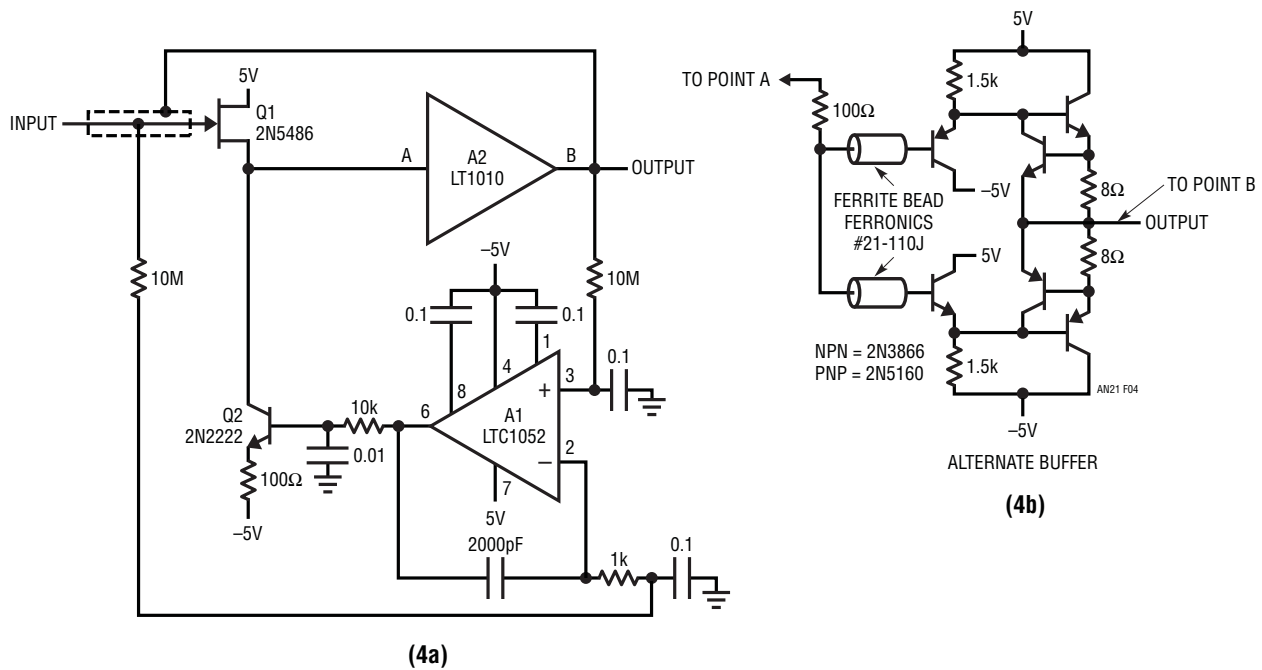


Figure 4. Wideband FET Input Stabilized Buffer

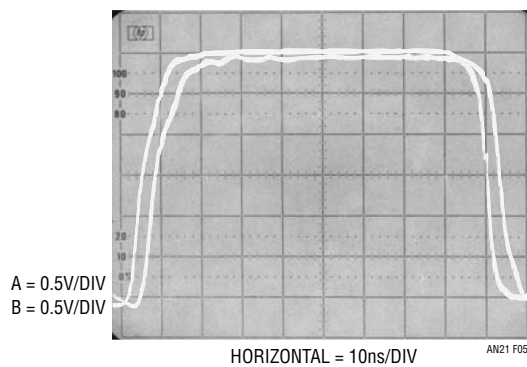


Figure 5. Figure 4's Waveforms

Application Note 21

A potential difficulty with Figure 4's circuit is that the gain is not quite unity. Figure 6 maintains high speed and low bias while achieving a true unity-gain transfer function.

This circuit is somewhat similar to Figure 4, except that the Q2-Q3 stage takes gain. A2 DC stabilizes the input-output path, and A1 provides drive capability. Feedback is to Q2's emitter from A1's output. The 1k adjustment allows the gain to be precisely set to unity. With the LT1010 output stage slew and full-power bandwidth ($1V_{P-P}$) are $100V/\mu s$ and 10MHz, respectively. $-3dB$ bandwidth exceeds 35MHz. At

$A = 10$ (e.g., 1k adjustment set at 50Ω) full-power bandwidth stays at 10MHz while the $-3dB$ point falls to 22MHz.

With the optional discrete stage, slew exceeds $1000V/\mu s$ and full-power bandwidth ($1V_{P-P}$) is 18MHz. $-3dB$ bandwidth is 58MHz. At $A = 10$, full power is available to 10MHz, with the $-3dB$ point at 36MHz.

Figures 7a and 7b show response with both output stages. The LT1010 is used in Figure 7a (Trace A = input, Trace B = output). Figure 7b uses the discrete stage and is slightly faster. Either stage provides more than adequate

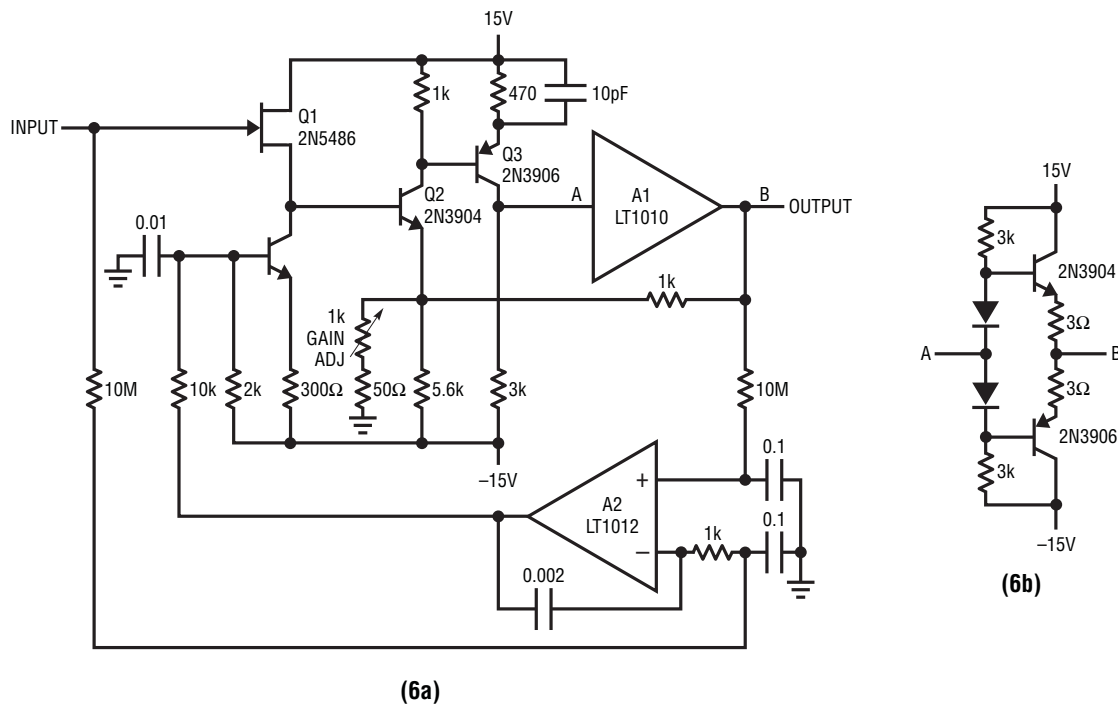


Figure 6. Gain Trimmable Wideband FET Amplifier

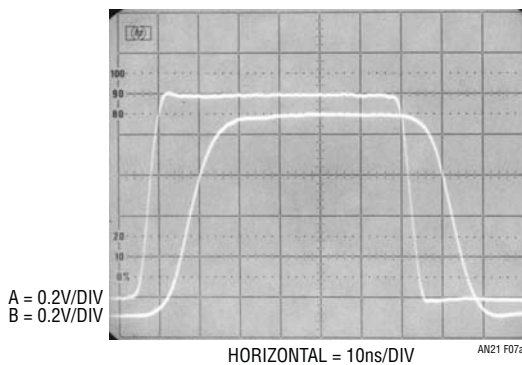


Figure 7a. Figure 6's Waveforms Using the LT1010

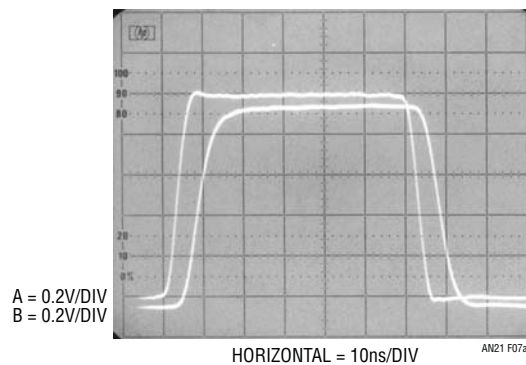


Figure 7b. Figure 6's Waveforms Using Discrete Stage

performance for driving video cable or data converters, and the LT1012 maintains DC stability under all conditions.

Figure 8 is another DC-stabilized fast amplifier which functions over a wide range of gains (typically 1-10). It combines the LT1010 and a fast discrete stage with an LT1008 based DC stabilizing loop. Q1 and Q2 form a differential stage which single-ends into the LT1010. The circuit delivers $1V_{P-P}$ into a typical 75Ω video load. At $A = 2$, the gain is within 0.5dB to 10MHz with the $-3dB$ point occurring at 16MHz. At $A = 10$, the gain is flat ($\pm 0.5dB$ to 4MHz) with a $-3dB$ point at 8MHz. The peaking adjustment should be optimized under loaded output conditions.

Normally, the Q1-Q2 pair would be quite drifty, but the LT1008 corrects for this. This correction stage is similar

to the one in Figures 4 and 6, except that the feedback is taken from a divided down sample of the fast amplifier. The ratio of this divider should be set to the same value as the circuit's closed-loop gain. Frequency roll-off of this stage is set by the $1M-0.022\mu F$ filters in the LT1008's input lines. The $0.22\mu F$ capacitor at the amplifier eliminates oscillations. The DC loop servo controls drift by biasing the DC operating point of Q2's collector to force zero error between the LT1008's inputs.

This is a simple stage for fast applications where relatively low output swing is required. Its $1V_{P-P}$ output works nicely for video circuits. A possible problem is the relatively high bias current, typically $10\mu A$. Additional swing is possible, but more circuitry is needed.

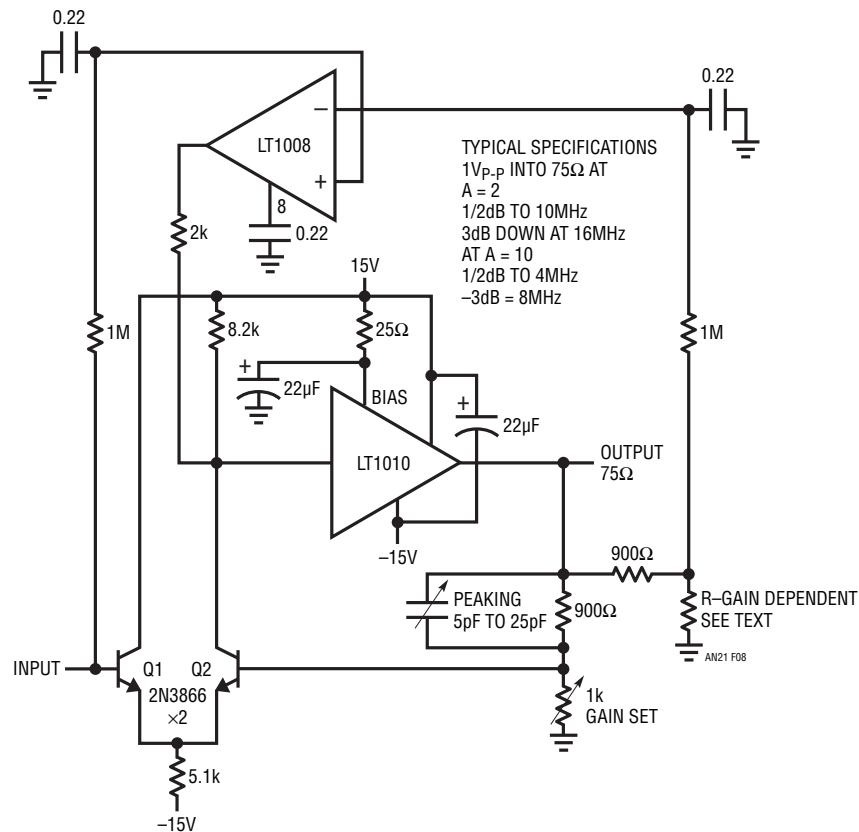


Figure 8. Fast, Stabilized Noninverting Amplifier

Application Note 21

Figure 9's circuit addresses these issues. It trades speed for output swing and reduced bias current. As before, a separate loop maintains DC stability. This circuit is a good example of an approach made practical by composite techniques. Without the separate stabilizing loop, the DC imbalances in the signal path would preclude any level of operation.

In this arrangement a PNP level-shifting stage (Q4) has been added to Figure 8's circuit to increase available swing at the LT1010 output. This is obtained at the expense of available bandwidth and amplifier stability. The 33pF capacitor from Q4's collector to the circuit's summing node (Q3's gate) affords stable loop compensation.

Figure 8's bias current errors are eliminated by Q3, a FET source follower. This device buffers the summing point from the relatively high bias current required by Q2. Normally, this configuration would cause volts of offset, due to Q3's gate-source voltage. Here, A1 closes a DC restoration loop, forcing Q1's base to whatever point is required to compensate for the offset. Thus, A1's operation not only provides low DC error but permits a simplistic approach to minimizing summing point bias current. Figure 10 shows operating waveforms for a 10V output. Trace A is the input, while Trace B is the output. Slew rate is about 100V/ μ s, with a full-power bandwidth of 1MHz. The LT1010 allows 100mA outputs and makes cable driving practical at these speeds.

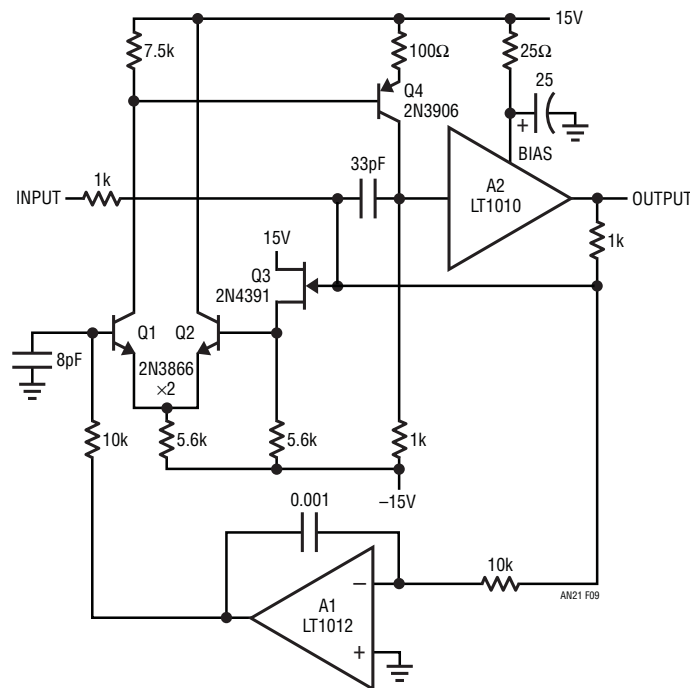


Figure 9. Fast, Stabilized Inverting Amplifier with Low Summing Point Bias Current

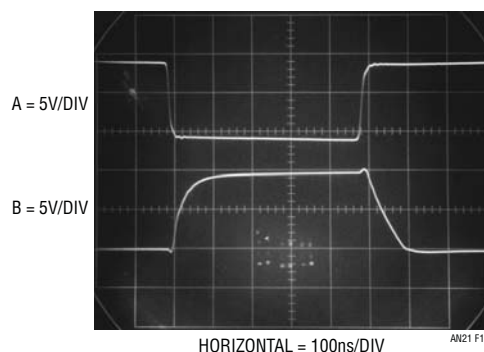


Figure 10. Figure 9's Pulse Response

Figure 11 shows another fast stage with wide output swing. The circuit is noninverting, and has higher input impedance than Figure 9. Additionally, its operation is based on an arrangement commonly referred to as “current mode” feedback. This technique, well established in RF design and also employed in some monolithic instrumentation amplifiers, permits fixed bandwidth over a wide range of closed-loop gains. This contrasts with normal feedback schemes, where bandwidth degrades as closed-loop gain increases.

The overall amplifier is composed of two LT1010 buffers and a gain stage, Q1 and Q2. A3 acts as a DC restoration loop. The 33Ω resistors sense A1’s operating current, biasing Q1 and Q2. These devices furnish complementary voltage gain to A2, which provides the circuit’s output. Feedback is from A2’s output to A1’s output, which is a low impedance point.

A3’s stabilizing loop compensates large offsets in the signal path, which are dominated by mismatch in Q1 and

Q2. Correction is implemented by controlling the current through Q3, which shunts Q2’s base bias resistor. Adequate loop capture range is assured by deliberate skewing of Q1’s operating point via the 330Ω unit. The 9k-1k feedback divider feeding A3 is selected to equal the gain ratio of the circuit, in this case 10.

The feedback scheme makes A1’s output look like the negative input of the amplifier, with closed-loop gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that bandwidth becomes relatively independent of closed-loop gain over a reasonable range. For this circuit, full-power bandwidth remains at 1MHz over gains of 1 to about 20. The loop is quite stable, and the 15pF value at A2’s input provides good damping over a wide range of gains. The LT1010 buffers limit bandwidth in this circuit. Dramatic speed improvement is possible if they are replaced by discrete stages.

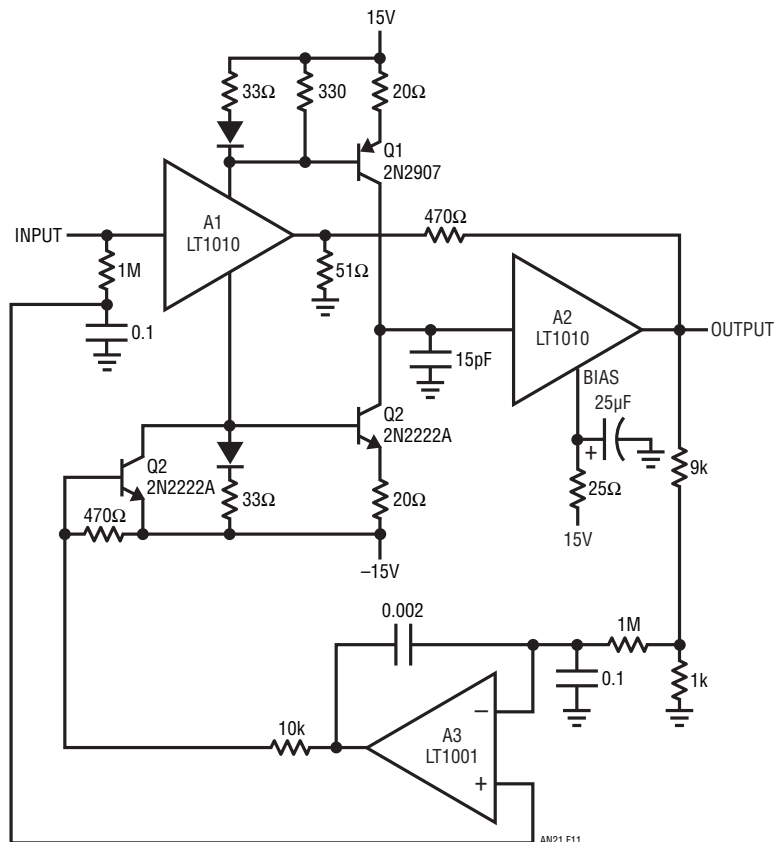


Figure 11. “Current Mode Feedback” Amplifier

Application Note 21

Figure 12 substitutes discrete elements for Figure 11's LT1010s. Although this arrangement is substantially more complex, it provides an extraordinarily wideband amplifier. This composite design is composed of three amplifiers;

the discrete wideband stage, a quiescent current control amp and an offset servo. Q1-Q4 replace Figure 11's A1, although complementary voltage gain is taken at the collectors Q3 and Q4. Q5 and Q6 provide additional

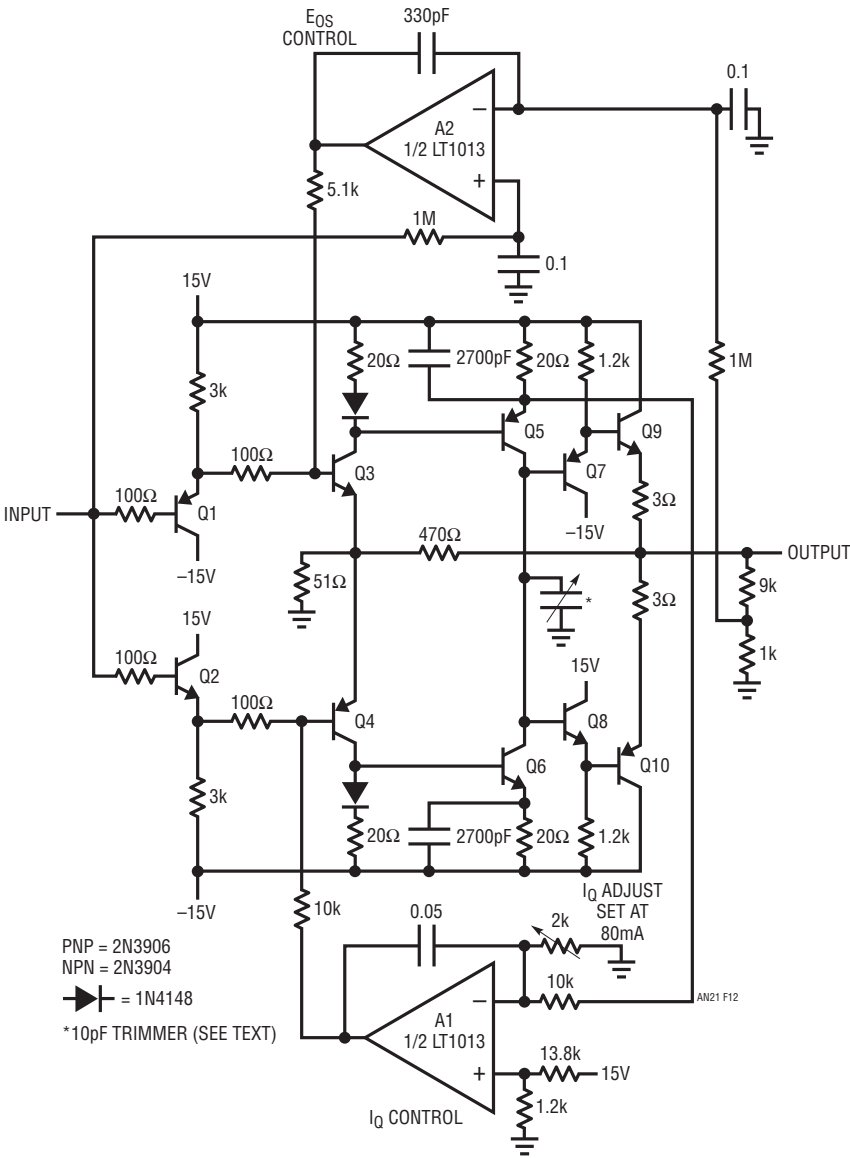


Figure 12. Stabilized, Ultra-Wideband “Current Mode Feedback” Amplifier (Son of Godzilla Amplifier)

gain, similar to Q1 and Q2 in Figure 11. Q7-Q10 form the output buffer stage. The feedback scheme is identical to Figure 11's, with summing action at the Q3-Q4 emitter connection. To obtain maximum bandwidth, quiescent current is quite high. Without closed-loop control, the circuit will quickly go into thermal runaway and destroy itself. A1 provides the required servo control of quiescent current. It downs this by sampling a resistively divided version of the voltage across Q5's emitter resistor and comparing it to a power supply derived reference. A1's output biases Q4, completing a loop which forces fixed current through Q5. This action effectively controls overall quiescent current in the discrete stage. Simultaneously, A2 corrects for offset by forcing Q3's base to equalize the DC input and output values at the discrete stage. Because the closed-loop gain is set at 10 (470Ω and 51Ω ratio), A2 samples the output via the 10:1 divider. Both A1 and A2 have local roll-off, limiting their response to low frequency. Casual consideration of A1 and A2's operation might raise concern about interaction, but detailed analysis shows this

is not so. The offset and quiescent current loops do not influence each others operation.

When this circuit is constructed using high frequency layout techniques and a ground plane, performance is quite impressive. For gains of 1 to 20, full-power bandwidth remains at 25MHz, with the -3dB point beyond 110MHz. Slew rate exceeds $3000\text{V}/\mu\text{s}$. These figures can be improved upon by using RF transistors, although the types shown are inexpensive and readily available. Figure 13 shows pulse response for a $\pm 12\text{V}$ output (Trace B) at a gain of 10 (input is Trace A). Delay is about 6ns, with rise time limited by the input pulse generator. Damping is optimized with the 10pF trimmer at the Q5-Q6 collector line. To use this circuit, adjust the I_Q level to 80mA *IMMEDIATELY* after turn on. Next, set A2's input resistor divider to a ratio appropriate to the closed-loop circuit gain. Finally, adjust the 10pF trimmer for best response. Note that, in the interests of speed, this circuit has no output protection.

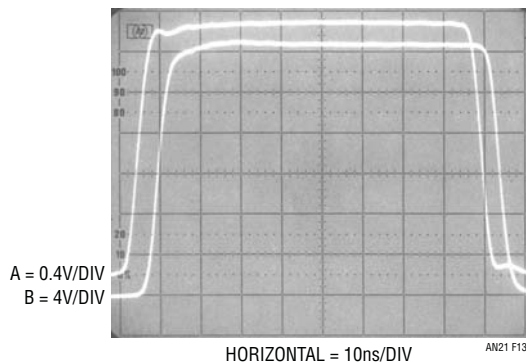


Figure 13. Figure 12's Pulse Response (Measurement Limited by Pulse Generator)

Application Note 21

Although speed and offset combinations are the most common area for composite techniques, other circuits are possible. Figure 14 shows a way to combine a low drift chopper-stabilized amplifier with an ultralow noise bipolar amplifier. The LTC1052 measures the DC error at the LT1028's input terminals and biases its offset pins to force offset to a few microvolts. The 1N758 Zeners allow the LTC1052 to function from $\pm 15V$ rails. The offset pin biasing at the LT1028 is arranged so the LTC1052 will always

be able to find the servo point. The $0.01\mu F$ capacitor rolls off the LTC1052 at low frequency, and the LT1028 handles high frequency signals. The combined characteristics of these amplifiers yield the following performance:

Offset Voltage	5 μV Max
Offset Drift	50nV/ $^{\circ}C$ Max
Noise	1.1nV \sqrt{Hz} Max

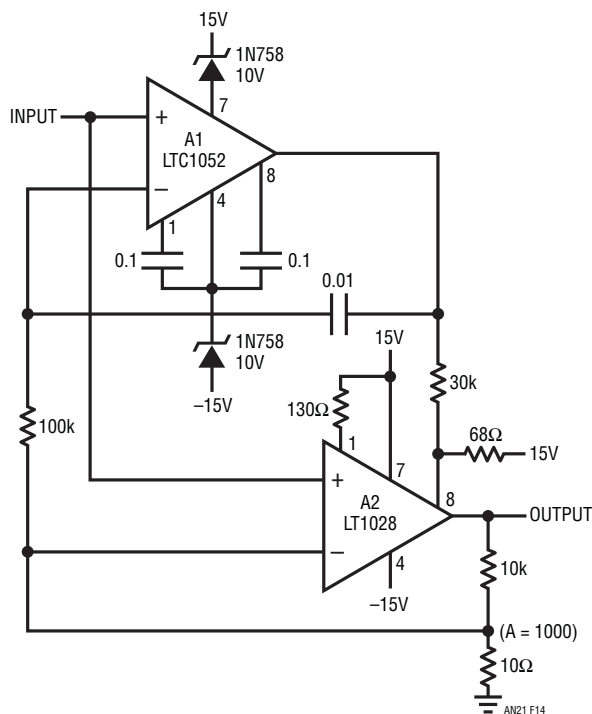


Figure 14. DC-Stabilized, Low Noise Amplifier

Figure 15 plots noise amplitude over time in a 0.1Hz to 10Hz bandwidth.

Figure 16 uses multiple LT1028 low noise amplifiers in a statistical noise reduction technique. It is based on the fact that noise decreases by the \sqrt{N} of the number of devices in

parallel. For example, for nine paralleled amplifiers, noise would decrease by a factor of three, to about $0.33\text{nV}/\sqrt{\text{Hz}}$ at 1kHz. A potential penalty of this connection is that the input current noise increases by \sqrt{N} devices.

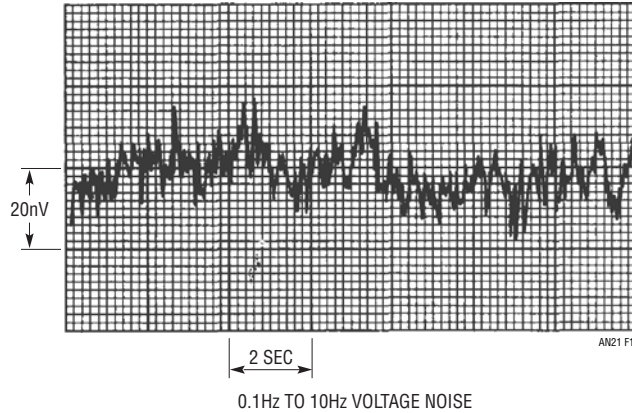


Figure 15. Figure 14's Noise vs Time

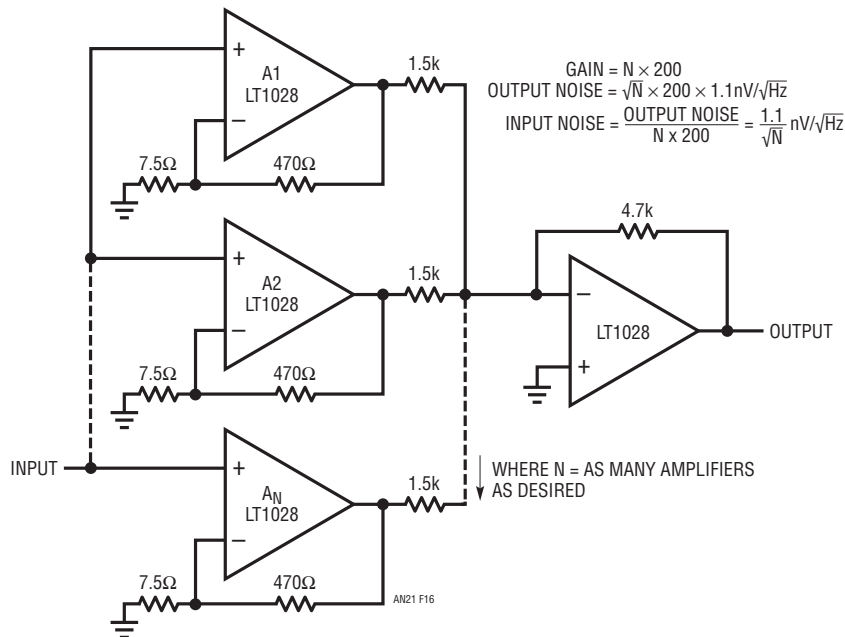


Figure 16. Low Noise Amplifier Using Paralleled Amplifiers

Application Note 21

A final circuit, Figure 17, uses a composite of paralleled LT1010 buffers to create a simple, high current stage. Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of LT1010s can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance or offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT} , flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}}$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst-case ($V_{IN} \rightarrow V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT} V_T$, where V_T is the total supply voltage.

Offset voltage is specified worst-case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst-case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25^\circ C$ will suffice for a worst-case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage above, the $25^\circ C$ limits should be used for worst-case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at $25^\circ C$.

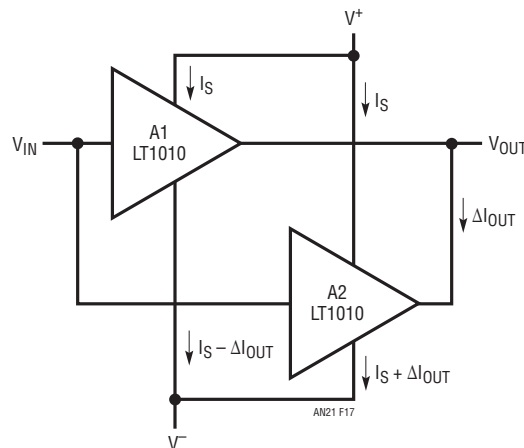


Figure 17. Paralleling Scheme for High Current Output

A Monolithic IC for 100MHz RMS-DC Conversion

Jim Williams

Previous monolithic circuits that converted waveforms to their DC-RMS equivalents utilized logarithmic techniques. This method limits bandwidth to below 1MHz and crest factor performance to about 10:1. Practically speaking, a waveform's RMS value is defined as its heating value in the load. Specialized instruments employ thermally based assemblies that compute the RMS value of the input. The thermal method provides substantially improved bandwidth and crest factor capability compared to logarithmically based converters.

Applications such as wideband RMS voltmeters, RF leveling loops, wideband AGC, high crest factor measurements, SCR power monitoring and high frequency noise measurements require the advantages of thermally based conversion.

Thermal RMS-DC converters are direct acting, thermo-electronic analog computers. The thermal technique is explicit, relying on "first principles." The simple operation permits wideband performance unattainable with implicit, indirect methods based on logarithmic computing.

Previously, thermally based converters were large and expensive to produce. A new IC, the LT1088, brings the advantages of thermal conversion to the circuit board in a 14 pin DIP, and at reasonable cost. Before discussing the LT1088, it is worthwhile reviewing thermal RMS-DC conversion.

Figure 1 shows a conceptual thermal RMS-DC converter. The input waveform warms the heater, resulting in increased output from the temperature sensor. The heating is related to the RMS value of the input waveform. The temperature sensor's DC output represents this heating.

Although simple, this method has some problems. The temperature sensor cannot distinguish between signal and ambient induced temperature changes. This issue could be addressed by summing in ambient temperature information, but a more significant problem remains. Even if the electrical portions of the design are perfectly linear, overall response is not. The power produced by the heater is non-linearly related to the input voltage ($P = I^2R$); hence temperature rise is similarly non-linearly proportioned.

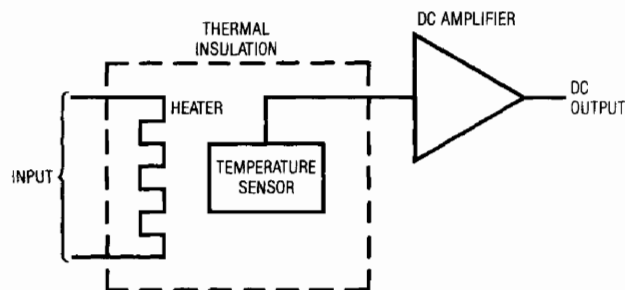


Figure 1. Conceptual RMS-DC Converter (with some problems)

Application Note 22

Additional non-linear signal conditioning is necessary for an output which linearly corresponds to the input voltage.

Figure 2 shows a classic scheme which corrects both of Figure 1's deficiencies. Here, the DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal interaction is non-linear, the input-output voltage relationship is linear with unity gain.

The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier will reject this common-mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure 2's output is linear because the matched thermal pair's non-linear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS-DC measurements. Typically, the assembly is composed of matched heater resistors, sensors and thermal insulation. These assemblies are relatively large and expensive to produce. In theory, monolithic IC techniques can be used to replace such assemblies, but the thermal insulation requirements present problems.

A simplified monolithically based circuit which accomplishes this function appears in Figure 3. It is quite similar to Figure 2's generalized approach. Here, the input drives R1, producing heating which lowers the value of D1's voltage. A1 responds by driving R2 to heat D2, closing a loop around the amplifier. Because the transistors and resistors are matched, A1's DC output equals the RMS value of the input, regardless of input frequency or waveshape. The aforementioned thermal terms limit the circuit's practical performance. In particular, thermal cross-coupling between the R1-D1 and R2-D2 pairs degenerates gain, degrading available signal. Also, differences in the dissipation constants and thermal capacity of the R-D pairs

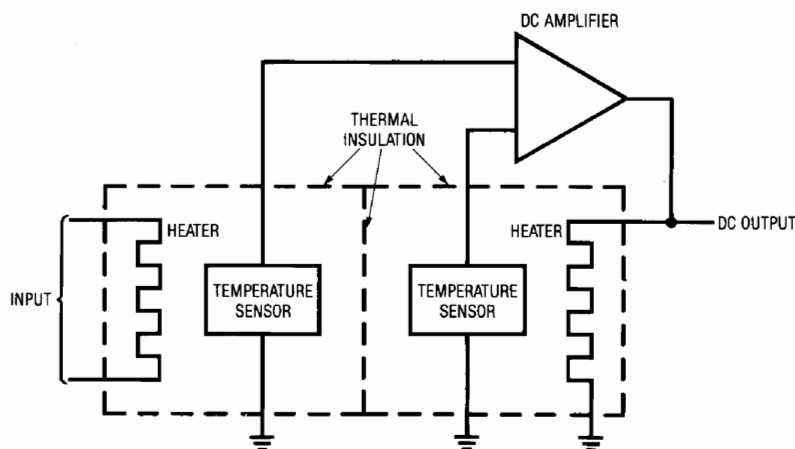


Figure 2. (A Better) Conceptual Thermal RMS-DC Converter

result in overall gain errors. Additionally, thermal resistance to ambient must be high to maximize D1-D2 signal output for reasonable input drive. Finally, the thermal path between the mated resistor-transistor pairs must be designed for efficient, low loss heat transfer.

Although the converter's basic principle is a straightforward extension of Figure 2, the electro-thermal design must be carefully addressed to produce a practical monolithic circuit. These thermal considerations dominate the design and form of the circuit.

Figure 4 shows a simple electro-analog of the thermal terms in the converter. The overall lumped matching of these terms heavily influences achievable performance. In particular, the die attach thermal resistance dominates

the thermal impedance path. If this resistance is made very high, the effects of mismatch in the other terms are minimized.

Thermal cross-coupling is almost entirely eliminated by using separate, identical die for the diode-heater pairs. This eliminates cross heating more effectively than any possible single die approach. A gain error, which is corrected by introducing a corresponding gain trim, is caused by residual mismatch in thermal terms. These include die size, dissipation constant, and thermal capacity differences. The most significant term is differing amounts and distribution of the die attach material. The gain correcting trim is introduced by altering the gain of the output stage in Figure 3.

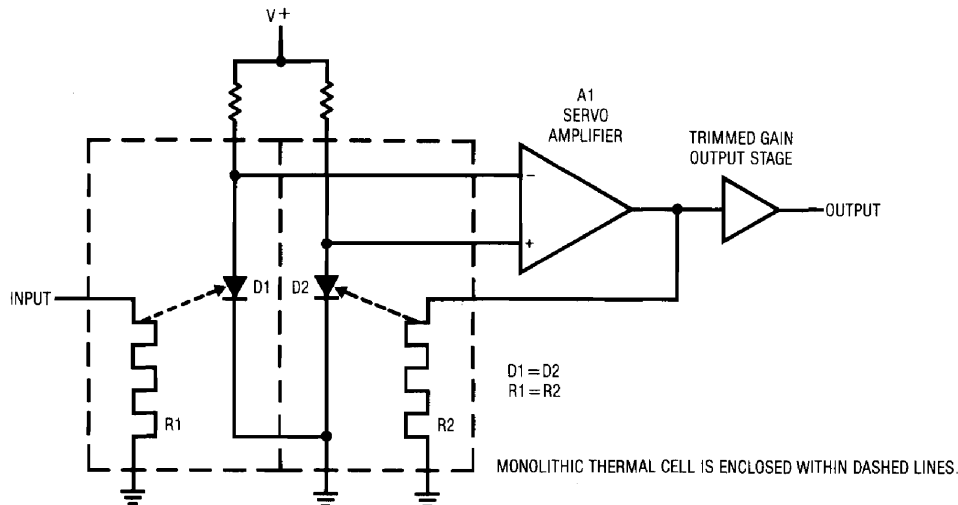


Figure 3. Simplified Monolithic Thermal RMS-DC Converter

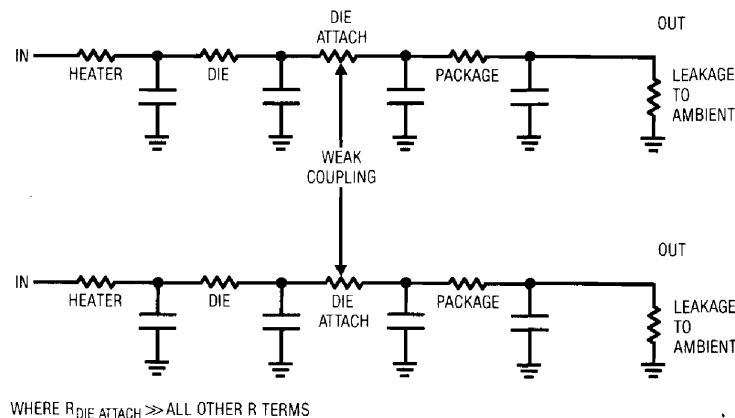


Figure 4. Simplified Electro-Analog of the LT1088

Application Note 22

Because the die attach resistance is so important (see Box Section, "Measuring Thermal Resistance") it must be carefully considered. Figure 5 shows results for various die attach methods. As might be suspected, die suspended in free air offer the highest thermal resistance, although the approach is impractical. Conversely, standard eutectic bonding gives low thermal resistance but is easy to produce. Another die attach method, air impregnated polymer, is nearly as good as air suspension, and is practical. The OTT™ process (Oracular Thermal Transfer) was developed to allow use of air impregnated polymer die attach. Figure 6 is a side-on die photo showing the results of OTT processing beneath the die. Large areas beneath the die are filled with air, resulting in the high thermal resistance noted in Figure 5. Sufficient amounts of polymer attach material ensure a reliable die attach.

OTT™ is a trademark of Linear Technology Corp.

Die Attach Type	Thermal Resistance°C Per Watt
Air Suspended	460
Air Impregnated Polymer	300
Epoxy/2 Mil Polymer Barrier	250
Glass-10 Mil	115
Epoxy/1 Mil Polymer Barrier	107
Eutectic	54

Figure 5 Thermal Resistance vs Die Attach Types



Figure 6. Side-On Chip Photo Details the Air Impregnated Die Attach Produced by the OTT Process. The Two Distinct Die Regions are Caused by Scribe and Break Operations.

Figure 7 is a die shot of one heater resistor-diode pair of the LT1088. The circular, concentric heater resistors promote evenly distributed, isothermal characteristics. The placement and aspect ratio of the heater rings is optimized for an even thermal flow across the die. The sensing diode is actually a paralleled quad located symmetrically about the die center. This quad arrangement provides improved temperature sensing characteristics over a single device. The separate heater rings allow the user to select either a 50Ω or 250Ω input. The test structure in the die center is not used. It is designed to offset effects described by Counts Theorem (see References). Note that the IC contains only the basic thermal components to maintain isothermal conditions. Inclusion of support circuitry would add thermally based error terms, degrading performance.

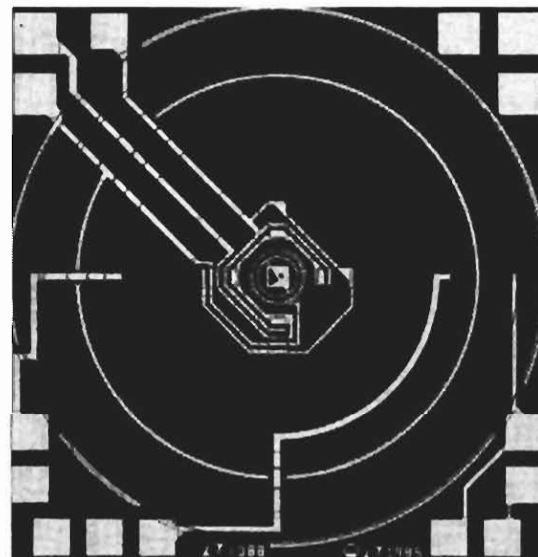


Figure 7. Die Photo of the LT1088 Showing 50Ω (inner ring) and 250Ω (outer ring) Heaters

Figure 8 shows a detailed circuit using the LT1088. Typical performance specifications are given in Figure 9. The LT1088's temperature sensing diodes are biased from the supply. A1, set up as a differential servo amplifier with a

gain of 9000, extracts the diode's difference signal and biases Q1. Q1 drives one of the LT1088's heaters, completing a loop. The 3300pF capacitor gives a stable roll-off. The 1.5M-0.022μF combination improves settling by reducing

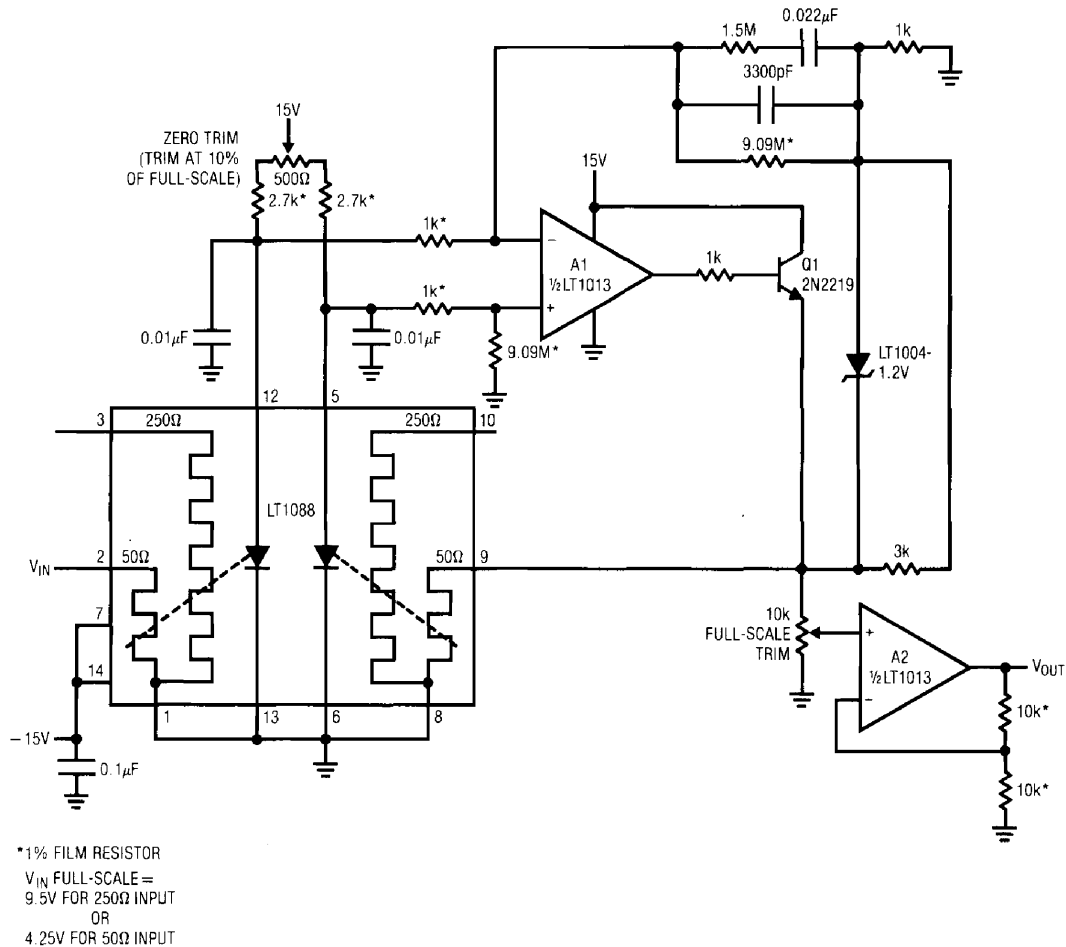


Figure 8. Practical Circuit for the LT1088

Accuracy:	Crest Factor:
50Ω Input	50Ω Input 50:1
DC to 50MHz 1% FS	250Ω Input 40:1
DC to 100MHz 2% FS	3dB Bandwidth 300MHz
250Ω Input	Full-Scale Settling Time (1%) 500ms
DC to 20MHz 1% FS	Input Voltage Range
Temperature Effect on Accuracy 100ppm/°C	50Ω Input 4.25V
Dynamic Range 20:1	250Ω Input 9.5V

Figure 9. Typical Specifications for Figure 8's Circuit

Application Note 22

gain during output slew. The square-law thermal gain of the LT1088 means overall loop gain is lower for small inputs. Normally, this would result in slow settling for values below about 10–20% of scale. The LT1004 1k-3k network is a simple breakpoint, boosting amplifier gain in this region to improve settling. A2, a gain trimmable output stage, serves to compensate for gain variations in the two sides of the LT1088. To trim the circuit, put in about a 10% scale DC signal (e.g., 1V for the 250 Ω input, 500mV for the 50 Ω input). Adjust the “zero trim” so that $V_{OUT} = V_{IN}$. Next, apply a full-scale DC input and set the “full-scale trim” to that value at the output. Repeat the trims until both are fixed well within 1% of full-scale. An alternate trim scheme involves applying no input, grounding Q1’s base and setting the “zero trim” until A1’s output is active. Then, unground Q1’s base and apply a full-scale input and trim the “full-scale” adjustment for that value at the output.

At frequencies above 10MHz, input connections require care. Parasitic inductance builds quickly in wire runs, so the LT1088’s input heater lead should be *directly* con-

nected to the source to be measured. It is also wise to shield the input line from the rest of the circuit. Figure 10 shows one way to do this. A simple copper RF shield isolates the circuitry from the input. The LT1088 is mounted so the input pin is as close as possible to the input connector pin. An additional precaution is to mount the 0.01 μ F bypass capacitors right at the LT1088 package. These units minimize the effects of RF pick-up by the temperature sensing diodes. Another layout concern involves thermal considerations. Because the LT1088’s operation depends on thermal symmetry, it is sensitive to external temperature gradients. This is particularly the case for small inputs which force the device to run very close to ambient temperature. The device should be mounted in an area which is isothermal and free of drafts. Power generating components should be kept away from the LT1088 and particular caution taken in fan cooled equipment. Under normal conditions no thermal baffle or enclosure is required. Under no circumstances should a heat sink be used.

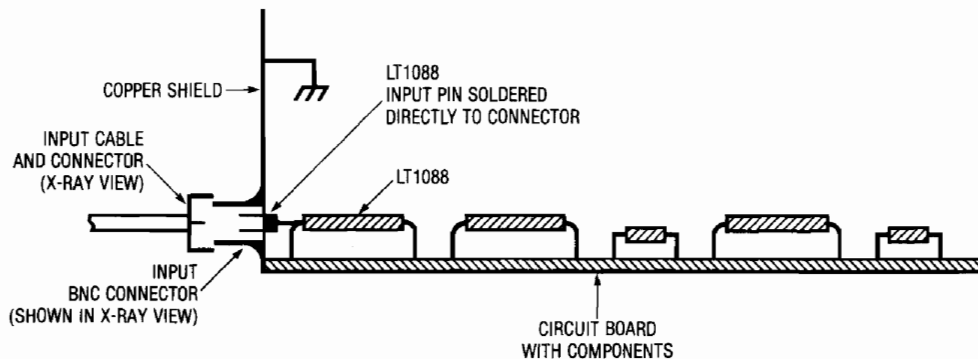


Figure 10. Recommended Layout

Figure 11 is a plot of output error vs input frequency using the 50Ω input at full-scale. There is no degradation of bandwidth for smaller inputs. Thermal transfer standards (Fluke Model 540B with A-55 converters) certified to 50MHz were used as references. The data above 50MHz was also taken with these references, although the individual units used had not been certified at these frequencies. The accuracy of units of this type which have been certified is normally inside the tolerances listed, so there is good probability the data is valid. Figure 12 is a similar plot but over extended ranges of frequency and flatness. Unfortunately, equipment and test set-up limitations imposed uncertainties at the highest frequencies, but the data probably approximates actual performance. The peaking followed by the steep roll-off is most likely due to the LT1088's high frequency limitations. In particular, bond wire inductance becomes increasingly significant as frequency increases. Also, capacitance between the heater and sensing diode permits RF pumping of the

diode, almost certainly causing deleterious results. The 1% error point using the 250Ω range is lower. The parasitics described combine with the higher input voltage swing to limit 1% bandwidth to about 20MHz.

The low end of the frequency spectrum is limited by loop time constants. For Figure 8's values, the circuit begins to follow the input below about 50Hz. Lower frequency operation requires longer loop time constants (e.g., increasing the 3300pF value), increasing settling time.

Crest factor performance is set by IC breakdown limits and the usable low input power range. Breakdown limits are a function of processing. The usable low input power range is a basic signal-to-noise conflict. Low input power produces small amounts of signal. This makes accurate, stable discrimination between desired inputs and ambient thermal phenomena uncertain and noisy.

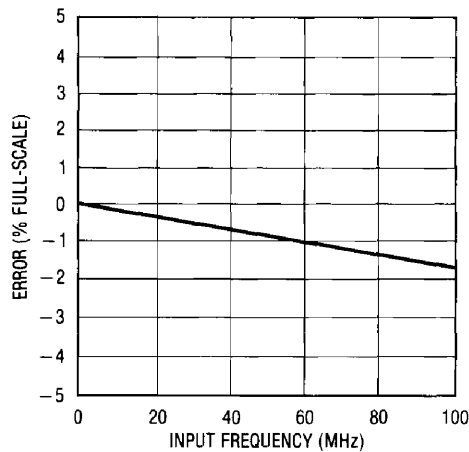


Figure 11. Error vs Frequency

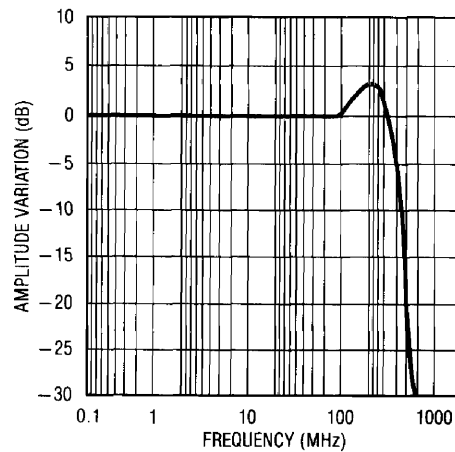


Figure 12. Extended Plot of LT1088 Frequency Response

Application Note 22

Step response is determined by the servo electronics roll-off. Figure 13 shows response for a full-scale step into the 250Ω heater. Loop response is nicely damped. The small glitching at the beginning of the step is due to the gain breakpoint in A1's feedback loop. Figure 14 shows the negative going step. Although the response appears clean (again, the gain glitch is due to A1's breakpoint network), Figure 15 reveals the loop coming to a new value well after it appears to have settled. This photo is a slower version of Figure 14 (initial negative going step is just visible at the extreme left). Almost 5 seconds after settling apparently occurs the loop abruptly assumes a new value. This effect

is due to the loop being driven into saturation. The allowable low range operating area (defined by the dynamic range specification) has been exceeded, forcing the servo into saturation. This causes thermal imbalances in the LT1088, resulting in the extended length of time before the loop becomes active again.† Figure 16 shows response when the input is kept within the specified operating range. Settling on both edges is clean, and the loop quickly assumes and maintains its final value.

*As an interesting exercise, consider what would happen if the servo amplifier could somehow extract, as well as supply, heat to the system.

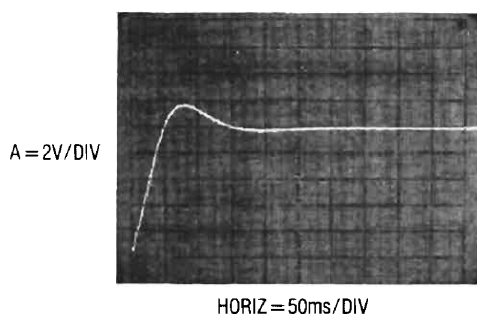


Figure 13. Loop Response for Input Step

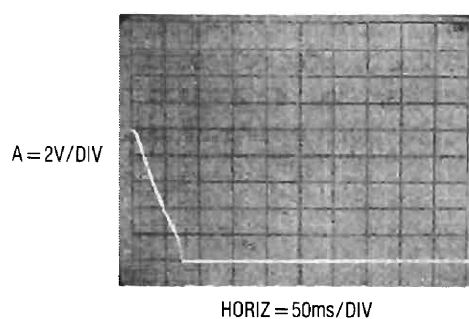


Figure 14. Falling Edge with Loop Driven into Cut-Off

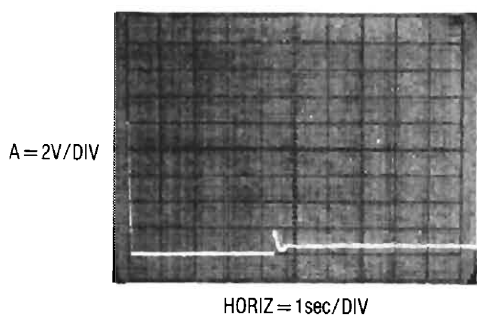


Figure 15. Loop Recovery from Cut-Off

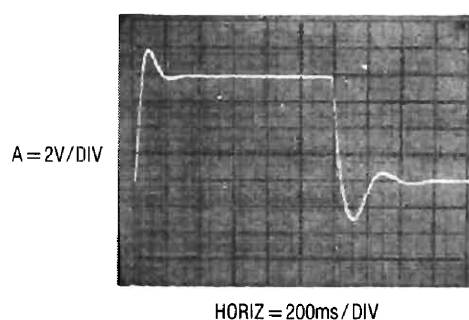


Figure 16. Loop Response with Input Kept in the Linear Region

Some applications may drive the LT1088 outside its operating range, forcing thermal imbalance. If fast settling is required, Figure 17's circuit is useful. This scheme speeds settling by applying an open loop heating correction when thermal imbalance occurs. When the input (Trace A, Figure 18) steps negatively, A1's output (Trace B) slews. Loop delays cause A1 to overshoot, turning off

heater drive and thermally unbalancing the LT1088. Diode steering at the LT1010 buffer's output sinks current from the 250Ω input heater (Trace C). This produces heating, tending to compensate the thermal imbalance, thereby decreasing settling time. Trace D, A2's output, settles fairly quickly after it recovers from the open loop correction.

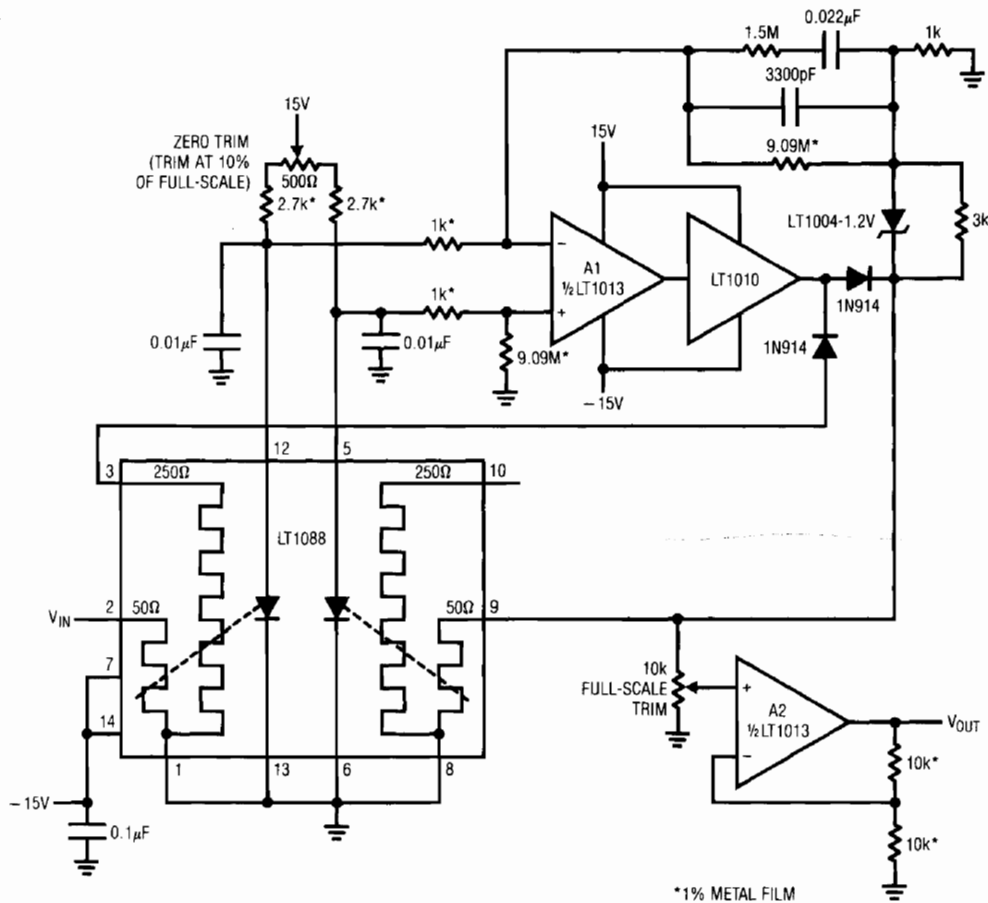


Figure 17. Fast Recovery Circuit (diode steering provides compensation for thermal imbalance)

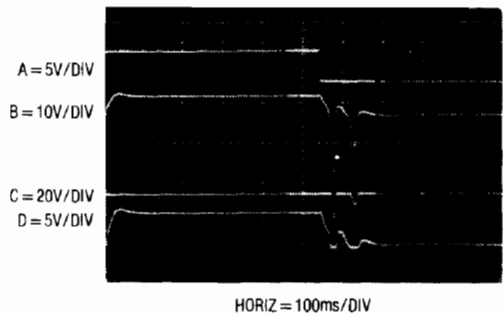


Figure 18. Waveforms for Fast Recovery Circuit

Application Note 22

Any study of LT1088 dynamics must consider that although the output voltage has settled, internal die temperature may still be moving towards final value. It is important to distinguish between voltage and thermal dynamics when observing LT1088 operation.

Most LT1088 failures will be caused by excessive heater drive. Input power (25°C) is specified at 375mW continuous with 30 second excursions to 435mW permitted. These figures are derated by $-3\text{mW}/^\circ\text{C}$ above 25°C. Figure 19 plots safe operating limits for input duty cycle vs input voltage. Accidental heater overdrives can damage or destroy the LT1088. In situations where overdrive may occur, some form of heater protection should be employed.

Figure 20 shows a heater protection circuit which responds quickly enough to prevent damage from most overloads. C1's input is connected to the output of the LT1088 servo circuit. If the LT1088 circuit's output exceeds the threshold at C1's other input, C1 trips, discharging the $2\mu\text{F}$ capacitor. This causes C2's output to go low, energizing the relay and breaking the heater circuit. The 560k resistor provides a long recharge for the capacitor, preventing "chattering" action. This arrangement's speed of response is limited by the RMS circuit's slew rate, about $0.2\text{V}/\text{ms}$. For reasonable overloads, the LT1088's temperature increases about $1^\circ\text{C}/\text{ms}$. A 10V LT1088 output step takes 50ms, causing a temperature rise of about 50°C .

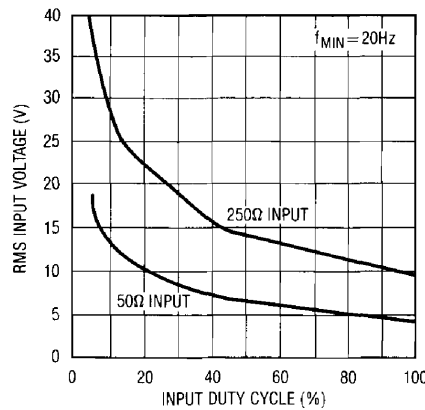


Figure 19. LT1088 Safe Operating Limits

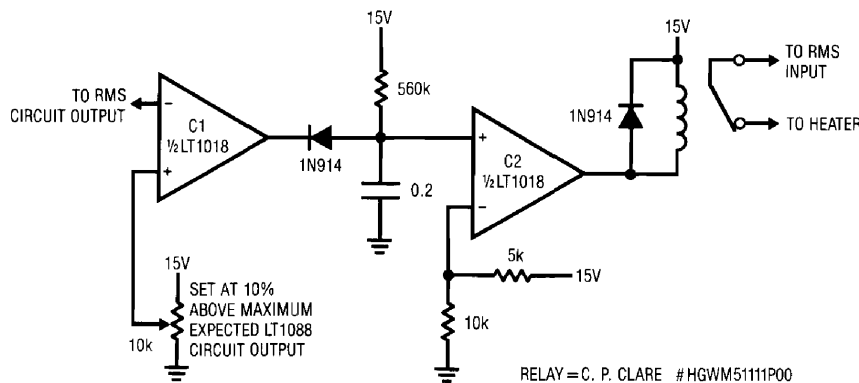


Figure 20. Servo-Sensed Heater Protection Circuit

Severe overloads will cause faster heating, and this circuit may not act quickly enough to prevent damage. Figure 21's circuit is faster, but requires a trim. It works by directly sensing the temperature of the LT1088, instead of the servo amplifier output. Circuit action is similar to Figure 20, except that the input is taken from the LT1088's input temperature sensing diode. Figure 22 shows waveforms. Excessive drive to the LT1088 (Trace A, Figure 22) forces the servo amplifier (Trace B) into slew. The sensing diode, responding more quickly than the servo, causes the circuit to switch the relay (Trace C), removing heater drive in 15ms. Because loop response lags temperature, the servo amplifier's output peaks at only 6V, about one-third of the input step. This circuit has the disadvantage of requiring a trim, due to initial diode tolerances. To trim, measure diode output at 25°C and set

C1's negative input to the desired temperature cut-off point. Assume a diode slope of 1.8mV/°C.

Some applications may require buffering the LT1088's relatively low input impedance. This is not easy if the device's wide bandwidth and accuracy must be preserved. With an LT1010 buffer, bandwidths in the low megahertz region are achievable. Figure 23's circuit, a FET input, complementary emitter follower output design, extends bandwidth out to 25MHz. If gain is desired, Figure 24 furnishes low megahertz performance at a gain of ten. Figure 25's design, although complex, has 32MHz bandwidth at a gain of ten. Detailed discussion of Figures 24 and 25 appears in Application Note 21, "Composite Amplifiers." Figure 26's table summarizes performance of the buffer amplifiers.

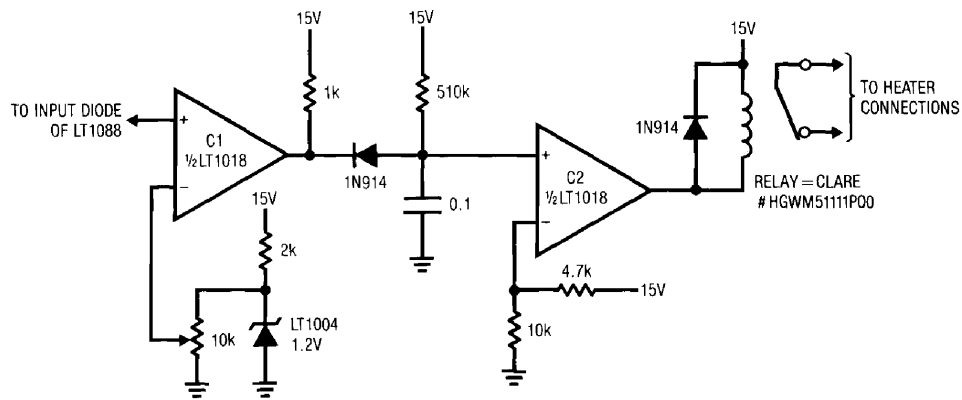


Figure 21. Diode Sensed Heater Protection Circuit

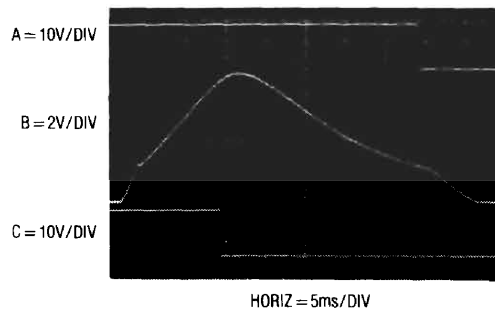


Figure 22. Response of Diode Sensed Heater Protection Circuit

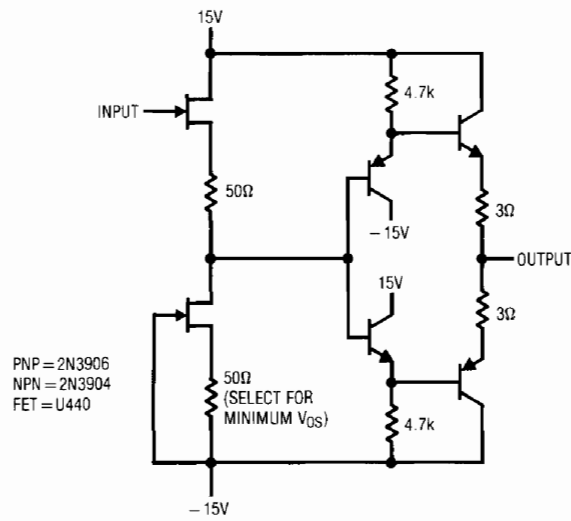


Figure 23. Input Buffer for the LT1088

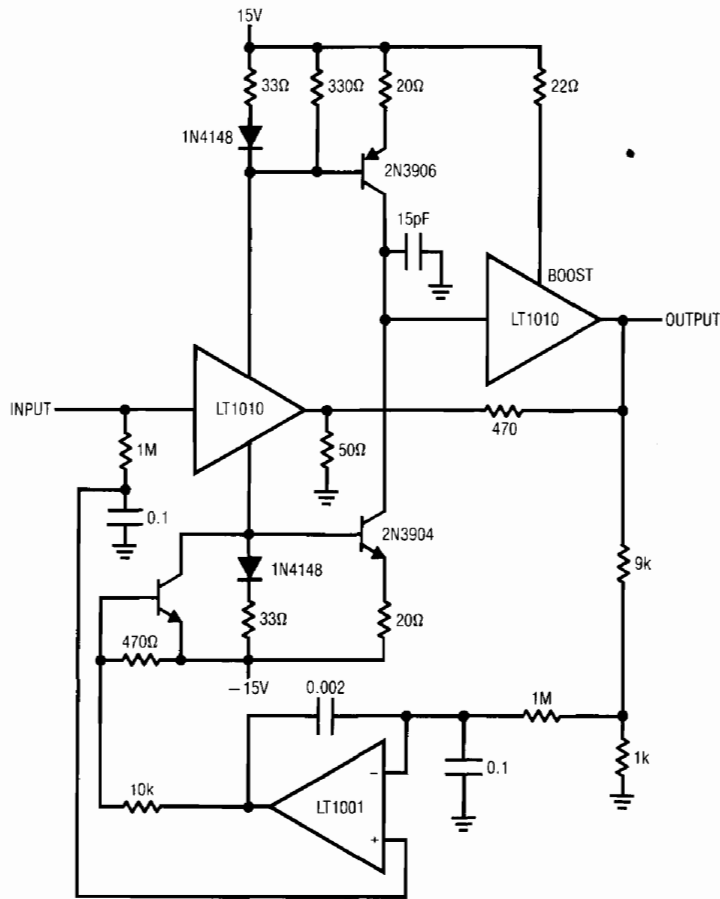


Figure 24. Fast, "Current Mode" Amplifier-Buffer

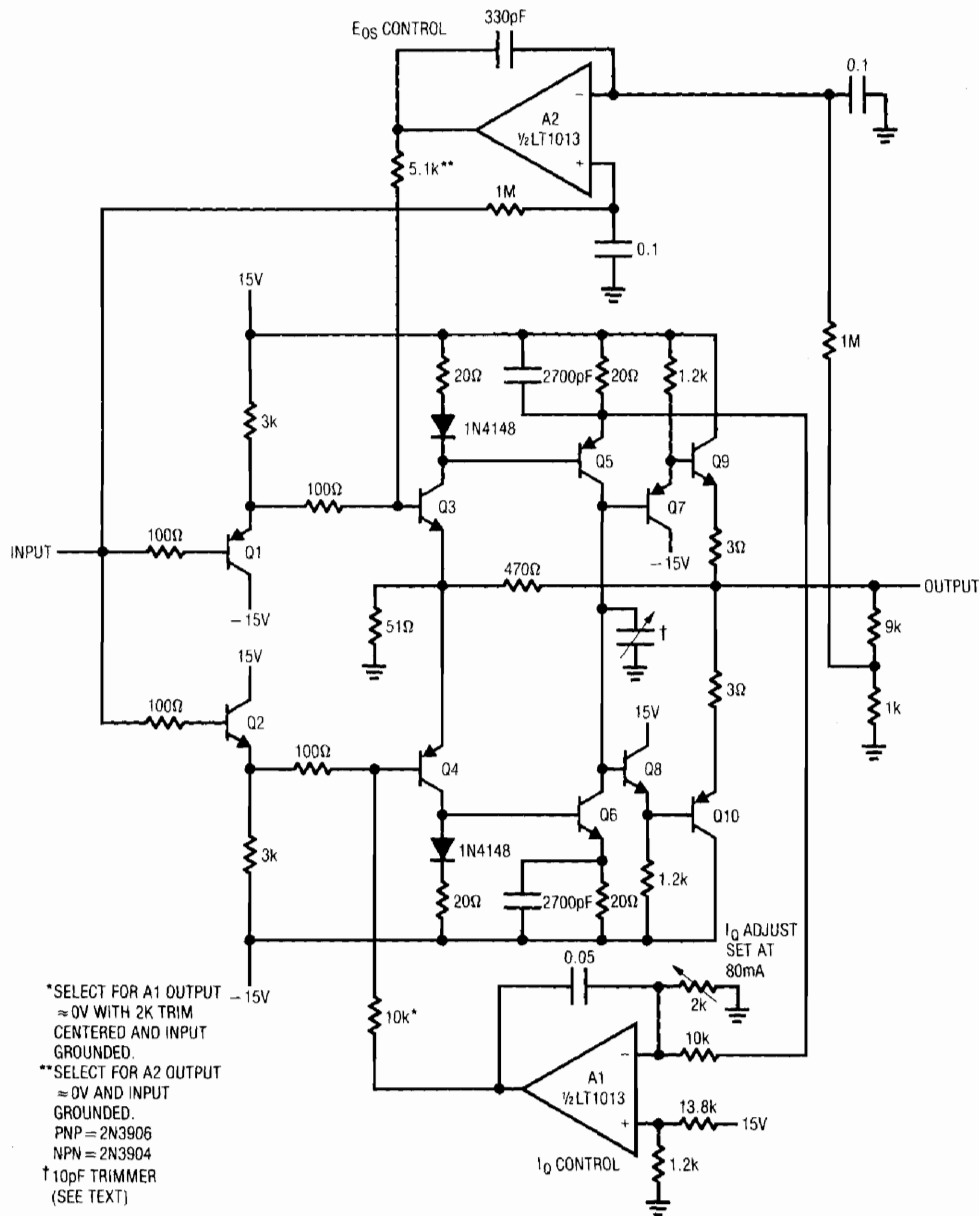


Figure 25. Ultra-Wideband "Current Mode Feedback" Buffer Amplifier

Type of Buffer	Slew Rate	1% Error Bandwidth	
		250Ω Load (±10V _{OUT})	50Ω Load (±5V _{OUT})
Discrete—A = 10	3000V/μs	25MHz	32MHz
LT1010 Based—A = 10	100V/μs	0.75MHz	2MHz
Discrete—A = 1	2000V/μs	15MHz	25MHz
LT1010 Based—A = 1	100V/μs	0.75MHz	2MHz

Figure 26. Summary of Buffer Characteristics

Application Note 22

Applications for the LT1088's wideband capability exist in AC voltmeters, SCR power monitoring, wideband AGC, noise measurement and RF leveling loops. Figure 27 shows a 10MHz RF leveling loop. The RF input is applied to the AD539 wideband multiplier. The multiplier's output drives an RF amplifier. The discrete transistors furnish gain with the LT1010 serving as an output buffer. The LT1012 DC stabilizes the stage (for operating details of this circuit, see Application Note 21). The RF amplifier's output is converted to DC by the LT1088 based RMS-DC converter. A servo amplifier compares this output with a

settable DC reference and biases the multiplier's control channel, completing a loop. The 0.33 μ F capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo. The loop maintains the output's 10MHz RMS amplitude at the DC reference's value. Changes in load, input, power supply and other variables are rejected. Figure 28 shows loop response for a step test signal injected at the servo amplifier's positive input (Trace A). Response (Trace B) is clean, with settling occurring in about a second.

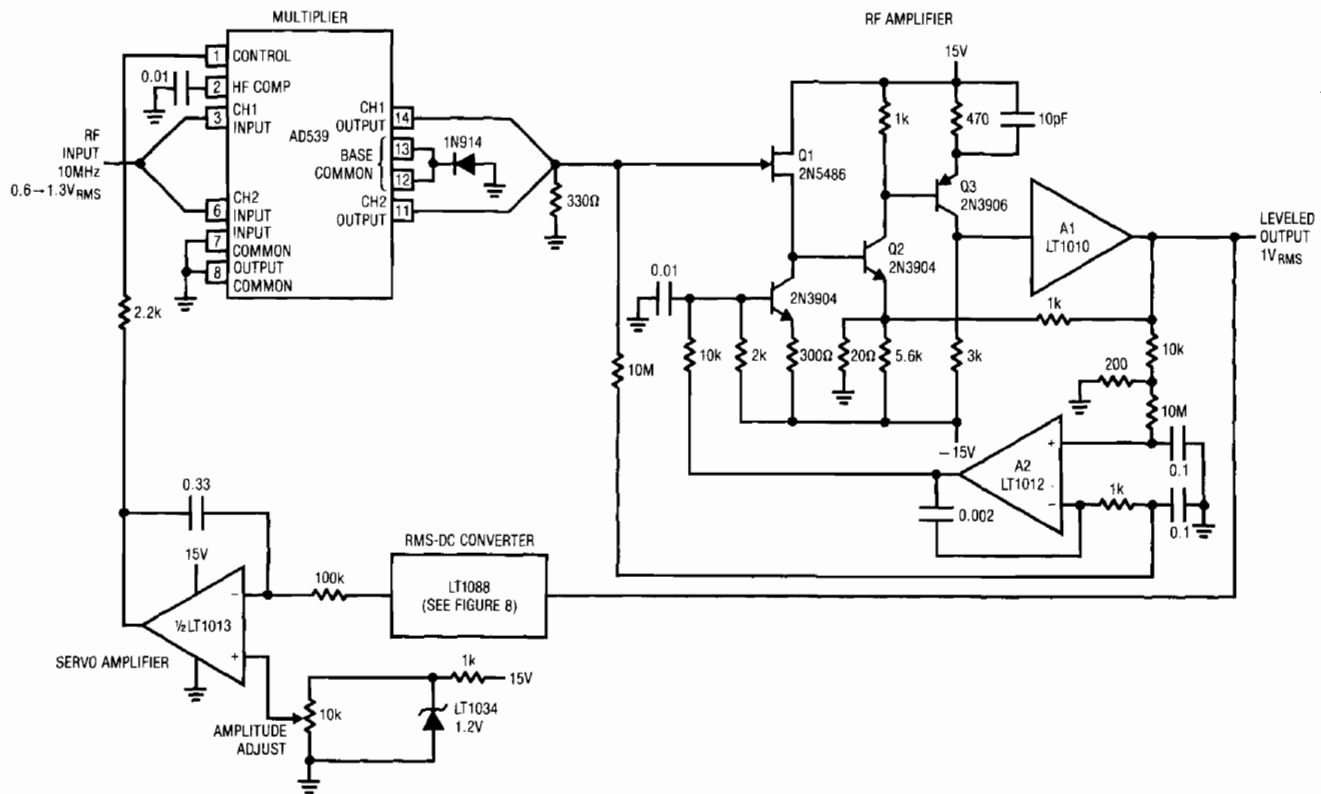


Figure 27. RF Leveling Loop

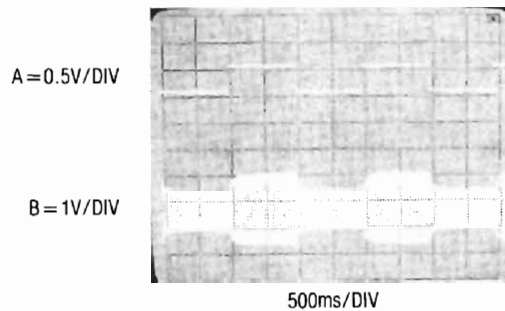


Figure 28. RF Leveling Loop Response

BOX SECTION

Measuring Thermal Resistance

Establishing, maintaining and verifying proper thermal resistance between the LT1088 and ambient is extremely important to its operation. Because thermal resistance is a gain term, it must be constant with time, cycling and power level. Additionally, it must fall within limits. Low thermal resistance results in poor sensitivity to downscale inputs, limiting dynamic range. Too high a thermal resistance causes excessive die heating, leading to failure.

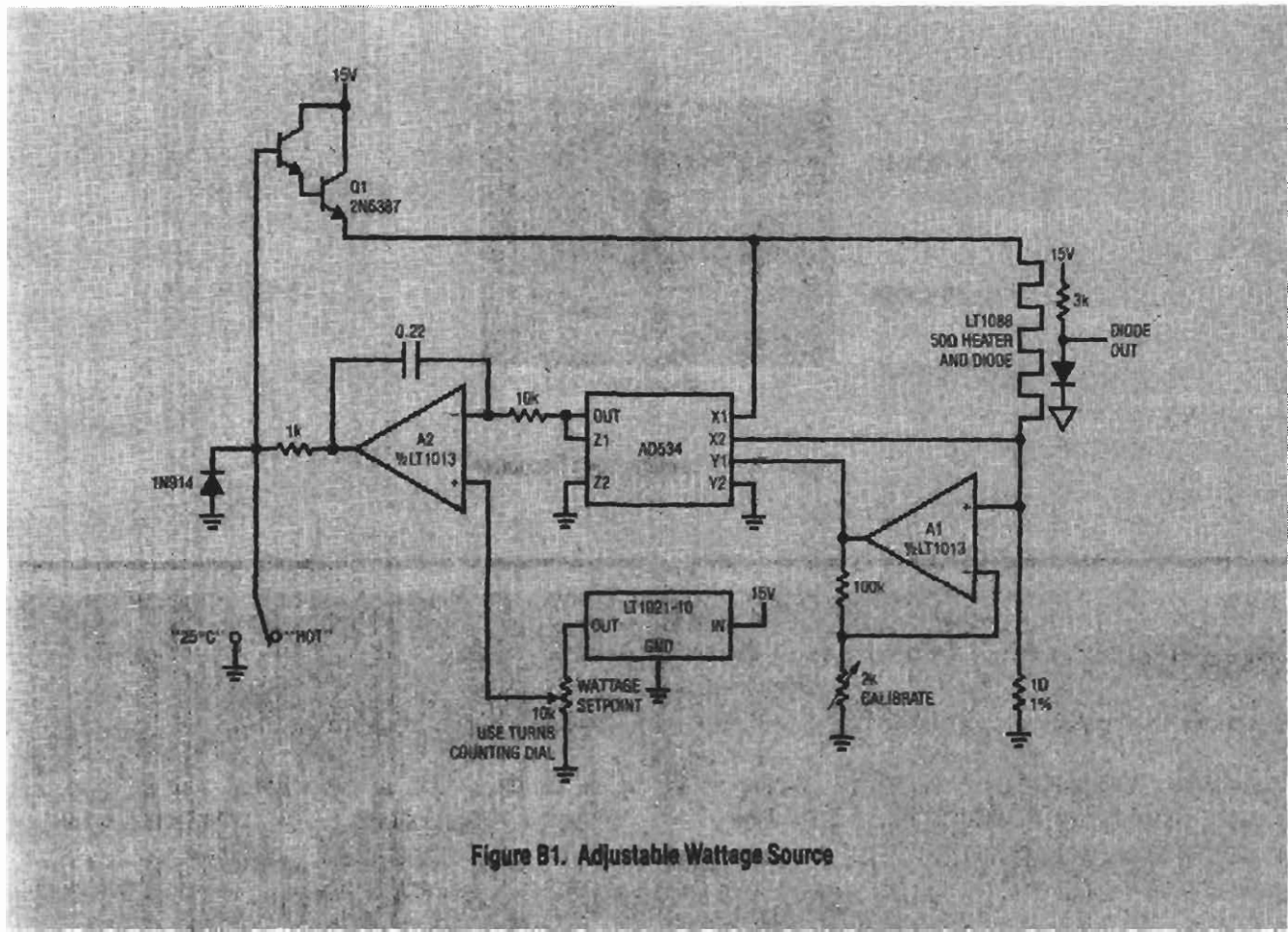
Thermal crosstalk, the heat conduction between the two die, must be minimized. Such thermal conduction between die lowers available gain, degrading performance for small inputs.

Ensuring proper thermal resistance for both cases requires an accurate measurement technique. Figure B1 shows a circuit which reliably measures thermal resistance. It works by supplying constant *wattage* to the LT1088 heater, regardless of its resistance. Because heater resistance moves with die temperature, the circuit must continually control the $E \times I$ product supplied to the heater. It does this by measuring heater current and forcing voltage to keep the $E \times I$ product at a constant, calibrated value. The resultant die temperature rise, picked up

by the diode sensor, allows thermal resistance to be determined. A1, measuring heater current across the 1Ω shunt, feeds the Y input of an analog multiplier. The voltage across the heater is differentially sensed at the multiplier's X input. The multiplier's $E \times I$ product output is compared to a scaled, adjustable reference at A2. A2's output biases Q1, closing a loop around the heater. The $0.22\mu\text{F}$ capacitor stabilizes the loop. To trim this circuit, put a 50Ω , 1W resistor in place of the LT1088 heater. Next, adjust the 2k potentiometer so the measured heater wattage (E across heater times I through the 1Ω shunt) corresponds to the voltage at the potentiometer wiper. Scale factor will be 10V/W . Disconnect the 50Ω resistor and the circuit is ready for use.

To measure thermal resistance, adjust the wattage control for 350mW, place the switch in the "25°C" position and read the diode potential. Then, switch to "hot" and read the diode voltage when it has settled. Assuming $1.8\text{mV}/^\circ\text{C}$, calculate the thermal resistance in $^\circ\text{C/W}$. Thermal crosstalk is measured the same way, except that the sensing diode and heater are not on the same die.

Application Note 22



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4. Ott, W.E., "A New Technique of Thermal RMS Measurement." IEEE Journal of Solid State Circuits, December, 1974.
5. Counts Theorem, propounded by L.W. Counts at the 1986 ISSCC, states that $9 \neq 10$.
6. RMS to DC Conversion Application Guide, Analog Devices, Norwood, Massachusetts.
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Micropower Circuits for Signal Conditioning

Jim Williams

Low power operation of electronic apparatus has become increasingly desirable. Medical, remote data acquisition, power monitoring and other applications are good candidates for battery driven, low power operation. Micropower analog circuits for transducer-based signal conditioning present a special class of problems. Although micropower ICs are available, the interconnection of these devices to form a functioning micropower circuit requires care. (See Box Sections, "Some Guidelines for Micropower Design and an Example" and "Parasitic Effects of Test Equipment on Micropower Circuits.") In particular, trade-offs between signal levels and power dissipation become painful when performance in the 10-bit to 12-bit area is desirable. Additionally, many transducers and analog signals produce

inherently small outputs, making micropower requirements complicate an already difficult situation. Despite the problems, design of such circuits is possible by combining high performance micropower ICs with appropriate circuit techniques.

Platinum RTD Signal Conditioner

Figure 1 shows a simple circuit for signal conditioning a platinum RTD. Correction for the platinum sensor's nonlinear response is included. Accuracy is 0.25°C over a 2°C to 400°C sensed range. One side of the sensor is grounded, highly desirable for noise considerations. For a 2°C sensed temperature, current consumption is $250\mu\text{A}$, increasing to $335\mu\text{A}$ for a 400°C sensed temperature.

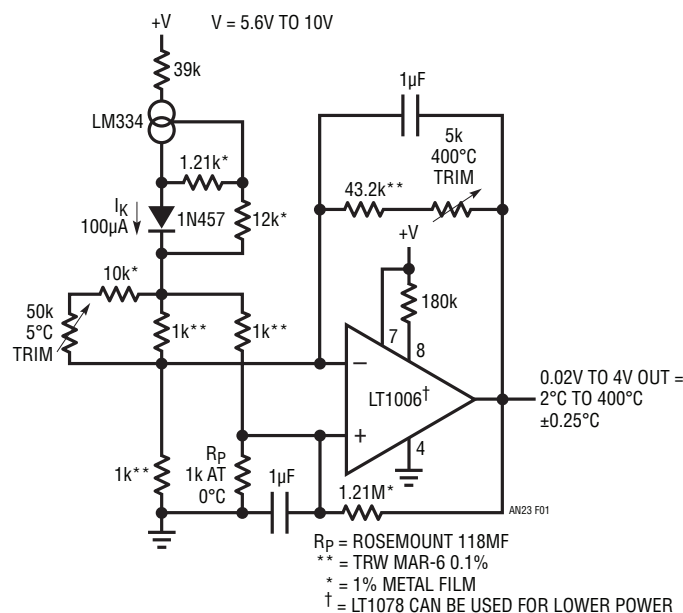


Figure 1. Platinum RTD Signal Conditioner with Curvature Correction

Application Note 23

The platinum sensor is placed in a current driven bridge with the 1k resistors. The LM334 current source drives the bridge and its associated resistors set a 100 μ A operating level. The diode provides temperature compensation (see LM334 data sheet). The 39k resistor deliberately sustains voltage drop, minimizing LM334 die temperature rise to ensure good temperature tracking with the diode. The 100 μ A current is split by the bridge. This light current saves power, but restricts the platinum sensor's output to about 200 μ V/ $^{\circ}$ C. The circuit's 0.25 $^{\circ}$ C accuracy specification requires the LT[®]1006 low power precision op amp for stable gain. The LT1006 takes the signal differentially from the bridge to provide the circuit's output. Normally, the platinum sensor's slightly nonlinear response would cause several degrees error over the sensed temperature range. The 1.2M resistor gives slight positive feedback to correct for this. The amplifier's negative feedback path dominates, and the configuration is stable. The 1 μ F capacitors give a high frequency roll-off and the 180k resistor programs the LT1006 for 80 μ A quiescent current.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432) for R_p. Set the box to the 5 $^{\circ}$ C value (1019.9 Ω) and adjust the "5 $^{\circ}$ C trim" for 0.05V output at the LT1006. Next, set the box for the 400 $^{\circ}$ C value (2499.8 Ω) and adjust the "400 $^{\circ}$ C trim" for 4.000V output. Repeat this sequence until both points are fixed. The resistance values given are for a nominal 1000.0 Ω (0 $^{\circ}$ C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 1000.0 Ω . This deviation, which is manufacturer-specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Thermocouple Signal Conditioner

Figure 2 is another temperature sensing circuit, except the transducer is a thermocouple. Accuracy is within 1.5 $^{\circ}$ C over a 0 $^{\circ}$ C to 60 $^{\circ}$ C sensed temperature and current consumption is about 125 μ A.

Thermocouples are inexpensive, have low impedances and feature self-generating outputs. They also produce low level outputs and require cold junction compensation, complicating signal conditioning. The bridge network, composed of the thermistor and R1-R4, provides cold junction compensation with the LT1004 acting as a voltage reference. The lithium battery noted allows the bridge to float and the thermocouple to be ground referred, eliminating the requirement for a differential amplifier. For the battery specified, life will approach 10 years. This is a good way to avoid the additional power drain of a multi-amplifier differential stage. The LT1006 is set up with a gain scaled to produce the output shown and the 270k resistor programs it for low current drain. Note that this circuit requires no trims.

Sampled Strain Gauge Signal Conditioner

Strain gauge bridge-based transducers present a challenge where low power operation is needed. The 350 Ω impedance combined with low signal outputs (typically 1mV to 3mV output per volt of drive) presents problems. Even with only 1V of drive, bridge consumption still approaches 3mA. Dropping drive to 100mV reduces current to acceptable levels, but precludes high accuracy operation due to the miniscule output available. In many situations, continuous transducer information is unnecessary and sampled operation is viable. Short sampling duty cycle

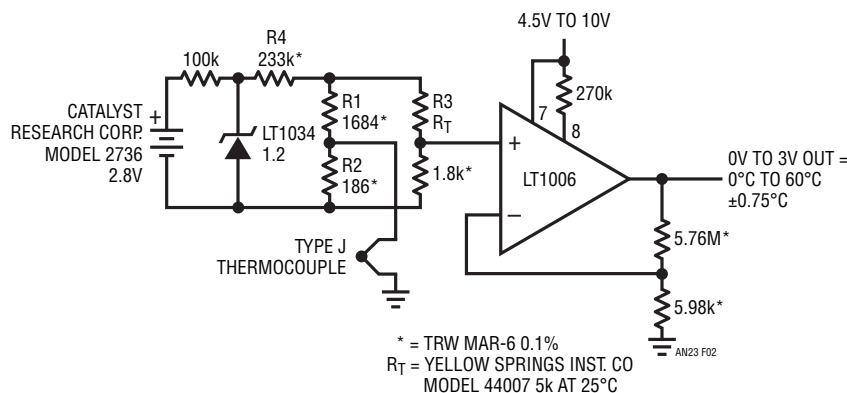


Figure 2. Thermocouple Signal Conditioner with Cold Junction Compensation

permits high current bridge drive while maintaining low power operation. Figure 3 uses such a scheme to achieve dramatic power saving in a strain gauge bridge application (for a discussion of sampled operation considerations, see Box Section B, “Sampling Techniques and Components for Micropower Circuits”).

In this circuit, Q2 is off when the “sample command” is low. Under these conditions only A4 and the CD4016 receive power, and current drain is inside 125 μ A. When the sample command is pulsed high, Q2’s collector (Trace A, Figure 4) goes high, providing power to all other circuit elements. The 10 Ω -1 μ F RC at the LT1021 prevents the strain bridge

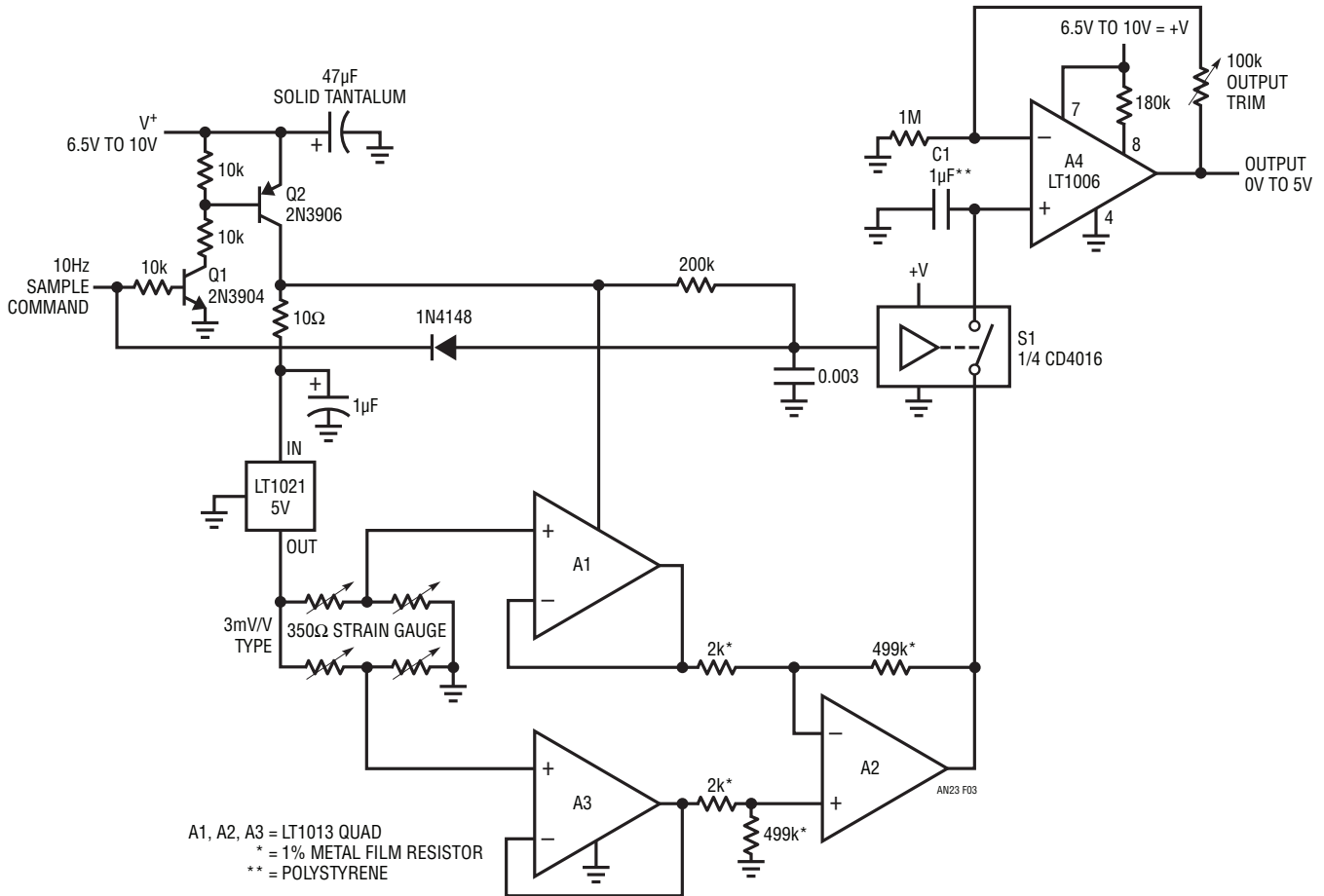


Figure 3. Sampled Strain Gauge Bridge Signal Conditioner

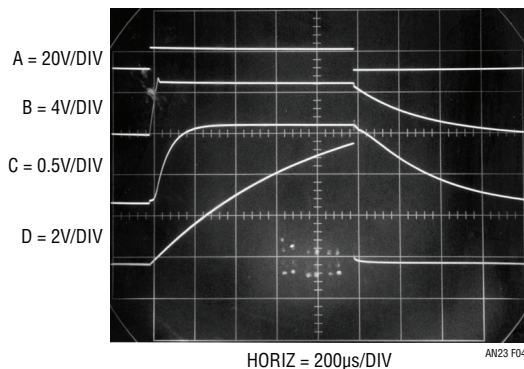


Figure 4. Waveforms for the Sampled Strain Gauge Signal Conditioner

Application Note 23

from seeing a fast rise pulse which could cause long-term transducer degradation. The LT1021-5 reference output (Trace B) drives the strain bridge, and differential amplifier A1-A3's output appears at A2 (Trace C). Simultaneously, S1's switch control input (Trace D) ramps toward Q2's collector. At about one-half Q2's collector voltage (in this case just before mid-screen) S1 turns on, and A2's output is stored in C1. When the sample command drops low, Q2's collector falls, the bridge and its associated circuitry shut down and S1 goes off. C1's stored value appears at gain scaled A4's output. The RC delay at S1's control input ensures glitch-free operation by preventing C1 from updating until A2 has settled. During the 1ms sampling phase, supply current approaches 20mA, but a 10Hz sampling rate cuts effective drain below 200 μ A. Slower sampling rates will further reduce drain, but C1's droop rate (about 1mV/100ms) sets an accuracy constraint. The 10Hz rate provides adequate bandwidth for most transducers. For 3mV/V slope factor transducers, the gain trim shown allows calibration. It should be rescaled for other types. This circuit's effective current drain is about 300 μ A and A4's output is accurate enough for 12-bit systems.

Strobed Operation Strain Gauge Bridge Signal Conditioner

Figure 5's circuit also switches power to minimize strain bridge caused losses, but is not intended for continuously sampled operation. This circuit is designed to sit in the quiescent state for long periods with relatively brief on times. A typical application would be remote weight information in storage tanks where weekly readings are sufficient. This circuit has the advantage of not requiring a differential amplifier, despite the strain bridge's floating output. Additionally, it provides almost full rated drive to the strain bridge, enhancing accuracy. Quiescent current is about 150 μ A with on-state current typically 50mA.

With Q1's base unbiased, all circuitry is off except the LT1054 plus-to-minus voltage converter, which draws a 150 μ A quiescent current. When Q1's base is pulled low, its collector supplies power to A1 and A2. A1's output goes high, turning on the LT1054. The LT1054's output (Pin 5) heads toward -5V and Q2 comes on, permitting bridge current to flow. To balance its inputs, A1 servo controls the LT1054 to force the bridge's midpoint to 0V.

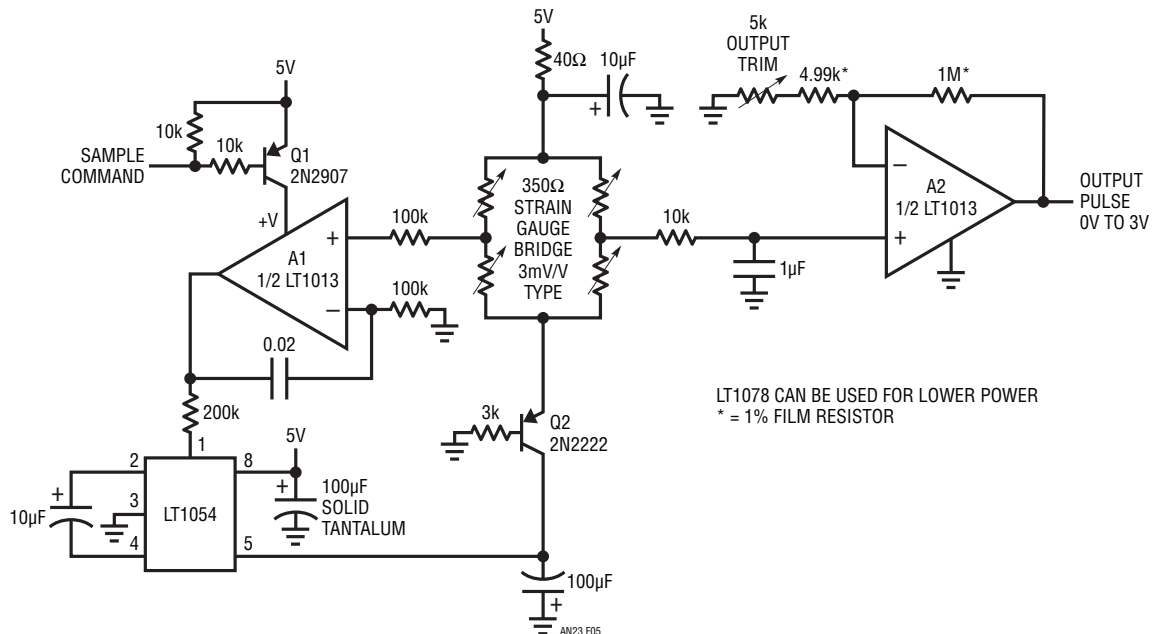


Figure 5. Strobed Power Strain Bridge Signal Conditioner

The bridge ends up with about 8V across it, requiring the 100mA capability LT1054 to sink about 24mA. The 0.02 μ F capacitor stabilizes the loop. The A1-LT1054 loop negative output sets the bridge's common mode voltage to zero, allowing A2 to take a simple single-ended measurement. The "output trim" scales the circuit for 3mV/V type strain bridge transducers, and the 100k-0.1 μ F combination provides noise filtering.

Thermistor Signal Conditioner for Current Loop Application

4mA to 20mA "current loop" control is common in industrial environments. Circuitry used to modulate transducer data into this loop must operate well below the 4mA minimum current.

Figure 6 shows a complete 2-wire thermistor temperature transducer interface with a 4mA to 20mA output. Over a 0°C to 100°C range, accuracy is $\pm 0.3^\circ\text{C}$ and the circuit is current loop powered. No external supply is required. The LM134 current source absorbs the 40V input, preventing

the LTC1040 from seeing too high a supply potential. It does this by fixing the current well below the 4mA loop minimum. The LTC1040 (detailed data on this device appears in Box Section B, "Sampling Techniques and Components for Micropower Circuits") senses the YSI thermistor network output and forces this voltage across the output resistor to set total circuit current. Current is adjusted by varying the gate voltage on the 2N6657 FET. Note that the comparator output operates in pulse-width modulation mode, with the FET gate voltage filtered to DC by the 1M-1 μ F combination. An important LTC1040 feature is that very little current, on the order of nanoamperes, flows from the V⁻ supply. This allows the V⁻ supply to be connected to ground with negligible current error in the output sensing resistor. The differential input of the LTC1040 can sense the current through R_{OUT} because its common mode range includes the V⁻ supply. Trims shown are for 0°C and 100°C and are made by exposing the thermistor to those temperatures or by electrically simulating the conditions (see manufacturer's data sheet).

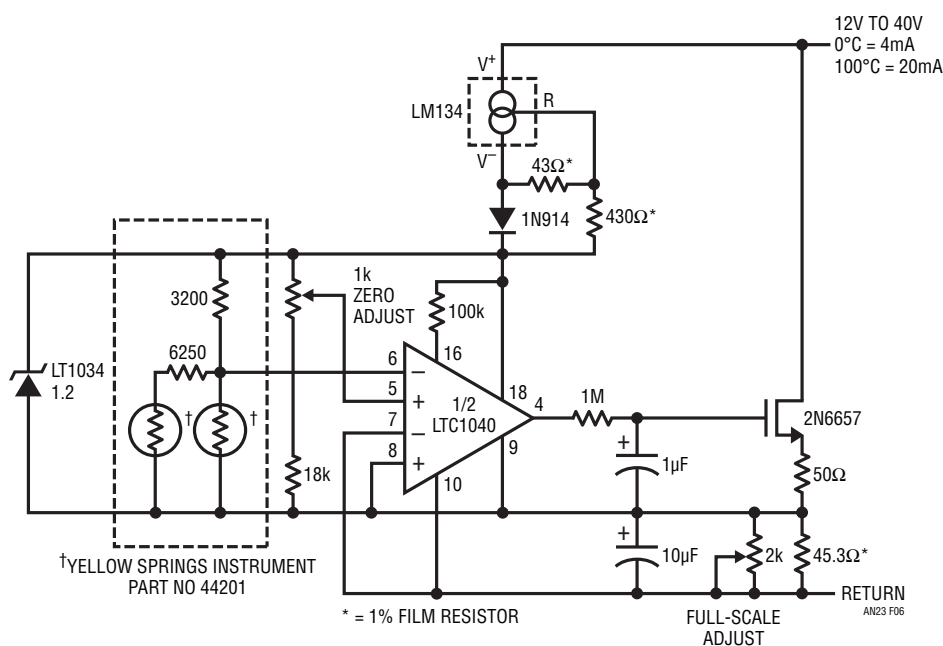


Figure 6. Thermistor-Based Current Loop Signal Conditioner

Application Note 23

Microampere Drain Wall Thermostat

Figure 7 shows a battery-powered thermostat using the LTC1041 (see Box Section B for details on this device). Temperature is sensed using a thermistor connected in a bridge with a potentiometer to set the desired temperature.

The bridge is not driven from the battery but from Pin 7 on the LTC1041. Pin 7 is the pulsed power (V_{PP}) output and turns on only while the LTC1041 is sampling the inputs. With this pulse technique, average system power consumption is quite small. In this application the total system current is below $1\mu A$! This is far less than the self discharge rate of the battery, meaning battery life is shelf life limited. A lithium battery will run this circuit for 10 to 20 years.

An external RC network sets the sampling frequency. When an internal sampling cycle is initiated, power is turned on to the comparators and to the V_{PP} output. The analog inputs are sampled and the resultant outputs are stored in CMOS latches. Power is then switched off although the outputs are maintained. The unlocked CMOS logic consumes almost no DC current. The sampling process takes approximately $80\mu s$. During this $80\mu s$ interval, the LTC1041 draws typically $1.7mA$ of current at $V^+ = 6V$. Because the sample rate is low, average power is extremely small.

The low sample rate is adequate for a thermostat because of the low rate of change normally associated with temperature.

A power MOSFET in a diode bridge switches 26VAC to the heater control circuitry. The MOSFET is a voltage controlled device with no DC current required from the battery.

The voltage from DELTA (Pin 5) to GND (Pin 4) sets the dead-band. Dead-band is desirable to prevent excessive heater cycling. The dead-band equals two times DELTA and is independent of both V_{IN} (Pin 3) and SET POINT (Pin 2). This means that as the SET POINT is varied, the dead-band is fixed at two times DELTA. Conversely, as dead-band is varied, SET POINT does not move.

Freezer Alarm

Figure 8 shows a very simple configuration for a freezer alarm. Such circuits are used in industrial and home freezers as well as refrigerated trucks and rail cars. The LTC1042 is a sampled operation window comparator (for details on this device see Box Section B). The $10M-0.05\mu F$ combination sets a sample rate of 1Hz, and the bridge values program the internal window comparator for the outputs shown. For normal freezer operation, Pin 1 is high and Pin 6 is low. Overtemperature reverses this state and can trigger an alarm. Circuit current consumption is about $80\mu A$.

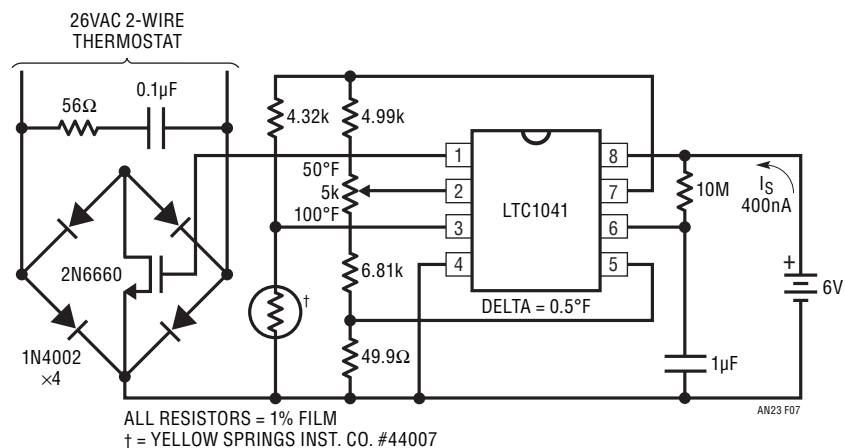


Figure 7. Wall Type Thermostat

12-Bit A/D Converter

Integrating A/D converters with low power consumption are available. Although capable of 12-bit measurements, they are quite slow, typically in the 100ms range. Higher speeds require a successive approximation (SAR)

approach. No commercially produced 12-bit SAR converter features micropower (e.g., below 1mA) capability at the time of writing. Figure 9's design converts in 300 μ s, while consuming only 890 μ A.

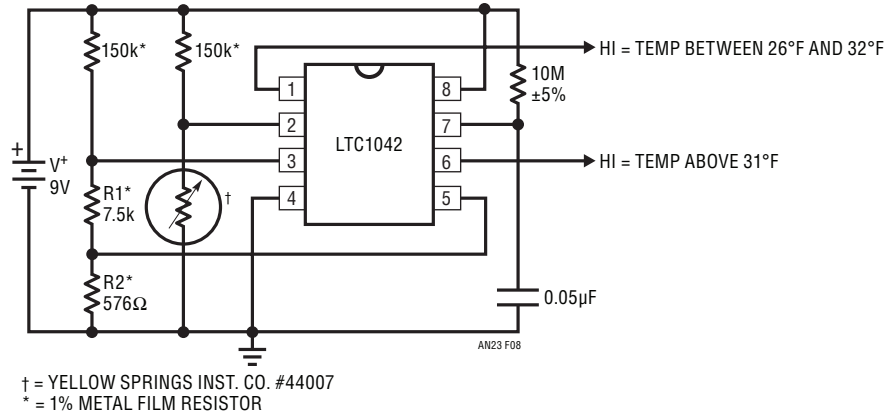


Figure 8. Freezer Alarm

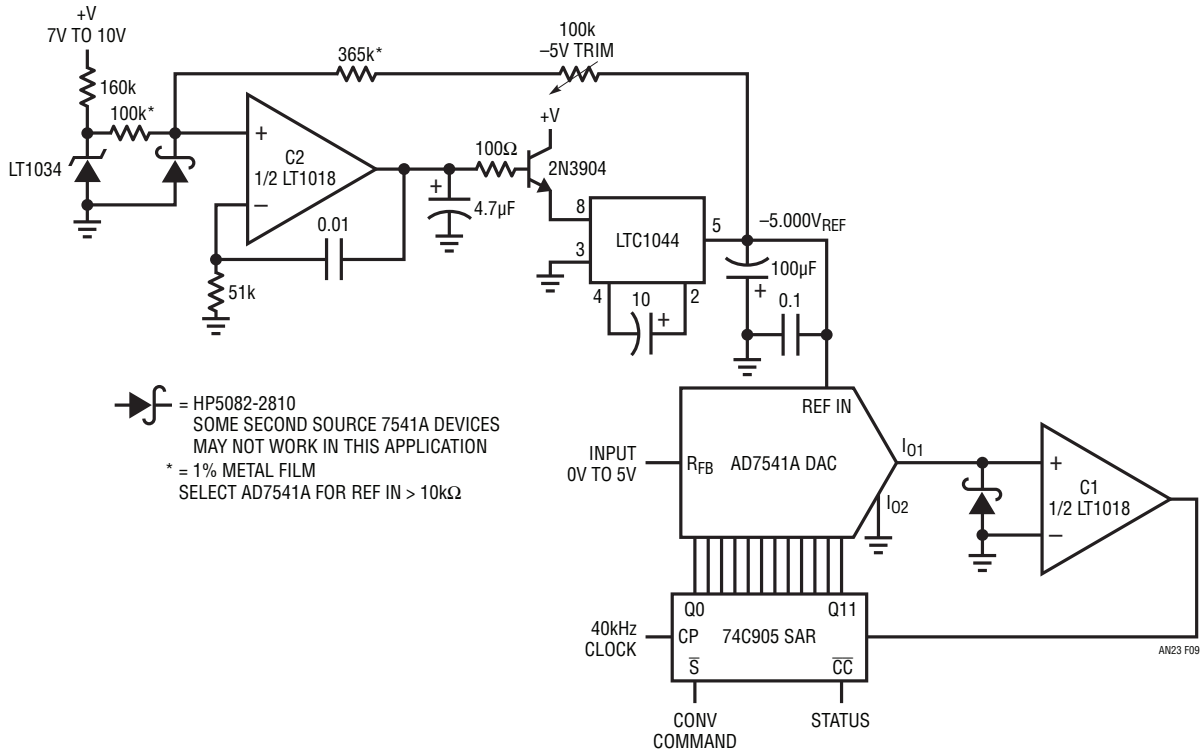


Figure 9. Micropower 12-Bit, 300 μ s A/D

Application Note 23

Conceptually, this design is a straightforward SAR type converter, although some special measures are needed to achieve low power operation. The SAR chip and the DAC are arranged in the standard fashion, with C1 closing a loop. Normally, CMOS DACs are not used for SAR applications because their output capacitance slows operation. In this case, the CMOS DAC's low power consumption is attractive and speed is traded away. This is not too great a penalty, because micropower comparator C1 is a good speed match for the DAC specified. A limitation with CMOS DACs is that their outputs must terminate into 0V. This mandates a current summing comparison, meaning the reference must be of opposite polarity to the input. Since most micropower systems run from single-sided positive rails, it is unrealistic to expect the user to supply the A/D with a negative input. To be readily usable, the converter should accept positive inputs and derive a negative reference internally. This issue is addressed by C2 and the LTC1044 plus-to-minus voltage converter, which form a negative reference.

C2, compensated as an op amp, servo controls the LTC1044 via the boost transistor. The LTC1044's negative output is fed back to C2's input, closing a regulation loop. Scaled current summing from the output and the LT1034 forces a 5.000V output. The Schottky diode prevents possible summing point negative overdrive during start-up. The choice of 5V for a reference maintains reasonable LSB overdrive for C1, but accounts for over half the circuit's current requirement. This limitation is set by the DAC's relatively low input impedance. Dropping the reference voltage would save significant power, but would also reduce LSB size below a millivolt. This would cause comparator offset and gain to become significant error sources.

Although the DAC has no negative supply, it can accept the negative reference because its thin film resistors are not intrinsic to the monolithic structure. Ground referred C1 cannot accept any negative voltages, however, and is Schottky clamped.

Performance includes a typical tempco of 30ppm/°C, 300µs conversion time, 890µA current consumption and an accuracy of ±2 LSBs. Trimming involves adjusting the 100k potentiometer for exactly -5V at V_{REF} . The DAC's internal feedback resistor serves as the input. Figure 10 shows operating waveforms. Trace A is the clock. Trace B is the convert command. The SAR is cleared on Trace B's falling edge and conversion commences on the rise. During conversion, C1's input (Trace C) sequentially converges towards zero. When conversion is complete, the status line (Trace D) drops low.

10-Bit, 100µA A/D Converter

Figure 11's A/D has less resolution than the previous circuit, but requires only 100µA. The design consists of a current source, an integrating capacitor, a comparator and some logic elements. When a pulse is applied to the convert command input (Trace A, Figure 12), the paralleled 74C906 sections reset the 0.075µF capacitor to zero (Trace B). Simultaneously, 74C14 inverter A goes low, biasing the 2N3809 current source on. During this interval the current source stabilizes, delivering its output to ground via the paralleled 74C906 sections. On the falling edge of the convert command pulse the 0.075µF capacitor begins to charge linearly. When the ramp voltage equals the input, C1 switches. Inverter A goes high, shutting off the current source. A small current is bled through the 10M diode connection to keep the ramp charging, but at a greatly reduced

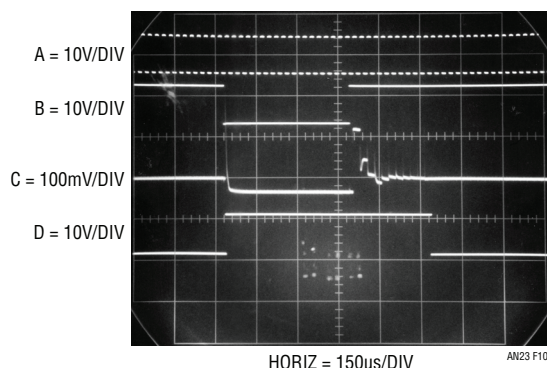


Figure 10. Micropower SAR A/D Waveforms

rate. This ensures overdrive for C1, but minimizes current source on-time, saving power. C1's output, a pulse (Trace C) width, is directly dependent on the value of E_x . This pulse width gates C2's clock output via the 74C00 configuration. The 74C00s also gate out the portion of C1's output due to the convert command pulse. Thus, the clock pulse bursts appearing at the output (Trace D) are proportional to E_x . For the arrangement shown, 1024 pulses appear for a 5V full-scale input. The current source scaling resistor and ramp capacitor specified provide good temperature compensation because of their opposing thermal coefficients. The circuit will typically hold ± 1 LSB accuracy over 0°C to 70°C with an additional ± 1 LSB due to the asynchronous relationship between the clock and the conversion sequence. If the conversion sequence is synchronized to the clock, the ± 1 LSB asynchronous limitation is removed, and total error falls to ± 1 LSB over 0°C to 70°C . The flop-flop shown in dashed lines permits such synchronization. Conversion

rate varies with input. At tenth-scale 150Hz is possible, decreasing to 20Hz at full-scale.

Power consumption of the A/D is extremely low, due to the CMOS logic elements and the LT1017 comparator. Quiescent ($E_{IN} = 0\text{V}$) current is $100\mu\text{A}$ at $V_{\text{SUPPLY}} = 9\text{V}$, decreasing to $80\mu\text{A}$ for $V_{\text{SUPPLY}} = 7\text{V}$. Because current source on-time varies with input, power consumption also varies. For $E_{IN} = 5\text{V}$, current consumption rises to $125\mu\text{A}$ for $E_{\text{SUPPLY}} = 9\text{V}$, and $105\mu\text{A}$ at $E_{\text{SUPPLY}} = 7\text{V}$. Additional power savings are possible by shutting off the current source during capacitor reset, but accuracy suffers due to current source settling time requirements. The $0.075\mu\text{F}$ capacitor's accumulated charge is thrown away at each reset. A smaller capacitor would help, but C1's bias currents would introduce significant error.

Turning off the current source after C1 switches saves significant power. Figure 13, taken at a 25mV input, shows

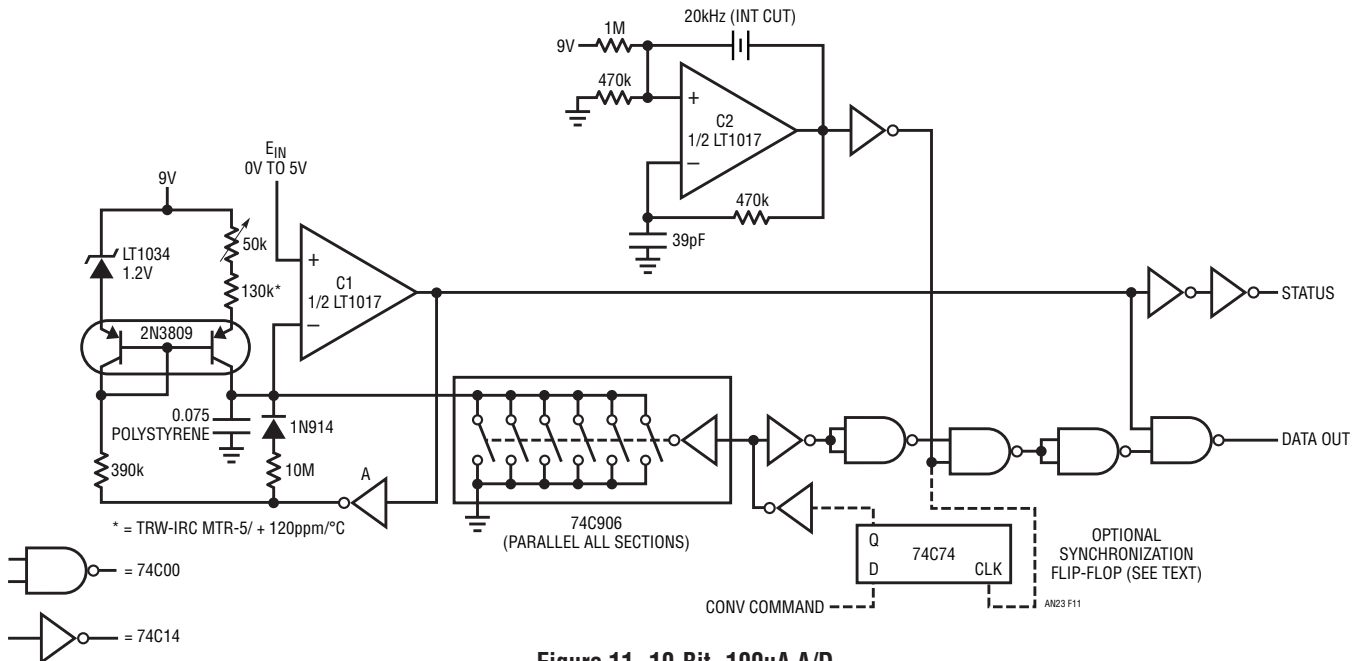


Figure 11. 10-Bit, 100µA A/D

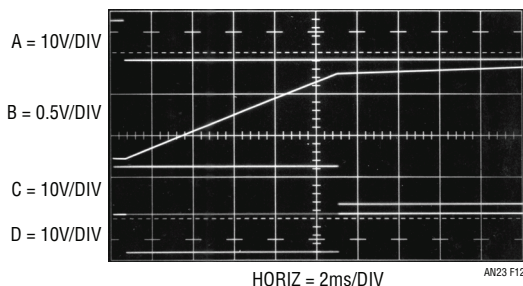


Figure 12. Waveforms for the 100µA A/D

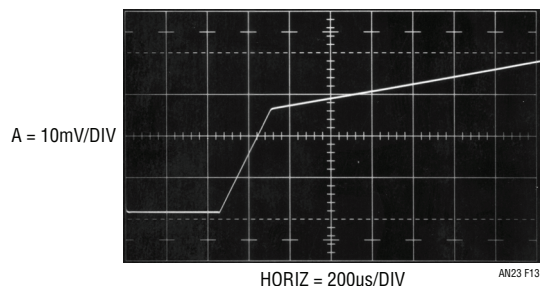


Figure 13. Detail of the Switched Slope Capacitor Charging

Application Note 23

the ramp zero reset and the clean switching. When the current source switches off, the ramp slope decreases but continues to move upward, ensuring overdrive. The 10M diode pair provides the charge, but less than a microampere is lost.

20µs Sample-Hold

Figure 14 is a companion sample-hold for the SAR A/D. Acquisition time is 20µs, with low power operation (see Figure 14 table). This circuit takes full advantage of the programming pin on the LT1006 op amp to maximize speed-power performance. When the sample command (Trace A, Figure 15) is given, the CD4066 switches close. S1 and S2 allow A1's output (Trace B) to charge the capacitor (Trace C is capacitor current). Simultaneously S3 and S4 close, raising the op amp's internal bias network. This

puts both amplifiers into hyperdrive, boosting slew rate to speed acquisition time. A2 (Trace D) is seen to settle cleanly to 1mV in 20µs. When the sample command goes low, all switches go off, A2 follows the voltage stored on the capacitor, and supply current drops by a factor of five (see Figure 14 table). In normal operation, sample time is short compared to hold and current consumption is low. The 360k resistors set the circuit's hold mode quiescent current at the value noted in the table.

10kHz Voltage-to-Frequency Converter

Figure 16, another data converter, is a voltage-to-frequency converter. A 0V to 5V input produces a 0kHz to 10kHz output, with a linearity of 0.02%. Gain drift is 40ppm/°C. Maximum current consumption is only 145µA, far below currently available units.

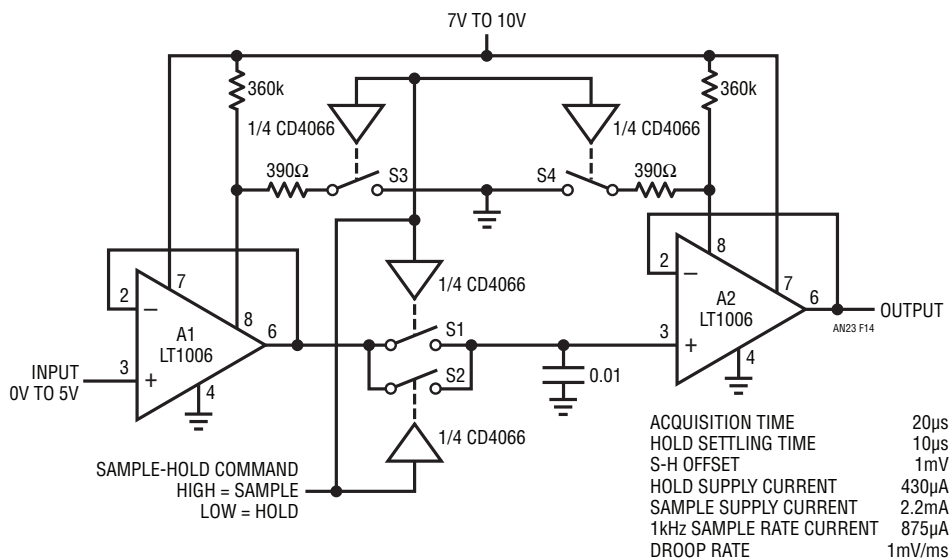


Figure 14. Micropower Sample-Hold

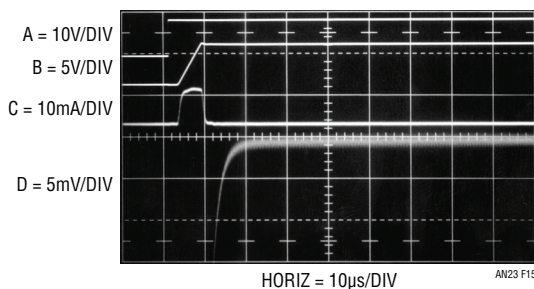


Figure 15. Figure 14's Waveforms

The evolution of this circuit is described in Box Section A, "Some Guidelines for Micropower Design and an Example". To understand circuit operation, assume C1's positive input is slightly below its negative input (C2's output is low). The input voltage causes a positive going ramp at C1's positive input (Trace A, Figure 17). C1's output is low, biasing the CMOS inverter outputs high. This allows current to flow from Q1's emitter, through the inverter supply pin to the 0.001 μ F capacitor. The 10 μ F capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The voltage to which the 0.001 μ F unit charges is a function

of Q1's emitter potential and Q6's drop. When the ramp at C1's positive input goes high enough, C1's output goes high (Trace B) and the inverters switch low (Trace C). The Schottky clamp prevents CMOS inverter input overdrive. This action pulls current from C1's positive input capacitor via the Q5-0.001 μ F route (Trace D). This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output to go low. The 50pF capacitor connected to the circuit output furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 0.001 μ F capacitor. The Schottky diode prevents C1's input from being driven

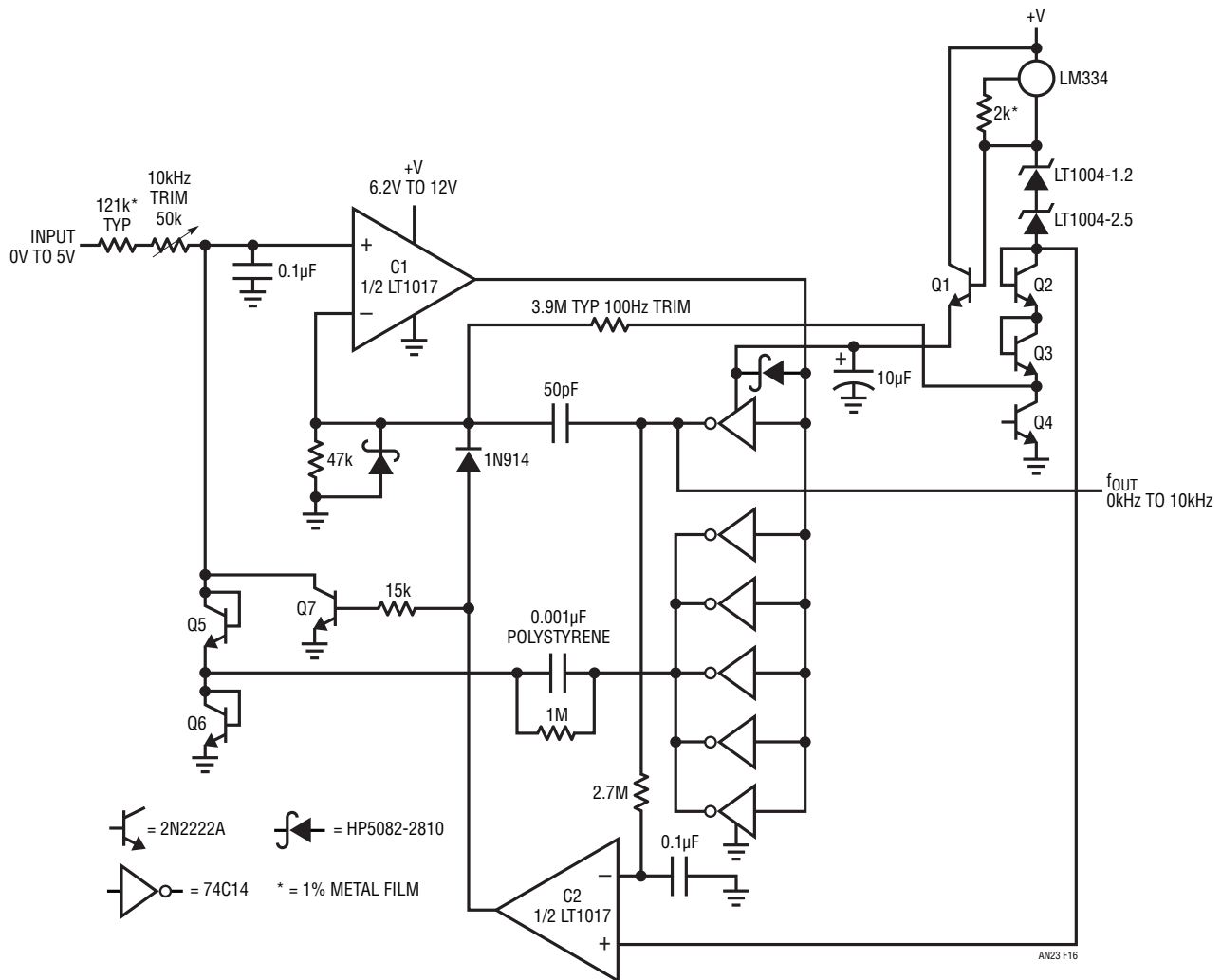


Figure 16. Micropower 10kHz V→F Converter

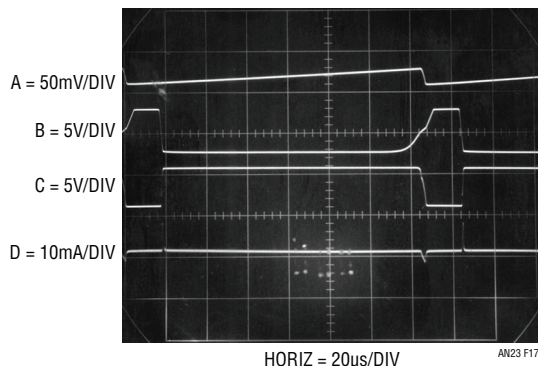


Figure 17. Figure 16's Waveforms

outside its negative common mode limit. When the 50pF unit's feedback decays, C1 again switches low and the entire cycle repeats. The oscillation frequency depends directly on the input voltage derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE} . The two LT1004s are the actual voltage reference and the LM334 current source provides 35µA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by utilizing the LM334's 0.3%/°C tempco to slightly temperature modulate the voltage drop in the Q2-Q4 trio. This correction's sign and magnitude directly oppose that of the -120ppm/°C 0.001µF polystyrene capacitor, aiding overall circuit stability.

The Q1 emitter-follower delivers charge to the 0.001µF capacitor efficiently. Both base and collector current end up in the capacitor. The paralleled CMOS inverters provide low loss SPDT reference switching without significant drive losses. The 0.001µF capacitor, as small as accuracy permits, draws only small transient currents during its

charge and discharge cycles. The 50pF-47k positive feedback combination draws insignificantly small switching currents. Figure 18, a plot of supply current vs operating frequency, reflects the low power design. At zero frequency, the LT1017's quiescent current and the 35µA reference stack bias accounts for all current drain. There are no other paths for loss. As frequency scales up, the charge-discharge cycle of the 0.001µF capacitor introduces the 7µA/kHz increase shown. A smaller value capacitor would cut power, but the effects of stray capacitance, charge imbalance in the 74C14, and LT1017 bias currents would introduce accuracy errors.

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high. C2, detecting this via the inverters and the 2.7M-0.1µF lag, also goes high. This lifts C1's negative input and grounds the positive input with Q7, initiating normal circuit action.

Because the charge pump is directly coupled to C1's output, response is fast. Figure 19 shows the output (Trace B) settling within one cycle for a fast input step (Trace A).

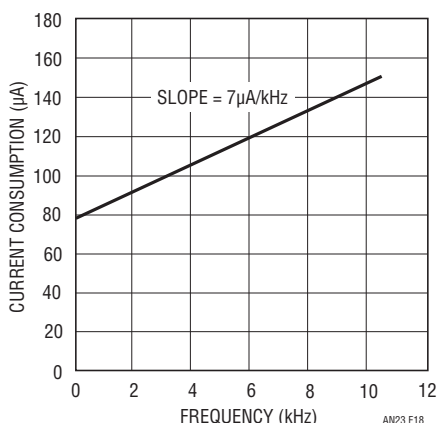


Figure 18. Current Consumption vs Frequency for Figure 16

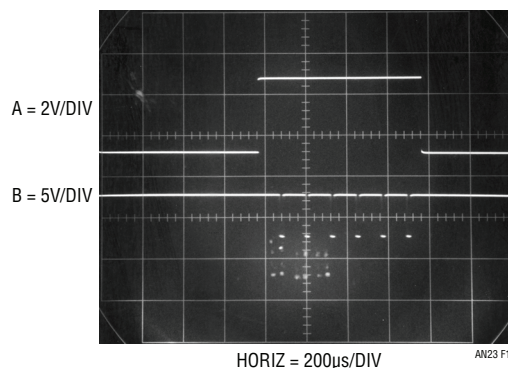


Figure 19. Figure 16's Step Response

To calibrate this circuit, apply 50mV and select the value at C1's input for a 100Hz output. Then, apply 5V and trim the input potentiometer for a 10kHz output.

An evolutionary history of this design appears in Box Section A, "Some Guidelines for Micropower Design and an Example".

A nice day at the San Francisco Zoo with Celia Moreno M.D., instrumental in arriving at the final configuration, is happily acknowledged.

1MHz Voltage-to-Frequency Converter

Figure 20 is also a V→F converter, but runs at 1MHz full-scale. Quiescent current is 90μA, ascending linearly

to 360μA at 1MHz output. Obtaining higher operating frequency requires trade-offs in power consumption and step response performance. Linearity is 0.02% over a 100Hz to 1MHz range, drift about 50ppm/°C and step response inside 350ms to full-scale.

This circuit has similarities to Figure 16, although operation is somewhat different. An input causes A1 to swing towards ground, biasing Q8. Q8's collector ramps (Trace A, Figure 21) as it charges the 3pF capacitor plus stray capacitance associated with Q7 and the 74C14 Schmitt input connected to the node. When the ramp hits the Schmitt's threshold its output (Trace B) goes low, turning on diode connected Q7. Q7's path discharges the node capacitances,

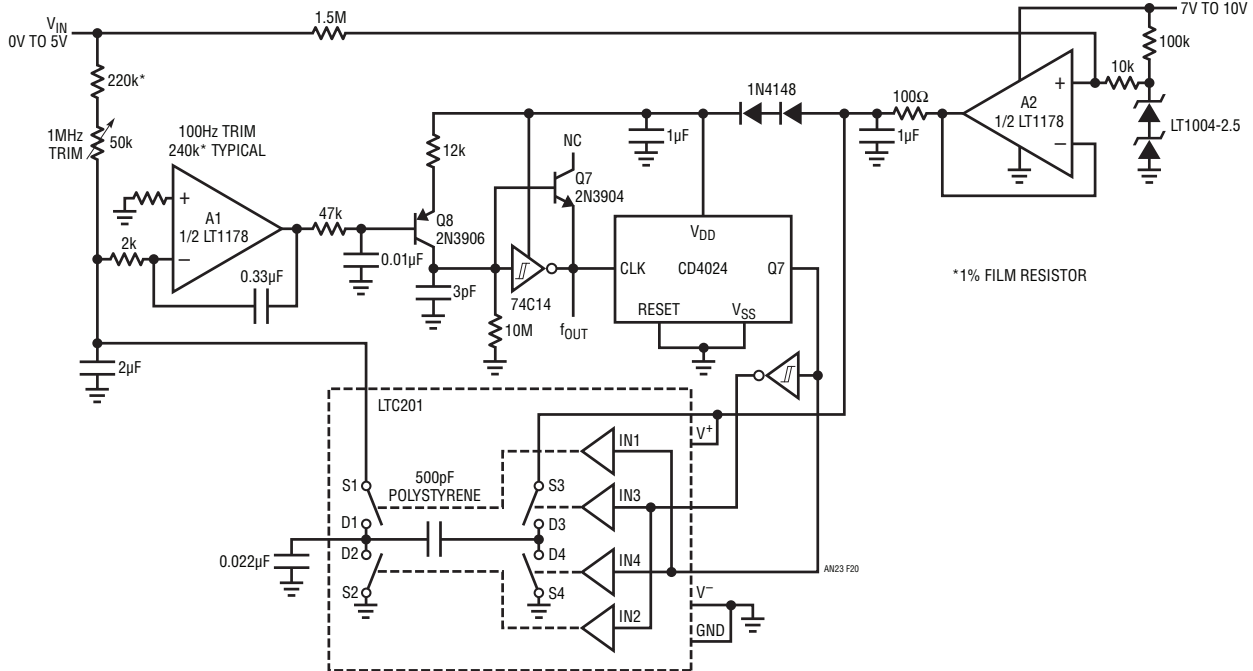


Figure 20. Micropower 1MHz V→F Converter

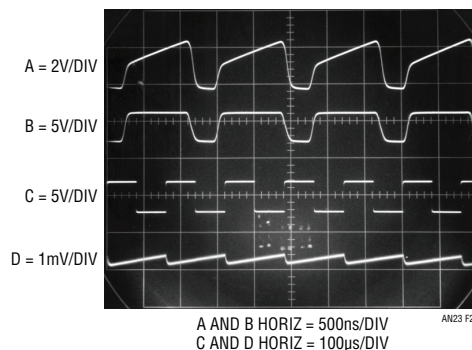


Figure 21. Figure 20's Waveforms

Application Note 23

forcing ramp reset. The 74C14 returns high, and oscillation commences. The 74C14 also drives the CD4024 divider, and serves as the circuit's output. The divider's $\div 128$ output (Trace C) controls a reference charge pump arrangement similar to Figure 16's. A2 furnishes a buffered reference. The 500pF capacitor is alternately charged and discharged by the LTC201 switch sections. The charge increments pulled through S1 continually force A1's 2 μ F capacitor to zero (Trace D), balancing the input derived current. The 0.022 μ F capacitor at the D1-D2 LTC201 node eliminates excessive differentiated response, preventing spurious modes. This action closes a loop around A1, and it servo controls the Q7, Q8, 74C14 oscillator to run at whatever frequency is required to maintain its negative input at zero. This servo behavior eliminates oscillator drift and nonlinearity as error terms, allowing the performance specifications noted. The 0.33 μ F capacitor at A1 stabilizes the loop. This capacitor accounts for the circuit's 350ms settling time.

The resistor from the input to A2 sums a small input related voltage to the reference, improving linearity. The 10M resistor at Q8's collector deliberately introduces leakage to ground, dominating all node leakages. This ensures low frequency operation by forcing Q8 to source current to maintain oscillations.

The circuit's current drain, while low, is larger than Figure 16's. The increase is primarily due to high frequency oscillator and divider operation. The series diodes in the oscillator-divider supply line lower supply voltage, decreasing current consumption. Oscillator current is also heavily influenced by the capacitance and swing at Q8's collector. The swing is fixed by the 74C14 thresholds. Capacitance has been chosen at the lowest possible value commensurate with desired low frequency operation.

To trim this circuit, put in 500 μ V and select the indicated value at A1's positive input for 100Hz out. Then, put in 5V and trim the 50k potentiometer for 1MHz out. Repeat this procedure until both points are fixed.

Switching Regulator

No discussion of micropower circuitry is complete without mention of switching regulators. Often, battery voltages must be efficiently converted to different potentials to meet circuit requirements. Figure 22 shows a micropower buck type switching regulator with a quiescent drain of 70 μ A and 20mA output current capability. When the output

voltage drops (Trace A, Figure 23) C1's negative input also falls, causing its output (Trace B) to rise. This turns on the paralleled 74C907 open-source buffers, and their outputs (Trace C) go high. Current ramps up through the inductor, maintaining the regulator output. When output voltage rises a small amount, C1's output returns low and the cycle repeats. This action maintains regulator output despite line and load changes. The LT1004 serves as a reference and the 5pF capacitor ensures clean switching at C1. The 2810 Schottky diode prevents negative overdrives due to the 5pF unit's differentiated response; the 1N5817 is a catch diode, preventing excessive inductor caused negative voltages.

This circuit's low quiescent drain is due to the LT1017's small operating currents and the 74C907's low input drive requirements. Circuit resistor values are kept high to save current. C2 shuts down the regulator when output current exceeds 50mA. It does this by comparing the potential across the 0.2 Ω shunt to a resistively divided portion of the LT1004 reference. Excessive current drain trips C2 high, forcing C1's negative input high. This removes drive from the 74C907 buffers, shutting down the regulator.

Utilization of a CMOS buffer as a pass switch for a switching regulator is somewhat unusual, but performance is quite good. Figure 24 plots efficiency vs output current at two input voltages. Efficiencies above 90% are possible, with output current to 20mA depending on input.

Post Regulated Micropower Switching Regulator

Figure 25 is another buck type switching regulator, but features a low loss linear post regulator, quiescent current of 40 μ A and 50mA output capacity. The LT1020 linear regulator provides lower noise than a straight switching approach. Additionally, it offers internal current limiting and contains an auxiliary comparator which is used to form the switching regulator.

The switching loop is similar to Figure 22's circuit. A drop at the switching regulator's output (Pin 3 of the LT1020 regulator; Trace A, Figure 26) causes the LT1020's comparator to go high. The 74C04 inverter chain switches, biasing the P-channel MOSFET switch's grid (Trace B). The MOSFET comes on (Trace C), delivering current to the inductor (Trace D). When the voltage at the inductor-220 μ F junction goes high enough (Trace A), the comparator switches high, turning off MOSFET current flow. This switching

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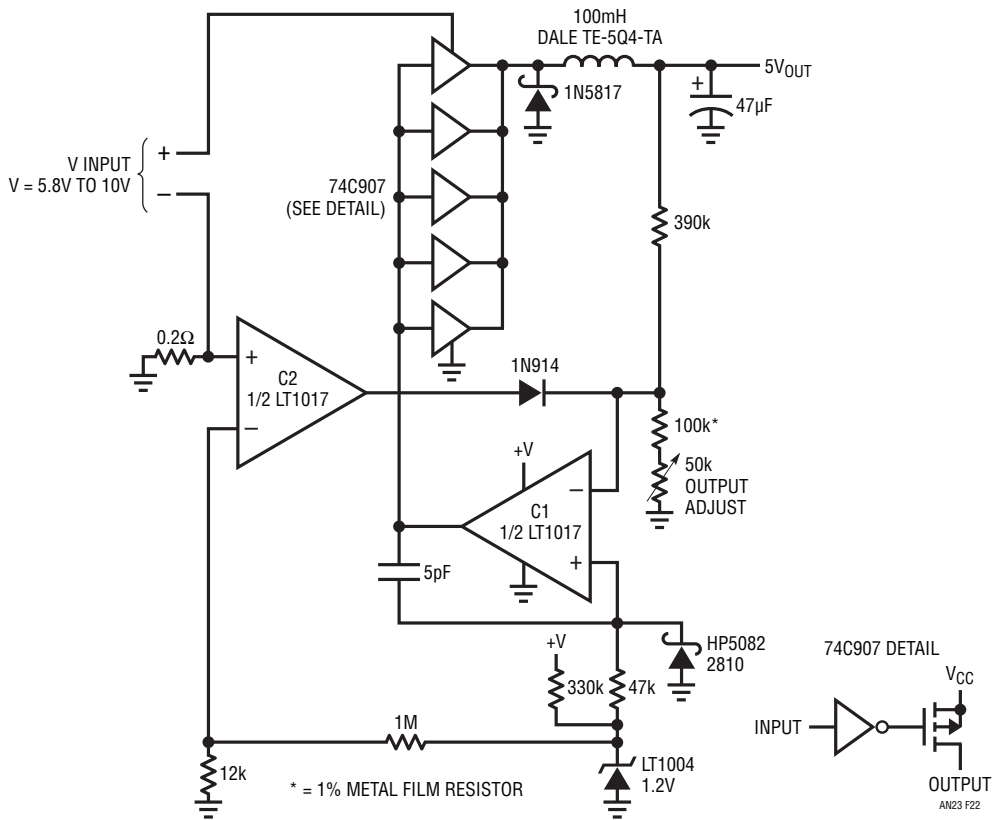


Figure 22. Micropower Switching Regulator

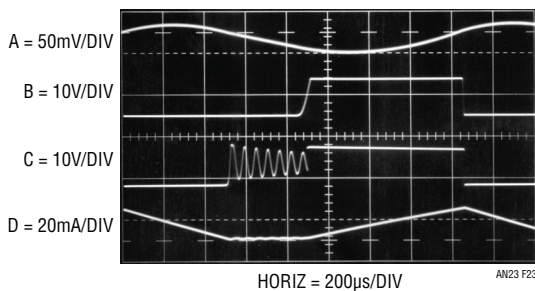


Figure 23. Figure 22's Waveforms

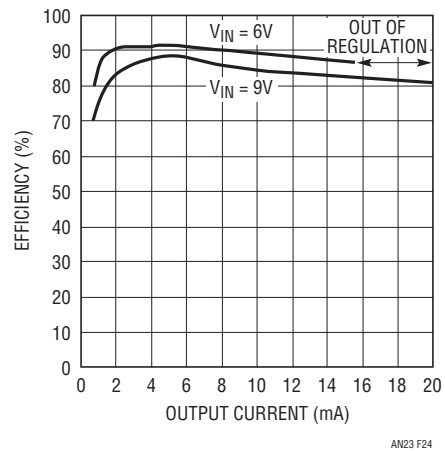


Figure 24. Figure 22's Efficiency vs Output Current

Application Note 23

loop regulates the LT1020's input pin at a value set by the resistor divider in the comparator's negative input and the LT1020's 2.5V reference. The 680pF capacitor stabilizes the loop and the 1N5817 is the catch diode. The 270pF capacitor aids comparator switching and the 2810 diode prevents negative overdrives.

The low dropout LT1020 linear regulator smooths the switched output. Output voltage is set with the feedback pin associated divider. A potential problem with this circuit is start-up. The switching loop supplies the LT1020's input but relies on the LT1020's internal comparator to function. Because of this, the circuit needs a start-up mechanism. The 74C04 inverters serve this function. When power is applied, the LT1020 sees no input, but the inverters do. The 220k path lifts the first inverter high, causing the chain to switch, biasing the MOSFET and starting the circuit. The inverter's rail-to-rail swing also provides ideal MOSFET grid drive.

Even though this circuit's 40μA quiescent current is lower than Figure 22's, it can source more current. The extremely small quiescent current is due to the low LT1020 drain and the MOS elements. Figure 27 plots efficiency vs output current for two LT1020 input-output differential voltages. Efficiency exceeding 80% is possible, with outputs to 50mA available.

Figures 28 and 29 show two other LT1020 micropower regulator-based circuits. In many processor-based systems it is desirable to monitor or control the power-down sequence. Figure 28 produces a logical "1" output when the regulator output begins to drop out (e.g., battery is low). Here, the regulator is programmed for a 5V output with the 1M feedback resistors. The 0.001μF capacitor provides frequency compensation. The LT1020's internal comparator senses the difference between the chip's 2.5V reference and a small portion of the IC's pass transistor current (supplied at Pin 13). At the edge of dropout, the

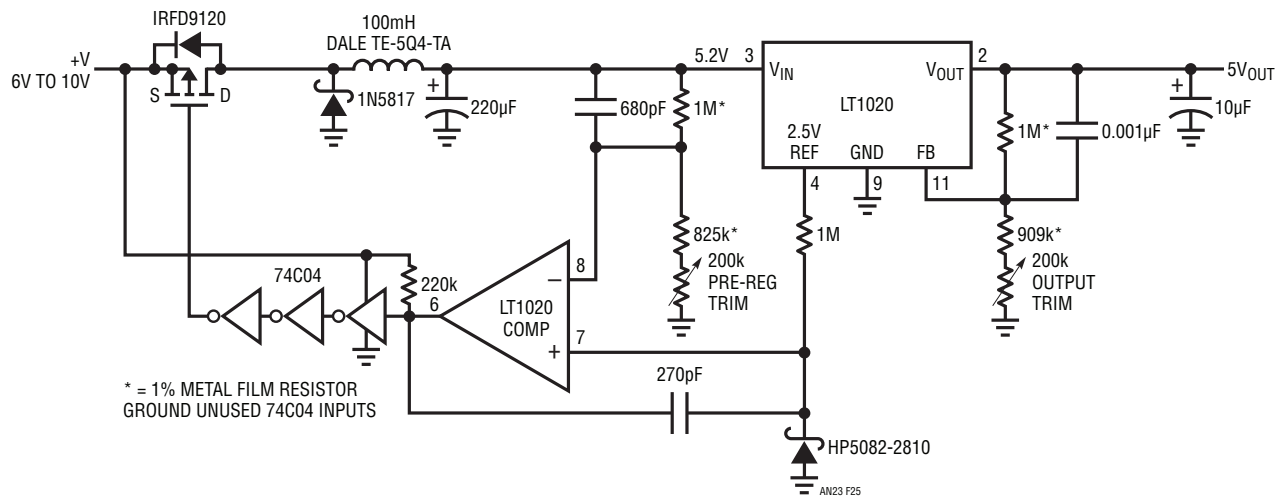


Figure 25. Micropower Post-Regulated Switching Regulator

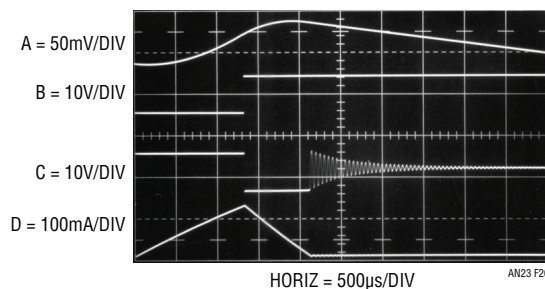
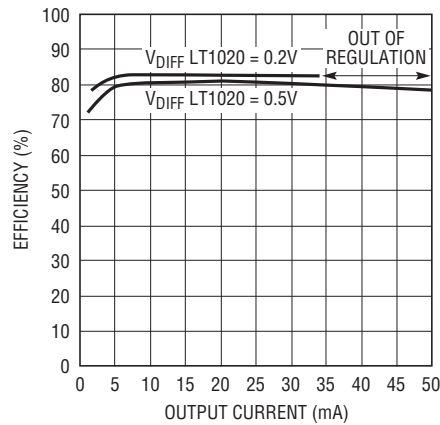


Figure 26. Figure 25's Waveforms



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Figure 27. Figure 25's Efficiency vs Output Current

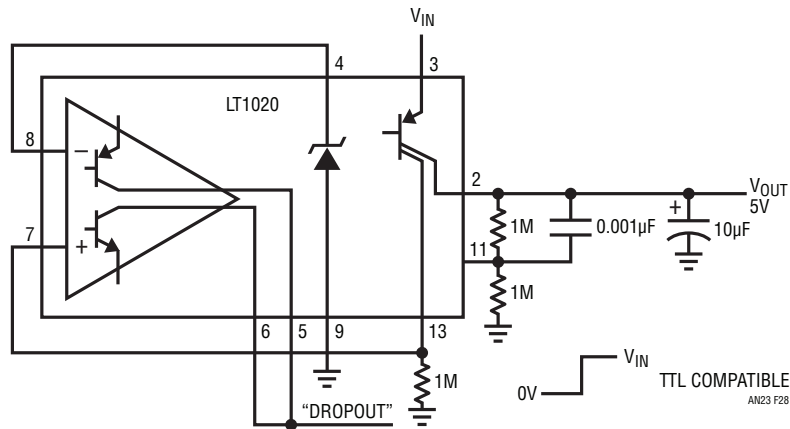


Figure 28. Regulator with Logic Output on Dropout

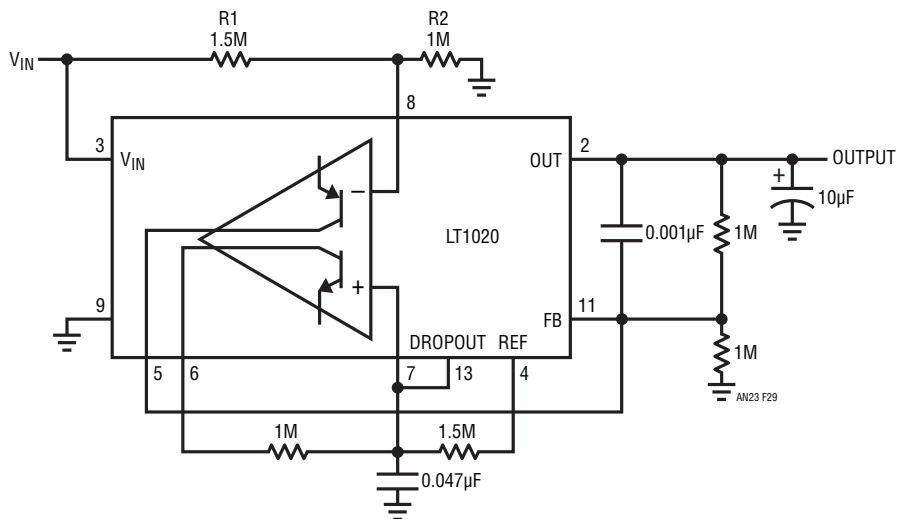


Figure 29. Regulator with Output Shutdown on Dropout

Application Note 23

LT1020's pass transistor goes towards saturation, raising Pin 13's voltage. This trips the comparator, and its output goes high. This signal can be used to alert a processor that power is about to go down.

Figure 29 is similar, except that power is turned completely off when dropout begins to occur, preventing unregulated supply conditions. The comparator feedback is arranged for a hysteresis type response. Although the output turns off at dropout, it will not turn on until:

$$\text{Turn On} = \frac{V_{IN} \cdot R2}{R1 + R2} = 2.5V$$

This prevents battery "creep back" from causing oscillation.

Figure 30 shows a simple way to shut the LT1020 down. In this state it draws only 40µA. The logic signal forces the feedback pin above the internal 2.5V reference, and all drive is removed from the output transistor. Figure 31 shows a low loss way to implement a "glitchless" memory battery backup. During line-powered operation, the right LT1020 does the work. The feedback string is arranged so that the left LT1020 does not conduct under line-powered conditions. When the line goes down, the associated LT1020 begins to go off, allowing the battery-driven regulator to turn on, maintaining the load.

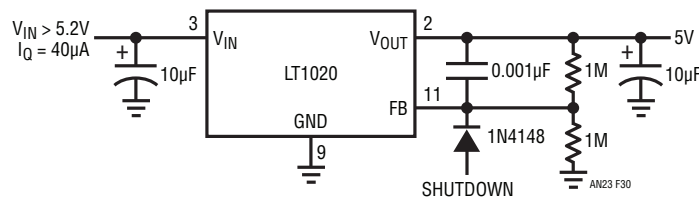


Figure 30. LT1020 Shutdown

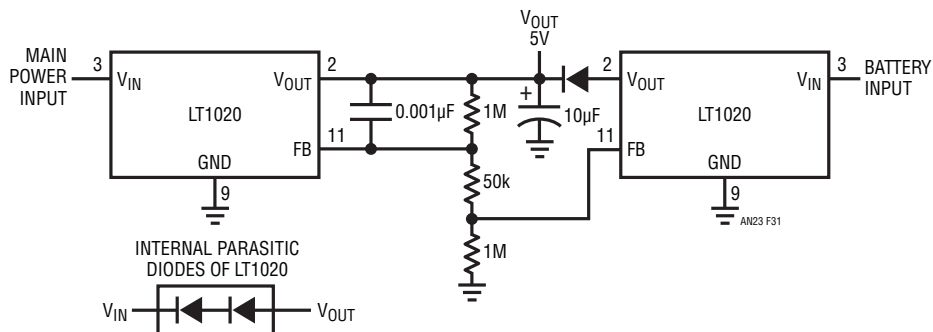


Figure 31. Battery Backup Regulator

BOX SECTION A

Some Guidelines for Micropower Design and an Example

As with all engineering, micropower circuitry requires attention to detail, awareness of trade-offs and an opportunistic bent towards achieving the design goal.

The most obvious way to save power is to choose components which require little energy. Additional savings require more effort.

Circuits should be examined in terms of current flow. Consider such flow in all DC and AC paths. For example, do DC base currents go where they can do some useful work, or are they thrown away? Try to keep AC signal swings down, particularly if capacitors (parasitic or intended) must be continually charged and discharged.

Examine the circuit for areas where power strobing may be allowable.

Consider quiescent vs dynamic power requirements of components to avoid unpleasant surprises. Data sheets usually specify quiescent power because the manufacturer doesn't know what the user's circuit conditions are. For example, everyone "knows" that "MOS devices draw no current." Unfortunately, Mother Nature dictates that as frequency and signal swings go up, the capacitances associated with MOS devices begin to require more power. It is often a mistake to automatically associate low power operation with a process technology. While it's likely that CMOS will provide lower power operation for a given function than 12AX7s, a bipolar approach may be even better. Consider individual situations on the basis of their specific requirements before committing to a technology. Very often, circuits require several technologies (e.g., CMOS, bipolar and discrete) for best results.

Usually, achieving low power operation requires performance trade-offs. Minimizing signal swings and current saves power, but moves circuit operation closer to the noise floor. Offsets, drift, bias currents and noise become increasingly significant error factors as signal amplitudes are constricted to save power. This is a fundamental trade-off and must be carefully considered. Circuits employing power strobing can sometimes get around this problem by utilizing low duty cycles. Text Figure 3 uses this technique to achieve dramatic power savings in a circuit with an on-state drain approaching 20mA (see also Box Section B, "Sampling Techniques and Components for Micropower Circuits").

Text Figure 16, a voltage-to-frequency converter, furnishes an example of the evolution of a low power design. Design goals included a 10kHz maximum output, fast step response, linearity inside 0.05% and a maximum supply current of 150 μ A. Other specifications appear in the text.

Figure A1 shows an early version of this circuit. Operation is similar to the text described for Figure 16, but a brief description follows: When the input current-derived ramp at C1's negative input crosses zero, C1's output drops low, pulling charge through C1. This forces the negative input below zero. C2 provides positive feedback, allowing a complete discharge for C1. When C2 decays,

C1A's output goes high, clamping at the level set by D1, D2 and V_{REF} . C1 receives charge and recycling occurs when C1A's negative input again arrives at zero. The frequency of this action is related to the input voltage. Diodes D3 and D4 provide steering, and are temperature compensated by D1 and D2. C1A's sink saturation voltage is uncompensated, but small. C1B is a start-up loop.

Although the LT1017 and LT1034 have low operating currents, this circuit pulls almost 400 μ A. The AC current paths include C1's charge-discharge cycle, and C2's branch. The DC path through D2 and V_{REF} is particularly costly. C1's charging must occur quickly enough for 10kHz operation, meaning the clamp seen by C1A's output must have low impedance at this frequency. C3 helps, but significant current still must come from somewhere to keep impedance low. C1A's current-limited output cannot do the job unaided, and the resistor from the supply is required. Even if C1A could supply the necessary current, V_{REF} 's settling time would be an issue. Dropping C1's value will reduce impedance requirements proportionally, and would seem to solve the problem. Unfortunately, such reduction magnifies the effects of stray capacitance at the D3-D4 junction. It also mandates increasing R_{IN} 's value to keep scale factor constant. This lowers operating currents at C1A's negative input, making bias current and offset more significant error sources.

Figure A2 shows an initial attempt at dealing with these issues. This scheme is similar to Figure A1, except that Q1 and Q2 appear. V_{REF} receives switched bias via Q1, instead of being on all the time. Q2 provides the sink path for C1. These transistors invert C1A's output, so its input pin assignments are exchanged. R1 provides a light current from the supply, improving reference settling time. This arrangement decreases supply current to about 300 μ A, a significant improvement. Several problems do exist, however. Q1's switched operation is really effective only at higher frequencies. In the lower ranges, C1A's output is low most of the time, biasing Q1 on and wasting power. Additionally, when C1A's output switches, Q1 and Q2 simultaneously conduct during the transition, effectively shunting R2 across the supply. Finally, the base currents of both transistors flow to ground and are lost. The basic temperature compensation is as before, except that Q2's saturation term replaces the comparator's.

Application Note 23

Figure A3 is better. Q1 is gone, Q2 remains but Q3, Q4 and Q5 have been added. V_{REF} and its associated diodes are biased from R1. Q3, an emitter-follower, is used to source current to C1. Q4 temperature compensates Q3's V_{BE} , and Q5 switches Q3.

This method has some distinct advantages. The V_{REF} string can operate at greatly reduced current because of Q3's current gain. Also, Figure A2's simultaneous conduction problem is largely alleviated because Q5 and Q2 are switched at the same voltage threshold out of C1A. Q3's base and emitter currents are delivered to C1. Q5's currents are wasted, although they are much smaller than Q3's. Q2's small base current is also lost. The values for C2 and R3 have been changed. The time

constant is the same, but some current reduction occurs due to R3's increase.

If C1 cannot be reduced for performance reasons, then its AC currents cannot be avoided. This leaves only the aforementioned Q5 and Q2 currents as significant wasted terms, along with R3's now smaller loss. Current drain for this circuit is about $200\mu\text{A}$ maximum. Text Figure 16's circuit is very similar, but eliminates Q5 and Q2's losses to achieve maximum operating current below $150\mu\text{A}$ with quiescent current under $80\mu\text{A}$. Some other refinements are included, but the circuit is the final iteration of the three versions shown here. A complete description of Figure 16 appears in the text.

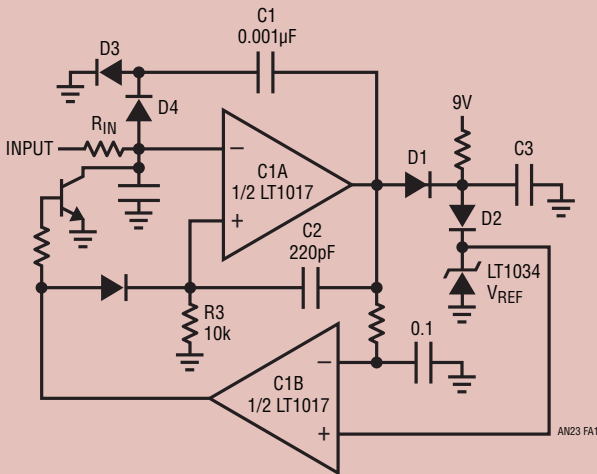


Figure A1

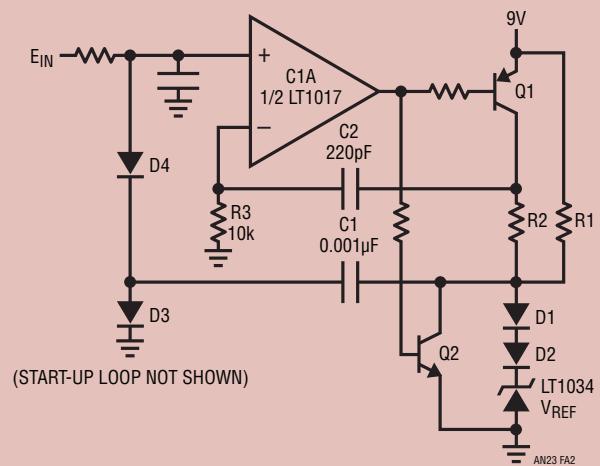


Figure A2

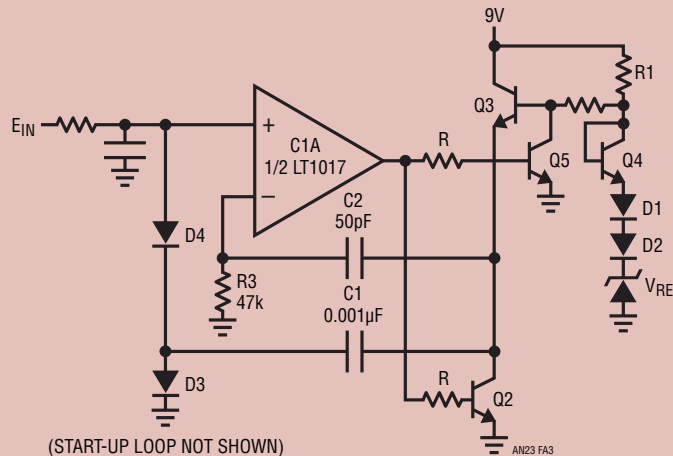


Figure A3

BOX SECTION B

Sampling Techniques and Components for Micropower Circuits

The best way to get low power circuit characteristics is to turn off the power. While there are some obvious problems with this approach, it does point a way towards minimizing power consumption. In many applications continuous circuit power is not necessary. If bandwidth requirements are low, sampling techniques offer a simple way to save power. With low duty cycles, instantaneous current can be relatively high while average drain remains low. When considering a sampled approach some issues should be examined. The required circuit bandwidth dictates the minimum sampling frequency in accordance with Nyquist criteria. The sampling interval's duration is determined by circuit settling time to the required accuracy. This settling time should be considered for all circuit elements (transducers, ICs and discrete components) singularly and together. Additionally, effects of sampled operation on component life and operating characteristics should be examined. This is particularly the case for transducers, which may be designed and tested under DC operating conditions.

Once these issues have been addressed, components can be selected. The LTC1040, LTC1041 and LTC1042 have been specifically designed for sampled operation. Figure B1 details the LTC1040, dual micropower comparator. Its programmable internal oscillator sets the sampling rate with a sampling interval lasting 80µs. The V_{PP} output supplies power during the sampling interval, allowing drive for external circuitry or transducers. Note that the input common mode range includes both rails. Figure B2 plots supply current vs sampling frequency.

A related device is similar, but dedicated to “bang-bang” on-off type servo loops. The LTC1041 appears in Figure B3. Servo SET POINT and DELTA are controllable from the inputs. The associated diagram (Figure B4) graphically defines operation. Operating current is similar to the LTC1040.

A final device, the LTC1042, is also similar but is set up as a window comparator. Its internals appear in Figure B5 and the graphic operation description is shown in Figure B6. Operating current, input range and sampling characteristics are similar to the LTC1040 and LTC1041.

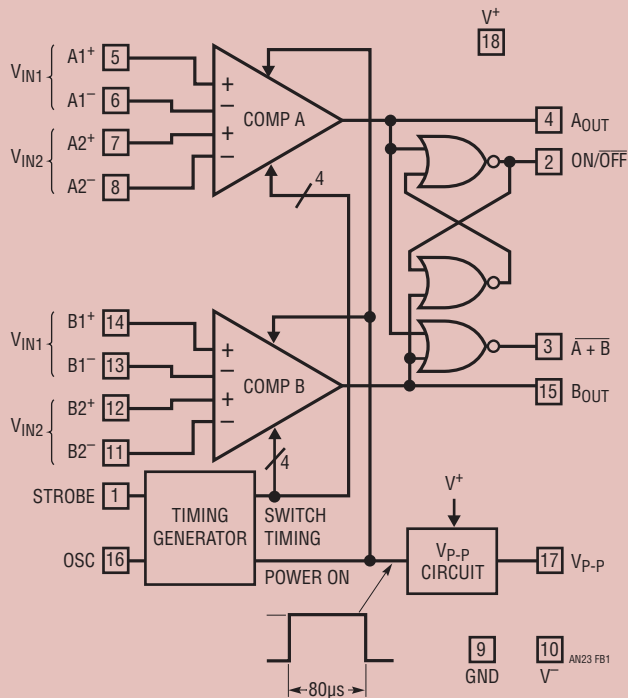


Figure B1. LTC1040 Internal Details

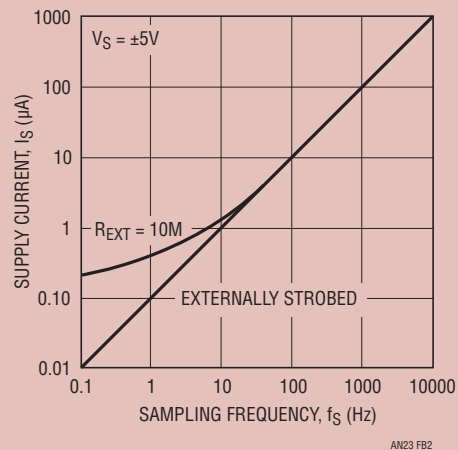


Figure B2. LTC1040 Power Consumption vs Sampling Frequency

Application Note 23

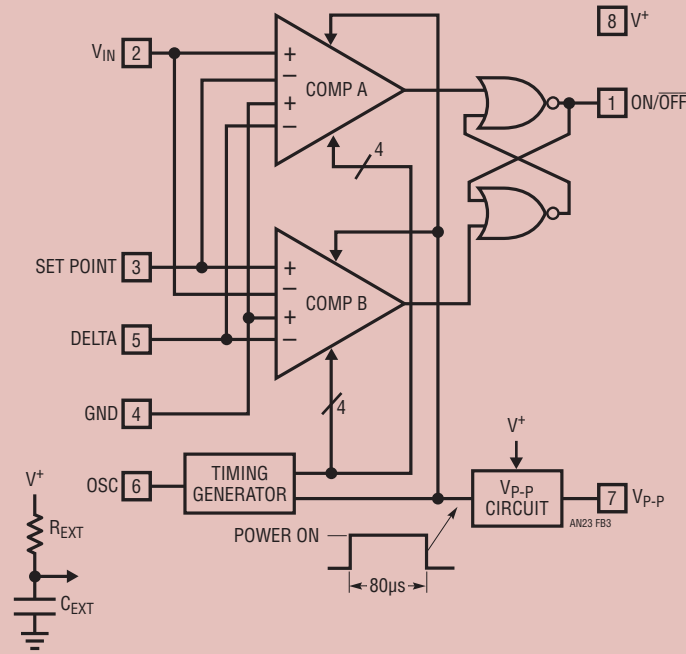


Figure B3. LTC1041 Details

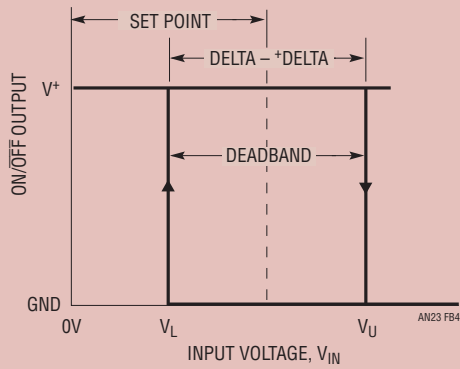


Figure B4. LTC1041 Operation Diagram

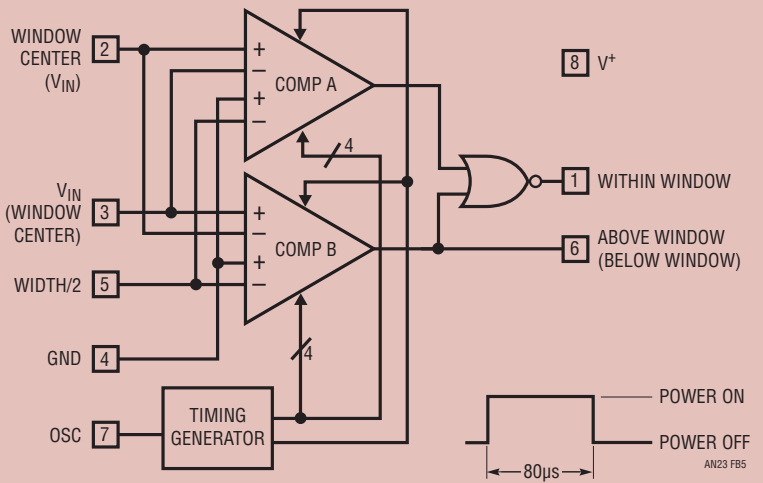


Figure B5. LTC1042 "Window" Comparator Details

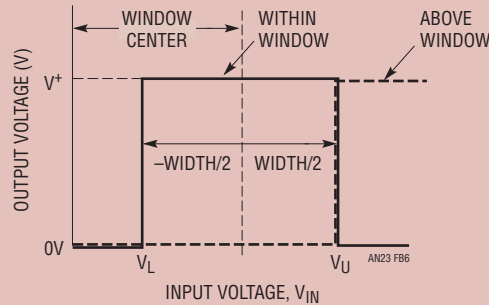


Figure B6. LTC1042 Operating Diagram

BOX SECTION C

Parasitic Effects of Test Equipment on Micropower Circuits

The energy absorbed by test equipment connections to micropower circuits can be significant. Under normal circumstances test equipment and probes have negligible power drain, but microampere level operating currents mandate care. Test instrumentation should be regarded as an integral part of the circuit. DC and AC loading and parasitic effects must be kept in mind to avoid unpleasant surprises. Such instrument connection errors can make the circuit under test look unfairly bad or good.

The DC resistance of oscilloscope probes varies from hundreds of ohms (1x types) to 10M (10x), with some 10x types as low as 1M. Contrary to some expectations, FET probes do not have high input resistance—some types are as low as 100k, although most are about 10M. The DC loading of a 10x 1M probe could introduce as much as 9 μ A of loss, almost 10% of Figure 11's total! The AC loading of a 10pF probe looking at Figure 11's 20kHz clock will cause apparent circuit consumption of 5 μ A, a significant loss in a low power circuit. 1x type probes present about 50pF of loading, with 1M DC resistance when connected to the 'scope. This kind of probe loading can cause large errors in micropower circuits, while virtually disabling some. Such a probe, introduced at Pin 6 of text Figure 7, would stop the circuit's oscillator. If placed across the supply of the

same circuit it would consume 15 times the circuit's operating current. Similarly, the probe's 50pF input capacitance connected to Figure 20 (Q8's collector) results in a 25% apparent increase in circuit current at 1MHz output.

Probe AC and DC loading are not the only effects. Some DVMs produce "charge spitting" at their inputs. Such parasitic charge, introduced into high impedance nodes, can cause substantial errors. It's also worth remembering that DVM DC loading may change with range. Lower ranges may have very high input impedance, but higher ranges are typically 10M Ω . A 10M Ω DVM reading Figure 7's supply consumes 1 1/2 times the circuit current.

Figure C1 shows a way test equipment can make the circuit look too good, instead of too bad. If the pulse generator is adjusted more than a diode drop above the regulator's output, the bypass capacitor peak detects the charge delivered through the IC's internal diode. The regulator can't sink current, and with its output forced high it won't source anything. Under these conditions, the circuit functions while the current meter reads zero... a very low power circuit indeed!*

*Practically speaking, most regulators and power supplies can sink small amounts of current. Because of this, the current meter may actually read negative.

Application Note 23

Figure C2 shows a very simple, but useful, circuit which greatly aids probe loading problems in micropower circuits. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows DVM cable and probe driving and also biases the circuit's input shield. This bootstraps the input capacitance, reducing its

effect. DC and AC errors of this circuit are low enough for almost all work, with enough bandwidth for just about any low power circuit. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.

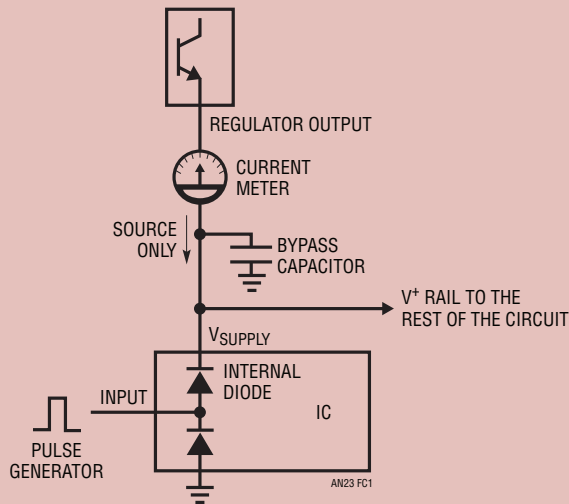


Figure C1

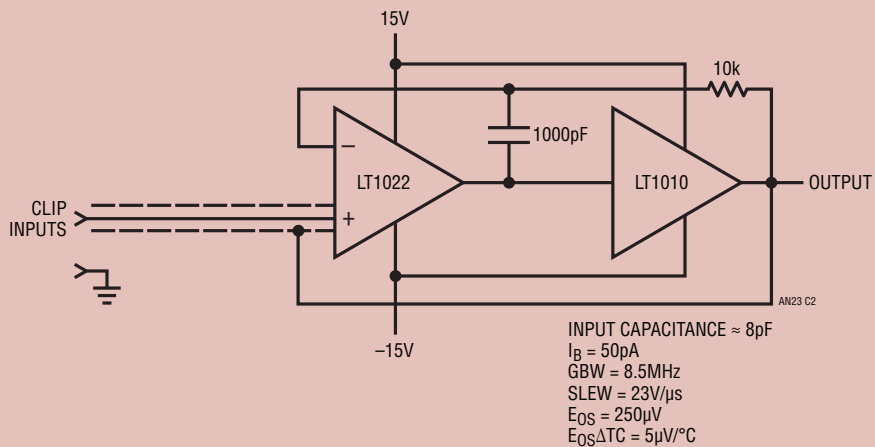


Figure C2

Switching Regulators for Poets

A Gentle Guide for the Trepidatious

Jim Williams

The above title is not happenstance and was arrived at after considerable deliberation. As a linear IC manufacturer, it is our goal to encourage users to design and build switching regulators. A problem is that while everyone agrees that *working* switching regulators are a good thing, everyone also agrees that they are difficult to get working. Switching regulators, with their high efficiency and small size, are increasingly desirable as overall package sizes shrink. Unfortunately, switching regulators are also one of the most difficult linear circuits to design. Mysterious modes, sudden, seemingly inexplicable failures, peculiar regulation characteristics and just plain explosions are common occurrences. Diodes conduct the wrong way. Things get hot that shouldn't. Capacitors act like resistors, fuses don't blow and transistors do. The output is at ground, and the ground terminal shows volts of noise.

Added to this poisonous brew is the regulator's feedback loop, sampled in nature and replete with uncertain phase shifts. Everything, of course, varies with line and load conditions—and the time of day, or so it seems. In the face of such menace, what are Everyman and the poets to do?

The classic approach is to seek wisdom. Substantial expertise exists but is concentrated in a small number of corporate and academic areas. These resources are not readily accessed by Everyman and some cynics might suggest that they are deliberately protected by a self-serving priesthood. A glance through conference proceedings and published literature yields either a storm of mathematics or absurdly coy and simple little block diagrams that make everything look just so easy. Either way, Everyman loses. And the poets don't even get to try.

Something to think about is that most people who want switching regulators don't need 98.2% efficiency or 100W/cubic inch. They aren't trying to get tenure and don't care about inventing a new type of circuit. What they want are concepts directly applicable to construction of working circuits with readily-available parts. Thus equipped, Everyman can build and sell useful products, presumably buy more components and everyone's interests (not incidentally, including ours) are served.

As author, I must confess that I am more poet than switching regulator designer, and my poetry ain't very good. Before this effort, my enthusiasm level for switchers resided somewhere between trepidation and terror. This position has changed to one of cautiously respectful optimism. Several things aided this transformation and significantly influenced this publication. The "encouragement" of the Captains of this corporation, emphasized over the last year at increasingly insistent levels, constituted one form of inspiration. Conversations with users (or people who wanted to be) provided more valuable perspective and strength in the knowledge that I was not alone in my difficulties with switchers.

At the circuit level, a significant decision was to employ standard, off-the-shelf magnetics exclusively.¹ This policy was driven by the observation that the majority of problems encountered with switchers centered around inductive components. This approach almost certainly prevents precisely-optimized performance and may horrify some veteran switcher designers. It also eliminates inductor construction uncertainties, saves time and greatly increases the likelihood of getting a design running. It's

NOTE 1: For recommended magnetics supplier, see page 13.

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Application Note 25

much easier to work with, and get enthusiastic about, a functional circuit than the smoking carcass of a devastated breadboard. If standard inductor characteristics aren't optimal, it's easier to see the evidence on a 'scope than to guess why you don't see anything.

Additionally, once the circuit is running, an optimized version of the standard product can be supplied by the inductor manufacturer. It's generally easier for the inductor manufacturer to modify its standard product than to start from scratch. The process of communicating and translating circuit performance requirements into inductor construction details is tricky. Using standard product as a starting point accelerates the dialogue, minimizing the number of iterations required for satisfactory results. Often, the standard product suffices for the purpose and no further effort is required.

Strictly speaking, it makes more sense to design the inductor to meet circuit requirements than to fashion a circuit around a standard inductor. Deliberately ignoring this consideration considerably complicated the author's work, but hopefully will simplify the reader's (such is the lot of an application note writer's life). Those interested in inductor design theory are commended to LTC Application Note AN-19, "LT[®]1070 Design Manual."

A final aid in achieving my new outlook on switchers was the LT1070 family. In terms of circuit construction and ease of use they really are superior switching regulator ICs. A 75V, 5A (LT1070HV) on-chip power switch, complete control loop, oscillator and only 5 pins eliminate a lot of the ambiguity of other devices. Internal details and operating features of the LT1070 family are detailed in Appendix A, "Physiology of the LT1070."

Basic Flyback Regulator

Figure 1 shows a basic flyback regulator using the LT1070. It converts a 5V input to a 12V output. Figure 2 shows the voltage (Trace A) and the current (Trace B) waveforms at the V_{SWITCH} pin. The V_{SW} output is the collector of a common emitter NPN, so current flows when it is low. Current is pulled through the 100 μ H inductor and controlled to a value of which forces the 12V output to be constant. The circuit's 40kHz repetition rate is set by the LT1070's internal oscillator. During the time V_{SW} is low, current flow through the inductor causes a magnetic field

to be induced into the area around the inductor. The amount of energy stored in this field is a function of the current level, how long current flows, the characteristics of the inductor and its core material. It is often useful to think of the inductor as a bucket and analogize current flow as water pouring into it. The ultimate limit on energy storage is set by the bucket's capacity, corresponding to the inductor's saturation limitations. The amount of energy that can be put into an inductor in a given time is limited by the applied voltage and the inductance. The amount of energy that can be stored without saturating the inductor is limited by the core characteristics. Size, core material, operating frequency, voltage and current influence inductor design.

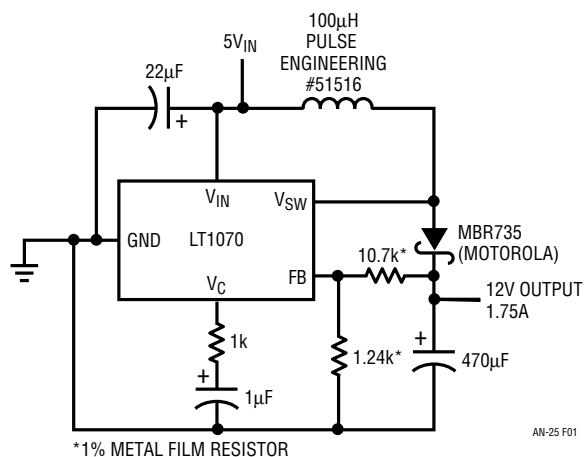


Figure 1. Flyback-Type Regulator

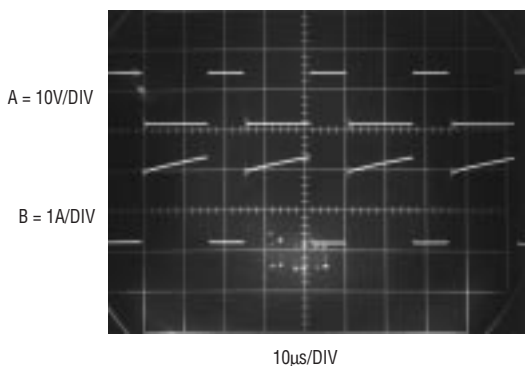


Figure 2. Flyback Regulator's Waveforms at 7W Loading

If the inductor is enclosed in a feedback-enforced loop, such as Figure 1, the energy put into it will be controlled to meet circuit output demands. Figure 3 shows what happens when output demand doubles. In this case duty

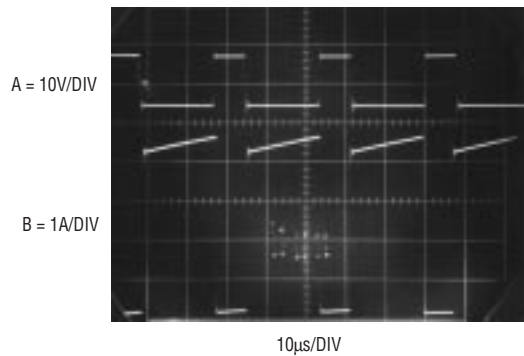


Figure 3. Flyback Regulator's Waveforms at 14W Loading

cycle doesn't change much but current doubles. This requires the inductor to store more energy. If it couldn't meet the storage requirement, e.g., it saturated and could not hold any more magnetic flux, it would cease to look inductive. If this point is reached, current flow is limited only by the resistance of the wire and rapidly builds to excessive and destructive values. This behavior is exactly the opposite of a capacitor, where current diminishes upon entering saturation. Capacitors can maintain energy storage with no current flowing; inductors cannot. See Appendix C, "A Checklist for Switching Regulator Designs," for details.

At the end of each inductor charge cycle, current flow in the inductor decays, and the magnetic field around it abruptly collapses. The V_{SW} pin is seen to rise rapidly to a voltage higher than the 5V input. This flyback action gives the regulator its voltage boost characteristics and its name. The boost characteristic is caused by the collapsing magnetic field's lines of flux cutting across the inductor's conductive wire turns. This satisfies the basic requirement for generation of a current in (and hence, a voltage across) a conductor. This moving magnetic field deposits energy into the wire in proportion to how much was stored in the core during the current charge cycle. It is worth noting that the operating characteristics shown here are similar to the Kettering ignition system used in automobiles, explaining why spark occurs when the points open.²

In this circuit the flyback is seen to clamp to a level just above the output voltage. This is so because the flyback pulse is steered through the Schottky diode to the output. The 470 μ F capacitor integrates the repetitive flyback events to DC, providing the circuit's output. The feedback pin (FB)

samples this output via the 10.7k to 1.24k divider. The LT1070 compares the feedback pin voltage to its internal 1.24V reference and controls the V_{SW} pin's duty cycle and current, closing a loop. Since the LT1070 is trying to force its feedback pin to 1.24V, output voltage may be set by varying the 10.7k or 1.24k values.

All feedback loops require some form of stability compensation (see the appended section of LTC Application Note AN-18, "The Oscillation Problem—Frequency Compensation Without Tears," for general discussion). The LT1070 is no exception. Its voltage gain characteristics, combined with the substantial phase shift of the circuit's sampled energy delivery, ensure oscillation if uncompensated. While the large output capacitor smooths the output to DC, it also teams up with the sampled energy coming into it to create phase shift. To complicate matters, the load, which may vary, also influences phase characteristics. The regulator can only source into the output capacitor. The load determines the sink time constant, influencing phase performance and overall stability.

The LT1070's internals have been designed with all this in mind and compensation is usually fairly simple. In this case the 1k to 1 μ F combination at the compensation pin (V_C) rolls off the circuit, providing stable compensation for all operating conditions (see Appendix B, "Frequency Compensation," for details and suggestions on achieving stability in switching regulator loops).

As innocent as Figure 1 appears, it's not too difficult to get into odd and seemingly inexplicable problems. Note that the ground connection appears at the ground pin, as opposed to its customary location at the bottom of the diagram. This is deliberate and the supply and load return connections should be made there. The high speed, high current returns from the output transistor's emitter (the "other end" of the V_{SW} pin) should not be allowed to mix with the small currents of the output divider or the V_C pin.

Such mixing can promote poor regulation, unstable operation or outright oscillation. Similarly, the 22 μ F bypass capacitor ensures clean local power at the LT1070, even during the fast, high current drain periods when V_{SW} comes on. It should have good high frequency characteristics (tantalum or aluminum paralleled by a disc ceramic type). More discussion of these considerations appears in Appendix C.

NOTE 2: Back when giants walked the earth, Real Cars used ignition points.

Application Note 25

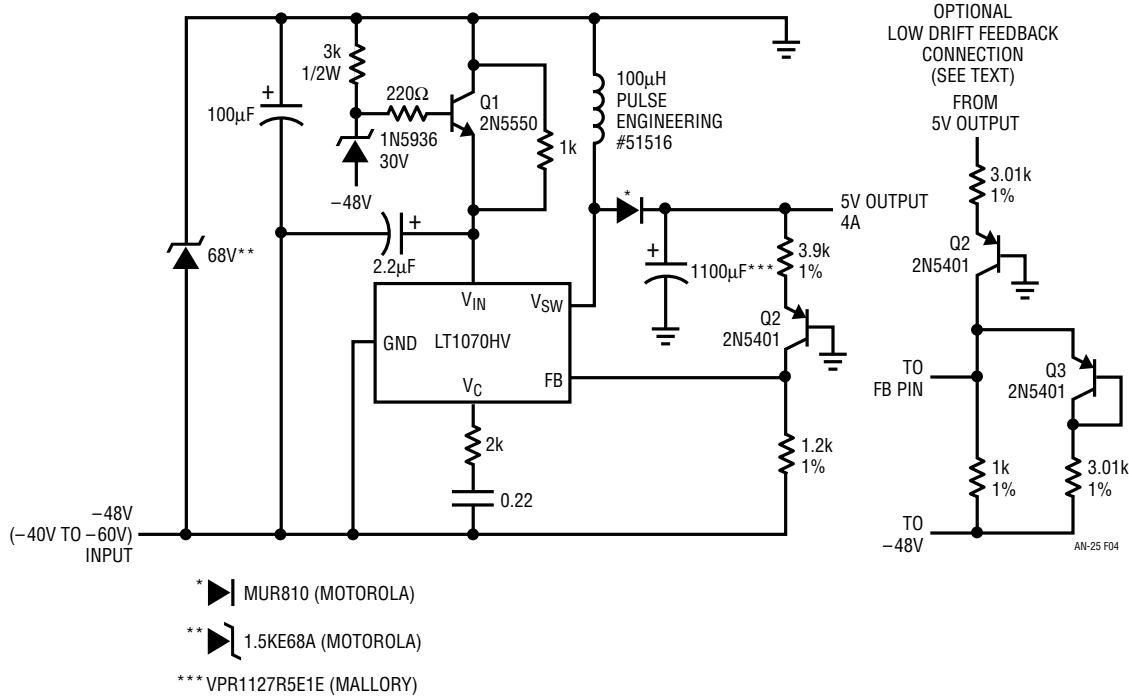


Figure 4. Nonisolated -48V to 5V Regulator

-48V to 5V Telecom Flyback Regulator

Figure 4’s circuit is operationally similar to Figure 1 but is intended for telecom applications. The raw telecom supply is nominally -48V but can vary from -40V to -60V. This range of voltages is acceptable to the V_{SW} pin but protection is required for the V_{IN} pin ($V_{MAX} = 60V$). Q1 and the 30V zener diode serve this purpose, dropping V_{IN} ’s voltage to acceptable levels under all line conditions.

Here, the “top” of the inductor is at ground and the LT1070’s ground pin at -48V. The feedback pin senses with respect to the ground pin, so a level shift is required for the 5V output. Q2 serves this purpose, introducing only $-2mV/^\circ C$ drift. This is normally not objectionable in a logic supply, but can be compensated with the optional appropriately scaled diode-resistor shown.

Frequency compensation is similar to Figure 1, although a low ESR (equivalent series resistance) capacitor gives less phase shift, permitting faster loop response with the reduced compensation time constant. The 68V zener is a type designed to clamp and absorb excessive line

transients which might otherwise damage the LT1070 (V_{SW} maximum voltage is 75V).

Figure 5 shows operating waveforms at the V_{SW} pin. Trace A is the voltage and Trace B the current. Switching characteristics are fast and clean. The ripples in the current trace are due to nonoptimal breadboard layout (ground as I say, not as I do). Inductor ringing on turn-off (Trace A) is characteristic of flyback configurations.

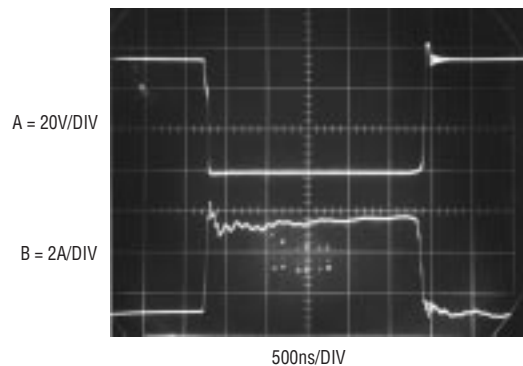


Figure 5. Nonisolated Regulator’s Waveforms

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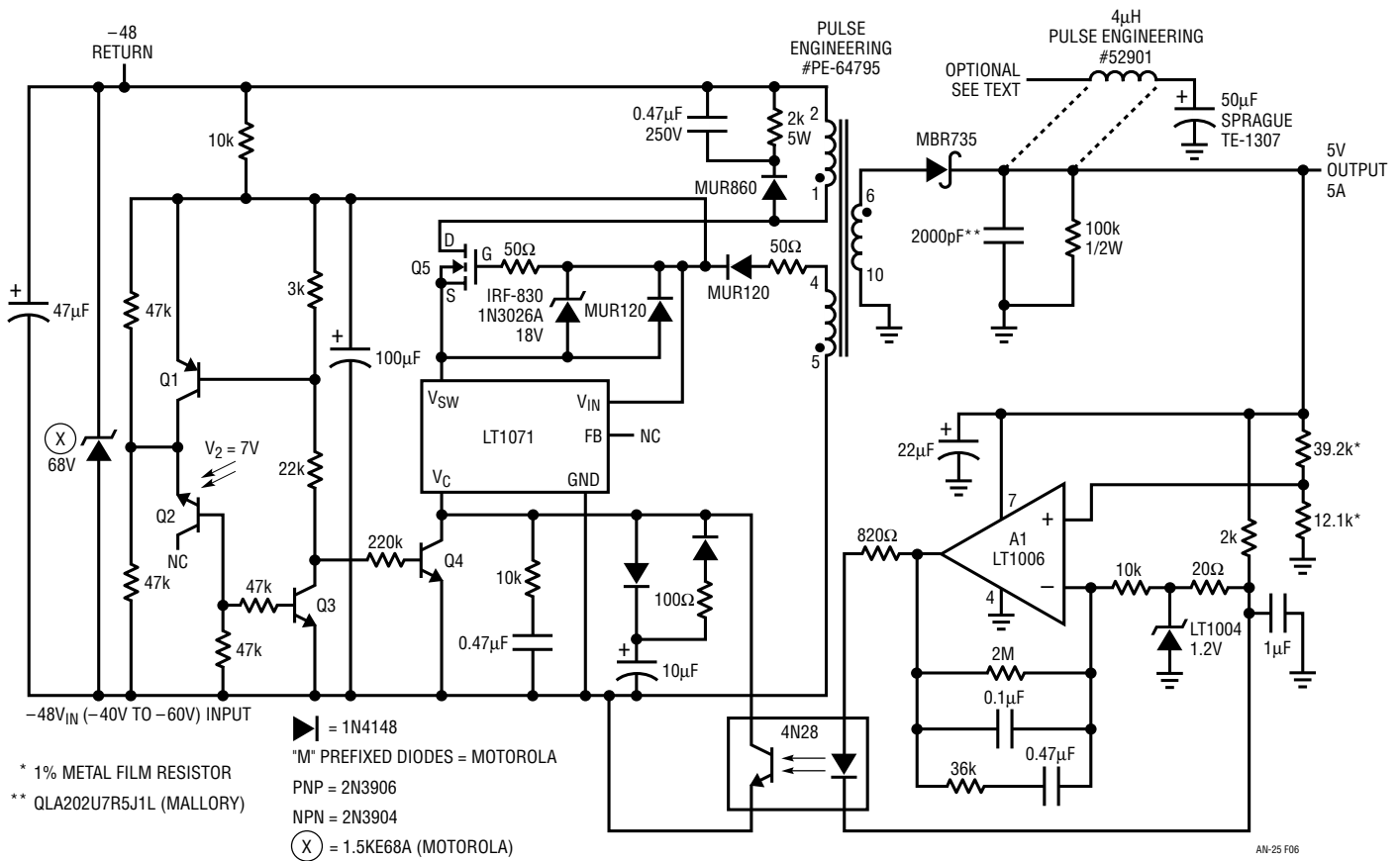


Figure 6. Fully Isolated -48V to 5V Regulator

Fully-Isolated Telecom Flyback Regulator

Figure 6's circuit is another telecom regulator. Although it looks more complex, it's really a closely related extension of the previous flyback circuits. The fundamental difference is that the output is fully galvanically isolated from the input, often a requirement in equipment. This necessitates a transformer instead of a simple 2-terminal inductor. It also requires output feedback information to be transmitted to the regulator across a nonconducting path. The transformer complicates the circuit's start-up and switching characteristics while the isolated feedback requires attention to frequency compensation.

In this circuit the V_{IN} pin receives power from a transformer winding. This winding cannot supply power at start-up because the circuit is nonfunctional. Q1 through Q4 address this issue. When power is applied, Q5 cannot conduct because the LT1071 is unpowered. Q1 zener-

connected Q2 and Q3 are off. Under these conditions Q4 is on, pulling the V_C pin down and strobing off the LT1071. The potential at Q1's emitter slowly rises as the 10k-100µF combination charges. When Q1's emitter rises high enough, it turns on. Zener-connected Q2 conducts when the voltage across it is about 7V, biasing Q3 on. Q1 sees regenerative feedback, turning Q3 on harder. Q3's turn-on cuts off Q4, allowing the V_C pin to rise and biasing up the LT1071. The rate of rise is limited by the 10µF diode combination at the V_C pin. This network forces the V_C pin to come up slowly, providing a soft-start characteristic (the 100Ω diode string discharges the 10µF capacitor when circuit input power is removed). Because of this sequence, the LT1071 cannot start up the circuit until the V_{IN} potential is well established. This prevents start-up at "starved" or unstable V_{IN} voltages which could cause erratic or destructive modes. When start-up does occur, the transformer feeds the V_{IN} pin with DC via the MUR120 diode.

Application Note 25

The 50 Ω resistor combines with the 100 μ F capacitor to give good ripple and transient filtering. This voltage is ample to run the LT1071 and reduces the current through the 10k resistor, saving power. Q1, Q2 and Q3 remain on, biasing Q4 to allow LT1071 operation.

In the previous flyback circuits, the V_{SW} pin drove the inductor directly. Here, a power MOSFET is interposed between the V_{SW} pin and the inductor. In this arrangement the inductor is a transformer and its flyback characteristics are different from a simple 2-terminal inductor. For the simple inductor, the flyback energy was clamped by and dumped directly into the output capacitor. Excessive voltages did not occur. In the transformer case, all the flyback energy does not end up in the output capacitor. Substantial flyback voltage spikes (>100V) appear across the transformer primary when the LT1071 driven MOSFET turns off.

Several measures prevent these spikes from destroying the circuit. The 0.47 μ F-2k-diode combination, a damper network, conducts during the flyback event. This loads the transformer primary, minimizing flyback amplitude. The damper values are selected empirically, with the trade-off being power dissipation in them. Very low values markedly reduce flyback potentials but cause excessive dissipation. High values permit low dissipation but allow excessive flyback voltages. The damper values should be selected under fully-loaded output conditions because flyback energy is proportionate to transformer power levels. Appendix C contains additional information on damper network considerations.

Even with the damper network, the flyback voltage is too high for the LT1071 output transistor. Q5 prevents the LT1071 from seeing the high voltage. It is connected in series with the LT1071's output transistor. This connection, sometimes called a cascode, lets Q5 stand off the high voltage and the LT1071 operates well within its breakdown limits. Development and testing of this configuration is detailed in Appendix D. Q5 has large parasitic capacitances associated with all terminals. During

switching, these capacitances can cause excessive transient voltages to appear. The 18V zener diode insures against gate-source breakdown ($V_{GS\text{MAX}} = 20\text{V}$) and the diode clamps the V_{SW} pin to the V_{IN} potential. Mention of these considerations appears in Appendix C.

The transformer's rectified and filtered secondary produces the 5V output. This output is galvanically isolated from the circuit's input. To preserve this desired feature, the feedback path must also be galvanically isolated. A1, the optoisolator and their associated components serve this function. A1, powered by the 5V output, compares a resistively-sampled portion of the output with the LT1004 1.2V reference. Operating at a gain of 200, it drives the optoisolator's LED. The optoisolator's output transistor biases the LT1071's V_C pin, closing a regulation loop. The feedback amplifier inside the LT1071 is essentially bypassed by the A1 optoisolator combination and is not used. Normally, the optoisolator's drift transmission characteristics over time and temperature would result in unstable feedback. Here, A1's gain is placed ahead of the optoisolator. This attenuates these uncertainties, providing a stable loop. This approach is not too different from inside-the-loop booster transistors and buffers used with op amps. Both schemes rely on the op amp's gain to eliminate uncertainties and drifts. Returning the optoisolator to V_{REF} instead of ground forces the op amp to bias well above ground, minimizing saturation effects during output transients.

Frequency compensation is somewhat more involved in this circuit than the previous examples. A1 is rolled off by the 0.1 μ F unit. This keeps gain low at high frequency, preventing amplified ripple and noise from being fed back to the LT1071. Local compensation at the LT1071 V_C pin stabilizes the loop. The 100 Ω resistor at the 5V output, a deliberate sink path, allows loop stability at light or no load. Appendix B discusses frequency compensation.

Additional transformer secondary windings could be added if desired. The input zener clips transient voltages.

Circuit waveforms appear in Figure 7. Trace A is Q5's drain voltage and Trace B the drain current. Trace A shows that the MOSFET sees about 100V due to flyback effects, but this is well within its rating. The ringing on turn-off is normal and is similar to the waveform observed in Figure 4's circuit. Trace B shows that the current flow is fast, clean and controlled. Figure 8 shows transient response for a 1A step on a 2.5A output. When Trace A goes high the step occurs. Trace B shows that output sag is corrected in about 8ms. When Trace A returns low the 1A load is removed and recovery is similar to the positive step. Broadband output noise, about 75mV_{P-P}, may be reduced with the optional filter shown.

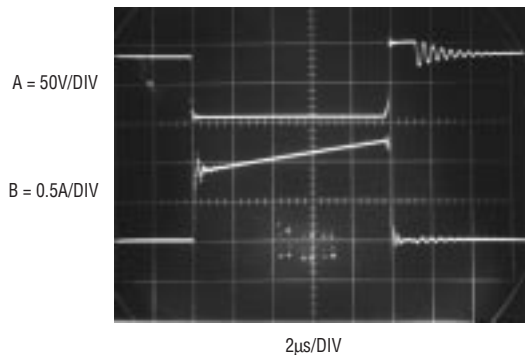


Figure 7. Fully Isolated Regulator's Waveforms

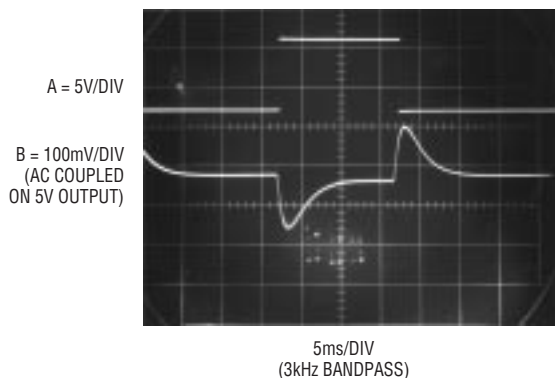


Figure 8. Fully Isolated Regulator's Transient Response for a 1A Change on a 2.5A Load

100W Off-Line Switching Regulator

One of the most desirable switching regulator circuits is also one of the most difficult to design. Figure 9's circuit has many similarities to the previous design but is powered directly from the 115V AC line. This off-line operation is desirable because it eliminates large, heavy and inefficient 60Hz magnetics and filter capacitors. The circuit provides an isolated 5V, 20A output as well as isolated $\pm 12V$, 1A outputs. Additional features include operation over a 90V AC to 140V AC input range, AC line surge suppression, soft-starting and loop stability under all conditions. Efficiency exceeds 75%.

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

AC line power is rectified and filtered by the diode bridge–470 μ F combination. The MOV device provides surge suppression and the thermistor limits turn-on in-rush current. Start-up and soft-start circuitry is similar to Figure 6's circuit, with some changes necessitated by the higher input voltage. Erratic operation at extremely low AC line voltages (70V AC) is prevented by the 220k–1.24k divider. At very low AC line inputs, this divider forces the LT1071 feedback pin to a low state, shutting down the circuit. The high input voltage, typically 160V DC, means that the LT1071's internal current limit is set too high to protect the regulator if the circuit's output is shorted. Q6 and its associated components provide about 2A limiting. The LT1071's GND pin current flows through the 0.3 Ω resistor, turning on Q6 if current is too high. The 22k–50pF RC filters noise, preventing erratic Q6 operation.

Application Note 25

Q5, a power MOSFET, is cascoded with the LT1071 for high voltage switching. Circuit topology is similar to Figure 6, with Q5's voltage breakdown increased to 500V.

Additionally, the 50Ω resistor combines with the gate capacitance to slightly slow Q5's transitions, reducing high frequency harmonics. This measure eases layout considerations. The transformer's damper network borrows from Figure 6, with values reestablished for this circuit.

The A1-optocoupler-enforced feedback loop preserves the transformer's galvanic isolation, allowing the regulator output to be ground referenced. The feedback loop is also similar to Figure 6. Compensation values at A1 and the

LT1071 have changed, reflecting this circuit's different gain-phase characteristics.

ALL WAVEFORM PHOTOGRAPHS WERE TAKEN WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE CIRCUIT'S 90V AC-140V AC INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF THIS CIRCUIT MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN FIGURE 9'S CIRCUIT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.

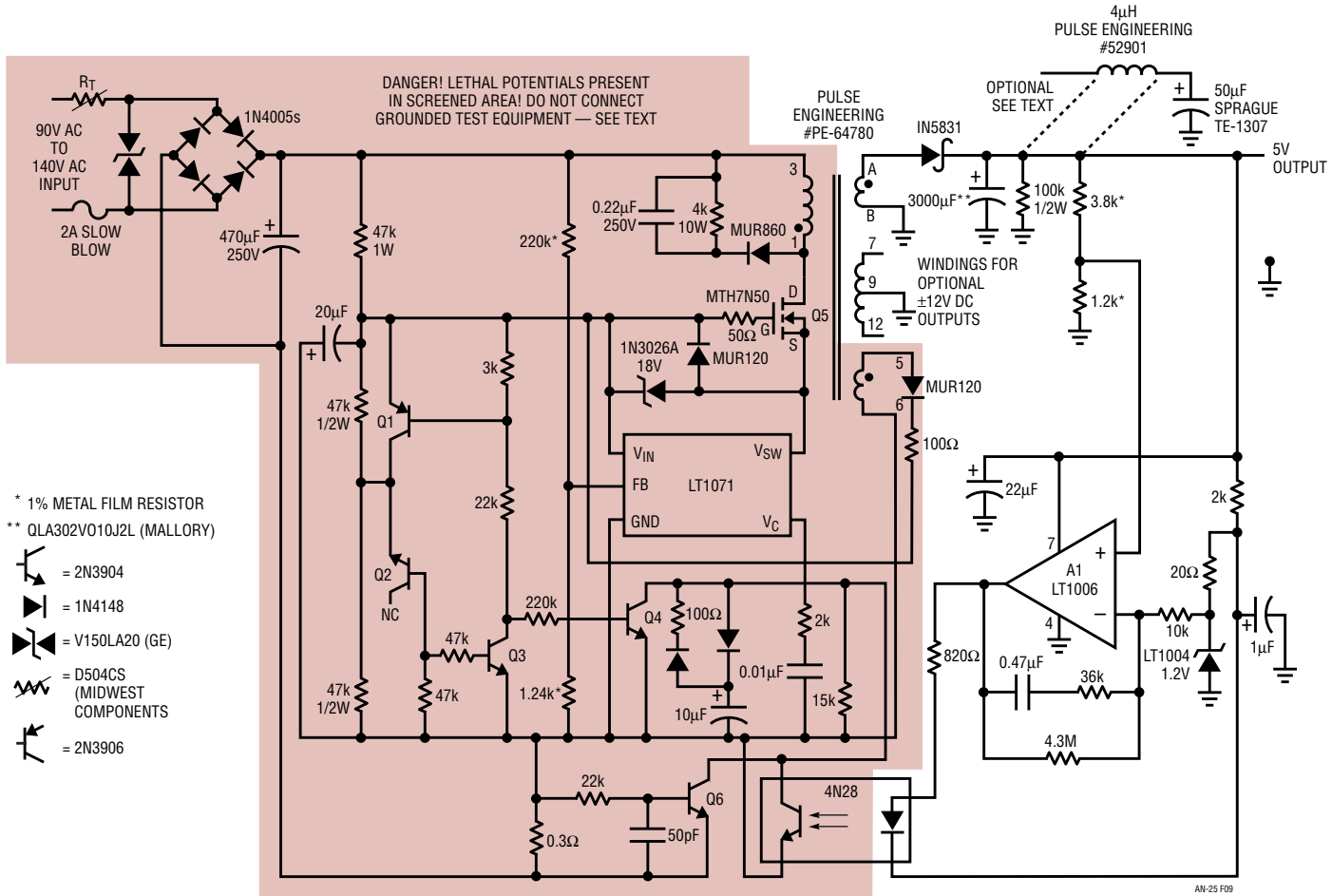


Figure 9. 100W Off-Line Switching Regulator
DANGER! Lethal Potentials Present—See Text

Figure 10 shows circuit waveforms at 15A output. Trace A, Q5's drain, shows the flyback pulse being damped below 300V (for a discussion of the procedures used to design the damper network and other design techniques in this circuit, see Appendix D, "Evolution of a Switching Regulator Design"). Trace B, the LT1071's V_{SW} pin, stays well within its voltage rating, despite Q5's high voltage switching. Trace C, Q5's drain current, shows that transformer current is well controlled with no saturation effects. Trace D, damper network current, is active when Q5 goes off.

Figure 11 is a time and amplitude expansion of Q5's drain (Trace A) and transformer primary current (Trace B). Switching is clean, with residual noise due to nonideal transformer behavior. The damper network clamps the

flyback pulse well below Q5's 500V rating and the transformer rings off after the flyback interval. The noise on the current pulse, due to resonances in the transformer, has no significant effect on circuit operation.

Figure 12 shows output noise with the optional LC filter in use. Without the filter, noise is about 150mV. Superimposed, residual 120Hz modulation accounts for trace thickening at the peaks and could be eliminated by increasing the 470 μ F value.

Figure 13 shows transient response performance. When Trace A goes high, a 5A transient is added to a 10A steady-state load. Recovery amplitude is low and clean with a first order response. When Trace A goes low, the transient load is removed with similar results.

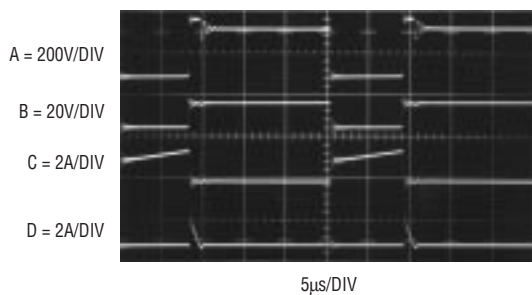


Figure 10. Off-Line Switcher's Waveforms
DANGER! Take This Measurement *Only* With an Isolation Transformer in Use—See Text

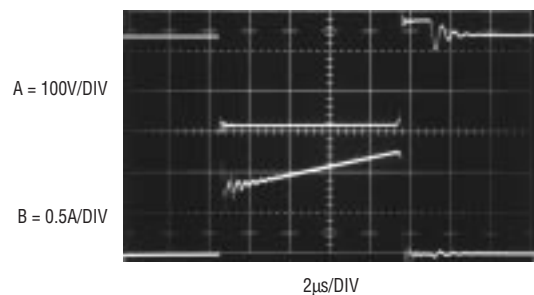


Figure 11. Detail of Off-Line Switcher's Transformer Primary Voltage and Current Waveforms
DANGER! Take This Measurement *Only* With an Isolation Transformer in Use—See Text

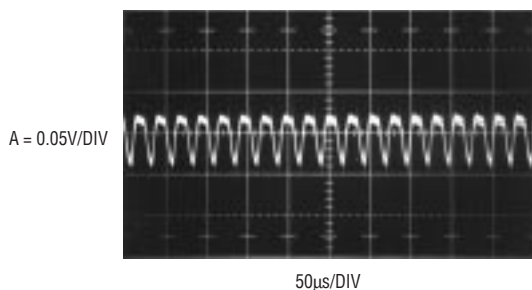


Figure 12. Figure 9's Output Ripple at 10A Output with the Optional LC Filter Added—Without the Filter, Ripple Increases to About 150mV_{p-p}

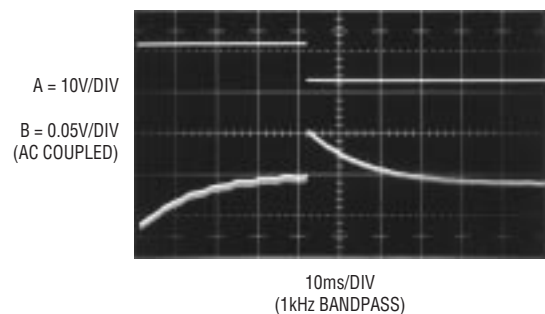


Figure 13. Figure 9's Circuit Responding to a 5A Change on a 10A Output

Application Note 25

Figure 14 shows response for shifts in the line. When Trace A is high, the AC line is at 140V AC. Line voltage drops to 90V AC with Trace A low. Trace B, the regulator's AC-coupled output, shows a clean recovery with small amplitude error. The ripples in the waveform, 120Hz input residue, could be reduced by increasing the 470 μ F capacitor.

Figure 15 shows the 5V output at start-up into a 20A load. Response is slightly underdamped and can be modified by adjusting the frequency compensation. The compensation shown in Figure 9 is a good compromise between transient response and turn-on characteristics. The delay on turn-on and the controlled rise time are due to the slow-start circuitry.

Figure 16 plots regulator efficiency. As would be expected, efficiency is best at high currents, where static losses are a small percentage of output power.

Switch-Controlled Motor Speed Controller

Voltage regulators are not the only switching power circuits. Figure 17 shows a motor speed regulator. The LT1070 provides simplicity and switch-mode control efficiency. Although this circuit controls a motor, it shares many considerations common to voltage regulators. When power is applied, the tachometer output is zero and the feedback pin (FB) is also at zero. This causes the LT1070 to begin pulsing its V_{SW} pin at maximum duty cycle. The motor turns, forcing tachometer output. When the FB pin

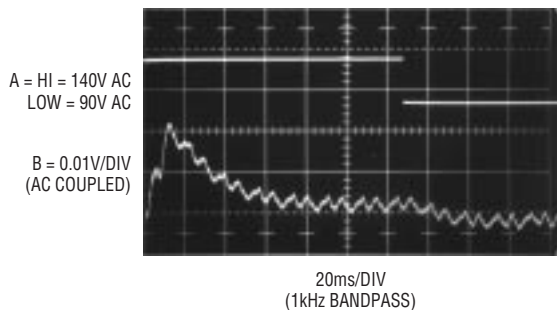


Figure 14. Figure 9 Responds to a 90V AC—140V AC Line Change—Loading is 10A—120Hz Residue in Output Could be Reduced by Increasing the 470 μ F Input Filter

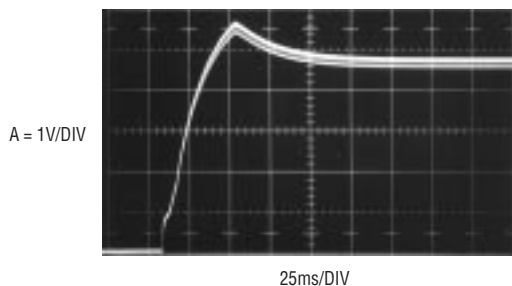
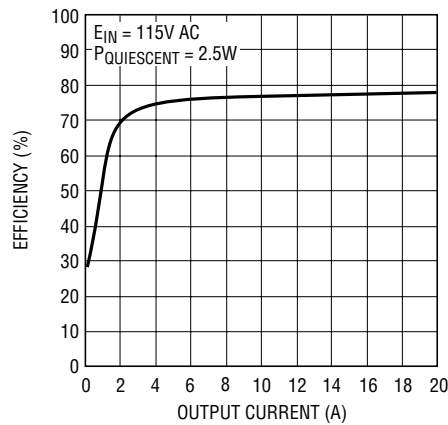


Figure 15. Start-Up for Figure 9 at 20A Loading—The 10 μ F Capacitor at the LT1070's V_C Pin Produces the Slow-Start Characteristic. If the Small Overshoot is Objectionable, Modified Frequency Compensation Can Eliminate it at Some Cost to Transient Response

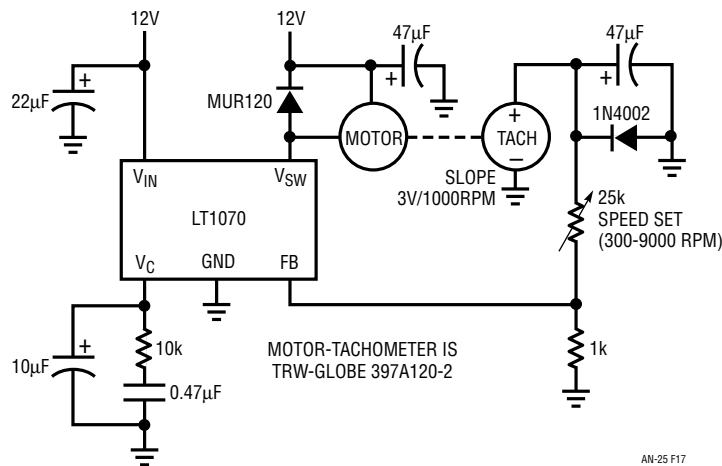
arrives at the LT1070's internal voltage reference value (1.24V), the loop stabilizes. Speed is adjustable with the 25k potentiometer in the feedback string. The MUR120 damps the motor's flyback spike. The characteristics of the motor specified permit no current limiting in series with the diode. Other motors might require this and

damper network optimization should be done for any specific unit. Similarly, frequency compensation values will vary with different motor types. The diode at the tachometer output prevents transient reverse voltages due to tachometer commutator switching.



AN-25 F16

Figure 16. Figure 9's Efficiency vs Operating Point



AN-25 F17

Figure 17. A Simple Motor-Tachometer Servo Loop

Application Note 25

Switch-Controlled Peltier 0°C Reference

Figure 18 is another switch-mode control circuit. Here, the LT1070 controls power to a Peltier cooler, providing a 0°C temperature reference for transducer calibration.

A platinum RTD is thermally mated to the Peltier cooler. The RTD combines with a bridge network to give a differential output. A1 provides maximum bridge drive without introducing significant heating in the RTD. The LTC[®]1043 switched capacitor network converts this output to a single-ended signal at A2. A2, operating at a gain of 400,

biases the LT1070's V_C pin. This closes a control loop around the Peltier cooler, forcing its temperature low enough to balance the bridge. The 0°C trim adjusts the servo point to precisely 0°C. A standard RTD should monitor Peltier temperature when making this trim. Alternately, the sensor specified should be supplied with a certified 0°C resistance. With the RTD and Peltier cooler tightly mated, stability is excellent. Figure 19, a plot of stability over hours in a 25°C \pm 3°C ambient, shows a 0.15°C baseline.

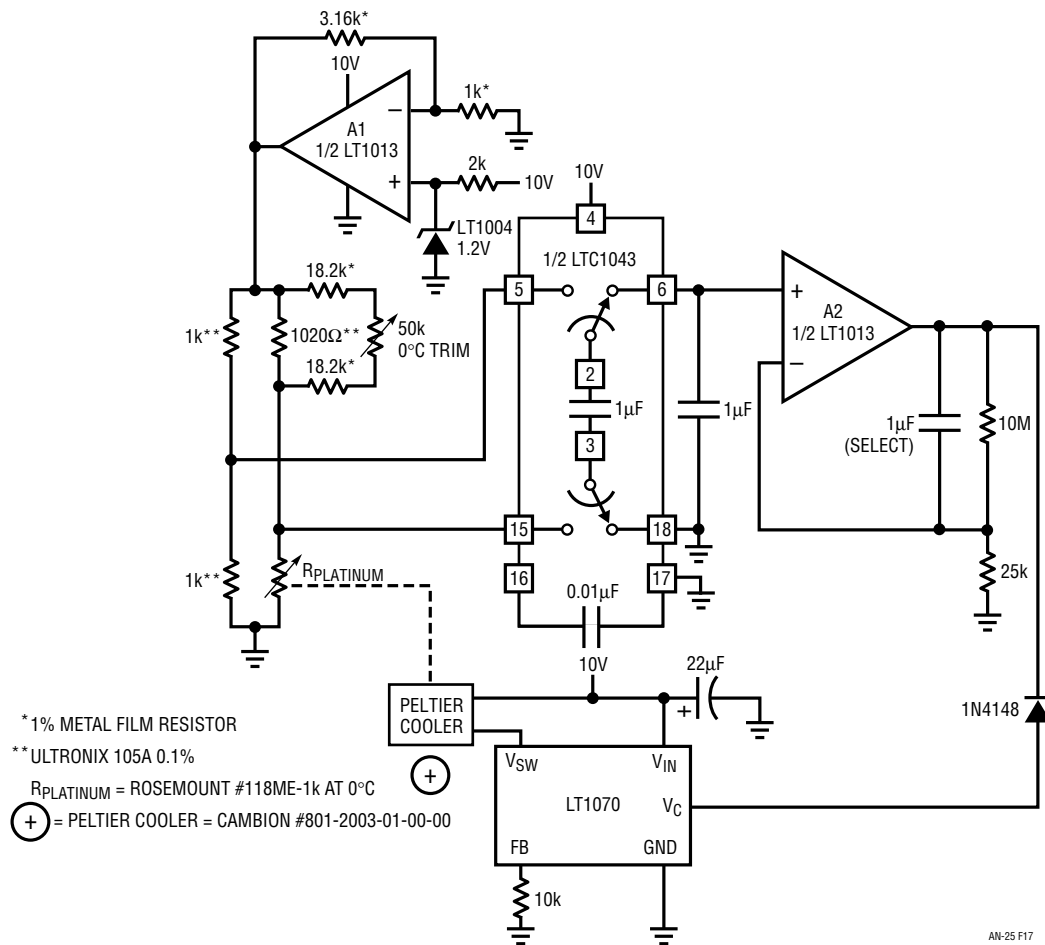


Figure 18. A Peltier-Cooled Switched-Mode 0°C Reference

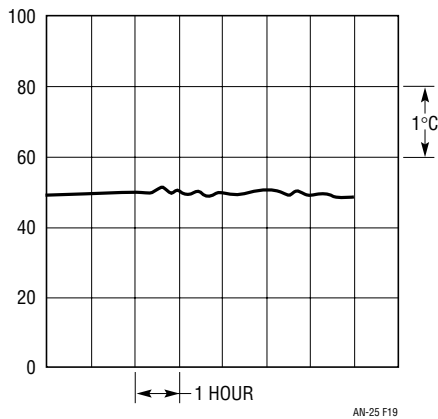


Figure 19. Stability of Figure 18's Circuit Over Many Hours with a 25°C ±3°C Ambient

Acknowledgments

The author acknowledges Carl Nelson's abundance of commentary, some of which was useful, during preparation of this work. Bob Dobkin's thoughts and patience are also appreciated. Ron Young made significant contributions towards Figure 6's circuit. Bill McColey and other members of the Engineering staff of Pulse Engineering, Inc.³, supplied invaluable insight and assistance on magnetics issues. As usual, our customers' requests and requirements provided the most valuable source of guidance, and they are due a special thanks.

NOTE 3: P.O. Box 12235, San Diego, CA 92112 (619/268-2400)

APPENDIX A

Physiology of the LT1070

The LT1070 is a current-mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to Figure A1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 6V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

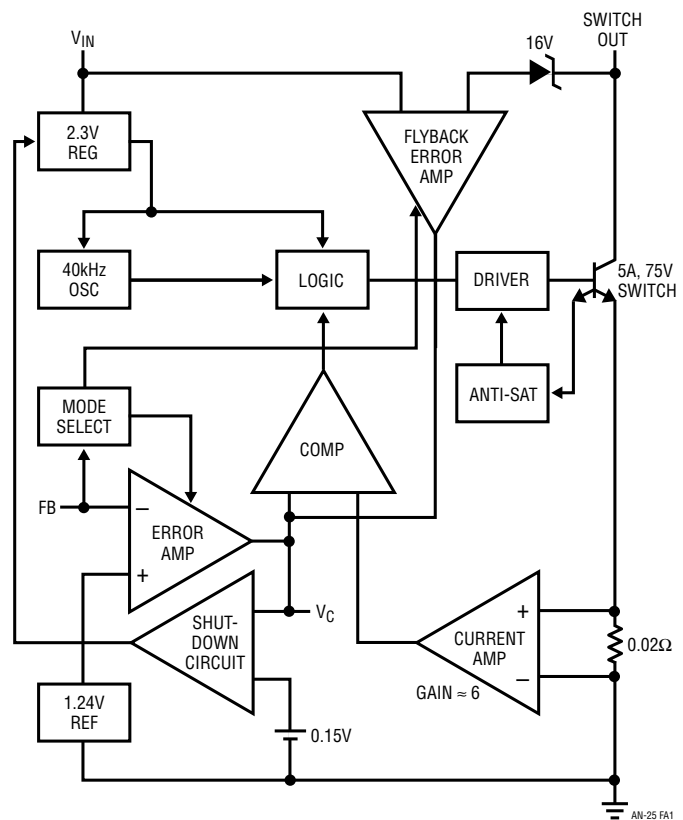


Figure A1. LT1070 Internal Details

Application Note 25

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50 μ A supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

APPENDIX B

Frequency Compensation

Although the architecture of the LT1070 is simple enough to lend itself to a mathematical approach to frequency compensation, the added complications of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage and load current variations all suggest a more practical empirical method. Many hours spent on breadboards have shown that the simplest way to optimize the frequency compensation of the LT1070 is to use transient response techniques and an R/C box to quickly iterate toward the final compensation network.

There are many ways to inject a transient signal into a switching regulator, but the suggested method is to use an AC-coupled output load variation. This technique avoids problems of injection point loading and is general to all switching topologies. The only variation required may be an amplitude adjustment to maintain small signal conditions with adequate signal strength. Figure B1 shows the setup.

A function of generator with 50 Ω output impedance is coupled through a 50 Ω /1000 μ F series RC network to the regulator output. Generator frequency is noncritical. A good starting point is 50Hz. Lower frequencies may cause a blinking scope display which is annoying to work with. Higher frequencies may not allow sufficient settling time for the output transient. Amplitude of the generator output is typically set at 5V_{P-P} to generate a 100mA_{P-P} load variation.

For lightly loaded output ($I_{OUT} < 100$ mA), this level may be too high for small signal response. If the positive and negative transition settling waveforms are significantly different, amplitude should be reduced. Actual amplitude is not particularly important because it is the shape of the resulting regulator output waveform that indicates loop stability.

A 2-pole oscilloscope filter with $f = 10$ kHz is used to block switching frequencies. Regulators without added LC output filters have switching frequency signals at their

outputs which may have much higher amplitude than the low frequency settling waveform to be studied. The filter frequency is high enough to pass the settling waveform with no distortion.

Oscilloscope and generator connections should be made exactly as shown to prevent ground loop errors. The oscilloscope is synced by connecting the channel B probe to the generator output, with the ground clip of the second probe connected to exactly the same place as the channel A ground. The standard 50Ω BNC sync output of the generator should not be used because of ground loop errors. It may also be necessary to isolate either the generator or oscilloscope from its third wire (earth ground) connection in the power plug to prevent ground loop errors in the 'scope display. These ground loop errors are checked by connecting the channel A probe tip to exactly

the same point as the probe ground clip. Any reading on channel A indicates a ground loop problem.

Once the proper setup is made, finding the optimum values for the frequency compensation network is fairly straightforward. Initially, C2 is made large ($\geq 2\mu\text{F}$), and R3 is made small ($\approx 1\text{k}\Omega$). This nearly always ensures that the regulator will be stable enough to start iteration. Now, if the regulator output waveform is single-pole overdamped (see the waveforms in Figure B2), the value of C2 is reduced in steps of about 2:1 until the response becomes slightly underdamped. Next, R3 is increased in steps of 2;1 to introduce a loop "zero." This will normally improve damping and allow the value of C2 to be further reduced. Shifting back and forth between R3 and C2 variations will now allow one to quickly find optimum values.

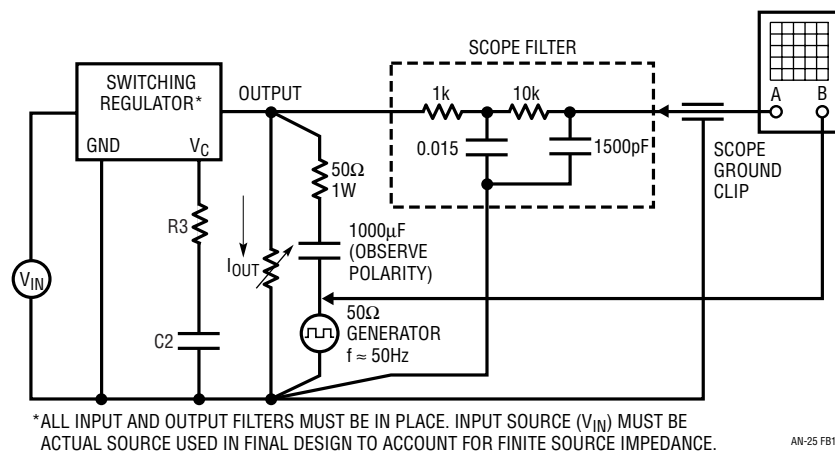


Figure B1. Testing Loop Stability

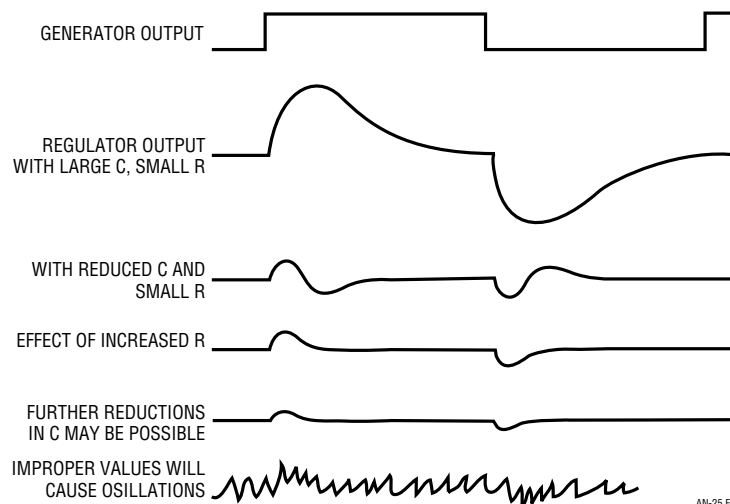


Figure B2. Output Transient Response

Application Note 25

If the regulator response is underdamped with the initial large value of C, R should be increased immediately before larger values of C are tried. This will normally bring about the overdamped starting condition for further iteration.

Just what is meant by “optimum values” for R3 and C2? This normally means the smallest value for C2 and the largest value for R3, which still guarantee no loop oscillations, and which result in loop settling that is as rapid as possible. The reason for this approach is that it minimizes the variations in output voltage caused by input ripple voltage and output load transients. A switching regulator which is grossly overdamped will never oscillate but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It may also suffer from excessive overshoot problems on start-up or short-circuit recovery.

To guarantee acceptable loop stability under all conditions, the initial values chosen for R3 and C2 should be checked under all conditions of input voltage and load current. The simplest way to accomplish this is to apply load currents of minimum, maximum, and several points in between. At each load current, input voltage is varied

from minimum to maximum while observing the settling waveform. The additional time spent “worst-casing” in this manner is definitely necessary. Switching regulators, unlike linear regulators, have large shifts in loop gain and phase with operating conditions. If large temperature variations are expected for the regulator, stability checks should also be done at the temperature extremes. There can be significant temperature variations in several key component parameters which affect stability—in particular, input and output capacitor values and their ESRs and inductor permeability. The LT1070 parametric variations also need some consideration. Those which affect loop stability are error amplifier gm, and the transfer function of V_C pin voltage versus switch current (listed as a transconductance under electrical specifications.) For modest temperature variations, conservative overdamping under worst-case temperature conditions is usually sufficient to guarantee adequate stability at all temperatures.

If external amplifiers or other active devices are included in the loop (e.g., Figures 6 and 9), their effects must be included in stabilizing the loop. LTC Application Note AN-18, pages 12-15, provides commentary that may be useful in these situations.

APPENDIX C

A Checklist for Switching Regulator Designs

1. The most common problem area in switching designs is the inductor and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions the current flow through it is limited only by its DC copper resistance and the source capacity. This is why saturation often results in destructive failures. Figure C1 demonstrates saturation effects. The pulse generator drives Q1, forcing current into the inductor. The diode and RC combination form a typical load. Figure C2 shows results. The voltage at Q1's collector falls when it turns on (Trace A is pulse generator output, Trace B is Q1's collector). Trace C, the inductor current, ramps in controlled fashion. When Q1 goes off, current falls and the induc-

tor rings off. In Figure C3, drive pulse width is longer, allowing more inductor current buildup. This requires the inductor to store more magnetic flux. Its ramp waveform is clean and controlled, indicating that it has the necessary capacity. Figure C4 brings some unpleasant surprises. Drive pulse width has been increased. Now, the inductor current departs from its ramp characteristic into a nonlinear slope. The nonlinear behavior starts between the third and fourth vertical divisions. This curve shows a rapidly increasing current characteristic. These conditions indicate that the inductor is entering saturation. If pulse width is increased much more, the current will rise to destructive levels. It is worth noting that some inductors saturate much more abruptly than this case.

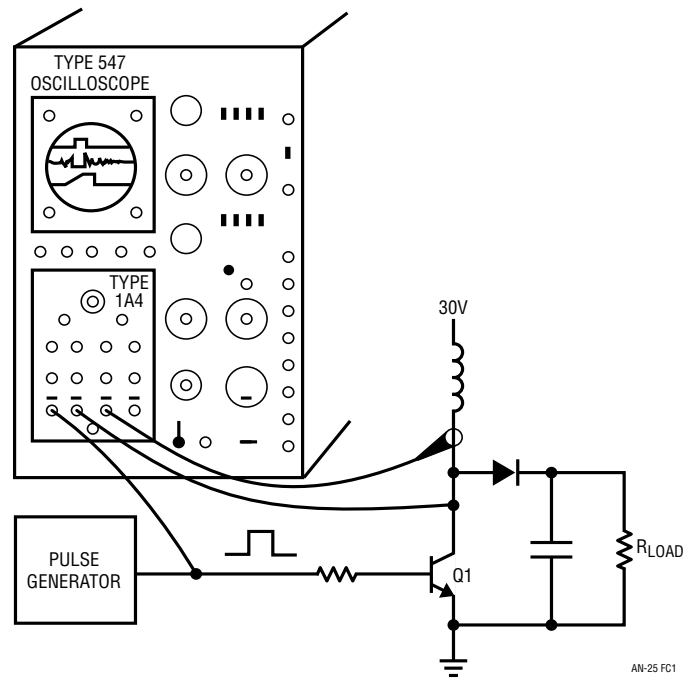


Figure C1. Inductor Saturation Test Circuit

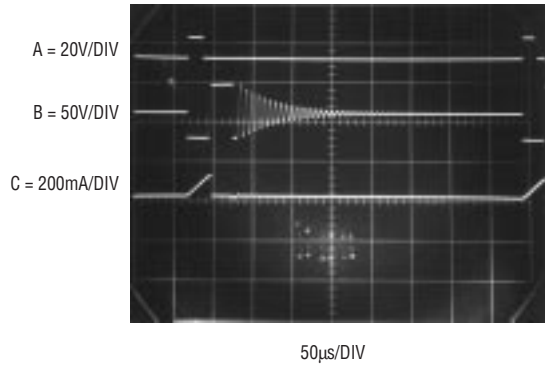


Figure C2. Normal Inductor Operation

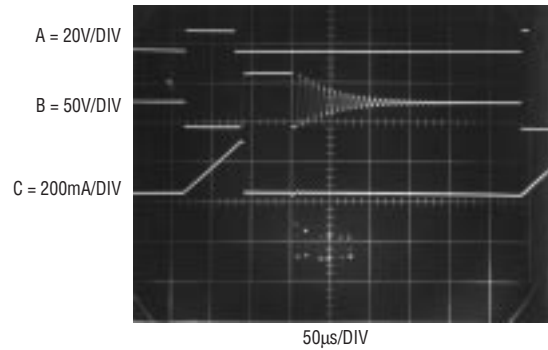


Figure C3. Normal Inductor Operation at Increased Current

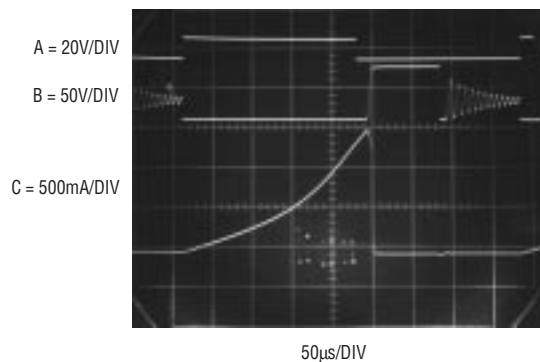


Figure C4. Inductor Being Driven into Saturation

Application Note 25

2. Always consider inductive flyback effects. Are semiconductor breakdown ratings adequate to withstand them? Is a snubber (damper) network required? Consider all possible voltages and current paths, including the transient ones via semiconductor junction capacitances, to avoid evil problems.
3. Think about requirements in capacitors. All operating conditions should be accounted for. Voltage rating is the most obvious consideration, but remember to plan for the effects of equivalent series resistance (ESR) and inductance. These specifications can have significant impact on circuit performance. In particular, an output capacitor with high ESR can make loop compensation difficult.
4. Layout is vital. Don't mix signal, frequency compensation, and feedback returns with high current returns. Arrange the grounding scheme for the best compromise between AC and DC performance. In many cases, a ground plane may help. Account for possible effects of stray inductor-generated flux on other components and plan layout accordingly.
5. Semiconductor breakdown ratings must be thought through. Account for all conditions. Transient events usually cause the most trouble, introducing stresses that are often hard to predict. Things to watch for include effects of feedthrough via semiconductor junction capacitances (note the clamping of Q5's gate in Figures 6 and 9). Such capacitances can allow excessive voltages to occur for brief durations at what is normally a low voltage node. Study the data sheet breakdown, current capacity, and switching speed ratings carefully. Were these specifications written under the same conditions that your circuit is using the device in? If in doubt, consult the manufacturer.

"Simple" diodes furnish a good example of how carefully semiconductor operating conditions must be considered in switching regulators. Switching diodes have two important transient characteristics—reverse recovery time and forward turn-on time. Reverse recovery time occurs because the diode stores charge during its forward

conducting cycle. This stored charge causes the diode to act as a low impedance conductive element for a short period of time after reverse drive is applied. Reverse recovery time is measured by forward biasing the diode with a specified current, then forcing a second specified current backwards through the diode. The time required for the diode to change from a reverse conducting state to its normal reverse nonconducting state is reverse recovery time. Hard turn-off diodes switch abruptly from one state to the other following reverse recovery time. They therefore dissipate very little power even with moderate reverse recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable diode dissipation during the turn-off interval. Figure C5 shows typical current and voltage waveforms for several commercial diode types used in an LT1070 flyback converter with $V_{IN} = 10V$, $V_{OUT} = 20V$, $2A$.

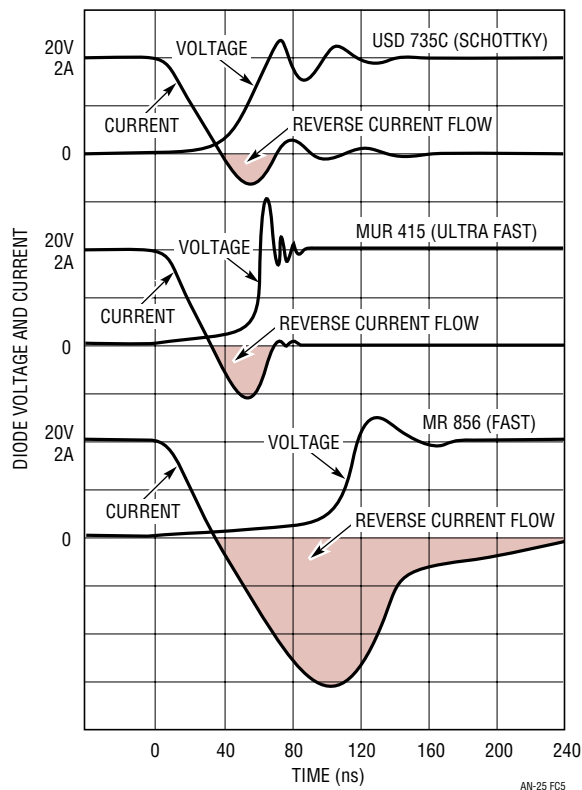


Figure C5. Diode Turn-Off Characteristics

Long reverse recovery times can cause significant extra heating in the diode or the LT1070 switch. Total power dissipated is given by:

$$P_{trr} = V \cdot f \cdot t_{RR} \cdot I_F$$

V = reverse diode voltage

f = LT1070 switching frequency

t_{RR} = reverse recovery time

I_F = diode forward current just prior to turn-off

With the circuit mentioned, I_F is 4A, $V = 20V$, and $f = 40kHz$. Note that diode on current is twice output current for this particular boost configuration. A diode with $t_{rr} = 300ns$ creates a power loss of:

$$P_{trr} = (20)(40 \cdot 10^3)(300 \cdot 10^{-6})(4) = 0.96W$$

If this same diode had a forward voltage of 0.8V at 4A, its forward loss would be 2A (average current) times 0.8V equals 1.6W. Reverse recovery losses in this example are nearly as large as forward losses. It is important to realize however, that reverse losses may not necessarily increase diode dissipation significantly. A hard turn-off diode will shift much of the power dissipation to the LT1070 switch, which will undergo a high current and high voltage condition during the duration of reverse recovery time. This has not been shown to be harmful to the LT1070, but the power loss remains.

Diode turn-on time can potentially be more harmful than reverse turn-off. It is normally assumed that the output diode clamps to the output voltage and prevents the inductor or transformer connection from rising higher than the output. A diode that turns on slowly can have a very high forward voltage for the duration of turn-on time. The problem is that this increased voltage appears across the LT1070 switch. A 20V turn-on spike superimposed on a 40V flyback mode output pushes switch voltage perilously close to the 65V limit. The graphs in Figure C6

show diode turn-on spikes for three common diode types—fast, ultrafast, and Schottky. The height of the spike will be dependent on rate of rise of current and the final current value, but these graphs emphasize the need for fast turn-on characteristics in applications which push the limits of switch voltage.

Fast diodes can be useless if the stray inductance is high in the diode, output capacitor or LT1070 loop. 20-gauge hook-up wire has 30nH/inch inductance. The current fall time of the LT1070 switch is $10^8A/sec$. This generates a voltage of $(10^8)(30 \cdot 10^{-9}) = 3V$ per inch in stray wiring. Keep the diode, capacitor and LT1070 ground/switch lead lengths *short!*

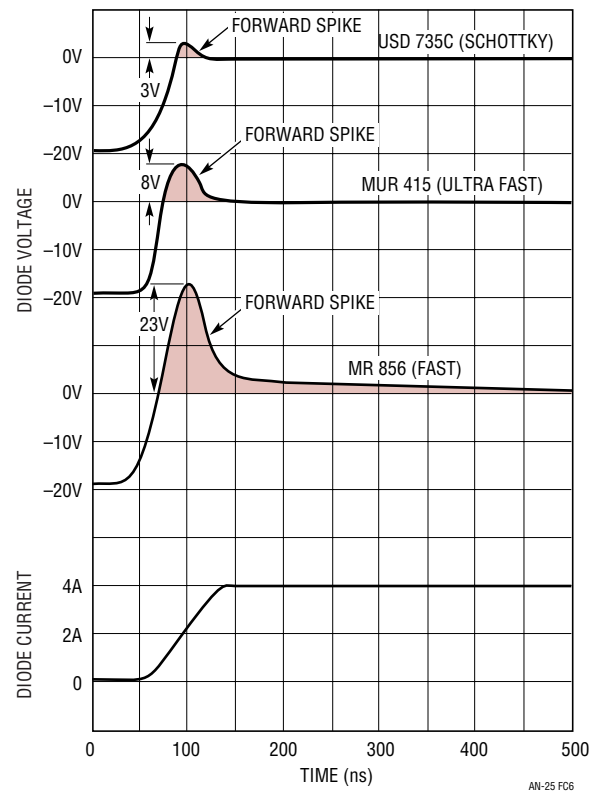


Figure C6. Diode Turn-On Spike

Application Note 25

APPENDIX D

Evolution of a Switching Regulator Design

A good way to approach designing a switching regulator is to break the problem into small tasks and then integrate everything. The combination of inductors, a sampled feedback loop, and high speed currents and voltages leaves much room for confusion. The approach used in Figure 9's design is illustrated as an example of an iterative approach in switching regulator design. This off-line circuit features high power, an isolated feedback loop and the aforementioned complexities. Any attempt to get everything working on the first try is beyond risky.

The transformer drive is the most critical part of Figure 9's design. Fast switching of over 100W at high voltage requires care. In particular, two issues must be addressed. Will the high voltage FET-LT1071 cascode connection really work? What amplitudes of flyback voltage are going to occur and what will their effects be?

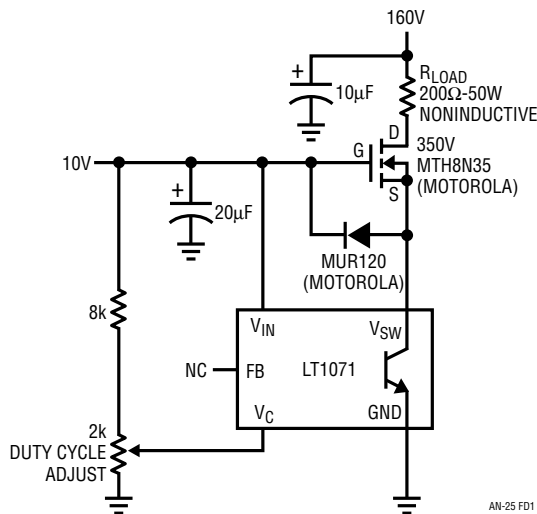


Figure D1. Test Circuit for MOSFET-LT1071 Cascode with Resistive Load

Figure D1 begins the investigation. This test circuit allows checking of the high voltage cascode. To start, a resistive load is used, eliminating the possible (certain!) complications of the inductive load. Figure D2 shows waveforms. Switching is clean. Trace A is the FET drain, while Trace B is the LT1071 V_{SW} pin. Drain current appears in Trace C. Pulse width is kept deliberately low, minimizing load power dissipation. Everything appears well ordered, and the LT1071 V_{SW} pin does not see any high voltage excursions. Artifacts of the MOSFET's high voltage switching do, however, appear at the LT1071 V_{SW} pin. On the falling edge, the ringing appears, albeit at lower amplitude. The rising edge shows a slight peaking. These effects are due to the high voltage coupling through the MOSFET's junction capacitances. The diode clamps the source to 10V, but the effects of the high voltage slewing are still noticeable. This doesn't cause much trouble with the resistive load, but what will happen with the inductor's higher flyback voltages?

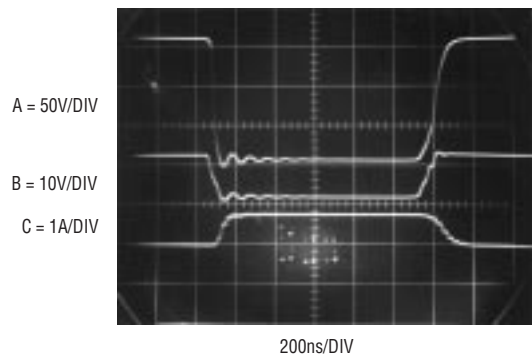


Figure D2. Testing the MOSFET-LT1071 Cascode Switch with a Resistive Load

Figure D3 shows the test circuit rearranged to accommodate the transformer load. The transformer replaces the resistor. Its terminated secondary allows it to present a significant load. The fixed 160V supply has been replaced with a 0V to 200V unit, permitting voltage to be slowly and cautiously increased¹. The 350V transistor is replaced with a 1000V unit, in preparation for inductive events. Figure D4 shows waveforms. As expected, the inductive flyback (Trace A) is significant, even at low supply voltage ($V_{\text{SUPPLY}} = 60\text{V}$ in this photo).

Trace C, the drain current, rises with a characteristic indicating the inductive load. Trace B, the source voltage, is of greater concern. The flyback event, feeding through the MOSFET's capacitances, causes the source (and gate) to rise above nominal clamped value. At the higher supply voltages planned, this could cause excessive gate-source voltages with resultant device destruction. Because of this, the zener diode in dashed lines is installed, clamping gate-source voltages to safe values. This component appears in Figure 9's final design. With this correction, behavior at higher supply voltages may be investigated.

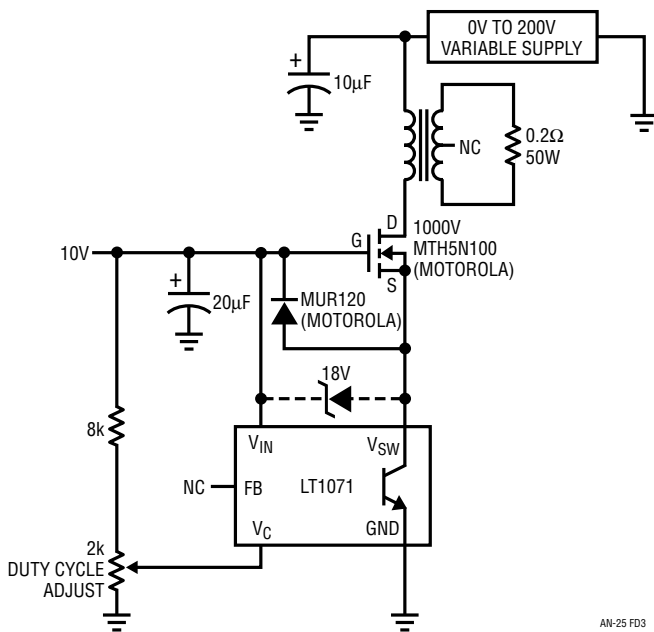


Figure D3. Test Circuit for MOSFET-LT1071 Cascode with Transformer Load

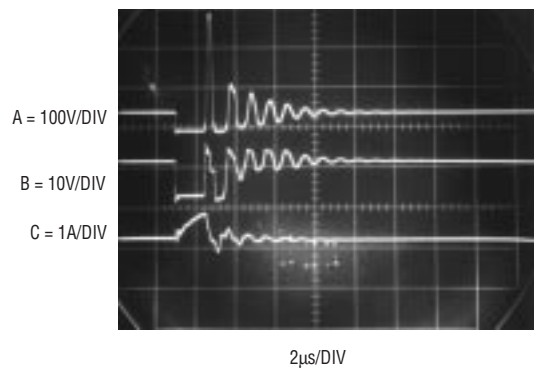


Figure D4. MOSFET-LT1071 Cascode Switching the Transformer Primary—Secondary Load is 0.2Ω

NOTE 1: "For fools rush in where angels fear to tread"—An Essay on Criticism, A. Pope.

Application Note 25

Figure D5 shows the MOSFET drain at $V_{\text{SUPPLY}} = 160\text{V}$. The load draws about 2.5A. Flyback voltage rises to 400V. At 5A loading this voltage approaches 500V (Figure D6), while a 10A load (Figure D7) forces almost 900V flyback. In actual regulator operation, supply voltages, switch on-time and output current can go higher, meaning flyback

potentials will exceed 1000V. This graphically mandates the need for a damper network. A simple reverse-biased diode or zener clipper will work, but will suffer from excessive dissipation. The network shown in Figure 9 is a good compromise between dissipation and reasonable flyback voltages.

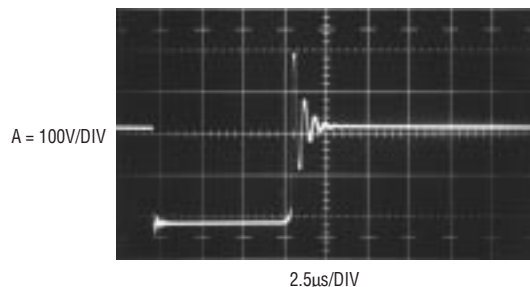


Figure D5. Undamped Regulator Flyback Pulse at 2.5A Output

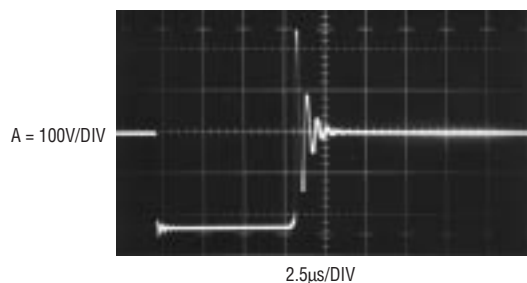


Figure D6. Undamped Regulator Flyback Pulse at 5A Output

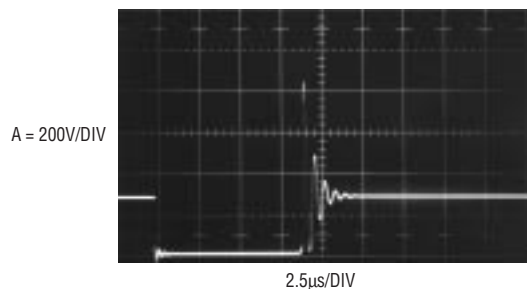


Figure D7. Undamped Regulator Flyback Pulse at 10A Output

Once the drive-flyback issues are settled, a feedback loop is closed around the transformer. This allows checking to see that loop stabilization is possible. Figure D8 diagrams the loop. In this configuration the regulator will function, but is unusable. The output is not galvanically isolated from the input, which ultimately must be directly AC line driven. After this loop has been successfully closed, the isolated version is tried (Figure D9). This introduces more

phase shift, but is also found to be stable with appropriate frequency compensation. Finally, the connection between the input and output common potentials is broken, achieving the desired galvanic isolation. The start-up, soft-start and current limit features are then added and optimized. Testing involves checking performance under various line and load conditions. Details on circuit operation are covered in the text associated with Figure 9.

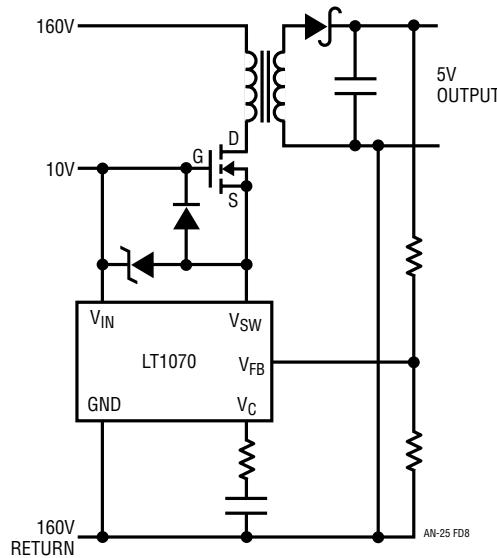


Figure D8. Developmental Version of Off-Line Switching Regulator—No Isolation is Included and the Scheme is Solely Intended to Verify that a Loop Can be Closed Around the Transformer

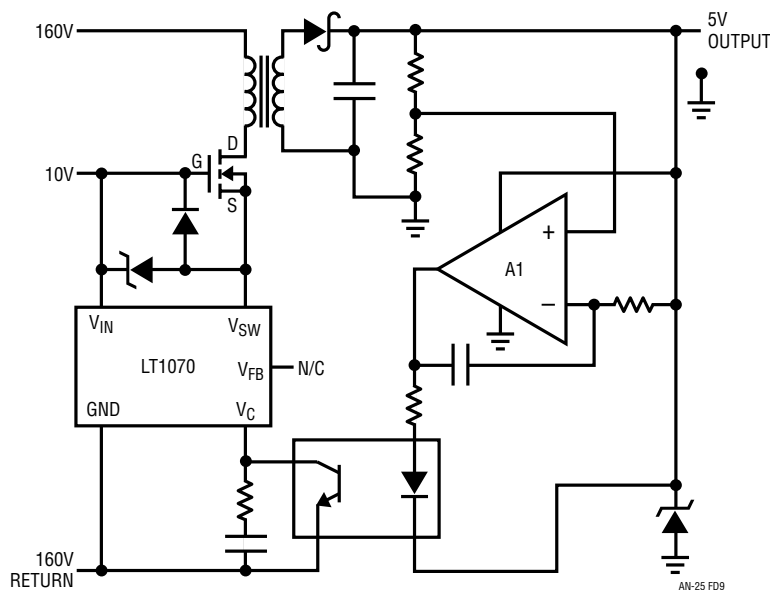
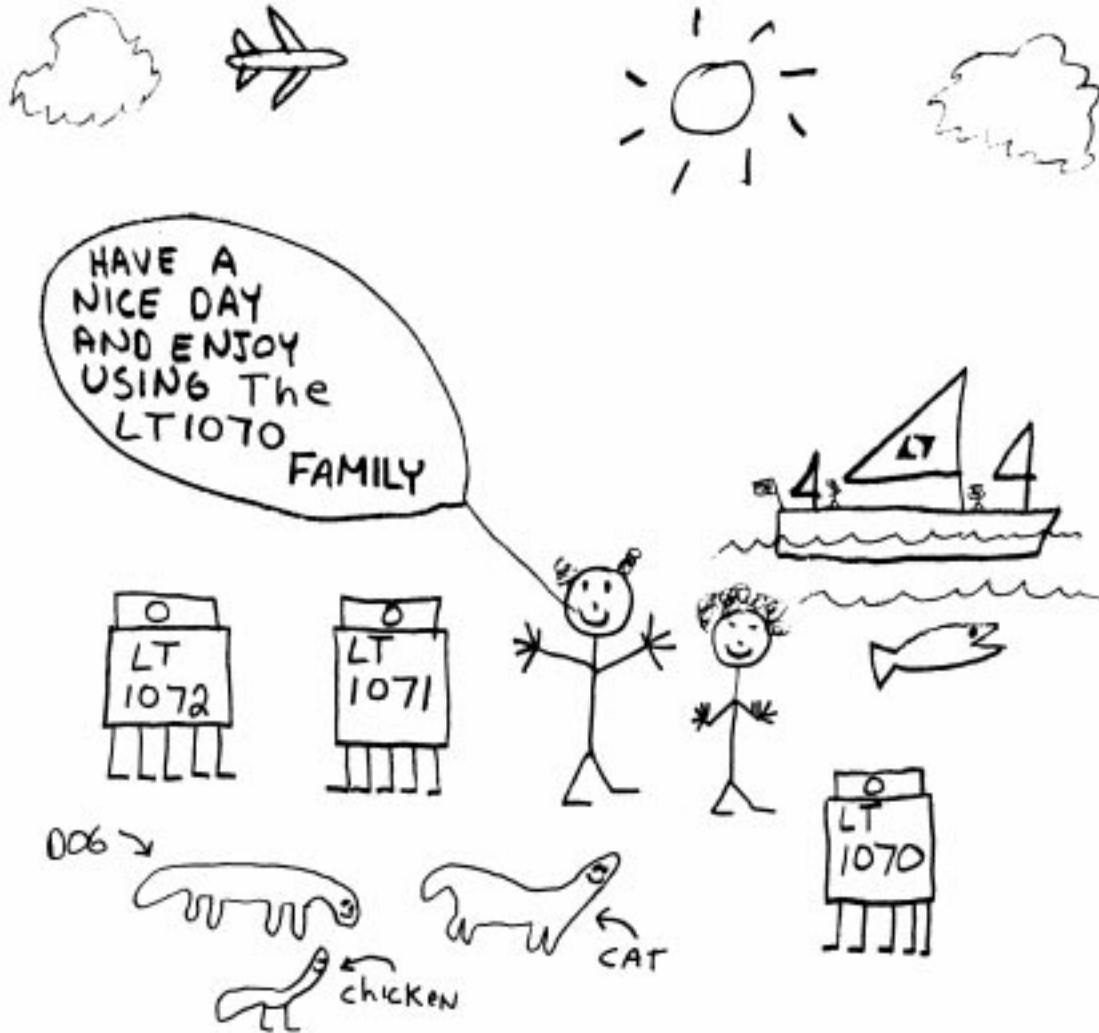


Figure D9. Developmental Version of Off-Line Regulator with Isolation—the Circuit Verifies That Loop Stability is Achievable with the Added Phase Shift of A1 and the Opto-Isolator—Start-Up, Current Limit and Soft-Start Features Must be Added to Complete the Design

an25fa

Application Note 25



(They told me I couldn't leave the last page blank)

William

'87

Thermocouple Measurement

Jim Williams

Introduction

In 1822, Thomas Seebeck, an Estonian physician, accidentally joined semicircular pieces of bismuth and copper (Figure 1) while studying thermal effects on galvanic arrangements. A nearby compass indicated a magnetic disturbance. Seebeck experimented repeatedly with different metal combinations at various temperatures, noting relative magnetic field strengths. Curiously, he did not believe that electric current was flowing, and preferred to describe the effect as “thermo-magnetism.” He published his results in a paper, “Magnetische Polarisation der Metalle und Erze durch Temperatur-Differenz” (see references).

Subsequent investigation has shown the “Seebeck Effect” to be fundamentally electrical in nature, repeatable, and quite useful. Thermocouples, by far the most common transducer, are Seebeck’s descendants.

Thermocouples in Perspective

Temperature is easily the most commonly measured physical parameter. A number of transducers serve temperature measuring needs and each has advantages and considerations. Before discussing thermocouple-based measurement it is worthwhile putting these sensors in perspective. Figure 2’s chart shows some common contact temperature sensors and lists characteristics. Study reveals thermocouple strengths and weaknesses compared to other sensors. In general, thermocouples are inexpensive, wide range sensors. Their small size makes them fast and their low output impedance is a benefit. The inherent voltage output eliminates the need for excitation.

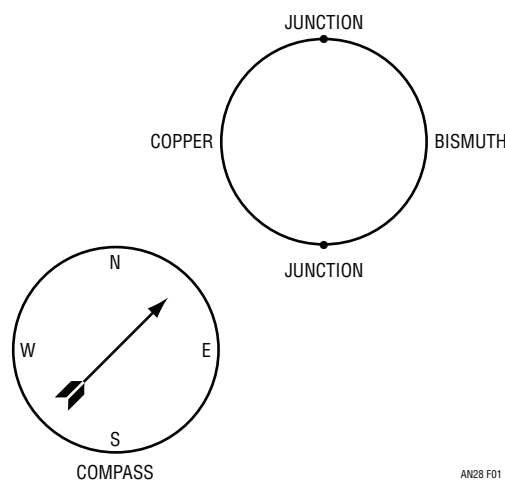


Figure 1. The Arrangement for Dr. Seebeck’s Accidental Discovery of “Thermo-Magnetism”

Application Note 28

TYPE	RANGE OF OPERATION	SENSITIVITY AT 25°C	ACCURACY	LINEARITY	SPEED IN STIRRED OIL	SIZE	PACKAGE	COST	COMMENTS
Thermocouples (All Types)	-270°C to 1800°C	Typically Less Than 50µV/°C	±0.5°C with Reference	Poor Over Wide Range, Better Over ≈100°C	Typically 1 Sec. Some Types are Faster	0.02 In. Bead Typical. 0.0005 In. Units are Available	Metallic Bead, Variety of Probes Available	\$1 to \$50 Depending On Type, Specifications and Package	Requires Reference. Low Level Output Requires Stable Signal Conditioning Components
Thermistors and Thermistor Composites	-100°C to 450°C	≈5%/°C for Thermistors. ≈0.5%/°C for Linearized Units	±0.1°C Standard from -40°C to 100°C; ±0.01°C from 0°C to 60°C Available	±0.2°C for Linearized Composite Units Over 100°C Ranges	1 to 10 Sec. is Standard; 3ms to 100ms Types are Available	Beads Can be as Small as 0.005 In., But 0.04 to 0.1 In. is Typical. "Flake" Types are Only 0.001 In. Thick	Glass, Epoxy, Teflon Encapsulated, Metal Housing, Etc.	\$2 to \$10 for Standard Units. \$10 to \$350 for High Precision Types and Specials	Highest Temperature Sensitivity of Any Common Sensor. Special Units Required for Long-Term Stability Above 100°C
Platinum Resistance Wire	-250°C to 900°C	Approximately 0.5%/°C	±0.1°C Readily Available. ±0.01°C in Precision Standards—Lab Units	Nearly Linear Over Large Spans; Typically Within 1° Over 200°C Ranges	Typically Several Seconds	1/8 to 1/4 In. Typical. Smaller Sizes Available	Glass, Epoxy, Ceramic, Teflon, Metal, Etc.	\$25 to \$1000 Depending On Specs; Most Industrial Types Below \$100	Sets Standard for Stability Over Long Term. Has Wider Temperature Range Than Thermistor, but Lower Sensitivity
Diodes and Transistors	-270°C to 175°C	-2.2mV/°C (Approx. 0.33%/°C)	±2°C to ±5°C Over -55°C to 125°C	Within 2° Over Operating Range	1 to 10 Sec. is Standard. Small Diode Packages Permit Speeds in ms Range	Standard Diode and Transistor Case Sizes. Glass Passivated Chips Permit Extremely Small Sizes	Glass, Metal	Below 50¢. Cryogenic Units More Expensive	Require Individual Calibration. Must be Driven from Current Source for Optimum Performance. Extremely Inexpensive. Calibrated Cryogenic Types Available
Integrated Circuit	-85°C to 125°C Typical	0.4%/°C Typical	Over -55°C to 125°C	Within 1° (0.2° from 0°C to 70°C) Typical	Several Seconds	TO-18 Transistor Package Size. Also MiniDIP	Metal, Plastic	\$1 to \$10	Current and Voltage Outputs Available

Figure 2. Characteristics of Some Contact Temperature Sensors (Chart Adapted from Reference 2)

JUNCTION MATERIALS	APPROXIMATE SENSITIVITY IN $\mu\text{V}/^\circ\text{C}$ AT 25°C	USEFUL TEMPERATURE RANGE ($^\circ\text{C}$)	APPROXIMATE VOLTAGE SWING OVER RANGE	LETTER DESIGNATION
Copper—Constantan	40.6	-270 to 600	25.0mV	T
Iron—Constantan	51.70	-270 to 1000	60.0mV	J
Chromel—Alumel	40.6	-270 to 1300	55.0mV	K
Chromel—Constantan	60.9	-270 to 1000	75.0mV	E
Platinum 10%—Rhodium/Platinum	6.0	0 to 1550	16.0mV	S
Platinum 13%—Rhodium/Platinum	6.0	0 to 1600	19.0mV	R

Figure 3. Temperature vs Output for Some Thermocouple Types

Signal Conditioning Issues

Potential problems with thermocouples include low level outputs, poor sensitivity and nonlinearity (see Figures 3 and 4). The low level output requires stable signal conditioning components and makes system accuracy difficult to achieve. Connections (see Appendix A) in thermocouple systems must be made with great care to get good accuracy. Unintended thermocouple effects (e.g., solder and copper create a $3\mu\text{V}/^\circ\text{C}$ thermocouple) in system connections make “end-to-end” system accuracies better than 0.5°C difficult to achieve.

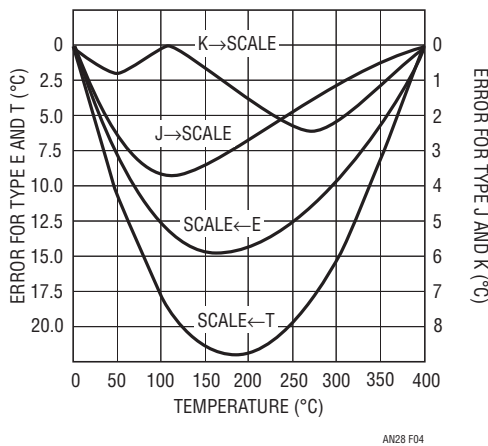


Figure 4. Thermocouple Nonlinearity for Types J, K, E and T Over 0°C to 400°C . Error Increases Over Wider Temperature Ranges

Cold Junction Compensation

The unintended, unwanted and unavoidable parasitic thermocouples require some form of temperature reference for absolute accuracy. (See Appendix A for a discussion on minimizing these effects). In a typical system, a “cold junction” is used to provide a temperature reference (Figure 5). The term “cold junction” derives from the historical practice of maintaining the reference junction at

0°C in an ice bath. Ice baths, while inherently accurate, are impractical in most applications. Another approach servo controls a Peltier cooler, usually at 0°C , to electronically simulate the ice bath (Figure 6). This approach* eliminates ice bath maintenance, but is too complex and bulky for most applications.

*A practical example of this technique appears in LTC Application Note AN-25, “Switching Regulators for Poets.”

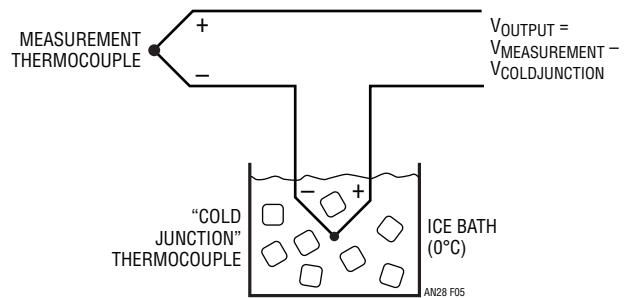


Figure 5. Ice Bath Based Cold Junction Compensator

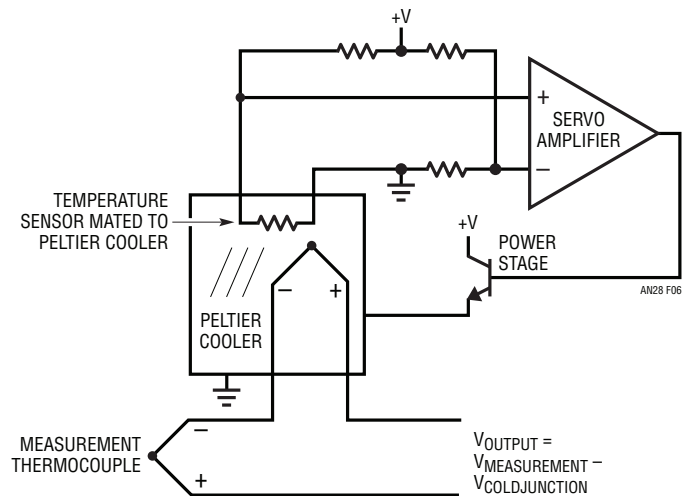


Figure 6. A 0°C Reference Based on Feedback Control of a Peltier Cooler (Sensor is Typically a Platinum RTD)

Application Note 28

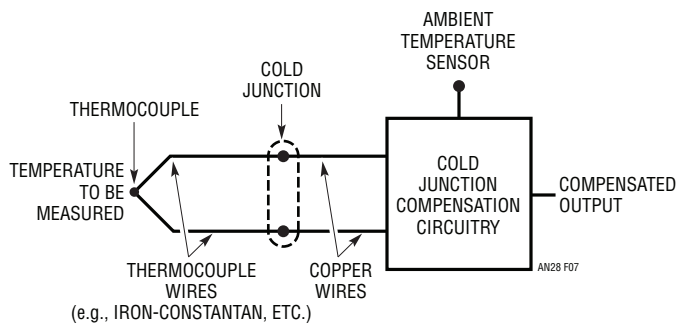


Figure 7. Typical Cold Junction Compensation Arrangement. Cold Junction and Compensation Circuitry Must be Isothermal

Figure 7 conveniently deals with the cold junction requirement. Here, the cold junction compensator circuitry does not maintain a stable temperature but tracks the cold junction. This temperature tracking, subtractive term has the same effect as maintaining the cold junction at constant temperature, but is simpler to implement. It is designed to produce 0V output at 0°C and have a slope equal to the thermocouple output (Seebeck coefficient) over the expected range of cold junction temperatures. For proper operation, the compensator must be at the same temperature as the cold junction.

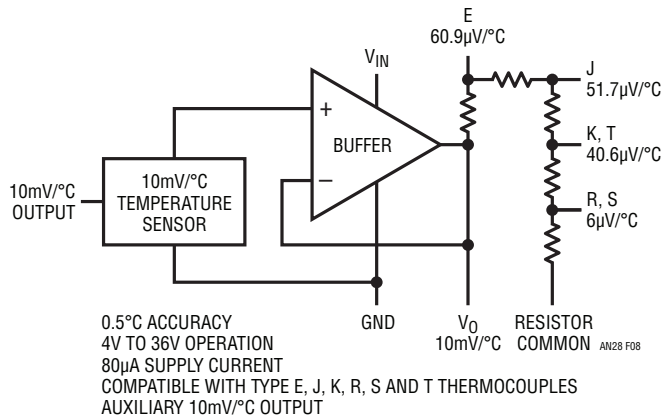


Figure 8. LT1025 Thermocouple Cold Junction Compensator

Figure 8 shows a monolithic cold junction compensator IC, the LT[®]1025. This device measures ambient (e.g., cold junction) temperature and puts out a voltage scaled for use with the desired thermocouple. The low supply current minimizes self-heating, ensuring isothermal operation with the cold junction. It also permits battery or low power operation. The 0.5°C accuracy is compatible with overall achievable thermocouple system performance. Various compensated outputs allow one part to be used with many thermocouple types. Figure 9 uses an LT1025 and an amplifier to provide a scaled, cold junction compensated output. The amplifier provides gain for the difference between the LT1025 output and the type J thermocouple. C1 and C2 provide filtering, and R5 trims gain. R6 is a typical value, and may require selection to accommodate R5's trim range. Alternately, R6 may be re-scaled, and R5 enlarged, at some penalty in trim resolution. Figure 10 is similar, except that the type K thermocouple subtracts from the LT1025 in series-opposed fashion, with the residue fed to the amplifier. The optional pull-down resistor allows readings below 0°C.

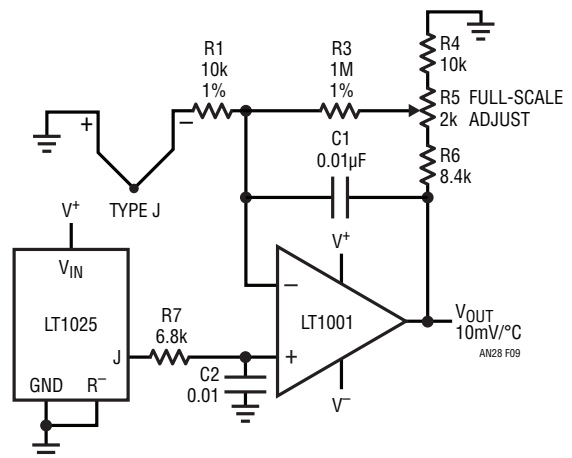


Figure 9. LT1025 Cold Junction Compensates a Type J Thermocouple. The Op Amp Provides the Amplified Difference Between the Thermocouple and the LT1025 Cold Junction Output

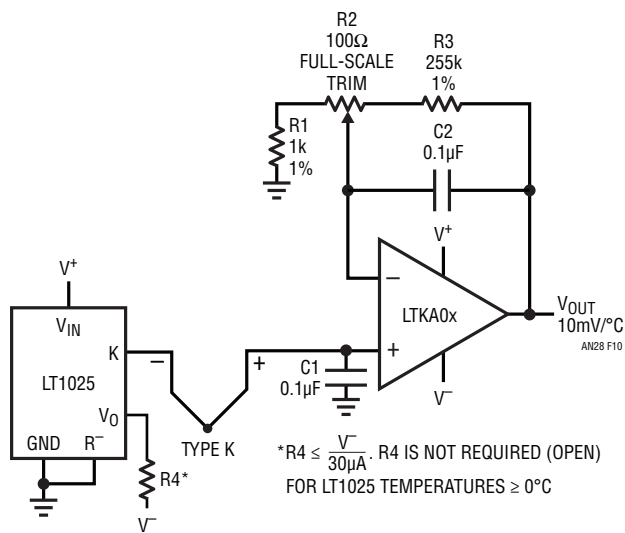


Figure 10. LT1025 Compensates a Type K Thermocouple. The Amplifier Provides Gain for the LT1025-Thermocouple Difference

Amplifier Selection

The operation of these circuits is fairly straightforward, although amplifier selection requires care.

Thermocouple amplifiers need very low offset voltage and drift, and fairly low bias current if an input filter is used. The best precision bipolar amplifiers should be used for type J, K, E and T thermocouples which have Seebeck coefficients to $40\mu\text{V}/^\circ\text{C}$ to $60\mu\text{V}/^\circ\text{C}$. In particularly critical applications, or for R and S thermocouples ($6\mu\text{V}/^\circ\text{C}$ to $15\mu\text{V}/^\circ\text{C}$), a chopper-stabilized amplifier is required. Linear Technology offers two amplifiers specifically tailored for thermocouple applications. The LTKA0x is a bipolar design with extremely low offset ($30\mu\text{V}$), low drift ($1.5\mu\text{V}/^\circ\text{C}$), very low bias current (1nA), and almost negligible warm-up drift (supply current is $400\mu\text{A}$).

For the most demanding applications, the LTC[®]1052 CMOS chopper-stabilized amplifier offers $5\mu\text{V}$ offset and $0.05\mu\text{V}/^\circ\text{C}$ drift. Input bias current is 30pA , and gain is typically 30 million. This amplifier should be used for R and S thermocouples, especially if no offset adjustments can be tolerated, or where a large ambient temperature swing is expected. Alternatively, the LTC1050, which has similar drift and slightly higher noise can be used. If board space is at a premium, the LTC1050 has the capacitors internally.

Regardless of amplifier type, for best possible performance dual-in-line (DIP) packages should be used to avoid thermocouple effects in the kovar leads of TO-5 metal can packages. This is particularly true if amplifier supply

current exceeds $500\mu\text{A}$. These leads can generate both DC and AC offset terms in the presence of thermal gradients in the package and/or external air motion.

In many situations, thermocouples are used in high noise environments, and some sort of input filter is required. To reject 60Hz pick-up with reasonable capacitor values, input resistors in the 10k to 100k range are needed. Under these conditions, bias current for the amplifier needs to be less than 1nA to avoid offset and drift effects.

To avoid gain error, high open-loop gain is necessary for single-stage thermocouple amplifiers with $10\text{mV}/^\circ\text{C}$ or higher outputs. A type K amplifier, for instance, with $100\text{mV}/^\circ\text{C}$ output, needs a closed-loop gain of 2,500. An ordinary op amp with a minimum loop of 50,000 would have an initial gain error of $(2,500)/(50,000) = 5\%$! Although closed-loop gain is commonly trimmed, temperature drift of open-loop gain will have a deleterious effect on output accuracy. Minimum suggested loop gain for type E, J, K and T thermocouples is 250,000. This gain is adequate for type R and S if output scaling is $10\text{mV}/^\circ\text{C}$ or less.

Additional Circuit Considerations

Other circuit considerations involve protection and common mode voltage and noise. Thermocouple lines are often exposed to static and accidental high voltages, necessitating circuit protection. Figure 11 shows two suggested approaches. These examples are designed to prevent excessive overloads from damaging circuitry. The added series resistance can serve as part of a filter. Effects of the added components on overall accuracy should be evaluated. Diode clamping to supply lines is effective, but leakage should be noted, particularly when large current limiting resistors are used. Similarly, IC bias currents combined with high value protection resistors can generate apparent measurement errors. Usually, a favorable compromise is possible, but sometimes the circuit configuration will be dictated by protection or noise rejection requirements.

Differential Thermocouple Amplifiers

Figure 12a shows a way to combine filtering and full differential sensing. This circuit features 120dB DC common mode rejection if all signals remain within the LTC1043 supply voltage range. The LTC1043, a switched-capacitor building block, transfers charge between the input

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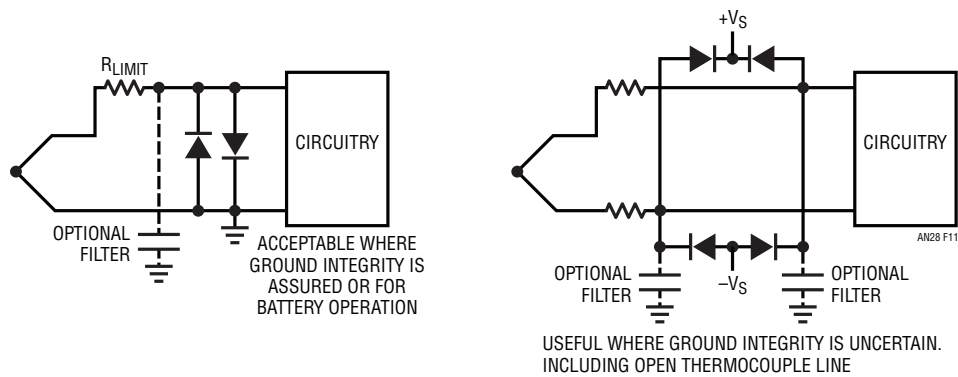


Figure 11. Input Protection Schemes

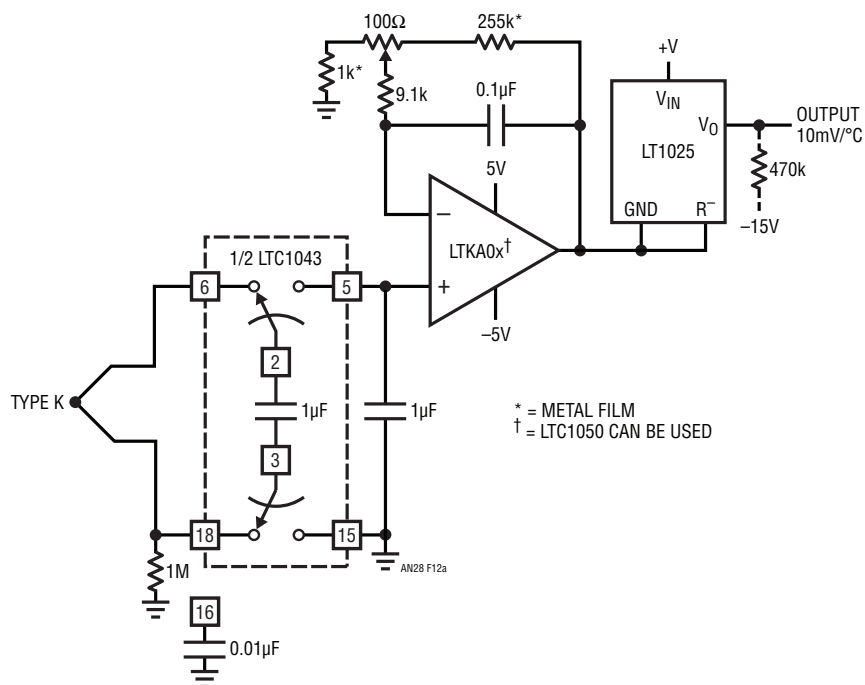


Figure 12a. Full Differential Input Thermocouple Amplifiers

“flying” capacitor and the output capacitor. The LTC1043’s commutating frequency, which is settable, controls rate of charge transfer, and hence overall bandwidth. The differential inputs reject noise and common mode voltages inside the LTC1043’s supply rails. Excursions outside these limits require protection networks, as previously discussed. As in Figure 9, an optional resistor pull-down permits negative readings. The 1M resistor provides a bias path for the LTC1043’s floating inputs. Figure 12b, for use with grounded thermocouples, subtracts sensor output from the LT1025.

Isolated Thermocouple Amplifiers

In many cases, protection networks and differential operation are inadequate. Some applications require continuous operation at high common mode voltages with severe noise problems. This is particularly true in industrial environments, where ground potential differences of 100V are common. Under these conditions the thermocouple and signal conditioning circuitry must be completely galvanically isolated from ground. This requires a fully isolated power source and an isolated

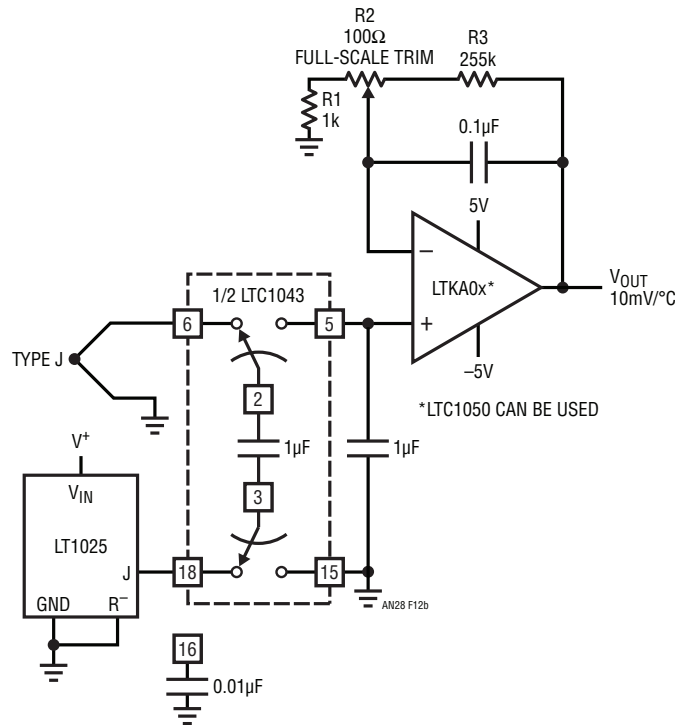


Figure 12b

signal transmission path to the ground referred output. Thermocouple work allows bandwidth to be traded for DC accuracy. With careful design, a single path can transfer floating power and isolated signals. The output may be either analog or digital, depending on requirements.

Figure 13 shows an isolated thermocouple signal conditioner which provides 0.25% accuracy at 175V common mode. A single transformer transmits isolated power and data. 74C14 inverter I₁ forms a clock (Trace A, Figure 14). I₂, I₃ and associated components deliver a stretched pulse to the 2.2k resistor (Trace B). The amplitude of this pulse is stabilized because A1's fixed output supplies 74C14 power. The resultant current through the 2.2k resistor drives L1's primary (Trace E). A pulse appears at L1's secondary (Trace F, Q2's emitter). A2 compares this amplitude with A5's signal conditioned thermocouple voltage. To close its loop, A2's output (Trace G) drives Q2's base to force L1's secondary (Pins 3 to 6) to clamp at A5's output value. Q2 operates in inverted mode, permitting clamping action even for very low A5 outputs. When L1's secondary (Trace F) clamps, its primary (Trace E) also clamps. After A2

settles, the clamp value is stable. This stable clamp value represents A5's thermocouple related information. Inverter I₄ generates a clock delayed pulse (Trace C) which is fed to A3, a sample-and-hold amplifier. A3 samples L1's primary winding clamp value. A4 provides gain scaling and the LT1004 and associated components adjust offset. When the clock pulse (Trace A) goes low, sampling ceases. When Trace B's stretched clock pulse goes low, the I₅-I₆ inverter chain output (Trace D) is forced low by the 470k-75pF differentiator's action. This turns on Q1, forcing substantial energy into L1's primary (Trace E). L1's secondary (Trace F) sees large magnetic flux. A2's output (Trace G) moves as it attempts to maintain its loop. The energy is far too great, however, and A2 rails. The excess energy is dumped into the Pin 1-Pin 4 winding, placing a large current pulse (Trace H) into the 22μF capacitor. This current pulse occurs with each clock pulse, and the capacitor charges to a DC voltage, furnishing the circuit's isolated supply. When the 470k-75pF differentiator times out, the I₅-I₆ output goes high, shutting off Q1. At the next clock pulse the entire cycle repeats.

Application Note 28

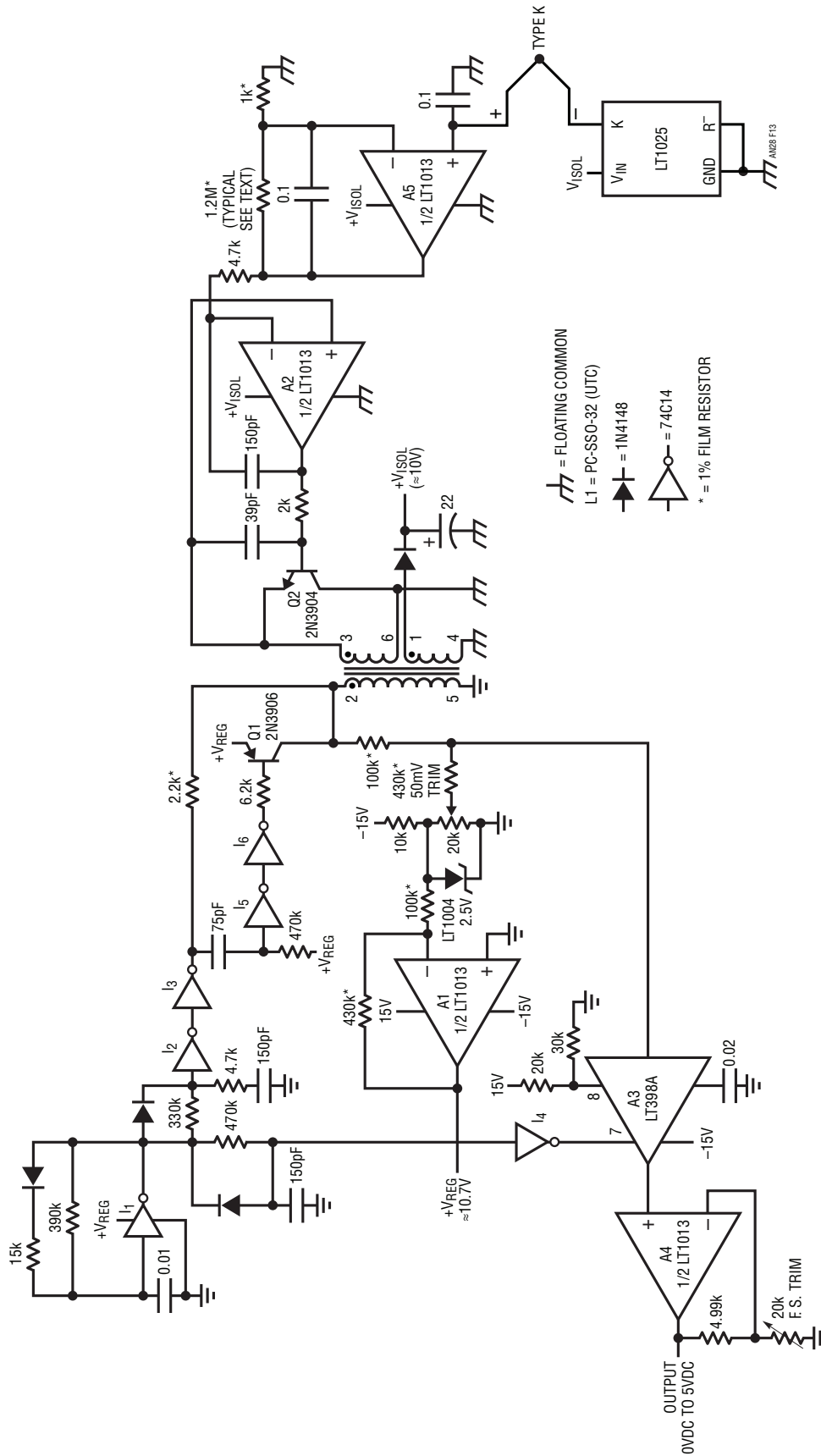


Figure 13. 0.25% Thermocouple Isolation Amplifier

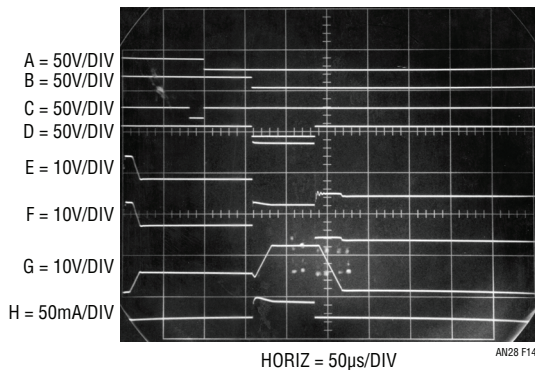


Figure 14. Waveforms for Figure 13's Thermocouple Isolation Amplifier

Proper operation of this circuit relies on several considerations. Achievable accuracy is primarily limited by transformer characteristics. Current during the clamp interval is kept extremely low relative to transformer core capacity. Additionally, the clamp period must also be short relative to core capacity. The clamping scheme relies on avoiding core saturation. This is why the power refresh pulse occurs immediately after data transfer, and not before. The transformer must completely reset before the next data transfer. A low clock frequency (350Hz) ensures adequate transformer reset time. This low clock frequency limits bandwidth, but the thermocouple data does not require any speed.

Gain slope is trimmed at A5, and will vary depending upon the desired maximum temperature and thermocouple type. The "50mV" trim should be adjusted with A5's output at 50mV. The circuit cannot read A5 outputs below 20mV (0.5% of scale) due to Q2's saturation limitations.

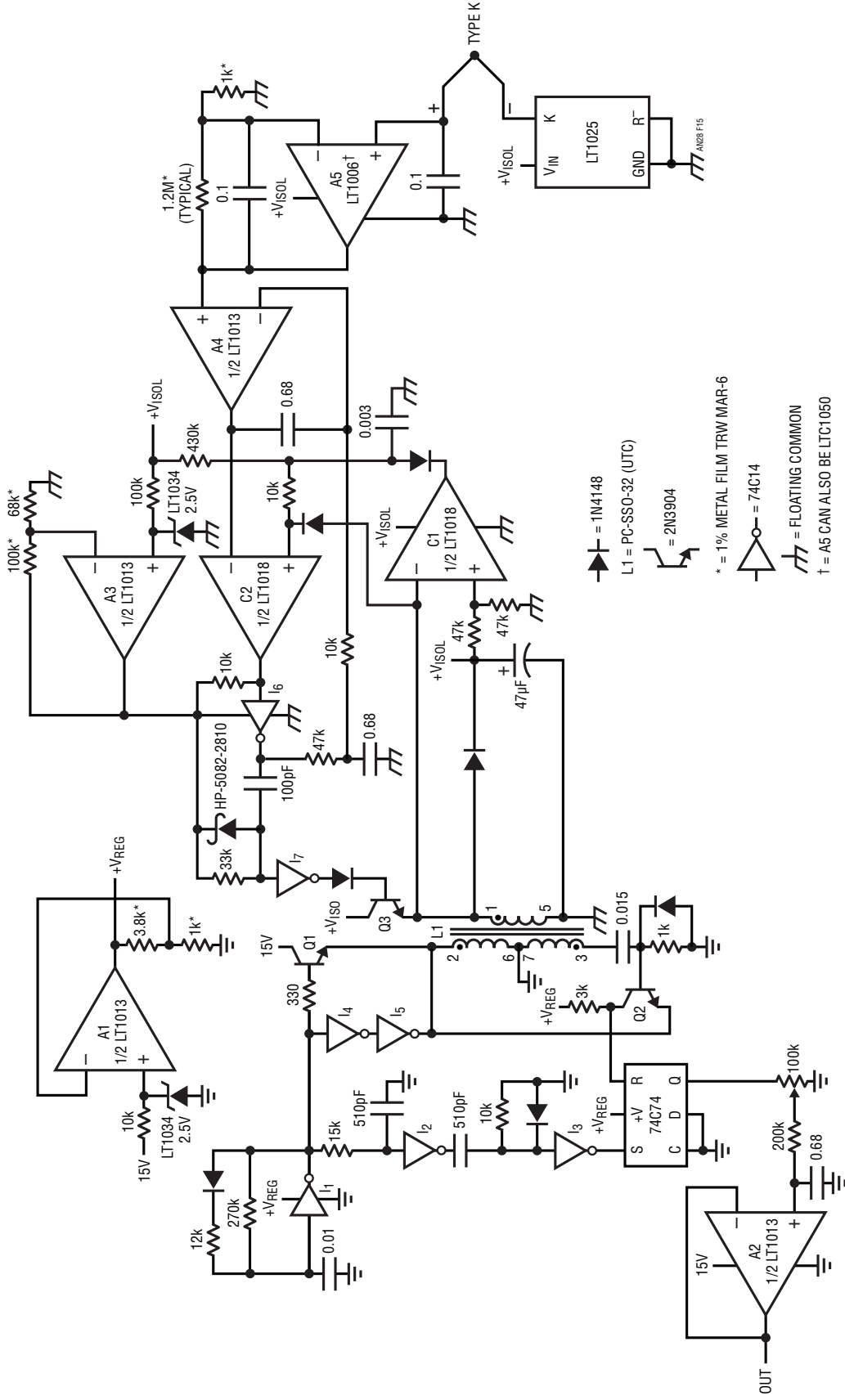
Drift is primarily due to the temperature dependence of L1's primary winding copper. This effect is swamped by the 2.2k series value with the 60ppm/°C residue partially compensated by I₃'s saturation resistance tempco. Overall tempco, including the LT1004, is about 100ppm/°C. Increased isolation voltages are possible with higher transformer breakdown ratings.

Figure 15's thermocouple isolation amplifier is somewhat more complex, but offers 0.01% accuracy and typical drift of 10ppm/°C. This level of performance is useful in servo systems or high resolution applications. As in Figure 13, a single transformer provides isolated data and power transfer. In this case the thermocouple information is width modulated across the transformer and then

demodulated back to DC. I₁ generates a clock pulse (Trace A, Figure 16). This pulse sets the 74C74 flip-flop (Trace B) after a small delay generated by I₂, I₃ and associated components. Simultaneously, I₄, I₅ and Q1 drive L1's primary (Trace C). This energy, received by L1's secondary (Trace H), is stored in the 47µF capacitor and serves as the circuit's isolated supply. L1's secondary pulse also clocks a closed-loop pulse width modulator composed of C1, C2, A3 and A4. A4's positive input receives A5's LT1025-based thermocouple signal. A4 servo-biases C2 to produce a pulse width each time C1 allows the 0.003µF capacitor (Trace E) to receive charge via the 430k resistor. C2's output width is inverted by I₆ (Trace F), integrated to DC by the 47k-0.68µF filter and fed back to A4's negative input. The 0.68µF capacitor compensates A4's feedback loop. A4 servo controls C2 to produce a pulse width that is a function of A5's thermocouple related output. I₆'s low loss MOS switching characteristics combined with A3's supply stabilization ensure precise control of pulse width by A4. Operating frequency, set by the I₁ oscillator on L1's primary side, is normally a stability concern, but ratios out because it is common to the demodulation scheme, as will be shown.

I₆'s output width's (Trace F) negative-going edge is differentiated and fed to I₇. I₇'s output (Trace G) drives Q3. Q3 puts a fast spike into L1's secondary (Trace H). "Sing around" behavior by C1 is gated out by the diode at C2's positive input. Q3's spike is received at L1's primary, Pins 7 and 3. Q2 serves as a clocked synchronous demodulator, pulling its collector low (Trace D) only when its base is high and its emitter is low (e.g., when L1 is transferring data, not power). Q2's collector spike resets the 74C74 flip-flop. The MOS flip-flop is driven from a stable source (A1) and it is also clocked at the same frequency as the pulse-width modulator. Because of this, the DC average of its Q output depends on A5's output. Variations with supply, temperature and I₁ oscillator frequency have no effect. A2 and its associated components extract the DC average by simple filtering. The 100k potentiometer permits desired gain scaling. Because this scheme depends on edge timing at the flip-flop, the delay in resetting the 0.003µF capacitor causes a small offset error. This term is eliminated by matching this delay in the 74C74 "set" line with the previously mentioned I₂-I₃ delay network. This delay is set so that the rising edge of the flip-flop output (Trace B) corresponds to I₆'s rising edge. No such

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- ▶ = 1N4148
- L1 = PC-SSO-32 (UTC)
- ↔ = 2N3904
- * = 1% METAL FILM TRW MAR-6
- ◊ = 74C14
- ⏏ = FLOATING COMMON
- † = A5 CAN ALSO BE LTC1050

Figure 15. 0.01% Thermocouple Isolation Amplifier

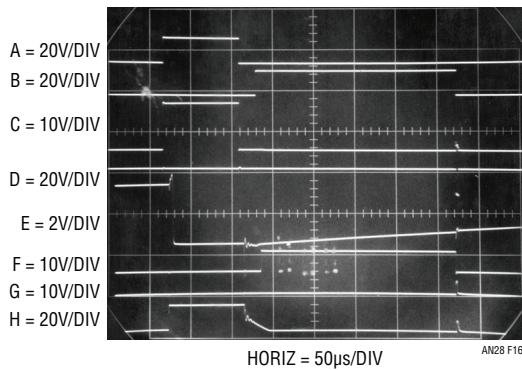


Figure 16. Pulse-Width-Modulation Based Thermocouple Isolation Amplifier Waveforms

compensation is required for falling edge data because circuit elements in this path (I_7 , Q3, L1 and Q2) are wideband. With drift matched LT1034s and the specified resistors, overall drift is typically 10ppm/°C with 0.01% linearity.

Digital Output Thermocouple Isolator

Figure 17 shows another isolated thermocouple signal conditioner. This circuit has 0.25% accuracy and features a digital (pulse width) output. I_1 produces a clock pulse (Trace A, Figure 18). I_2 - I_5 buffers this pulse and biases Q1 to drive L1. Concurrently, the 680pF-10k values provide a differentiated spike (Trace B), setting the 74C74 flip-flop (Trace C). L1's primary drive is received at the secondary.

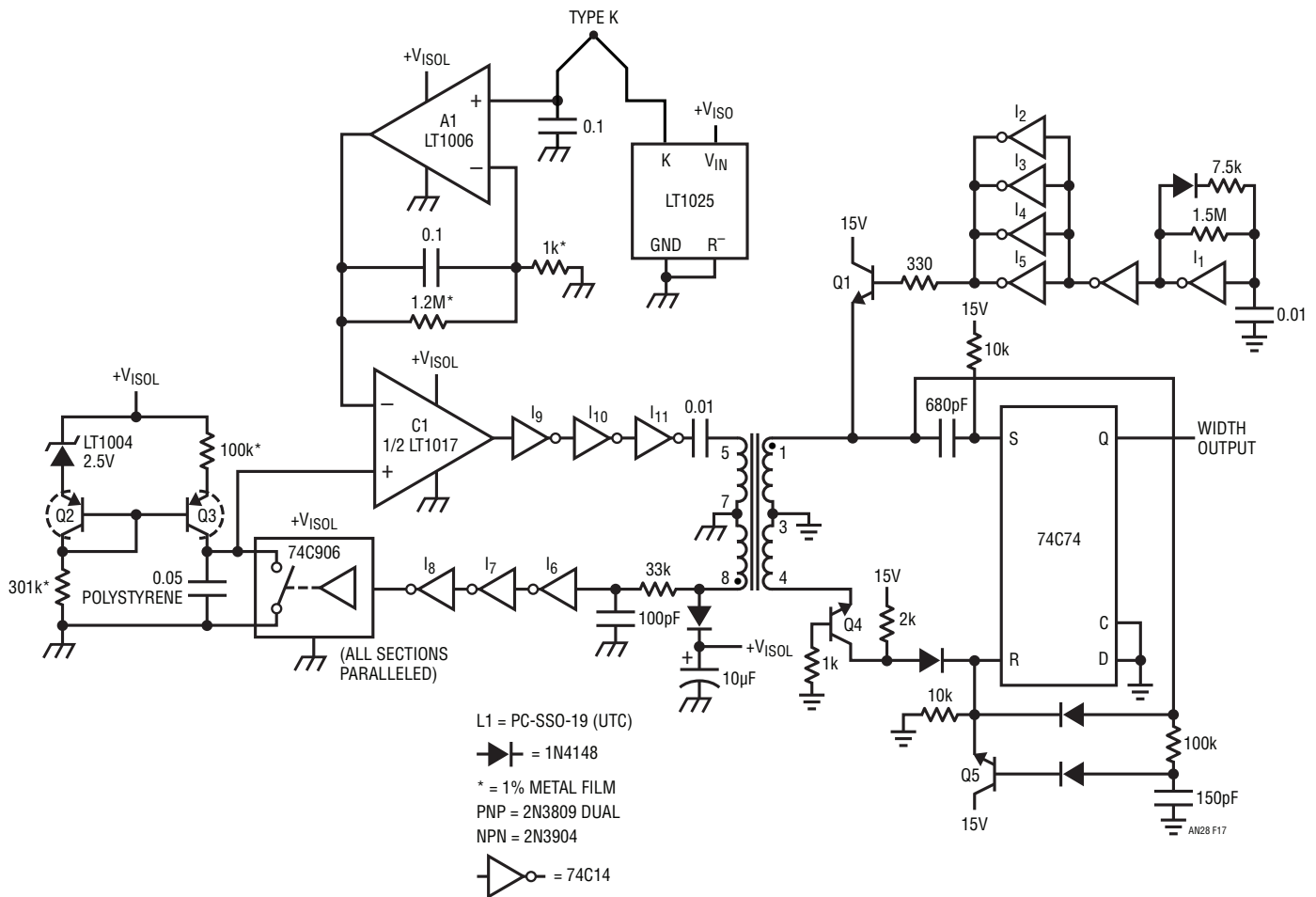


Figure 17. Digital Output Thermocouple Isolator

Application Note 28

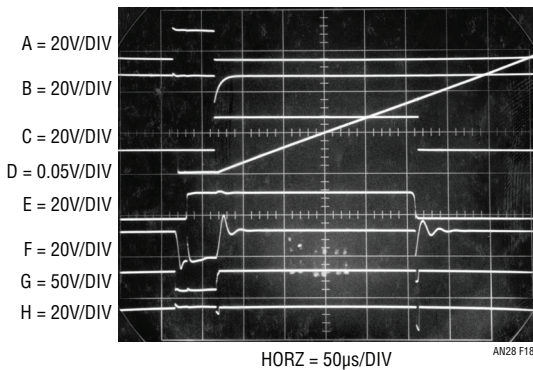


Figure 18. Waveforms for Digital-Output Thermocouple Isolator

The 10 μ F capacitor charges to DC, supplying isolated power. The pulse received at L1's secondary also resets the 0.05 μ F capacitor (Trace D) via the inverters (I₆, I₇, I₈) and the 74C906 open-drain buffer. When the received pulse ends, the 0.05 μ F capacitor charges from the Q2-Q3 current source. When the resultant ramp crosses C1's threshold (A1's thermocouple related output voltage) C1 switches high, tripping the I₉-I₁₁ inverter chain. I₁₁ (Trace E) drives L1's secondary via the 0.01 μ F capacitor (Trace F). The 33k-100pF filter prevents regenerative "sing around". The resultant negative-going spike at L1's primary biases Q4, causing its collector (Trace G) to go low. Q4 and Q5 form a clocked synchronous demodulator which can pull the 74C74 reset pin low only when the clock

is low. This condition occurs during data transfer, but not during power transfer. The demodulated output (Trace H) contains a single negative spike synchronous with C1's (e.g., I₁₁'s) output transition. This spike resets the flip-flop, providing the circuit output. The 74C74's width output thus varies with thermocouple temperature.

Linearization Techniques

It is often desirable to linearize a thermocouple-based signal. Thermocouples' significant nonlinear response requires design effort to get good accuracy. Four techniques are useful. They include offset addition, breakpoints, analog computation, and digital correction. Offset addition schemes rely on biasing the nonlinear "bow" with a constant term. This results in the output being high at low scale and low at high scale with decreased errors between these extremes (Figure 19). This compromise reduces overall error. Typically, this approach is limited to slightly nonlinear behavior over wide ranges or larger nonlinearity over narrow ranges.

Figure 20 shows a circuit utilizing offset linearization for a type S thermocouple. The LT1025 provides cold junction compensation and the LTC1052 chopper-stabilized amplifier is used for low drift. The type S thermocouple output slope varies greatly with temperature. At 25°C it

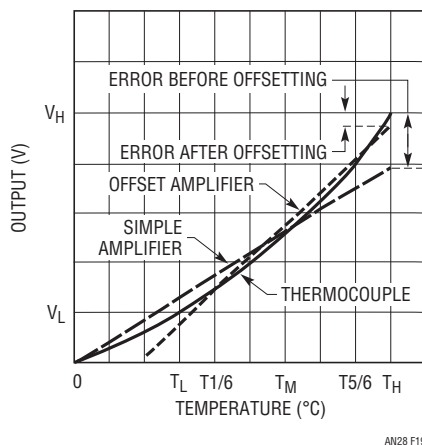


Figure 19. Offset Curve Fitting

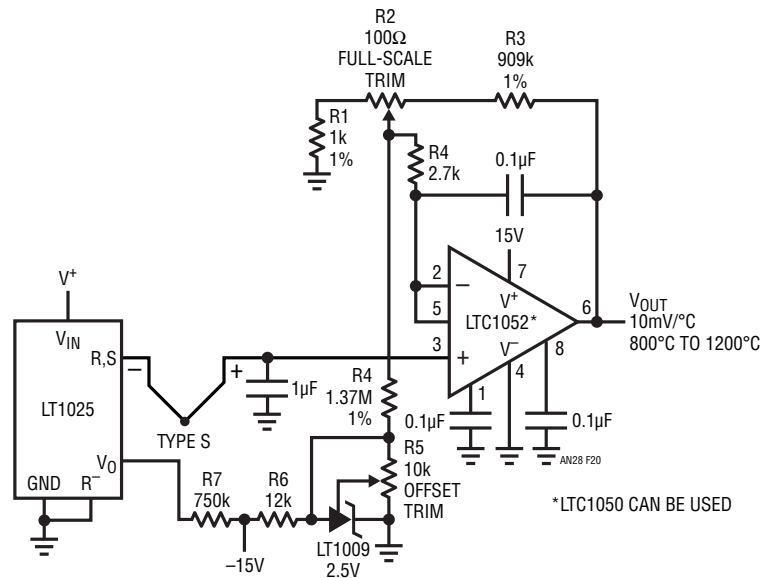


Figure 20. Offset-Based Linearization

is $6\mu\text{V}/^\circ\text{C}$, with an $11\mu\text{V}/^\circ\text{C}$ slope at 1000°C . This circuit gives 3°C accuracy over the indicated output range. The circuit, similar to Figure 10, is not particularly unusual except for the offset term derived from the LT1009 and applied through R4. To calibrate, trim R5 for $V_{\text{OUT}} = 1.669$ at $V_{\text{IN}} = 0.000\text{mV}$. Then, trim R2 for $V_{\text{OUT}} = 9.998\text{V}$ at $T = 1000^\circ\text{C}$ or for $V_{\text{IN}} (+ \text{input}) = 9.585\text{mV}$.

Figure 21, an adaption of a configuration shown by Sheingold (reference 3), uses breakpoints to change circuit gain as input varies. This method relies on scaling of the input and feedback resistors associated with A2-A6 and A7's reference output. Current summation at A8 is linear with the thermocouple's temperature. A3-A6 are the breakpoints, with the diodes providing switching when the respective summing point requires positive bias. As shown, typical accuracy of 1°C is possible over a 0°C to 650°C sensed range.

Figure 22, derived from Villanucci (reference 8), yields similar performance but uses continuous function analog computing to replace breakpoints, minimizing amplifiers and resistors. The AD538 combines with appropriate scaling to linearize response. The causality of this circuit is similar to Figure 22; the curve fit mechanism (breakpoint vs continuous function) is the primary difference.

Digital techniques for thermocouple linearization have become quite popular. Figure 23, developed by Guy M. Hoover and William C. Rempfer, uses a microprocessor fed from a digitized thermocouple output to achieve linearization. The great advantage of digital techniques is elimination of trimming. In this scheme a large number of breakpoints are implemented in software.

The 10-bit LTC1091A A/D gives 0.5°C resolution over a 0°C to 500°C range. The LTC1052 amplifies and filters the thermocouple signal, the LT1025A provides cold junction compensation and the LT1019A provides an accurate reference. The J type thermocouple characteristic is linearized digitally inside the processor. Linear interpolation between known temperature points spaced 30°C apart introduces less than 0.1°C error. The 1024 steps provided by the LTC1091 (24 more than the required 1000) ensure 0.5°C resolution even with the thermocouple curvature.

Offset error is dominated by the LT1025 cold junction compensator which introduces 0.5°C maximum. Gain

error is 0.75°C max because of the 0.1% gain resistors and, to a lesser extent, the output voltage tolerance of the LT1019A and the gain error of the LTC1091A. It may be reduced by trimming the LT1019A or gain resistors. The LTC1091A keeps linearity better than 0.15°C . The LTC1052's $5\mu\text{V}$ offset contributes negligible error (0.1°C or less). Combined errors are typically inside 0.5°C . These errors don't include the thermocouple itself. In practice, connection and wire errors of 0.5°C to 1°C are not uncommon. With care, these errors can be kept below 0.5°C .

The 20k-10k divider on CH1 of the LTC1091 provides low supply voltage detection (the LT1019A reference requires a minimum supply of 6.5V to maintain accuracy). Remote location is possible with data transferred from the MCU to the LTC1091 via the 3-wire serial port.

Figure 24 is a complete software listing* of the code required for the 68HC05 processor. Preparing the circuit involves loading the software and applying power. No trimming is required.

*Including of a software-based circuit was not without attendant conscience searching and pain on the author's part. Hopefully, the Analog Faithful will tolerate this transgression ...I'm sorry everybody, it just works too well!

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Application Note 28

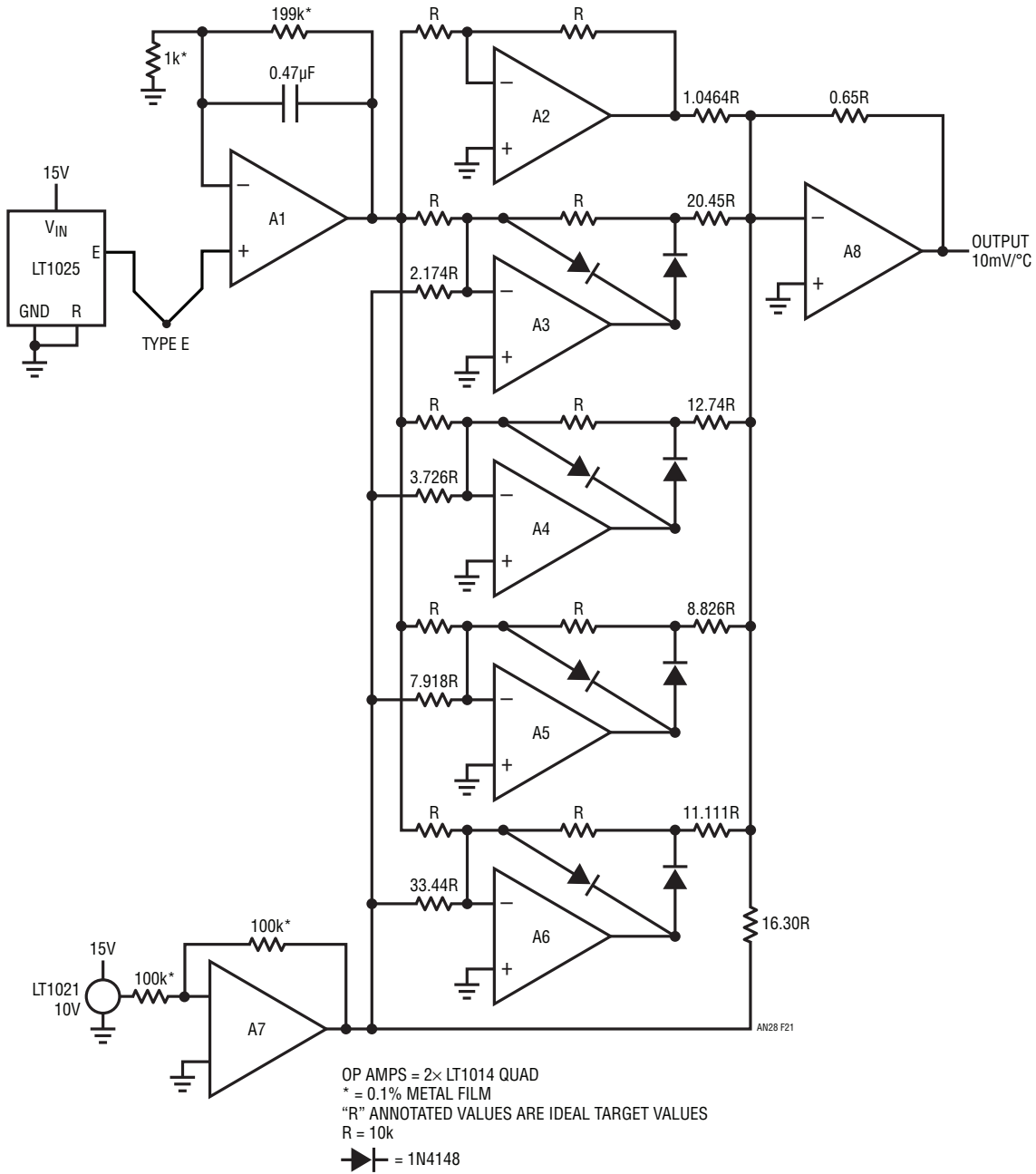


Figure 21. Breakpoint-Based Linearization (See Reference 3)

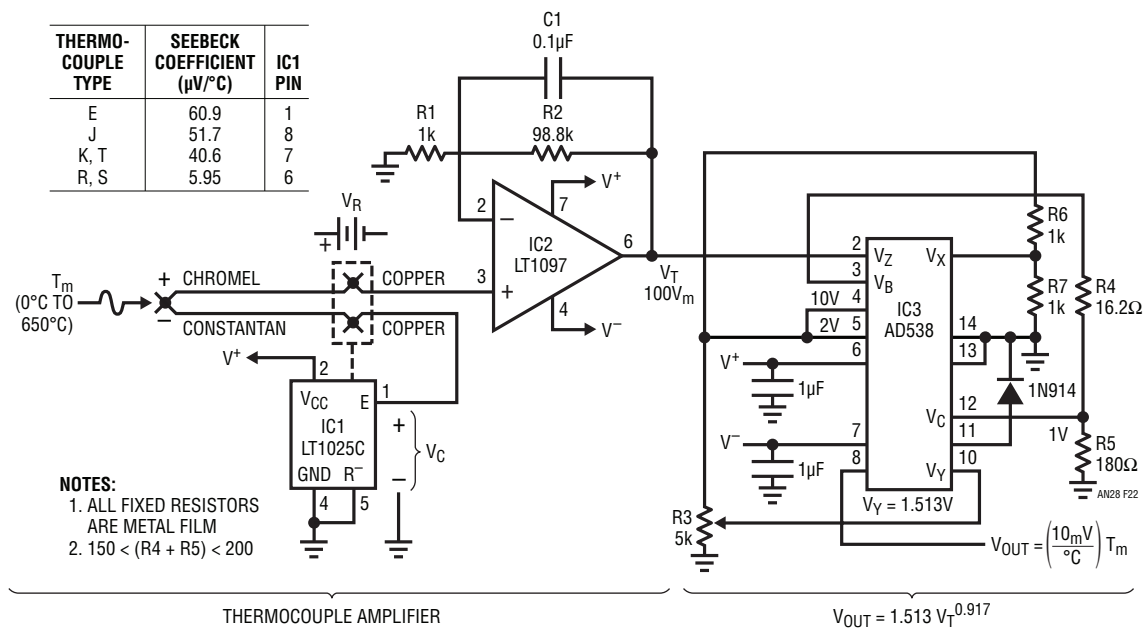


Figure 22. Continuous Function Linearization (See Reference 8)

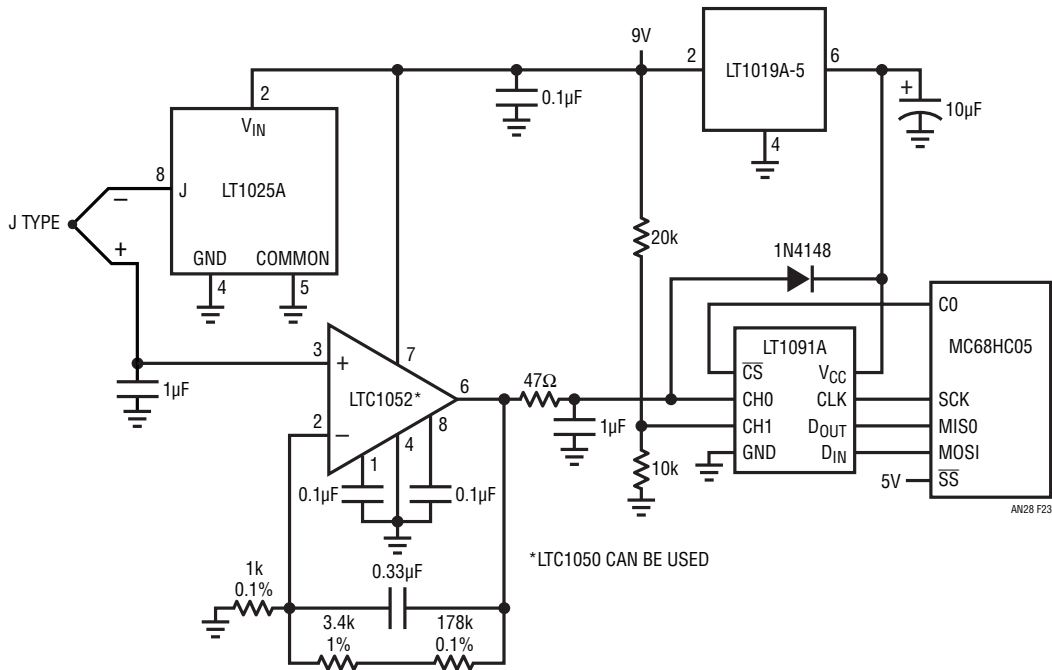


Figure 23. Processor-Based Linearization

Application Note 28

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*          TYPE J THERMOCOUPLE LINEARIZATION PROGRAM
*          WRITTEN BY GUY HOOVER LINEAR TECHNOLOGY CORPORATION
*          REV 1 10/4/87
*          N IS NUMBER OF SEGMENTS THAT THERMOCOUPLE RESPONSE IS DIVIDED INTO
*          TEMPERATURE (°C)=M•X+B
*          M IS SLOPE OF THERMOCOUPLE RESPONSE FOR A GIVEN SEGMENT
*          X IS A/D OUTPUT—SEGMENT END POINT
*          B IS SEGMENT START POINT IN DEGREES (°C • 2)

ORG      $1000
FDB      $00,$39,$74,$B0,$EE,$12B,$193,$262,$330,$397          TABLE FOR X
ORG      $1020
FDB      $85DD,$823A,$7FB4,$7DD4,$7CAF,$7BC3,$7B8A,$7C24,$7C1F,$7B3A  TABLE FOR M
ORG      $1040
FDB      $00,$3C,$78,$B4,$F0,$12C,$190,$258,$320,$384          TABLE FOR B
ORG      $10FF
FCB      $13                                                    N • 2
ORG      $0100
OPT      ]
STA      $0A          LOAD CONFIGURATION DATA INTO $0A
LDA      #$00          CONFIGURATION DATA FOR PORT A DDR
STA      $04          LOAD CONFIGURATION DATA INTO PORT A
LDA      #$FF          CONFIGURATION DATA FOR PORT B DDR
STA      $05          LOAD CONFIGURATION DATA INTO PORT B
LDA      #$F7          CONFIGURATION DATA FOR PORT C DDR
STA      $06          LOAD CONFIGURATION DATA INTO PORT C
JSR      HOUSEKP      INITIALIZE ASSORTED REGISTERS

MES92L   NPO
JSR      CHECK
LDA      #$6F          DIN WORD FOR LTC1091 CH0, W/RESPECT TO GND, MSB FIRST
STA      $50          STORE IN DIN BUFFER
JSR      READ91        READ LTC1091

LINEAR   LDX      $10FF      LOAD SEGMENT COUNTER INTO X
DOAGAIN  LDA      $1000,X    LOAD LSBs OF SEGMENT N
STA      $55          STORE LSBs IN $55
DECX     DECREMENT X
LDA      $1000,X    LOAD MSBs OF SEGMENT N
STA      $54          STORE MSBs IN $54
JSR      SUBTRCT
BPL      SEGMENT
JSR      ADDB
DECX     DECREMENT X

SEGMENT  JMP      DOAGAIN
LDA      $1020,X    LOAD MSBs OF SLOPE
STA      $54          STORE MSBs IN $54
INCX     INCREMENT X
LDA      $1020,X    LOAD LSBs OF SLOPE
STA      $55          STORE LSBs IN $55
JSR      TBMULT      RETURNS RESULT IN $61 AND $62
LDA      $1040,X    LOAD LSBs OF BASE TEMP
STA      $55          STORE LSBs IN $55
DECX     DECREMENT X
LDA      $1040,X    LOAD MSBs OF BASE TEMP
STA      $54
JSR      ADDB

CHECK    LDA      #$7F          DIN WORD FOR CH1
STA      $50          LOAD DIN WORD INTO $50
JSR      READ91        READ BATTERY VOLTAGE
LDA      #$02          LOAD MSB OF MIN BATT VOLTAGE
STA      $54          PUT IN MSB OF SUBTRACT BUFFER
LDA      #$CC          LOAD LSB OF MIN BATT VOLTAGE
STA      $55          PUT IN LSB OF SUBTRACT BUFFER
JSR      SUBTRCT      COMPARE BATT VOLTAGE WITH MINIMUM
BPL      NOPROB      IF BATT OK GOTO NOPROB

```

Figure 24. Code for Processor-Based Linearization

an28f

	JSR	ADDB	
	LDA	#\$01	
	STA	\$56	SET BATTERY LOW FLAG
	RTS		
NOPROB	JSR	ADDB	
	CLR	\$56	CLEAR LOW BATTERY FLAG
	RTS		
READ91	LDA	#\$50	CONFIGURATION DATA FOR SPCR
	STA	\$0A	LOAD CONFIGURATION DATA
	LDA	\$50	
	BCLR	2,\$02	BIT 0 PORT C GOES LOW (\overline{CS} GOES LOW)
	STA	\$0C	LOAD D_{IN} INTO SP1 DATA REG. START TRANSFER
BACK91	TST	\$0B	TEST STATUS OF SPIF
	BPL	BACK91	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	LDA	\$0C	LOAD CONTENTS OF SPI DATA REG. INTO ACC
	STA	\$0C	START NEXT CYCLE
	AND	#\$03	CLEAR 6 MSBs OF FIRST D_{OUT}
	STA	\$61	STORE MSBs IN \$61
BACK92	TST	\$0B	TEST STATUS OF SPIF
	BPL	BACK92	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	BSET	2,\$02	SET BIT 0 PORT C (\overline{CS} GOES HIGH)
	LDA	\$0C	LOAD CONTENTS OF SPI DATA INTO ACC
	STA	\$62	STORE LSBs IN \$62
	RTS		
SUBTRCT	LDA	\$62	LOAD LSBs
	SUB	\$55	SUBTRACT LSBs
	STA	\$62	STORE REMAINDER
	LDA	\$61	LOAD MSBs
	SBC	\$54	SUBTRACT W/CARRY MSBs
	STA	\$61	STORE REMAINDER
	RTS		
ADDB	LDA	\$62	LOAD LSBs
	ADD	\$55	ADD LSBs
	STA	\$62	STORE SUM
	LDA	\$61	LOAD MSBs
	ADC	\$54	ADD W/CARRY MSBs
	STA	\$61	STORE SUM
	RTS		
TBMULT	CLR	\$68	
	CLR	\$69	
	CLR	\$6A	
	CLR	\$6B	
	STX	\$58	STORE CONTENTS OF X IN \$58
	LSL	\$62	MULTIPLY LSBs BY 2
	ROL	\$61	MULTIPLY MSBs BY 2
	LDA	\$62	LOAD LSBs OF LTC1091 INTO ACC
	LDX	\$55	LOAD LSBs OF M INTO X
	MUL		MULTIPLY LSBs
	STA	\$6B	STORE LSBs IN \$6B
	STX	\$6A	STORE IN \$6A
	LDA	\$62	LOAD LSBs OF LTC1091 INTO ACC
	LDX	\$54	LOAD MSBs OF M INTO X
	MUL		
	ADD	\$6A	ADD NEXT BYTE
	STA	\$6A	STORE BYTE
	TXA		TRANSFER X TO ACC
	ADC	\$69	ADD NEXT BYTE
	STA	\$69	STORE BYTE
	LDA	\$61	LOAD MSBs OF LTC1091 INTO ACC
	LDX	\$55	LOAD LSBs OF M INTO X

Figure 24. Code for Processor-Based Linearization (Continued)

Application Note 28

	MUL		
	ADD	\$6A	ADD NEXT BYTE
	STA	\$6A	STORE BYTE
	TXA		TRANSFER X TO ACC
	ADC	\$69	ADD NEXT BYTE
	STA	\$69	STORE BYTE
	LDA	\$61	LOAD MSBs OF LTC1091 INTO ACC
	LDX	\$54	LOAD MSBs OF M INTO X
	MUL		
	ADD	\$69	ADD NEXT BYTE
	STA	\$69	STORE BYTE
	TXA		TRANSFER X TO ACC
	ADC	\$68	ADD NEXT BYTE
	STA	\$68	STORE BYTE
	LDA	\$6A	LOAD CONTENTS OF \$6A INTO ACC
	BPL	NNN	
	LDA	\$69	LOAD CONTENTS OF \$69 INTO ACC
	ADD	#\$01	ADD 1 TO ACC
	STA	\$69	STORE IN \$69
	LDA	\$68	LOAD CONTENTS OF \$68 INTO ACC
	ADC	#\$00	FLOW THROUGH CARRY
	STA	\$68	STORE IN \$68
NNN	LDA	\$68	LOAD CONTENTS OF \$68 INTO ACC
	STA	\$61	STORE MSBs IN \$61
	LDA	\$69	LOAD CONTENTS OF \$69 INTO ACC
	STA	\$62	STORE IN \$62
	LDX	\$58	RESTORE X REGISTER
	RTS		RETURN
HOUSEKP	BSET	0,\$02	SET B0 PORT C
	BSET	2,\$02	SET B2 PORT C
	RTS		

Figure 24. Code for Processor-Based Linearization (Continued)

APPENDIX A

Error Sources in Thermocouple Systems

Obtain good accuracy in thermocouple systems mandates care. The small thermocouple signal voltages require careful consideration to avoid error terms when signal processing. In general, thermocouple *system* accuracy better than 0.5°C is difficult to achieve. Major error sources include connection wires, cold junction uncertainties, amplifier error and sensor placement.

Connecting wires between the thermocouple and conditioning circuitry introduce undesired junctions. These junctions form unintended thermocouples. The number of junctions and their effects should be minimized, and kept isothermal. A variety of connecting wires and accessories are available from manufacturers and their literature should be consulted (reference 4).

Thermocouple voltages are generated whenever dissimilar materials are joined. This includes the leads of IC packages, which may be kovar in TO-5 cans, alloy 42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is “zero” if all are at exactly the same temperature, but temperature gradients exist within IC packages and across PC boards whenever power is dissipated. For this reason, extreme care must be used to ensure that no temperature gradients exist in the vicinity of the thermocouple terminations, the cold junction compensator (e.g., LT1025) or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be positioned isothermally, especially the LT1025 R⁻ and appropriate output pins, the amplifier input pins, and the gain setting resistor leads. An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire-bond/lead system of the IC

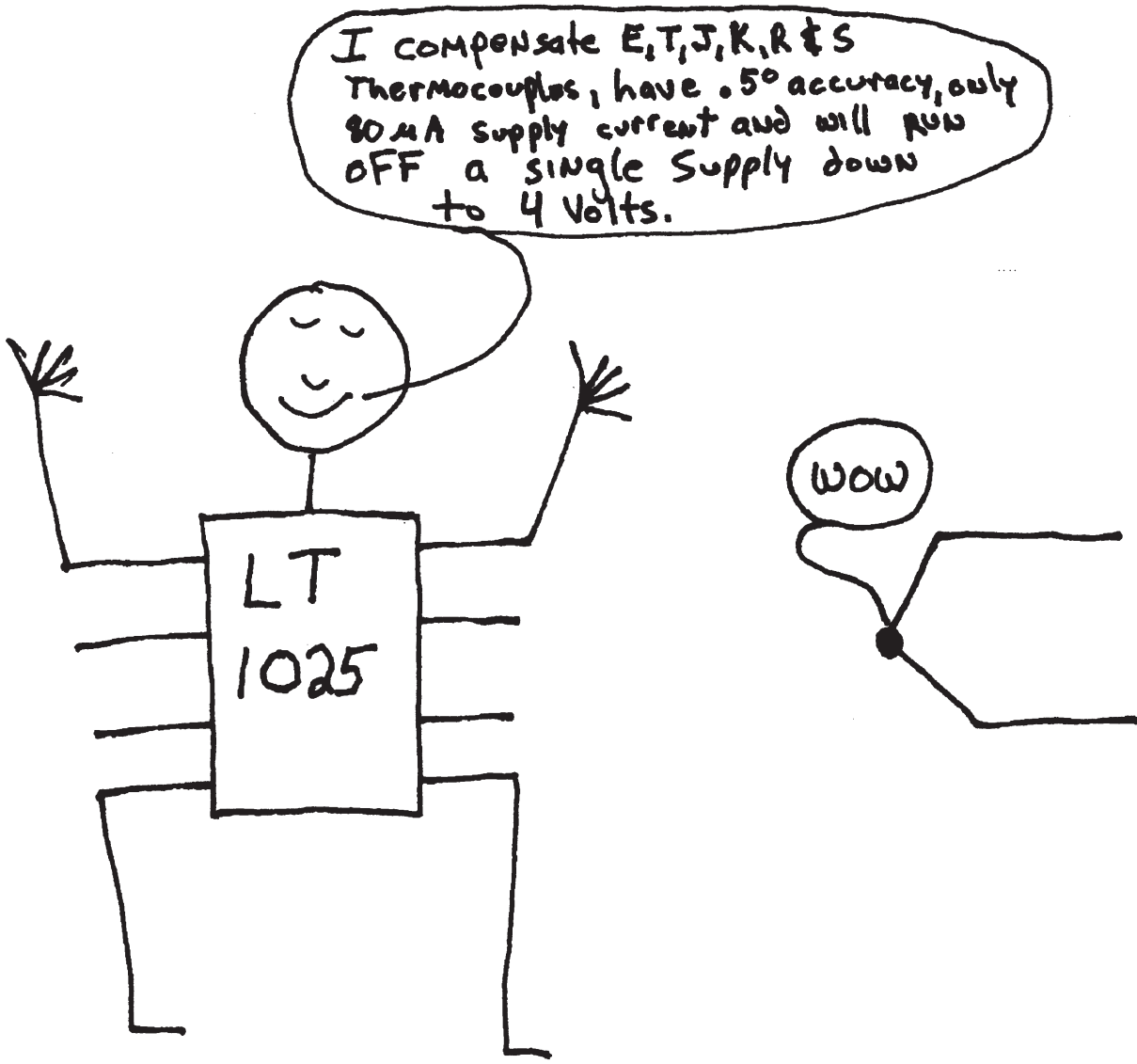
package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification of the amplifier and can occur in amplifiers with measured “zero” drift. Warm-up drift is directly proportional to amplifier power dissipation. It can be minimized by avoiding TO-5 cans, using low supply current amplifiers, and by using the lowest possible supply voltages. Finally, it can be accommodated by calibrating and specifying the system after a five minute warm-up period.

A significant error source is the cold junction. The error takes two forms. The subtractive voltage produced by the cold junction must be correct. In a true cold junction (e.g., ice point reference) this voltage will vary with inability to maintain the desired temperature, introducing error. In a cold junction compensator like the LT1025, error occurs with inability to sense and track ambient temperature. Minimizing sensing error is the manufacturer’s responsibility (we do our best!), but tracking requires user care. Every effort should be made to keep the LT1025 isothermal with the cold junction. Thermal shrouds, high thermal capacity blocks and other methods are commonly employed to ensure that the cold junction and the compensation are at the same temperature.

Amplifier offset uncertainties and, to a lesser degree, bias currents and open-loop gain should be considered. Amplifier selection criteria is discussed in the text under “Amplifier Selection.”

A final source of error is thermocouple placement. Remember that the thermocouple measures its own temperature. In flowing or fluid systems, remarkably large errors can be generated due to effects of laminar flow or eddy currents around the thermocouple. Even a “simple” surface measurement can be wildly inaccurate due to thermal conductivity problems. Silicone thermal grease can reduce this, but attention to sensor mounting is usually required. As much of the sensor surface as possible should be mated to the measured surface. Ideally, the sensor should be tightly mounted in a drilled recess in the surface. Keep in mind that the thermocouple leads act as heat pipes, providing a direct thermal path to the sensor. With high thermal capacity surfaces this may not be a problem, but other situations may require some thought. Often, thermally mating the lead wire to the surface or coiling the wire in the environment of interest will minimize heat piping effects.

As a general rule, skepticism is warranted, even in the most “obviously simple” situations. Experiment with several sensor positions and mounting options. If measured results agree, you’re probably on the right track. If not, rethink and try again.



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88

Some Thoughts on DC-DC Converters

Jim Williams
Brian Huffman

INTRODUCTION

Many systems require that the primary source of DC power be converted to other voltages. Battery driven circuitry is an obvious candidate. The 6V or 12V cell in a laptop computer must be converted to different potentials needed for memory, disc drives, display and operating logic. In theory, AC line powered systems should not need DC-DC converters because the implied power transformer can be equipped with multiple secondaries. In practice, economics, noise requirements, supply bus distribution problems and other constraints often make DC-DC conversion preferable. A common example is logic dominated, 5V powered systems utilizing $\pm 15V$ driven analog components.

The range of applications for DC-DC converters is large, with many variations. Interest in converters is commensurately quite high. Increased use of single supply powered systems, stiffening performance requirements and battery operation have increased converter usage.

Historically, efficiency and size have received heavy emphasis. In fact, these parameters can be significant, but often are of secondary importance. A possible reason behind the continued and overwhelming attention to size and efficiency in converters proves surprising. Simply put, these parameters are (within limits) *relatively easy to achieve!* Size and efficiency advantages have their place, but other system-oriented problems also need treatment. Low quiescent current, wide ranges of allowable inputs, substantial reductions in wideband output noise and cost effectiveness are important issues. One very important

converter class, the 5V to $\pm 15V$ type, stresses size and efficiency with little emphasis towards parameters such as output noise. This is particularly significant because wideband output noise is a frequently encountered problem with this type of converter. In the best case, the output noise mandates careful board layout and grounding schemes. In the worst case, the noise precludes analog circuitry from achieving desired performance levels (for further discussion see Appendix A, "The 5V to $\pm 15V$ Converter — A Special Case"). The 5V to $\pm 15V$ DC-DC conversion requirement is ubiquitous, and presents a good starting point for a study of DC-DC converters.

5V TO $\pm 15V$ CONVERTER CIRCUITS

Low Noise 5V to $\pm 15V$ Converter

Figure 1's design supplies a $\pm 15V$ output from a 5V input. Wideband output noise measures 200 microvolts peak-to-peak, a 100x reduction over typical designs. Efficiency at 250mA output is 60%, about 5-10% lower than conventional types. The circuit achieves its low noise performance by minimizing high speed harmonic content in the power switching stage. This forces the efficiency trade-off noted, but the penalty is small compared to the benefit.

The 74C14 based 30kHz oscillator is divided into a 15kHz two phase clock by the 74C74 flip flop. The 74C02 gates and 10K-0.001 μ F delays condition this two phase clock

Application Note 29

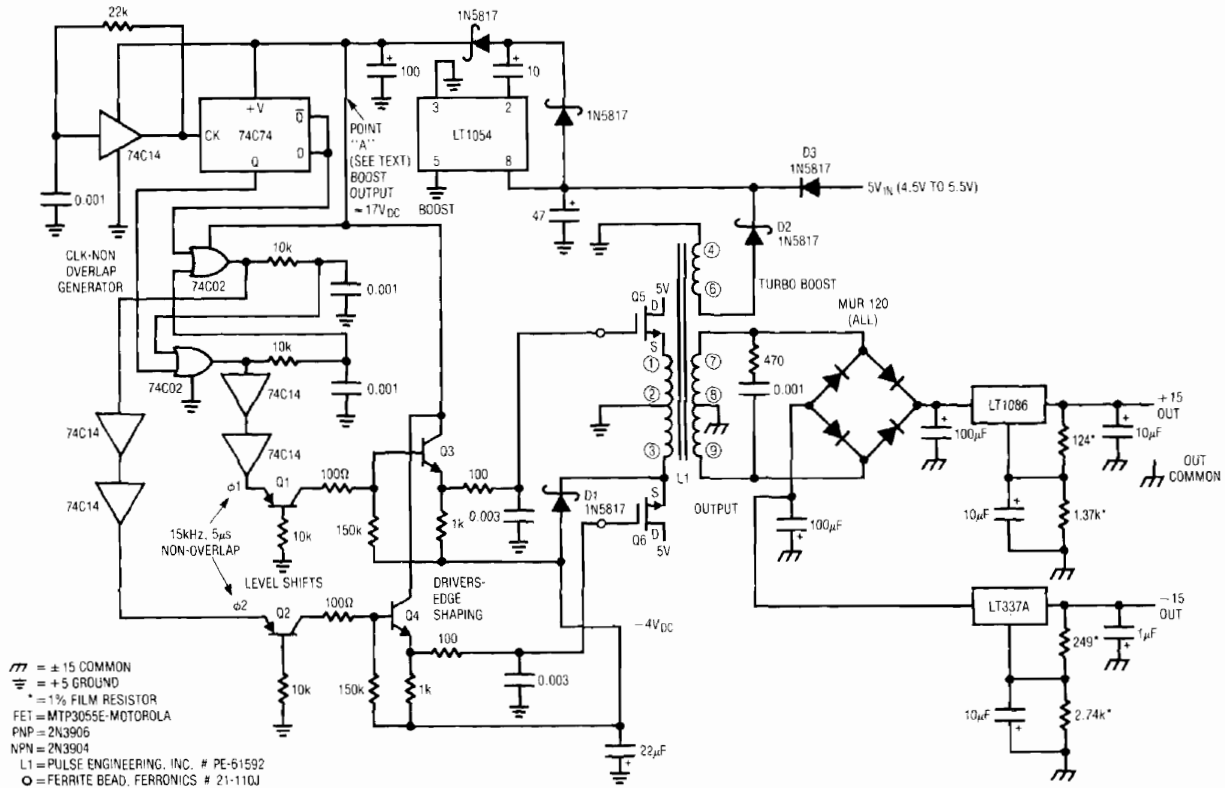


Figure 1. Low Noise 5V to ±15V Converter

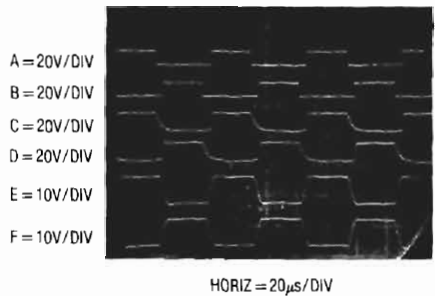


Figure 2. 5V to ±15V Low Noise Converter Waveforms

into non-overlapping, two phase drive at the emitters of Q1 and Q2 (Figure 2, traces A and B, respectively). These transistors provide level shifting to drive emitter followers Q3-Q4. The Q3-Q4 emitters see 100Ω-0.003μF filters, slowing drive to output MOSFET's Q5-Q6. The filter's effects appear at the gates of Q5 and Q6 (traces C and D, respectively). Q5 and Q6 are source followers, instead of the conventional common source connection. This limits transformer rise time to the gate terminals filtered slew rate, resulting in well controlled waveforms at the sources

of Q5 and Q6 (traces E and F, respectively). L1 sees complimentary, slew limited drive, eliminating the high speed harmonics normally associated with this type converter. L1's output is rectified, filtered and regulated to obtain the final output. The 470Ω-0.001μF damper in L1's output maintains loading during switching, aiding low noise performance. The ferrite beads in the gate leads eliminate parasitic RF oscillations associated with follower configurations.

The source follower configuration eases controlling L1's edge risetimes, but complicates gate biasing. Special provisions are required to get the MOSFET's fully turned on and off. Source follower connected Q5 and Q6 require voltage overdrive at the gates to saturate. The 5V primary supply cannot provide the specified 10V gate — channel bias required for saturation. Similarly, the gates must be pulled well below ground to turn the MOSFETs off. This is so because L1's behavior pulls the sources negative when the devices turn off. Turn-off bias is bootstrapped from the negative side of Q6's source waveform. D1 and the 22μF

capacitor produce a -4V potential for Q3 and Q4 to pull down to. Turn-on bias is generated by a two stage boost loop. The 5V supply is fed via D3 to the LT1054 switched capacitor voltage converter (switched capacitor voltage converters are discussed in Appendix B, "Switched Capacitor Voltage Converters — How They Work"). The LT1054 configuration, set up as a voltage doubler, initially provides about 9V boost to point "A" at turn-on. When the converter starts running L1 produces output ("Turbo Boost" on schematic) at windings 4–6 which is rectified by D2, raising the LT1054's input voltage. This further raises point "A" to the 17V potential noted on the schematic.

These internally generated voltages allow Q5 and Q6 to receive proper drive, minimizing losses despite their source follower connection. Figure 3, an AC coupled trace of the 15V converter output, shows $200\mu\text{Vp-p}$ noise at full power (250mA output). The -15V output shows nearly identical characteristics. Switching artifacts are comparable in amplitude to the linear regulators noise. Further reduction in switching based noise is possible by slowing Q5 and Q6 risetimes. This, however, necessitates reducing clock rate and increasing non-overlap time to maintain available output power and efficiency. The arrangement shown represents a favorable compromise between output noise, available output power, and efficiency.

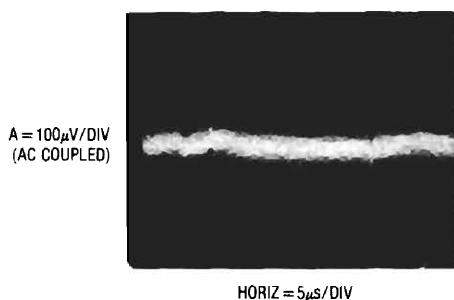


Figure 3. Output Noise of the Low Noise 5V to $\pm 15\text{V}$ Converter

Ultra-Low Noise 5V to $\pm 15\text{V}$ Converter

Residual switching components and regulator noise set Figure 1's performance limits. Analog circuitry operating at the very highest levels of resolution and sensitivity may require the lowest possible converter noise. Figure 4's converter uses sine wave transformer drive to reduce harmonics to negligible levels. The sine wave transformer drive combines with special output regulators to produce

less than $30\mu\text{V}$ of output noise. This is almost $7\times$ lower than the previous circuit and approaches a $1000\times$ improvement over conventional designs. The trade off is efficiency and complexity.

A1 is set up as a 16kHz Wien bridge oscillator. The single power supply requires biasing to prevent A1's output from saturating at the ground rail. This bias is established by returning the undriven end of the Wien network to a DC potential derived from the LT1009 reference. A1's output is a pure sine wave (Figure 5, trace A) biased off ground. A1's gain must be controlled to maintain sine wave output. A2 does this by comparing A1's rectified and filtered positive output peaks with an LT1009 derived DC reference. A2's output, biasing Q1, servo control A1's gain. The $0.22\mu\text{F}$ capacitor frequency compensates the loop, and the thermally mated diodes minimize errors due to rectifier temperature drift. These provisions fix A1's AC and DC output terms against supply and temperature changes.

A1's output is AC coupled to A3. The $2\text{k} - 820\Omega$ divider re-biases the sine wave, centering it inside A3's input common mode range even with supply shifts. A3 drives a power stage, Q2–Q5. The stages common emitter outputs and biasing permit 1V_{RMS} (3Vp-p) transformer drive, even at $V_{\text{supply}} = 4.5\text{V}$. At full converter output loading the stage delivers 3 ampere peaks but the waveform is clean (trace B), with low distortion (trace C). The $330\mu\text{F}$ coupling capacitor strips DC and L3 sees pure AC. Feedback to A3 is taken at the Q4–Q5 collectors. The $0.1\mu\text{F}$ unit at this point suppresses local oscillations. L3's secondary RC network adds additional high frequency damping.

Without control of quiescent current the power stage will encounter thermal runaway and destroy itself. A4 measures DC output current across Q5's emitter resistor and servo controls Q6 to fix quiescent current. A divided portion of the LT1009 reference sets the servo point at A4's negative input and the $0.33\mu\text{F}$ feedback capacitor stabilizes the loop.

L3's rectified and filtered outputs are applied to regulators designed for low noise. A5 and A7 amplify the LT1021's filtered 10V output up to 15V. A6 and A8 provide the -15V output. The LT1021 and amplifiers give better noise performance than three terminal regulators. The zener-resistor network clips overvoltages due to start-up transients.

Application Note 29

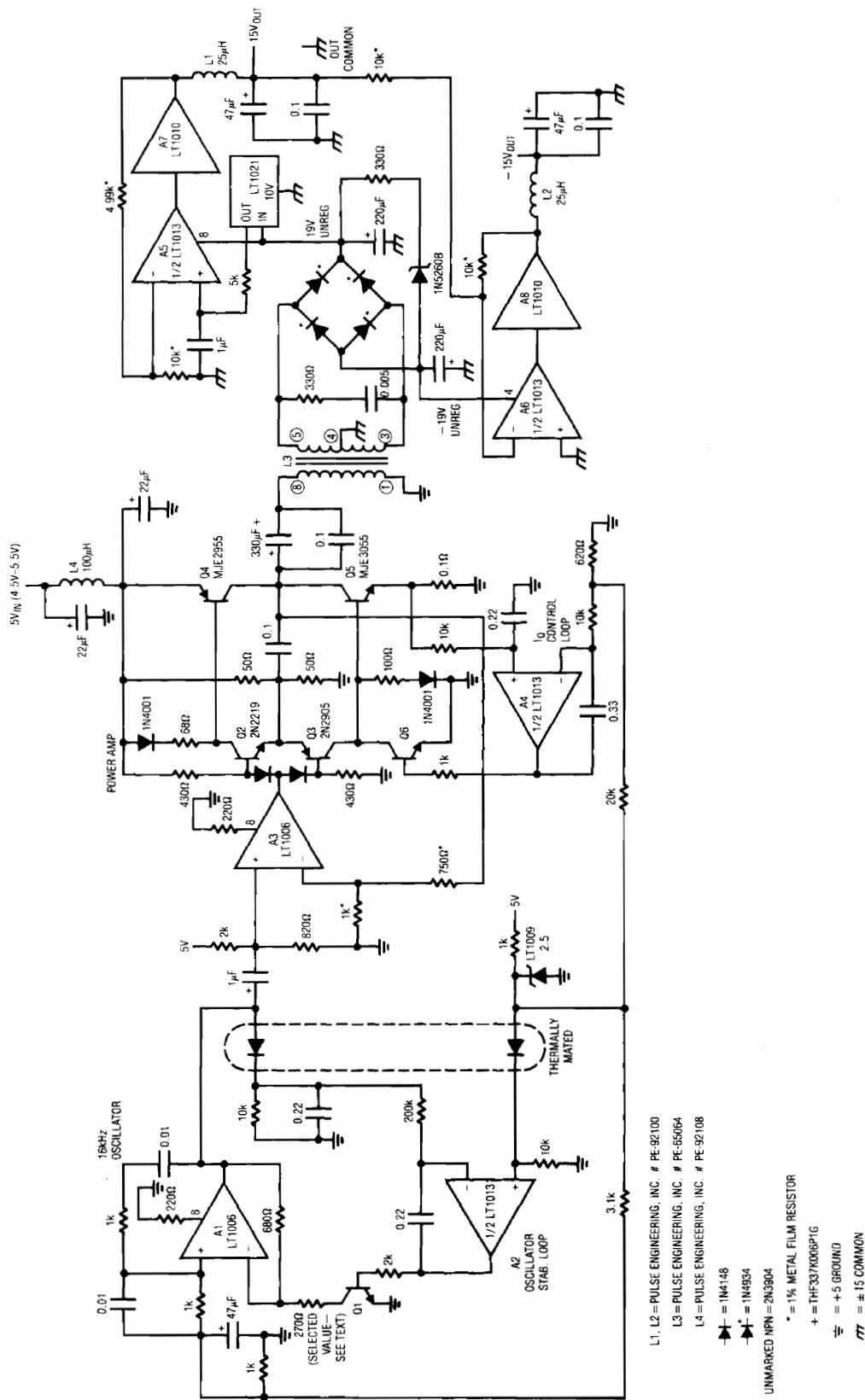


Figure 4. Ultra Low Noise Sine Wave Drive 5V to ±15V Converter

- L1, L2 = PULSE ENGINEERING, INC. # PE-92100
- L3 = PULSE ENGINEERING, INC. # PE-65064
- L4 = PULSE ENGINEERING, INC. # PE-92108
- ▷— = 1N4148
- ▷— = 1N4934
- UNMARKED NPN = 2N3904
- * = 1% METAL FILM RESISTOR
- + = THF337K008PTG
- ⊕ = +5 GROUND
- ⊖ = ±15 COMMON

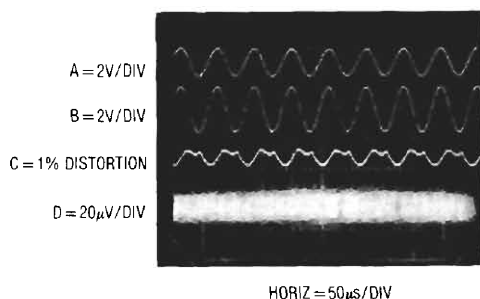


Figure 5. Waveforms for the Sine Wave Driven Converter.
Note that Output Noise (Trace D) is Only $30\mu\text{Vp-p}$.

L1 and L2 combine with their respective output capacitors to aid low noise characteristics. These inductors are outside the feedback loop, but their low copper resistance does not significantly degrade regulation. Trace D, the 15V output at full load, shows less than $30\mu\text{V}$ (2ppm) of noise. The most significant trade-off in this design is efficiency. The sine wave transformer drive forces substantial power loss. At full output (75mA), efficiency is only 30%.

Before use, the circuit should be trimmed for lowest distortion (typically 1%) in the sine wave delivered to L3. This trim is made by selecting the indicated value at A1's negative input. The 270Ω value shown is nominal, with a typical variance of $\pm 25\%$. The sine wave's 16kHz frequency is a compromise between the op amps available gain-bandwidth, magnetics size, audible noise, and minimization of wideband harmonics.

Single Inductor 5V to $\pm 15\text{V}$ Converter

Simplicity and economy are another dimension in 5V to $\pm 15\text{V}$ conversion. The transformer in these converters is usually the most expensive component. Figure 6's unusual drive scheme allows a single, two terminal inductor to replace the usual transformer at significant cost savings. Trade-offs include loss of galvanic isolation between input and output and lower power output. Additionally, the regulation technique employed causes about 50mV of clock related output ripple.

The circuit functions by periodically and alternately allowing each end of the inductor to flyback. The resultant positive and negative peaks are rectified and filtered. Regulation is obtained by controlling the number of flyback events during the respective output's flyback interval.

The leftmost logic inverter produces a 20kHz clock (trace A, Figure 7) which feeds a logic network composed of additional inverters, diodes and the 74C90 decade counter. The counter output (trace B) combines with the logic network to present alternately phased clock bursts (traces C and D) to the base resistors of Q1 and Q2. When $\phi 1$ (trace B) is unclocked it resides in its high state, biasing Q2 and Q4 on. Q4's collector effectively grounds the "bottom" of L1 (trace H). During this interval $\phi 2$ (trace A) puts clock bursts into Q1's base resistor. If the -15V output is too low servo comparator C1A's output (trace E) is high, and Q1's base can receive pulsed bias. If the converse is true the comparator will be low, and the bias gated away via Q1's base diode. When Q1 is able to bias, Q3 switches, resulting in negative going flyback events at the "top" of L1 (trace G). These events are rectified and filtered to produce the -15V output. C1A regulates by controlling the number of clock pulses that switch the Q1-Q3 pair. The LT1004 serves as a reference. Trace J, the AC coupled -15V output, shows the effect of C1A's regulating action. The output stays within a small error window set by C1A's switched control loop. As input voltage and loading conditions change C1A adjusts the number of clock pulses allowed to bias Q1-Q3, maintaining loop control.

When the $\phi 1$ and $\phi 2$ signals reverse state the operating sequence reverses. Q3's collector (trace G) is pulled high with Q2-Q4 switching controlled by C1B's servo action. Operating waveforms are similar to the previous case. Trace F is C1B's output, trace H is Q4's collector (L1's "bottom") and trace I is the AC coupled 15V output. Although the two regulating loops share the same inductor they operate independently, and asymmetrical output loading is not deleterious. The inductor sees irregularly spaced shots of current (trace K), but is unaffected by its multiplexed operation. Clamp diodes prevent reverse biasing of Q3 and Q4 during transient conditions. The circuit provides $\pm 25\text{mA}$ of regulated power at 60% efficiency.

Low Quiescent Current 5V to $\pm 15\text{V}$ Converter

A final area in 5V to $\pm 15\text{V}$ converter design is reduction of quiescent current. Typical units pull 100-150mA of quiescent current, unacceptable in many low power systems.

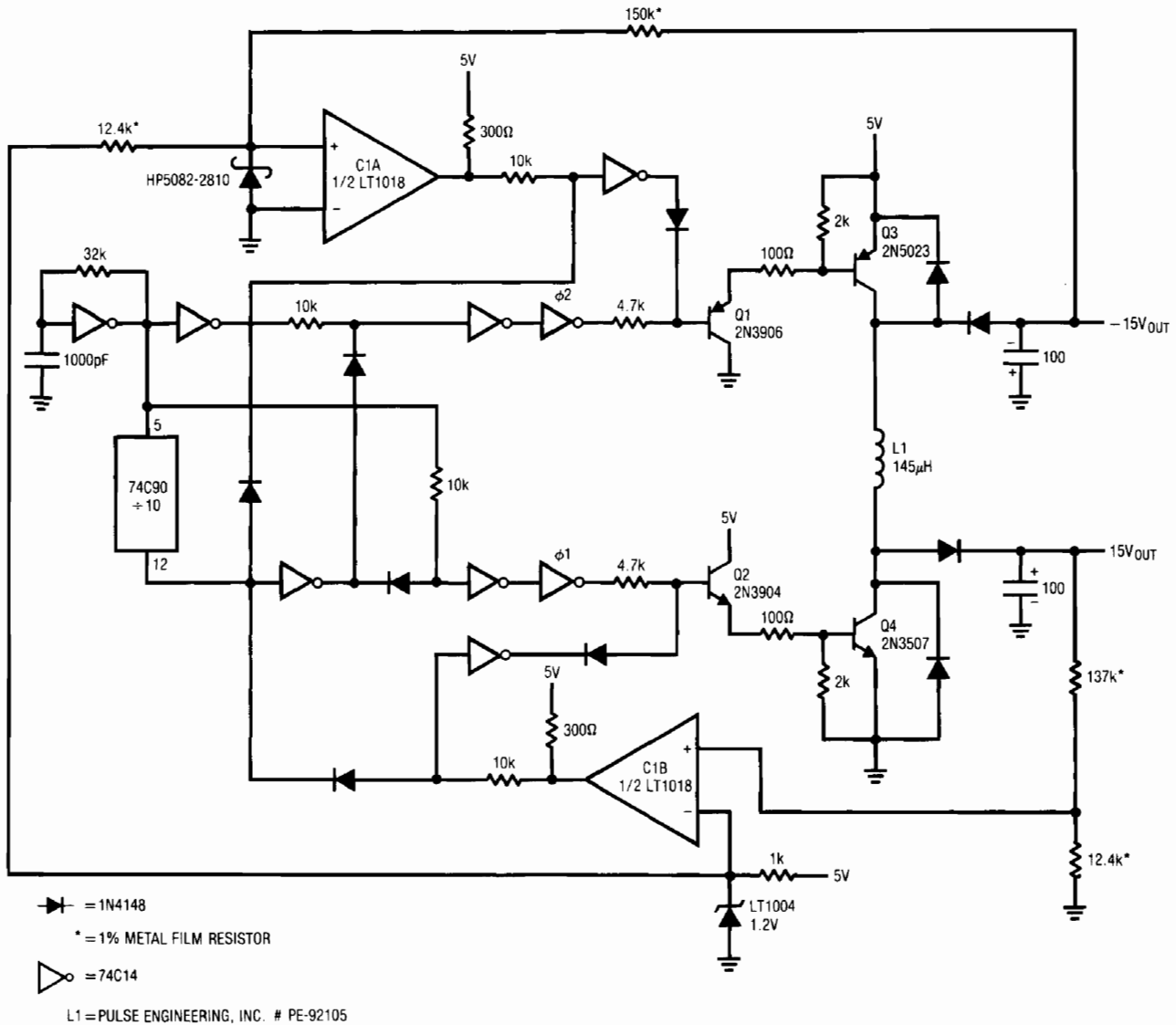


Figure 6. Single Inductor 5V to ±15V Regulated Converter

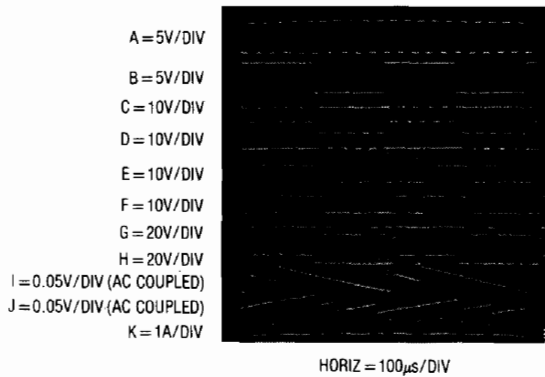


Figure 7. Waveforms for the Single Inductor, Dual-Output, Regulated Converter

Figure 8's design supplies $\pm 15V$ outputs at 100mA while consuming only 10mA quiescent current. The LT1070 switching regulator (for a complete description of this device, see Appendix C, "Physiology of the LT1070") drives L1 in flyback mode. A damper network clamps excessive flyback voltages. Flyback events at L1's secondary are half-wave rectified and filtered, producing positive and negative outputs across the 47µF capacitors. The positive 16V output is regulated by a simple loop. Comparator C1A balances a sample of the positive output with a 2.5V reference obtained from the LT1020. When the 16V output (trace A, Figure 9) is too low, C1A switches (trace B) high, turning off the 4N46 opto-isolator. Q1 goes off, and the

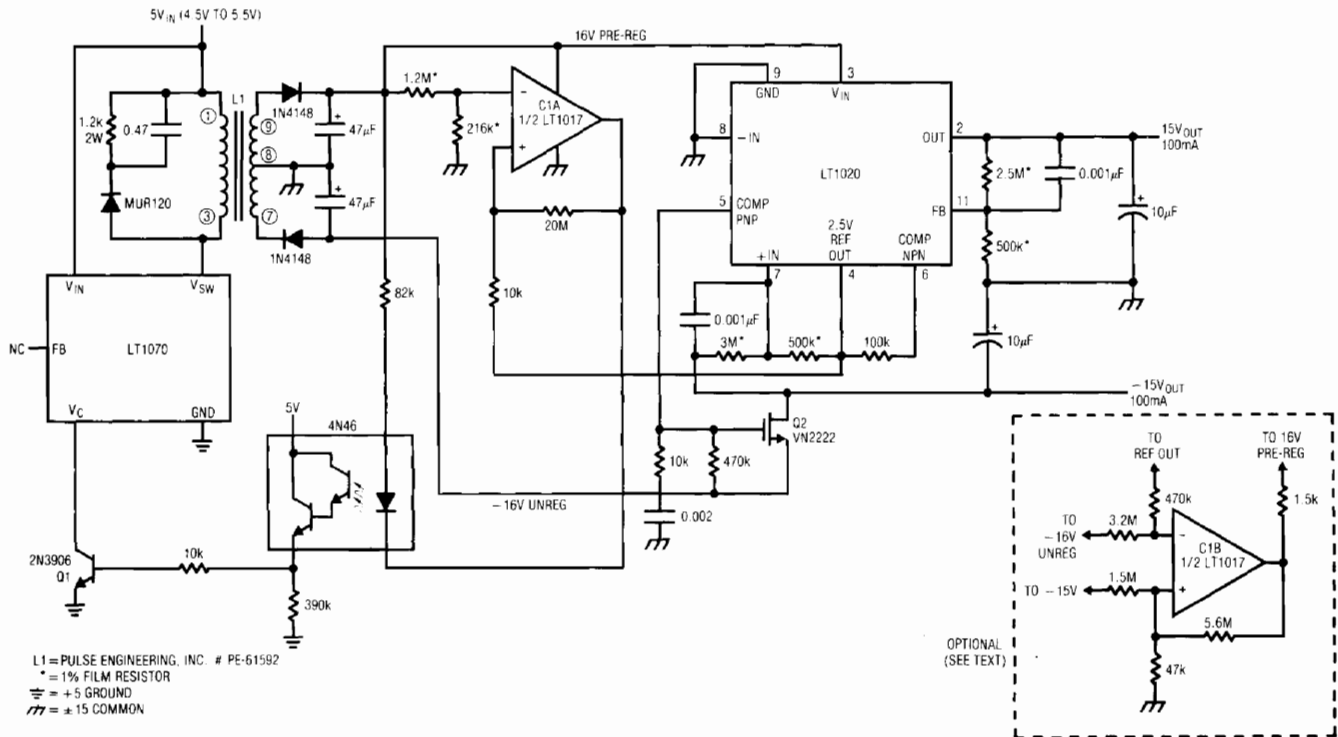


Figure 8. Low IQ, Isolated 5V to ±15V Converter

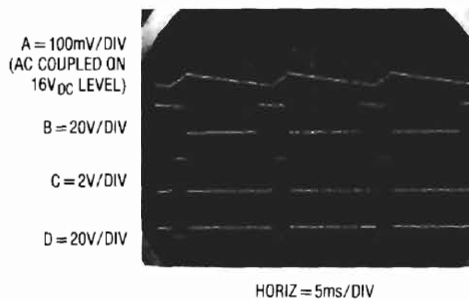


Figure 9. Waveforms for the Low IQ 5V to ±15V Converter

LT1070's control pin (V_C) pulls high (trace C). This causes full duty cycle 40kHz switching at the V_{SW} pin (trace D). The resultant energy into L1 forces the 16V output to ramp quickly positive, turning off C1A's output. The 20M value combined with the 4N46's slow response (note the delay between C1A going high and the V_C pin rise) gives about 40mV of hysteresis. The LT1070's on-off duty cycle is load dependent, saving significant power when the converter is lightly loaded. This characteristic is largely responsible for the 10mA quiescent current. The opto-isolator preserves the converters input-output isolation. The LT1020, a low quiescent current regulator with low drop-out, further regulates the 16V line, giving the 15V

output. The linear regulation eliminates the 40mV ripple and improves transient response. The -16V output tends to follow the regulated -16V line, but regulation is poor. The LT1020's auxiliary on-board comparator is compensated to function as an op amp by the RC damper at pin 5. This amplifier linearly regulates the -16V line. MOSFET Q2 provides low drop-out current boost, sourcing the -15V output. The -15V output is stabilized with the op amp by comparing it with the 2.5V reference via the 500K - 3M current summing resistors. 100pF capacitors frequency compensate each regulating loop. This converter functions well, providing ±15V outputs at 100mA with only 10mA quiescent current. Figure 10 plots efficiency vs. a conventional design over a range of loads. For high loads results are comparable, but the low quiescent circuit is superior at lower current.

A possible problem with this circuit is related to the poor regulation of the -16V line. If the positive output is lightly loaded L1's magnetic flux is low. Heavy negative output loading under this condition results in the -16V line falling below its output regulators drop-out value. Specifically, with no load on the 15V output only 20mA is available from the -15V output. The full 100mA is only available from the

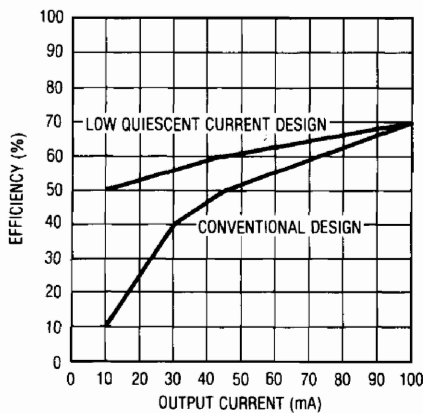


Figure 10. Efficiency vs Load for the Low I_Q Converter

– 15V output when the 15V output is supplying more than 8mA. This restriction is often acceptable, but some situations may not tolerate it. The optional connection in Figure 8 (shown in dashed lines) corrects the difficulty. C1B detects the onset of – 16V line decay. When this occurs its output pulls low, loading the 16V line to correct the problem. The biasing values given permit correction before the negative linear regulator drops out.

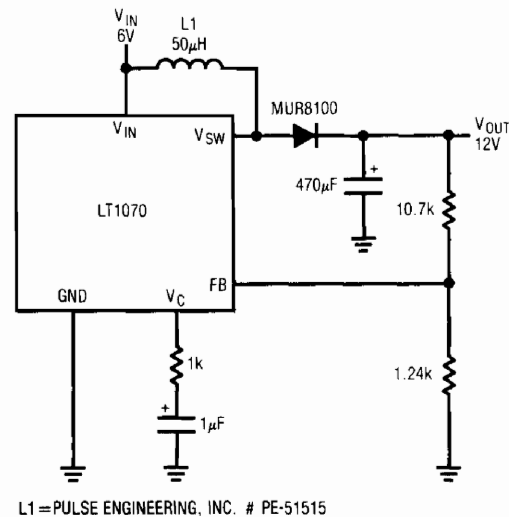
MICROPOWER QUIESCENT CURRENT CONVERTERS

Many battery powered applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or “sleep” modes draw only microamperes. A typical lap top computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any DC-DC converter designed for loop stability under no-load conditions will work. In practice, a converter’s relatively large quiescent current may cause unacceptable battery drain during low output current intervals.

Figure 11 shows a typical flyback based converter. In this case the 6V battery is converted to a 12V output by the inductive flyback voltage produced each time the LT1070’s V_{SW} pin is internally switched to ground (for commentary on inductor selection in flyback converters see Appendix D, “Inductor Selection for Flyback Converters”). An internal 40kHz clock produces a flyback event every 25 μ s. The energy in this event is controlled by the IC’s internal error amplifier, which acts to force the feedback (FB) pin to a 1.23V reference. The error amplifier’s high impedance

output (the V_C pin) uses an RC damper for stable loop compensation.

This circuit works well but pulls 9mA of quiescent current. If battery capacity is limited by size or weight this may be too high. How can this figure be reduced while retaining high current performance?



L1 = PULSE ENGINEERING, INC. # PE-51515

Figure 11. 6V to 12V, 2 Amp Converter with 9mA Quiescent Current

A solution is suggested by considering an auxiliary V_C pin function. If the V_C pin is pulled within 150mV of ground the IC shuts down, pulling only 50 microamperes. Figure 12’s special loop exploits this feature, reducing quiescent current to only 150 microamperes. The technique shown is particularly significant, with broad implication in battery powered systems. It is easily applied to a wide variety of DC-DC converters, meeting an acknowledged need across a wide spectrum of applications.

Figure 12’s signal flow is similar to Figure 11, but additional circuitry appears between the feedback divider and the V_C pin. The LT1070’s internal feedback amplifier and reference are not used. Figure 13 shows operating waveforms under no load conditions. The 12V output (trace A) ramps down over a period of seconds. During this time comparator A1’s output (trace B) is low, as are the 74C04 paralleled inverters. This pulls the V_C pin (trace C) low, putting the IC in its 50 μ A shutdown mode. The V_{SW} pin (trace D) is high, and no inductor current flows. When the 12V output drops about 20mV, A1 triggers and the inverters go high, pulling the V_C pin up and turning on the

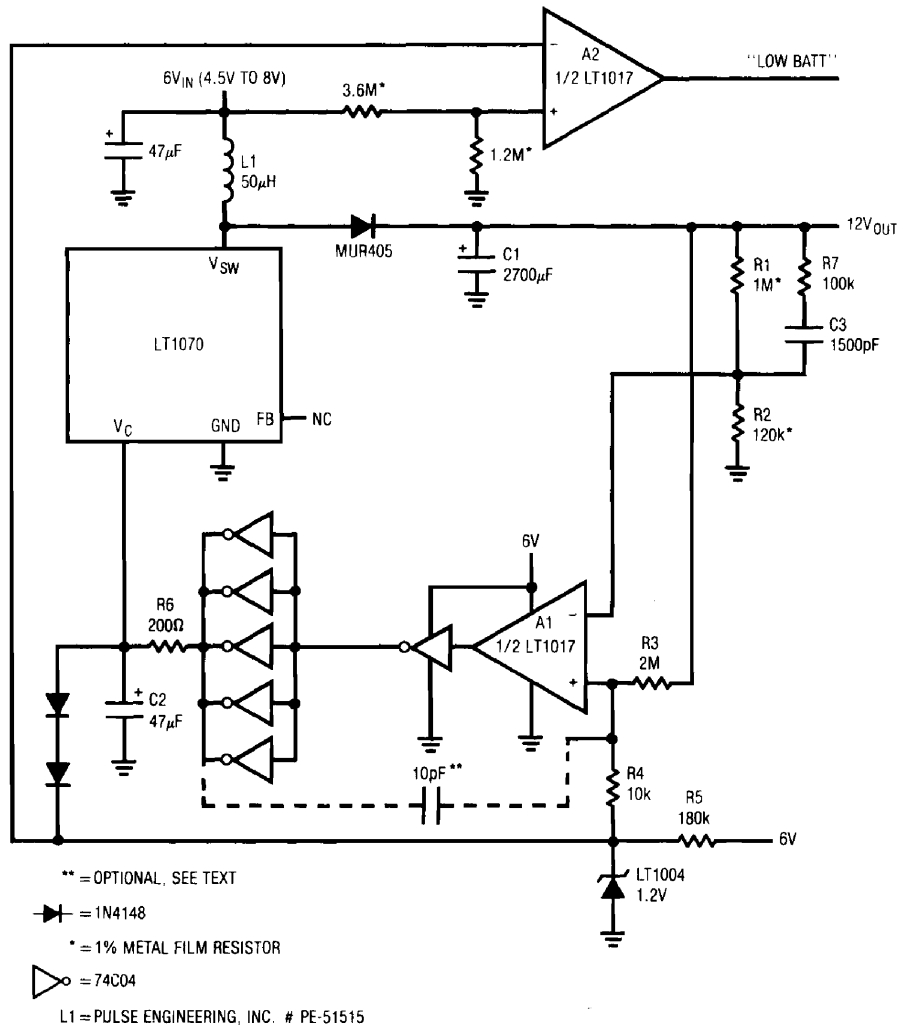


Figure 12. 6V to 12V, 2 Amp Converter with 150µA Quiescent Current

regulator. The V_{SW} pin pulses the inductor at the 40kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back into shutdown. This “bang-bang” control loop keeps the 12V output within the 20mV ramp hysteresis window set by R3-R4. Diode clamps prevent V_C pin overdrive. Note that the loop oscillation period of 4-5 seconds means the R6-C2 time constant at V_C is not a significant term. Because the LT1070 spends almost all of the time in shutdown, very little quiescent current (150µA) is drawn.

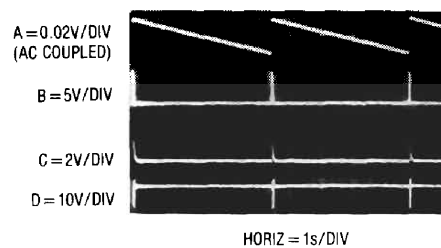


Figure 13. Low I_Q Converter Waveforms with No Load (Traces B and D Retouched for Clarity)

Application Note 29

Figure 14 shows the same waveforms with the load increased to 3mA. Loop oscillation frequency increases to keep up with the loads sink current demand. Now, the V_C pin waveform (trace C) begins to take on a filtered appearance. This is due to R6-C2's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R6-C2 time constant, however, is fixed. Beyond some frequency, R6-C2 must average loop oscillations to DC. Figure 15 shows the same circuit points at 1 ampere loading. Note that the V_C pin is at DC, and repetition rate has increased to the LT1070's 40kHz clock frequency. Figure 16 plots what is occurring, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 500Hz. At this point the R6-C2 time constant filters the V_C pin to DC and the LT1070 transitions into "normal" operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed loop gain set by the R1-R2 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R6-C2's break frequency. The phase error contributed by C1 (which was selected for low loop frequency at low output currents) is dominated by the R6-C2 roll off and the R7-C3 lead into A1. The loop is stable and responds linearly for all loads beyond 80mA. In this high current region the LT1070 is desirably "fooled" into behaving like Figure 11's circuit.

A formal stability analysis for this circuit is quite complex, but some simplifications lend insight into loop operation. At $100\mu\text{A}$ loading ($120\text{k}\Omega$) C1 and the load form a decay time constant exceeding 300 seconds. This is orders of magnitude larger than R7-C3, R6-C2, or the LT1070's 40kHz commutation rate. As a result, C1 dominates the loop. Wideband A1 sees phase shifted feedback, and very low frequency oscillations similar to Figure 13's occur. Although C1's decay time constant is long, its charge time constant is short because the circuit has low sourcing impedance. This accounts for the ramp nature of the oscillations.

Increased loading reduces the C1-load decay time constant. Figure 16's plot reflects this. As loading increases, the loop oscillates at a higher frequency due to C1's decreased decay time. When the load impedance becomes low enough C1's decay time constant ceases to dominate the loop. This point is almost entirely determined by R6

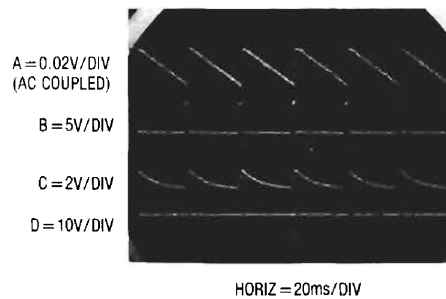


Figure 14. Low Iq Converter Waveforms at Light Loading

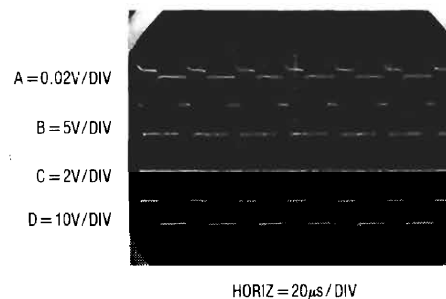


Figure 15. Low Iq Converter Waveforms at 1 Amp Loading

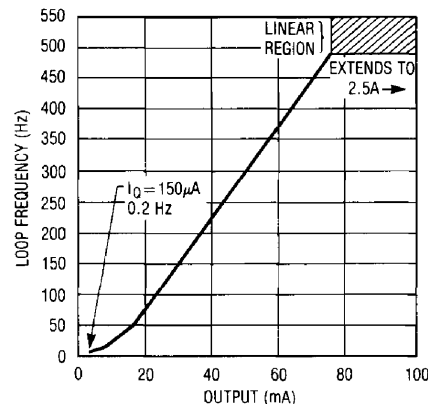


Figure 16. Figure 12's Loop Frequency vs Output Current. Note Linear Loop Operation Above 80mA.

and C2. Once R6 and C2 "take over" as the dominant time constant the loop begins to behave like a linear system. In this region (e.g. above about 75mA, per Figure 16) the LT1070 runs continuously at its 40kHz rate. Now, the R7-C3 time constant becomes significant, performing as a simple feedback lead to smooth output response. There is a fundamental trade-off in the selection of the R7-C3 lead network values. When the converter is running in its linear

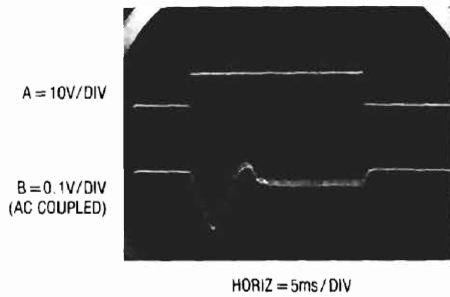


Figure 17. Load Transient Response for Figure 12's Low I_Q Regulator

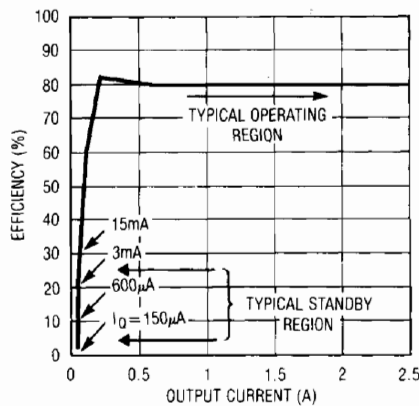


Figure 18. Efficiency vs Output Current for Figure 12. Standby Efficiency is Poor, But Power Loss Approaches Battery Self-Discharge.

region they must dominate the DC hysteresis deliberately generated by R3-R4. As such, they have been chosen for the best compromise between output ripple at high load and loop transient response.

Despite the complex dynamics transient response is quite good. Figure 17 shows performance for a step from no load to 1 ampere. When trace A goes high a 1 ampere load appears across the output (trace B). Initially, the output sags almost 150mV due to slow loop response time (the R6-C2 pair delay V_C pin response). When the LT1070 comes on (signaled by the 40kHz “fuzz” at the bottom extreme of trace B) response is reasonably quick and surprisingly well behaved considering circuit dynamics. The

multi-time constant decay (“rattling” is perhaps more appropriate) is visible as trace B approaches steady state between the 4th and 5th vertical divisions.

A2 functions as a simple low battery detector, pulling low when V_{IN} drops below 4.8V.

Figure 18 plots efficiency vs. output current. High power efficiency is similar to standard converters. Low power efficiency is somewhat better, although poor in the lowest ranges. This is not particularly bothersome, as *power* loss is very small.

This loop provides a controlled, conditional instability instead of the more usually desirable (and often elusive) unconditional stability. This deliberately introduced characteristic lowers converter quiescent current by a factor of 60 without sacrificing high power performance. Although demonstrated in a boost converter, it is readily exportable to other configurations. Figure 19A's step down (buck mode) configuration uses the same basic loop with almost no component changes. P-channel MOSFET Q1 is driven from the LT1072 (a low power version of the LT1070) to convert 12V to a 5V output. Q2 and Q3 provide current limiting, while Q4 supplies turn off drive to Q1. The lower output voltage mandates slightly different hysteresis biasing than Figure 12, accounting for the 1MΩ value at the comparators positive input. In other respects the loop and its performance are identical. Figure 19B uses the loop in a transformer based multi-output converter. Note that the floating secondaries allow a -12V output to be obtained with a positive voltage regulator.

Low Quiescent Current Micropower 1.5V to 5V Converter

Figure 20 extends our study of low quiescent current converters into the low voltage, micropower domain. In some circumstances, due to space or reliability considerations, it is preferable to operate circuitry from a single 1.5V cell. This eliminates almost all IC's as design candidates. Although it is possible to design circuitry which runs directly

¹ Some layouts may require substantial trace area to A1's inputs. In such cases the optional 10pF capacitor shown ensures clean transitions at A1's output.

² “Zero Compensation” for all you technosnobs out there.

³ Once again, “multi-pole settling” for those who adore jargon.

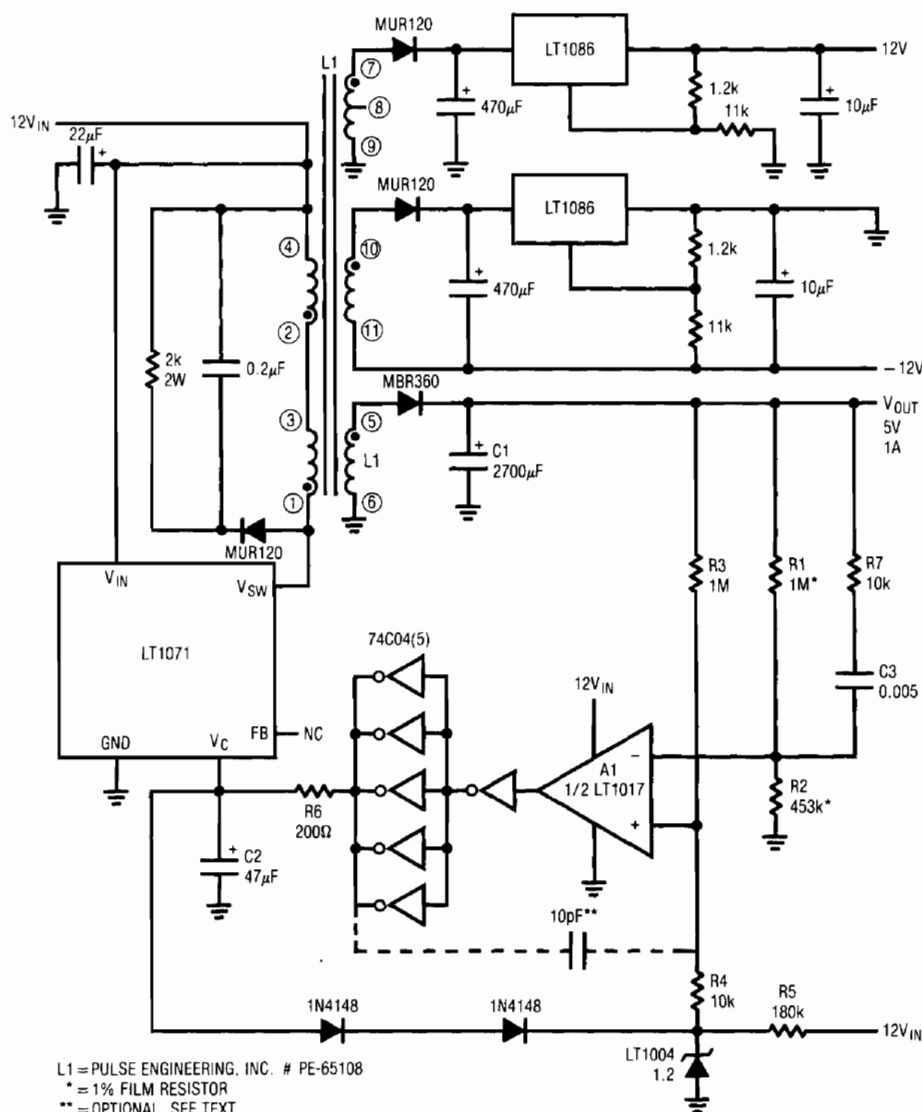


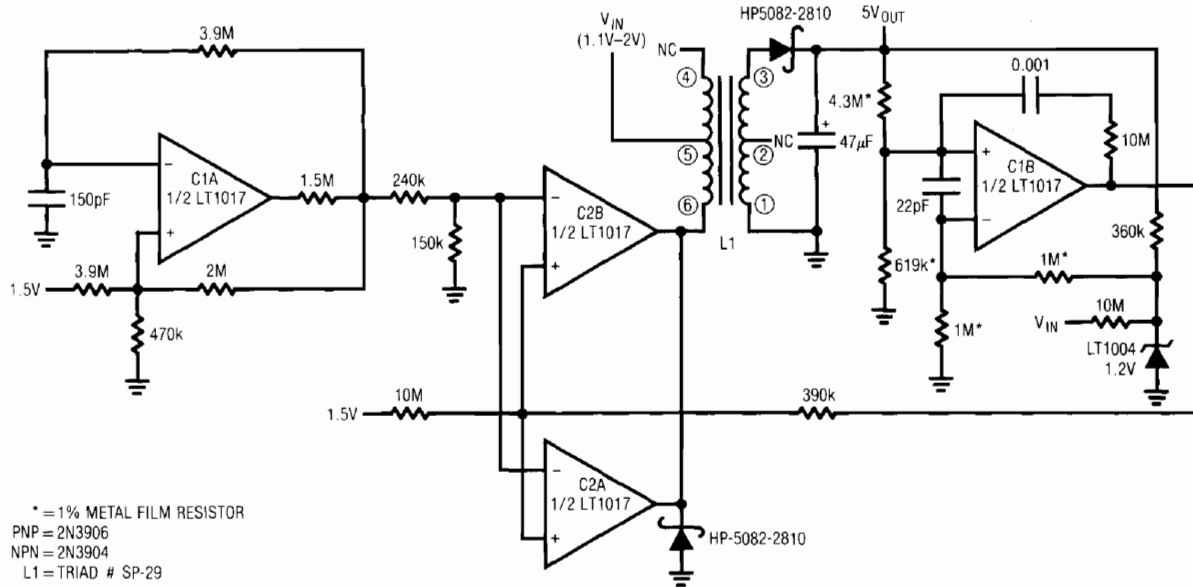
Figure 19B. Multi-Output, Transformer Coupled Low Quiescent Current Converter

The 1.2V LT1004 reference biasing is bootstrapped to the 5V output, permitting circuit operation down to 1.1V. A 10M bleed to supply ensures start-up. The 1M resistors divide down the 1.2V reference, keeping C1B inside common mode limits. C1B's positive feedback RC pair sets about 100mV hysteresis and the 22pF unit suppresses high frequency oscillation.

The micropower comparators and very low duty cycles at light load minimize quiescent current. The 125µA figure noted is quite close to the LT1017's steady state currents. As load increases the duty cycle rises to meet the

demand, requiring more battery power. Decrease in battery voltage produces similar behavior. Figure 22 plots available output current vs. battery voltage. Predictably, the highest power is available with a fresh cell (e.g. 1.5V-1.6V), although regulation is maintained down to 1.15V for 250µA loading. The plot shows that the test circuit continued to regulate below this point, but this cannot be relied on in practice (LT1017 $V_{MIN} = 1.15V$). The low supply voltage makes saturation and other losses in this circuit difficult to control. As such, efficiency is about 50%.

Application Note 29



OPTIONAL FOR
 NEGATIVE
 OUTPUT
 (SEE TEXT)

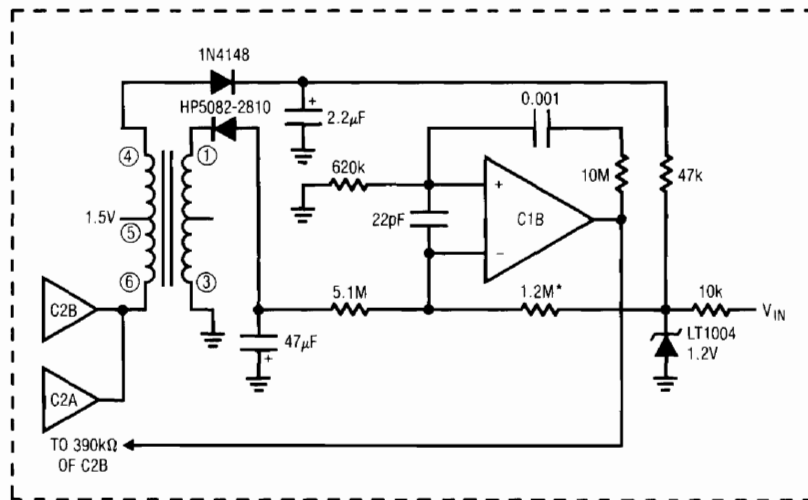


Figure 20. 800 μ A Output 1.5V to 5V Converter

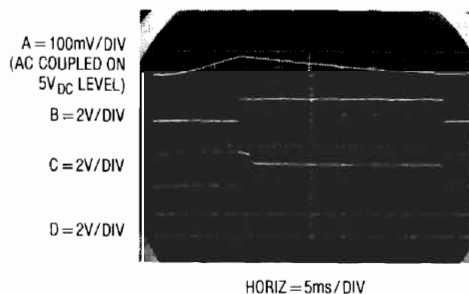


Figure 21. Waveforms for Low Power 1.5V to 5V Converter

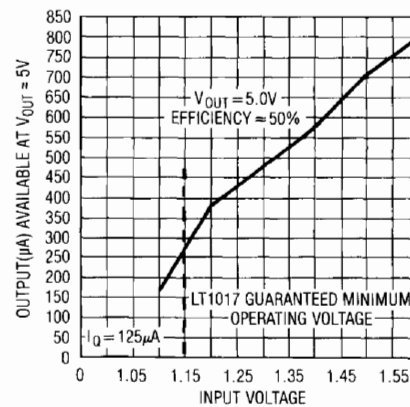


Figure 22. Output Current Capability vs Input Voltage for Figure 20

The optional connection in Figure 20 (shown in dashed lines) takes advantage of the transformers floating secondary to furnish a $-5V$ output. Drive circuitry is identical, but C1B is rearranged as a current summing comparator. The LT1004's bootstrapped positive bias is supplied by L1's primary flyback spikes.

200mA Output 1.5V to 5V Converter

Although useful, the preceding circuit is limited to low power operation. Some 1.5V powered systems (survival 2-way radios, remote, transducer fed data acquisition systems, etc.) require much more power. Figure 23's design supplies a 5V output with 200mA capacity. Some sacrifice in quiescent current is made in this circuit. This is predicated on the assumption that it operates continuously at

high power. If lowest quiescent current is necessary the technique detailed back in Figure 12 is applicable.

The circuit is essentially a flyback regulator, similar to Figure 11. The LT1070's low saturation losses and ease of use permit high power operation and design simplicity. Unfortunately, this device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible, but requires some form of start-up mechanism. Dual comparator C1 and the transistors form a start-up loop. When power is applied C1A oscillates (trace A, Figure 24) at 5kHz. Q1 biases, driving Q2's base hard. Q2's collector (trace B) pumps L1, causing voltage step-up flyback events. These events are rectified and stored in the $500\mu F$ capacitor, producing the circuit's DC output. C1B is set up so it (trace C) goes low when circuit

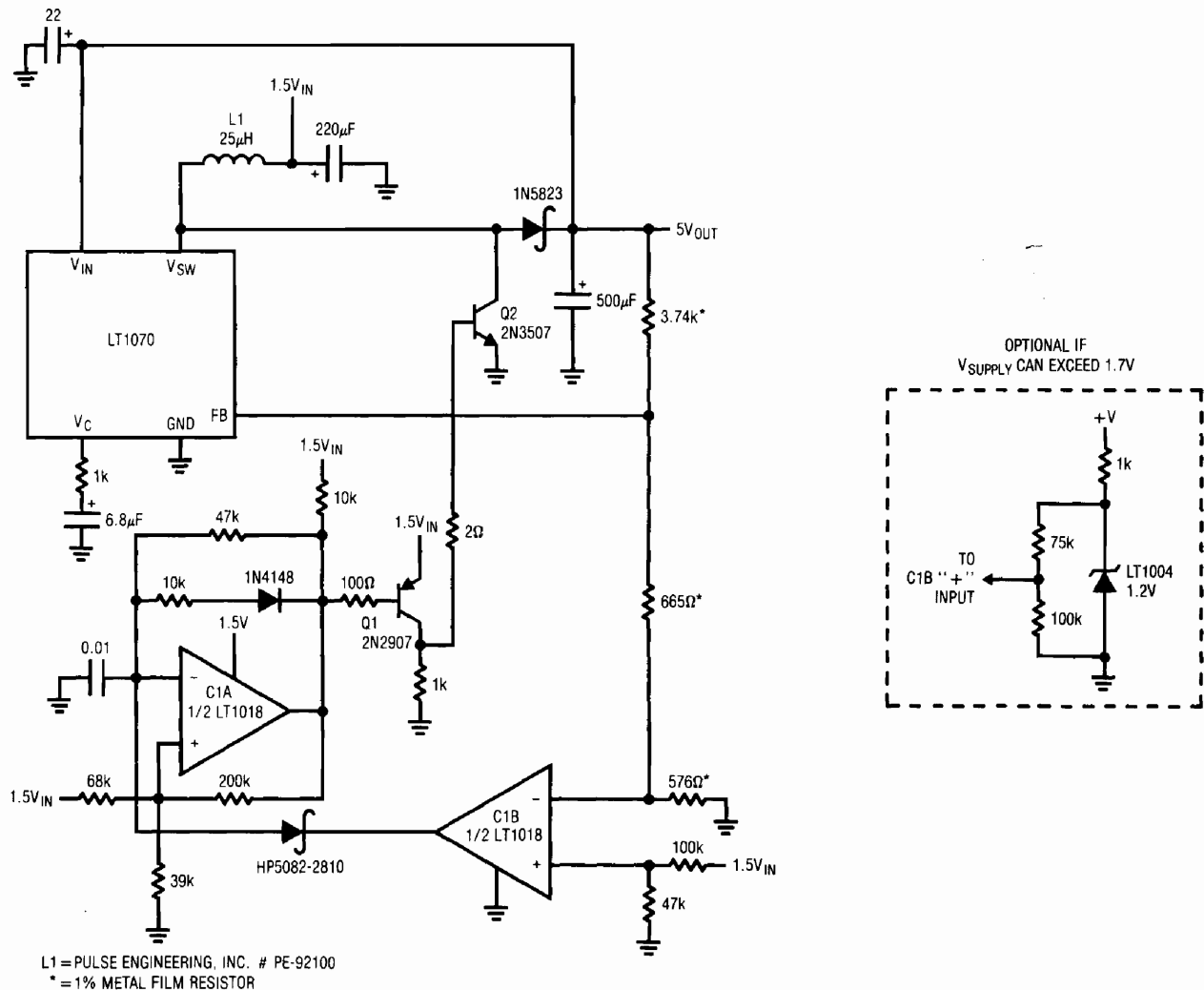


Figure 23. 200mA Output 1.5V to 5V Converter

Application Note 29

output crosses about 4.5V. When this occurs C1A's integration capacitor is pulled low, stopping it from oscillating. Under these conditions Q2 can no longer drive L1, but the LT1070 can. This behavior is observable at the LT1070's V_{SW} pin (the junction of L1, Q2's collector and the LT1070), trace D. When the start-up circuit goes off, the LT1070 V_{IN} pin has adequate supply voltage and it begins operation. This occurs at the 4th vertical division of the photograph. There is some overlap between start-up loop turn-off and LT1070 turn-on, but it has no detrimental effect. Once the circuit is running it functions similarly to Figure 11.

The start-up loop must be carefully designed to function over a wide range of loads and battery voltages. Start-up currents exceed 1 ampere, necessitating attention to Q2's saturation and drive characteristics. The worst case is a nearly depleted battery and heavy output loading. Figure 25 shows circuit output starting into a 100mA load at $V_{BATT} = 1.2V$. The sequence is clean, and the LT1070 takes over at the appropriate point. In Figure 26, loading is increased to 200mA. Start-up slope decreases, but starting still occurs. The abrupt slope increase (6th vertical

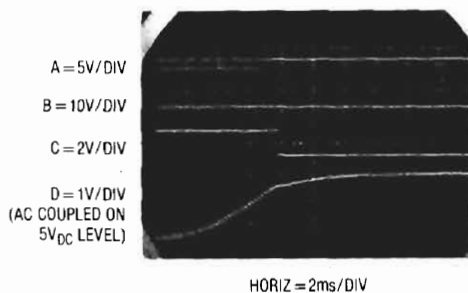


Figure 24. High Power 1.5V to 5V Converter Start-Up Sequence

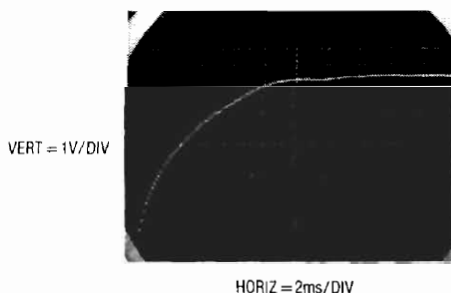


Figure 25. High Power 1.5V to 5V Converter Turn-On Into A 100mA Load at $V_{BATT} = 1.2V$

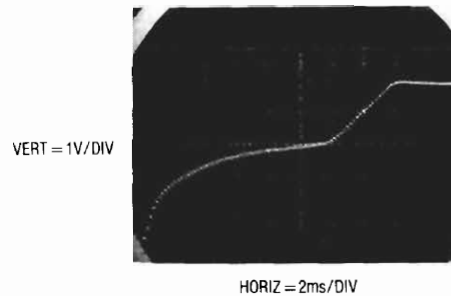


Figure 26. High Power 1.5V to 5V Converter Turn-On Into A 200mA Load at $V_{BATT} = 1.2V$

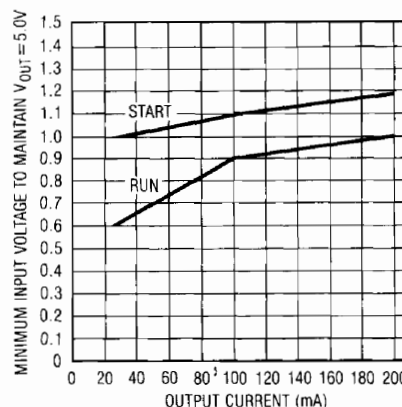


Figure 27. Input-Output Data for Figure 23

division) is due to overlapping operation of the start-up loop and the LT1070.

Figure 27 plots input-output characteristics for the circuit. Note that the circuit will start into all loads with $V_{BATT} = 1.2V$. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive full 200mA loads down to $V_{BATT} = 1.0V$. Reduced drive is possible down to $V_{BATT} = 0.6V$ (a very dead battery)! Figures 28 and 29, dynamic XY crossplot versions of Figure 27, are taken at 20 and 200 milliamperes, respectively. Figure 30 graphs efficiency at two supply voltages over a range of output currents. Performance is attractive, although at lower currents circuit quiescent power degrades efficiency. Fixed junction saturation losses are responsible for lower overall efficiency at the lower supply voltage. Figure 31 shows quiescent current increasing as supply decays. Longer inductor current charge intervals are necessary to compensate the decreased supply voltage.

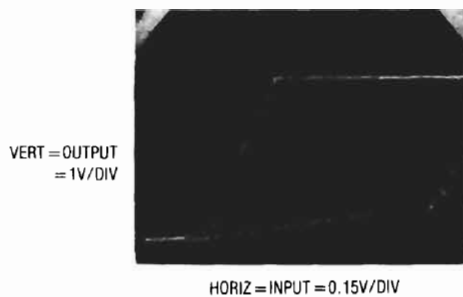


Figure 28. Input-Output XY Characteristics of the 1.5V to 5V Converter at 20mA Loading

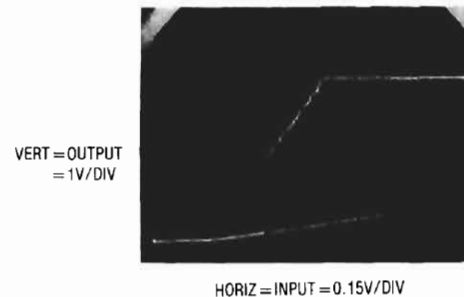


Figure 29. Input-Output XY Characteristics of the 1.5V to 5V Converter at 200mA Loading

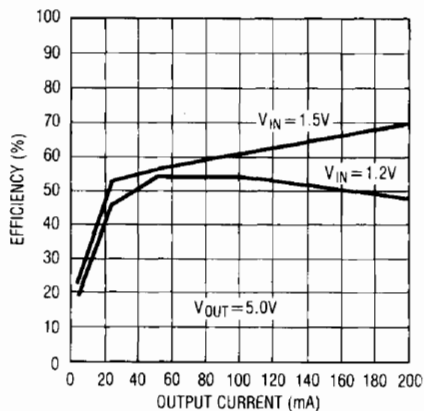


Figure 30. Efficiency vs Operating Point for Figure 23

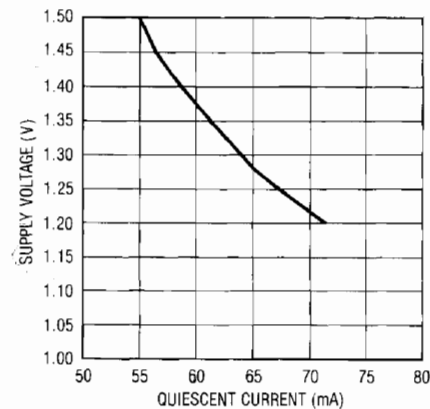


Figure 31. I_Q vs Supply Voltage for Figure 23

HIGH EFFICIENCY CONVERTERS

High Efficiency 12V to 5V Converter

Efficiency is sometimes a prime concern in DC-DC converter design (see Appendix E, "Optimizing Converters for Efficiency"). In particular, small portable computers frequently use a 12V primary supply which must be converted down to 5V. A 12V battery is attractive because it offers long life when all trade-offs and sources of loss are considered. Figure 32 achieves 90% efficiency. This circuit can be recognized as a positive buck converter. Transistor Q1 serves as the pass element. The catch diode is replaced with a synchronous rectifier, Q2, for improved efficiency. The input supply is nominally 12V but can vary from 9.5V to 14.5V. Power losses are minimized by utilizing low source-to-drain resistance, 0.028 Ω , NMOS transistors for the catch diode and pass element. The inductor, Pulse Engineering PE-92210K, is made from a low loss core material which squeezes a little more efficiency out of the

circuit. Also, keeping the current sense threshold voltage low minimizes the power lost in the current limit circuit.

Figure 33 shows the operating waveforms. Q5 drives the synchronous rectifier, Q2, when the V_{SW} pin (trace A) is turned "off". Q2 is turned off through D1 and D2 when the V_{SW} pin is "on". To turn on Q1, the gate (trace B) must be driven above the input voltage. This is accomplished by bootstrapping the capacitor, C1, off the drain of Q2 (trace C). C1 charges up through D1 when Q2 is turned on. When Q2 is turned off, Q3 is able to conduct, providing a path for C1 to turn Q1 on. During this time current flows through Q1 (trace D), through the inductor (trace E) and into the load. To turn Q1 off, the V_{SW} pin must be "off." Q5 is now able to turn on Q4 and the gate of Q1 is pulled low through D3 and the 50 Ω resistor. This resistor is used to reduce the voltage noise generated by fast switching characteristics of Q1. When Q2 is conducting (trace F), Q1

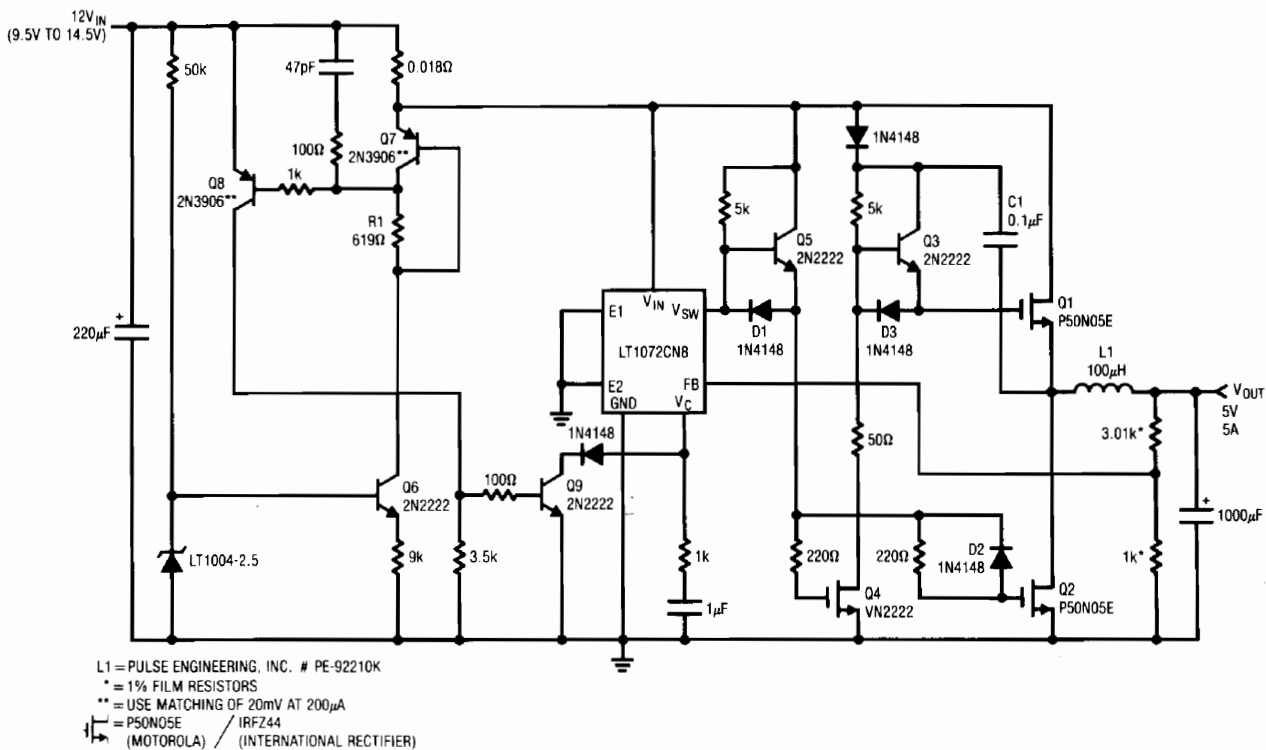


Figure 32. 90% Efficiency Positive Buck Converter with Synchronous Switch

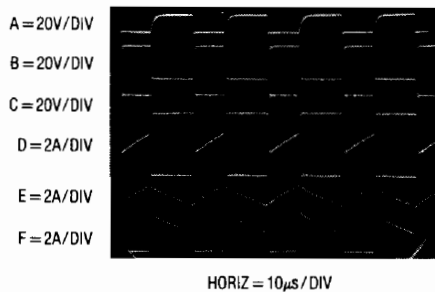


Figure 33. Waveforms for 90% Efficiency Buck Converter

must be off. The efficiency will be decreased if both transistors are conducting at the same time. The 220Ω resistors and D2 are used to minimize the overlap of the switch cycles. Figure 34 shows the efficiency vs. load plot for the circuit as shown. The other plots are for non-synchronously switched buck regulators (see indicated Figures).

Short circuit protection is provided by Q6 through Q9. A 200µA current source is generated from an LT1004, Q6 and the 9k resistor. This current flows through R1 and generates a threshold voltage of 124mV for the comparator, Q7

and Q8. When the voltage drop across the 0.018Ω sense resistor exceeds 124mV, Q8 is turned on. The LT1072's V_{SW} pin goes off when the V_C pin is pulled below 0.9V. This occurs when Q8 forces Q9 to saturate. An RC damper suppresses line transients that might prematurely turn on Q8.

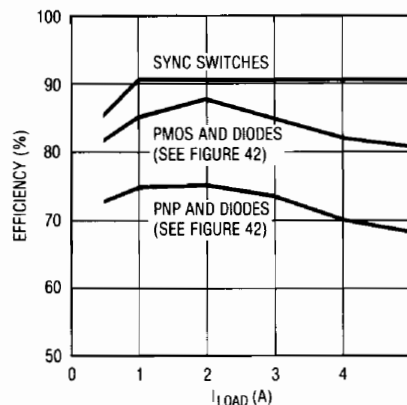
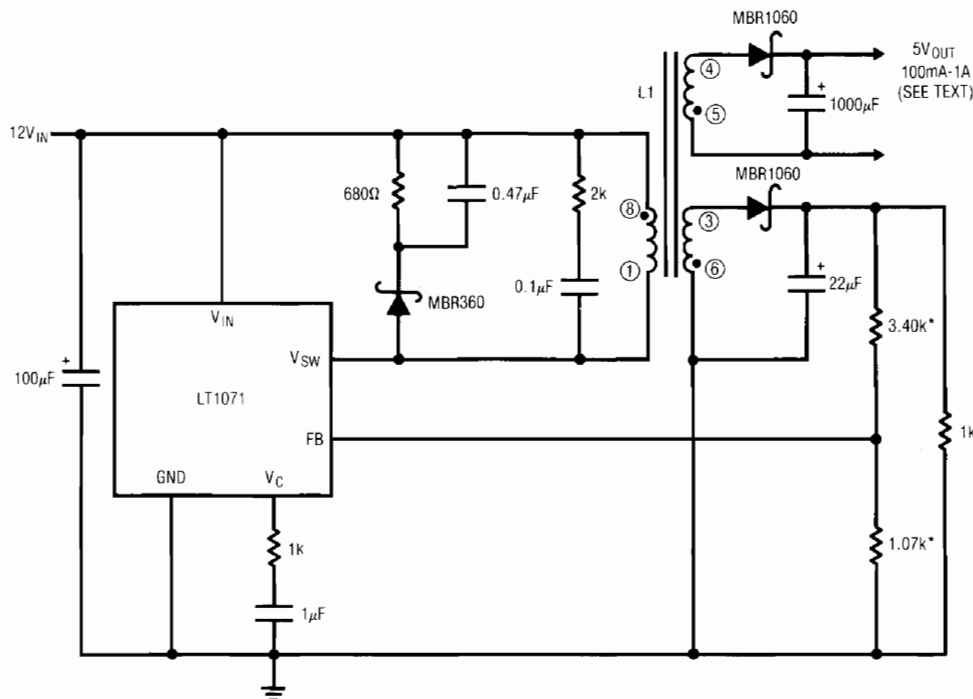


Figure 34. Efficiency vs Load for Figure 32. The Synchronous Switches Give Higher Efficiency than Simple FET or Bipolar Transistors and Diodes.



L1 = PULSE ENGINEERING, INC. # PE-65066
 * = 1% FILM RESISTORS
 MBR1060 = MOTOROLA

Figure 35. High Efficiency Flux Sensed Isolated Converter

High Efficiency, Flux Sensed Isolated Converter

Figure 35's 75% efficiency is not as good as the previous circuit, but it has a fully floating output. This circuit uses a bifilar wound flux sensing secondary to provide isolated voltage feedback. In operation the LT1070's V_{SW} pin (trace A, Figure 36) pulses L1's primary, producing identical waveforms at the floating power and flux sensing secondaries (traces B and C). Feedback occurs from the flux sense winding via the diode and capacitive filter. The 1k resistor provides a bleed current, while the 3.4k-1.07k divider sets output voltage. The diode partially compensates the diode in the power output winding, resulting in an overall temperature coefficient of about 100ppm/°C. The oversized diode aids efficiency, although significant improvement (e.g. 5%-10%) is possible if synchronous rectification is employed, as in Figure 32. The primary damper network is unremarkable, although the 2k-0.1μF network has been added to suppress excessive ringing at low output current. This ringing is not deleterious to circuit

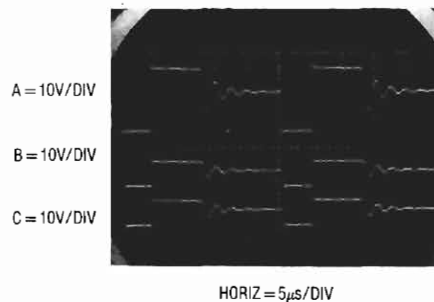


Figure 36. Waveforms for Flux Sensed Converter

operation, and the network is optional. Below about 10% loading non-ideal transformer behavior introduces significant regulation error. Regulation stays within $\pm 100\text{mV}$ from 10% to 100% of output rating, with excursion exceeding 900mV at no load. Figure 37's circuit trades away isolation for tight regulation with no output loading restrictions. Efficiency is the same.

Application Note 29

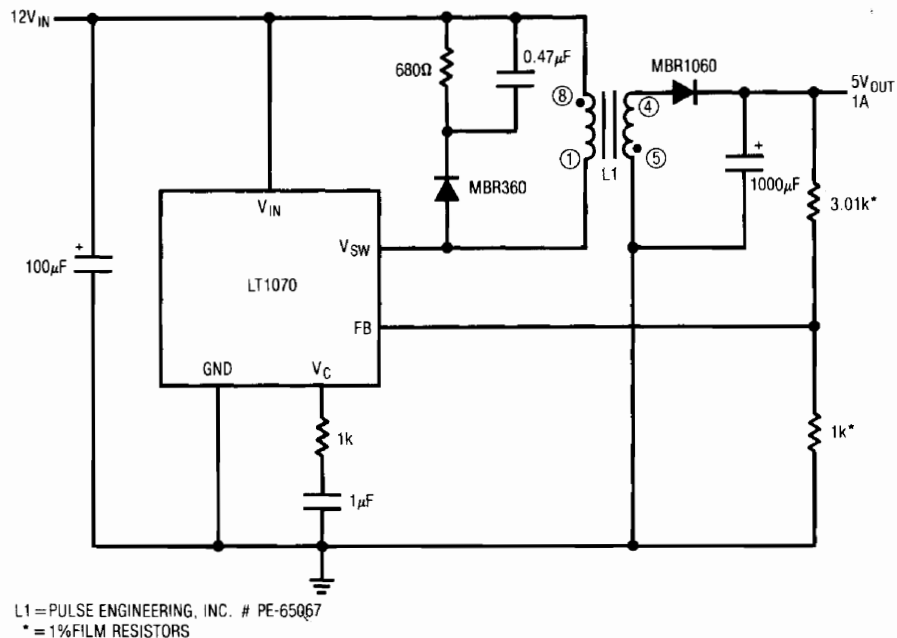


Figure 37. Non-Isolated Version of Figure 35

WIDE RANGE INPUT CONVERTERS

Wide Range Input – 48V to 5V Converter

Often converters must accommodate a wide range of inputs. Telephone lines can vary over considerable tolerances. Figure 38's circuit uses an LT1072 to supply a 5V output from a telecom input. The raw telecom supply is nominally –48V but can vary from –40V to –60V. This range of voltages is acceptable to the V_{SW} pin but protection is required for the V_{IN} pin ($V_{MAX} = 60V$). Q1 and the 30V zener diode serve this purpose, dropping V_{IN} 's voltage to acceptable levels under all line conditions.

Here, the “top” of the inductor is at ground and the LT1072's ground pin at –V. The feedback pin senses with respect to the ground pin, so a level shift is required from the 5V output. Q2 serves this purpose, introducing only –2mV/°C drift. This is normally not objectionable in a logic supply. It can be compensated with the optional appropriately scaled diode-resistor shown in Figure 38.

Frequency compensation uses an RC damper at the V_C pin. The 68V zener is a type designed to clamp and absorb excessive line transients which might otherwise damage the LT1072 (V_{SW} maximum voltage is 75V).

Figure 39 shows operating waveforms at the V_{SW} pin. Trace A is the voltage and trace B the current. Switching is crisp, with well controlled waveforms. A higher current version of this circuit appears in LTC Application Note AN-25, “Switching Regulators For Poets.”

3.5V to 35V_{IN} – 5V_{OUT} Converter

Figure 40's approach has an even wider input range. In this case it produces either a –5V or 5V output (shown in dashed lines). This circuit is an extension of Figure 11's basic flyback topology. The coupled inductor allows the option for buck, boost, or buck-boost converters. This circuit can operate down to 3.5V for battery applications while accepting 35V inputs.

Figure 41 shows the operating waveforms for this circuit. During the V_{SW} (trace A) “on” time, current flows through the primary winding (trace B). No current is transferred to the secondary because the catch diode, D1, is reverse biased. The energy is stored in the magnetic field. When the switch is turned “off” D1 forward biases and the energy is transferred to the secondary winding. Trace C is

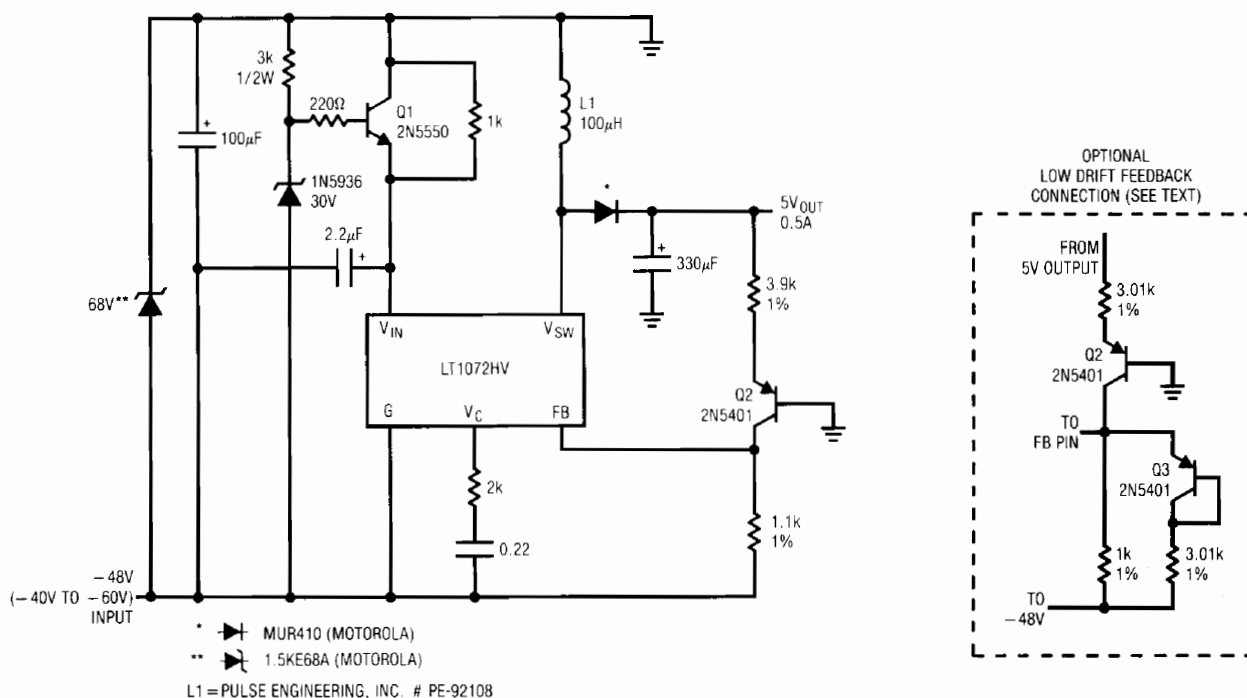


Figure 38. Wide Range Input Converter

the voltage seen on the secondary and trace D is the current flowing through it. This is not an ideal transformer so not all of the primary windings energy is coupled into the secondary. The energy left in the primary winding causes the overvoltage spikes seen on the V_{SW} pin (trace E). This phenomenon is modeled by a leakage inductance term which is placed in series with the primary winding. When the switch is turned "off" current continues to flow in the inductor causing the snubber diode to conduct (trace F). The snubber diode current falls to zero as the inductor loses its energy. The snubber network clamps the voltage spike. When the snubber diode current reaches zero, the V_{SW} pin voltage settles to a potential related to the turns ratio, output voltage and input voltage.¹

The feedback pin senses with respect to ground, so Q1 through Q3 provides the level shift from the -5V output. Q1 introduces a $-2mV/^\circ C$ drift to the circuit. This effect can be compensated by a circuit similar to the one shown in Figure 38. Line regulation is degraded due to Q3's output impedance. If this is a problem, an op amp must be used to perform the level shift (see AN-19, Figure 29).

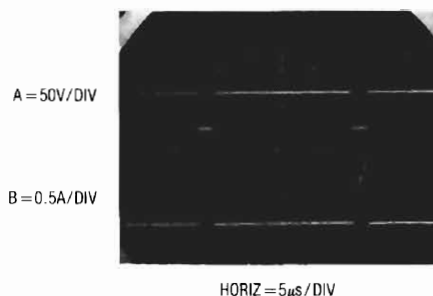


Figure 39. Waveforms for Wide Range Input Converter

Wide Range Input Positive Buck Converter

Figure 42 is another example of a positive buck converter. This is a simpler version compared to the synchronous switch buck, Figure 32. However, efficiency isn't as high (see Figure 34). If the PMOS transistor is replaced with a Darlington PNP transistor (shown in dashed lines) efficiency decreases further.

¹ Application Note AN-19, "LT1070 Design Manual," page 25.

Application Note 29

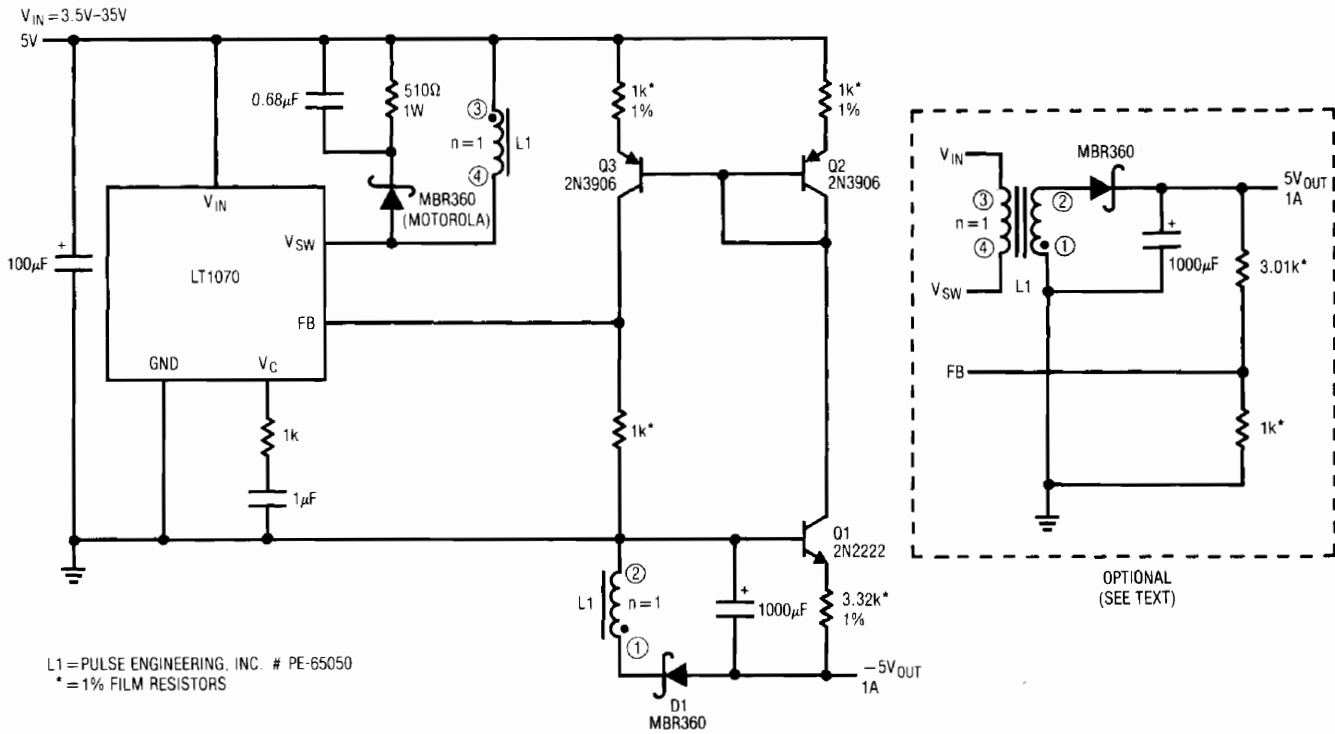


Figure 40. Wide Range Input Positive to Negative Flyback Converter

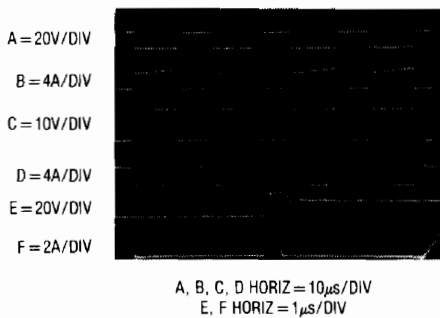


Figure 41. Waveforms for Wide Range Input Positive -5V Output Flyback Converter

Figure 43A shows the operating waveforms for this circuit. The pass transistor's (Q1) drive scheme is similar to the one shown in Figure 32. During the V_{SW} (trace A) "on" time, the gate of the pass transistor is pulled down through D1. This forces Q1 to saturate. Trace B is the voltage seen on the drain of Q1 and trace C is the current passing through Q1. The supply current flows through the inductor (trace D) and into the load. During this time energy is being stored in the inductor. When voltage is applied to the inductor, current does not instantly rise. As

the magnetic field builds up, the current builds. This is seen in the inductor current waveform (trace D). When the V_{SW} pin is "off," Q2 is able to conduct and turns Q1 off. Current can no longer flow through Q1, instead D2 is conducting (trace E). During this period some of the energy stored in the inductor will be transferred to the load. Current will be generated from the inductor as long as there is any energy in it. This can be seen in Figure 43A. This is known as continuous mode operation. If the inductor is completely discharged, no current will be generated (see Figure 43B). When this happens neither switch, Q1 or D2, is conducting. The inductor looks like a short and the voltage on the cathode of D2 will settle to the output voltage. These "boingies" can be seen in trace B of Figure 43B. This is known as discontinuous mode operation. Higher input voltages can be handled with the gate-source zener clamped by D2. The 400 milliwatt zener's current must be rescaled by adjusting the 50Ω value. Maximum gate-source voltage is 20V. The circuit will function up to 35V_{IN}. At inputs beyond 35V all semiconductor breakdown voltages must be considered.

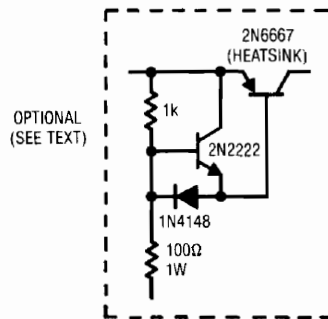
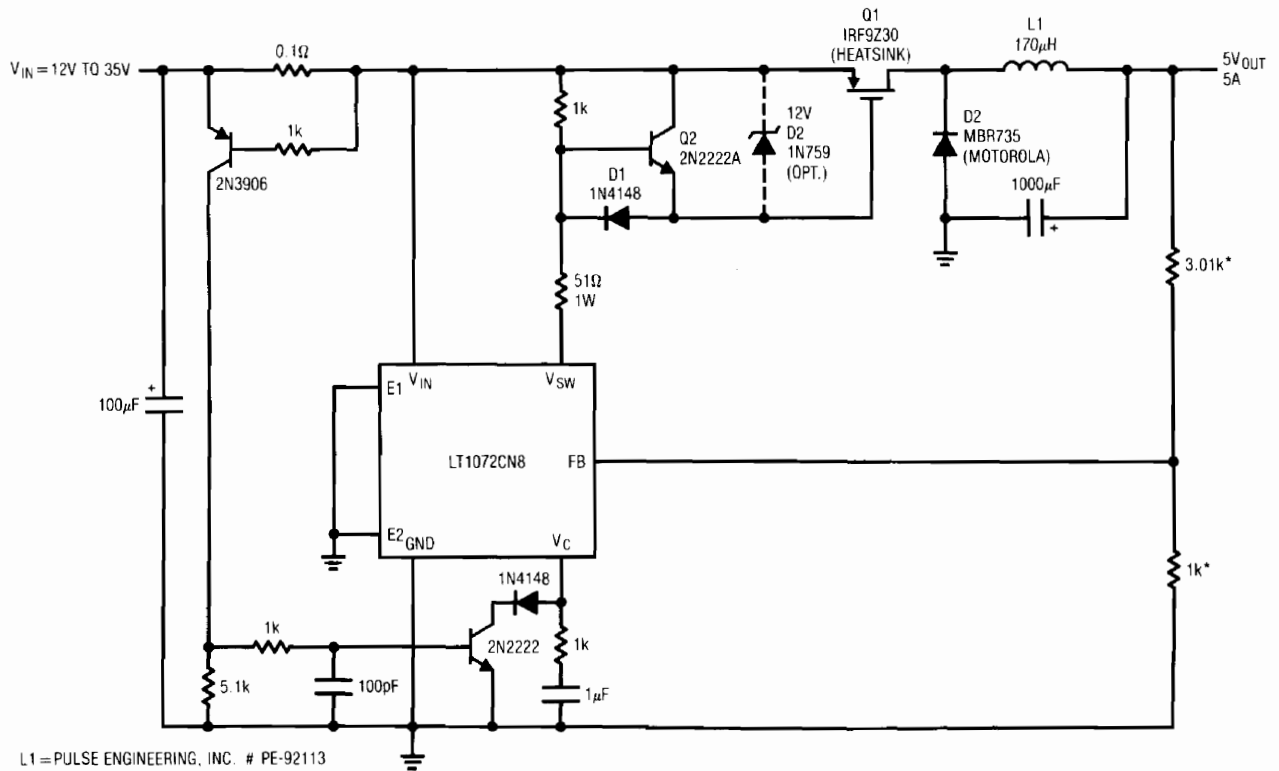


Figure 42. Positive Buck Converter

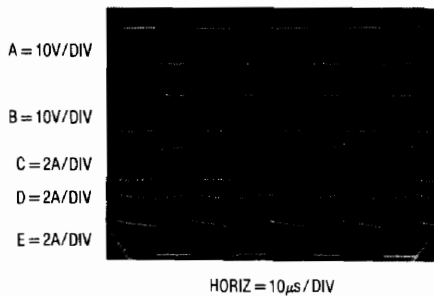


Figure 43A. Waveforms for Wide Range Input Positive Buck Converter (Continuous Mode)

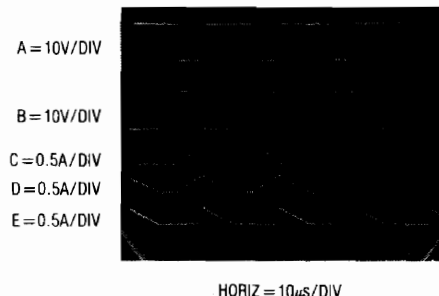


Figure 43B. Waveforms for Wide Range Input Positive Buck Converter (Discontinuous Mode)

Application Note 29

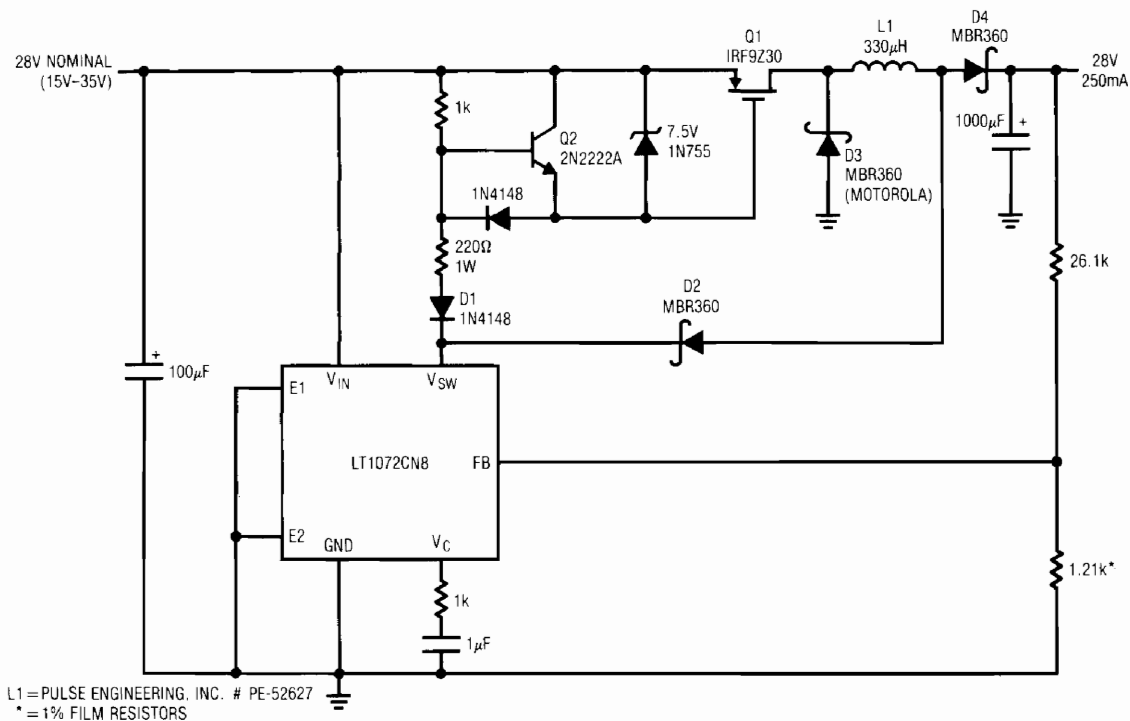


Figure 44. Positive Buck-Boost Converter

Buck Boost Converter

The buck boost topology is useful when the input voltage can either be higher or lower than the output. In this example, Figure 44, this is accomplished with a single inductor instead of a transformer, as in Figure 40 (optional). However, the input voltage range only extends down to 15V and can reach to 35V. If the maximum 1.25A switch current rating of the LT1072 is exceeded an LT1071 or LT1070 can be used instead. At high power levels package thermal characteristics should be considered.

The operation of the circuit is similar to the positive buck converter, Figure 42. The gate drive to the pass transistor is derived the same way except the gate-source voltage is clamped. Remember, the gate-source maximum voltage rating is specified at $\pm 20V$. Figure 45 shows the operating waveforms. When the V_{SW} pin is "on" (trace A), the pass transistor, Q1, is saturated. The gate voltage (trace B) is clamped by the zener diode. Trace C is the voltage on the drain of Q1 and trace D is the current through it. This is where the similarities between the two circuits end. Notice the inductor is pulled to within a diode drop, D2, above

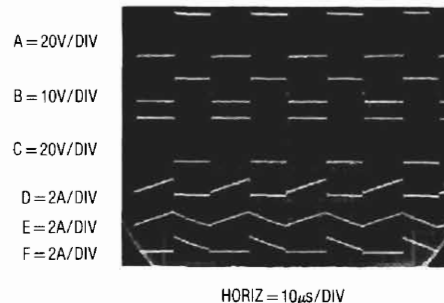


Figure 45. Waveforms for Positive Buck-Boost Converter

ground, instead of being tied to the output (see Figure 42). In this case, the inductor has the input voltage applied across it, except for a V_{be} and saturation losses. D4 is reverse biased and blocks the output capacitor from discharging into the V_{SW} pin. When the V_{SW} pin is "off" Q1 and D2 cease to conduct. Since the current in the inductor (trace E) continues to flow, D3 and D4 are forward biased and the energy in the inductor is transferred into the load. Trace F is the current through D3. Also, D2 keeps Q1 from staying on if the circuit is operating in buck mode. D1, on the other hand, blocks current from flowing into the gate drive circuit when operating in boost mode.

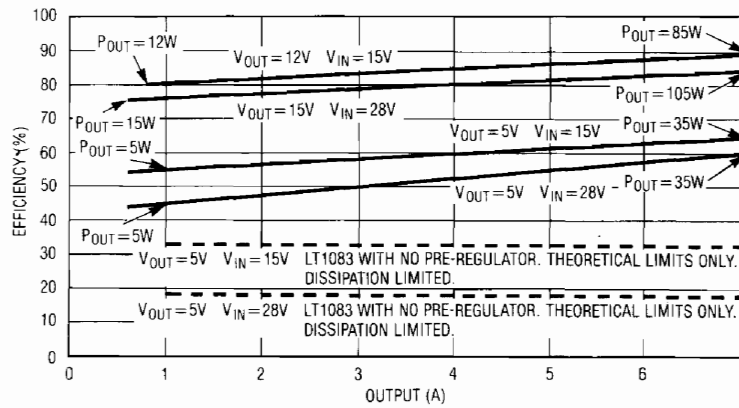


Figure 48. Efficiency vs Output Current for Figure 46 at Various Operating Points

Figure 48 plots efficiency at various operating points. Junction losses and the loop enforced 1.8V across the LT1083 are relatively small at high output voltages, resulting in good efficiency. Low output voltages do not fare as well, but compare very favorably to the theoretical data for the LT1083 with no pre-regulator. At the higher theoretical dissipation levels the LT1083 will shut down, precluding practical operation.

HIGH VOLTAGE CONVERTERS

High Voltage Converter — 1000V_{OUT}, Non-Isolated

Photomultiplier tubes, ion generators, gas based detectors, image intensifiers and other applications need high voltages. Converters frequently supply these potentials. Generally, the limitation on high voltage is transformer insulation breakdown. A transformer is almost always used because a simple inductor forces excessive voltages on the semiconductor switch. Figure 49's circuit, reminiscent of Figure 11's basic flyback configuration, is a 15V to 1000V_{OUT} converter. The LT1072 controls output by modulating the flyback energy into L1, forcing its feedback (FB) pin to 1.23V (the internal reference value). In this example loop compensation is heavily overdamped by the V_C pin capacitor. L1's damper network limits flyback spikes within the V_{SW} pin's 75V rating.

Fully Floating, 1000V_{OUT} Converter

Figure 50 is similar to Figure 49 but features a fully floating output. This provision allows the output to be referenced off system ground, often desirable for noise or

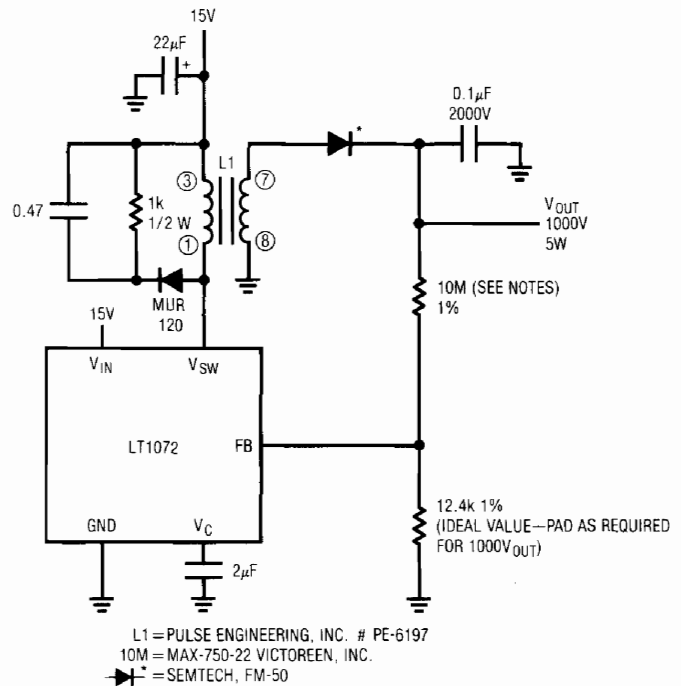


Figure 49. Non-Isolated 15V to 1000V Converter

biasing reasons. Basic loop action is as before, except that the LT1072's internal error amplifier and reference are replaced with galvanically isolated equivalents. Power for these components is bootstrapped from the output via source follower Q1 and its 2.2M ballast resistor. A1 and the LT1004, micropower components, minimize dissipation in Q1 and its ballast. Q1's gate bias, tapped from the output divider string, produces about 15V at its source. A1 compares the scaled divider output with the LT1004 reference. The error signal, A1's output, drives the optocoupler.

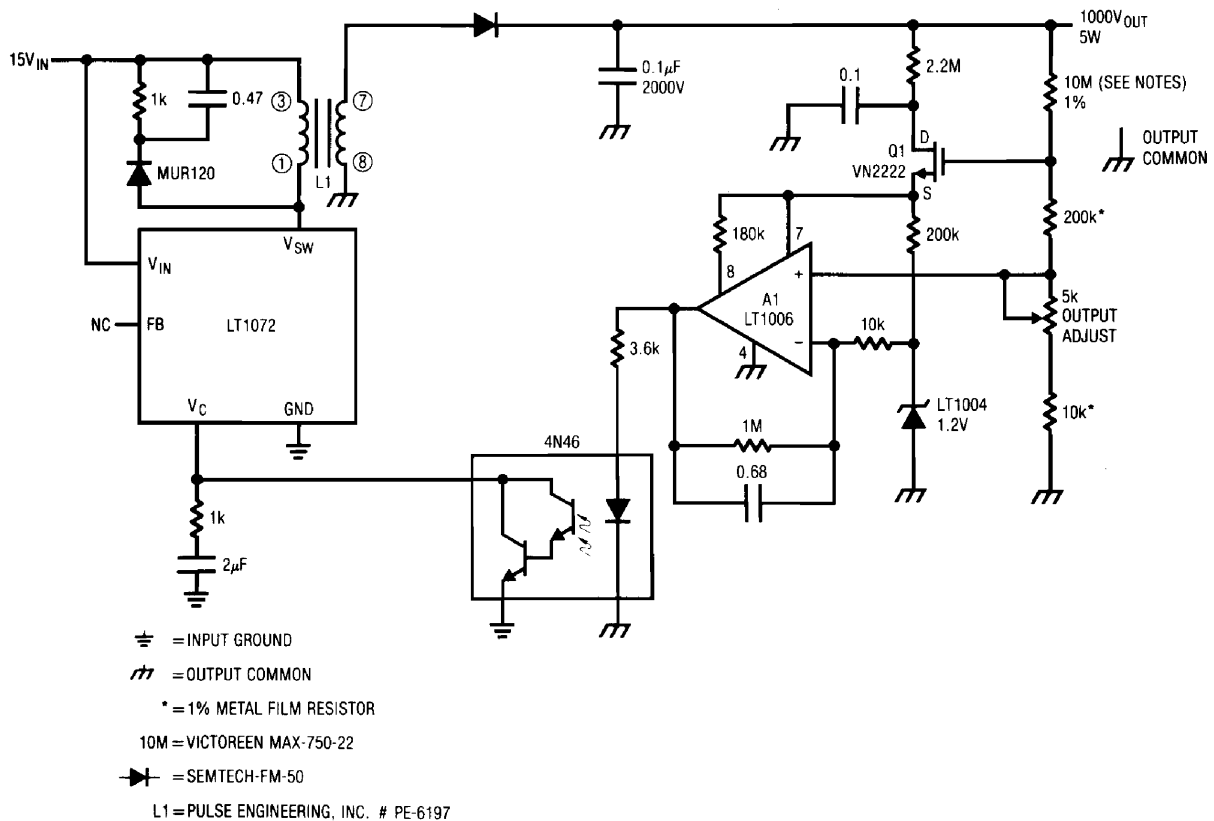


Figure 50. Isolated Output 15V to 1000V Converter

Photocurrent is kept low to save power. The optocoupler output pulls down on the V_C pin, closing a loop. Frequency compensation at the V_C pin and A1 stabilizes the loop.

The transformers isolated secondary and optical feedback produce a regulated, fully galvanically floating output. Common mode voltages of 2000V are acceptable.

20,000V_{CMV} Breakdown Converter

Figure 50's common mode breakdown limits are imposed by transformer and optocoupler restrictions. Isolation amplifiers, transducer measurement at high common mode voltages (e.g. winding temperature of a utility company transformer and ESD sensitive applications) require high breakdowns. Additionally, very precise floating measurements, such as signal conditioning for high impedance bridges, can require extremely low leakage to ground.

Achieving high common mode voltage capability with minimal leakage requires a different approach. Magnetics is usually considered the only approach for isolated transfer

of appreciable amounts of electrical energy. Transformer action is, however, achievable in the acoustic domain. Some ceramic materials will transfer electrical energy with galvanic isolation. Conventional magnetic transformers work on an electrical-magnetic-electrical basis using the magnetic domain for electrical isolation. The acoustic transformer uses an acoustic path to get isolation. The high voltage breakdown and low electrical conductance associated with ceramics surpasses isolation characteristics of magnetic approaches. Additionally, the acoustic transformer is simple. A pair of leads bonded to each end of the ceramic material forms the device. Insulation resistance exceeds $10^{12}\Omega$, with primary-secondary capacitances of 1-2pF. The material and its physical configuration determine its resonant frequency. The device may be considered as a high Q resonator, similar to a quartz crystal. As such, drive circuitry excites the device in the positive feedback path of a wideband gain element. Unlike a crystal, drive circuitry is arranged to pass substantial current through the ceramic, maximizing power into the transformer.

Application Note 29

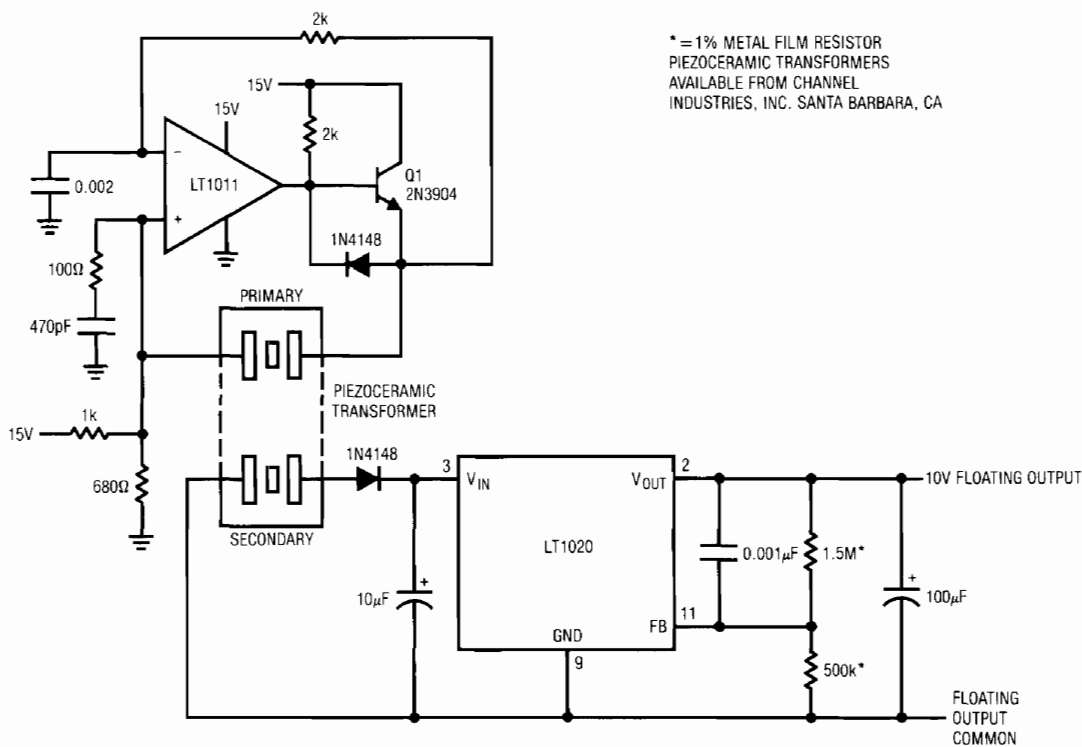


Figure 51. 15V to 10V Converter with 20,000V Isolation

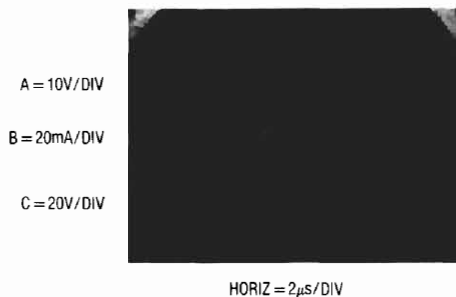


Figure 52. Waveforms for the 20,000V Isolation Converter

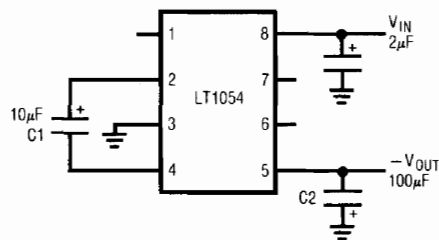


Figure 53. A Basic Switched Capacitor Converter

In Figure 51 the piezo-ceramic transformer is in the LT1011 comparators positive feedback loop. Q1 is an active pull-up for the LT1011, an open collector device. The 2k-0.002μF path biases the negative input. Positive feedback occurs at the transformers resonance, and oscillation commences (trace A, Figure 52 is Q1's emitter). Similar to quartz crystals, the transformer has significant harmonic and overtone modes. The 100Ω-470pF damper suppresses spurious oscillations and "mode hopping."

Drive current (trace B) approximates a sine wave, with peaking at the transitions. The transformer looks like a highly resonant filter to the resultant acoustic wave propagated in it. The secondary voltage (trace C) is sinusoidal. Additionally, the transformer has voltage gain. The diode and 10μF capacitor convert the secondary voltage to DC. The LT1020 low quiescent current regulator gives a stabilized 10V output. Output current for the circuit is a few milliamperes. Higher currents are possible with attention to transformer design.

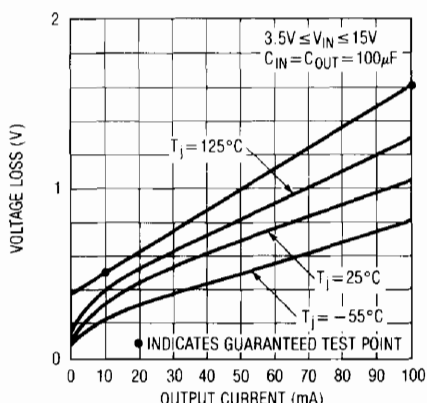


Figure 54. Losses for the Basic Switched Capacitor Converter

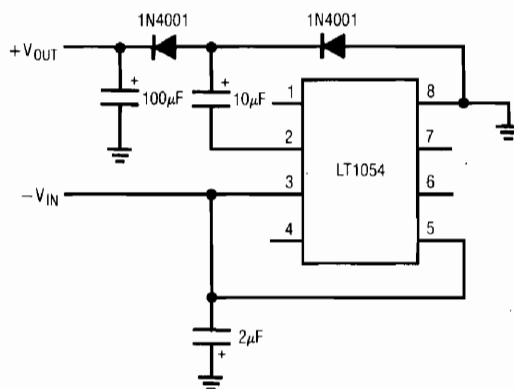


Figure 55. Switched Capacitor $-V_{IN}$ to $+V_{OUT}$ Converter

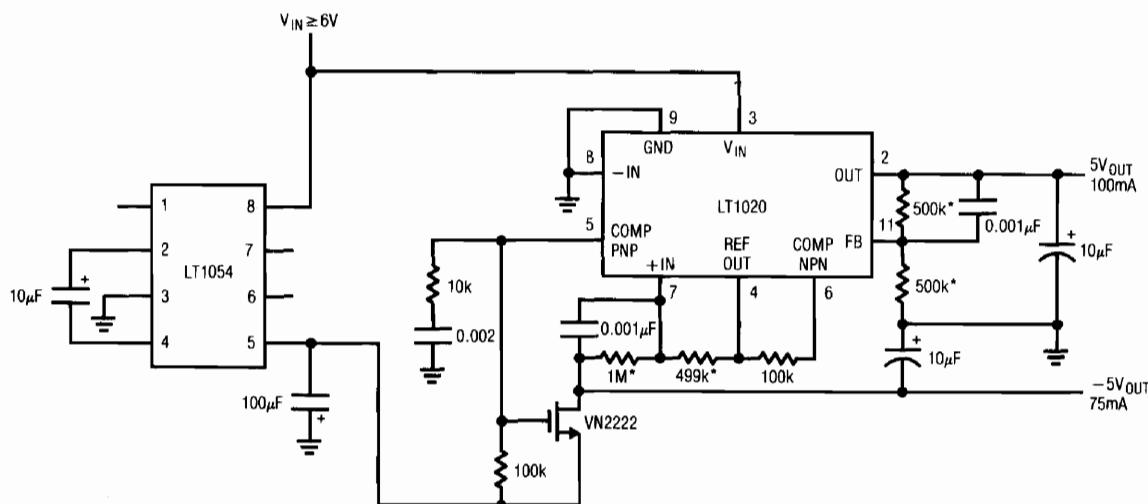


Figure 56. High Current Switched Capacitor 6V to $\pm 5V$ Converter

SWITCHED CAPACITOR BASED CONVERTERS

Inductors are used in converters because they can store energy. This stored magnetic energy, released and expressed in electrical terms, is the basis of converter operation. Inductors are not the only way to store energy with efficient release expressed in electrical terms. Capacitors store charge (already an electrical quantity) and as such, can be used as the basis for DC-DC conversion. Figure 53 shows how simple a switched capacitor based converter can be (the fundamentals of switched capacitor based conversion are presented in Appendix B, "Switched Capacitor Voltage Converters — How They Work"). The LT1054 provides clocked drive to charge C1. A second clock phase discharges C1 into C2. The internal switching

is arranged so C1 is "flipped" during the discharge interval, producing a negative output at C2. Continuous clocking allows C2 to charge to the same absolute value as C1. Junction and other losses preclude ideal results, but performance is quite good. This circuit will convert V_{IN} to $-V_{OUT}$ with losses shown in Figure 54. Adding an external resistive divider allows regulated output (see Appendix B).

With some additional steering diodes this configuration can effectively run "backwards" (Figure 55), converting a negative input to a positive output. Figure 56's variant gives low dropout linear regulation for 5V and $-5V$ outputs from $6V_{IN}$. The LT1020 based dual output regulation

Application Note 29

scheme is adapted from Figure 8. Figure 57 uses diode steering to get voltage boost, providing $\approx 2V_{IN}$. Bootstrapping this configuration with Figure 54's basic circuit leads to Figure 58, which converts a 5V input to 12V and $-12V$ outputs. As might be expected output current capacity is traded for the voltage gain, although 25mA is still available. Figure 59, another boost converter, employs a dedicated version of Figure 58 (the LT1026) to get regulated $\pm 7V$ from a 6V input. The LT1026 generates unregulated $\pm 11V$ rails from the 6V input with the LT1020 and associated components (again, purloined from Figure 8) producing regulation. Current and boost capacity are reduced from Figure 58's levels, but the regulation and simplicity are noteworthy. Figure 60 combines the LT1054's clocked switched capacitor charging with classical diode voltage multiplication, producing positive and negative outputs. At no load $\pm 13V$ is available, falling to $\pm 10V$ with each side supplying 10mA.

High Power Switched Capacitor Converter

Figure 61 shows a high power switched capacitor converter with a 1A output capacity. Discrete devices permit high power operation.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the 12V supply current flows through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 62, are the LTC1043-supplied drives to Q3 and Q4, respectively. Q1 and Q2 receive similar drive from pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one-half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the output (trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043 oscillator pin (trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF capacitor provides sharp transitions. The loop regulates

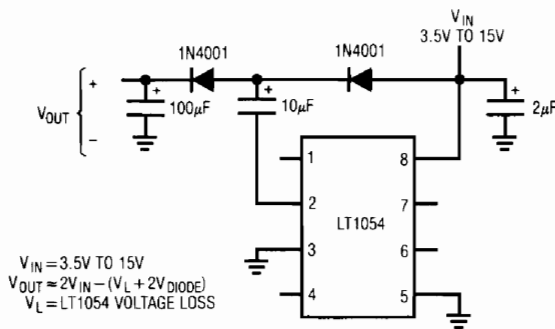


Figure 57. Voltage Boost Switched Capacitor Converter

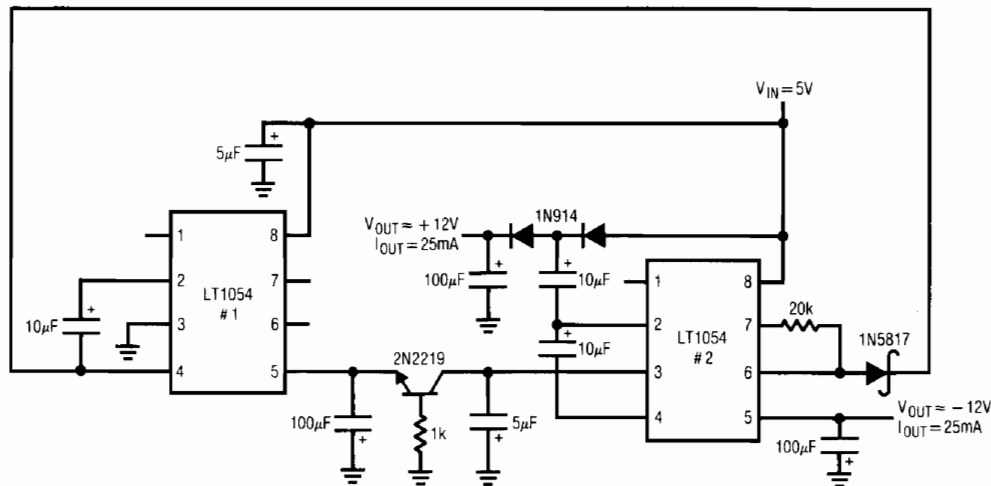


Figure 58. Switched Capacitor 5V to $\pm 12V$ Converter

the output to 5V by feedback controlling the turn-off point of the series phase. The circuit constitutes a large scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

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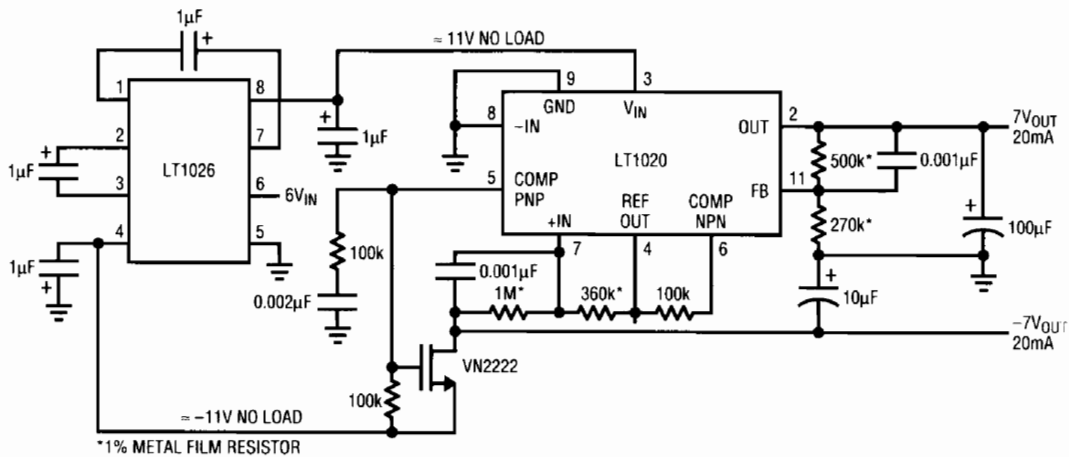


Figure 59. Switched Capacitor Based 6V to ±7V Converter

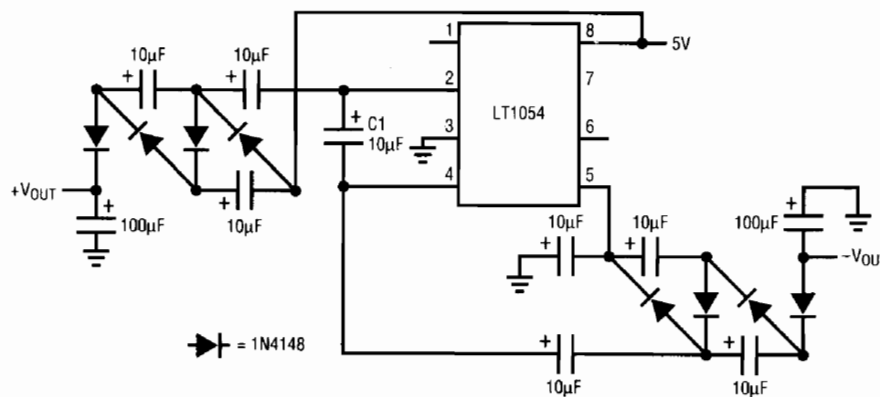


Figure 60. Switched Capacitor Charge Pump Based Voltage Multiplier

Application Note 29

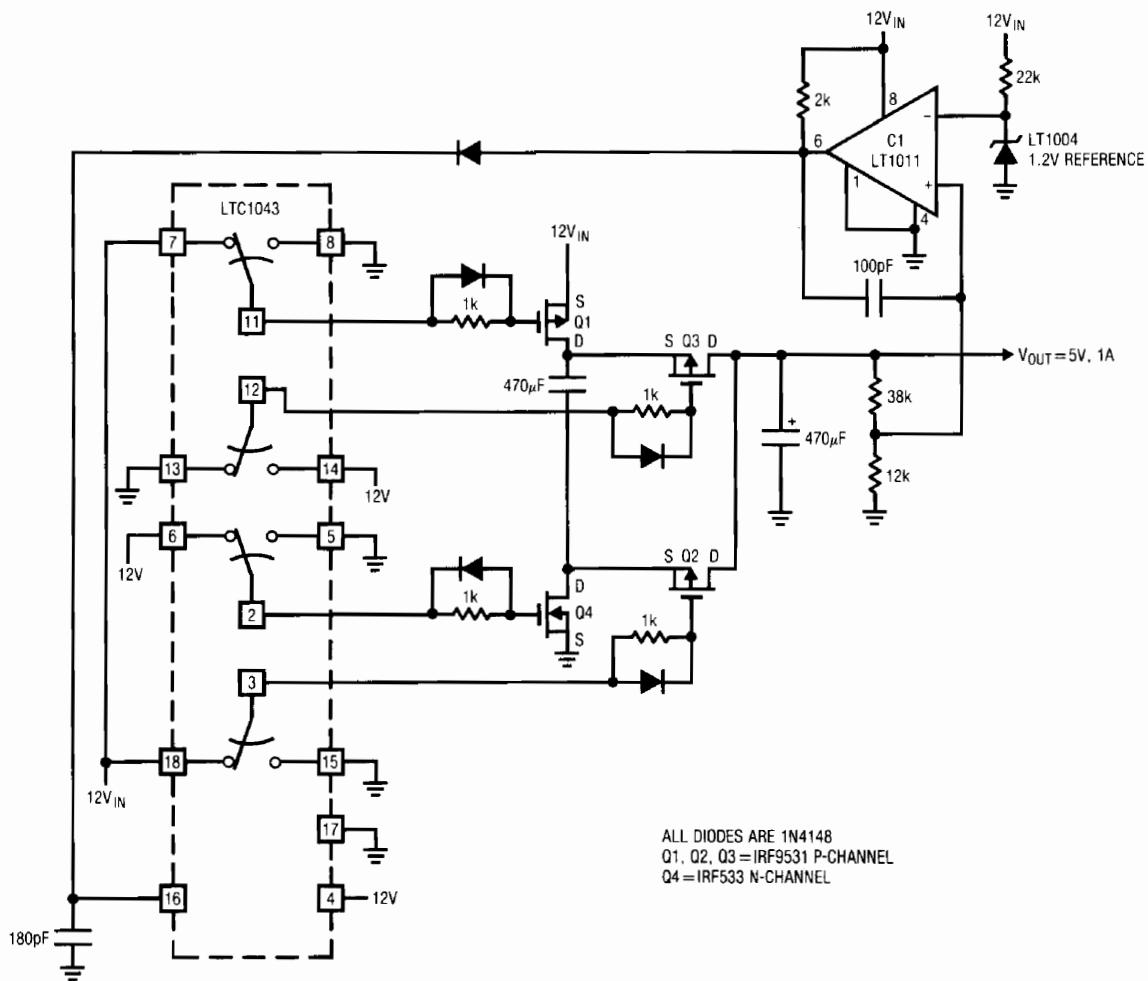


Figure 61. High Power Switched Capacitor Converter

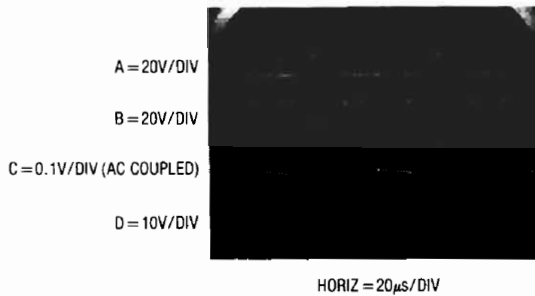


Figure 62. Waveforms for Figure 61

APPENDIX A

The 5V to $\pm 15V$ Converter — A Special Case

Five volt logic supplies have been standard since the introduction of DTL logic over twenty years ago. Preceding and during DTL's infancy the modular amplifier houses standardized on $\pm 15V$ rails. As such, popular early monolithic amplifiers also ran from $\pm 15V$ rails (additional historical perspective on amplifier power supplies appears in AN-11's appended section, "Linear Power Supplies—Past, Present, and Future"). The 5V supply offered process, speed and density advantages to digital IC's. The $\pm 15V$ rails provided a wide signal processing range to the analog components. These disparate needs defined power supply requirements for mixed analog-digital systems at 5V and $\pm 15V$. In systems with large analog component populations the $\pm 15V$ supply was and still is usually derived from the AC line. Such line derived $\pm 15V$ power becomes distinctly undesirable in predominantly digital systems. The inconvenience, difficulty and cost of distributing analog rails in heavily digital systems makes local generation attractive. 5V to $\pm 15V$ DC-DC converters were developed to fill this need and have been with us for about as long as 5V logic.

Figure A1 is a conceptual schematic of a typical converter. The 5V input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure A2, traces A and C are Q1's collector and base, while traces B and D are Q2's collector and base) each time the transformer saturates.[†] Transformer saturation causes a quickly rising, high current to flow (trace E). This current spike, picked up by the base drive winding, switches the transistors. Transformer current abruptly drops and then slowly rises until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%. The transformer's secondary is rectified, filtered and regulated to produce the outputs.

This configuration has a number of desirable features. The complementary high frequency (typically 20kHz) square wave drive makes efficient use of the transformer and allows relatively small filter capacitors. The self-oscillating primary drive tends to collapse under overload, providing desirable short circuit characteristics. The transistors switch in saturated mode, aiding efficiency. This hard switching, combined with the transformer's deliberate saturation does, however, have a drawback. During the saturation interval a significant, high frequency current

Note 1: This type of converter was originally described by Royer, et al. See References.

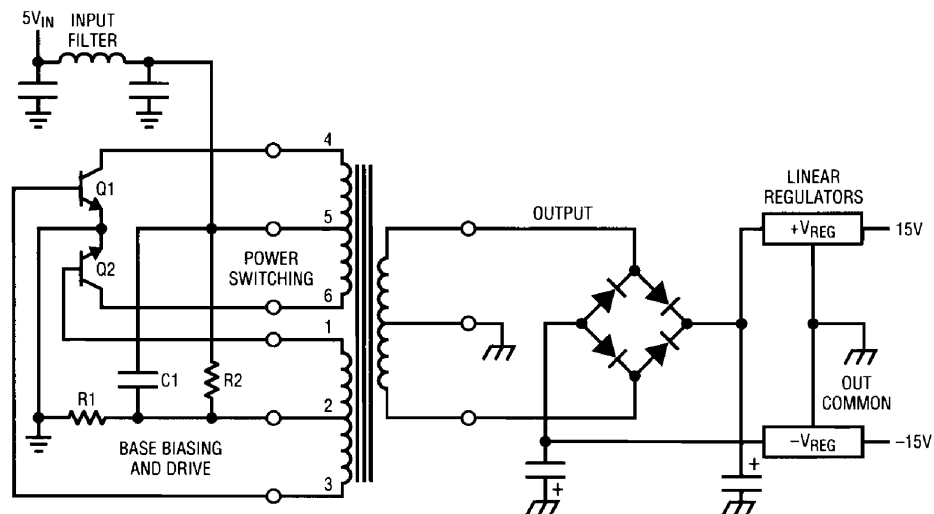


Figure A1. Conceptual Schematic of a Typical 5V to $\pm 15V$ Converter

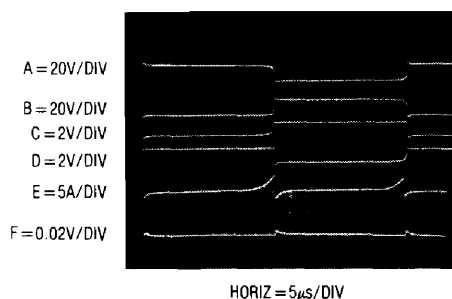


Figure A2. Typical 5V to $\pm 15V$ Saturating Converters Waveforms

spike is generated (again, trace E). This spike causes noise to appear at the converter outputs (trace F is the AC coupled 15V output). Additionally, it pulls significant current from the 5V supply. The converters input filter partially smooths the transient, but the 5V supply is usually so noisy the disturbance is acceptable. The spike at the output, typically 20mV high, is a more serious problem. Figure A3 is a time and amplitude expansion of Figure A2's traces B, E and F. It clearly shows the relationship between transformer current (trace B, Figure A3), transistor collector voltage (trace A, Figure A3) and the output spike (trace C, Figure A3). As transformer current rises the transistor starts coming out of saturation. When current rises high enough the circuit switches, causing the characteristic noise spike. This condition is exacerbated by the other transistors concurrent switching, causing both ends of the transformer to simultaneously conduct current to ground.

Selection of transistors, output filters and other techniques can reduce spike amplitude, but the converters inherent operation ensures noisy outputs.

This noisy operation can cause difficulties in precision analog systems. IC power supply rejection at the high harmonic spike frequency is low, and analog system errors frequently result. A 12-bit SAR A-to-D converter is a good candidate for such spike-noise caused problems. Sampled data IC's such as switched capacitor filters and chopper amplifiers often show apparent errors which are due to spike induced problems. "Simple" DC circuits can exhibit baffling "instabilities" which in reality are spike caused problems masquerading as DC shifts.

The drive scheme is also responsible for high quiescent current consumption. The base biasing always supplies

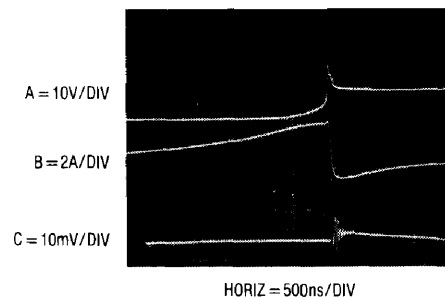


Figure A3. Switching Details of Saturating Converter

full drive, ensuring transistor saturation under heavy loading but wasting power at lighter loads. Adaptive bias schemes will mitigate this problem, but increase complexity and almost never appear in converters of this type.

The noise problem is, however, the main drawback of this approach to 5V to $\pm 15V$ conversion. Careful design, layout, filtering and shielding (for radiated noise) can reduce noise, but cannot eliminate it.

Some techniques can help these converters with the noise problem. Figure A4 uses a "bracket pulse" to warn the powered system when a noise pulse is about to occur. Ostensibly, noise sensitive operations are not carried out during the bracket pulse interval. The bracket pulse (trace A, Figure A5) drives a delayed pulse generator which triggers (trace B) the flip-flop. The flip-flop output biases the switching transistors (Q1 collector is trace C). The output noise spike (trace D) occurs within the bracket pulse interval. The clocked operation can also prevent transformer saturation, offering some additional noise reduction. This scheme works well, but presumes the powered system can tolerate periodic intervals where critical operations cannot take place.

In Figure A6 the electronic tables are turned. Here, the host system silences the converter when low noise is required. Traces B and C are base and collector drives for one transistor while traces D and E show drive to the other device. The collector peaking is characteristic of saturating converter operation. Output noise appears on trace F. Trace A's pulse gates off the converter's base bias, stopping switching. This occurs just past the 6th vertical division. With no switching, the output linear regulator sees the filter capacitor's pure DC and noise disappears.

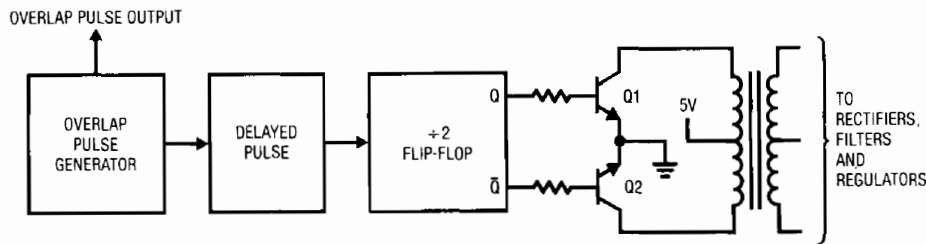


Figure A4. Overlap Generator Provides a “Bracket Pulse” Around Noise Spikes

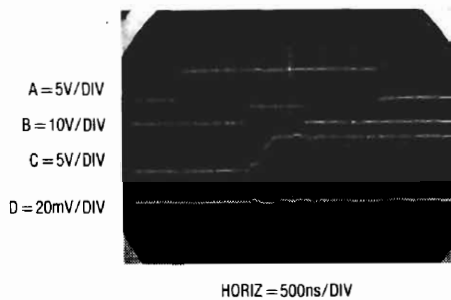


Figure A5. Waveforms for the Bracket Pulse Based Converter

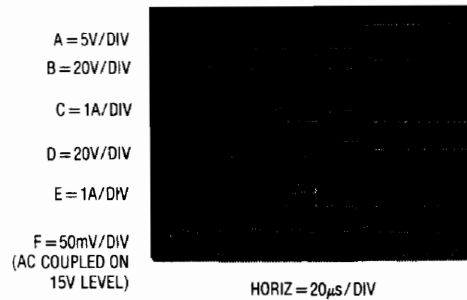


Figure A6. Detail of the Strobed Operation Converter

This arrangement also works nicely but assumes the control pulse can be conveniently generated by the system. It also requires larger filter capacitors to supply power during the low noise interval.

^{PN} Other methods involve clock synchronization, timing skewing and other schemes which prevent noise spikes from coinciding with sensitive operations. While useful, none of these arrangements offer the flexibility of the inherently noise free converters shown in the text.

APPENDIX B

Switched Capacitor Voltage Converters — How They Work

To understand the theory of operation of switched capacitor converters, a review of a basic switched capacitor building block is helpful.

In Figure B1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be Q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is Q2 = C1V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$Q = Q1 - Q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times Q = f \times C1 (V1 - V2)$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

Application Note 29

A new variable, R_{EQUIV} , is defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure B2. The LT1054 and other switched capacitor converters have the same switching action as the basic switched capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency. As frequency is decreased, the output impedance will eventually be dominated by the $1/fC1$ term and voltage losses will rise.

Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillators of practical converters are designed to run in the frequency band where voltage losses are at a mini-

imum. Figure B3 shows the block diagram of the LT1054 switched capacitor converter.

The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. It provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5mA.

The LT1054 also provides regulation. By adding an external resistive divider, a regulated output can be obtained. This output will be regulated against changes in input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shutdown is less than $100\mu A$.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

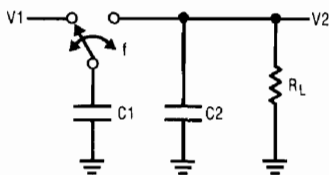


Figure B1. Switched Capacitor Building Block

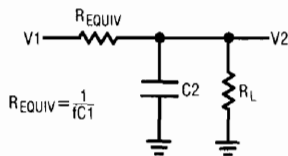


Figure B2. Switched Capacitor Equivalent Circuit

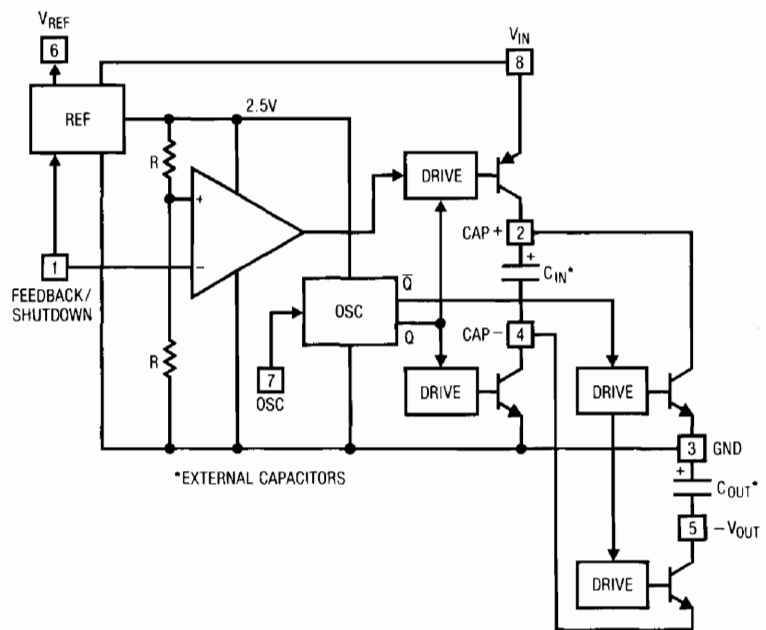


Figure B3. LT1054 Switched Capacitor Converter Block Diagram

APPENDIX C

Physiology of the LT1070

The LT1070 is a current-mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to Figure C1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output

overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs

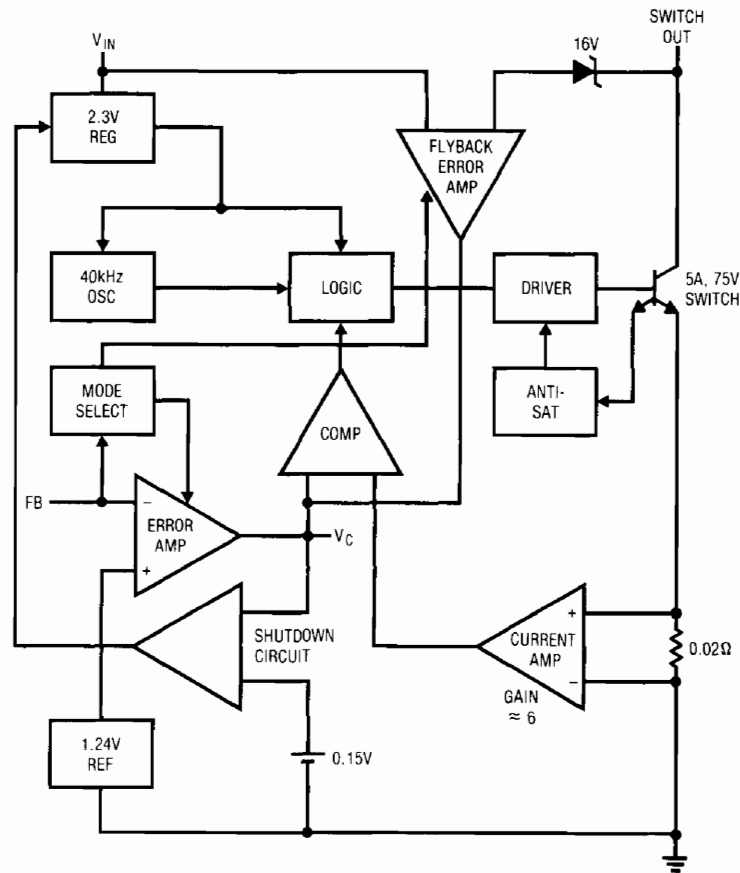


Figure C1. LT1070 Internal Details

Application Note 29

the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50 μ A supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

APPENDIX D

Inductor Selection for Flyback Converters

A common problem area in DC-DC converter design is the inductor, and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to address inductor selection. It permits real time analysis under actual circuit operating conditions using the ultimate simulator — a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure D1 shows a typical flyback based converter utilizing the LT1070 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit¹ shown in Figure D2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure D1.

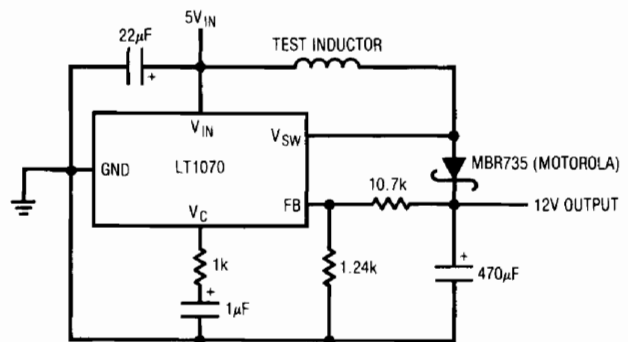


Figure D1. Basic LT1070 Flyback Converter Test Circuit

¹ Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, 619-268-2400

Figure D3 was taken with a $450\mu\text{H}$ value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1070's V_{SW} pin voltage while trace B shows its current. When V_{SW} pin voltage is low, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure D4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure D5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure D6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

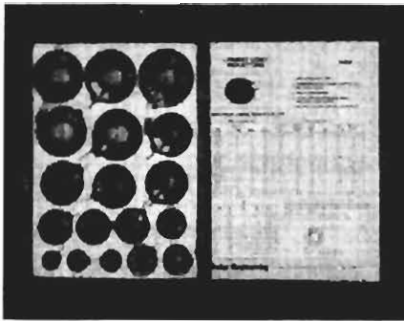


Figure D2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. (Includes 18 Fully Specified Devices)

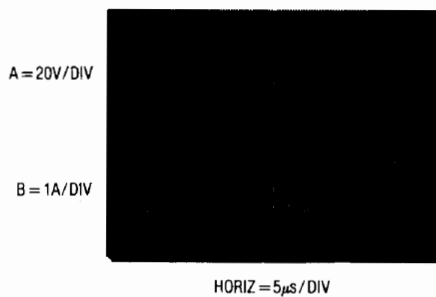


Figure D3. Waveforms for $450\mu\text{H}$, High Capacity Core Unit

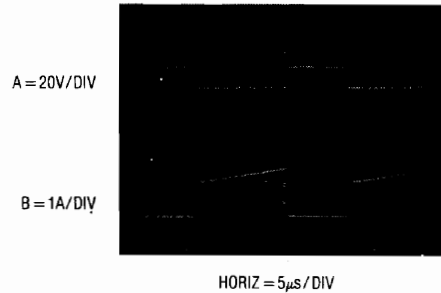


Figure D4. Waveforms for $170\mu\text{H}$, High Capacity Core Unit

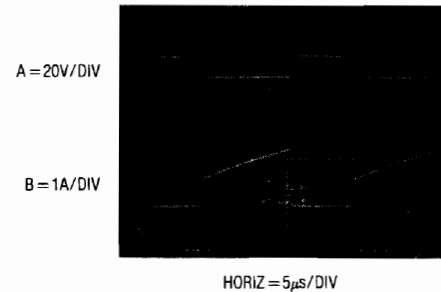


Figure D5. Waveforms for $55\mu\text{H}$, High Capacity Core Unit

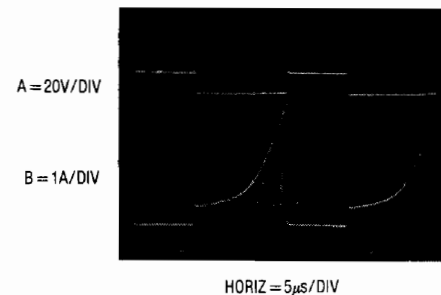


Figure D6. Waveforms for $500\mu\text{H}$, Low Capacity Core Inductor (Note Saturation Effects)

APPENDIX E

Optimizing Converters for Efficiency

Squeezing the utmost efficiency out of a converter is a complex, demanding design task. Efficiency exceeding 80–85% requires some combination of finesse, witchcraft and just plain luck. Interaction of electrical and magnetic terms produces subtle effects which influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency is not readily described but some guidelines are possible.

Losses fall into several loose categories including junction, ohmic, drive, switching, and magnetic losses.

Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low voltage output converters. A 700mV drop in a 5V output converter introduces more than 10% loss. Schottky devices will cut this nearly in half, but loss is still appreciable. Germanium (rarely used) is lower still, but switching losses negate the low DC drop at high speeds. In very low power converters Germanium's reverse leakage may be equally oppressive. Synchronously switched rectification is more complex, but can sometimes simulate a more efficient diode (see text Figure 32). When evaluating such a scheme remember to include both AC and DC drive losses in efficiency estimates. DC losses include base or gate current in addition to DC consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation (the switch spends some time in its linear region) and power lost due to timing skew between drive and actual switch action.

Transistor saturation losses are also a significant term. Channel and collector-emitter saturation losses become increasingly significant as operating voltages decrease. The most obvious way to minimize these losses is to select low saturation components. In some cases this will work, but remember to include the drive losses (usually higher) for lower saturation devices in overall loss estimates. Actual losses caused by saturation effects and diode drops is sometimes difficult to ascertain. Changing duty cycles and time variant currents make determination tricky. One simple way to make relative loss judgements is to measure device temperature rise. Appropriate tools

here include thermal probes and (at low voltages) the perhaps more readily available human finger. At lower power (e.g., less dissipation, even though loss percentage may be as great) this technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting efficiency change allows loss determination.

Ohmic losses in conductors are usually only significant at higher currents. "Hidden" ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally drops with capacitor value and rises with operating frequency, and should be specified on the capacitor data sheet. Consider the copper resistance of inductive components. It is often necessary to evaluate trade-offs of an inductor's copper resistance vs magnetic characteristics.

Drive losses were mentioned, and are important in obtaining efficiency. MOSFET gate capacitance draws substantial AC drive current per cycle, implying higher average currents as frequency goes up. Bipolar devices have lower capacitance, but DC base current eats power. Large area devices may appear attractive for low saturation, but evaluate drive losses carefully. Usually, large area devices only make sense when operating at a significant percentage of rated current. Drive stages should be thought out with respect to efficiency. Class A type drives (e.g., resistive pull-up or pull-down) are simple and fast, but wasteful. Efficient operation usually requires active source-sink combinations with minimal cross conduction and biasing losses.

Switching losses occur when devices spend significant amounts of time in their linear region relative to operating frequency. At higher repetition rates transition times can become a substantial loss source. Device selection and drive techniques can minimize these losses.

Magnetics design also influences efficiency. Design of inductive components is well beyond the scope of this appended section, but issues include core material selection, wire type, winding techniques, size, operating frequency, current levels, temperature and other issues.

Some of these topics are discussed in LTC Application Note AN-19, but there is no substitute for access to a skilled magnetics specialist. Fortunately, the other categories mentioned usually dominate losses, allowing good

efficiencies to be obtained with standard magnetics. Custom magnetics are usually only employed after circuit losses have been reduced to lowest practical levels.

APPENDIX F

Instrumentation for Converter Design

Instrumentation for DC-DC converter design should be selected on the basis of *flexibility*. Wide bandwidths, high resolution and computational sophistication are valuable features, but are usually not required for converter work. Typically, converter design requires simultaneous observation of many circuit events at relatively slow speeds. Single ended and differential voltage and current signals are of interest, with some measurements requiring fully floating inputs. Most low level measurement involves AC signals and is accommodated with a high sensitivity plug-in. Other situations call for observation of small, slowly changing (e.g., 0.1Hz to 10Hz) events on top of DC levels. This range falls outside the AC coupled cut-off of most oscilloscopes, mandating differential DC nulling or "slide-back" plug-in capability. Other requirements include high impedance probes, filters and oscilloscopes with very versatile triggering and multi-trace capability. In our converter work we have found a number of particularly noteworthy instruments in several categories.

PROBES

For many measurements standard 1x and 10x scope probes are fine. In most cases the ground strap may be used, but low level measurements, particularly in the presence of wideband converter switching noise, should be taken with the shortest possible ground return. A variety of probe tip grounding accessories are available, and are usually supplied with good quality probes (see Figure F1). In some cases, directly connecting the breadboard to the 'scope may be necessary (Figure F2).

Wideband FET probes are not normally needed, but a moderate speed, high input impedance buffer probe is quite useful. Many converter circuits, especially micropower designs, require monitoring of high impedance nodes. The 10M Ω loading of standard 10x probes usually suffices, but sensitivity is traded away. 1x probes retain

sensitivity, but introduce heavier loading. Figure F3 shows an almost absurdly simple, but useful, circuit which greatly aids probe loading problems. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows cable and probe driving and also biases the circuit's input shield. This bootstraps the input capacitance, reducing its effect. DC and AC errors of this circuit are low enough for almost all converter work, with enough bandwidth for most circuits. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.

Figure F4 shows a simple probe filter which sets high and low bandwidth restrictions. This circuit, placed in series with the 'scope input, is useful for eliminating switching artifacts when observing circuit nodes.

An *isolated* probe allows fully floating measurements, even in the presence of high common mode voltages. It is often desirable to look across floating points in a circuit. The ability to directly observe an ungrounded transistor's saturation characteristics or monitor waveforms across a floating shunt makes this probe valuable. One probe, the Signal Acquisition Technologies, Inc. Model SL-10, has 10MHz bandwidth and 600V common mode capability.

Current probes are an indispensable tool in converter design. In many cases current waveforms contain more valuable information than voltage measurements. The clip-on types are quite convenient. Hall effect based versions respond down to DC, with bandwidths of 50MHz. Transformer types are faster, but roll off below several hundred cycles (Figure F5). Both types have saturation limitations which, when exceeded, cause odd results on the CRT, confusing the unwary. The Tektronix P6042 (and the more recent AM503) Hall type and P6022/134 transformer based type give excellent results. The Hewlett-Packard 428B

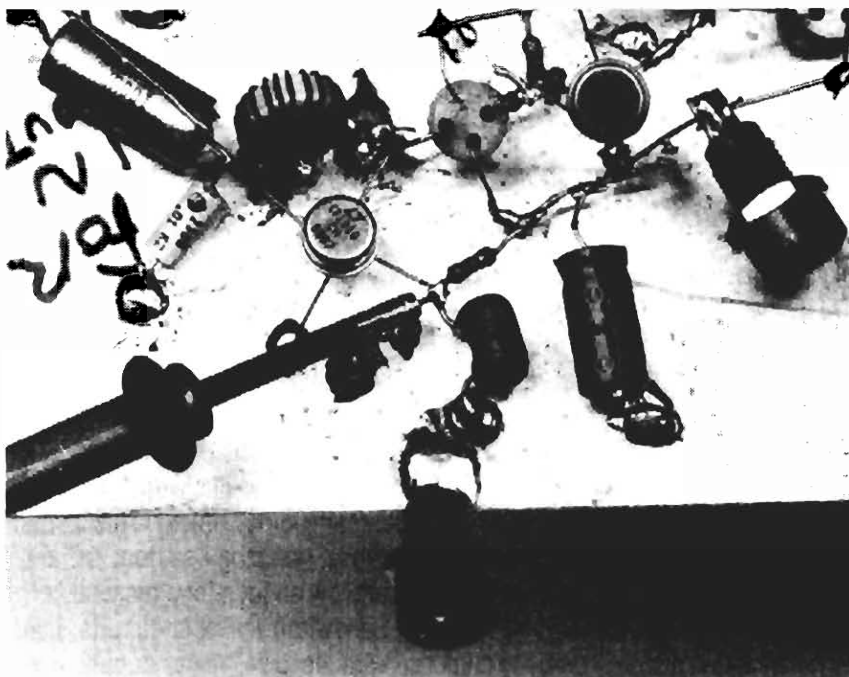


Figure F1. Proper Probing Technique for Low Level Measurements in the Presence of High Frequency Noise

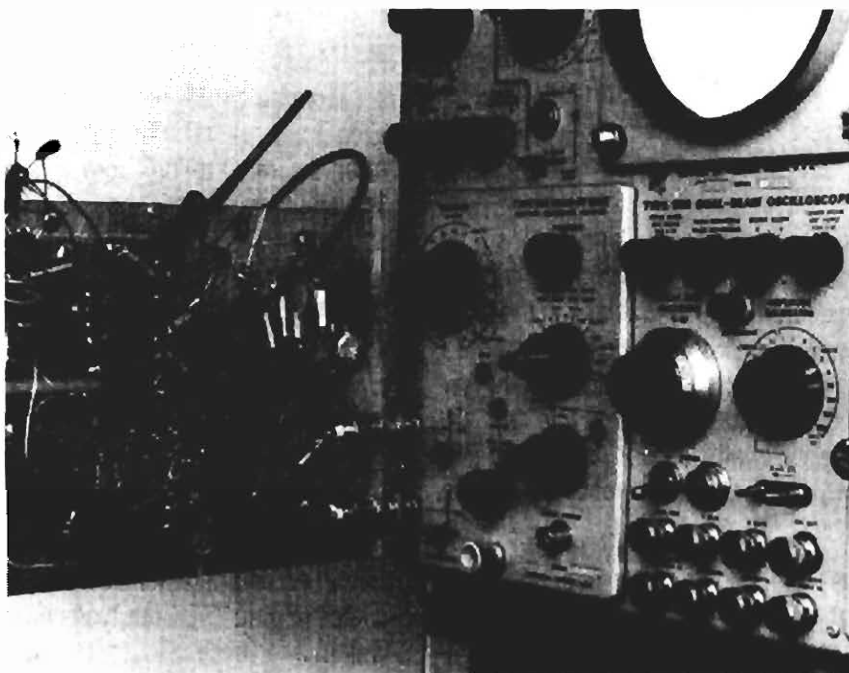


Figure F2. Direct Connections to the Oscilloscope Give Best Low Level Measurements. Note Ground Reference Connection to the Differential Plug-In's Negative Input.

clip-on current probe responds from DC to only 400Hz, but features 3% accuracy over a 100 μ A to 10A range. This instrument, useful for determining efficiency and quiescent current, eliminates shunt caused measurement errors.

OSCILLOSCOPES AND PLUG-INS

The oscilloscope plug-in combination is an important choice. Converter work almost demands multi-trace capability. Two channels are barely adequate, with four far preferable. The Tektronix 2445/6 offers four channels, but two have limited vertical capability. The Tektronix 547 (and

the more modern 7603), equipped with a type 1A4 (2 dual trace 7A18's required for the 7603) plug-in, has four full capability input channels with flexible triggering and superb CRT trace clarity. This instrument, or its equivalent, will handle a wide variety of converter circuits with minimal restrictions. The Tektronix 556 offers an extraordinary array of features valuable in converter work. This dual beam instrument is essentially two fully independent oscilloscopes sharing a single CRT. Independent vertical, horizontal and triggering permit detailed display of almost any converters operation. Equipped with two type 1A4

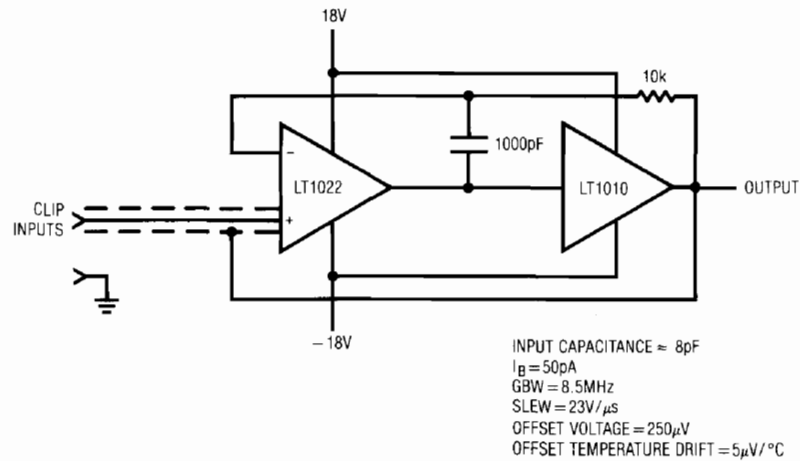


Figure F3. A Simple High Impedance Probe

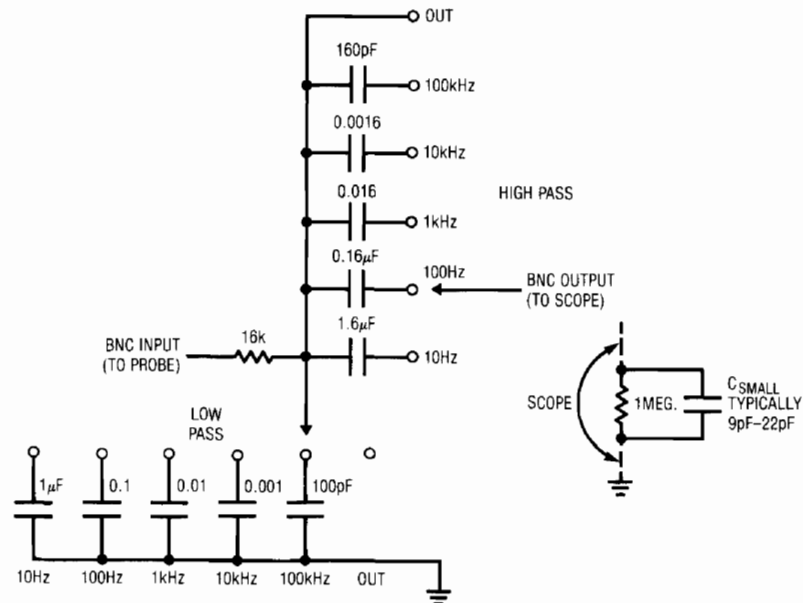


Figure F4. Oscilloscope Filter

Application Note 29

plug-in's, the 556 will display eight real time inputs. The independent triggering and time bases allow stable display of asynchronous events. Cross beam triggering is also available, and the CRT has exceptional trace clarity.

Two oscilloscope plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7 and 7A22 feature $10\mu\text{V}$

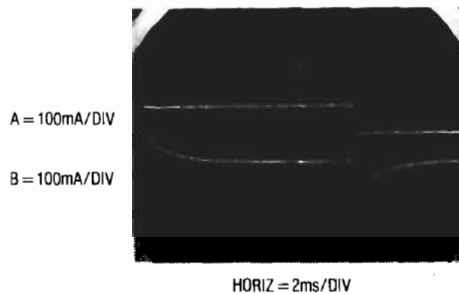


Figure F5. Hall (Trace A) and Transformer (Trace B) Based Current Probes Responding to Low Frequency

sensitivity, although bandwidth is limited to 1MHz. The units also have selectable high and low pass filters and good high frequency common mode rejection. Tektronix types W, 1A5 and 7A13 are differential comparators. They have calibrated DC nulling ("slideback") sources, allowing observation of small, slowly moving events on top of common mode DC.

VOLTMETERS

Almost any DVM will suffice for converter work. It should have current measurement ranges and provision for battery operation. The battery operation allows floating measurements and eliminates possible ground loop errors. Additionally, a *non-electronic* (VOM) voltmeter (e.g., Simpson 260, Triplett 630) is a worthwhile addition to the converter design bench. Electronic voltmeters are occasionally disturbed by converter noise, producing erratic readings. A VOM contains no active circuitry, making it less susceptible to such effects.

APPENDIX G

The Magnetics Issue

Magnetics is probably the most formidable issue in converter design. Design and construction of suitable magnetics is a difficult task, particularly for the non-specialist. It is our experience that the majority of converter design problems are associated with magnetics requirements. This consideration is accentuated by the fact that most converters are employed by non-specialists. As a purveyor of



Figure G1. Magnetics for LTC Applications Circuits are Designed and Supplied as Standard Product by Pulse Engineering, Inc.

switching power IC's we incur responsibility towards addressing the magnetics issue (our publicly spirited attitude is, admittedly, capitalistically influenced). As such, it is LTC's policy to use off-the-shelf magnetics in our circuits. In some cases, available magnetics serve a particular design. In other situations the magnetics have been specially designed, assigned a part number and made available as standard product. In these endeavors our magnetics supplier and partner is;

Pulse Engineering, inc.
P.O. Box 12235
7250 Convoy Court
San Diego, California 92112
619-268-2400

In many circumstances a standard product is suitable for production. Other cases may require modifications or changes which Pulse Engineering can provide. Hopefully, this approach serves the needs of all concerned.

Linear Circuits for Digital Systems

Some Affable Analogs for Digital Devotees

Jim Williams

The pristine, regimented symmetry of digital circuit boards is occasionally interrupted by an irregular huddle of linear components. These aberrants are tolerated because they perform a variety of ancillary tasks necessary to keep the digital system running. While I certainly wouldn't wish lifetime employment on a digital circuit board to anyone*, the reality is that the need exists. Power control, clock circuits and memory management are areas where linear circuits are needed in digital systems. Recently introduced flash memories offer a good example of linear circuits supporting a predominantly digital function. Flash memory adds electrical chip-erase and reprogramming to conventional EPROM capability. A full chip erasure takes 1 second with 100 μ s byte-program times and 4 seconds for full chip programming. These features make flash memories an attractive non-volatile memory option. Additional information on these devices appears in Appendix A, "A Primer on Flash Memory," guest written by Saul Zales of Intel Corporation.

These devices require carefully controlled, high voltage programming power. A typical unit, the Intel 28F010 1 megabit flash memory, specifies V_{PP} ($V_{PROGRAM POWER}$) pulses of $12V \pm 0.6V$ or $12.75V \pm 0.2V$, depending on part type. V_{PP} excursions beyond 14V (for 20ns or longer) will destroy the ETOX[†] process based device. Reliably generating such pulses in a 5V powered digital system involves several analog issues. High voltage must be derived and controlled within the tight tolerances noted (see Appendix B for an expanded discussion of this topic). Additionally, it is desirable to control the high voltage pulses from a 5V logic command.

Basic Flash Memory Programming Voltage Supply

Figure 1's circuit meets almost all flash memory V_{PP} requirements. When the V_{PP} command goes low (Trace A, Figure 2) the LT1072** switching regulator drives L1, producing high voltage. DC feedback occurs via R1 and R2,

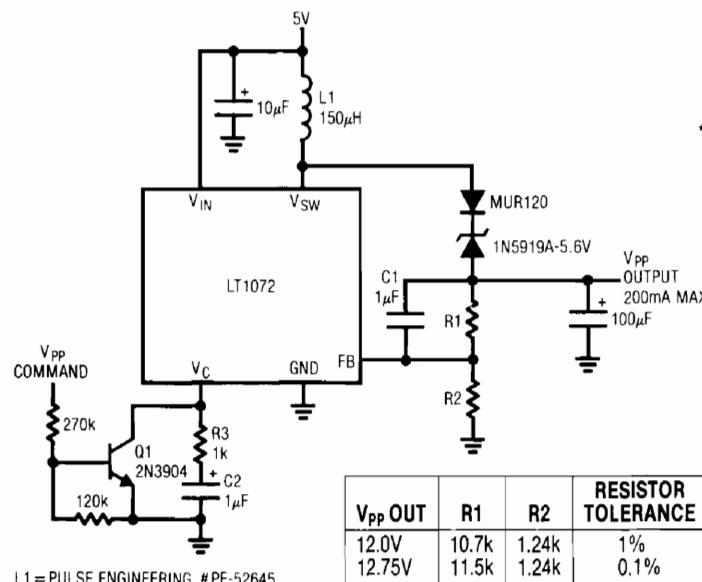


Figure 1. Basic Flash Memory V_{PP} Programming Voltage Supply

*I suppose it's not all that bad. Some of my best friends are digital circuits. If I had a daughter, I'd even consider letting her go out with one.

[†]ETOX is a trademark of Intel Corporation.

**See Appendix C and References for detailed information on the LT1072.

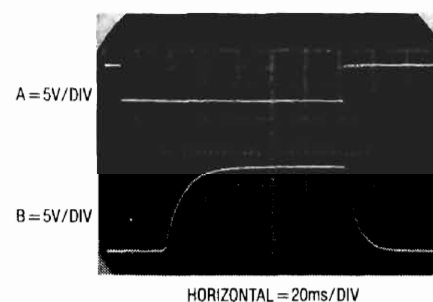


Figure 2. Waveforms for Basic Flash Programming Supply

Application Note 31

with AC roll-off controlled by C1 and R3-C2. The result is a smoothly rising V_{pp} (Trace B) which settles to the required value. The specified R1 values allow either 12.0V or 12.75V outputs. The 5.6V zener permits the output to return to 0V when the V_{pp} command goes high. It may be deleted in cases where a 4.5V minimum output is acceptable or desirable (see Intel 28F010 datasheet). Precision resistors combine with the LT1072's tight internal reference to eliminate circuit trimming requirements. Alternately, 1% resistors and a trimmer may be used. Additionally, this circuit will not spuriously overshoot during power-up or down, preventing memory destruction. Figure 3's table details circuit changes permitting higher power outputs. Figure 3's table details circuit changes permitting higher power outputs. The synchronous switch option can be used to eliminate the zener and its attendant power dissipation.

High Repetition Rate V_{pp} Programming Supplies

Figure 1's repetition rate is limited because the regulator must fully rise and settle for each V_{pp} command. Figure 4's circuit serves special cases which require higher repetition rate. Here, the switching regulator runs continuously, with the V_{pp} generated by the A1-A2 loop. If desired, the V_{pp} lock line can be driven, shutting down the regulator to preclude any possibility of inadvertent V_{pp} outputs. When V_{pp} lock goes low (Trace A, Figure 5) the LT1072 loop

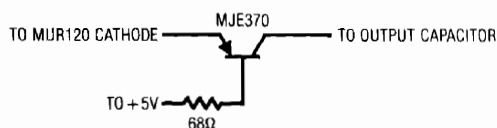


Figure 3. Synchronous Switch Option

Power Options for Basic V_{pp} Pulse Generator

OUTPUT CURRENT	C_{OUT}	REGULATOR	INDUCTOR	ZENER
400mA	200 μ F	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800mA	400 μ F	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note: Assume each 28F010 device requires 30mA of V_{pp} current.

comes on (Trace B), stabilizing at about 17V. 2 pole compensation ensures a clean rise time. Pulling the V_{pp} command line low causes the 74C04 (Trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V with A1 and A2 giving a scaled output (Trace D). The 680pF capacitor controls loop slewing, eliminating overshoots. Figure 6 details the V_{pp} output. Trace A is the 74C04 output, with Trace B showing clean V_{pp} characteristics.

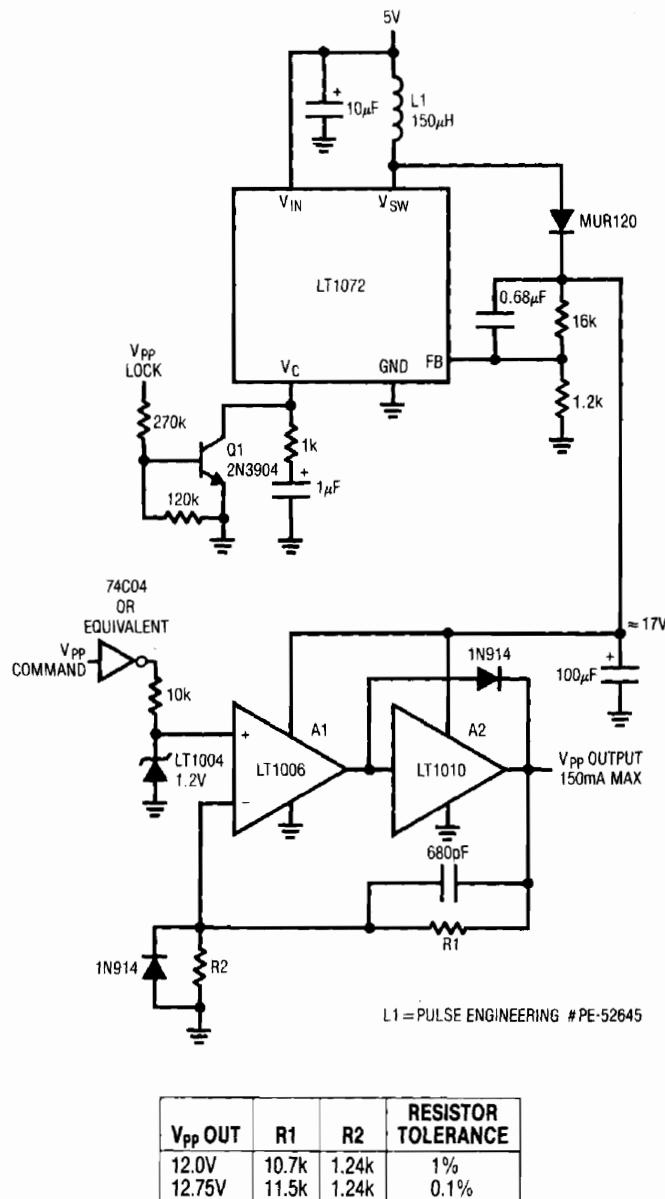


Figure 4. High Repetition Rate V_{pp} Programming Supply

As in Figure 1, spurious V_{pp} outputs are suppressed during power-up or down. The LT1010 provides 150mA drive (5 28F010's) and short circuit protection. The diode path around the LT1010 prevents destructive overshoot when the circuit is recovering from output shorts. The diode at A1's input clips excessive negative voltages due to the 680pF unit's differentiated response. Figure 7's circuit is similar to Figure 4's, except that the LT1010 has been replaced with a discrete power output stage, Q2-Q3. Q3 furnishes up to 800mA (26 28F010 memories), with Q2 used for current limiting. The feedback values have been increased, preventing Q2's collector current from causing excessive heating in the grounded resistor. This could occur during prolonged short circuit conditons. The feedback capacitor is re-established accordingly. The circuit's AC dynamics, including a glitchless short circuit recovery, are identical to Figure 4.

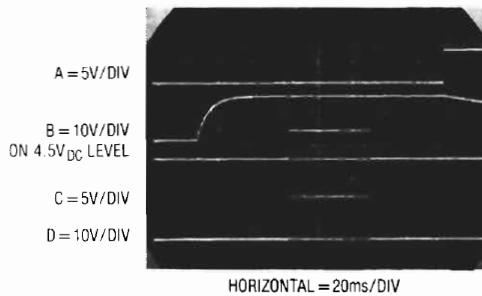


Figure 5. Operating Details of High Repetition Rate Flash Memory Programming Supply

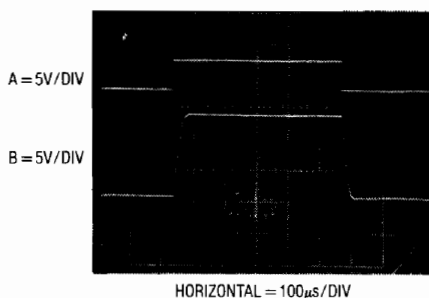
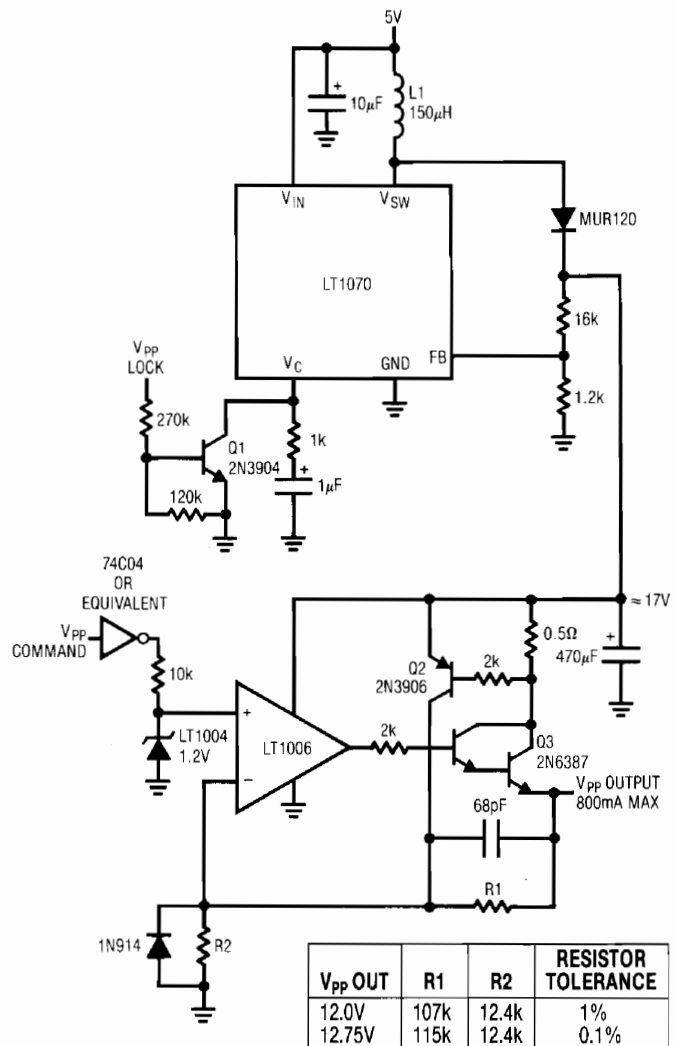


Figure 6. Expanded Scale Display of Figure 4's V_{pp} Output. Controlled Rise Time Eliminates Overshoots

In some systems high voltage is already available. In such cases the LT1070/72 circuitry may be deleted from Figures 4 and 7.

A good question might be: "Why not set the switching regulator output voltage at the desired V_{pp} level and use a simple low resistance FET or bipolar switch?". In theory, this approach will work. In practice, transmission line effects in printed circuit trace runs may cause memory destroying overshoots. Appendix B, "Preventing Memory Destruction," details this phenomenon.



L1 = PULSE ENGINEERING # PE-51516

Figure 7. High Power, High Repetition Rate V_{pp} Pulse Generator

Application Note 31

V_{pp} Handshake Circuit

Both V_{pp} circuits shown require a small waiting period for the regulator to settle before proceeding with a V_{pp} operation. In almost all circumstances this is acceptable, but some situations may require verification that V_{pp} is within tolerance before pulsing begins. Figure 8's circuit, used in conjunction with either V_{pp} circuit, gives a handshake output when V_{pp} has settled. This simple circuit works by comparing the V_{pp} output against the known LT1004 reference voltage. The resistor values given allow for possible variations in V_{pp} voltage due to component tolerance stack-up. When this circuit is in use, the output of the V_{pp} generator circuit should be set within 0.4% of nominal value. This can be done by trimming, or using 0.05% resistors in place of the 0.1% units specified.

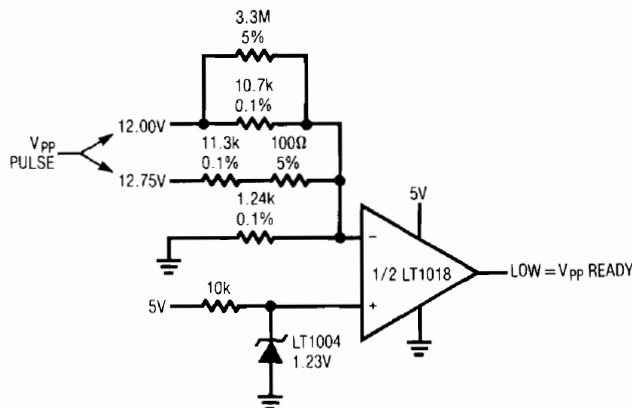


Figure 8. V_{pp} Handshake Circuit

EEPROM V_{pp} Pulse Generator

EEPROMs do not offer the advantages of flash memories, but are sometimes used. Their V_{pp} pulse requirements have commonalities with flash types. The 2816 specifies 21V ± 1V V_{pp} amplitude with a maximum allowable voltage of 22.5. A special EEPROM stipulation is that the V_{pp} pulse must have a 600μs rise time. Figure 9's circuit meets these requirements. The LT1072 generates the high voltage while A1 and A2 form the actual V_{pp} pulse. With the

Erase/Write lock line low (Trace A, Figure 10), the LT1072 is in standby; no high voltage is produced and there is no circuit activity. Under these conditions the V_{pp} output line is pulled towards +5V via the 1N914 diode (see 2816 data-sheet for details). When the Erase/Write lock line (Trace A, Figure 10) goes high, the regulator output (Trace C) builds smoothly and regulates at 25V. The 2 pole LT1072 compensation allows the regulator output to rise relatively quickly. When the V_{pp} command line (Trace B) is pulsed high, the LT1004 reference clamps at 1.23V and the RC network delivers a 600μs edge to A1's input. A1 combines with power buffer A2 and the feedback resistors to produce a 21V pulse at the V_{pp} output (Trace D). Trace E is a time and amplitude expanded version of this pulse. The 600μs RC rise time condition is met, with the 21V amplitude assured by the LT1004 reference and closed loop operation. When the V_{pp} command goes low, the V_{pp} output returns cleanly to 4.5 V. The diode path speeds recovery of the 0.005μF capacitor at A1's input. A2 provides a 150mA (ten 2816 EEPROMs) output with short circuit protection. As in Figure 4, a diode path around the LT1010 prevents overshoot when the circuit is recovering from output shorts. When the Erase/Write lock line returns low, the regulator output decays towards zero. As with the other V_{pp} circuits, this design does not produce undesired outputs during power-up or down.

5V Powered 4–20mA Current Loop Generator

Figure 11's circuit also employs voltage step-up, but for a different purpose. Transmission of industry standard 4–20mA current loop signals to valves and other actuators is a common requirement. Resistive line losses and actuator impedances require current transmitters to be able to force a compliance voltage of at least 20V. Because of this, 5V powered systems usually cannot meet current loop transmitter requirements, but Figure 11 shows a way to do this. This 5V powered circuit utilizes a servo controlled DC-DC converter to generate the compliance voltage necessary for loop current requirements. It will drive 4–20mA into loads as high as 2200Ω (44V compliance) and is inherently short circuit protected. Its digital inputs permit easy interface to digital systems.

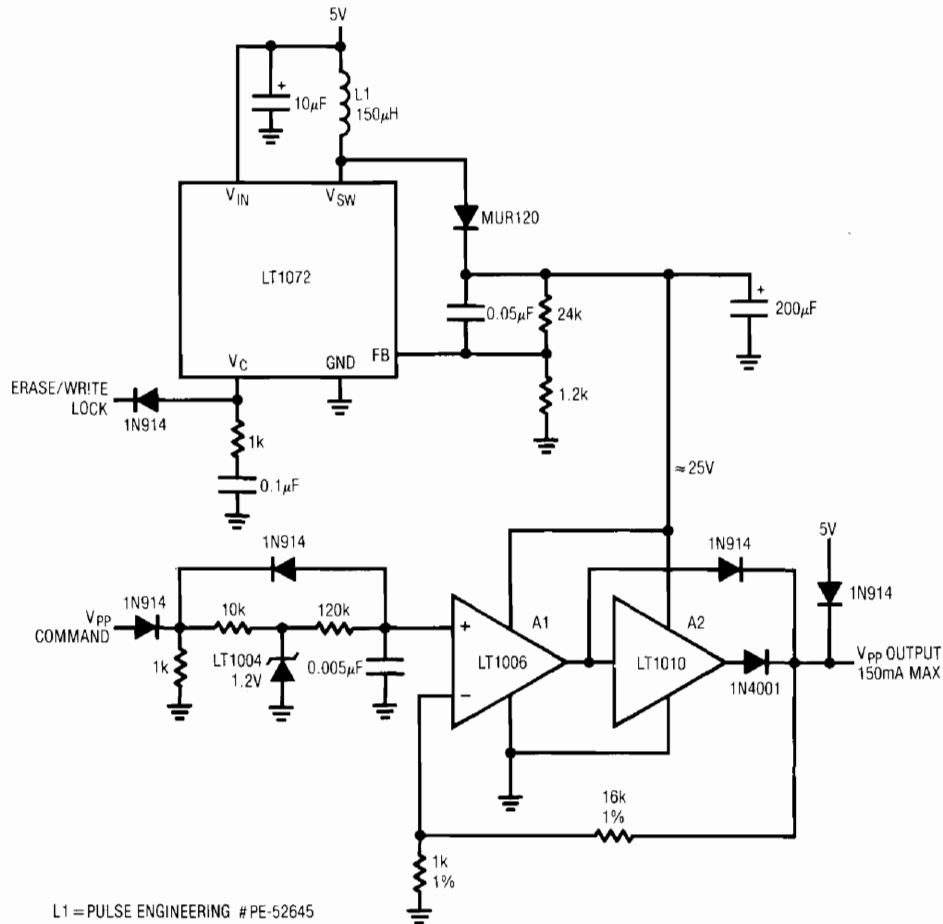


Figure 9. EEPROM V_{pp} Pulse Generator

The AD558 8 bit D→A converter receives the circuit's digital inputs, producing a 2.56V full-scale output. A1's positive input voltage is determined by the D→A output and the 4mA trim network output. A1's output biases the LT1072's V_C pin. This forces the switching regulator to run at the output voltage necessary to balance A1's inputs. The feedback path for this action is through the load, across the 75Ω resistor and back to A1's negative input. The 240Ω-0.05µF combination stabilizes the loop. The 7.5V zener permits regulator output down to 0V. The resistors connected to the LT1072's feedback (FB) pin prevent circuit output from running away in the event the load opens up. Normally, A1 controls the loop, forcing the LT1072 to produce the voltage required to maintain the D→A directed current through the load. If the load opens, A1 receives no feedback, but the FB pin becomes active at 1.2V, forc-

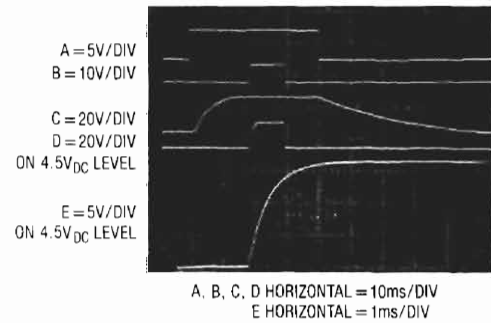


Figure 10. EEPROM Pulse Generator Waveforms

ing the loop to close locally around the LT1072. In this fashion the circuit automatically crosses over from a current to a voltage regulator, preventing excessive output voltages from occurring.

Application Note 31

Figure 12 details LT1072 operation under normal conditions. Trace A is V_{SWITCH} pin voltage, while Trace B indicates its current. Trace C, the MUR120 diode current, clearly shows the switched packets of energy delivered to the $22\mu\text{F}$ output capacitor. The resultant output ripple voltage (Trace D) measures only 25mV at the load.

Figure 13 catches circuit output at the instant a load open has occurred. Normal current mode operation ceases just past the third vertical division. The “+” output line heads positive until the LT1072 FB pin rises to 1.2V. At this point (just past the 6th vertical division), the LT1072’s internal feedback amplifier activates, causing local loop closure and regulating the output at about 57V. The non-linear slew characteristic is due to A1’s feedback capacitor re-

strained response. Once A1’s output rails, slew increases to a limit imposed by L1, the $22\mu\text{F}$ output capacitor and the LT1072’s 40kHz switching rate.

To trim this circuit, connect any load below $2\text{k}\Omega$ and set all DAC bits low. Adjust the 4mA trim for 0.300V across the 75Ω resistor. Next, put all DAC bits high and set the 20mA trim for 1.500V across the 75Ω resistor. Repeat this procedure until both points are fixed.

AC Line Dropout Detector

Digital systems driven from the AC line often require power dropout detection. Fast AC line dropout detection allows a memory store command to be issued before DC

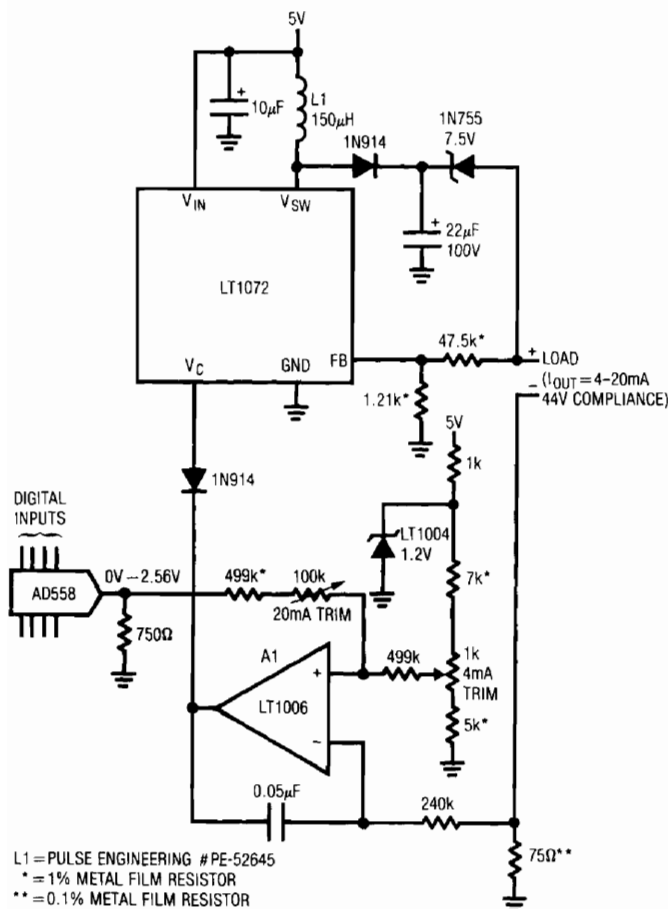


Figure 11. 5V Powered, Digitally Controlled 4-20mA Current Loop Generator



Figure 12. Figure 11's Waveforms

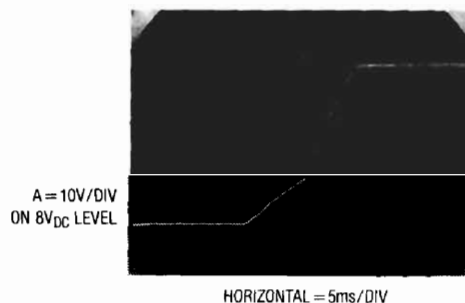


Figure 13. Open Load Characteristics for Figure 11's Current Source. LT1072 Crosses over into Constant Voltage Mode at 57V

power falls. Figure 14's circuit detects AC dropout by connecting an optoisolator across the power transformer's rectified secondary. Normally, the AC line (Trace A, Figure 15) turns on the LED every 8ms (1/2 cycle of the line), causing the output transistor to reset the 0.01 μ F capacitor (Trace B). When the line drops out, the capacitor charges via the 33k resistor. The resultant ramp voltage is compared by C1A to a +5V supply derived reference. In this case, the 2k-3k resistors bias C1A to go low (Trace C) within one cycle of AC line dropout. Typically, the DC regulator will supply 50ms-100ms of hold-up before it begins to sag.

This hold-up period, which should be verified in any individual application, permits adequate time to execute a memory store operation. C1B serves as a final warning that power failure is imminent. It goes low when the 5V regulator input drops below the threshold set by the selected resistor shown on the schematic. This value should be chosen so that C1B trips when the regulator input approaches its specified dropout voltage.

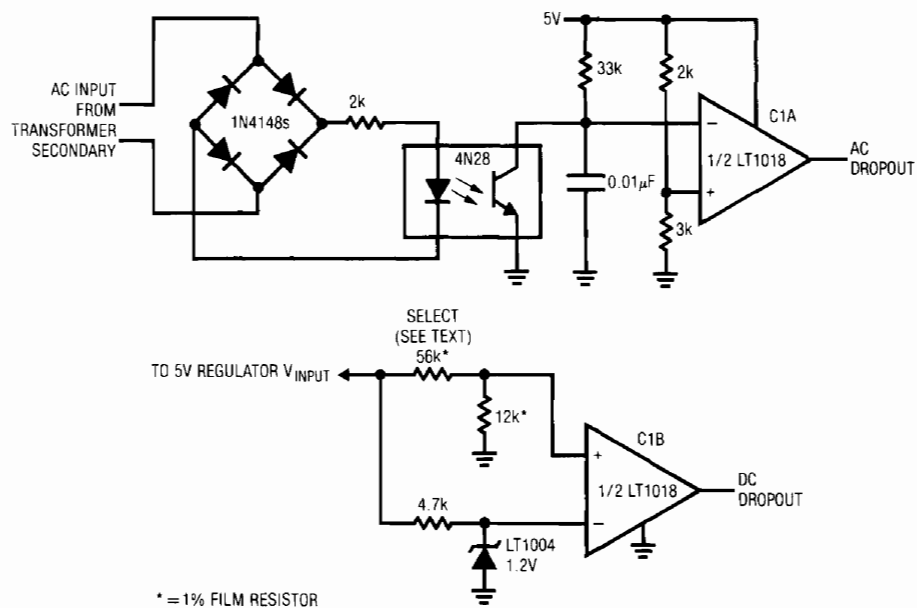


Figure 14. AC-DC Dropout Detector

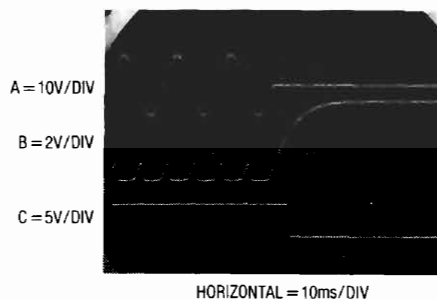


Figure 15. AC Line Dropout Detector Operates within a Half Cycle

Application Note 31

Memory Save Circuit

Figure 16 is another circuit for saving memory contents when power goes down. This DC sensing circuit is useful where AC line dropout detection is not feasible. It functions by utilizing the different dropout voltages of two regulators. In operation, the LT1086 supplies 5V power to the main system, while the LT1020 drives the memory section. When input power, which could be from a battery or filter capacitor, falls (Trace A, Figure 17) the LT1086 drops out first (Trace B). This is detected by the LT1020's on-board auxiliary comparator, which goes low (Trace C). This alerts the memory section to store data. The LT1020 regulator output (Trace D) maintains memory power for additional time due to its extremely low dropout characteristics. It finally begins to fall about 50ms after the memory store command. The optional connections shown allow extended hold up times.

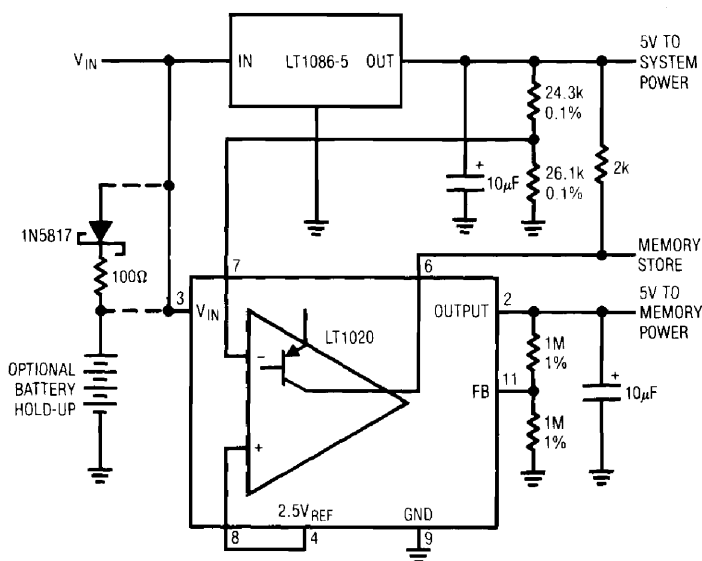


Figure 16. Memory-Save-On-Power Down

Overvoltage Protection Circuit

Figure 18's circuit represents the other extreme in power supply protection. It prevents system damage due to overvoltage produced by regulator failure. If the regulator fails in a way which effectively connects the raw DC supply to the 5V rail, overvoltage will occur. This failure mode is possible if the pass transistor shorts or the feedback loop opens up. C1A compares the 5V supply (Trace A, Figure 19) to the LT1004 reference via a resistive divider. If the supply rises beyond 5.5V (rise starts just past the first vertical division), C1A's output goes high (Trace B), turning on the SCR via Q1. SCR current (Trace C) peaks at almost 6A as it "crowbars" the supply, blowing the downstream fuse. C1B simultaneously pulls the supply feedback node low, ensuring minimum pass transistor on-resistance if the overvoltage is due to feedback or error amplifier malfunction. About 5μs elapses from the time the supply peaks (5.5V) until it begins to shut down. In this case the maximum overvoltage is 5.7V. The 4.3k-1.2k resistor string ratio can be altered for different trip values, and the optional filter used to suppress transients. Note that the LT1018's 1.2V minimum supply voltage combines with the diode in the SCR's gate to eliminate false tripping on power-up.

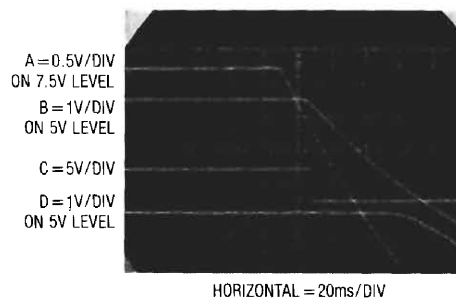


Figure 17. Differential Dropout Between Regulators Provides a Memory Store Pulse and Power Hold-Up

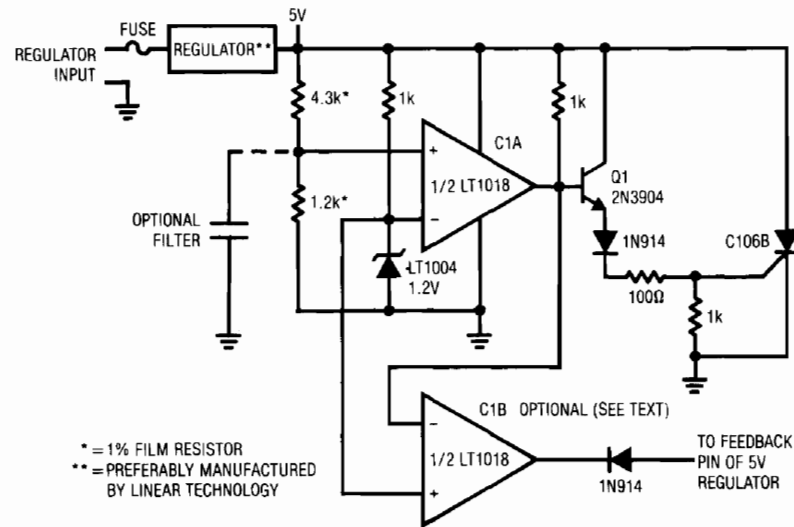


Figure 18. "Crowbar" Overvoltage Protection Circuit

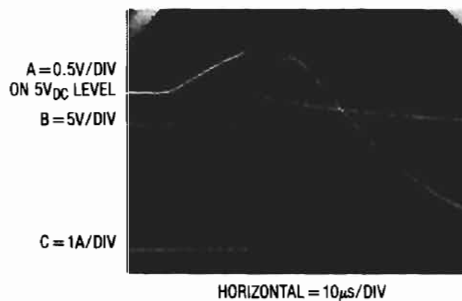


Figure 19. "Crowbar" Stops Overvoltage in 5µs

Power-On-Reset Generator

Another power related requirement involves generating a system reset pulse after supply turn-on. When supply power is applied to Figure 20, the 5V rail comes up (Trace A, Figure 21). The LT1004 clamps at 1.2V and C1A's positive input (Trace B) ramps at a time constant determined by the 0.5% resistors and the 0.1µF capacitor. When C1A's positive input ramps beyond the LT1004 potential, its output goes high, delivering a differentiated pulse to C1B's negative input (Trace C). C1B's output (Trace D) goes low for a period determined by the 0.01µF-680k differentiator. This pulse is used for system reset. The 1N914 gives quick reset for the 0.1µF delay capacitor and the Schottky diode clip's differentiator

caused negative voltages at C1B's input. The turn-on threshold, in this case 4.8V, is set by the ratio of the 0.5% resistors. The output pulse delay time is controlled by the 0.1µF unit, which may be varied. Similarly, the RC combination at C1B sets output pulse width, and may be varied. The LT1018's 1.2V minimum supply voltage prevents spurious output during supply power-up.

"Watchdog" Timer Circuit

Figure 22's circuit is not for power supply management, but serves to prevent lock-up in processor based systems. This can occur if the system misses an instruction due to transient hardware or software events. Such a processor hang-up will usually cause predictable cessation of pulse events somewhere in the system. This circuit issues a reset command in response to such a cessation. In normal operation, a pulse train (Trace A, Figure 23) appears at the circuit input, causing C1A's output (Trace B) to pulse low. The diode path discharges the 0.01µF capacitor (Trace C) each time C1A's output goes low. Interruption of the input pulse train (after the 7th vertical division) allows the capacitor to charge beyond C1B's threshold, triggering it low. This pulse can be used to reset the system. C1B's negative input RC values may be adjusted to accommodate various input pulse train repetition rates.

Application Note 31

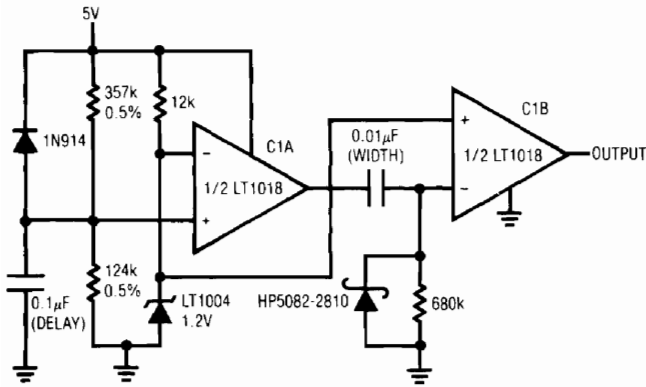


Figure 20. Power-On-Reset Pulse Generator

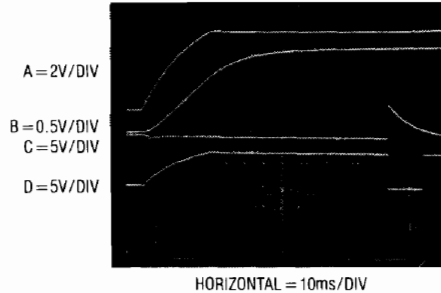


Figure 21. Power-On-Reset Pulse is Generated after Supply Stabilizes

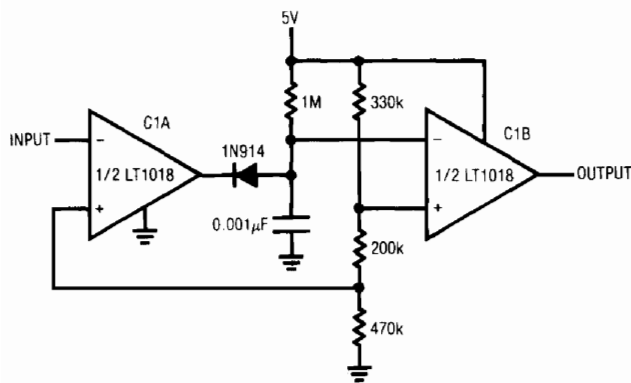


Figure 22. "Watchdog" Timer Circuit

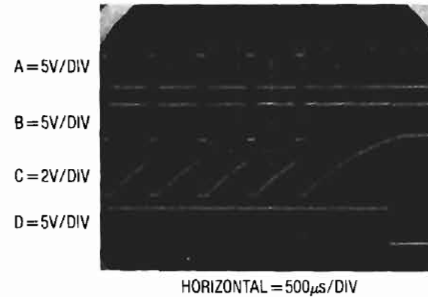


Figure 23. "Watchdog" Drops Low (Trace D) when Pulse Train Ceases

Clock Circuits

Almost all digital systems require a clock source. Generating accurate and reliable clock pulses usually involves quartz based circuits. Figure 24's two circuits cover a 1MHz-25MHz range. In Figure 24A, the LT1016 comparator is set up with DC negative feedback. The 2k resistors set the common-mode level at the device's positive input. Without the crystal, the circuit may be considered as a very wideband (50GHz GBW) amplifier biased at 2.5V. With the crystal inserted, positive feedback occurs and oscillation commences. Figure 24A is useful with AT-cut funda-

mental mode crystals up to 10MHz. Figure 24B is similar, but supports oscillation frequencies to 25MHz. Above 10MHz, AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, ensuring proper operation.

Figure 25's circuit is also similar, but optimized for lower frequency crystals. C1A is the oscillator, with C1B and Q1 used as a sink-source buffer if desired. These circuits also operate with lower cost and lower performance ceramic resonators substituted for the crystal.

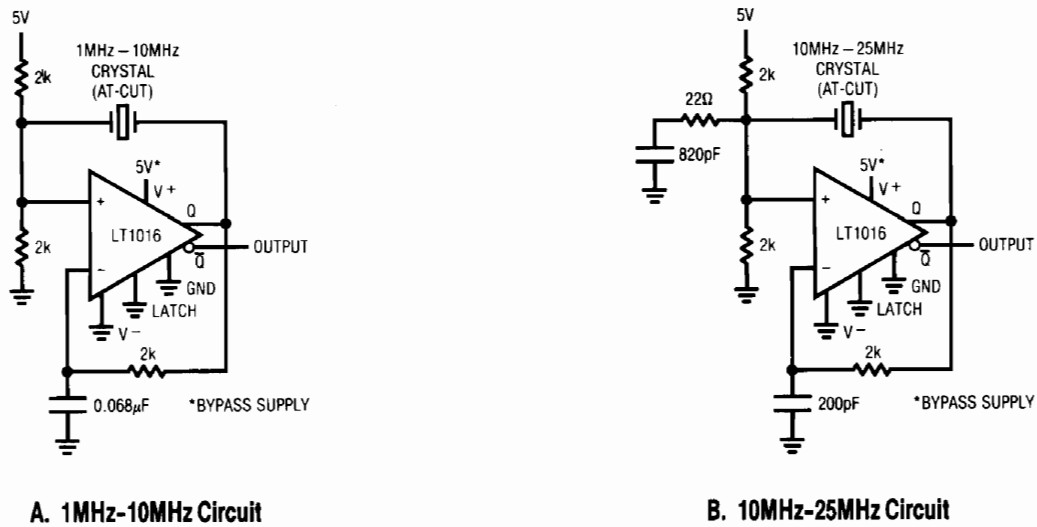


Figure 24. Crystal Oscillator Clock Circuits

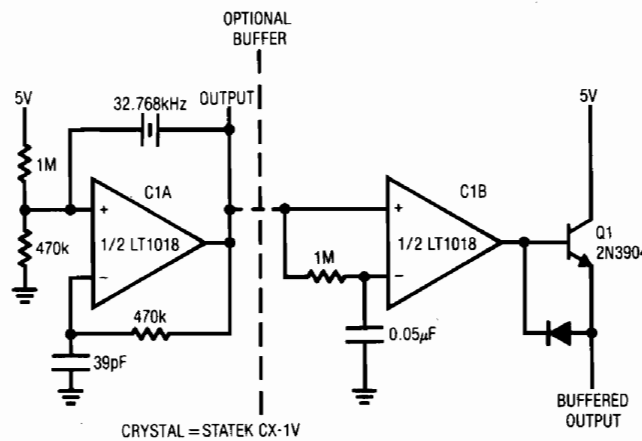


Figure 25. Low Frequency Crystal Oscillator Clock

High Noise Immunity Line Synchronous Clock

Although crystal based circuits are universally applied, they cannot serve all clock requirements. As an example, many systems require a reliable 60Hz line synchronous clock. Zero crossing detectors or simple voltage level detectors are often employed, but have poor noise rejection characteristics. The key to achieving a good line clock under adverse conditions is to design a circuit which takes advantage of the narrow bandwidth of the 60Hz fundamental. Approaches utilizing wide gain-bandwidth, even if hys-

teresis is applied, invite trouble with noise. Figure 26 shows a line synchronous clock which will not lose lock under noisy line conditions. The basic RC multivibrator is tuned to free run near 60Hz, but the AC-line-derived synchronizing input forces the oscillator to lock to the line. The circuit derives its noise rejection from the integrator characteristics of the RC network. As Figure 27 shows, noise and fast spiking on the 60Hz input (Trace A, Figure 27) has little effect on the capacitor's charging characteristics (Trace B) and the circuit's output (Trace C) is stable.

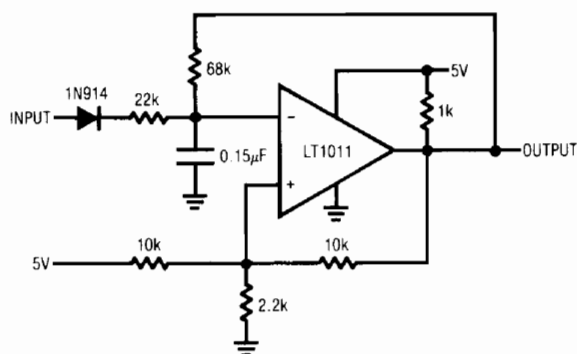


Figure 26. High Noise Immunity Line Synchronization Circuit

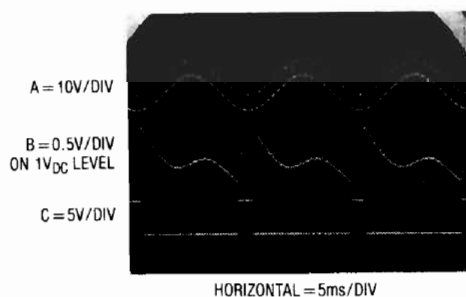


Figure 27. Line Synchronization is Maintained Despite Noisy Input

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

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APPENDIX A

A Primer on Flash Memory

Saul Zales
Intel Corporation

High integration, supported by dense memory, is the key to compact, reliable firmware-based equipment. These products often need post-sales update service for the latest software revisions. While providing high density, EPROMs are costly to update. Equipment must be dismantled, either to UV-erase and then reprogram the EPROMs or to replace them with new ones. This takes at least 15 minutes of a technician's time. Double that if you wait for UV erasure. In contrast, flash memories allow reprogramming "in-system" — in seconds. They are not discarded as EPROMs often are. The simplicity and speed of

the update process yields even bigger savings. Thus, flash memory technology dramatically reduces firmware update costs in EPROM applications.

Non-volatile memory history illustrates flash memory technology's utility. EPROM gave users more control over their code than with ROM by moving the memory coding operation from component purchasing to factory assembly. Similarly, flash technology extends this flexibility. In the factory, it allows multiple test code programming during a single board-testing step. Testing enhances product quality while reducing rework and warranty repair costs.

Beyond the factory, flash technology provides the highest level of code management functionality. Though E²PROM has more functions, its characteristics best suit parameter, as opposed to code, storage. Parameters need to be rewritten individually in real time, that is, while the system is on-line, in normal operation. Parameters also require less memory than code. E²PROM trades off density for the byte-alterable functionality needed for parameter storage.

In contrast, flash memories ideally match embedded code needs. Even if only one line of code needs modification, an entirely new microcomputer program results. Software updates are done as a complete copy for simple code verification. This ensures error-free updating. Flash memory technology mirrors this process with its full-chip erase characteristics in a few seconds of off-line system time.

This framework for delineating non-volatile memory roles is summarized in Figure A1. ROM, EPROM, and flash memory handle large amounts of code, which is installed or modified (excepting ROM) off-line, along an 'increasing flexibility' scale. E²PROM handles smaller amounts of on-line-modified parameters.

The most powerful reprogramming method is In-System Write (ISW). ISW eliminates external programming equipment altogether. It facilitates updates through an existing data communication channel, such as a modem. ISW utilizes the embedded, local CPU for the flash memory device

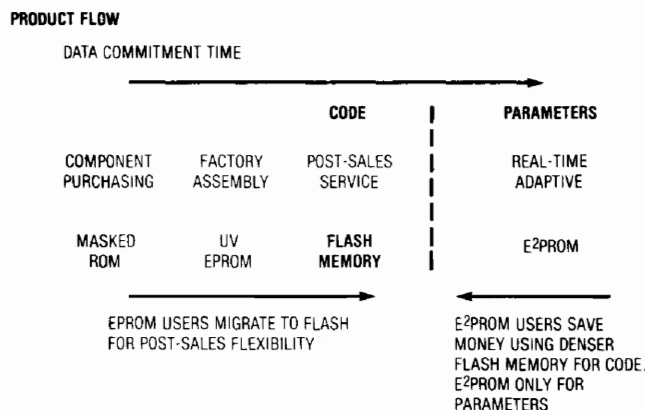


Figure A1. Non-Volatile Memory Flexibility Spectrum

reprogramming 'intelligence,' taking advantage of the off-line nature of updates. The only new requirement for ISW is providing a local programming power supply (V_{PP}), either 12.0V or 12.75V, depending on device specifications. Intel's command register architecture drives reprogramming control: 1) without extra device pins, 2) from a fixed V_{PP} supply, and 3) using standard system read and write timings (though some operations require millisecond-range durations, they are initiated and terminated with standard memory interface timings). See Figure A2 for system block diagram.

Reliability

Intel's ETOX flash memory devices endure up to 10,000 reprogramming cycles, just like E²PROM, yet with EPROM-like quality. The cycling advantage over E²PROM is derived partly from lower-voltage operation. This reduces the electric field intensity across the tunnel oxide by about 2 megavolts per centimeter. Each MV/cm electric field reduction increases the device reliability lifetime by at least one thousand (and as much as ten million) times.

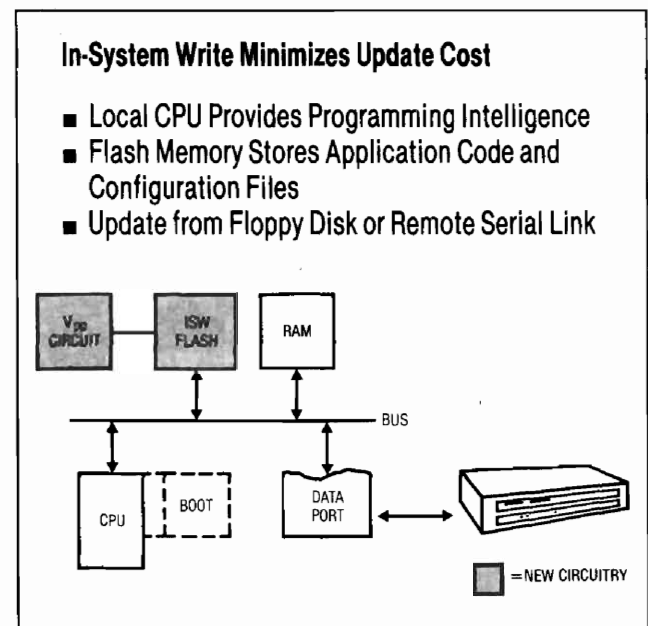


Figure A2. In-System Write

Application Note 31

The common-source approach for erasure is another key contributor. Unlike other E²PROM and flash technologies, ETOX technology uses separate junctions for program and erase which yields: 1) much lower oxide stress, and 2) the ability to optimize the manufacturing process for both program and erase performance and durability. Finally, cycling and overall reliability of ETOX technology-based products is enhanced by the tunnel oxide process employed.

Intel specifies flash memory endurance to be less than 0.01% failures over 100 cycles and 0.1% for 10,000 cycles. In contrast, E²PROMs typically specify 5% failure rates for 10,000 cycles. Lifetime reliability testing of the data retention shows that ETOX technology meets or exceeds EPROM reliability.

APPENDIX B Preventing Memory Destruction

The 12V or 12.75V V_{pp} supplies used with flash memories seem uncomfortably close to the devices 14V breakdown limit. In actuality, the precautions required are similar to overvoltage considerations for 5V rails. Excursions beyond 14V for durations longer than 20ns exceed the chip's absolute maximum rating. As such, the design of V_{pp} generating circuitry requires care to avoid seemingly mysterious memory failures. Although this section uses the 28F010 flash memory as an example, the considerations are generally applicable to other type devices (e.g., 2816).

In theory, a simple low loss transistor switching a low impedance power supply will work. In practice, this is a hazardous approach. Figure B1 shows an ideal V_{pp} pulse produced by simple transistor switching from a power

supply. Settling to the desired V_{pp} level occurs quickly, with no overshoots or aberrations. Figure B2 shows *the same output* measured at the memory pins after a printed circuit trace run. The PC trace looks like an unterminated transmission line with ill-defined characteristics. Reflections occur, causing ringing which exceeds 20V. This is well beyond specified destructive levels, and almost guarantees chip failures. Similar overshooting on the falling edge can cause equally destructive negative voltages to appear at the memory pins.

PN These effects demonstrate the necessity for rise time control. The controlled edge times of the text's closed loop circuits eliminate this problem. Some other features of these circuits make them attractive. Short circuit protection is obviously desirable to protect the V_{pp} generator.

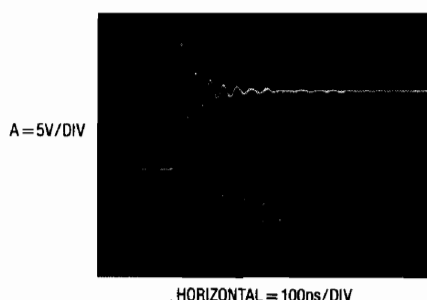
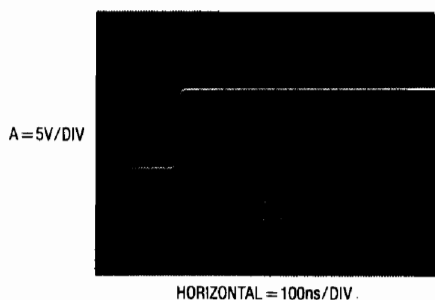


Figure B1. An "Ideal" Flash Memory V_{pp} Output Figure B2. Rings at Destructive Voltages After a PC Trace Run

More subtly, it also protects the memory. In an unprotected V_{PP} generator, the pass switch may fail in a shorted condition. This will cause the memory to see destructive overvoltage and fail. The short circuit protection must be designed so that it does not cause overshoots when operating or recovering from overload. For example, removing A2's shunt diode path in text Figure 4 causes dangerous overshoots on short circuit recovery. Figure B3 shows V_{PP} output recovery with the diode removed. In

Figure B4, the diode is installed and recovery is benign. Similar considerations apply on power-up and down. The V_{PP} generator must not produce spurious outputs during power application or removal. In the text circuits, this is facilitated by employing circuit techniques and ICs which operate down to low voltages. This makes V_{PP} outputs predictable and controllable during transient supply conditions.

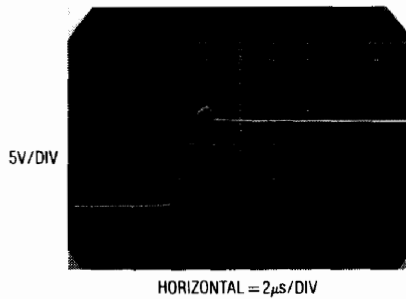


Figure B3.

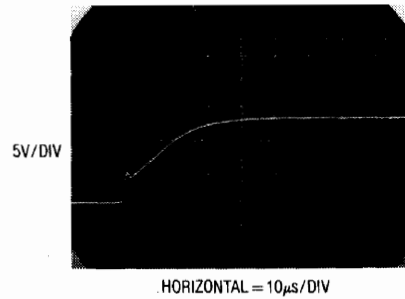


Figure B4.

Short Circuit Recovery for Poorly (Figure B3) and Properly (Figure B4) Designed Connections. Figure B3's Overshoot on Recovery Can Cause Memory Chip Failures

APPENDIX C

Physiology of the LT1070/LT1071/LT1072

The LT1070 series is a family of current-mode switchers with switch duty cycle directly controlled by switch current rather than by output voltage. Referring to Figure C1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or

output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short circuit conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisaturation circuitry detects onset of saturation in the power switch and adjusts drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

Application Note 31

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting, and total regulator shut-down. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50 μ A supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

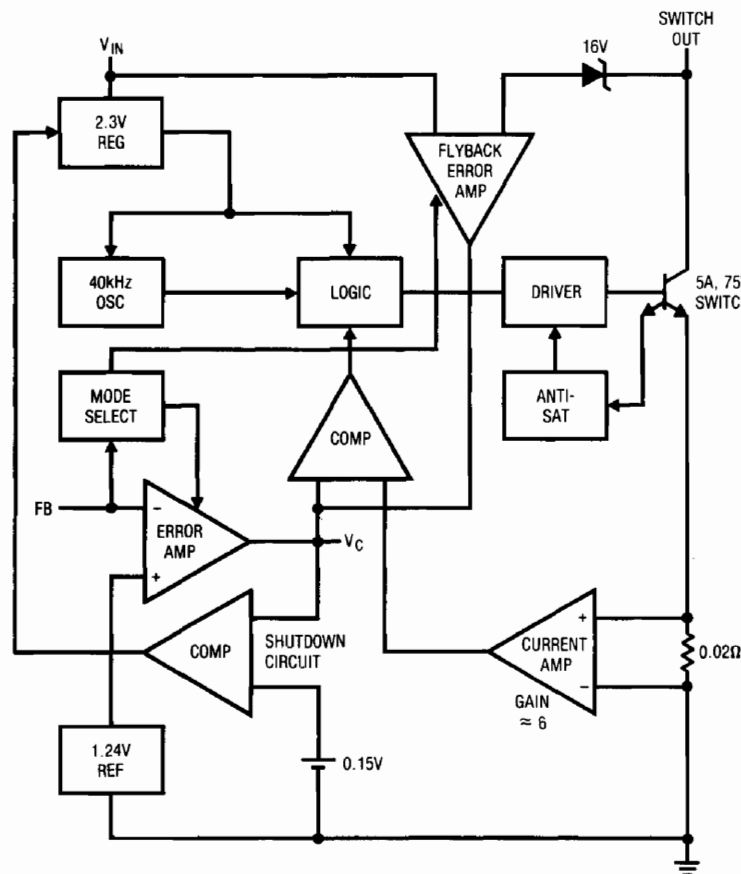


Figure C1. LT1070 Internal Details

High Efficiency Linear Regulators

Jim Williams

Introduction

Linear voltage regulators continue to enjoy widespread use despite the increasing popularity of switching approaches. Linear regulators are easily implemented, and have much better noise and drift characteristics than switchers. Additionally, they do not radiate RF, function with standard magnetics, are easily frequency compensated, and have fast response. Their largest disadvantage is inefficiency. Excess energy is dissipated as heat. This elegantly simplistic regulation mechanism pays dearly in terms of lost power. Because of this, linear regulators are associated with excessive dissipation, inefficiency, high operating temperatures and large heat sinks. While linears cannot compete with switchers in these areas they can achieve significantly better results than generally supposed. New components and some design techniques permit retention of linear regulator's advantages while improving efficiency.

One way towards improved efficiency is to minimize the input-to-output voltage across the regulator. The smaller this term is, the lower the power loss. The minimum input/output voltage required to support regulation is referred to as the "dropout voltage." Various design techniques and technologies offer different performance capabilities. Appendix A, "Achieving Low Dropout," compares some approaches. Conventional three terminal linear regulators have a 3V dropout, while newer devices feature 1.5V dropout (see Appendix B, "A Low Dropout Regulator Family") at 7.5A, decreasing to 0.05V at 100 μ A.

Regulation from Stable Inputs

Lower dropout voltage results in significant power savings where input voltage is relatively constant. This is normally the case where a linear regulator post-regulates a

switching supply output. Figure 1 shows such an arrangement. The main output ("A") is stabilized by feedback to the switching regulator. Usually, this output supplies most of the power taken from the circuit. Because of this, the amount of energy in the transformer is relatively unaffected by power demands at the "B" and "C" outputs. This results in relatively constant "B" and "C" regulator input voltages. Judicious design allows the regulators to run at or near their dropout voltage, regardless of loading or switcher input voltage. Low dropout regulators thus save considerable power and dissipation.

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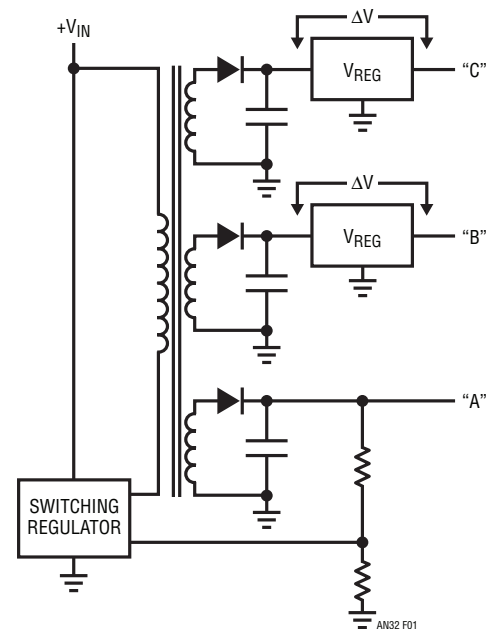


Figure 1. Typical Switching Supply Arrangement Showing Linear Post-Regulators

Application Note 32

Regulation from Unstable Input—AC Line Derived Case

Unfortunately, not all applications furnish a stable input voltage. One of the most common and important situations is also one of the most difficult. Figure 2 diagrams a classic situation where the linear regulator is driven from the AC line via a step-down transformer. A 90VAC (brownout) to 140VAC (high line) line swing causes the regulator to see a proportionate input voltage change. Figure 3 details efficiency under these conditions for standard (LM317) and low dropout (LT[®]1086) type devices. The LT1086's lower dropout improves efficiency. This is particularly evident at 5V output, where dropout is a significant percentage of

the output voltage. The 15V output comparison still favors the low dropout regulator, although efficiency benefit is somewhat reduced. Figure 4 derives resultant regulator power dissipation from Figure 3's data. These plots show that the LT1086 requires less heat sink area to maintain the same die temperature as the LM317.

Both curves show the deleterious effects of poorly controlled input voltages. The low dropout device clearly cuts losses, but input voltage variation degrades obtainable efficiency.

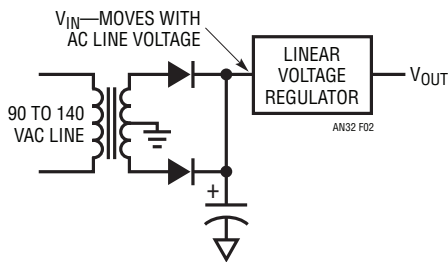
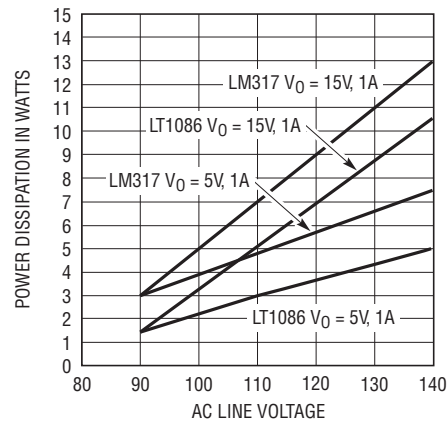
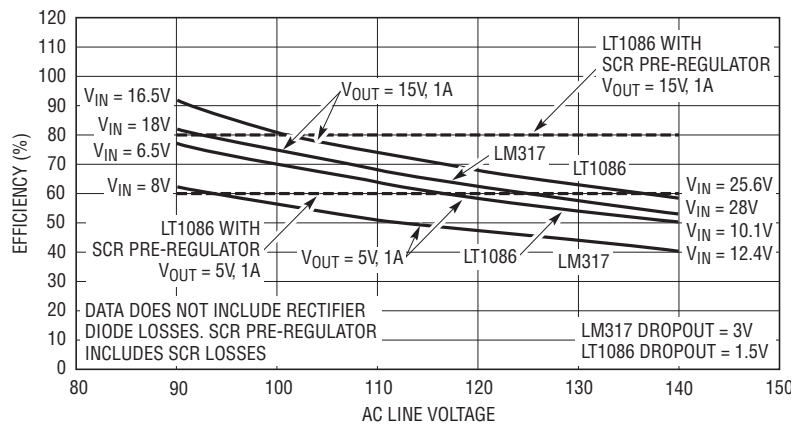


Figure 2. Typical AC Line Driven Linear Regulator



AN32 F04

Figure 4. Power Dissipation for Different Regulators vs AC Line Voltage. Rectifier Diode Losses are not Included



AN32 F03

Figure 3. Efficiency vs AC Line Voltage for LT1086 and LM317 Regulators

Application Note 32

This circuit has a dramatic impact on LT1086 efficiency versus AC line swing*. Referring back to Figure 3, the data shows good efficiency with no change for 90VAC to 140VAC input variations. This circuit's slow switching preserves the linear regulators low noise. Figure 7 shows slight 120Hz residue with no wideband components.

*The transformer used in a pre-regulator can significantly influence overall efficiency. One way to evaluate power consumption is to measure the actual power taken from the 115VAC line. See Appendix C, "Measuring Power Consumption."

DC Input Pre-Regulator

Figure 8a's circuit is useful where the input is DC, such as an unregulated (or regulated) supply or a battery. This circuit is designed for low losses at high currents. The LT1083 functions in conventional fashion, supplying a regulated output at 7.5A capacity. The remaining components form a switched-mode dissipation regulator. This regulator maintains the LT1083 input just above the dropout voltage under all conditions. When the LT1083 input (Trace A, Figure 9) decays far enough, C1A goes high,

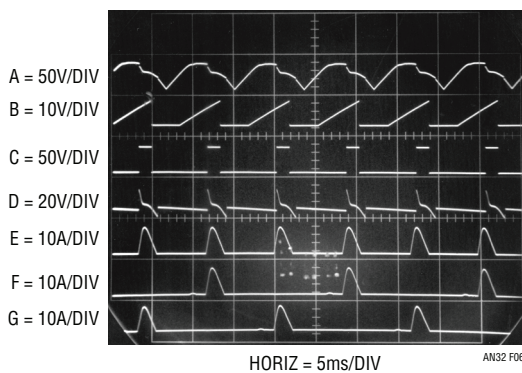


Figure 6. Waveforms for the SCR Pre-Regulator

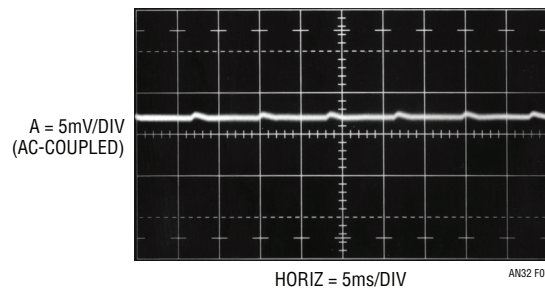


Figure 7. Output Noise for the SCR Pre-Regulated Circuit

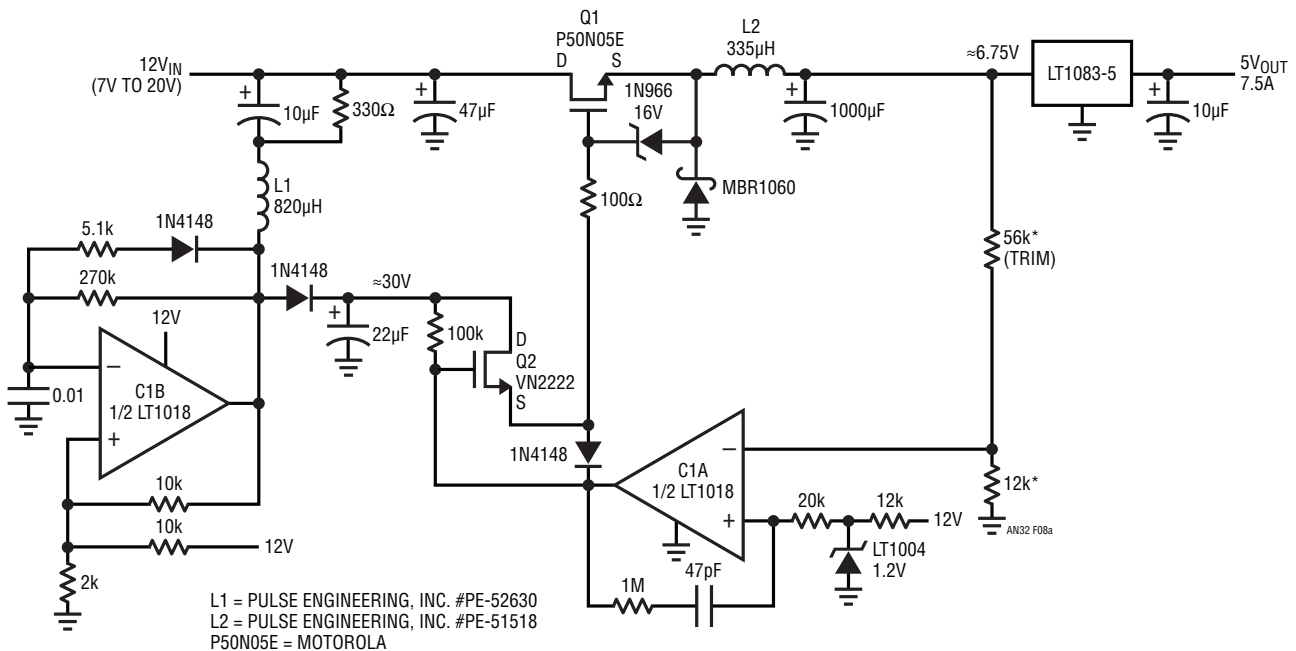


Figure 8a. Pre-Regulated Low Dropout Regulator

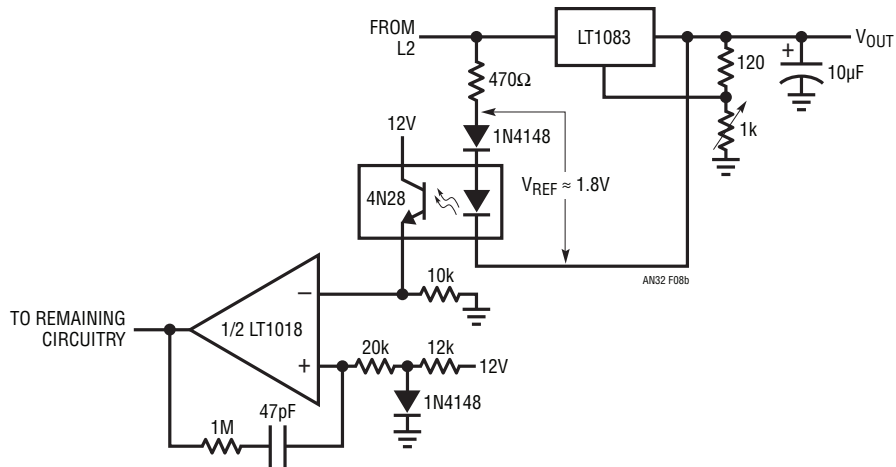


Figure 8b. Differential Sensing for the Pre-Regulator Allows Variable Outputs

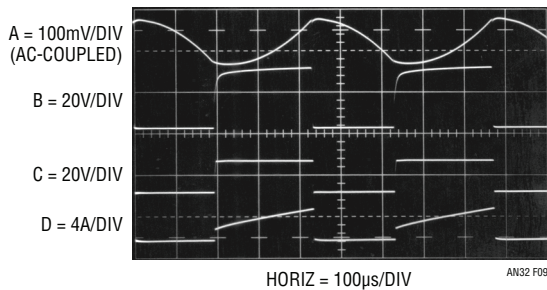


Figure 9. Pre-Regulator Waveforms

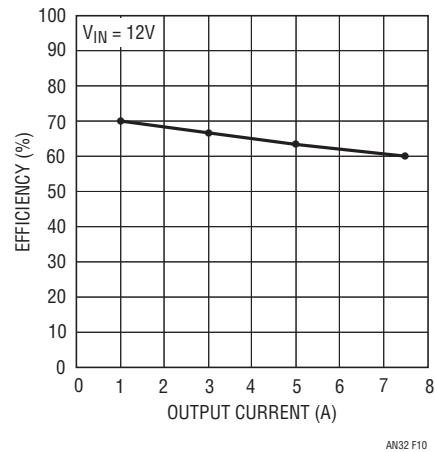


Figure 10. Efficiency vs Output for Figure 8a

allowing Q1's gate (Trace B) to rise. This turns on Q1, and its source (Trace C) drives current (Trace D) into L2 and the 1000μF capacitor, raising regulator input voltage. When the regulator input rises far enough C1A returns low, Q1 cuts off and capacitor charging ceases. The MBR1060 damps L2's flyback spike and the 1M-47pF combination sets loop hysteresis at about 100mV.

Q1, an N-channel MOSFET, has only 0.028Ω of saturation loss but requires 10V of gate-source turn-on bias. C1B, set up as a simple flyback voltage booster, provides about 30V DC boost to Q2. Q2, serving as a high voltage pull-up for C1A, provides voltage overdrive to Q1's gate. This ensures Q1 saturation, despite its source follower connection. The Zener diode clamps excessive gate-source

overdrives. These measures are required because alternatives are unattractive. Low loss P-channel devices are not currently available, and bipolar approaches require large drive currents or have poor saturation. As before, the linear regulator's current limit protects against overloads. Figure 10 plots efficiency for the pre-regulated LT1083 over a range of currents. Results are favorable, and the linear regulator's noise and response advantages are retained.

Figure 8b shows an alternate feedback connection which maintains a fixed small voltage across the LT1083 in applications where variable output is desired. This scheme maintains efficiency as the LT1083's output voltage is varied.

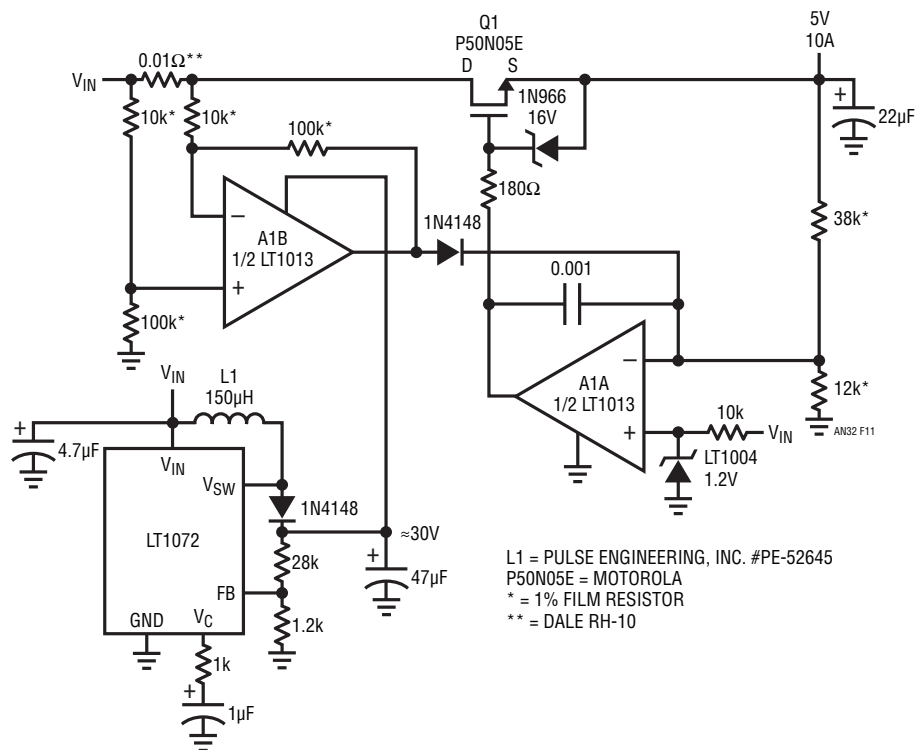


Figure 11. 10A Regulator with 400mV Dropout

10A Regulator with 400mV Dropout

In some circumstances an extremely low dropout regulator may be required. Figure 11 is substantially more complex than a three terminal regulator, but offers 400mV dropout at 10A output. This design borrows Figure 8A's overdriven source follower technique to obtain extremely low saturation resistance. The gate boost voltage is generated by the LT1072 switching regulator, set up as a flyback converter.* This configuration's 30V output powers A1, a dual op amp. A1A compares the regulators output to the LT1004 reference and servo controls Q1's gate to close the loop. The gate voltage overdrive allows Q1 to attain its 0.028Ω saturation, permitting the extremely low dropout noted. The Zener diode clamps excessive gate-source voltage and the 0.001μF capacitor stabilizes the loop. A1B, sensing current

*If boost voltage is already present in the system, significant circuit simplification is possible. See LTC Design Note 32, "A Simple Ultra-Low Dropout Regulator."

across the 0.01Ω shunt, provides current limiting by forcing A1A to swing negatively. The low resistance shunt limits loss to only 100mV at 10A output. Figure 12 plots current limit performance for the regulator. Roll-off is smooth, with no oscillation or undesirable characteristics.

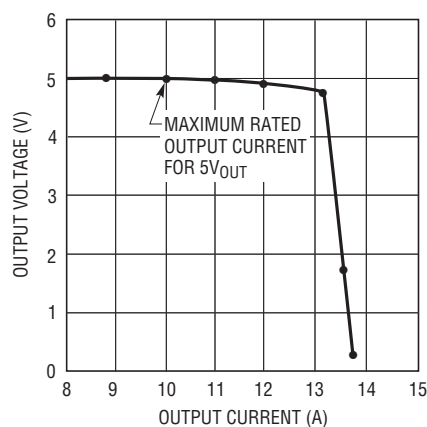


Figure 12. Current Limit Characteristics for the Discrete Regulator

Application Note 32

Ultrahigh Efficiency Linear Regulator

Figure 13 combines the preceding discrete circuits to achieve highly efficient linear regulation at high power. This circuit combines Figure 8a's pre-regulator with Figure 11's discrete low dropout design. Modifications include deletion of the linear regulators boost supply and slight adjustment of the gate-source Zener diode values. Similarly, a single 1.2V reference serves both pre-regulator and linear output regulator. The upward adjustment in the Zener clamp values ensures adequate boost voltage under low voltage input conditions. The pre-regulator's feedback resistors set the linear regulators input voltage just above its 400mV dropout.

This circuit is complex, but performance is impressive. Figure 14 shows efficiency of 86% at 1A output, decreasing to 76% at full load. The losses are approximately evenly distributed between the MOSFETs and the MBR1060 catch diode. Replacing the catch diode with a synchronously switched FET (see Linear Technology AN29, Figure 32) and trimming the linear regulator input to the lowest possible value could improve efficiency by 3% to 5%.

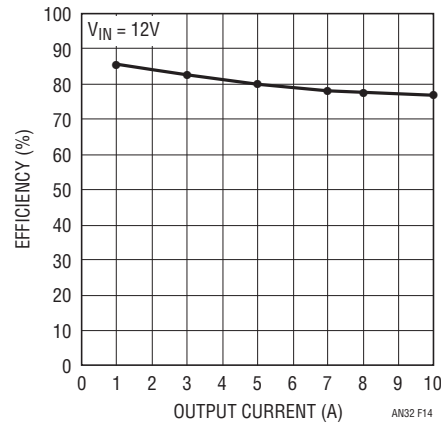


Figure 14. Efficiency vs Output Current for Figure 13

Micropower Pre-Regulated Linear Regulator

Power linear regulators are not the only types which can benefit from the above techniques. Figure 15's pre-regulated micropower linear regulator provides excellent efficiency and low noise. The pre-regulator is similar to Figure 8a. A drop at the pre-regulator's output (Pin 3 of the LT1020 regulator, Trace A, Figure 16) causes the LT1020's comparator to go high. The 74C04 inverter chain switches,

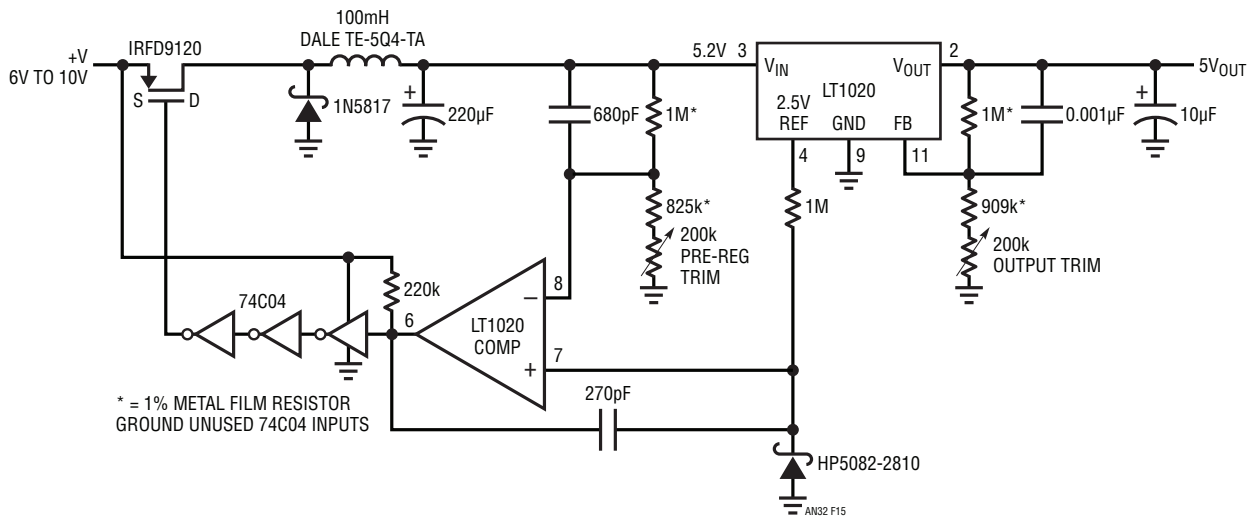


Figure 15. Micropower Pre-Regulated Linear Regulator

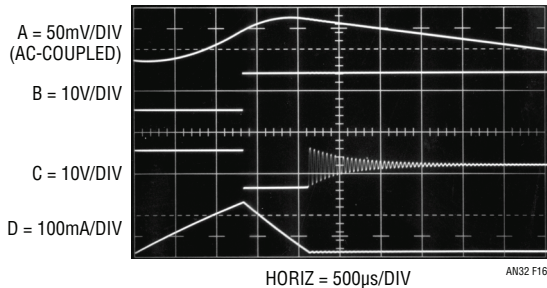


Figure 16. Figure 15's Waveforms

biasing the P-channel MOSFET switch's grid (Trace B). The MOSFET comes on (Trace C), delivering current to the inductor (Trace D). When the voltage at the inductor-220µF junction goes high enough (Trace A), the comparator switches high, turning off MOSFET current flow. This loop regulates the LT1020's input pin at a value set by the resistor divider in the comparator's negative input and the LT1020's 2.5V reference. The 680pF capacitor stabilizes the loop and the 1N5817 is the catch diode. The 270pF capacitor aids comparator switching and the 2810 diode prevents negative overdrives.

The low dropout LT1020 linear regulator smooths the switched output. Output voltage is set with the feedback pin associated divider. A potential problem with this circuit is start-up. The pre-regulator supplies the LT1020's input but relies on the LT1020's internal comparator to function. Because of this, the circuit needs a start-up mechanism. The 74C04 inverters serve this function. When power is applied, the LT1020 sees no input, but the inverters do. The 200k path lifts the first inverter high, causing the chain to switch, biasing the MOSFET and starting the circuit. The inverter's rail-to-rail swing also provides good MOSFET grid drive.

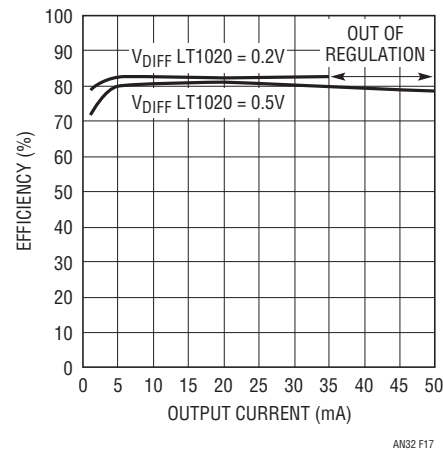


Figure 17. Efficiency vs Output Current for Figure 15

The circuit's low 40µA quiescent current is due to the low LT1020 drain and the MOS elements. Figure 17 plots efficiency versus output current for two LT1020 input-output differential voltages. Efficiency exceeding 80% is possible, with outputs to 50mA available.

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1. Lambda Electronics, Model LK-343A-FM Manual
2. Grafham, D.R., "Using Low Current SCRs," General Electric AN200.19. Jan. 1967
3. Williams, J., "Performance Enhancement Techniques for Three-Terminal Regulators," Linear Technology Corporation. AN2
4. Williams, J., "Micropower Circuits for Signal Conditioning," Linear Technology Corporation. AN23
5. Williams, J. and Huffman, B., "Some Thoughts on DC-DC Converters," Linear Technology Corporation. AN29
6. Analog Devices, Inc, "Multiplier Application Guide"

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

APPENDIX A

Achieving Low Dropout

Linear regulators almost always use Figure A1a's basic regulating loop. Dropout limitations are set by the pass elements on-impedance limits. The ideal pass element has zero impedance capability between input and output and consumes no drive energy.

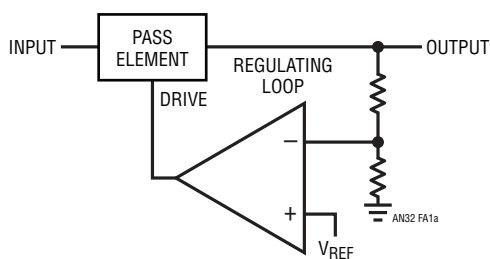


Figure A1a. Basic Regulating Loop

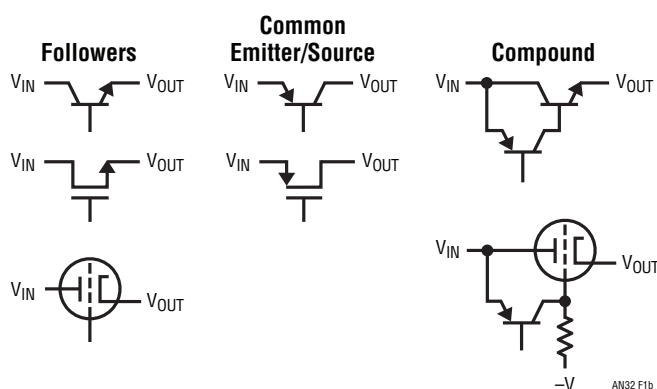


Figure A1b. Linear Regulator with Some Pass Element Candidates

A number of design and technology options offer various trade-offs and advantages. Figure A1b lists some pass element candidates. Followers offer current gain, ease of loop compensation (voltage gain is below unity) and the drive current ends up going to the load. Unfortunately, saturating a follower requires voltage overdriving the input (e.g., base, gate). Since drive is usually derived directly from V_{IN} this is difficult. Practical circuits must either generate the overdrive or obtain it elsewhere. This is not easily done in IC power regulators, but is realizable in discrete circuits (e.g., Figure 11). Without voltage overdrive the saturation loss is set by V_{be} in the bipolar case and channel on-resistance for MOS. MOS channel

on-resistance varies considerably under these conditions, although bipolar losses are more predictable. Note that voltage losses in driver stages (Darlington, etc.) add directly to the dropout voltage. The follower output used in conventional three terminal IC regulators combines with drive stage losses to set dropout at 3V.

Common emitter/source is another pass element option. This configuration removes the V_{be} loss in the bipolar case. The PNP version is easily fully saturated, even in IC form. The trade-off is that the base current never arrives at the load, wasting substantial power. At higher currents, base drive losses can negate a common emitter's saturation advantage. This is particularly the case in IC designs, where high beta, high current PNP transistors are not practical. As in the follower example, Darlington connections exacerbate the problem. At moderate currents PNP common emitters are practical for IC construction. The LT1020/LT1120 uses this approach.

Common source connected P-channel MOSFETs are also candidates. They do not suffer the drive losses of bipolars, but typically require 10V of gate-channel bias to fully saturate. In low voltage applications this usually requires generation of negative potentials. Additionally, P-channel devices have poorer saturation than equivalent size N-channel devices.

The voltage gain of common emitter and source configurations is a loop stability concern, but is manageable.

Compound connections using a PNP driven NPN are a reasonable compromise, particularly for high power (beyond 250mA) IC construction. The trade-off between the PNP V_{ce} saturation term and reduced drive losses over a straight PNP is favorable. Also, the major current flow is through a power NPN, easily realized in monolithic form. This connection has voltage gain, necessitating attention to loop frequency compensation. The LT1083-6 regulators use this pass scheme with an output capacitor providing compensation.

Readers are invited to submit results obtained with our emeritus thermionic friends, shown out of respectful courtesy.

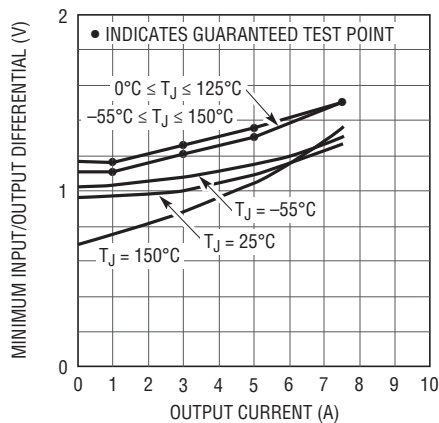
APPENDIX B

A Low Dropout Regulator Family

The LT1083-6 series regulators detailed in Figure B1 feature maximum dropout below 1.5V. Output currents range from 1.5A to 7.5A. The curves show dropout is significantly lower at junction temperatures above 25°C. The NPN pass transistor based devices require only 10mA load current for operation, eliminating the large base drive loss characteristic of PNP approaches (see Appendix A for discussion).

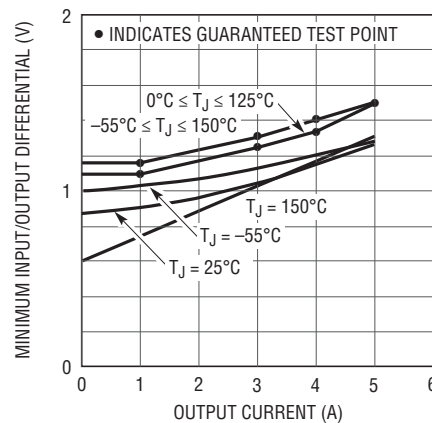
In contrast, the LT1020/LT1120 series is optimized for lower power applications. Dropout voltage is about 0.05V at 100µA, rising to only 400mV at 100mA output. Quiescent current is 40µA.

LT1083 Dropout Voltage vs Output Current



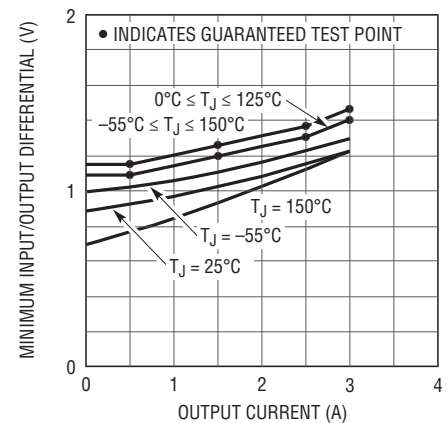
AN32 FB1a

LT1084 Dropout Voltage vs Output Current



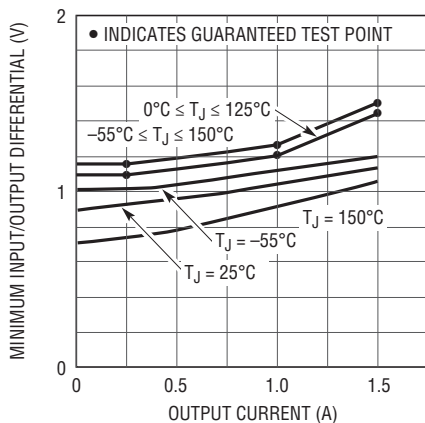
AN32 FB1b

LT1085 Dropout Voltage vs Output Current



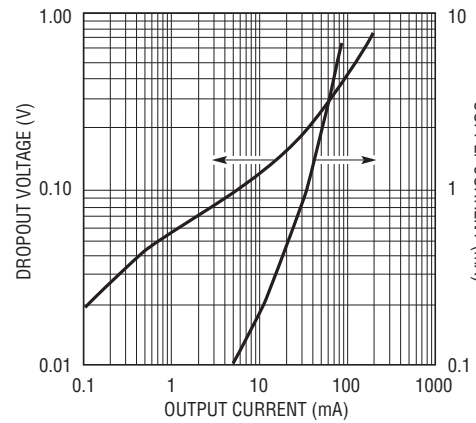
AN32 FB1c

LT1086 Dropout Voltage vs Output Current



AN32 FB1d

LT1020/LT1120 Dropout Voltage and Supply Current



AN32 FB1e

Figure B1. Characteristics of Low Dropout IC Regulators

Application Note 32

APPENDIX C

Measuring Power Consumption

Accurately determining power consumption often necessitates measurement. This is particularly so in AC line driven circuits, where transformer uncertainties or lack of manufacturer's data precludes meaningful estimates. One way to measure AC line originated input power (Watts) is a true, real time computation of E-I product. Figure C1's circuit does this and provides a safe, usable output.

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

The AC load to be measured is plugged into the test socket. Current is measured across the 0.01Ω shunt by A1A with additional gain and scaling provided by A1B. The diodes and fuse protect the shunt and amplifier against severe

overloads. Load voltage is derived from the 100k-4k divider. The shunts low value minimizes voltage burden error.

The voltage and current signals are multiplied by a 4-quadrant analog multiplier (AD534) to produce the power product. All of this circuitry floats at AC line potential, making direct monitoring of the multipliers output potentially lethal. Providing a safe, usable output requires a galvanically isolated way to measure the multiplier output. The 286J isolation amplifier does this, and may be considered as a unity-gain amplifier with inputs fully isolated from its output. The 286J also supplies the floating $\pm 15V$ power required for A1 and the AD534. The 286J's output is referred to circuit common (\perp). The 281 oscillator/driver is necessary to operate the 286J (see Analog Devices data sheet for details). The LT1012 and associated components provide a filtered and scaled output. A1B's gain switching provides decade ranging from 20W to 2000W full scale. The signal path's bandwidth permits accurate results, even for nonlinear or discontinuous loads (e.g. SCR choppers). To calibrate this circuit install a known full-scale load, set A1B to the appropriate range, and adjust the trimpot for a correct reading. Typical accuracy is 1%.

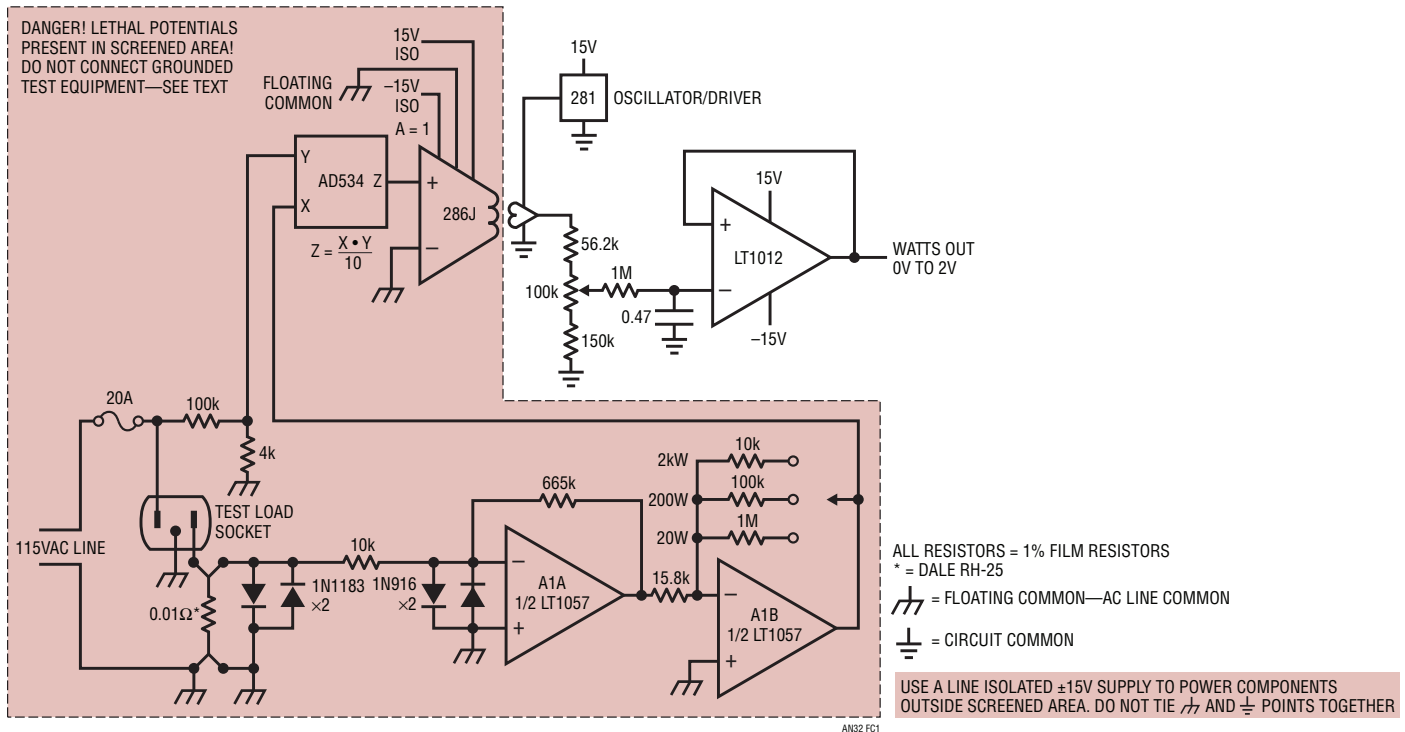


Figure C1. AC Wattmeter **DANGER! Lethal Potentials Present—See Text**

Step-Down Switching Regulators

Jim Williams

A substantial percentage of regulator requirements involve stepping down the primary voltage. Although linear regulators can do this, they cannot achieve the efficiency of switching based approaches¹. The theory supporting step-down (“buck”) switching regulation is well established, and has been exploited for some time. Convenient, easily applied ICs allowing implementation of practical circuits are, however, relatively new. These devices permit broad application of step-down regulation with minimal complexity and low cost. Additionally, more complex functions incorporating step-down regulation become realizable.

Basic Step Down Circuit

Figure 1 is a conceptual voltage step-down or “buck” circuit. When the switch closes the input voltage appears at the inductor. Current flowing through the inductor-capacitor combination builds over time. When the switch

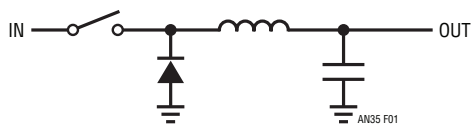


Figure 1. Conceptual Voltage Step-Down (“Buck”) Circuit

opens current flow ceases and the magnetic field around the inductor collapses. Faraday teaches that the voltage induced by the collapsing magnetic field is opposite to the originally applied voltage. As such, the inductor’s left side heads negative and is clamped by the diode. The capacitors accumulated charge has no discharge path, and a DC potential appears at the output. This DC potential is lower than the input because the inductor limits current during the switch’s on-time. Ideally, there are no dissipative elements in this voltage step-down conversion. Although the output *voltage* is lower than the input, there is no *energy*

lost in this voltage-to-current-to-magnetic field-to-current-to-charge-to-voltage conversion. In practice, the circuit elements have losses, but step-down efficiency is still higher than with inherently dissipative (e.g., voltage divider) approaches. Figure 2 feedback controls the basic circuit to regulate output voltage. In this case switch on-time (e.g., inductor charge time) is varied to maintain the output against changes in input or loading.

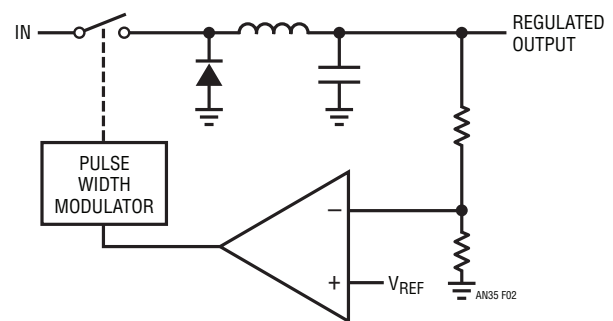


Figure 2. Conceptual Feedback Controlled Step-Down Regulator

Practical Step-Down Switching Regulator

Figure 3, a practical circuit using the LT[®]1074² IC regulator, shows similarities to the conceptual regulator. Some new elements have also appeared. Components at the LT1074’s “V_{COMP}” pin control the IC’s frequency compensation, stabilizing the feedback loop. The feedback resistors are selected to force the “feedback” pin to the device’s internal 2.5V reference value. Figure 4 shows operating waveforms for the regulator at V_{IN} = 28V with a 5V, 1A load.

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Note 1: While linear regulators cannot compete with switchers, they can achieve significantly better efficiencies than generally supposed. See LTC Application Note 32, “High Efficiency Linear Regulators,” for details.

Note 2: See Appendix A for details on this device.

Application Note 35

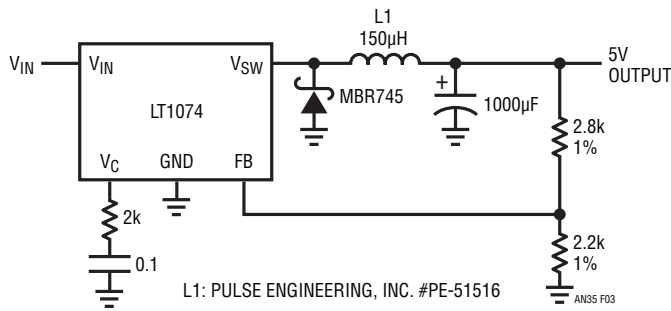


Figure 3. A Practical Step-Down Regulator Using the LT1074

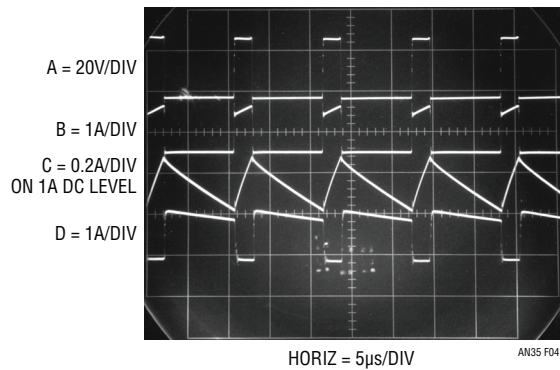


Figure 4. Waveforms for the Step-Down Regulator at $V_{IN} = 28V$ and $V_{OUT} = 5V$ at 1A

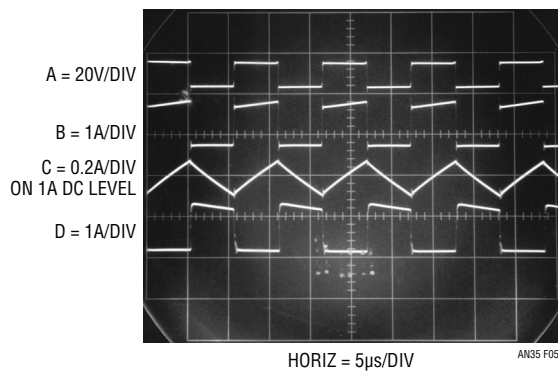


Figure 5. Waveforms for the Step-Down Regulator at $V_{IN} = 12V$ and $V_{OUT} = 5V$ at 1A

Trace A is the V_{SW} pin voltage and Trace B is its current. Inductor current³ appears in Trace C and diode current is Trace D. Examination of the current waveforms allows determination of the V_{SW} and diode path contributions to inductor current. Note that the inductor current's waveform occurs on top of a 1A DC level. Figure 5 shows significant duty cycle changes when V_{IN} is reduced to 12V. The lower input voltage requires longer inductor charge times to maintain the output. The LT1074 controls inductor charge characteristics (see Appendix A for operating details), with resulting waveform shape and time proportioning changes.

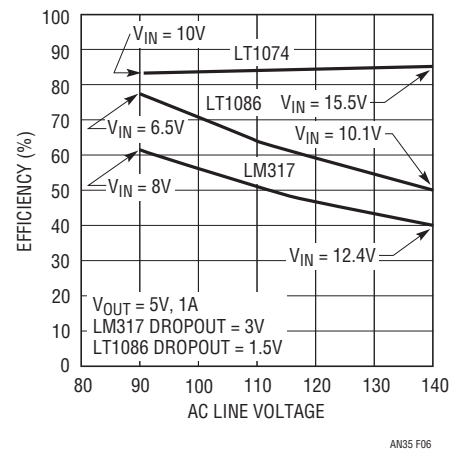


Figure 6. Efficiency vs AC Line Voltage for the LT1074. LT1086 and LM317 Linear Regulators are Shown for Comparison

Figure 6 compares this circuit's efficiency with linear regulators in a common and important situation. Efficient regulation under varying AC line conditions is a frequent requirement. The figure assumes the AC line has been transformed down to acceptable input voltages. The input voltages shown correspond to the AC line voltages given on the horizontal axis. Efficiency for the LM317 and LT1086 linear regulators suffers over the wide input range.

Note 3: Methods for selecting appropriate inductors are discussed in Appendix B.

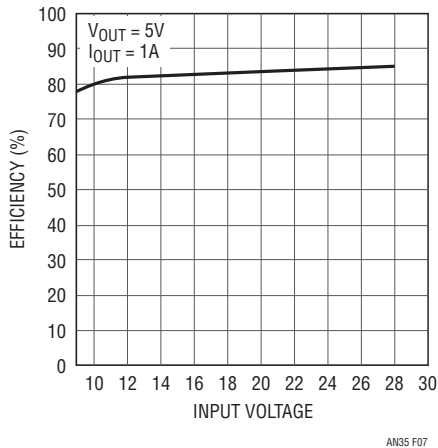


Figure 7. Efficiency Plot for Figure 3. Higher Input Voltages Minimize Effects of Saturation Losses, Resulting in Increased Efficiency

The LT1086 is notably better because its lower dropout voltage cuts dissipation over the range. Switching pre-regulation⁴ can reduce these losses, but cannot equal the LT1074's performance. The plot shows minimum efficiency of 83%, with some improvement over the full AC line excursion. Figure 7 details performance. Efficiency approaches 90% as input voltage rises. This is due to minimization of the effects of fixed diode and LT1074 junction losses as input increases. At low inputs these losses are a higher percentage of available supply, degrading efficiency. Higher inputs make the fixed losses a smaller percentage, improving efficiency. Appendix D presents detail on optimizing circuitry for efficiency.

Dual Output Step-Down Regulator

Figure 8, a logical extension of the basic step-down converter, provides positive and negative outputs. The circuit is essentially identical to Figure 3's basic converter with the addition of a coupled winding to L1. This floating winding's output is rectified, filtered and regulated to a -5V output. The floating bias to the LT1086 positive voltage regulator permits negative outputs by assigning the regulator's output terminal to ground. Negative output power is set by flux pick-up from L1's driven winding. With a 2A load at the +15 output the -5V output can supply over 500mA. Because L1's secondary winding is floating its output may be referred to any point within the breakdown capability of the device. Hence, the secondary output could be 5V or, if stacked on the +15 output, 20V.

Negative Output Regulators

Negative outputs can also be obtained with a simple 2-terminal inductor. Figure 9 demonstrates this by essentially grounding the inductor and steering the catch diodes negative current to the output. A1 facilitates loop closure by providing a scaled inversion of the negative output to the LT1074's feedback pin. The 1% resistors set the scale factor (e.g., output voltage) and the RC network around A1 gives frequency compensation. Waveforms for this circuit are reminiscent of Figure 5, with the exception that diode

Note 4: See Reference 1.

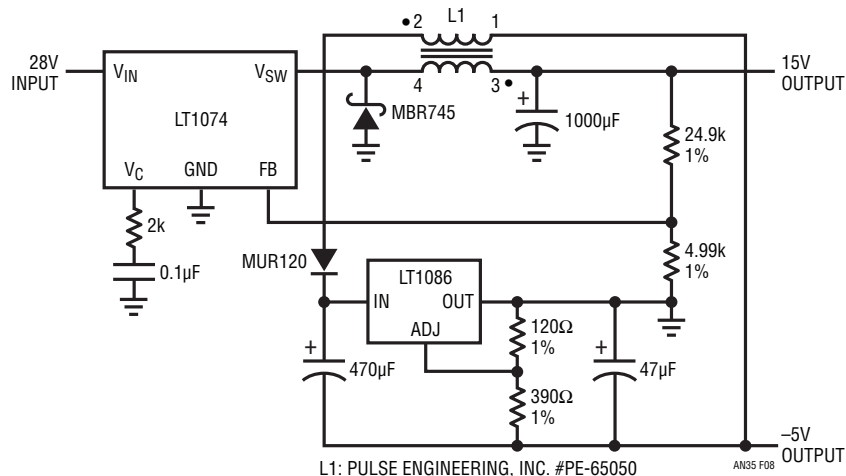


Figure 8. Coupled Inductor Provides Positive and Negative Outputs

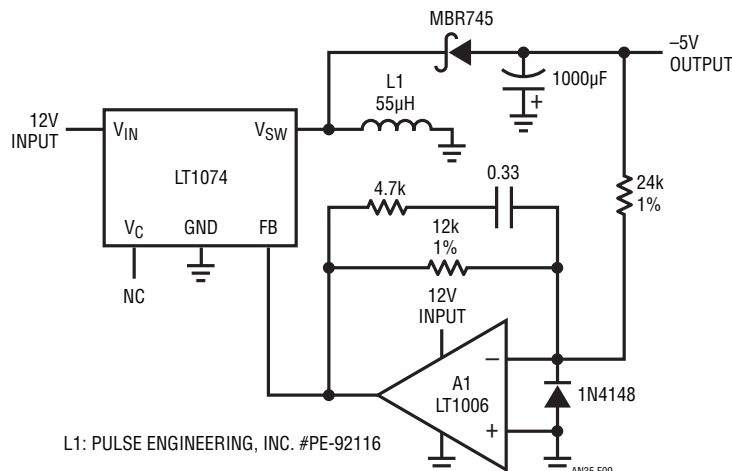


Figure 9. A Negative Output Step-Down Regulator

current (Trace D) is negative. Traces A, B and C are V_{SW} voltage, inductor current and V_{SW} current respectively.

Figure 11, commonly referred to as “Nelson’s Circuit,” provides the same function as the previous circuit, but eliminates the level-shifting op amp. This design accomplishes the level shift by connecting the LT1074’s “ground” pin to the negative output. Feedback is sensed from circuit ground, and the regulator forces its feedback pin 2.5V above its “ground” pin. Circuit ground is common to input and output, making system use easy. Operating waveforms are essentially identical to Figure 10. Advantages of the previous circuit compared to this one are that the LT1074 package can directly contact a grounded heat sink and that control signals may be directly interfaced to the ground referred pins.

The inductor values in both negative output designs are notably lower than in the positive case. This is necessitated

by the reduced loop phase margin of these circuits. Higher inductance values, while preferable for limiting peak current, will cause loop instability or outright oscillation.

Current-Boosted Step-Down Regulator

Figure 12 shows a way to obtain significantly higher output currents by utilizing efficient energy storage in the LT1074 output inductor. This technique increases the duty cycle over the standard step-down regulator allowing more energy to be stored in the inductor. The increased output current is achieved at the expense of higher output voltage ripple.

The operating waveforms for this circuit are shown in Figure 13. The circuit operating characteristics are similar to that of the step-down regulator (Figure 3). During the V_{SW} (Trace A) “on” time the input voltage is applied to one end of the coupled inductor. Current through the V_{SW} pin (Trace B) ramps up almost instantaneously (since inductor current (Trace F) is present) and then slows as energy is stored in the core. The current proceeds into the inductor (Trace D) and finally is delivered to the load. When the V_{SW} pin goes off, current is no longer available to charge the inductor. The magnetic field collapses, causing the V_{SW} pin voltage to go negative. At this point similarity with the basic regulator vanishes. In this modified version the output current (Trace F) receives a boost as the magnetic field collapses. This results when the energy stored in

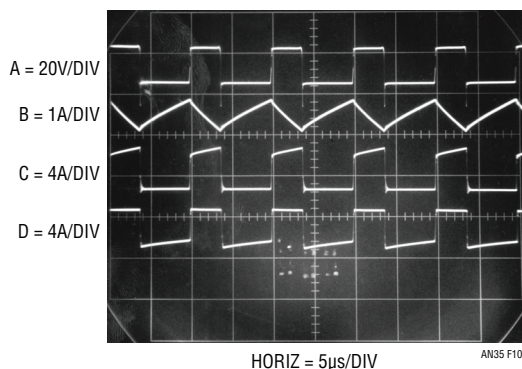


Figure 10. Figure 9’s Waveforms

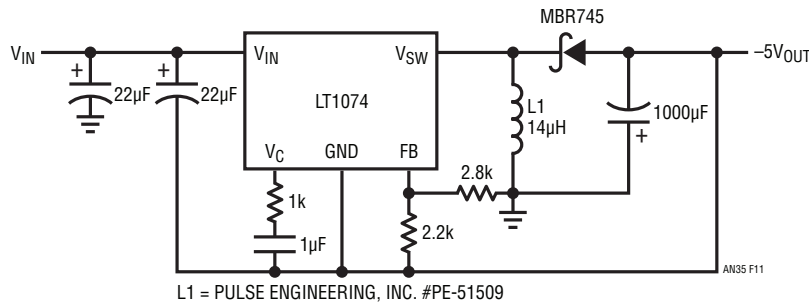


Figure 11. Nelson's Circuit...A (Better) Negative Output Step-Down Regulator

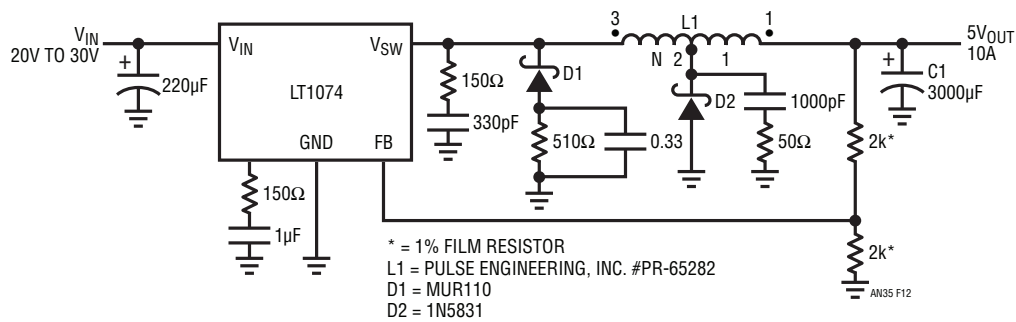


Figure 12. "Current Boosted" Step-Down Regulator. Boost Current is Supplied By Energy Stored in the Tapped Inductor

the core is transferred to the output. This current step circulates through C1 and D2 (Trace E), somewhat increasing output voltage ripple. Not all the energy is transferred to the "1" winding. Current (Trace C) will continue to flow in the "N" winding due to leakage inductance. A snubber network suppresses the effects of this leakage inductance. For lowest snubber losses the specified tapped inductor is bifilar wound for maximum coupling.

Post Regulation-Fixed Case

In most instances the LT1074 output will be applied directly to the load. Those cases requiring faster transient response or reduced noise will benefit from linear post regulation. In Figure 14 a 3-terminal regulator follows the LT1074 output. The LT1074 output is set to provide just enough voltage

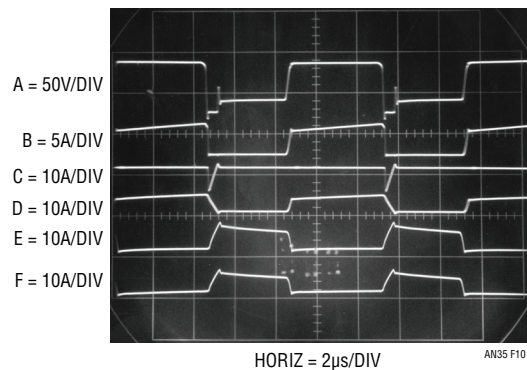


Figure 13. AC Current Flow for the Boosted Regulator

to the LT1084 to maintain regulation. The LT1084's low dropout characteristics combined with a high circuit input voltage minimizes the overall efficiency penalty.

Application Note 35

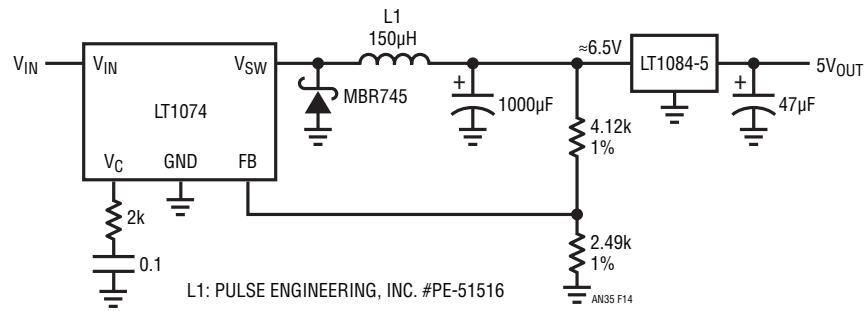


Figure 14. Linear Post-Regulator Improves Noise and Transient Response

Post Regulation-Variable Case

Some situations require variable linear post regulation. Figure 15 does this with little efficiency sacrifice. The LT1085 operates in normal fashion, supplying a variable 1.2V to 28V output. The remainder of the circuit forms a switched mode pre-regulator which maintains a small, fixed voltage across the LT1085 regardless of its output voltage. A1 biases the LT1074 to produce whatever voltage is necessary to maintain the “E diodes” potential across the LT1085. A1’s inputs are balanced when the LT1085 output is “E diodes” above its input. A1 maintains this condition regardless of line, load or output voltage conditions. Thus, good efficiency is maintained over the full range of output voltages. The RC network at A1 compensates the loop. Loop start-up is assured by deliberately introducing a positive offset to A1. This is done by grounding A1’s appropriate balance pin (5), resulting in a positive 6mV offset. This increases amplifier drift, and is normally considered poor practice, but causes no measurable error in this application.

As shown, the circuit cannot produce outputs below the LT1085’s 1.2V reference. Applications requiring output adjustability down to 0V will benefit from option “A” shown on the schematic. This arrangement replaces L1 with L2. L2’s primary performs the same function as L1 and its coupled secondary winding produces a negative bias output ($-V$). The full-wave bridge rectification is necessitated by widely varying duty cycles. A2 and its attendant circuitry replace all components associated with

the LT1085 V_{ADJ} pin. The LT1004 reference terminates the 10k to 250k feedback string at $-1.2V$ with A2 providing buffered drive to the LT1085 V_{ADJ} pin. The negative bias allows regulated LT1085 outputs down to 0V. The $-V$ potential derived from L2’s secondary varies considerably with operating conditions. The high feedback string values and A2’s buffering ensure stable circuit operation for “starved” values of $-V$.

Low Quiescent Current Regulators

Many applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or “sleep” modes draw only microamperes. A typical laptop computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any regulator designed for loop stability under no-load conditions will work. In practice, a converter’s relatively large quiescent current may cause unacceptable battery drain during low output current intervals. Figure 16’s simple loop effectively reduces circuit quiescent current from 6mA to only 150µA. It does this by utilizing the LT1074’s shutdown pin. When this pin is pulled within 350mV of ground the IC shuts down, pulling only 100µA. Comparator C1 combines with the LT1004 reference and Q1 to form a “bang-bang” control loop around the LT1074. The LT1074’s internal feedback amplifier and voltage reference are bypassed by this loop’s operation. When the circuit output (Trace C, Figure 17) falls slightly below 5V C1’s output (Trace A) switches low, turning off Q1 and enabling the

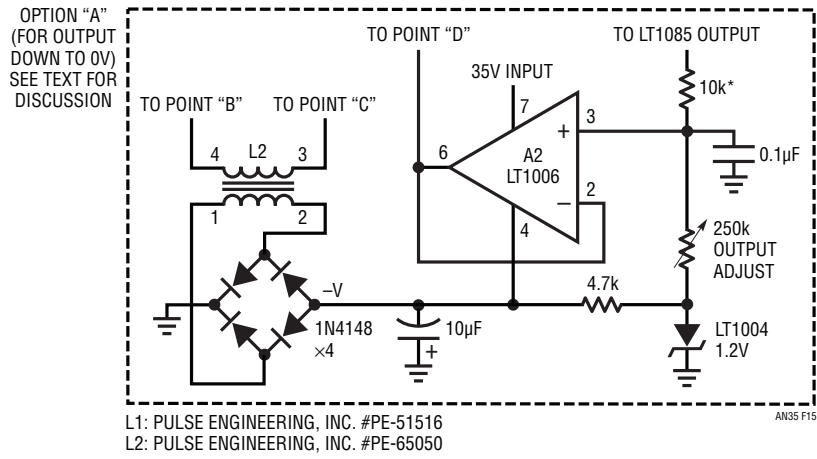
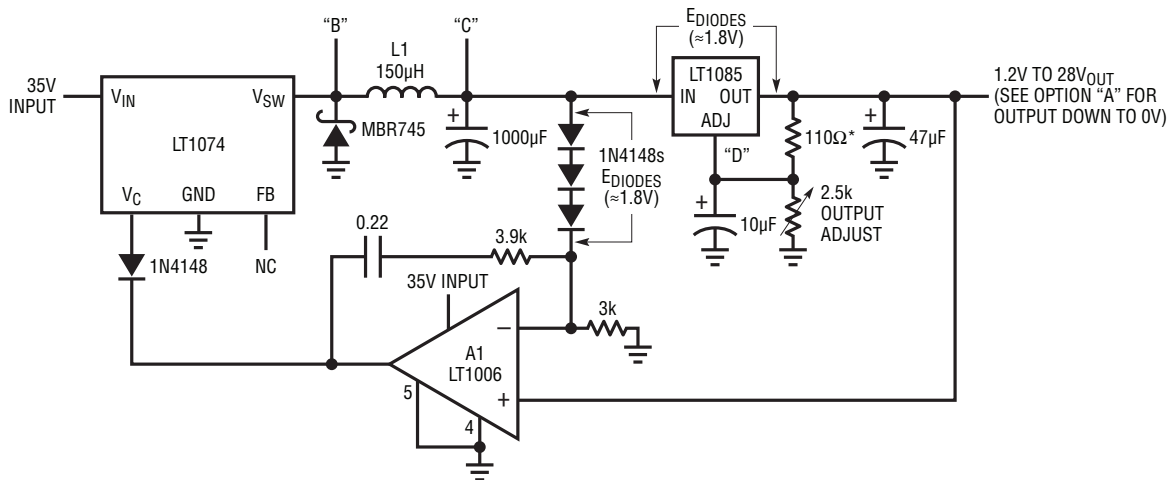


Figure 15. Adjustable Linear Post-Regulator Maintains Efficiency Over Widely Varying Operating Conditions

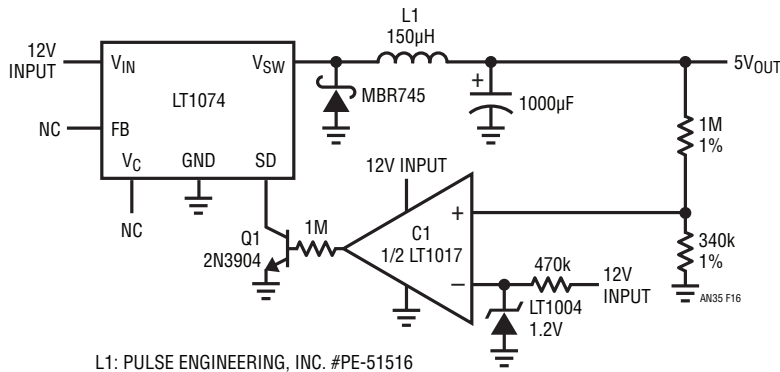


Figure 16. A Simple Loop Reduces Quiescent Current to 150µA

Application Note 35

LT1074. The V_{SW} pin (Trace B) pulses at full duty cycle, forcing the output back above 5V. C1 then biases Q1 again, the LT1074 goes into shutdown, and loop action repeats. The frequency of this on-off control action is directly load dependent, with typical repetition rates of 0.2Hz at no load. Short on-times keep duty cycle low, resulting in the small effective quiescent current noted. The on-off operation combines with the LC filtering action in the regulator's V_{SW} line to generate an output hysteresis of about 50mV (again, see Figure 17, Trace C).

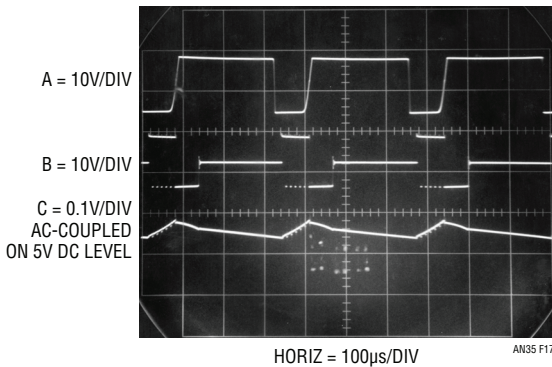


Figure 17. The Low Quiescent Current Loop's Waveforms

The loop performs well, but has two potential drawbacks. At higher output currents the loop oscillates in the 1kHz to 10kHz range, causing audible noise which may be objectionable. This is characteristic of this type of loop, and is the reason that ICs employing gated oscillators invariably produce such noise. Additionally, the control loops operation causes about 50mV of ripple on the output. Ripple frequency ranges from 0.2Hz to 10kHz depending upon input voltage and output current.

Figure 18's more sophisticated circuit eliminates these problems with some increase in complexity. Quiescent current is maintained at 150µA. The technique shown is particularly significant, with broad implication in battery powered systems. It is easily applied to a wide variety of regulator requirements, meeting an acknowledged need across a wide spectrum of applications.

Figure 18's signal flow is similar to Figure 16, but additional circuitry appears between the feedback divider and the LT1074. The LT1074's internal feedback amplifier and reference are not used. Figure 19 shows operating

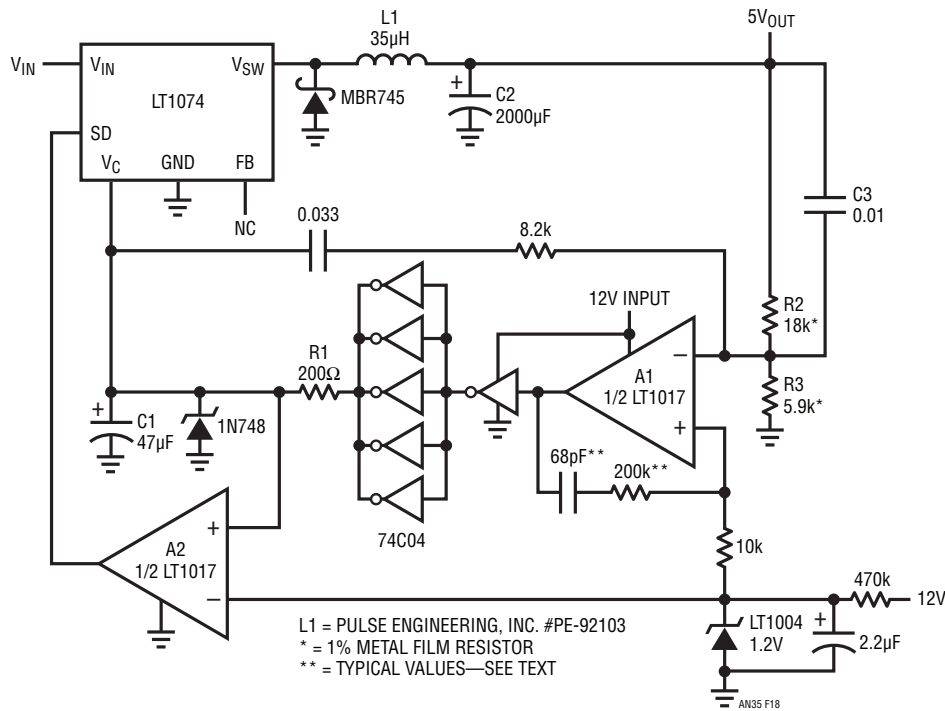


Figure 18. A More Sophisticated Loop Gives Better Regulation While Maintaining 150µA Quiescent Current

waveforms under no-load conditions. The output (Trace A) ramps down over a period of seconds. During this time comparator A1's output (Trace B) is low, as are the 74C04 paralleled inverters. This pulls the V_C pin (Trace D) low, forcing the regulator to zero duty cycle. Simultaneously, A2 (Trace C) is low, putting the LT1074 in its $100\mu\text{A}$ shutdown mode. The V_{SW} pin (Trace E) is off, and no inductor current flows. When the output drops about 60mV , A1 triggers and the inverters go high, pulling the V_C pin up and biasing the regulator. The Zener diode prevents V_C pin overdrive. A2 also rises, taking the IC out of shutdown mode. The V_{SW} pin pulses the inductor at the 100kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back low and shutting off V_{SW} pulsing. A2 also goes low, putting the LT1074 into shutdown.

This “bang-bang” control loop keeps the 5V output within the 60mV ramp hysteresis window set by the loop. Note that the loop oscillation period of seconds means the R1-C1

time constant at V_C is not a significant term. Because the LT1074 spends almost all of the time in shutdown, very little quiescent current ($150\mu\text{A}$) is drawn.

Figure 20 shows the same waveforms with the load increased to 2mA . Loop oscillation frequency increases to keep up with the load's sink current demand. Now, the V_C pin waveform (Trace D) begins to take on a filtered appearance. This is due to R1-C1's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R1-C1 time constant, however, is fixed. Beyond some frequency, R1-C1 must average loop oscillations to DC. At 7mA loading (Figure 21) loop frequency further increases, and the V_C waveform (Trace D) appears heavily filtered.

Figure 22 shows the same circuit points at 2A loading. Note that the V_C pin is at DC, as is the shutdown pin. Repetition rate has increased to the LT1074's 100kHz

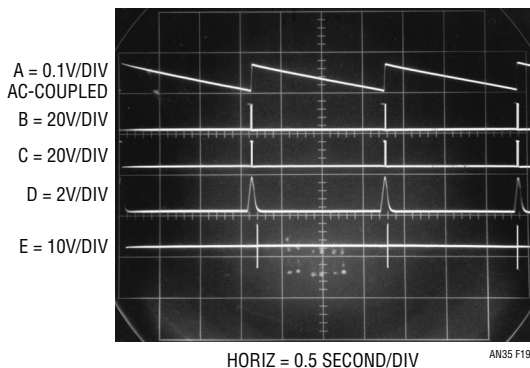


Figure 19. Low Quiescent Current Regulator's Waveforms with No Load (Traces B, C and E Retouched for Clarity)

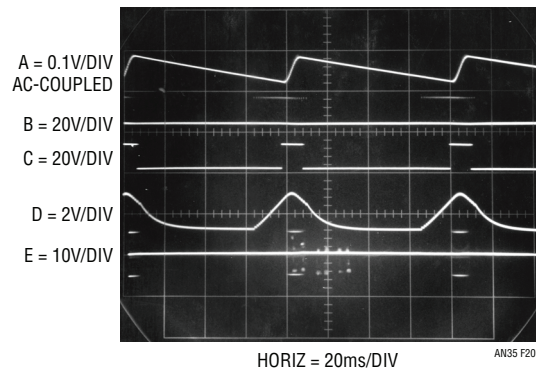


Figure 20. Low Quiescent Current Regulator's Waveforms at 2mA Loading

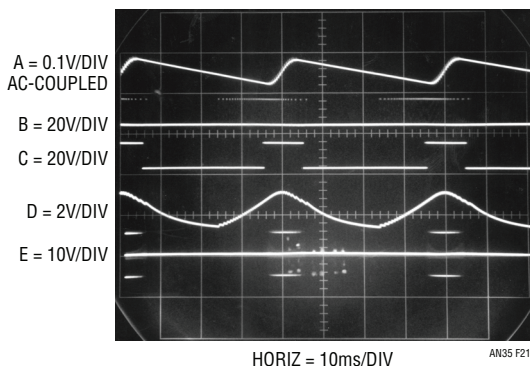


Figure 21. Low Quiescent Current Regulator's Waveforms at 7mA Loading

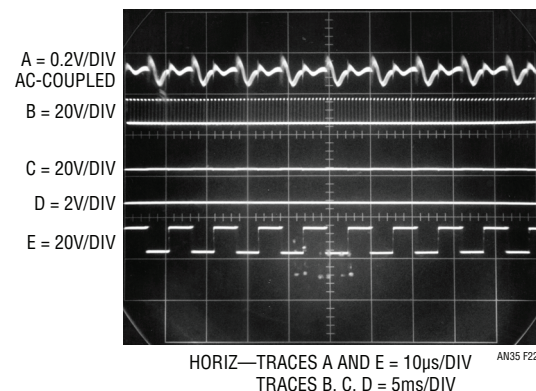


Figure 22. Low Quiescent Current Regulator's Waveforms at 2A Loading

Application Note 35

clock frequency. Figure 23 plots what is occurring, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 23Hz. At this point the R1-C1 time constant filters the V_C pin to DC and the LT1074 transitions into “normal” PWM operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed-loop gain set by the R2-R3 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R1-C1’s break frequency. The phase error contributed by C2 (which was selected for low loop frequency at low output currents) is dominated by the R1-C1 roll off and the C3 lead into A1. The loop is stable and responds linearly for all loads beyond 10mA. In this high current region the LT1074 is desirably “fooled” into behaving like a conventional step-down regulator.

A formal stability analysis for this circuit is quite complex, but some simplifications lend insight into loop operation. At 250 μ A loading (20k Ω) C2 and the load form a decay time constant exceeding 30 seconds. This is orders of magnitude larger than R2-C3, R1-C1, or the LT1074’s 100kHz commutation rate. As a result, C2 dominates the loop. Wideband A1 sees phase shifted feedback, and very low frequency oscillations similar to Figure 19’s occur⁵. Although C2’s *decay* time constant is long, its *charge* time constant is short because the circuit has low sourcing impedance. This accounts for the ramp nature of the oscillations.

Increased loading reduces the C2-load decay time constant. Figure 23’s plot reflects this. As loading increases,

the loop oscillates at a higher frequency due to C2’s decreased decay time. When the load impedance becomes low enough C2’s decay time constant ceases to dominate the loop. This point is almost entirely determined by R1 and C1. Once R1 and C1 “take over” as the dominant time constant the loop begins to behave like a linear system. In this region (e.g., above about 10mA, per Figure 23) the LT1074 runs continuously at its 100kHz rate. Now, C3 becomes significant, performing as a simple feedback lead⁶ to smooth output response. There is a fundamental trade-off in the selection of the C3 lead value. When the converter is running in its linear region it must dominate the loops time lag generated hysteretic characteristic. As such, it has been chosen for the best compromise between output ripple at high load and loop transient response.

Despite the complex dynamics transient response is quite good. Figure 24 shows performance for a step from no load to 1A. When Trace A goes high a 1A load appears across the output (Trace C). Initially, the output sags almost 200mV due to slow loop response time (the R1-C1 pair delay V_C pin (Trace B) response). When the LT1074 comes on response is reasonably quick and surprisingly well behaved considering circuit dynamics. The multi-time constant recovery⁷ (“rattling” is perhaps more appropriate) is visible in Trace C’s response.

Note 5: Some layouts may require substantial trace area to A1’s inputs. In such cases the optional RC network around A1 ensures clean transitions at A1’s output.

Note 6: “Zero Compensation” for all you technosnobs out there.

Note 7: Once again, “multi-pole settling” for those who adore jargon.

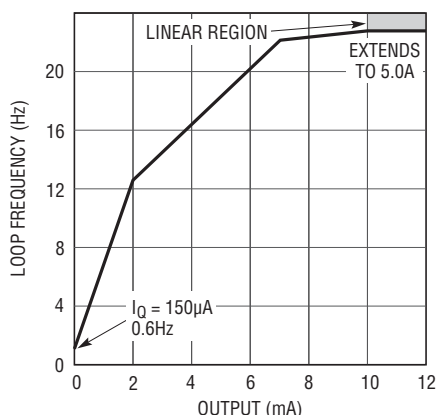


Figure 23. Figure 18’s Loop Frequency vs Output Current. Note Linear Loop Operation Above 10mA

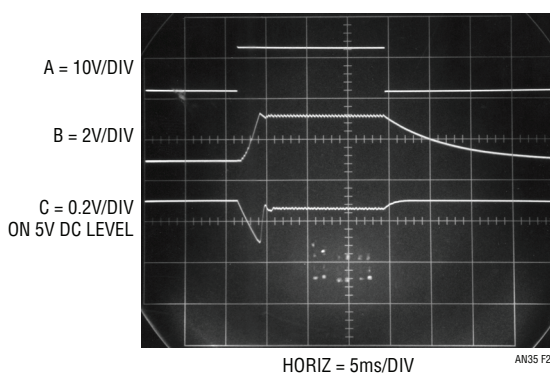


Figure 24. Load Transient Response for Figure 18

Figure 25 plots efficiency versus output current. High power efficiency is similar to standard converters. Low power efficiency is somewhat better, although poor in the lowest ranges. This is not particularly bothersome, as *power* loss is very small.

The loop provides a controlled, conditional instability instead of the usually more desirable (and often elusive) unconditional stability. This deliberately introduced characteristic dramatically lowers converter quiescent current without sacrificing high power performance.

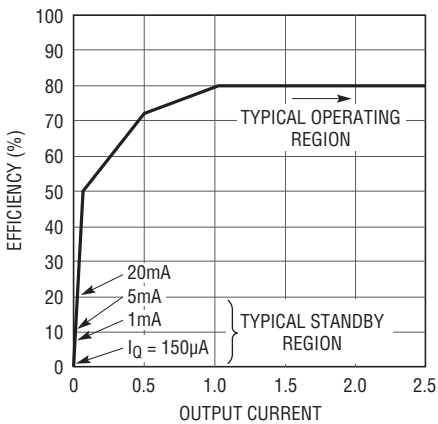


Figure 25. Efficiency vs Output Current for Figure 18. Standby Efficiency is Poor, But Power Loss Approaches Battery Self-Discharge

Wide Range, High Power, High Voltage Regulator

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 26 is an example of the LT1074 making a complex function practical. This regulator provides outputs from millivolts to 500V at 100W with 80% efficiency. A1 compares a variable reference voltage with a resistively scaled version of the circuit's output and biases the LT1074 switching regulator configuration. The switcher's DC output drives

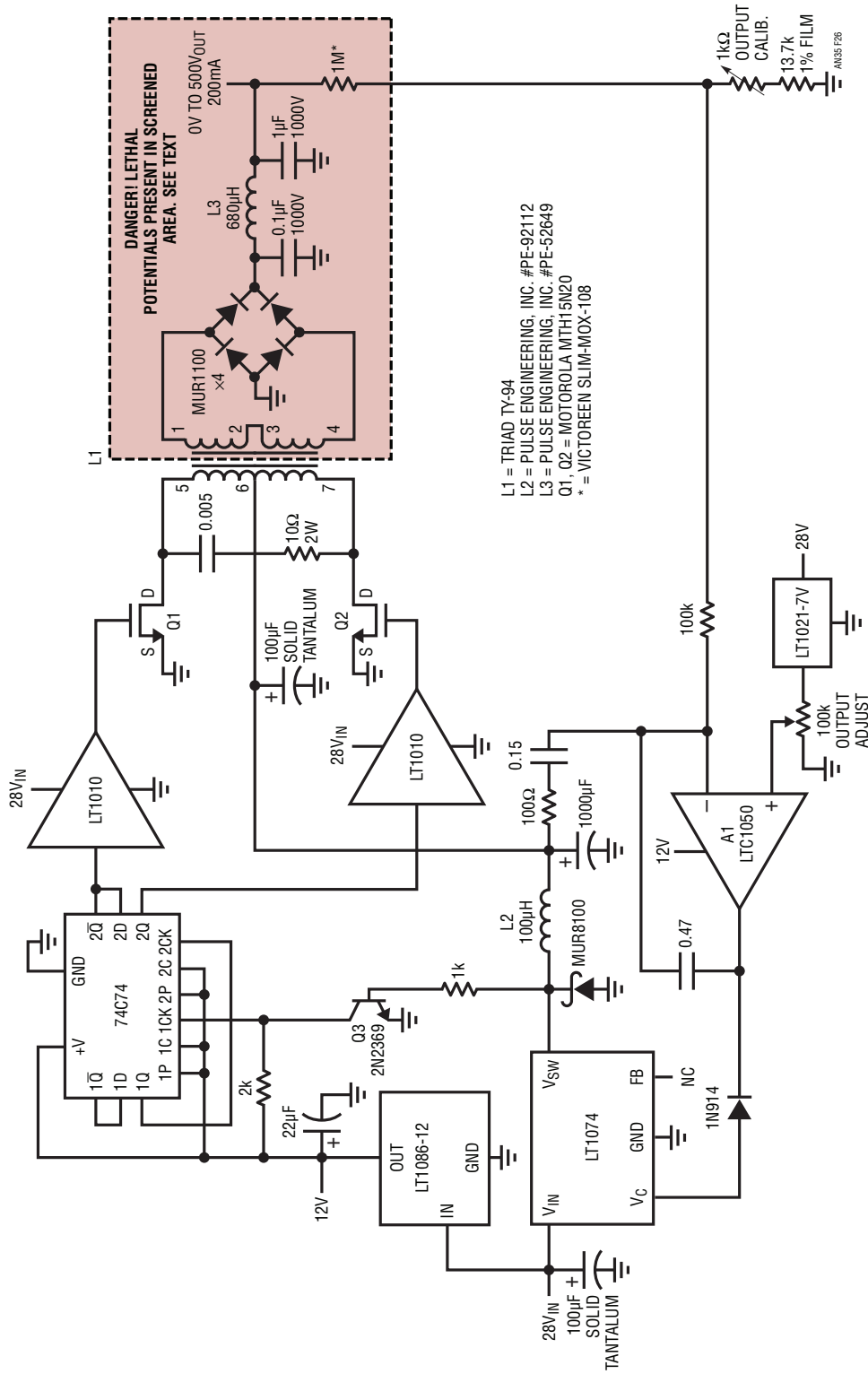
a toroidal DC/DC converter comprised of L1, Q1 and Q2. Q1 and Q2 receive out of phase square wave drive from the 74C74 ÷ 4 flip-flop stage and the LT1010 buffers. The flip-flop is clocked from the LT1074 V_{SW} output via the Q3 level shifter. The LT1086 provides 12V power for A1 and the 74C74. A1 biases the LT1074 regulator to produce the DC input at the DC/DC converter required to balance to loop. The converter has a voltage gain of about 20, resulting in high voltage output. This output is resistively divided down, closing the loop at A1's negative input. Frequency compensation for this loop must accommodate the significant phase errors generated by the LT1074 configuration, the DC/DC converter and the output LC filter. The $0.47\mu\text{F}$ roll-off term at A1 and the 100Ω - $0.15\mu\text{F}$ RC lead network provide the compensation, which is stable for all loads.

Figure 27 gives circuit waveforms at 500V output into a 100W load. Trace A is the LT1074 V_{SW} pin while Trace B is its current. Traces C and D are Q1 and Q2's drain waveforms. The disturbance at the leading edges is due to cross-current conduction, which lasts about 300ns—a small percentage of the cycle. Transistor currents during this interval remain within reasonable values, and no overstress or dissipation problems occur. This effect could be eliminated with non-overlapping drive to Q1 and Q2⁸, although there would be no reliability or significant efficiency gain. The 500kHz ringing on the same waveforms is due to excitation of transformer resonances. These phenomena are not deleterious, although L1's primary RC damper is included to minimize them.

All waveforms are synchronous because the flip-flop drive stage is clocked from the LT1074 V_{SW} output. The LT1074's maximum 95% duty cycle means that the Q1-Q2 switches can never see destructive DC drive. The only condition allowing DC drive occurs when the LT1074 is at zero duty cycle. This case is clearly non-destructive, because L1 receives no power.

Figure 28 shows the same circuit points as Figure 27, but at only 5mV output. Here, the loop restricts drive to the DC/DC converter to small levels. Q1 and Q2 chop just 70mV into L1. At this level L1's output diode drops look large, but loop action forces the desired 0.005V output.

Note 8: For an example of this technique see LTC Application Note 29, Figure 1.



L1 = TRIAD TY-94
 L2 = PULSE ENGINEERING, INC. #PE-92112
 L3 = PULSE ENGINEERING, INC. #PE-52649
 Q1, Q2 = MOTOROLA MTH15N20
 * = VICTOREEN SLIM-MOX-108

Figure 26. LT1074 Permits High Voltage Output Over 100dB Range with Power and Efficiency. DANGER! Lethal Potentials Present—See Text

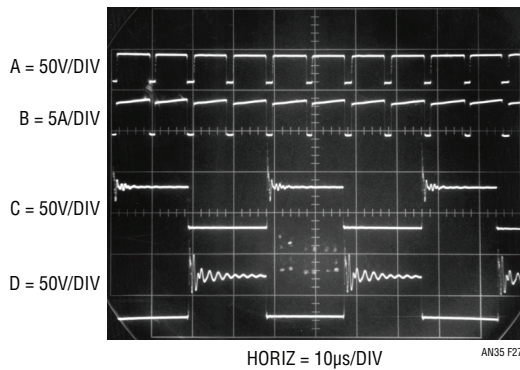


Figure 27. Figure 26's Operating Waveforms at 500V Output into a 100W Load

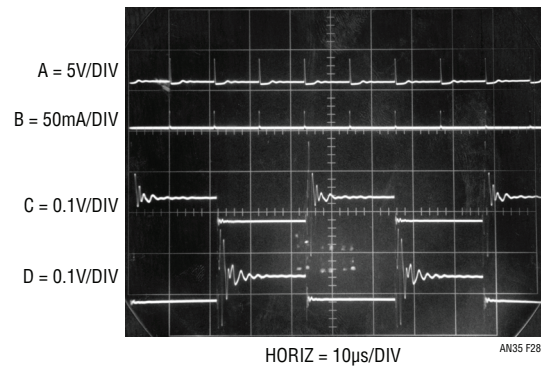


Figure 28. Figure 26's Operating Waveforms at 0.005V Output

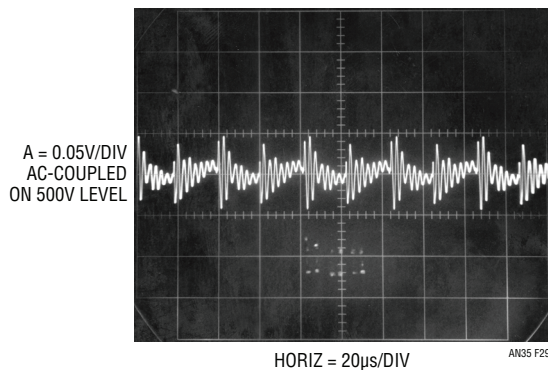


Figure 29. Figure 26's Output Noise at 500V into a 100W Load. Residue is Composed of Q1-Q2 Chopping Artifacts and Transformer Related Ringing. **DANGER! Lethal Potentials Present—See Text**

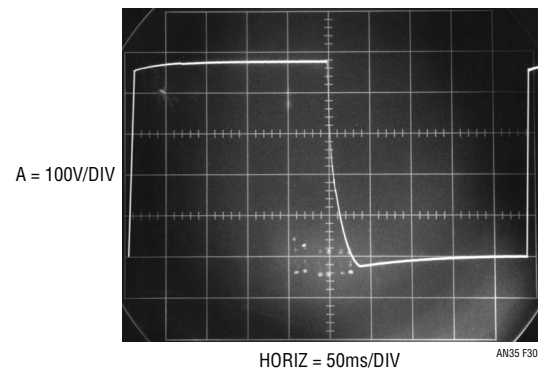


Figure 30. 500V Step Response with 100W Load (Photo Retouched for Clarity). **DANGER! Lethal Potentials Present—See Text**

The LT1074's switched mode drive to L1 maintains high efficiency at high power, despite the circuit's wide output range⁹.

Figure 29 shows output noise at 500V into a 100W load. Q1-Q2 chopping artifacts and transformer-related ringing are clearly visible, although limited to about 80mV. The coherent noise characteristic is traceable to the synchronous clocking of Q1 and Q2 by the LT1074.

A 50V to 500V step command into a 100W load produces the response of Figure 30. Loop response on both edges

is clean, with the falling edge slightly underdamped. This slew asymmetry is typical of switching configurations, because the load and output capacitor determine negative slew rate. The wide range of possible loads mandates a compromise when setting frequency compensation. The falling edge could be made critically or even overdamped, but response time for other conditions would suffer. The compensation used seems a reasonable compromise.

Note 9: A circuit related to the one presented here appears in the LTC Application Note 18 (Figure 13). Its linear drive to the step-up DC/DC converter forces dissipation, limiting output power to about 15W. Similar restrictions apply to Figure 7 in Application Note 6.

Regulated Sinewave Output DC/AC Converter

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT, EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 31 is another example of the LT1074 permitting the practical implementation of a complex function. It converts a 28V DC input to a regulated 115V_{AC} 400Hz sinewave output with 80% efficiency. Waveform distortion is below 1.6% at 50W output. This design shares similarities with the previous circuit. The LT1074 supplies efficient drive to a high voltage converter despite large line and load variations. An amplifier (A1) controls the input to the high voltage converter via A2 and the LT1074 switching regulator. The high voltage output is divided down and fed back to the amplifier where it is compared to a reference to close a loop. In the previous circuit the output is DC; here the output is AC. As such, A1's reference (Trace A, Figure 32) is an amplitude and frequency stabilized 800Hz half-sine¹⁰. The high voltage converter is driven from a flip-flop clocked by a reference synchronized pulse (negative going excursions just visible in Trace B) via level shift transistor Q3. The reference synchronized pulse occurs at the zero voltage point of the half-sine. The flip-flop outputs (Traces C and D, respectively) drive the Q1 and Q2 gates. RC filters in the gate line retard the drive's slew rate.

A1 biases the LT1074's V_C pin via A2 to produce an 800Hz half-sine signal at L2's center tap (Trace E). Because Q1 and Q2 are synchronously driven with the reference half-sine their drain waveforms (Traces F and G) reveal alternate chopping of complete half cycles. L2 receives balanced drive and its secondary recombines the chopped half-sines into a 115V_{AC} 400Hz sinewave output (Trace H). The diode bridge rectifies L2's output back to an 800Hz half-sine which is fed to A1 via the resistor divider. A1 balances this signal against the reference half-sine to close a loop. Transmitting the 800Hz waveform around the loop requires attention to available bandwidth. The LT1074's 100kHz switching frequency is theoretically high enough to permit this, but the bandwidth attenuation of its output LC filter must be

considered. The unusually low output filter capacitor value allows the necessary frequency response. A1's 330k-0.01μF components combine with the RC lead network across the 16k feedback resistor to stabilize the loop.

A2 closes a local loop around the LT1074 configuration. This is necessary because L2 blocks DC information from being conducted around A1's loop. This is a concern because the waveform presented to L2's primary center tap must have no DC component. DC content at this point will cause waveform distortion, transformer power dissipation or both. The LT1074's V_C pin operates with substantial and uncertain DC bias, making A1's inability to control DC errors unacceptable. A2 corrects this by biasing the LT1074 V_C pin at its DC threshold so that no DC component is presented to L2. A1's output represents the difference between the AC-coupled circuit output and the half-sine reference. A2's output contains this information in addition to DC restoration information. L2 and A1 contribute essentially no DC error, so A2's loop may be closed at the LT1074 configuration's output. A2's feedback capacitor stabilizes this local loop.

The drive to L2 cannot sink current. This means that any residual energy stored in L2 when the drive waveform goes to zero sees no exit path. This is a relatively small effect, but can cause output crossover distortion. The synchronous switch option shown on the schematic provides such a path, and is recommended for lowest output distortion. This optional circuitry is detailed in Appendix E.

Figures 33a and 33b show waveforms in the "turnaround" region of circuit operation. This is the most critical part of the converter, and its characteristics directly determine output waveform purity. Figure 33a (Trace A), a highly amplitude and time expanded version of L2's center tap drive, arrives at 0V (upper cross-etched horizontal line) and turns around cleanly. This action is just slightly time skewed from the reference synchronized pulse (Trace B). The aberration on the rising edge is due to the optional synchronous switch's operation. This switch is shorted during the on-time of Trace C's pulse (see Appendix E for operating details of this option). Trace D, Q2's gate drive, aligns with Trace B's pulse. The slew reduction caused by

Note 10: Complete operating details of the half-sine reference generator appear in Appendix E.

Application Note 35

the 1k-0.01 μ F filter is clearly visible, and contributes to Trace A's low noise turnaround. The LT1074's 100kHz chopping related components are easily observed in Trace A. Waveforms at the next half cycle's zero point (e.g., Q1's gate driven) are identical.

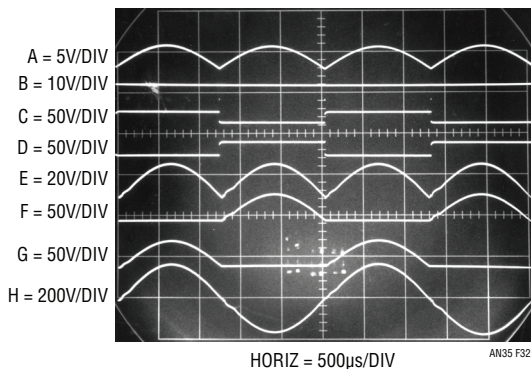


Figure 32. +28 to 110V_{AC}, 400Hz Converter's Waveforms. The Optional Synchronous Switch is Disabled in this Photo, Resulting in Relatively High Crossover Distortion (Trace H). DANGER! Lethal Potentials Present—See Text

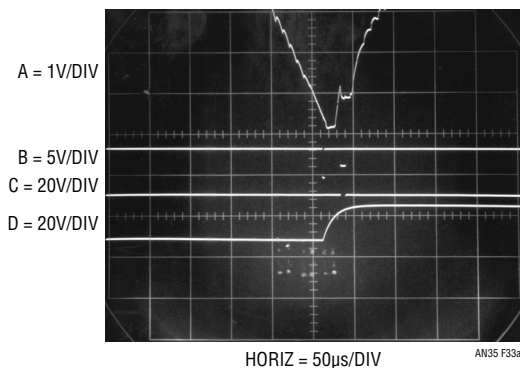


Figure 33a

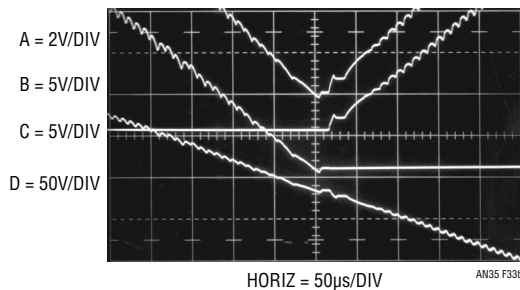


Figure 33b

Figure 33a and 33b. Details of "Turnaround" Sequence. Switching Characteristics Directly Determine Output Crossover Distortion. DANGER! Lethal Potentials Present—See Text

Figure 33b shows additional details at highly expanded amplitude and time scales. L2's center tap is Trace A, Q1's drain is Trace B and Q2's drain Trace C. The output sine wave (Trace D) is shown as it crosses through zero.

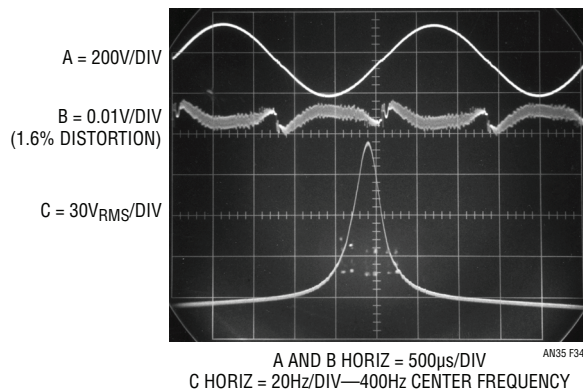


Figure 34. Distortion and Spectral Characteristics for the Sinewave Output Converter. Distortion Trace (B) Shows Crossover Aberrations and the LT1074 Wideband Chopping Residue. The Synchronous Switch Option is Employed in this Photo for Lowest Distortion. DANGER! Lethal Potentials Present—See Text

Figure 34 studies waveform purity. Trace A is the sinewave output at 50W loading. Trace B shows distortion products, which are dominated by turnaround related crossover aberrations and LT1074 100kHz chopping residue. Although not strictly necessary, the LT1074's switching can be synchronized to the reference half-sine for coherent noise characteristics. This option is discussed in Appendix E, along with other reference generator details. Trace C is a spectrum analysis centered at 400Hz¹¹. In this photo the optional synchronous switch is used, accounting for improved crossover characteristics over Figure 32.

If a fully floating output is desired the output diode bridge can be isolated by a simple 1:1 ratio transformer. To calibrate this circuit trim the "output adjust" potentiometer for a 115V_{AC} output. Regulation remains within 1% over wide variations of input and load.

¹¹Test equipment aficionados may wish to consider how this picture was taken. Hint: Double exposure techniques were not used. This photograph is a real time, simultaneous display of frequency and time domain information.

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3. LT1074 Data Sheet, Linear Technology Corporation.
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Note: *This application note was derived from a manuscript originally prepared for publication in EDN magazine.*

APPENDIX A

Physiology of the LT1074

The LT1074 uses standard (as opposed to current mode) pulse width modulation, with two important differences. First, it is a clocked system with a maximum duty cycle of approximately 95%. This allows a controlled start-up when it is used as a positive-to-negative converter or a negative boost converter. Second, duty cycle is an inverse function of input voltage ($DC \approx 1/V_{IN}$), without any change in error amplifier output. This greatly improves line transient response and ripple rejection, especially for designs which have the control loop over-damped.

Referring to the block diagram, the heart of the LT1074 consists of the oscillator, the error amplifier A1, an analog multiplier, comparator C6, and an RS flip-flop. A complete switching cycle begins with the reset (down ramp) period of the oscillator. During this time ($\approx 0.7\mu s$), the RS flip-flop is set and the switch driver Q104 is kept off via the "and" gate G1. At the end of the reset time, Q104 turns on and drives the output switch Q111, Q112 and Q113. The oscillator ramp starts upward, and when it is equal to the output voltage of the analog multiplier, C6 resets the RS flip-flop, turning off the output switch. Duty cycle is therefore controlled by the output of the multiplier which in turn is controlled by the output of the error amplifier, A1.

A multiplier is used in the LT1074 to provide a perfect "feedforward" function. Conventional switching regulators sometimes use a simple form of feedforward to adjust duty cycle immediately when input voltage changes. This reduces the requirement for voltage swing at the output of the error amplifier as it tries to correct for line variations. Bandwidth of switching regulator error amplifiers must be fairly low to maintain loop stability, so rather large output perturbations occur when the output of the error amplifier must move quickly to correct for line variations. Conventional feedforward schemes typically operate well over a restricted input voltage range or are effective only at certain frequencies. The multiplier technique is very effective over the full range of input voltage and at all frequencies. The basic function is to compensate for the generalized buck regulator transfer function; $V_{OUT} = (V_{IN}) (DC)$, where DC = switch duty cycle. This transfer function has two implications. First, it is obvious that to maintain a constant output, duty cycle must change inversely with input voltage. Second, input voltage appears in the loop transfer function, i.e., a fixed variation in duty cycle gives different variations in output voltage depending on input voltage. Loop gain is directly proportional to input voltage,

Application Note 35

and this can cause loop instability or slow loop response if input voltage varies over a wide range. The multiplier takes out all input voltage effects by automatically adjusting loop gain inversely with input voltage. The multiplier output (V_O) is equal to error amplifier output (V_E) divided by input voltage (V_{IN}); $V_O = (V_R) \cdot (V_E)/(V_{IN})$. V_R is a fixed voltage required by all analog multipliers to define multiplier gain. It has an effective value of approximately 20V in the LT1074.

The error amplifier used in the LT1074 is a transconductance type. It has high output impedance ($\approx 500k\Omega$), so that its AC voltage gain is defined by the impedance of external shunt frequency compensation components (Z_C) and the transconductance (g_m) of the amplifier, $A_V = (g_m) (A_C)$. g_m is $\approx 3500\mu\text{mho}$. The error amplifier has its noninverting input committed to an internal 2.3V reference. The inverting input (fb) is brought out for connection to an external voltage divider that establishes regulator output voltage.

Two other connections are made internally to the fb pin. A window comparator consisting of C4, C5, and some logic provides an “output status” function. It monitors the voltage on the fb pin and gives a “high” output only when the fb voltage is within $\pm 5\%$ of the internal reference voltage. This status output can be used to alert external circuitry that the regulator output is “in” or “out” of regulation. The delay and one-shot circuits ensure that switching EMI will not cause spurious outputs, and that the minimum time for an “out-of-bounds” (low) status output is $\approx 20\mu\text{s}$. Also tied to the fb pin is a frequency shift circuit consisting of R15 and Q36. The base of Q36 is biased at $\approx 1\text{V}$ so that Q36 turns on when the fb pin drops below $\approx 0.6\text{V}$. Current through Q36 smoothly decreases oscillator frequency. This is necessary for maintaining control of current limit at high input voltages. A “dead short” on the output of a switching regulator requires that switch “on” time reduce to $(V_D)/(V_{IN})(f)$, where V_D is the forward voltage of the output catch diode and f is switching frequency. V_D is typically 0.5V for a Schottky catch diode, forcing switch “on” time to shrink to a theoretical 0.1 μs for a 50V input and 100kHz switching frequency with a shorted output. In practical circuits, effective “on” time can stretch to 0.3 μs under these conditions due to losses in the inductor wire resistance and switch rise and fall time. The LT1074

cannot reduce switch “on” time to less than $\approx 0.6\mu\text{s}$ in current limit because it has true pulse-by-pulse switch current limiting. The current limit circuitry must sense switch current *after* the switch turns on, and then send a signal to turn the switch off. Minimum time for this signal path is 0.6 μs . Full control of current limit is maintained by reducing switching frequency when the output falls to less than approximately 15% of its regulated value. This has no effect on normal operation and does not change the selection of external components such as the inductor or output capacitor.

True pulse-by-pulse current limiting is performed by comparator C7. It monitors the voltage across sense resistor R52 and resets the RS flip-flop. Current limit threshold is set by the voltage across R47 which in turn is set by the voltage on the I_{LIM} pin. The I_{LIM} voltage is determined by an external resistor or by an internal clamp of 5V if no external resistor is used. To compensate for the temperature coefficient of R47 ($\approx +0.25\%/^{\circ}\text{C}$), the internal current source I_L has a matching positive temperature coefficient. Its nominal value is 300 μA at 25 $^{\circ}\text{C}$. Current limit can be set from 1A to 6A with one external resistor between I_{LIM} and ground. If no resistor is used, the I_{LIM} pin will self clamp at $\approx 5\text{V}$ and current limit will be $\approx 6.5\text{A}$. A small pre-bias is added to the negative input of C7 to ensure that current limit will go to zero (no switching) when the I_{LIM} pin is pulled to 0V, either by an external short or via Q11 during undervoltage lockout. Soft-start can be achieved by connecting a capacitor to the I_{LIM} pin. Foldback current limiting can also be implemented by connecting a resistor from I_{LIM} to the regulated output.

Switching frequency of the LT1074 is internally set at 100kHz, but can be increased by connecting a resistor from the frequency pin to ground. This resistor biases on Q79 and feeds extra current into the oscillator. Maximum suggested frequency is 200kHz. A comparator, C3, is also connected to the frequency pin and allows this pin to be used for synchronizing the oscillator to an external clock, even when the pin is also being used to boost oscillator frequency. R35 keeps the frequency pin biased correctly in a no-function state when it is left open and R36 limits Q79 current if the frequency pin is accidentally shorted to ground.

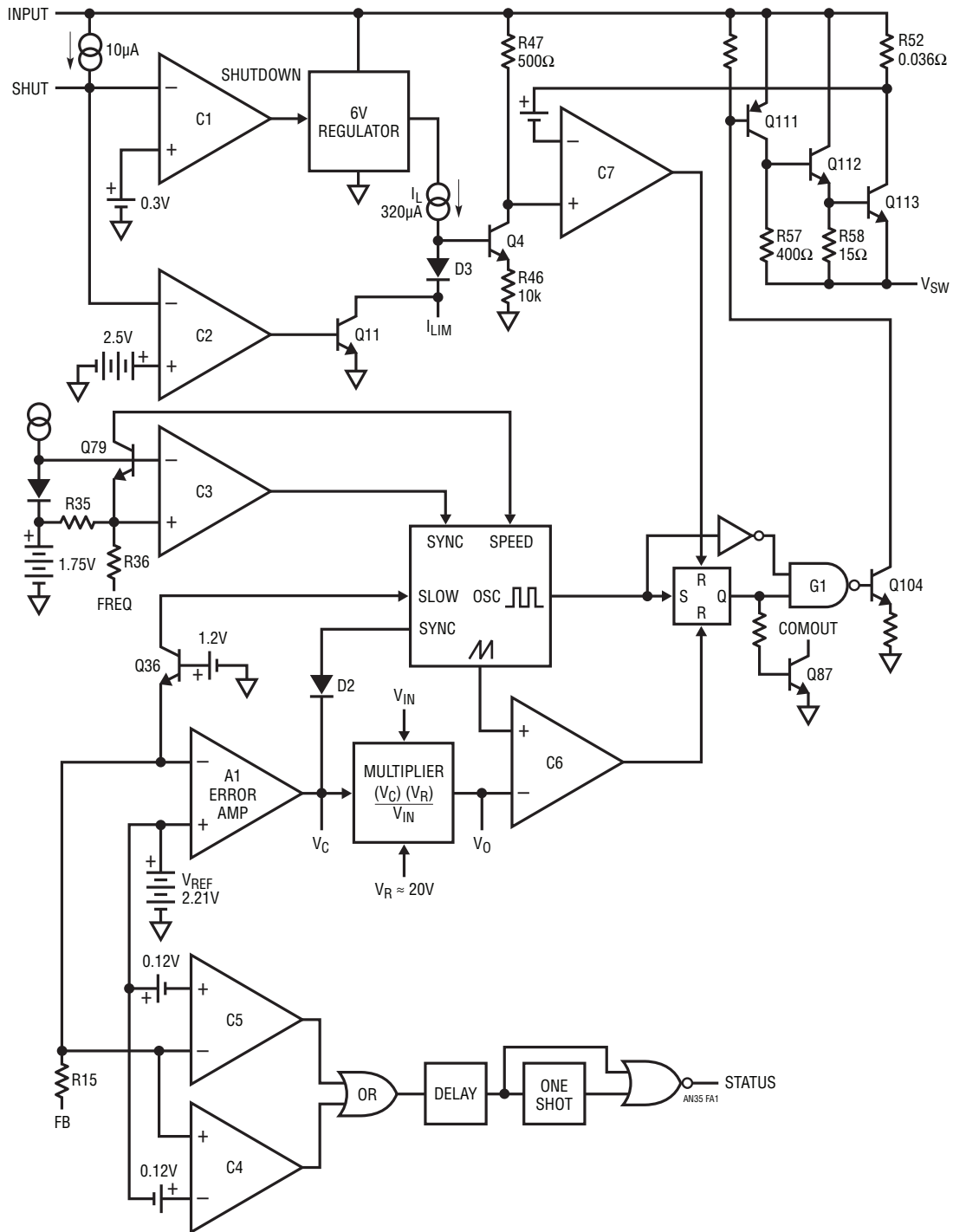


Figure A1. Simplified LT1074 Internal Details

Application Note 35

The shutdown pin on the LT1074 can be used as a logic control of output switching, as an undervoltage lockout, or to put the regulator into complete shutdown with $I_{SUPPLY} \approx 100\mu A$. Comparator C2 has a threshold of 2.5V. It forces the output switch to a 100% “off” condition by pulling the I_{LIM} pin low via Q11. Undervoltage lockout is implemented through C2 by connecting the tap of an input voltage divider to the shutdown pin. Full micropower shutdown of the regulator is achieved by pulling the shutdown pin below the 0.30V threshold of C1. This turns off the chip by shutting down the internal 6V bias supply. An internal $10\mu A$ current source pulls the shutdown pin high (inactive) if it is left open.

The Comout pin is an open-collector NPN whose collector voltage is the complement of the switch output (V_{SW}). Q87 is specified to drive up to 10mA and 30V. It is intended to drive the gate of an external N-channel MOS switch which is in parallel with the catch diode. The MOS switch then acts as a synchronous rectifier, which can significantly improve converter efficiency in low output voltage applications. The Comout pin can also be used to drive the gate of an external P-channel MOS switch in parallel with

the internal bipolar switch to provide ultrahigh efficiency switching at lower input voltages. A slight time-shift in the Comout signal prevents switch overlap problems.

The combination of these features produces a DC/DC converter with the electrical characteristics shown in Figure A2.

PARAMETER	CONDITIONS	UNITS
Input Voltage Range		4.5V to 60V
Output Voltage Range		2.5V to 50V
Output Current Range	Standard Buck Tapped Buck	0A to 5A 0A to 10A
Quiescent Input Current		7mA
Switching Frequency		100kHz to 200kHz
Switch Rise/Fall Times		50ns
Switch Voltage Loss	1A 5A	1.6V 2V
Reference Voltage		2.35V \pm 1.5%
Line/Load Regulation		0.05%
Efficiency	$V_{OUT} = 15V$ $V_{OUT} = 5V$	90% 80%

Figure A2. LT1074 Electrical Characteristics

APPENDIX B

GENERAL CONSIDERATIONS FOR SWITCHING REGULATOR DESIGN

Inductor Selection

Magnetic considerations are easily the most common problem area in switching regulator design. Ninety percent of the difficulties encountered are traceable to the inductive components in the circuit. The overwhelming level of difficulty associated with magnetics mandates a judicious selection process. The most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to address inductor selection. It permits real-time analysis under actual circuit operating conditions using the ultimate simulator—a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure B1 shows a typical step-down converter utilizing the LT1074 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit¹² shown in Figure B2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure B1.

Note 12: Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, California 92112, 619-268-2400.

Figure B3 was taken with a 450 μ H value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1074's V_{SW} pin voltage while Trace B shows its current. When V_{SW} pin voltage is high, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure B4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure B5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure B6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce

acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

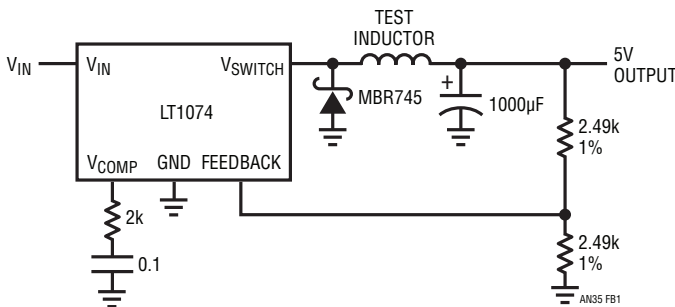


Figure B1. Basic LT1074 Test Circuit

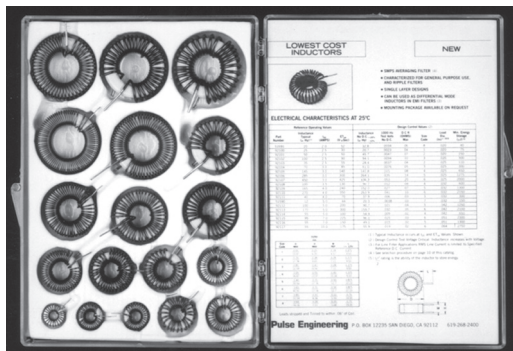


Figure B2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. Includes 18 Fully Specified Devices

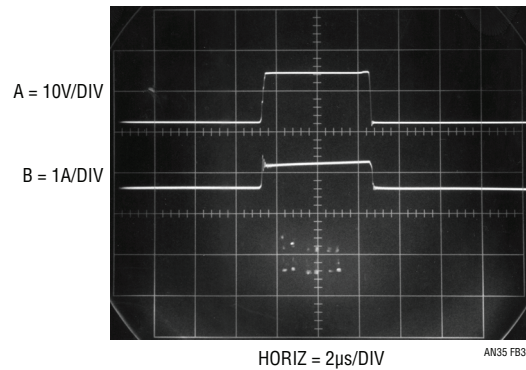


Figure B3. Waveforms for 450 μ H, High Capacity Core Unit

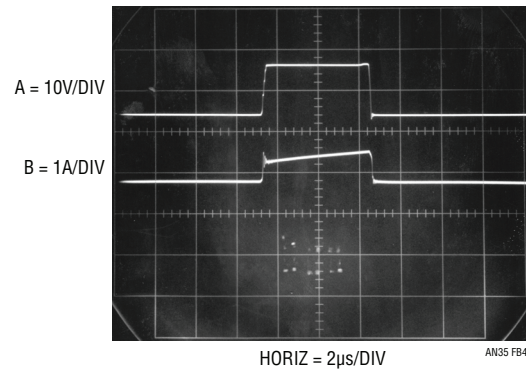


Figure B4. Waveforms for 170 μ H, High Capacity Core Unit

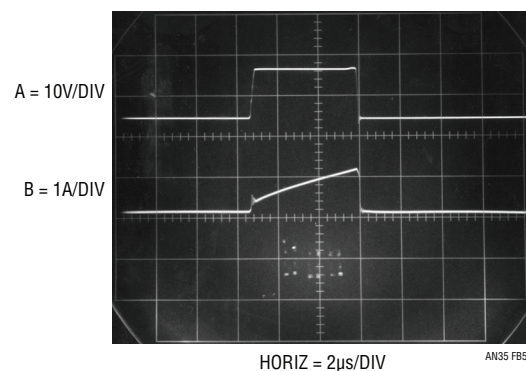


Figure B5. Waveforms for 55 μ H, High Capacity Core Unit

Application Note 35

Inductor Selection—Alternate Method

There are alternate inductor selection methods to the one described. One of the most popular is utilized by those devoid of the recommended inductor kit, time or adequate instrumentation. What is usually desired is to get a prototype LT1074 circuit running *NOW*. What is often available is limited to a drawer of inductors (see Figure B7) of unknown or questionable lineage. Selection of an appropriate inductor is (hopefully) made by simply inserting one of these drawer dwellers into an unsuspecting LT1074 circuit. Although this method's theoretical premise is perhaps questionable, its seemingly limitless popularity compels us to address it. We have developed a 2-step procedure for screening inductors of unknown characteristics. Inductors passing both stages of the test have an excellent chance (75%—based on our sample of

randomly selected inductors) of performing adequately in a prototype LT1074 circuit. The only instrumentation required is an ohmmeter and a scale.

Test 1 consists of weighing the candidate inductor. Acceptable limits range between 0.01 and 0.25 pounds. This test is best performed at an Inductor Test Facility (see Figure B8), where precision scales are readily available. To save time the quick checkout line is recommended (but only if you have nine¹³ inductors or less—no cheating).

Figure B9 shows an inductor under test. The 0.13 pound weight indicated by the scale places this unit well within acceptable limits.

Note 13: The maximum permitted number of items in the quick checkout line varies from facility to facility. Please be familiar with and respect local regulations.

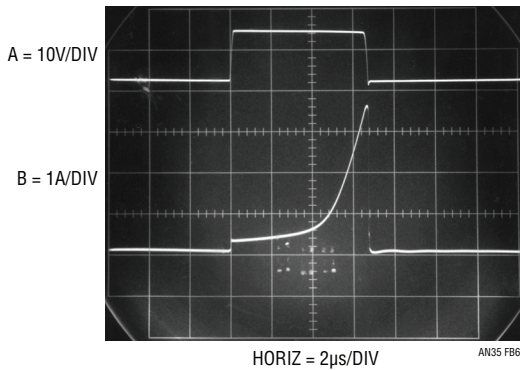


Figure B6. Waveforms for 500µH, Low Capacity Core Inductor (Note Saturation Effects)



Figure B7. “Yeah, We Got Some Inductors in a Drawer. I’m Sure They’ll Work...”



Figure B8. Typical Inductor Test Facility



Figure B9. Inductor Under Test (Don’t Forget to Pick Up a Loaf of Bread and a Dozen Eggs)

The second test involves measuring the inductors DC resistance. Acceptable limits are usually between 0.01Ω and 0.25Ω . Inductors passing both tests will probably function in a prototype LT1074 circuit. Figures B10 and B11 show typical acceptable and unacceptable inductors. Graduates tend to be relatively dense, with (where visible) thick wire. Flunkers are usually less dense, with small (again, where visible) wire sizes.

When using an inductor selected with this method try low power first, then gradually increase loading. Observe inductor and LT1074 heating, making sure their dissipation is reasonable (warm to the touch). Disproportionate increases in heating as load is increased probably indicate inductor saturation. Either reduce the load, or go back to the drawer and try again.

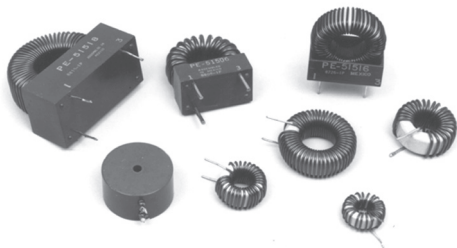


Figure B10. Typical Acceptable Inductors

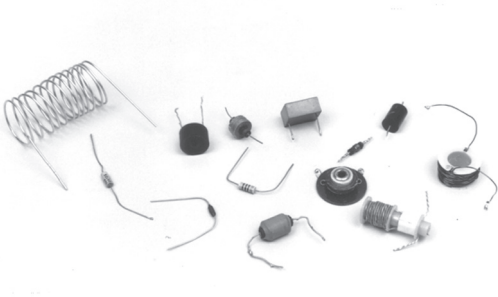


Figure B11. Typical Unacceptable Inductors

While these two tests are somewhat lacking in rigor they do increase the chances of quickly getting a circuit to run with available components. In the longer term, the appropriate inductor can be decided upon and specified.

For the theoretically minded, test 1 grades out inductors which are unlikely to have enough flux storage capability (core mass) to avoid saturation. Test 2 eliminates units with too high a resistance to efficiently support typical LT1074 operating currents. Expanded discussion and design considerations for inductors will be found in Reference 4.

Capacitors

Think about requirements in capacitors. All operating conditions should be accounted for. Voltage rating is the most obvious consideration, but remember to plan for the effects of equivalent series resistance (ESR) and inductance. These specifications can have significant impact on circuit performance. In particular, an output capacitor with high ESR can make loop compensation difficult or decrease efficiency.

Layout

Layout is vital. Don't mix signal, frequency compensation, and feedback returns with high current returns. Arrange the grounding scheme for the best compromise between AC and DC performance. In many cases, a ground plane may help. Account for possible effects of stray inductor-generated flux on other components and plan layout accordingly.

Diodes

Diode breakdown and switching ratings must be thought through. Account for all conditions. Transient events usually cause the most trouble, introducing stresses that are often hard to predict. Study the data sheet breakdown, current capacity, and switching speed ratings carefully. Were these specifications written under the same conditions that your circuit is using the device in? If in doubt, consult the manufacturer.

Switching diodes have two important transient characteristics—reverse recovery time and forward turn-on time.

Application Note 35

Reverse recovery time occurs because the diode stores charge during its forward conducting cycle. This stored charge causes the diode to act as a low impedance conductive element for a short period of time after reverse drive is applied. Reverse recovery time is measured by forward biasing the diode with a specified current, then forcing a second specified current backwards through the diode. The time required for the diode to change from a reverse conducting state to its normal reverse non-conducting state is reverse recovery time. Hard turn-off diodes switch abruptly from one state to the other following reverse recovery time. They therefore dissipate very little power even with moderate reverse recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable diode dissipation during the turn-off interval.

Fast diodes can be useless if stray inductance is high in the diode, output capacitor or LT1074 loop. 20-gauge hook-up wire has 30nH/inch inductance. Switching currents on the order of 10^8 A/sec are typical in regulator circuits. They can easily generate volts per inch in wiring. Keep the diode, capacitor and LT1074 input/switch lead lengths *SHORT!*

Frequency Compensation

The basic LT1074 step-down configuration is relatively free of frequency compensation difficulties. The simple RC damper networks shown from the V_C pin to ground will usually suffice. Things become more complex when gain and phase contributing elements are added to the basic loop. In these cases it is often useful to look at the LT1074 as a low bandwidth power stage. The delays are due to the sampled data nature of power delivery (100kHz switching frequency) and the output LC filter. In general, complex loops can be stabilized by limiting the gain bandwidth of the LT1074 below that of the added elements. This is in accordance with well know feedback theory. A discussion of practical techniques for stabilizing such loops, "The Oscillation Problem (Frequency Compensation Without Tears)," appears at the end of LTC Application Note 18. Other pertinent comments appear in the "Frequency Compensation" sections of LTC Application Notes 19 and 25.

APPENDIX C

Techniques and Equipment for Current Measurement

Accurate measurement of current flow under rapidly changing circuit conditions is essential to switching regulator design. In many cases current waveforms contain more valuable information than voltage measurements. The most powerful and convenient current measuring tool is the clip-on current probe. Several types appear in Figure C1. The Tektronix P-6042, shown bottom left, is a Hall effect stabilized current transformer which responds from DC to 50MHz. The more recent Tektronix AM-503 (not shown) has similar specifications. The combination of convenience, broad bandwidth and DC response make Hall effect stabilized current probes the instrument of choice for converter design. The DC response allows determination of DC content in high speed current waveforms. The clip-on probe contains a current transformer and a Hall effect device. The Hall device senses at DC and low frequency while the transformer simultaneously processes high frequency content. Careful roll-off matching allows

a composite output with no peaking or response aberrations at the two sensors bandwidth crossover. Sensitivity ranges from fractions of a milliampere to amperes and is switch selectable.

Transformer based clip-on current probes are also available. These types lack the DC response of their Hall effect augmented cousins, but are still quite useful. The Tektronix type 131 (and the more modern 134) responds from hundreds of hertz to about 40MHz. AC current probes (type 131 appears in C1, upper left) are as convenient to use as Hall types, but cannot respond at low frequency. AC current probes are also available with a simple termination (left foreground, Figure C1). These types are more difficult to use than the actively terminated models (e.g., type 131 shown) because of complex gain switching. Their low frequency limitations are also poorer, although their high frequency response exceeds 100MHz.

A final form of AC current probe is the simple transformer shown in Figure C1's foreground. These are not clip-on devices, and usually have significant performance limitations compared to the instruments discussed. However, they are inexpensive and can provide meaningful measurement results when used according to manufacturers' recommendations. In use, the conductor is threaded through the opening provided and the signal monitored at the output pins.

Figure C1 also shows a wide ranging DC clip-on current probe. The Hewlett-Packard 428B (upper right) responds from DC to only 400Hz, but features 3% accuracy over a 100 μ A to 10A range. This instrument obviously cannot discern high speed events, but is invaluable for determining overall efficiency and quiescent current.



Figure C1. Various Current Probe Types Provide Different Capabilities. Selection Criteria is Application Dependent

A great strength of the probes described is that they take a fully floating measurement. The extraction of current information by magnetic connection eliminates common mode voltage considerations. Additionally, the clip-on convenience makes the probes as easy to use as a standard voltage mode probe. As good as they are, current probes have limitations and characteristics which must be remembered to avoid unpleasant surprises. At high currents, probe saturation limits may be encountered. Resultant CRT waveforms will be corrupted, rendering the measurement useless and confusing the unwary. For Hall types, measurement below a few hundred microamperes is limited by noise, which is much more obvious on the display. Keep in mind that current probes have different signal transit delay times than voltage probes or dissimilar current probes. At high sweep speeds this effect shows up

in multi-trace displays as time skewing between individual channels. The current probes transit time delay can be mentally factored in to reduce error when interpreting the display. Note that active probes have the longest signal transit times, on the order of 25ns.

The AC probes low frequency bandwidth restriction must be kept in mind when interpreting CRT displays. Figure C2 clearly demonstrates this by showing the AC probes inability to follow low frequency. Similarly, remember that the probe's stated bandpass is a -3 dB figure, meaning signal information is not entirely present in the display at this frequency. When working in regions approaching either end of the probe bandpass consider that displayed information may be distorted or incomplete.

There are other ways, albeit less convenient and desirable than clip-on current probes, to measure wideband current signals. Ohm explains that measuring voltage across a resistor gives current. Current shunts (Figure C3 foreground) are low value (for LT1074 circuits 0.1 Ω to

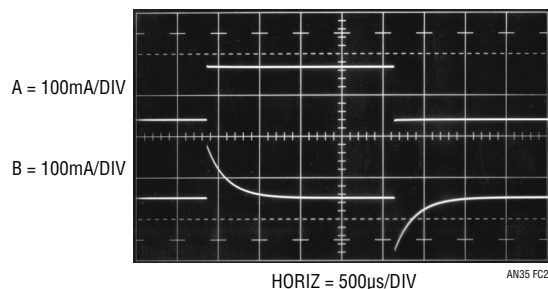


Figure C2. Hall Stabilized (Trace A) and Transformer (Trace B) Based Current Probes Responding to Low Frequency



Figure C3. Typical Current Shunts and an "Isolated" Probe

Application Note 35

0.01Ω is typical) resistors with four terminal connections for accurate measurement. In theory, measuring voltage across a current shunt should yield accurate information. In practice, common mode voltages introduce measurement difficulties, particularly at speed. Making this measurement requires an isolated probe or a high speed differential plug-in. The Signal Acquisition Technologies SL-10 (Figure C3) has 10MHz bandwidth, a galvanically floating input and 600V common mode capability. This probe allows any oscilloscope to take a floating measurement across a shunt.

Differential oscilloscope plug-ins, while not galvanically floating, can measure across a shunt. Tektronix types W, 1A5 and 7A13 have 1mV sensitivity with up to 100MHz bandwidth and excellent common mode rejection. Types 1A7 and 7A22 have 10μV sensitivity, although bandwidth is limited to 1MHz. All differential plug-ins have bandwidth and/or common mode voltage restrictions that vary with sensitivity. These trade-offs must be reviewed when selecting the optimal shunt value for a particular measurement. In general the smallest practical shunt value is desirable. This minimizes the inserted resistances parasitic effects on circuit operation.

APPENDIX D

Optimizing Switching Regulators for Efficiency

Squeezing the utmost efficiency out of a switching regulator is a complex, demanding design task. Efficiency exceeding 80% to 85% requires some combination of finesse, witchcraft and just plain luck. Interaction of electrical and magnetic terms produces subtle effects which influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency is not readily described but some guidelines are possible.

Losses fall into several loose categories including junction, ohmic, drive, switching, and magnetic losses.

Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low voltage output converters. A 700mV drop in a 5V output converter introduces more than 10% loss. Schottky devices will cut this nearly in half, but loss is still appreciable. Germanium (rarely used) is lower still, but switching losses negate the low DC drop at high speeds. In very low power converters Germanium's reverse leakage may be equally oppressive. Synchronously switched rectification is more complex, but can sometimes simulate a more efficient diode (see LTC Application Note 29, Figure 32). The LT1074's "Com Out" pin is intended to drive external synchronous switches. See Appendix A for details.

When evaluating synchronous rectification schemes remember to include both AC and DC drive losses in efficiency estimates. DC losses include base or gate current in

addition to DC consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation (the switch spends some time in its linear region) and power lost due to timing skew between drive and actual switch action.

The LT1074's output switch is composed of a PNP driving a power NPN (Figure D1). The switch drop can reach 2V at high currents. This will usually be the major loss in the circuit. Its effect on efficiency can be mitigated by using the highest possible input voltage. Text Figure 7 shows 5V regulator efficiency improving almost 10% for higher input voltages. Higher output voltages will further minimize the switch losses.

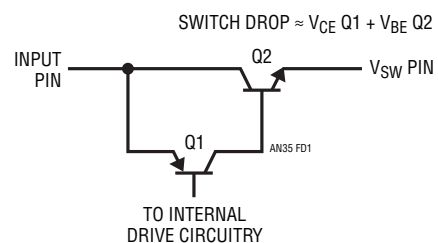


Figure D1. Simplified LT1074 Output Switch

Actual losses caused by switch saturation effects and diode drops are sometimes difficult to ascertain. Changing duty cycles and time variant currents make determination tricky. One simple way to make relative loss judgments is to measure device temperature rise. Appropriate tools here

include thermal probes and (at low voltages) the perhaps more readily available human finger. At lower power (e.g., less dissipation, even though loss percentage may be as great) this technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting efficiency change allows loss determination.

Ohmic losses in conductors are usually only significant at higher currents. “Hidden” ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally drops with capacitor value and rises with operating frequency, and should be specified on the capacitor data sheet. Consider the copper resistance of inductive components. It is often necessary to evaluate trade-offs of an inductor’s copper resistance versus magnetic characteristics.

Switching losses occur when the LT1074 spends significant amounts of time in its linear region relative to operating frequency. At higher switching frequencies transition times can become a substantial loss source. The LT1074’s 100kHz preset switching frequency is a good compromise (for this device) and changes should be carefully considered. Raising the switching frequency to gain some desired benefit necessitates consideration of increased LT1074 losses. 200kHz is the maximum practical operating frequency.

Magnetics design also influences efficiency. Design of inductive components is well beyond the scope of this appended section, but issues include core material selection, wire type, winding techniques, size, operating frequency current levels, temperature and other issues. Some of these topics are discussed in LTC Application Note 19,

but there is no substitute for access to a skilled magnetics specialist. Fortunately, the other categories mentioned usually dominate losses, allowing good efficiencies to be obtained with standard magnetics. Custom magnetics are usually only employed after circuit losses have been reduced to lowest practical levels.

A Special Circuit

In cases where input voltage must be low, but may float, Figure D2’s circuit may be preferable to an LT1074 based approach. This circuit uses the LT1070, a common emitter output device. With the emitter connected to the ground pin this device’s (LT1070 operating details are available in its data sheet, and in LTC Application Notes 19, 25 and 29) switch loss is significantly lower than the LT1074’s. Although intended for voltage step-up in flyback configurations the LT1070 can be arranged to perform the step-down function. The advantage is the efficiency gain due to the reduced switch loss. The circuit’s primary restriction is that the input must float with respect to the output. Q1 performs a level shift to get the feedback information referenced to the LT1070 “ground” pin, which floats with the input. The LT1070 is effectively “fooled” and behaves like a flyback regulator. It is oblivious to the fact that the overall function is step down, because the floating input is driven to the output potential. The negative side of the output filter capacitor is connected to the ground (\ominus) of the powered system, and the LT1070 input rail becomes the 5V output. Other voltages are obtainable by altering the 3.9k – 1.1k feedback ratio. Efficiency approaches 85%.

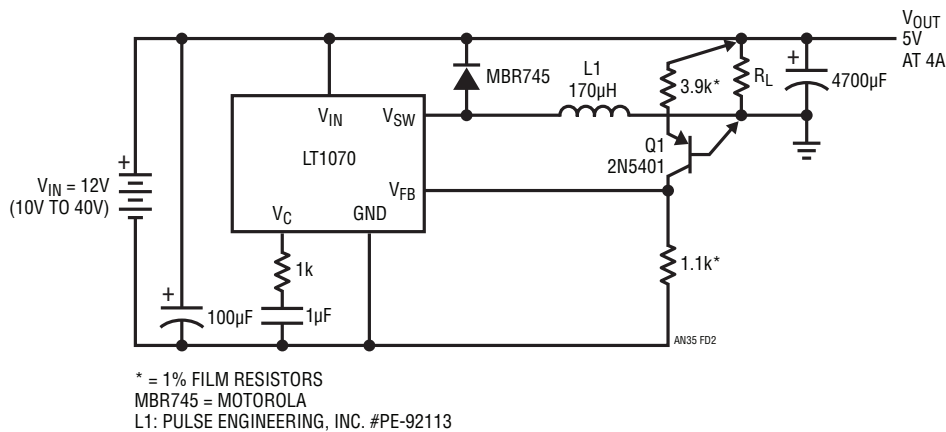


Figure D2. Floating Input Buck Regulator

APPENDIX E

A Half-Sine Reference Generator

Text Figure 31's half-sine reference must be amplitude and frequency stabilized to a fairly high degree. It is not unreasonable to expect a 115V_{AC} 400Hz source to be within 1V and 0.1Hz. Additionally, Figure 31's reference requires a half-sine, as opposed to the more normal full-sine. These requirements are achievable by classical analog techniques, but a digital approach eases complexity with no performance trade-off¹⁴. Figure E3 shows such an approach. C1 forms a 1.024MHz crystal oscillator which is divided down by the 7490. The 7490's differentiated ÷10 output becomes the LT1074's 102.4kHz sync. option output. The 7490's ÷5 output (204.8kHz) is fed to the 74191 counters. These counters parallel load a 2716 EPROM which is programmed to produce an 8-bit (256 states) digitally coded half-sine. The program, developed by Sean Gold and Guy M. Hoover, appears in Figure E1.

The 2716's parallel output is fed to an 8-bit DAC, which produces 800Hz 2.5V (peak) half-sines.

Those wishing to utilize this reference for full-sines will find the appropriate software in Figure E2.

Figure E3 also shows the synchronous switch option discussed in the text. The 74C122 monostable forms a simple delayed pulse generator which drives the Q4 switch. The 20µs delay and 6µs pulse width set at the 74C122 were empirically determined to produce lowest overall crossover distortion in Figure 31's output.

Note 14: The sinewave is probably the paramount expression of the analog world. The Old Man Himself, George A. Philbrick, once elegantly discussed analog functions as "those which are continuous in excursion and time." He might have viewed digital production of a sinewave with considerable suspicion, or simply labeled it blasphemous. Such are the wages of progress.

```

Line 10801  Column  Wrap          APL2/PC
GENCODES
00 03 06 09 0D 10 13 16 19 1C 1F 22 26 29 2C 2F
32 35 38 3B 3E 41 44 47 4A 4D 50 53 56 59 5C 5F
62 65 68 6B 6D 70 73 76 79 7B 7E 81 84 86 89 8C
8E 91 93 96 98 9B 9D A0 A2 A5 A7 A9 AC AE B0 B3
B5 B7 B9 BB BE C0 C2 C4 C6 C8 CA CB CD CF D1 D3
D5 D6 D8 DA DB DD DE E0 E1 E3 E4 E6 E7 E8 EA EB
EC ED EE EF F1 F2 F3 F3 F4 F5 F6 F7 F8 F8 F9 FA
FA FB FB FC FC FD FE FE FE FE FF FF FF FF FF
FF FF FF FF FE FE FE FE FD FD FC FC FB FB FA
FA F9 F8 F8 F7 F6 F5 F4 F3 F3 F2 F1 EF EE ED EC
EB EA E8 E7 E6 E4 E3 E1 E0 DE DD DB DA D8 D6 D5
D3 D1 CF CD CB CA C8 C6 C4 C2 C0 BE BB B9 B7 B5
B3 B0 AE AC A9 A7 A5 A2 A0 9D 9B 98 96 93 91 8E
8C 89 86 84 81 7E 7B 79 76 73 70 6D 6B 68 65 62
5F 5C 59 56 53 50 4D 4A 47 44 41 3E 3B 38 35 32
2F 2C 29 26 22 1F 1C 19 16 13 10 0D 09 06 03 00
    
```

Figure E1. Half-Sine Software Code for the 2716 EPROM

```

Line 10736  Column  Wrap          APL2/PC
GENCODES
FF FF FF FF FE FE FE FD FD FC FB FA F9 F9 F7 F6
F5 F4 F3 F1 F0 EE ED EB E9 E8 E6 E4 E2 E0 DE DC
D9 D7 D5 D2 D0 CE CB C9 C6 C3 C1 BE BB BB B6 B3
B0 AD AA A7 A4 A1 9E 9B 98 95 92 8E 88 88 85 82
7F 7C 78 75 72 6F 6C 69 66 63 60 5A 57 54 51
4E 4B 48 45 42 40 3D 3A 38 35 33 30 2E 2B 29 27
25 22 20 1E 1C 1A 18 17 15 13 11 10 0E 0D 0C 0A
09 08 07 06 05 04 03 03 02 02 01 01 00 00 00 00
00 00 00 00 01 01 02 02 03 03 04 05 06 07 08 09
0A 0C 0D 0E 10 11 13 15 17 18 1A 1C 1E 20 22 25
27 29 2B 2E 30 33 35 38 3A 3D 40 42 45 48 4B 4E
51 54 57 5A 5D 60 63 66 69 6C 6F 72 75 78 7C 7F
82 85 88 8B 8E 92 95 98 9B 9E A1 A4 A7 AA AD B0
B3 B6 B8 BB BE C1 C3 C6 C9 CB CE D0 D2 D5 D7 D9
DC DE E0 E2 E4 E6 E8 E9 EB ED EE F0 F1 F3 F4 F5
F6 F7 F9 F9 FA FB FC FD FD FE FE FE FF FF FF FF
    
```

Figure E2. Full-Sine Software Code for the 2716 EPROM (Bonus)

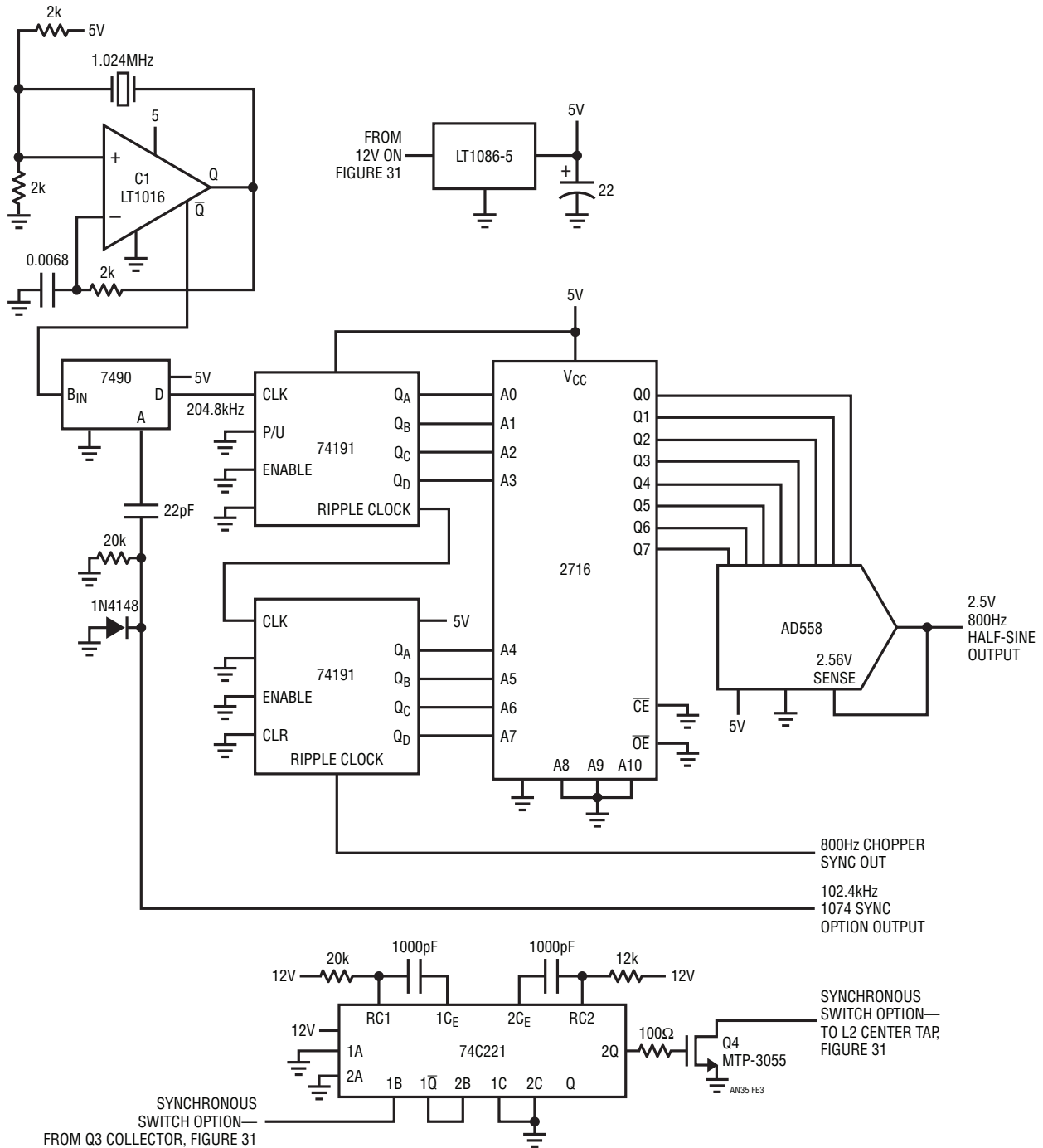


Figure E3. Timing and Reference Half-Sine Generator for Figure 31

APPENDIX F

The Magnetics Issue

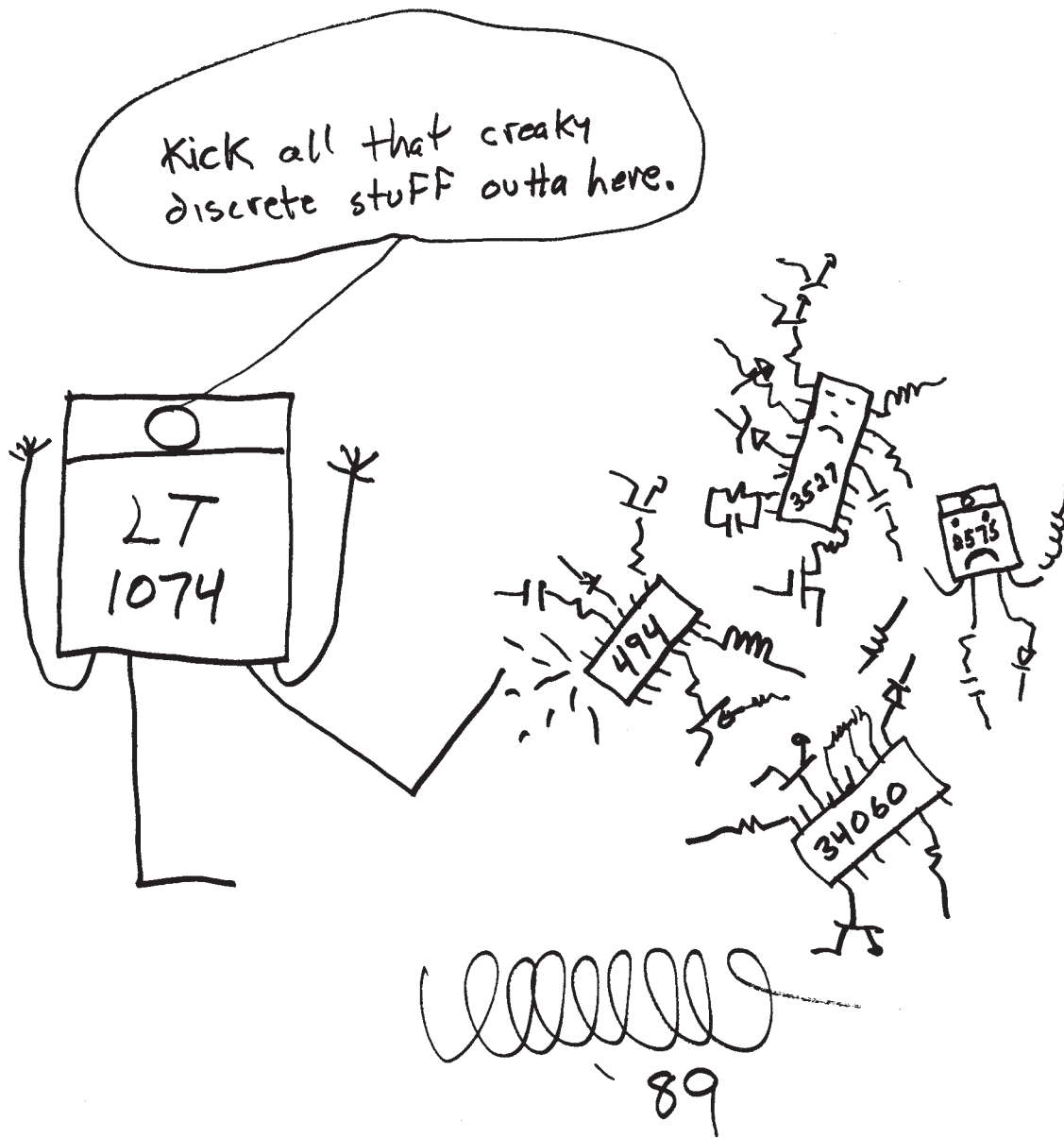
Magnetics is probably the most formidable issue in converter design. Design and construction of suitable magnetics is a difficult task, particularly for the non-specialist. It is our experience that the majority of converter design problems are associated with magnetics requirements. This consideration is accentuated by the fact that most converters are employed by non-specialists. As a purveyor of switching power ICs we incur responsibility towards addressing the magnetics issue (our publicly spirited attitude is, admittedly, capitalistically polluted). As such, it is LTC's policy to use off-the-shelf magnetics in our circuits. In some cases, available magnetics serve a particular design. In other situations the magnetics have been specially designed, assigned a part number and made available as standard product.

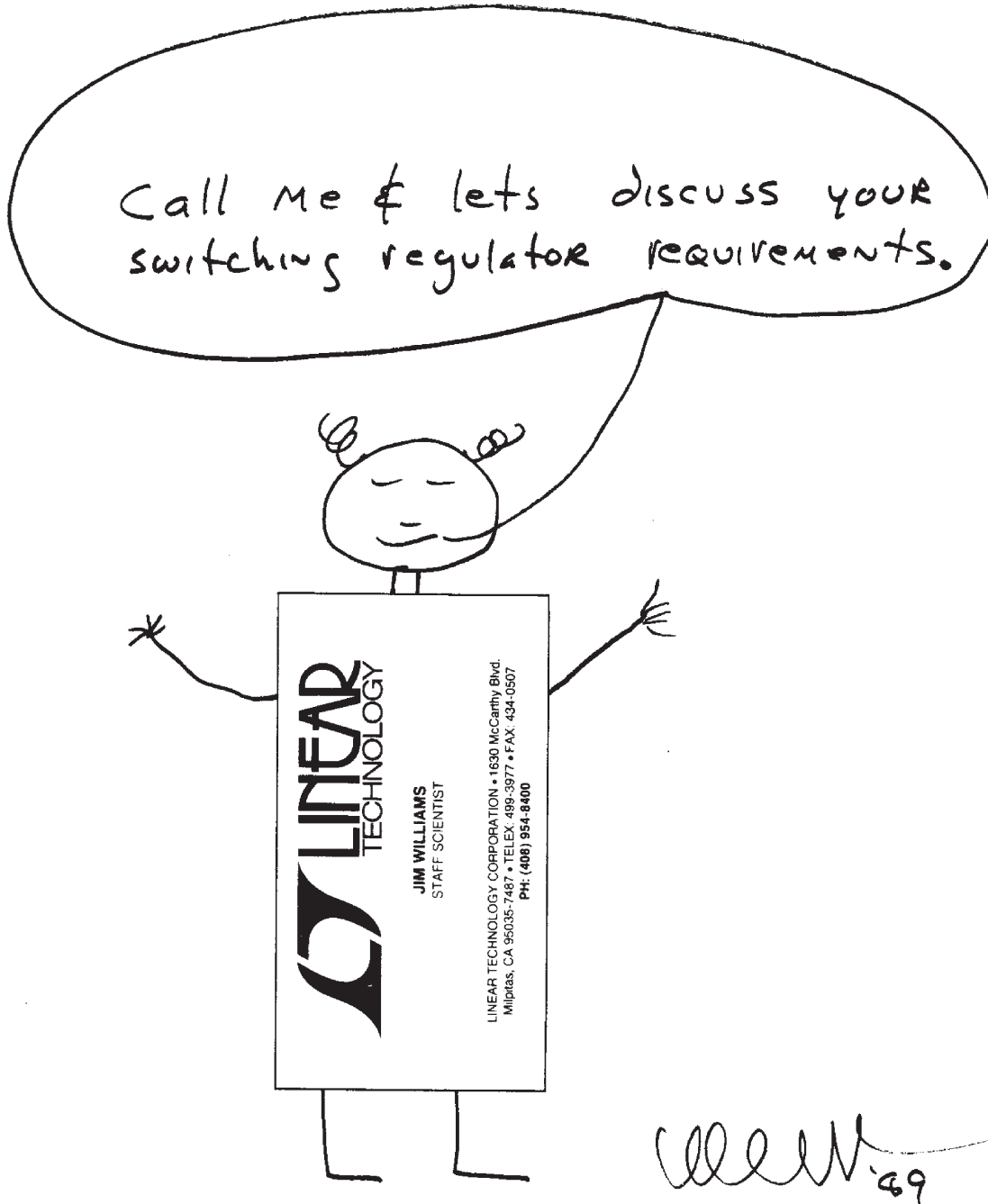
In many circumstances a standard product is suitable for production. Other cases may require modifications or changes which the manufacturer can provide or advise on. Hopefully, this approach serves the needs of all concerned.

Recommended magnetics manufacturers include the following;

Pulse Engineering, Inc
P.O. Box 12235
7250 Convoy Court
San Diego, California 92112
619-268-2400

Coiltronics
984 Southwest 13th Court
Pompano Beach, FL 33069
305-781-8900





Fast Charge Circuits for NiCad Batteries

Jim Williams

Safe, fast charging of NiCad batteries is attractive in many applications. Short charge time requires high current. A potential difficulty with high current charging is battery heating. Excessive internal heating degrades the battery and can cause gas venting to the outside atmosphere. Fast charge schemes based on monitoring cell voltage during charge suffer because cell voltage is not necessarily indicative of the battery's charge state. Additionally, the battery's charge-voltage relationship may alter over life and temperature. Similarly, open loop charging techniques involving high charge rates for a fixed time do not account for battery charge state or characteristic shifts over life and temperature.

One way to charge batteries without abuse is to measure cell temperature and taper the charge accordingly. This method is based on the fact that a discharged battery converts charging current to stored electrochemical energy, with relatively little heat produced. When the battery arrives at full charge the cell is saturated and cannot hold any more energy. As such, heat is produced, raising battery temperature. One way to detect this point is to measure cell surface temperature referred to ambient. An absolute temperature measurement is undesirable

because cell temperature represents the summation of excess charging energy and ambient temperature. Additionally, the ambient and battery temperatures must be measured in phase. The thermal time constant of a battery pack can easily exceed one hour. If battery temperature is referred to a quickly responding ambient temperature poor charging characteristics can result. Consider the case of a portable computer retrieved from a locked automobile on a summer day. Passenger compartment temperature can exceed 120°F. The computer is brought inside, where the ambient temperature sensor quickly settles to 73°F. The battery pack temperature is sitting at 120°F looking through a one hour thermal time constant. Under these conditions the system is fooled into believing the battery has just received a full charge, and no charge is delivered. The opposite effect occurs if the computer is in a car parked overnight in Minneapolis in January. These effects are avoidable by lagging the ambient temperature information with a time constant similar to the battery packs. Figure 1 shows a simple analog. The resistors represent thermal resistance while the capacitors correspond to thermal capacitance. Ambient temperature appears as a common mode term, while charger energy affects the battery only. Note that the ambient and battery

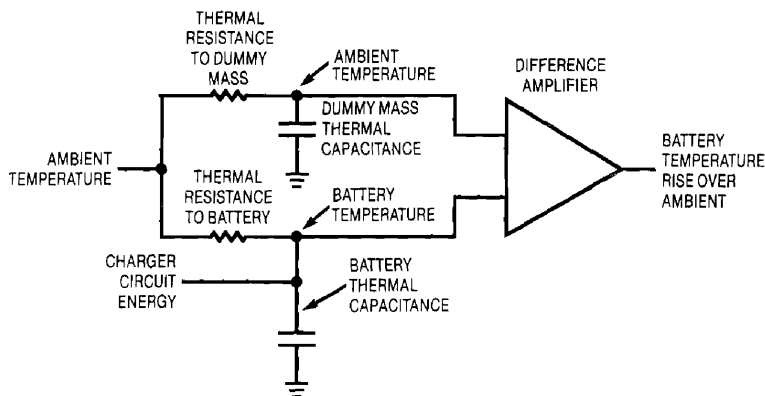


Figure 1. Simplified Thermal Analog. Matched Thermal RC Terms Provide Immunity to Ambient Temperature Shifts.

Application Note 37

temperatures do not require the same individual R-C values to present phased information to the difference amplifier. Rather, their RC *products* must be matched. A massive battery pack with relatively low thermal resistance to ambient can be matched by the time constant of a well insulated (e.g., high thermal resistance) small thermal mass.

Practical Thermally Based NiCad Charger

Figure 2 shows a practical circuit. Thermocouples sense cell and ambient temperatures. The LT1006 amplifier furnishes the low level capability necessary to work with the microvolt level thermocouple signals. To understand the circuit's operation, assume a discharged battery pack in the transistor collector line. The battery and ambient thermocouples are at the same temperature. The battery thermocouple is directly mounted to one of the cells in the pack. The ambient thermocouple is thermally insulated and mounted to a mass, perhaps a frame member of the equipment. Under these conditions the sensors are phase matched, their outputs cancel and A1 sees 0V. The offset adjustment deliberately introduces enough input offset for A1 to swing positively, turning on the transistor. Current flows from the supply, through the battery pack and to ground via the $250\mu\Omega$ shunt. The low impedance shunt minimizes losses, cost, and complexity. The voltage across the shunt rises to about $625\mu\text{V}$ (the amount of offset forced by the potentiometer), and the amplifier servo controls about 2.5A through the battery pack. As the battery charges, it heats. This heat is picked up by the

*See Appendix A for construction information on low resistance shunts.

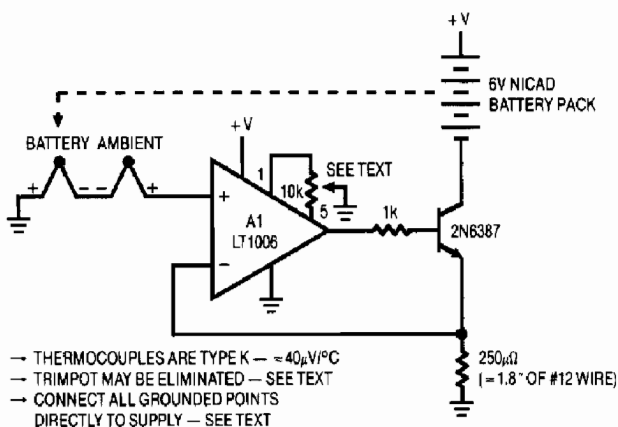


Figure 2. Thermally Controlled NiCad Battery Charger

battery-mounted thermocouple. The temperature difference between the two thermocouples determines the voltage which appears at the amplifier's positive input. As battery temperature rises, this small negative voltage (1°C difference between the thermocouples equals $40\mu\text{V}$) becomes larger. The amplifier gradually reduces the current through the battery to maintain its inputs at balance. The effect of this action is shown in Figure 3. The battery charges at a high rate until heating occurs and the circuit then tapers the charge. The values given in the circuit limit the battery surface temperature rise over ambient to about 15°C .

Figure 4's circuit is arranged for use with batteries which are committed to ground. The common emitter output necessitates exchanging amplifier input assignments, but circuit operation is identical to Figure 2. In both circuits the trimpot may be eliminated by specifying an LT1006 set at manufacture to the desired offset value.

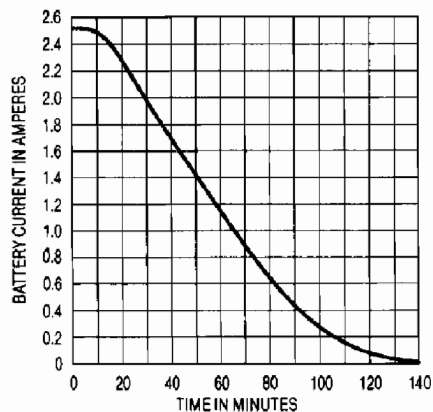


Figure 3. Figure 2's Charge Characteristics

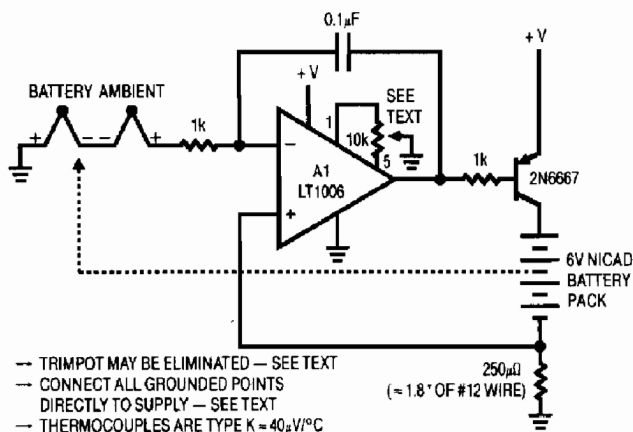


Figure 4. Figure 2's Circuit Arranged for a Grounded Battery

The small shunt sense voltage requires a high quality ground for accurate results. This ensures that the large current flow through the transistor does not combine with ground return impedances to create errors. In practice, all returns should be brought directly back to the supply common terminal. Similarly, parasitic thermocouple effects should be avoided (see LTC Application Note 9 for a discussion on minimizing parasitic thermocouple effects).

Both circuits force the transistor to dissipate some power, particularly in the middle of the charge curve. The heat produced may be a problem in a very small enclosure. Figure 5's circuit eliminates this problem. This design is similar to the others, except that the A2 duty cycle modulator configuration is interposed between A1 and the output transistor. The transistor, in this case a power FET, operates in switched mode, delivering duty cycle modu-

lated current pulses to the battery pack. R7-C4 filters the switching waveform to DC. R6 and R7 present a balanced source impedance to A1. C2 sets gain roll-off. This design relies on the source impedance of the wall transformer to limit the current through Q1 and the battery pack. This parameter may be set when specifying the transformer. Figure 6 should be used in cases where the charging source has low impedance. Here, the circuit's output is reconfigured as a simple step down switching regulator (basic operation of step down switching regulators is described in LTC Application Note 35). The 74C04's provide phase inversion and drive for Q1, a P-channel MOSFET. Figure 7 shows waveforms. Trace A is A2's output with trace B showing Q1's gate drive. Trace C is Q1's drain voltage and trace D its current. Trace E is the MR850 catch diode current. Trace F is L1's current. L1 smooths current flow, resulting in low loss operation.

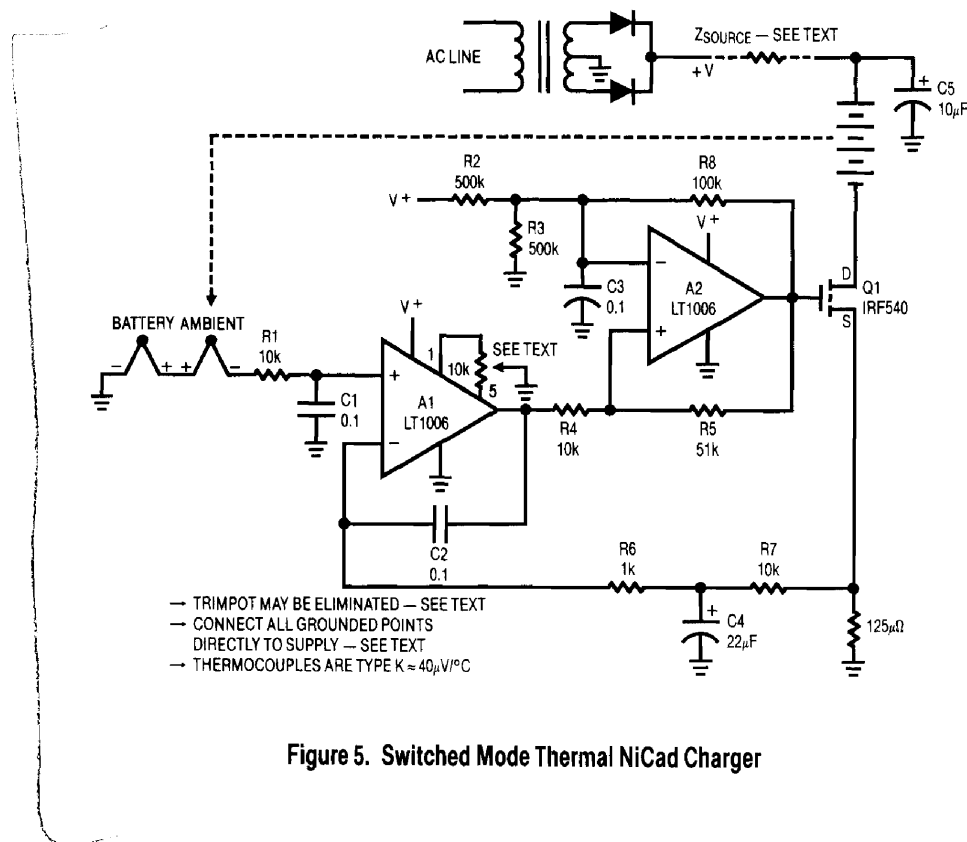


Figure 5. Switched Mode Thermal NiCad Charger

Application Note 37

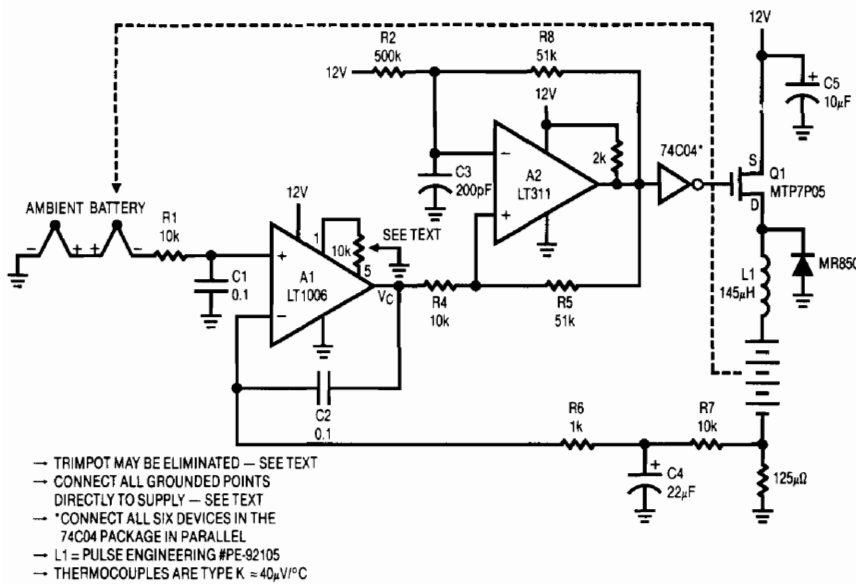


Figure 6. Switched Mode Thermal NiCad Charger

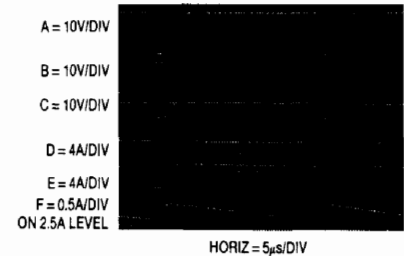


Figure 7. Figure 6's Switching Waveforms

Note — This application note was derived from a manuscript originally prepared for publication in EDN magazine.
 Acknowledgement — The contributions of William Cho towards the completion of this Application Note are gratefully acknowledged.

APPENDIX A

Construction of Low Resistance Shunts

A simple, inexpensive way to construct low resistance shunts is to use a small length of wire or PC trace. The type and length of wire determine shunt resistance, which will vary with desired charging characteristics. Figure A1

gives resistance vs length characteristics for various wire sizes. The shunt should have separate connections for sensing (Kelvin style) so that the high current does not corrupt readings. Figure A2 shows a typical configuration.

WIRE GAUGE	µΩ/INCH
10	83
11	100
12	130
13	160
14	210
15	265
16	335
17	421
18	530
19	670
20	890
21	1000
22	1300
23	1700
24	2100
25	2700

Figure A1. Resistance vs Size for Various Copper Wire Types

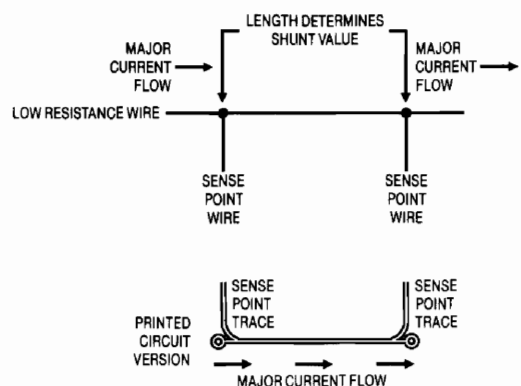


Figure A2. Detail of a Low Resistance Current Shunt

Bridge Circuits

Marrying Gain and Balance

Jim Williams

Bridge circuits are among the most elemental and powerful electrical tools. They are found in measurement, switching, oscillator and transducer circuits. Additionally, bridge techniques are broadband, serving from DC to bandwidths well into the GHz range. The electrical analog of the mechanical beam balance, they are also the progenitor of all electrical differential techniques.

Resistance Bridges

Figure 1 shows a basic resistor bridge. The circuit is usually credited to Charles Wheatstone, although S. H. Christie, who demonstrated it in 1833, almost certainly preceded him.¹ If all resistor values are equal (or the two sides *ratios* are equal) the differential voltage is zero. The excitation voltage does not alter this, as it affects both sides equally. When the bridge is operating off null, the excitation's magnitude sets output sensitivity. The bridge output is nonlinear for a single variable resistor. Similarly, two variable arms (e.g., R_C and R_B both variable) produce nonlinear output, although sensitivity doubles. Linear outputs are possible by complementary resistance swings in one or both sides of the bridge.

A great deal of attention has been directed towards this circuit. An almost uncountable number of tricks and techniques have been applied to enhance linearity, sensitivity

and stability of the basic configuration. In particular, transducer manufacturers are quite adept at adapting the bridge to their needs (see Appendix A, "Strain Gauge Bridges"). Careful matching of the transducer's mechanical characteristics to the bridge's electrical response can provide a trimmed, calibrated output. Similarly, circuit designers have altered performance by adding active elements (e.g., amplifiers) to the bridge, excitation source or both.

Bridge Output Amplifiers

A primary concern is the accurate determination of the differential output voltage. In bridges operating at null the absolute scale factor of the readout device is normally less important than its sensitivity and zero point stability. An off-null bridge measurement usually requires a well calibrated scale factor readout in addition to zero point stability. Because of their importance, bridge readout mechanisms have a long and glorious history (see Appendix B, "Bridge Readout—Then and Now"). Today's investigator has a variety of powerful electronic techniques available to obtain highly accurate bridge readouts. Bridge amplifiers are designed to accurately extract the bridges differential output from its common mode level. The ability to reject common mode signal is quite critical. A typical 10V powered strain gauge transducer produces only 30mV of signal "riding" on 5V of common mode level. 12-bit readout resolution calls for an LSB of only 7.3 μ V....almost 120dB below the common mode signal! Other significant error terms include offset voltage, and its shift with temperature and time, bias current and gain stability. Figure 2 shows an "Instrumentation Amplifier," which makes a very good bridge amplifier. These devices are usually the first choice for bridge measurement, and bring adequate performance to most applications.

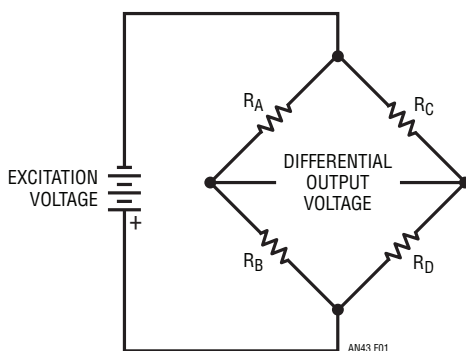



Figure 1. The Basic Wheatstone Bridge, Invented by S. H. Christie

Note 1: Wheatstone had a better public relations agency, namely himself. For fascinating details, see reference 19.

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Application Note 43

In general, instrumentation amps feature fully differential inputs and internally determined stable gain. The absence of a feedback network means the inputs are essentially passive, and no significant bridge loading occurs. Instrumentation amplifiers meet most bridge requirements. Figure 3 lists performance data for some specific instrumentation amplifiers. Figure 4's table summarizes some options for DC bridge signal conditioning. Various approaches are presented, with pertinent characteristics noted. The constraints, freedoms and performance requirements of any particular application define the best approach.

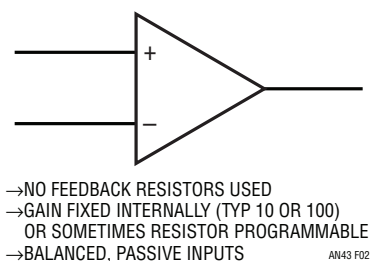


Figure 2. Conceptual Instrumentation Amplifier

DC Bridge Circuit Applications

Figure 5, a typical bridge application, details signal conditioning for a 350Ω transducer bridge. The specified strain gauge pressure transducer produces 3mV output per volt of bridge excitation (various types of strain-based transducers are reviewed in Appendix A, “Strain Gauge Bridges”). The LT®1021 reference, buffered by A1A and A2, drives the bridge. This potential also supplies the circuits ratio output, permitting ratiometric operation of a monitoring A/D converter. Instrumentation amplifier A3 extracts the bridge’s differential output at a gain of

100, with additional trimmed gain supplied by A1B. The configuration shown may be adjusted for a precise 10V output at full-scale pressure. The trim at the bridge sets the zero pressure scale point. The RC combination at A1B’s input filters noise. The time constant should be selected for the system’s desired lowpass cutoff. “Noise” may originate as residual RF/line pick-up or true transducer responses to pressure variations. In cases where noise is relatively high it may be desirable to filter ahead of A3. This prevents any possible signal infidelity due to nonlinear A3 operation. Such undesirable outputs can be produced by saturation, slew rate components, or rectification effects. When filtering ahead of the circuits gain blocks remember to allow for the effects of bias current induced errors caused by the filter’s series resistance. This can be a significant consideration because large value capacitors, particularly electrolytics, are not practical. If bias current induced errors rise to appreciable levels FET or MOS input amplifiers may be required (see Figure 3).

To trim this circuit apply zero pressure to the transducer and adjust the 10k potentiometer until the output *just* comes off 0V. Next, apply full-scale pressure and trim the 1k adjustment. Repeat this procedure until both points are fixed.

Common Mode Suppression Techniques

Figure 6 shows a way to reduce errors due to the bridges common mode output voltage. A1 biases Q1 to servo the bridges left mid-point to zero under all operating conditions. The 350Ω resistor ensures that A1 will find a stable operating point with 10V of drive delivered to the bridge. This allows A2 to take a single-ended measurement,

PARAMETER	LTC1100	LT1101	LT1102	LTC1043 (USING LTC1050 AMPLIFIER)
Offset	10μV	160μV	500μV	0.5μV
Offset Drift	100nV/°C	2μV/°C	2.5μV/°C	50nV/°C
Bias Current	50pA	8nA	50pA	10pA
Noise (0.1Hz to 10Hz)	2μV _{P-P}	0.9μV	2.8μV	1.6μV
Gain	100	10,100	10,100	Resistor Programmable
Gain Error	0.03%	0.03%	0.05%	Resistor Limited 0.001% Possible
Gain Drift	4ppm/°C	4ppm/°C	5ppm/°C	Resistor Limited <1ppm/°C Possible
Gain Nonlinearity	8ppm	8ppm	10ppm	Resistor Limited 1ppm Possible
CMRR	104dB	100dB	100dB	160dB
Power Supply	Single or Dual, 16V Max	Single or Dual, 44V Max	Dual, 44V Max	Single, Dual 18V Max
Supply Current	2.2mA	105μA	5mA	2mA
Slew Rate	1.5V/μs	0.07V/μs	25V/μs	1mV/ms
Bandwidth	8kHz	33kHz	220kHz	10Hz

Figure 3. Comparison of Some IC Instrumentation Amplifiers

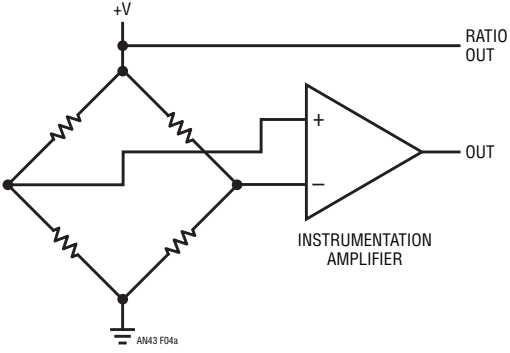
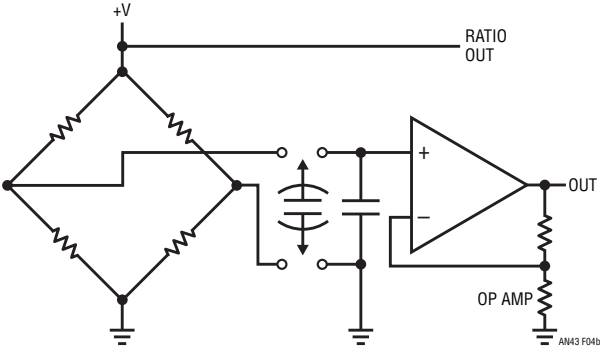
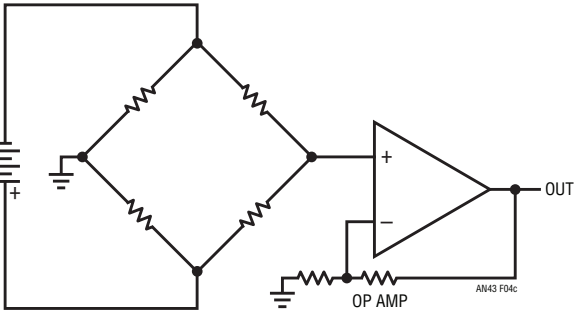
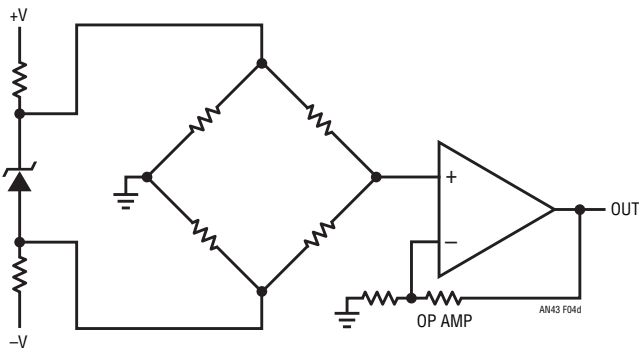
CONFIGURATION	ADVANTAGES	DISADVANTAGES
 <p>AN43 F04a</p>	<p>Best general choice. Simple, straightforward. CMRR typically >110dB, drift 0.05μV/$^{\circ}$C to 2μV/$^{\circ}$C, gain accuracy 0.03%, gain drift 4ppm/$^{\circ}$C, noise 10nV/$\sqrt{\text{Hz}}$ – 1.5μV for chopper-stabilized types. Direct ratiometric output.</p>	<p>CMRR, drift and gain stability may not be adequate in highest precision applications. May require second stage to trim gain.</p>
 <p>AN43 F04b</p>	<p>CMRR > 120dB, drift 0.05μV/$^{\circ}$C. Gain accuracy 0.001% possible. Gain drift 1ppm with appropriate resistors. Noise 10nV/$\sqrt{\text{Hz}}$ – 1.5μV for chopper-stabilized types. Direct ratiometric output. Simple gain trim. Flying capacitor commutation provides lowpass filtering. Good choice for very high performance—monolithic versions (LTC1043) available.</p>	<p>Multi-package—moderately complex. Limited bandwidth. Requires feedback resistors to set gain.</p>
 <p>AN43 F04c</p>	<p>CMRR > 160dB, drift 0.05μV/$^{\circ}$C to 0.25μV/$^{\circ}$C, gain accuracy 0.001% possible, gain drift 1ppm/$^{\circ}$C with appropriate resistors plus floating supply error, simple gain trim, Noise 1nV/$\sqrt{\text{Hz}}$ possible.</p>	<p>Requires floating supply. No direct ratiometric output. Floating supply drift is a gain term. Requires feedback resistors to set gain.</p>
 <p>AN43 F04d</p>	<p>CMRR \approx 140dB, drift 0.05μV/$^{\circ}$C to 0.25μV/$^{\circ}$C, gain accuracy 0.001% possible, gain drift 1ppm/$^{\circ}$C with appropriate resistors plus floating supply error, simple gain trim, noise 1nV/$\sqrt{\text{Hz}}$ possible.</p>	<p>No direct ratiometric output. Zener supply is a gain and offset term error generator. Requires feedback resistors to set gain. Low impedance bridges require substantial current from shunt regulator or circuitry which simulates it. Usually poor choice if precision is required.</p>

Figure 4. Some Signal Conditioning Methods for Bridges

Application Note 43

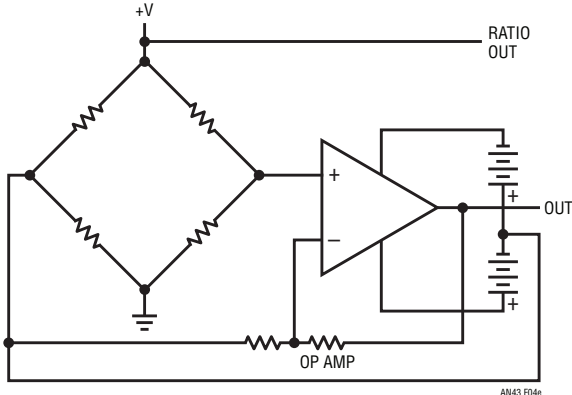
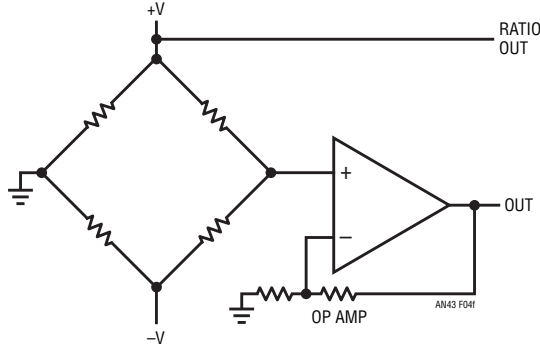
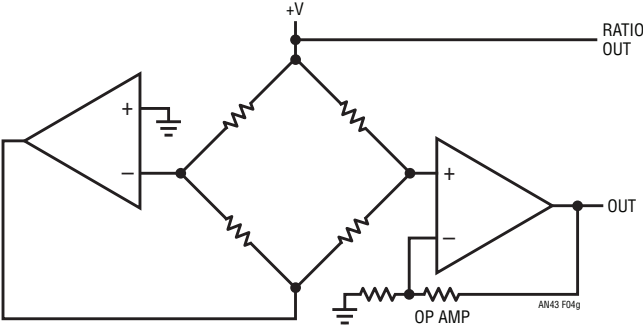
CONFIGURATION	ADVANTAGES	DISADVANTAGES
 <p style="text-align: right; font-size: small;">AN43 F04e</p>	<p>CMRR > 160dB, drift 0.05μV/$^{\circ}$C to 0.25μV/$^{\circ}$C, gain accuracy 0.001% possible, gain drift 1ppm/$^{\circ}$C with appropriate resistors, simple gain trim, ratiometric output, noise 1nV/$\sqrt{\text{Hz}}$ possible.</p>	<p>Requires precision analog level shift, usually with isolation amplifier. Requires feedback resistors to set gain.</p>
 <p style="text-align: right; font-size: small;">AN43 F04f</p>	<p>CMRR \approx 120dB to 140dB, drift 0.05μV/$^{\circ}$C to 0.25μV/$^{\circ}$C, gain accuracy 0.001% possible, gain drift 1ppm/$^{\circ}$C with appropriate resistors, simple gain trim, direct ratiometric output, noise 1nV/$\sqrt{\text{Hz}}$ possible.</p>	<p>Requires tracking supplies. Assumes high degree of bridge symmetry to achieve best CMRR. Requires feedback resistors to set gain.</p>
 <p style="text-align: right; font-size: small;">AN43 F04g</p>	<p>CMRR = 160dB, drift 0.05μV/$^{\circ}$C to 0.25μV/$^{\circ}$C, gain accuracy 0.001% possible, gain drift 1ppm/$^{\circ}$C, simple gain trim, direct ratiometric output, noise 1nV/$\sqrt{\text{Hz}}$ possible.</p>	<p>Practical realization requires two amplifiers plus various discrete components. Negative supply necessary.</p>

Figure 4. Some Signal Conditioning Methods for Bridges (Continued)

eliminating all common mode voltage errors. This approach works well, and is often a good choice in high precision work. The amplifiers in this example, CMOS chopper-stabilized units, essentially eliminate offset drift with time and temperature. Trade-offs compared to an instrumentation amplifier approach include complexity and the requirement for a negative supply. Figure 7 is similar, except that low noise bipolar amplifiers are used. This circuit trades slightly higher DC offset drift for lower noise and is a good candidate for stable resolution of small, slowly varying measurands. Figure 8 employs chopper-stabilized A1 to

reduce Figure 7's already small offset error. A1 measures the DC error at A2's inputs and biases A1's offset pins to force offset to a few microvolts. The offset pin biasing at A2 is arranged so A1 will always be able to find the servo point. The 0.01 μ F capacitor rolls off A1 at low frequency, with A2 handling high frequency signals. Returning A2's feedback string to the bridges mid-point eliminates A4's offset contribution. If this was not done A4 would require a similar offset correction loop. Although complex, this approach achieves less than 0.05 μ V/ $^{\circ}$ C drift, 1nV/ $\sqrt{\text{Hz}}$ noise and CMRR exceeding 160dB.

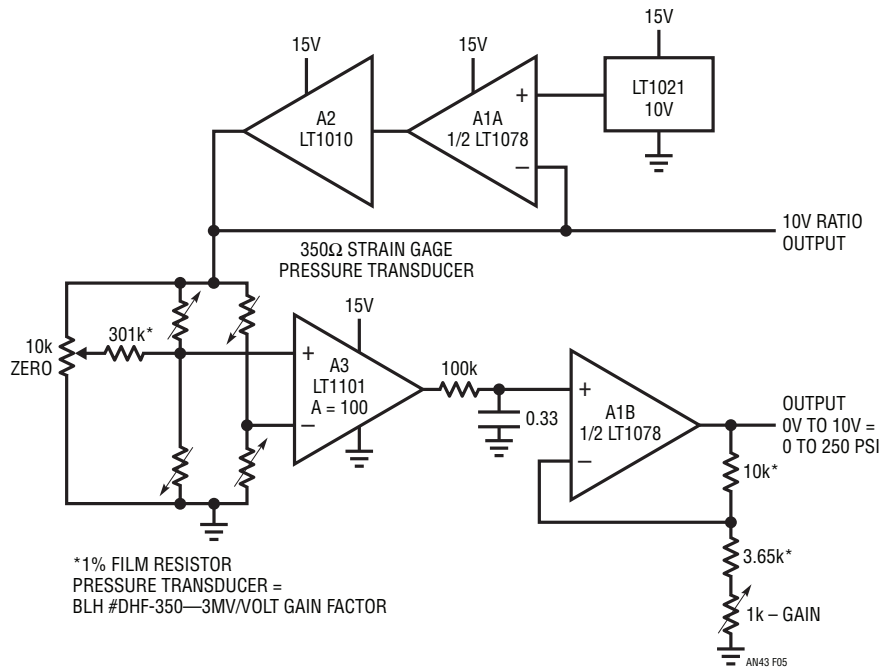


Figure 5. A Practical Instrumentation Amplifier-Based Bridge Circuit

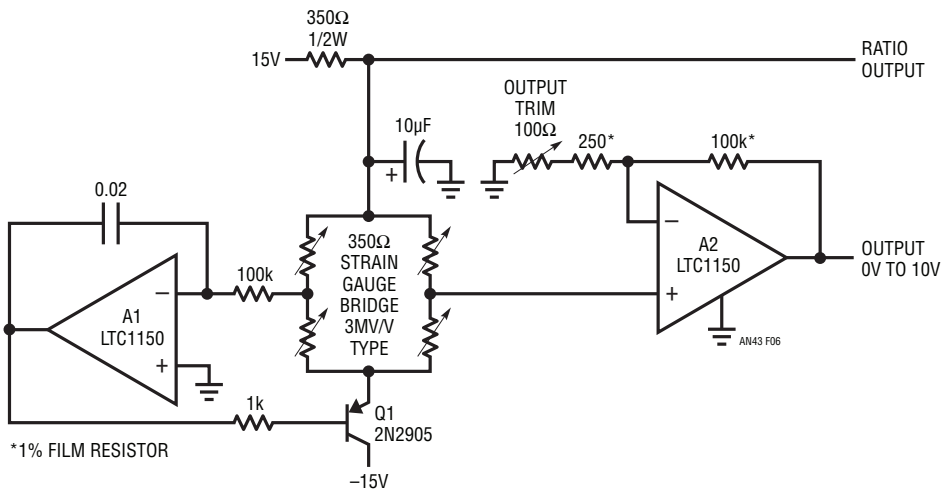


Figure 6. Servo Controlling Bridge Drive Eliminates Common Mode Voltage

Single Supply Common Mode Suppression Circuits

The common mode suppression circuits shown require a negative power supply. Often, such circuits must function in systems where only a positive rail is available. Figure 9 shows a way to do this. A2 biases the LTC®1044 positive-to-negative converter. The LTC1044's output pulls the bridge's output negative, causing A1's input to balance at 0V. This local loop permits a single-ended amplifier (A2)

to extract the bridge's output signal. The 100k-0.33μF RC filters noise and A2's gain is set to provide the desired output scale factor. Because bridge drive is derived from the LT1034 reference, A2's output is not affected by supply shifts. The LT1034's output is available for ratio operation. Although this circuit works nicely from a single 5V rail the transducer sees only 2.4V of drive. This reduced drive

Application Note 43

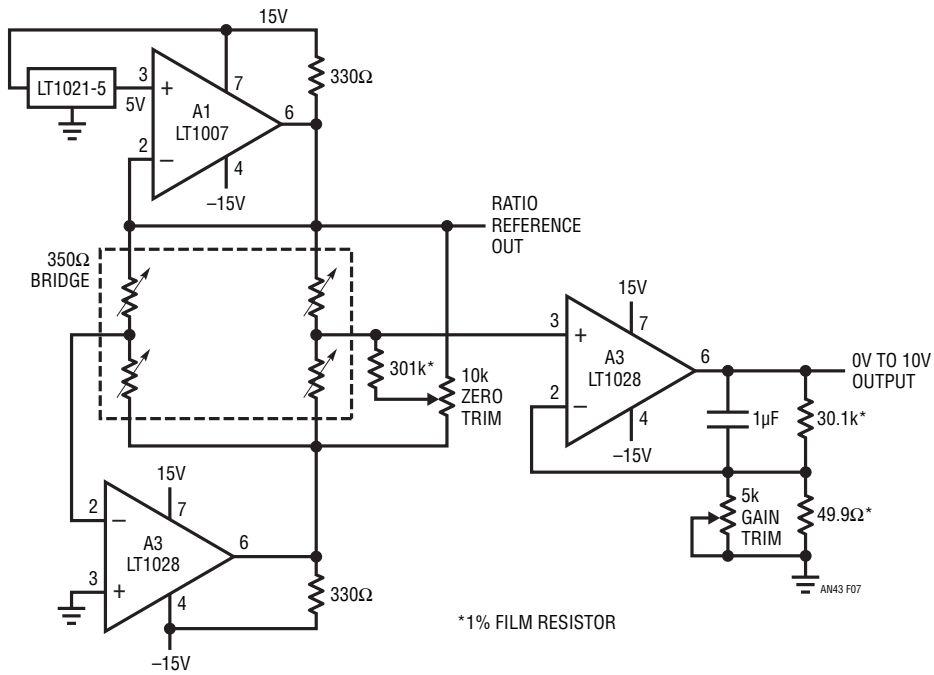


Figure 7. Low Noise Bridge Amplifier with Common Mode Suppression

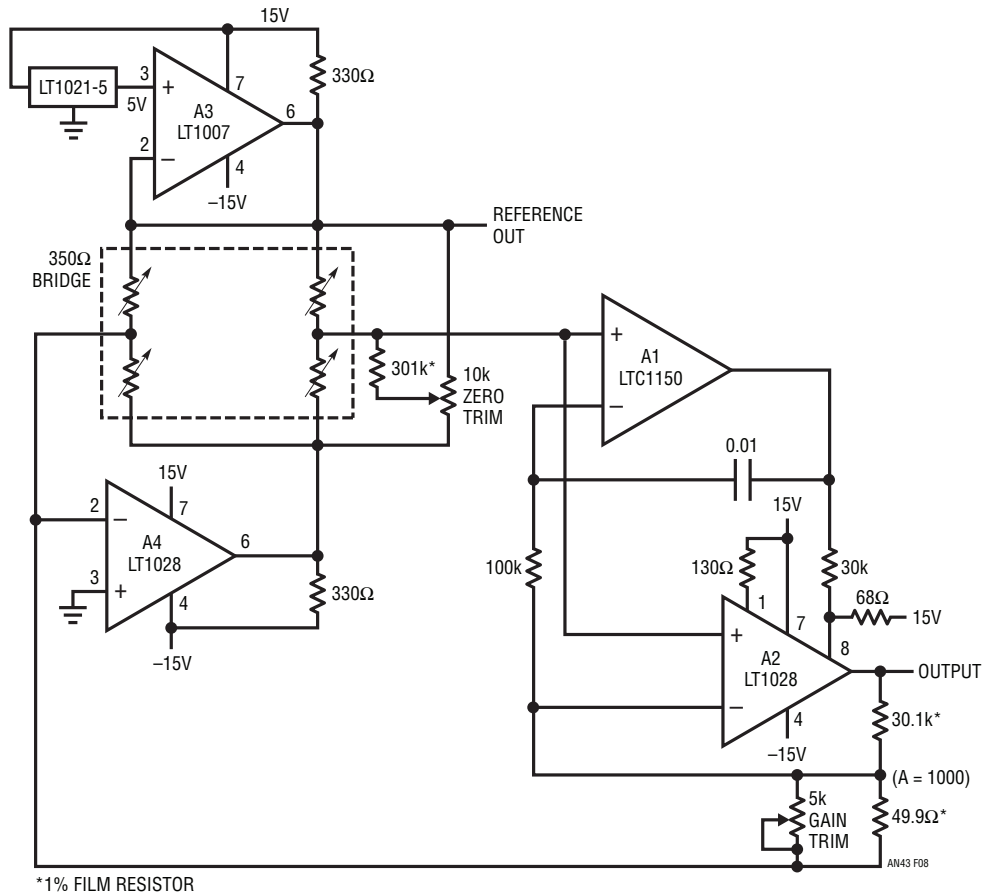


Figure 8. Low Noise, Chopper-Stabilized Bridge Amplifier with Common Mode Suppression

Application Note 43

Switched-Capacitor Based Instrumentation Amplifiers

Switched-capacitor methods are another way to signal condition bridge outputs. Figure 11 uses a flying capacitor configuration in a very high precision-scale application. This design, intended for weighing human subjects, will resolve 0.01 pound at 300.00 pounds full scale. The strain gauge based transducer platform is excited at 10V by the LT1021 reference, A1 and A2. The LTC1043 switched-capacitor building block combines with A3, forming a differential input chopper-stabilized amplifier. The LTC1043 alternately connects the 1 μ F flying capacitor between the strain gauge bridge output and A3's input. A second 1 μ F unit stores the LTC1043 output, maintaining A3's input at DC. The LTC1043's low charge injection maintains differential to single-ended transfer accuracy of about 1ppm at DC and low frequency. The commutation rate, set by the 0.01 μ F capacitor, is about 400Hz. A3 takes scaled gain, providing 3.0000V for 300.00 pounds full-scale output.

The extremely high resolution of this scale requires filtering to produce useful results. Very slight body movement acting on the platform can cause significant noise in A3's output. This is dramatically apparent in Figure 12's tracings. The total *force* on the platform is equal to gravity pulling on the body (the "weight") plus any additional accelerations within or acting upon the body. Figure 12 (Trace B) clearly shows that each time the heart pumps, the acceleration due to the blood (mass) moving in the arteries shows up as "weight". To prove this, the subject gets off the scale and runs in place for 15 seconds. When the subject returns to the platform the heart should work harder. Trace A confirms this nicely. The exercise causes the heart to work harder, forcing a greater acceleration-per-stroke.²

Note 2: Cardiology aficionados will recognize this as a form of *Ballistocardiograph* (from the Greek "ballein"—to throw, hurl or eject and "kardia," heart). A significant amount of effort was expended in attempts to reliably characterize heart conditions via acceleration detection methods. These efforts were largely unsuccessful when compared against the reliability of EKG produced data. See references for further discussion.

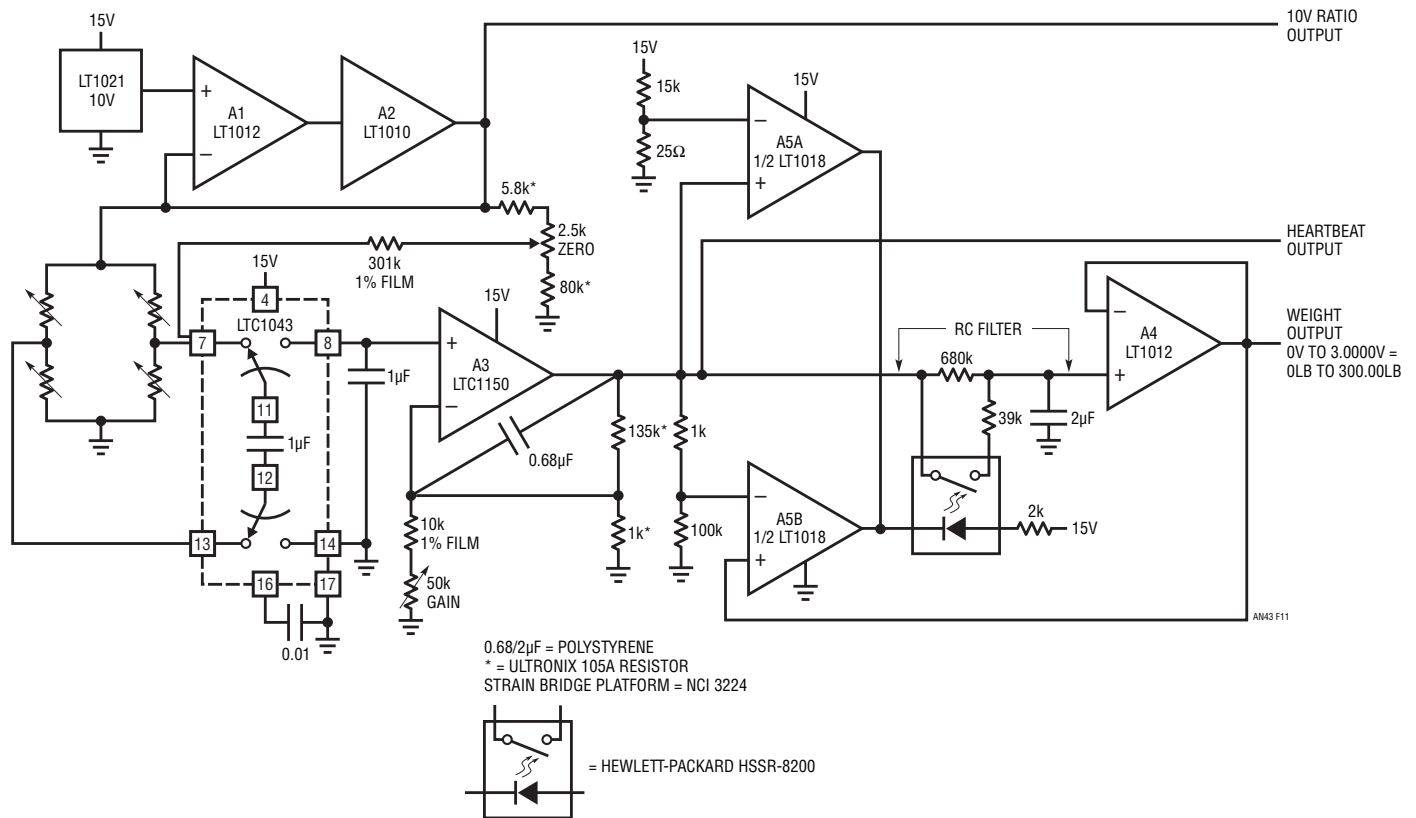


Figure 11. High Precision Scale for Human Subjects

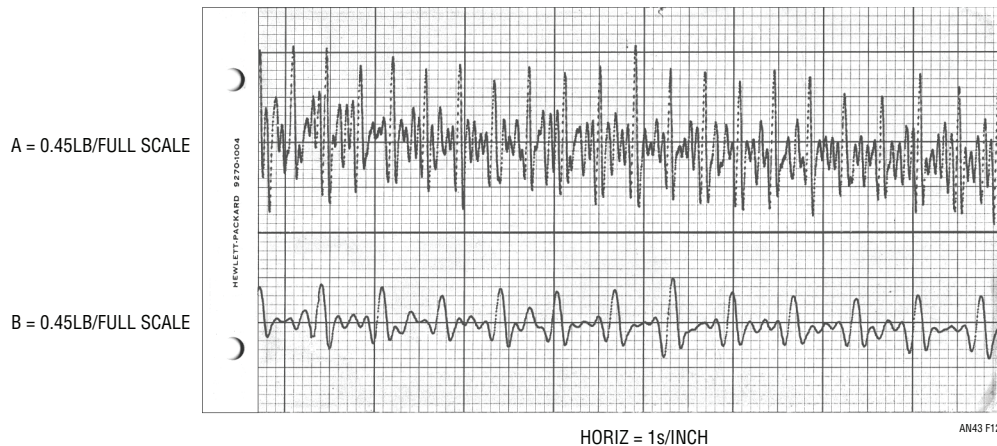


Figure 12. High Precision Scale's Heartbeat Output. Trace B Shows Subject at Rest; Trace A After Exercise. Discontinuous Components in Waveforms Leading Edges Are Due to XY Recorder Slew Limitations

Another source of noise is due to body motion. As the body moves around, its mass doesn't change but the instantaneous accelerations are picked up by the platform and read as "weight" shifts.

All this seems to make a 0.01 pound measurement meaningless. However, filtering the noise out gives a time averaged value. A simple RC lowpass will work, but requires excessively long settling times to filter noise fundamentals in the 1Hz region. Another approach is needed.

A4, A5 and associated components form a filter which switches its time constant from short to long when the output has nearly arrived at the final value. With no weight on the platform A3's output is zero. A4's output is also zero, A5B's output is indeterminate and A5A's output is low. The MOSFET opto-coupler LED comes on, putting the RC filter into short time constant mode. When someone gets on the scale A3's output rises rapidly. A5A goes high, but A5B trips low, maintaining the RC filter in its short time constant mode. The 2 μ F capacitor charges rapidly, and A4 quickly settles to final value \pm body motion and heartbeat noise. A5B's negative input sees 1% attenuation from A3; its positive input does not. This causes A5B to switch high when A4's output arrives within 1% of final value. The opto-coupler goes off and the filter switches into long time constant mode, eliminating noise in A4's output. The 39k resistor prevents overshoot, ensuring monotonic A4 outputs. When the subject steps off the scale A3 quickly returns to zero. A5A goes immediately low, turning on the opto-coupler. This quickly discharges

the 2 μ F capacitor, returning A4's output rapidly to zero. The bias string at A5A's input maintains the scale in fast time constant mode for weights below 0.50 pounds. This permits rapid response when small objects (or persons) are placed on the platform. To trim this circuit, adjust the zero potentiometer for 0V out with no weight on the platform. Next, set the gain adjustment for 3.0000V out for a 300.00 pound platform weight. Repeat this procedure until both points are fixed.

Optically Coupled Switched-Capacitor Instrumentation Amplifier

Figure 13 also uses optical techniques for performance enhancement. This switched-capacitor based instrumentation amplifier is applicable to transducer signal conditioning where high common mode voltages exist. The circuit has the low offset and drift of the LTC1150 but also incorporates a novel switched-capacitor "front end" to achieve some specifications not available in a conventional instrumentation amplifier.

Common mode rejection ratio at DC for the front end exceeds 160dB. The amplifier will operate over a \pm 200V common mode range and gain accuracy and stability are limited only by external resistors. A1, a chopper stabilized unit, sets offset drift at 0.05 μ V/ $^{\circ}$ C. The high common mode voltage capability of the design allows it to withstand transient and fault conditions often encountered in industrial environments.

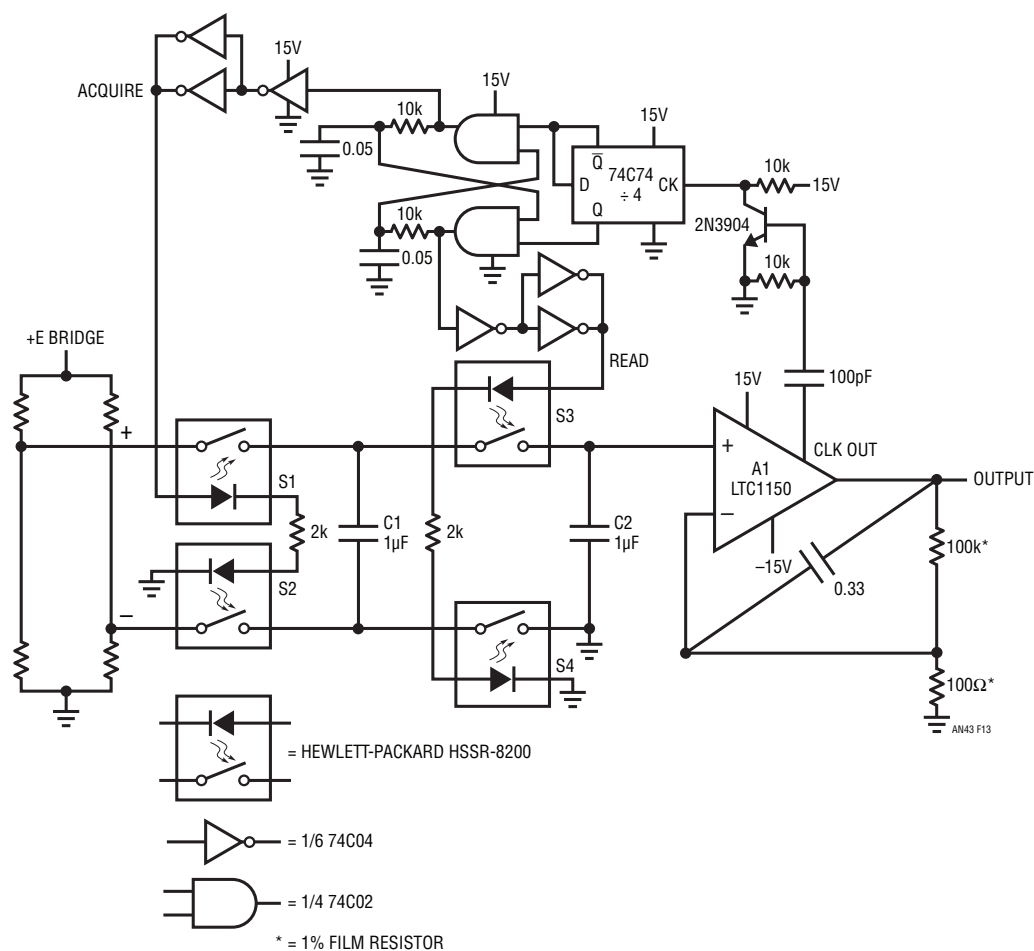


Figure 13. Floating Input Bridge Instrumentation Amplifier with 200V Common Mode Range

The circuit's inputs are fed to LED-driven optically-coupled MOSFET switches, S1 and S2. Two similar switches, S3 and S4, are in series with S1 and S2. CMOS logic functions, clocked from A1's internal oscillator, generate non-overlapping clock outputs which drive the switch's LEDs. When the "acquire pulse" is high, S1 and S2 are on and C2 acquires the differential voltage at the bridge's output. During this interval, S3 and S4 are off. When the acquire pulse falls, S1 and S2 begin to go off. After a delay to allow S1 and S2 to fully open, the "read pulse" goes high, turning on S3 and S4. Now C1 appears as a ground-referred voltage source which is read by A1. C2 allows A1's input to retain C1's value when the circuit returns to the acquire mode. A1 provides the circuit's output. Its gain is set in normal fashion by feedback resistors. The 0.33 μF feedback capacitor sets roll-off. The differential-to-single-ended transition performed by the switches and capacitors means that A1 never sees the input's common mode signal. The

breakdown specification of the optically-driven MOSFET switch allows the circuit to withstand and operate at common mode levels of ±200V. In addition, the optical drive to the MOSFETs eliminates the charge injection problems common to FET switched-capacitive networks.

Platinum RTD Resistance Bridge Circuits

Platinum RTDs are frequently used in bridge configurations for temperature measurement. Figure 14's circuit is highly accurate and features a ground referred RTD. The ground connection is highly desirable for noise rejection. The bridge's RTD leg is driven by a current source while the opposing bridge branch is voltage biased. The current drive allows the voltage across the RTD to vary directly with its temperature induced resistance shift. The difference between this potential and that of the opposing bridge leg forms the bridge's output.

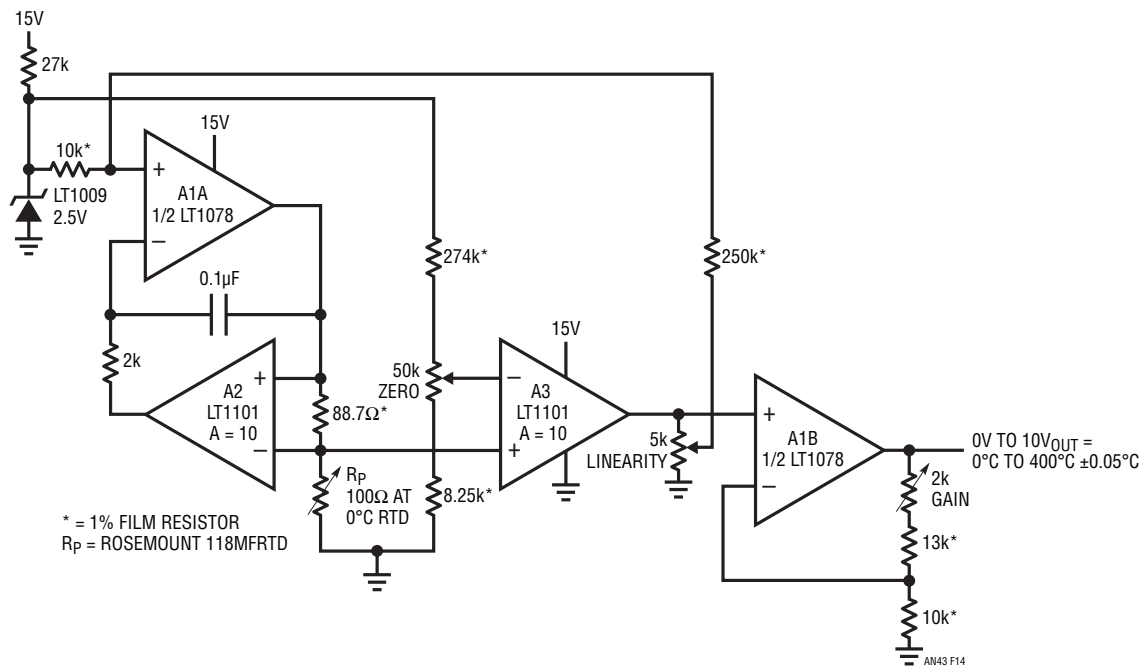


Figure 14. Linearized Platinum RTD Bridge. Feedback to Bridge from A3 Linearizes the Circuit

A1A and instrumentation amplifier A2 form a voltage-controlled current source. A1A, biased by the LT1009 reference, drives current through the 88.7Ω resistor and the RTD. A2, sensing differentially across the 88.7Ω resistor, closes a loop back to A1A. The $2k$ - $0.1\mu F$ combination sets amplifier roll-off, and the configuration is stable. Because A1A's loop forces a fixed voltage across the 88.7Ω resistor, the current through R_p is constant. A1's operating point is primarily fixed by the $2.5V$ LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The nonlinearity could cause several degrees of error over the circuit's $0^\circ C$ to $400^\circ C$ operating range. The bridge's output is fed to instrumentation amplifier A3, which provides differential gain while simultaneously supplying nonlinearity correction. The correction is implemented by feeding a portion of A3's output back to A1's input via the $10k$ - $250k$ divider. This causes the current supplied to R_p to slightly shift with its operating point, compensating sensor nonlinearity to

within $\pm 0.05^\circ C$. A1B, providing additional scaled gain, furnishes the circuit output.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432k) for R_p . Set the box to the $0^\circ C$ value (100.00Ω) and adjust the offset trim for a $0.00V$ output. Next, set the decade box for a $140^\circ C$ output (154.26Ω) and adjust the gain trim for a $3.500V$ output reading. Finally, set the box to 249.0Ω ($400.00^\circ C$) and trim the linearity adjustment for a $10.000V$ output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within $\pm 0.05^\circ C$. The resistance values given are for a nominal 100.00Ω ($0^\circ C$) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω . This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and has a very small error term.

Application Note 43

Figure 15 is functionally identical to Figure 14, except that A2 and A3 are replaced with an LTC1043 switched-capacitor building block. The LTC1043 performs the differential-to-single-ended transitions in the current source and bridge output amplifier. Value shifts in the current source and output stage reflect the LTC1043's lack of gain. The primary trade-off between the two circuits is component count versus cost.

Digitally Corrected Platinum Resistance Bridge

The previous examples rely on analog techniques to achieve a precise, linear output from the platinum RTD bridge. Figure 16 uses digital corrections to obtain similar results. A processor is used to correct residual RTD

nonlinearities. The bridges inherent nonlinear output is also accommodated by the processor.

The LT1027 drives the bridge with 5V. The bridge differential output is extracted by instrumentation amplifier A1. A1's output, via gain scaling stage A2, is fed to the LTC1290 12-bit A/D. The LTC1290's raw output codes reflect the bridges nonlinear output versus temperature. The processor corrects the A/D output and presents linearized, calibrated data out. RTD and resistor tolerances mandate zero and full-scale trims, but no linearity correction is necessary. A2's analog output is available for feedback control applications. The complete software code for the 68HC05 processor, developed by Guy M. Hoover, appears in Figure 17.

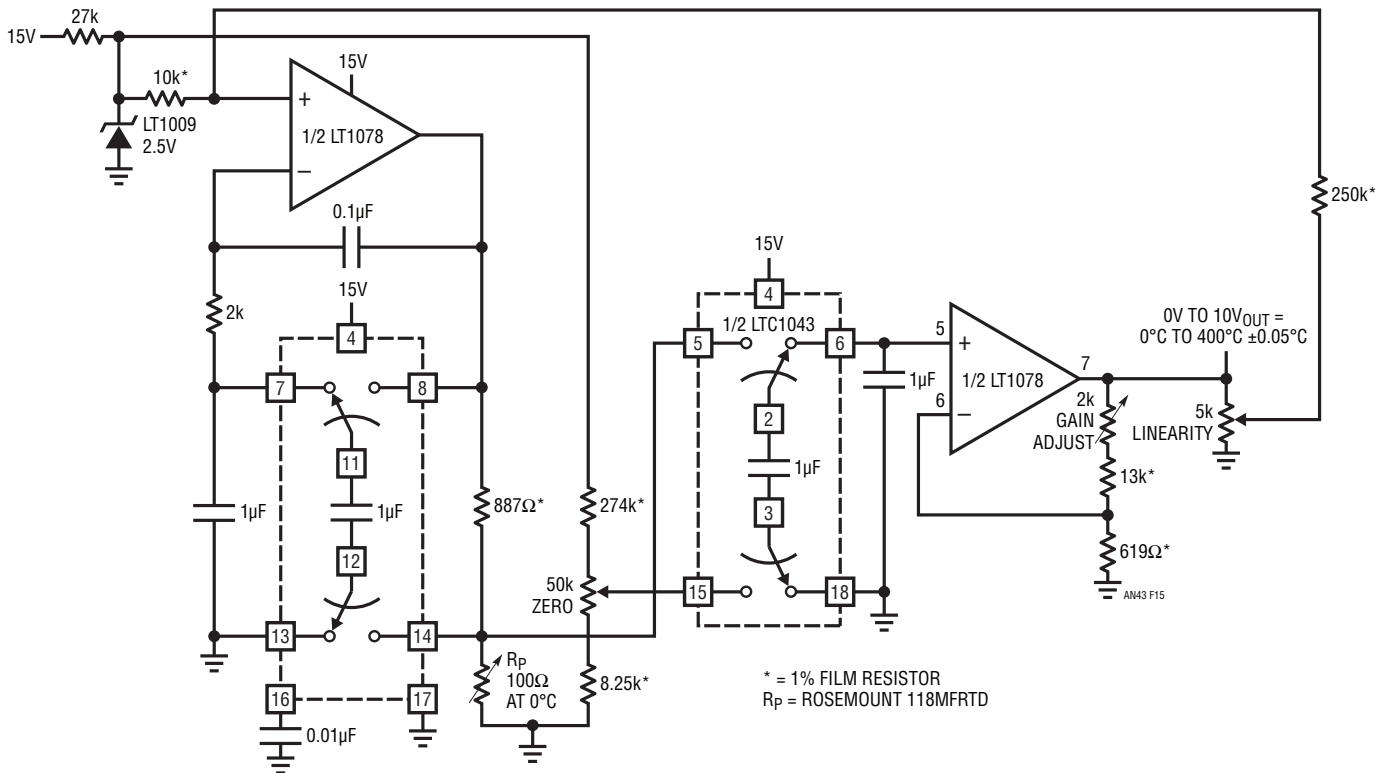


Figure 15. Switched-Capacitor-Based Version of Figure 14

Thermistor Bridge

Figure 18, another temperature measuring bridge, uses a thermistor as a sensor. The LT1034 furnishes bridge excitation. The 3.2k and 6250Ω resistors are supplied with the thermistor sensor. The networks overall response is linearly related to the thermistor's sensed temperature. The network forms one leg of a bridge with resistors furnishing the opposing leg. A trim in this opposing leg sets bridge output to zero at 0°C. Instrumentation amplifier A1 takes gain with A2 providing additional trimmed gain to furnish a calibrated output. Calibration is accomplished in similar fashion to the platinum RTD circuits, with the linearity trim deleted.

Low Power Bridge Circuits

Low power operation of bridge circuits is becoming increasingly common. Many bridge-based transducers are low impedance devices, complicating low power design. The most obvious way to minimize bridge power consumption is to restrict drive to the bridge. Figure 19a is identical to

Figure 5, except that the bridge excitation has been reduced to 1.2V. This cuts bridge current from nearly 30mA to about 3.5mA. The remaining circuit elements consume negligible power compared to this amount. The trade-off is the sacrifice in bridge output signal. The reduced drive causes commensurately lowered bridge outputs, making the noise and drift floor a greater percentage of the signal. More specifically, a 0.01% reading of a 10V powered 350Ω strain gauge bridge requires 3μV of stable resolution. At 1.2V drive, this number shrinks to a scary 360nV.

Figure 19b is similar, although bridge current is reduced below 700μA. This is accomplished by using a semiconductor-based bridge transducer. These devices have significantly higher input resistance, minimizing power dissipation. Semiconductor-based pressure transducers have major cost advantages over bonded strain gauge types, although accuracy and stability are reduced. Appendix A, "Strain Gauge Bridges," discusses trade-offs and theory of both technologies.

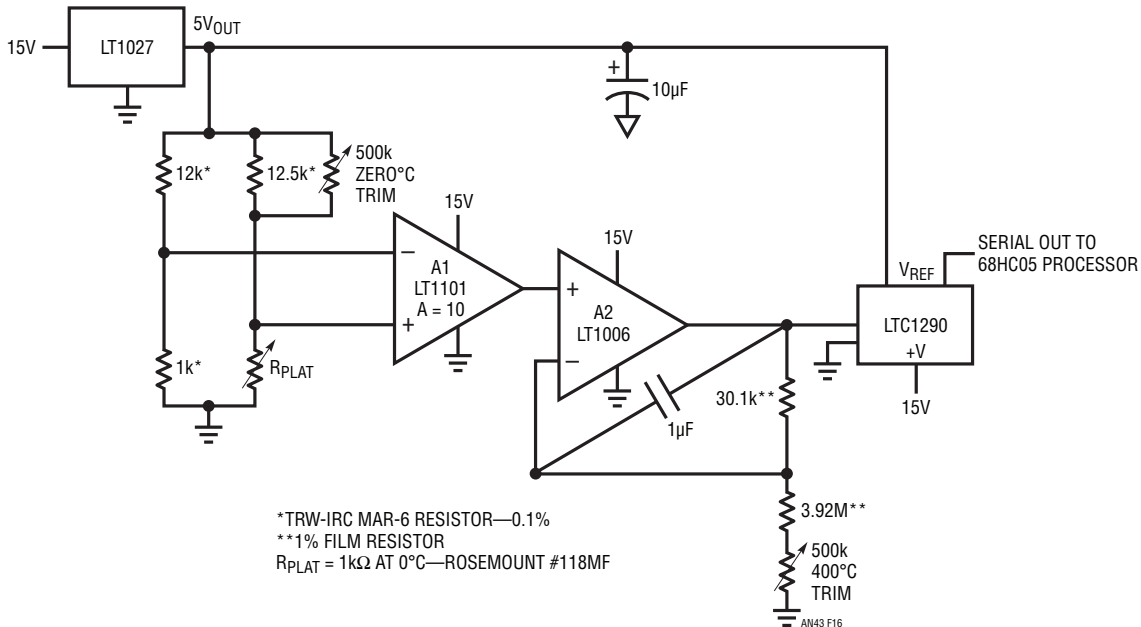


Figure 16. Digitally Linearized Platinum RTD Signal Conditioner

Application Note 43

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*          PLATINUM RTD LINEARIZATION PROGRAM (0.0 TO 400.0 DEGREES C)
*          WRITTEN BY GUY HOOVER LINEAR TECHNOLOGY CORPORATION
*          3/14/90
*          N IS THE NUMBER OF SEGMENTS THAT RTD RESPONSE IS DIVIDED INTO
*          TEMPERATURE (DEG. C*10)=M*X+B
*          M IS SLOPE OF RTD RESPONSE FOR A GIVEN SEGMENT
*          X IS A/D OUTPUT MINUS SEGMENT END POINT
*          B IS SEGMENT START POINT IN DEGREES C *10.
*
*****
*          LOOK UP TABLES
*
*          ORG $1000
*          TABLE FOR SEGMENT END POINTS IN DECIMAL
* X IS FORMED BY SUBTRACTING PROPER SEGMENT END POINT FROM A/D OUTPUT
*          FDB 60,296,527,753,976,1195,1410,1621,1829,2032
*          FDB 2233,2430,2623,2813,3000,3184,3365,3543,3718,3890
*          ORG $1030
*          TABLE FOR M IN DECIMAL
*          M IS SLOPE OF RTD OVER A GIVEN TEMPERATURE RANGE
*          FDB 3486,3535,3585,3685,3735,3784,3884,3934,3984,4083
*          FDB 4133,4232,4282,4382,4432,4531,4581,4681,4730,4830
*          ORG $1060
*          TABLE FOR B IN DECIMAL
*          B IS DEGREES C TIMES TEN
*          FDB 0,200,400,600,800,1000,1200,1400,1600,1800
*          FDB 2000,2200,2400,2600,2800,3000,3200,3400,3600,3800
*          ORG $10FF
*          FCB 39 (N*2)-1 IN DECIMAL
*
*          END LOOK UP TABLES
*****
*          BEGIN MAIN PROGRAM
*
*          ORG $0100
*          LDA #$F7          CONFIGURATION DATA FOR PORT C DDR
*          STA $06          LOAD CONFIGURATION DATA INTO PORT C
*          BSET 0,$02       INITIALIZE B0 PORT C
MES90L  NOP
*          LDA #$2F          DIN WORD FOR 1290 CH4 WITH RESPECT
*          TO CH5, MSB FIRST, UNIPOLAR, 16 BITS
*          STA $50          STORE DIN WORD IN DIN BUFFER
*          JSR READ90       CALL READ90 SUBROUTINE (DUMMY READ)
*          JSR READ90       CALL READ90 SUBROUTINE (MSBS IN $61 LSBS IN $62)
*          LDX $10FF       LOAD SEGMENT COUNTER INTO X          \ FOR N=20 TO 1
DOAGAIN LDA $1000,X       LOAD LSBS OF SEGMENT N              \
*          STA $55          STORE LSBS IN $55                  \
*          DECX            DECREMENT X                          \
*          LDA $1000,X     LOAD MSBS OF SEGMENT N              \
*          STA $54          STORE MSBS IN $54                  \ FIND B
*          JSR SUBTRCT     CALL SUBTRCT SUBROUTINE              /
*          BPL SEGMENT    IF RESULT IS PLUS GOTO SEGMENT       /
*          JSR ADDB       CALL ADDB SUBROUTINE                  /
*          DECX            DECREMENT X                          /
*          JMP DOAGAIN    GOTO CODE AT LABEL DOAGAIN           / NEXT N

```

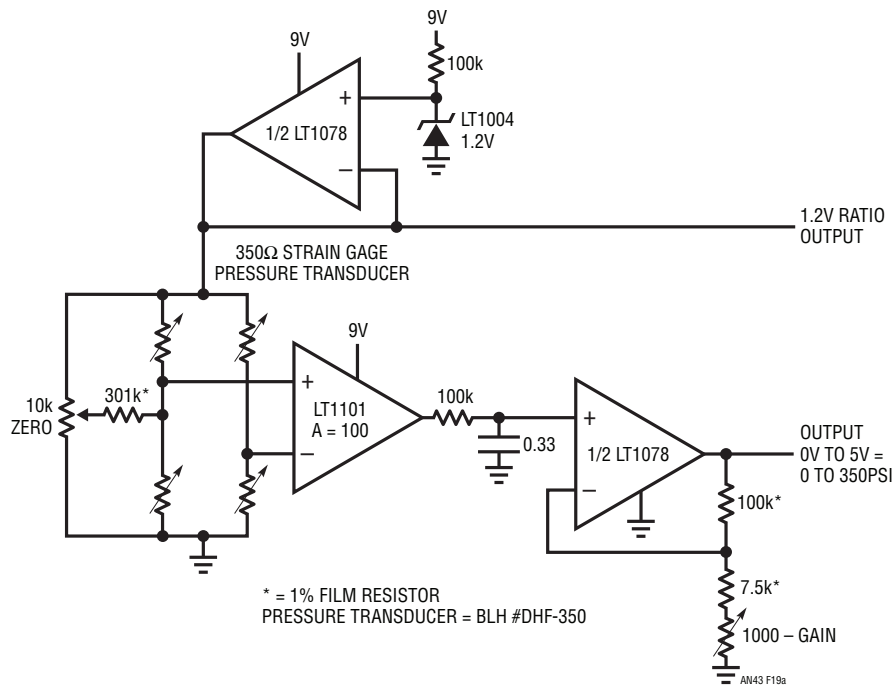
Figure 17. Software Code for 68HC05 Processor-Based RTD Linearization

Application Note 43

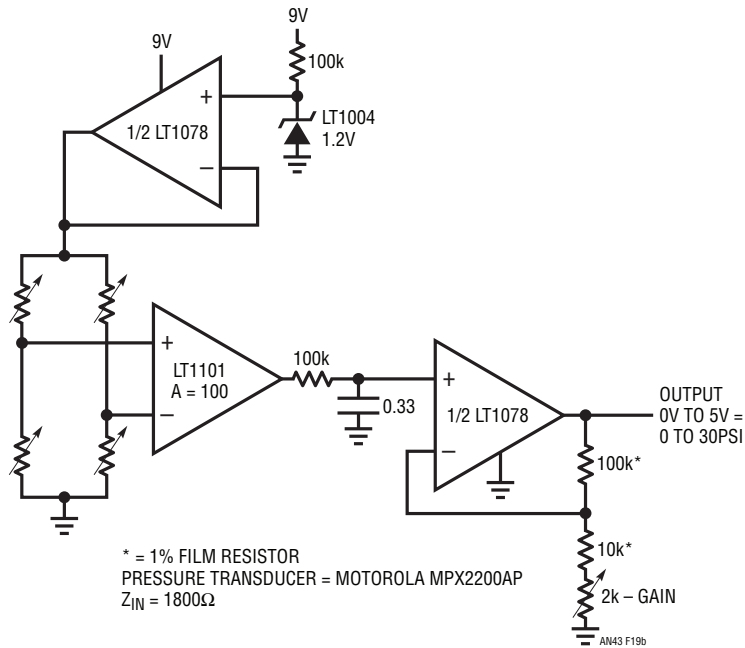
```
*****
*
*          SUBTRCT SUBTRACTS $54 AND $55 FROM $61 AND $62. RESULTS IN $61 AND $62
*
SUBTRCT LDA $62          LOAD LSBS
        SUB $55          SUBTRACT LSBS
        STA $62          STORE REMAINDER
        LDA $61          LOAD MSBS
        SBC $54          SUBTRACT W/CARRY MSBS
        STA $61          STORE REMAINDER
        RTS              RETURN TO MAIN PROGRAM
*
*
*                      END SUBTRCT
*****
*****
*
*ADDB RESTORES $61 AND $62 TO ORIGINAL VALUES AFTER SUBTRCT HAS BEEN PERFORMED
*
ADDB    LDA $62          LOAD LSBS
        ADD $55          ADD LSBS
        STA $62          STORE SUM
        LDA $61          LOAD MSBS
        ADC $54          ADD W/CARRY MSBS
        STA $61          STORE SUM
        RTS              RETURN TO MAIN PROGRAM
*
*
*                      END ADDB
*****
*****
*
*TBMULT MULTIPLIES CONTENTS OF $61 AND $62 BY CONTENTS OF $54 AND $55.
*16 MSBS OF RESULT ARE PLACED IN $61 AND $62
*
TBMULT  CLR $68          CLEAR CONTENTS OF $68 \
        CLR $69          CLEAR CONTENTS OF $69 \ RESET TEMPORARY
        CLR $6A          CLEAR CONTENTS OF $6A / RESULT REGISTERS
        CLR $6B          CLEAR CONTENTS OF $6B /
        STX $58          STORE CONTENTS OF X IN $58. TEMPORARY HOLD REG. FOR X
        LSL $62          MULTIPLY LSBS BY 2 \
        ROL $61          MULTIPLY MSBS BY 2 \
        LSL $62          MULTIPLY LSBS BY 2 \
        ROL $61          MULTIPLY MSBS BY 2 \ MULTIPLY $61 AND $62 BY 16
        LSL $62          MULTIPLY LSBS BY 2 / FOR SCALING PURPOSES
        ROL $61          MULTIPLY MSBS BY 2 /
        LSL $62          MULTIPLY LSBS BY 2 /
        ROL $61          MULTIPLY MSBS BY 2 /
        LDA $62          LOAD LSBS OF 1290 INTO ACC
        LDX $55          LOAD LSBS OF M INTO X
        MUL              MULTIPLY CONTENTS OF $55 BY CONTENTS OF $62
        STA $6B          STORE LSBS IN $6B
        STX $6A          STORE MSBS IN $6A
        LDA $62          LOAD LSBS OF 1290 INTO ACC
        LDX $54          LOAD MSBS OF M INTO X
        MUL              MULTIPLY CONTENTS OF $54 BY CONTENTS OF $62
        ADD $6A          LSBS OF MULTIPLY ADDED TO $6A
        STA $6A          STORE BYTE
        TXA              TRANSFER X TO ACC
```

Figure 17. Software Code for 68HC05 Processor-Based RTD Linearization (Continued)

Application Note 43



(19a)



(19b)

Figure 19. Power Reduction by Reducing Bridge Drive. Circuit is a Low Power Version of Figure 5

Application Note 43

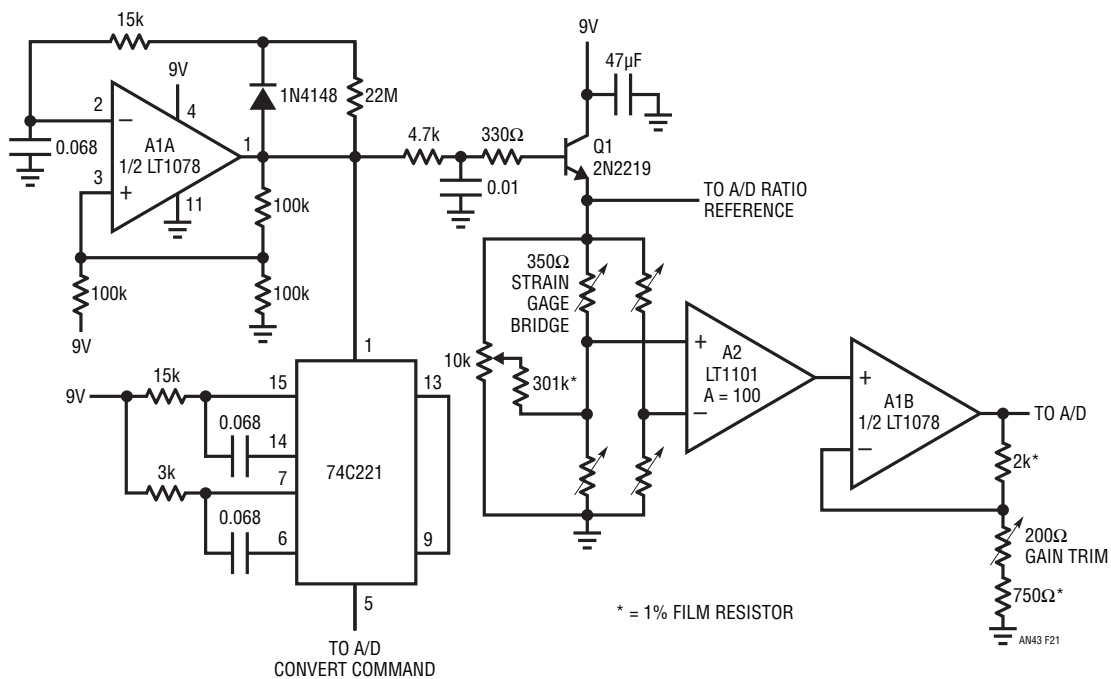


Figure 21. Sampled Output Bridge Signal Conditioner Uses Pulsed Excitation to Save Power

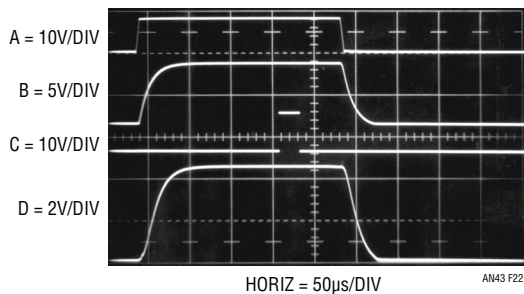


Figure 22. Figure 21's Waveforms. Trace C's Delayed Pulse Ensures A/D Converter Sees Settled Output Waveform (Trace D)

Continuous Output Sampled Bridge Signal Conditioner

Figure 23 extends the sampling approach to include a continuous output. This is accomplished by adding a sample-and-hold stage at the circuit output. In this circuit, Q2 is off when the “sample command” is low. Under these conditions only A2 and S1 receive power, and current drain is inside 60µA. When the sample command is pulsed high, Q2’s collector (Trace A, Figure 24) goes high, providing

power to all other circuit elements. The 10Ω-1µF RC at the LT1021 prevents the strain bridge from seeing a fast rise pulse, which could cause long term transducer degradation. The LT1021-5 reference output (Trace B) drives the strain bridge, and instrumentation amplifier A1 output responds (Trace C). Simultaneously, S1’s switch control input (Trace D) ramps toward Q2’s collector.

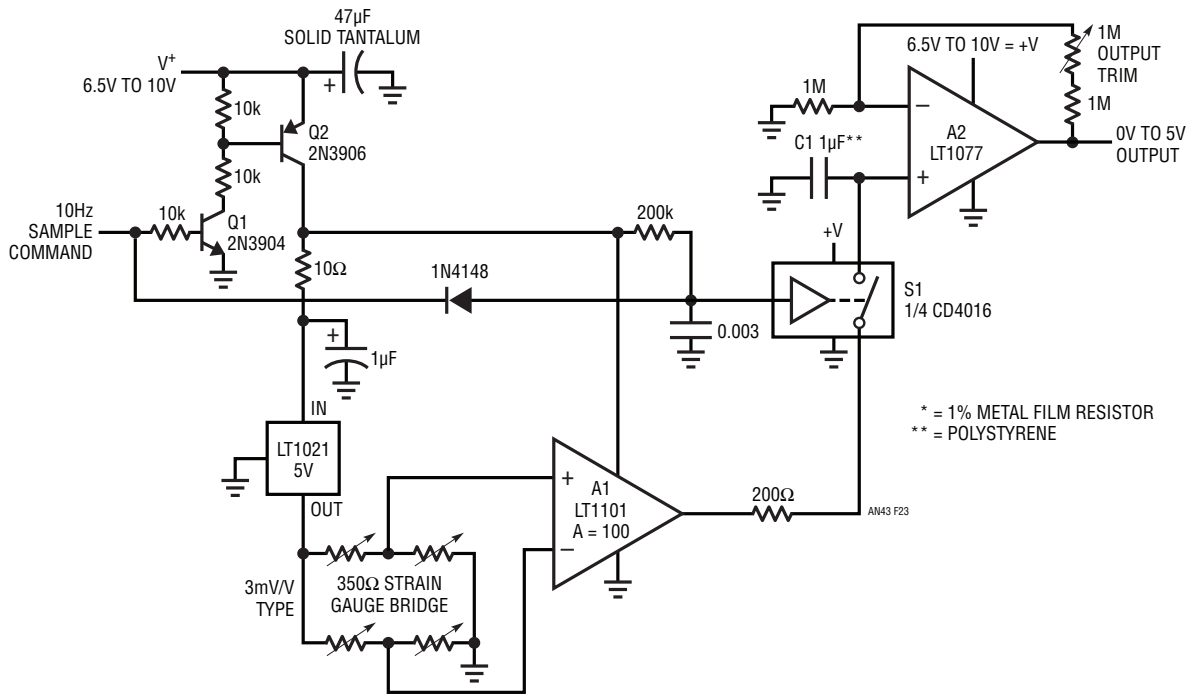


Figure 23. Pulsed Excitation Bridge Signal Conditioner. Sample-Hold Stage Gives DC Output

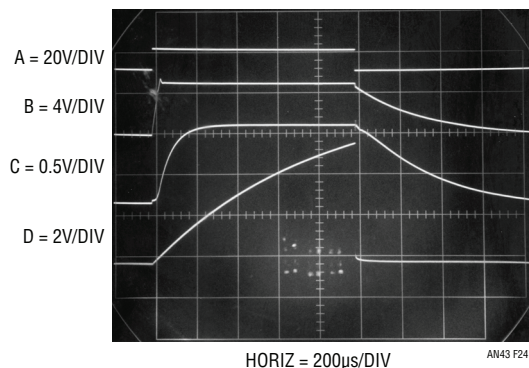


Figure 24. Waveforms for Figure 23's Sampled Strain Gauge Signal Conditioner

Application Note 43

At about one-half Q2's collector voltage (in this case just before mid-screen) S1 turns on, and A1's output is stored in C1. When the sample command drops low, Q2's collector falls, the bridge and its associated circuitry shut down and S1 goes off. C1's stored value appears at gain scaled A2's output. The RC delay at S1's control input ensures glitch-free operation by preventing C1 from updating until A1 has settled. During the 1ms sampling phase, supply current approaches 20mA but a 10Hz sampling rate cuts effective drain below 250 μ A. Slower sampling rates will further reduce drain, but C1's droop rate (about 1mV/100ms) sets an accuracy constraint. The 10Hz rate provides adequate bandwidth for most transducers. For 3mV/V slope factor transducers the gain trim shown allows calibration. It should be rescaled for other types. This circuit's effective current drain is about 250 μ A, and A2's output is accurate enough for 12-bit systems.

It is important to remember that this circuit is a sampled system. Although the output is continuous, information is being collected at a 10Hz rate. As such, the Nyquist limit applies, and must be kept in mind when interpreting results.

High Resolution Continuous Output Sampled Bridge Signal Conditioner

Figure 25 is a special case of sampled bridge drive. It is intended for applications requiring extremely high resolution outputs from a bridge transducer. This circuit puts 100V across a 10V, 350 Ω strain gauge bridge for short periods of time. The high pulsed voltage drive increases bridge output proportionally, without forcing excessive dissipation. In fact, although this circuit is not intended for power reduction, average bridge power is far below the normal 29mA obtained with 10V_{DC} excitation.

Combining the 10 \times higher bridge gain (300mV full scale versus the normal 30mV) with a chopper-stabilized amplifier in the sample-hold output stage is the key to the high resolution obtainable with this circuit.

When oscillator A1A's output is high Q6 is turned on and A2's negative input is pulled above ground. A2's output goes negative, turning on Q1. Q1's collector goes low,

robbing Q3's base drive and cutting it off. Simultaneously, A3 enforces its loop by biasing Q2 into conduction, softly turning on Q4. Under these conditions the voltage across the bridge is essentially zero. When A1A oscillates low (Trace A, Figure 26) RC filter driven Q6 responds by cutting off slowly. Now, A2's negative input sees current only through the 3.6k resistor. The input begins to head negative, causing A2's output to rise. Q1 comes out of saturation, and Q3's emitter (Trace B) rises. Initially this action is rapid (fast rise slewing is just visible at the start of Q3's ascent), but feedback to A2's negative input closes a control loop, with the 1000pF capacitor restricting rise time. The 72k resistor sets A2's gain at 20 with respect to the LT1004 2.5V reference, and Q3's emitter servo controls to 50V.

Simultaneously, A3 responds to the bridges biasing by moving its output negatively. Q2 tends towards cut-off, increasing Q4's conduction. A3 biases its loop to maintain the bridge midpoint at zero. To do this, it must produce a complimentary output to A2's loop, which Trace C shows to be the case. Note that A3's loop roll-off is considerably faster than A2's, ensuring that it will faithfully track A2's loop action. Similarly, A3's loop is slaved to A2's loop output, and produces no other outputs.

Under these conditions the bridge sees 100V drive across it for the 1ms duration of the clock pulse.

A1A's clock output also triggers the 74C221 one-shot. The one-shot delivers a delayed pulse (Trace D) to Q5. Q5 comes on, charging the 1 μ F capacitor to the bridges output voltage. With A3 forcing the bridges left side midpoint to zero, Q5, the 1 μ F capacitor and A4 see a single-ended, low voltage signal. High transient common mode voltages are avoided by the control loops complimentary controlled rise times. A4 takes gain and provides the circuit output. The 74C221's pulse width ends during the bridge's on-time, preserving sampled data integrity. When the A1A oscillator goes high the control loops remove bridge drive, returning the circuit to quiescence. A4's output is maintained at DC by the 1 μ F capacitor. A1A's 1Hz clock rate is adequate to prevent deleterious droop of the 1 μ F capacitor, but slow enough to limit bridge power dissipation. The controlled

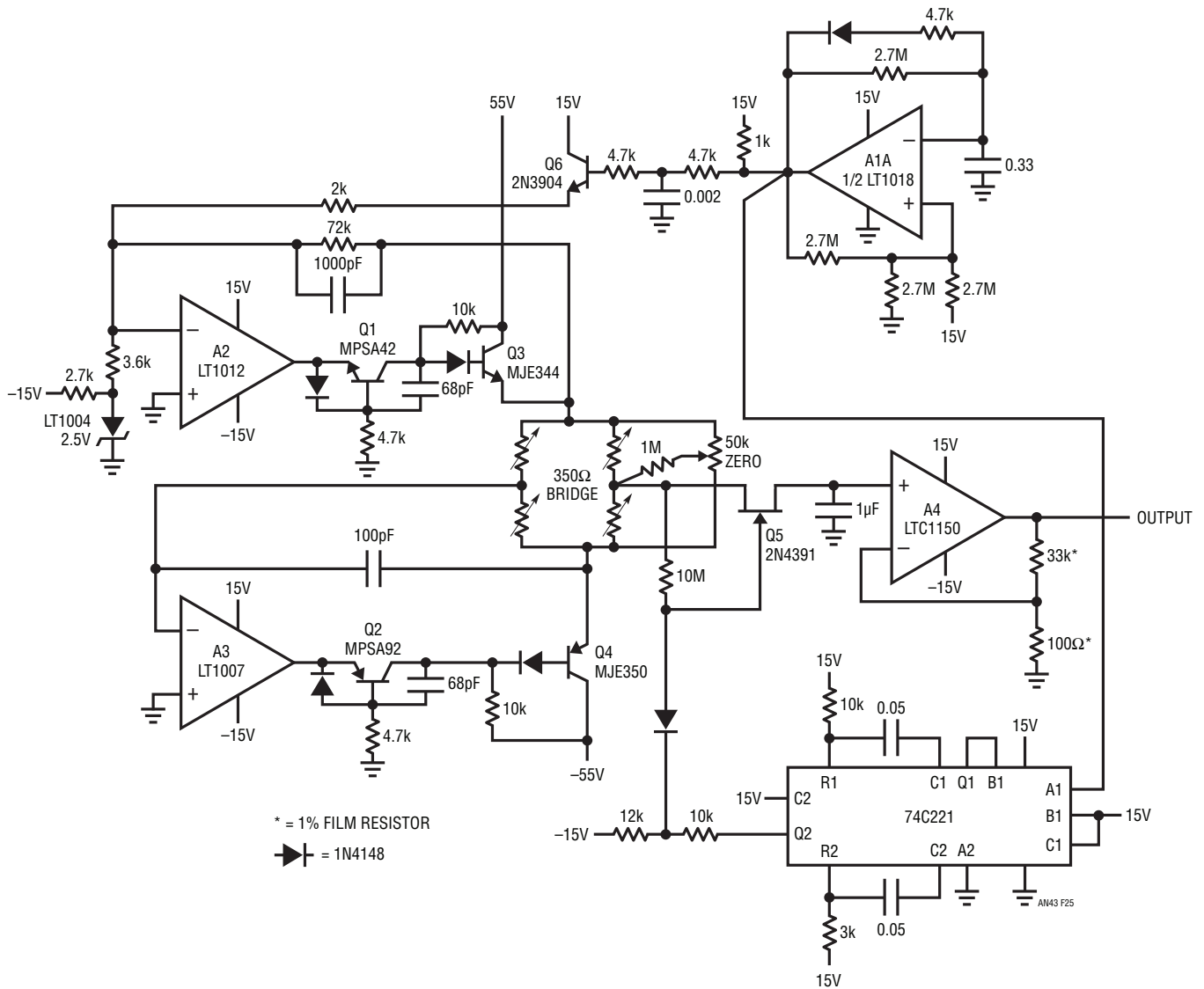


Figure 25. High Resolution Pulsed Excitation Bridge Signal Conditioner. Complementary 50V Drive Increases Bridge Output Signal

rise and fall times across the bridge prevent possible long-term transducer degradation by eliminating high $\Delta V/\Delta T$ induced effects.

When using this circuit it is important to remember that it is a sampled system. Although the output is continuous, information is being collected at a 1Hz rate. As such, the Nyquist limit applies, and must be kept in mind when interpreting results.

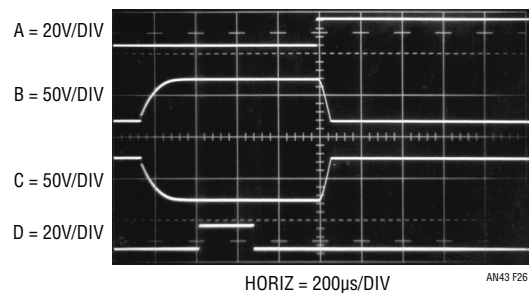


Figure 26. Figure 25's Waveforms. Drive Shaping Results in Controlled, Complementary Bridge Drive Waveforms. Bridge Power is Low Despite 100V Excitation

Application Note 43

AC Driven Bridge/Synchronous Demodulator

Figure 27, an extension of pulse excited bridges, uses synchronous demodulation to obtain very high noise rejection capability. An AC carrier excites the bridge and synchronizes the gain stage demodulator. In this application, the signal source is a thermistor bridge which detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber.

The 500Hz carrier is applied at T1's input (Trace A, Figure 28). T1's floating output drives the thermistor bridge, which presents a single-ended output to A1. A1 operates at an AC gain of 1000. A 60Hz broadband noise source is also deliberately injected into A1's input (Trace B). The carrier's zero crossings are detected by C1. C1's output clocks the LTC1043 (Trace C). A1's output (Trace D) shows the desired 500Hz signal buried within the 60Hz noise source. The LTC1043's zero-cross-synchronized switching at A2's positive input (Trace E) causes A2's gain to alternate between plus and minus one. As a result, A1's output is

synchronously demodulated by A2. A2's output (Trace F) consists of demodulated carrier signal and non-coherent components. The desired carrier amplitude and polarity information is discernible in A2's output and is extracted by filter-averaging at A3. To trim this circuit, adjust the phase potentiometer so that C1 switches when the carrier crosses through zero.

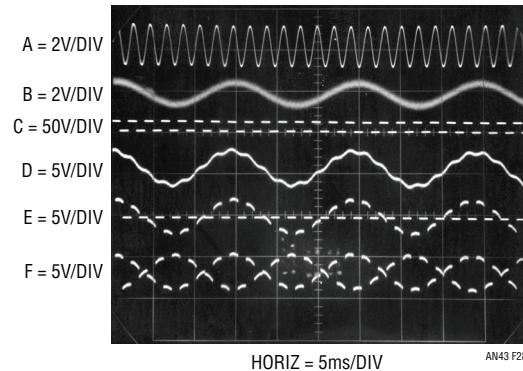


Figure 28. Details of Lock-In Amplifier Operation. Narrowband Synchronous Detection Permits Extraction of Coherent Signals Over 120dB Down

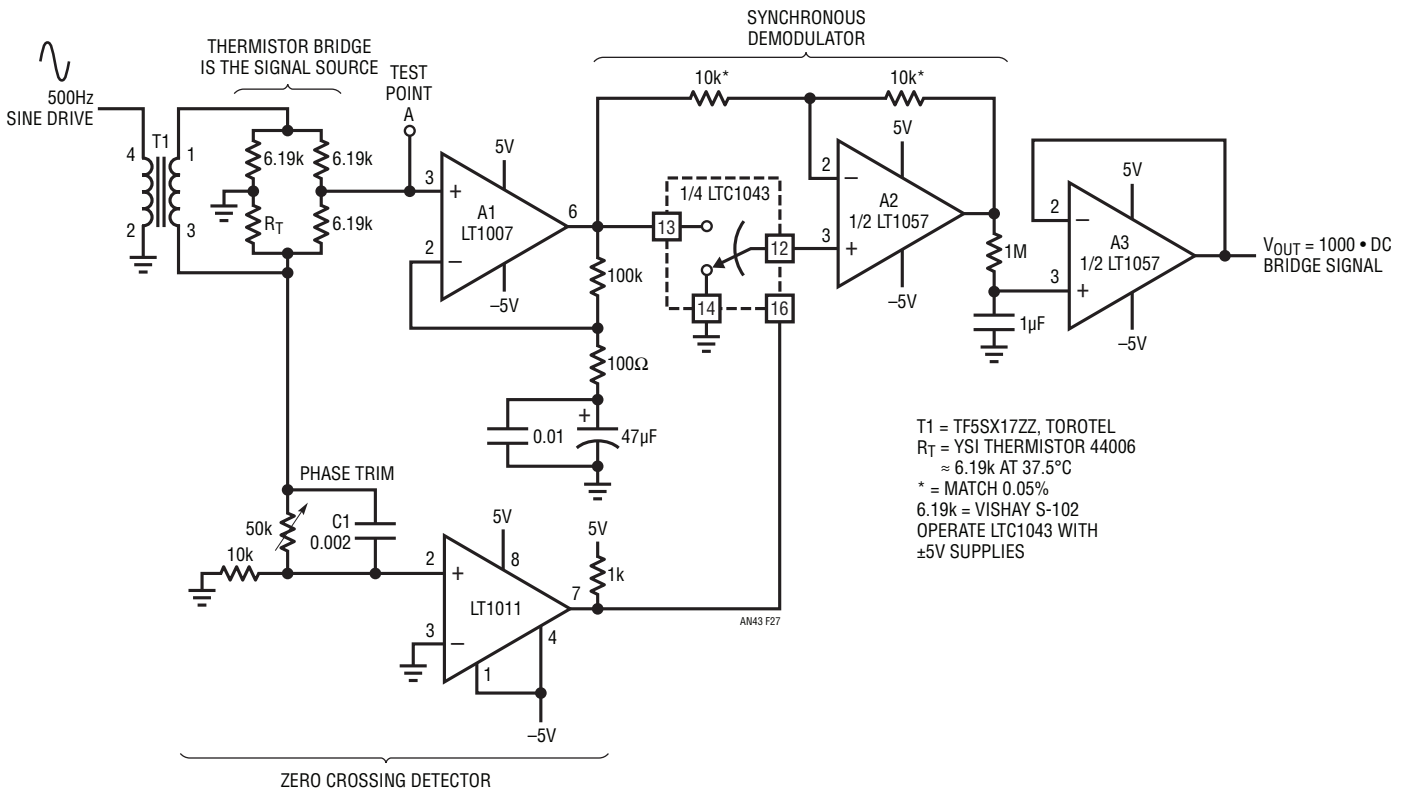


Figure 27. "Lock-In" Bridge Amplifier. Synchronous Detection Achieves Extremely Narrow Band Gain, Providing Very High Noise Rejection

AC Driven Bridge for Level Transduction

Level transducers which measure angle from ideal level are employed in road construction, machine tools, inertial navigation systems and other applications requiring a gravity reference. One of the most elegantly simple level transducers is a small tube nearly filled with a partially conductive liquid. Figure 29a shows such a device. If the tube is level with respect to gravity, the bubble resides in the tube's center and the electrode resistances to common are identical. As the tube shifts away from level, the resistances increase and decrease proportionally. By controlling the tube's shape at manufacture it is possible to obtain a linear output signal when the transducer is incorporated in a bridge circuit.

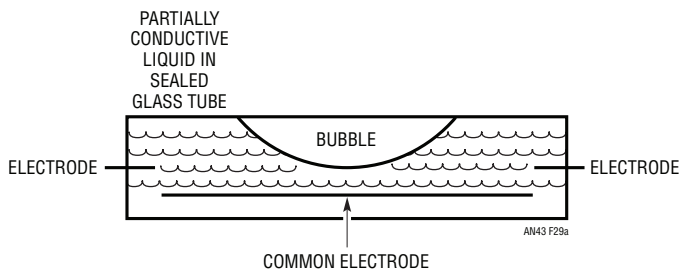


Figure 29a. Bubble-Based Level Transducer

Transducers of this type must be excited with an AC waveform to avoid damage to the partially conductive liquid inside the tube. Signal conditioning involves generating this excitation as well as extracting angle information and polarity determination (e.g., which side of level the tube is on). Figure 29b shows a circuit which does this, directly producing a calibrated frequency output corresponding to level. A sign bit, also supplied at the output, gives polarity information.

The level transducer is configured with a pair of $2k\Omega$ resistors to form a bridge. The required AC bridge excitation is developed at C1A, which is configured as a multivibrator. C1A biases Q1, which switches the LT1009's 2.5V potential

through the $100\mu\text{F}$ capacitor to provide the AC bridge drive. The bridge differential output AC signal is converted to a current by A1, operating as a Howland current pump. This current, whose polarity reverses as bridge drive polarity switches, is rectified by the diode bridge. Thus, the $0.03\mu\text{F}$ capacitor receives unipolar charge. Instrumentation amplifier A2 measures the voltage across the capacitor and presents its single-ended output to C1B. When the voltage across the $0.03\mu\text{F}$ capacitor becomes high enough, C1B's output goes high, turning on the LTC201A switch. This discharges the capacitor. When C1B's AC positive feedback ceases, C1B's output goes low and the switch goes off. The $0.03\mu\text{F}$ unit again receives constant current charging and the entire cycle repeats. The frequency of this oscillation is determined by the magnitude of the constant current delivered to the bridge-capacitor configuration. This current's magnitude is set by the transducer bridge's offset, which is level related.

Figure 30 shows circuit waveforms. Trace A is the AC bridge drive, while Trace B is A1's output. Observe that when the bridge drive changes polarity, A1's output flips sign rapidly to maintain a constant current into the bridge-capacitor configuration. A2's output (Trace C) is a unipolar, ground-referred ramp. Trace D is C1B's output pulse and the circuit's output. The diodes at C1B's positive input provide temperature compensation for the sensor's positive tempco, allowing C1B's trip voltage to ratiometrically track bridge output over temperature.

A3, operating open loop, determines polarity by comparing the rectified and filtered bridge output signals with respect to ground.

To calibrate this circuit, place the level transducer at a known 40 arc-minute angle and adjust the $5k\Omega$ trimmer at C1B for a 400Hz output. Circuit accuracy is limited by the transducer to about 2.5%.

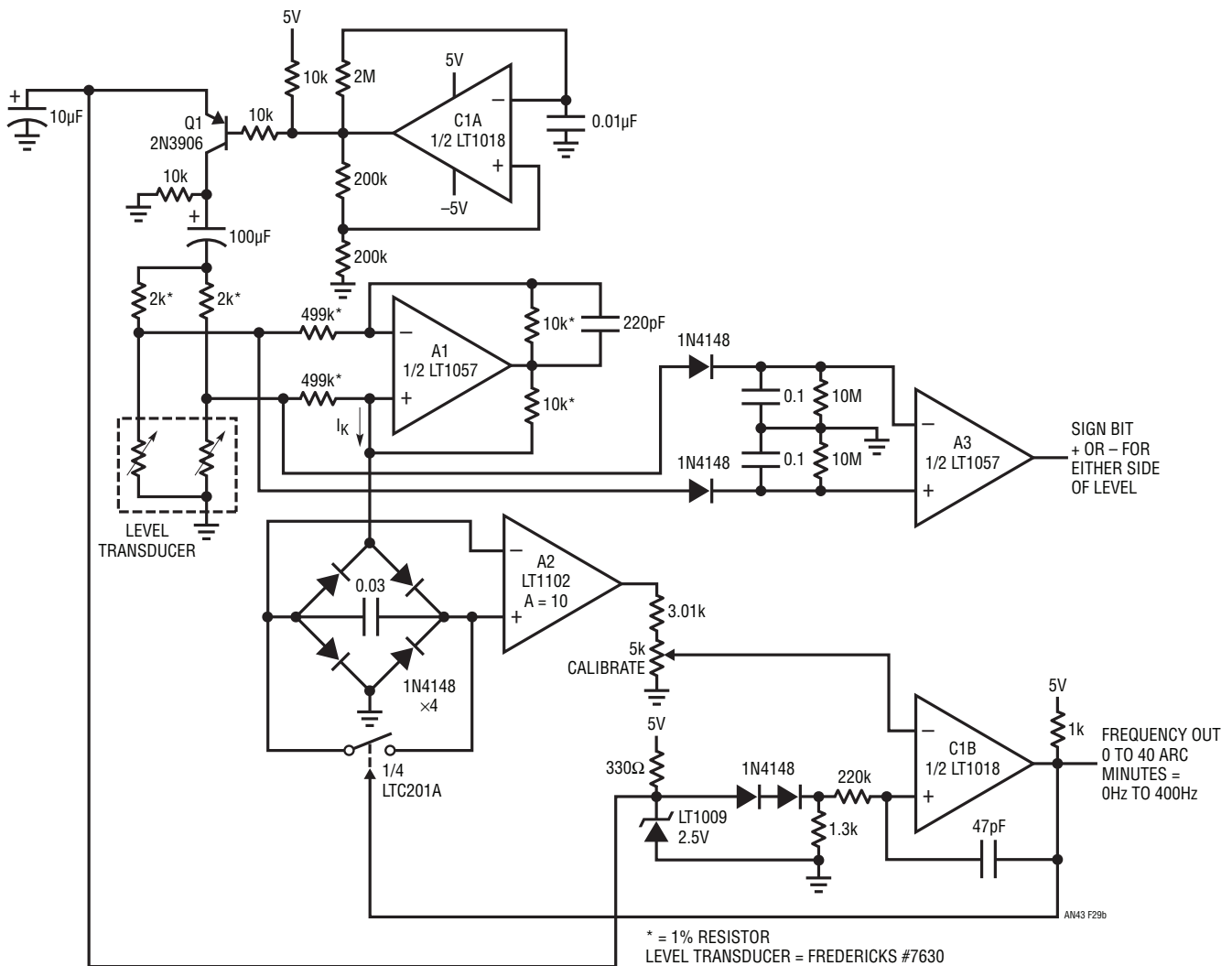


Figure 29b. Level Transducer Digitizer Uses AC Bridge Technique

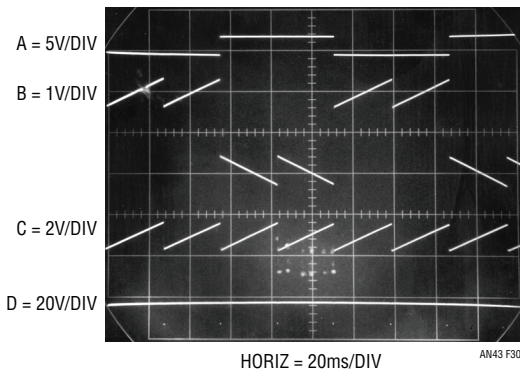


Figure 30. Level Transducer Bridge Circuit's Waveforms

Time Domain Bridge

Figure 31 is another AC-based bridge, but works in the time domain. This circuit is particularly applicable to capacitance measurement. Operation is straightforward. With S1 closed the comparators output is high. When S1 opens, capacitor C_X charges. When C_X 's potential crosses the voltage established by the bridge's left side resistors the comparator trips low. The elapsed time between the switch opening and the comparator going low is proportionate to C_X 's value. This circuit is insensitive to supply and

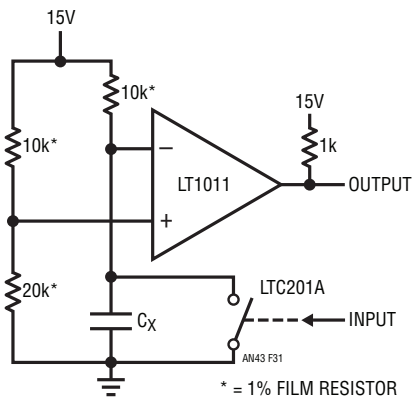


Figure 31. Time Domain Bridge

repetition rate variations and can provide good accuracy if time constants are kept much larger than comparator and switch delays. For example, the LT1011's delay is about 200ns and the LTC201A contributes 450ns. To ensure 1% accuracy the bridge's right side time constant should not drop below 65µs. Extremely low values of capacitance may be influenced by switch charge injection. In such cases switching should be implemented by alternating the bridge drive between ground and +15.

Bridge Oscillator—Square Wave Output

Only an inattentive outlook could resist folding Figure 31's bridge back upon itself to make an oscillator. Figure 32 does this, forming a bridge oscillator. This circuit will also be recognized as the classic op amp multivibrator. In this version the 10k to 20k bridge leg provides switching point hysteresis with C_X charged via the remaining 10k resistor. When C_X reaches the switching point the amplifier's output changes state, abruptly reversing the sign of its positive input voltage. C_X 's charging direction also reverses, and

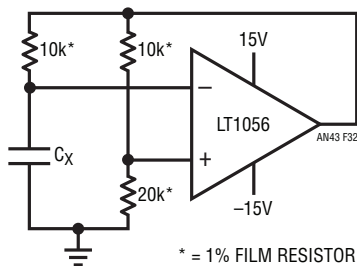


Figure 32. "Bridge Oscillator" (Good Old Op Amp Multivibrator with a Fancy Name)

oscillations continue. At frequencies that are low compared to amplifier delays output frequency is almost entirely dependent on the bridge components. Amplifier input errors tend to ratiometrically cancel, and supply shifts are similarly rejected. The duty cycle is influenced by output saturation and supply asymmetries.

Quartz Stabilized Bridge Oscillator

Figure 33, generically similar to Figure 32, replaces one of the bridge arms with a resonant element. With the crystal removed the circuit is a familiar noninverting gain of 2 with a grounded input. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency. The amplifier output (Trace A, Figure 34) swings in an attempt to maintain input balance. Excessive circuit gain prevents linear operation, and oscillations commence as the amplifier repeatedly overshoots in its attempts to null the bridge. The crystal's high Q is evident in the filtered waveform (Trace B) at the amplifier's positive input.

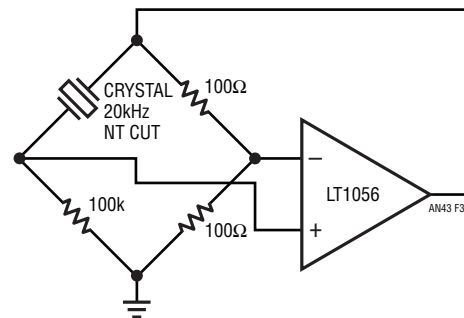


Figure 33. Bridge-Based Crystal Oscillator

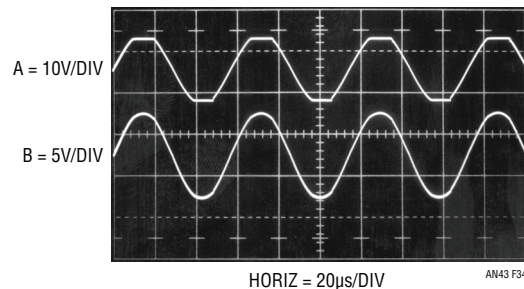


Figure 34. Bridge-Based Crystal Oscillator's Waveforms. Excessive Gain Causes Output Saturation Limiting

Application Note 43

Sine Wave Output Quartz Stabilized Bridge Oscillator

Figure 35 takes the previous circuit into the linear region to produce a sine wave output. It does this by continuously controlling the gain to maintain linear operation. This arrangement uses a classic technique first described by Meacham in 1938 (see References).

In any oscillator it is necessary to control the gain as well as the phase shift at the frequency of interest. If gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting, as in Figure 33. Here, gain control comes from the positive temperature coefficient of the lamp. When power is applied, the lamp is at a low resistance value, gain is high and oscillation amplitude builds. As amplitude builds, the lamp current increases, heating occurs and its resistance goes up. This causes a reduction in amplifier gain and the circuit finds a stable operating point. The 15pF capacitor suppresses spurious oscillation.

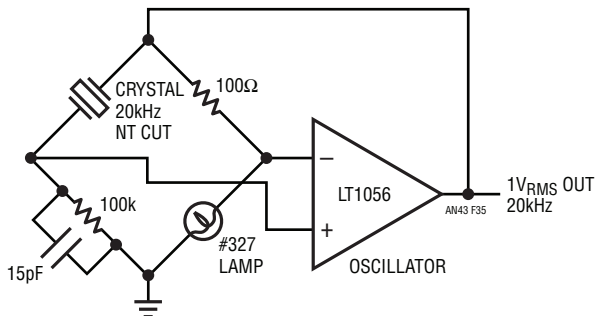


Figure 35. Figure 33 with Lamp Added for Gain Stabilization

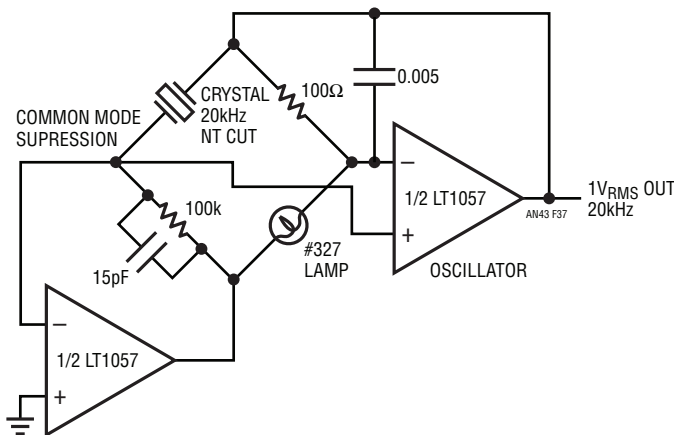


Figure 37. Common Mode Suppression for Quartz Oscillator Lowers Distortion

Operating waveforms appear in Figure 36. The amplifier output (Trace A, Figure 36) is a sine wave, with about 1.5% distortion (Trace B). The relatively high distortion content is almost entirely due to the common mode swing seen by the amplifier. Op amp common mode rejection suffers at high frequency, producing output distortion. Figure 37 eliminates the common mode swing by using a second amplifier to force the bridge's midpoint to virtual ground.³ It does this by measuring the midpoint value, comparing it to ground and controlling the formerly grounded end of the bridge to maintain its inputs at zero. Because the bridge drive is complementary the oscillator amplifier now sees no common mode swing, dramatically reducing distortion. Figure 38 shows less than 0.005% distortion (Trace B) in the output (Trace A) waveform.

Note 3: Sharp-eyed readers will recognize this as an AC version of the DC common mode suppression technique introduced back in Figure 6.

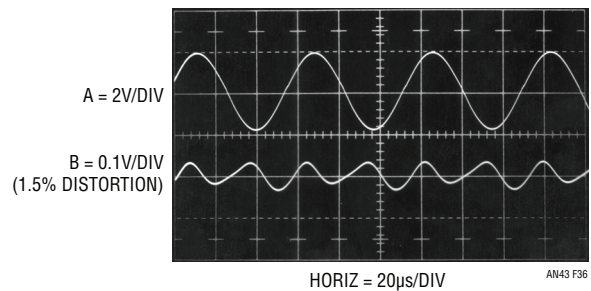


Figure 36. Lamp-Based Amplitude Stabilization Produces Sine Wave Output

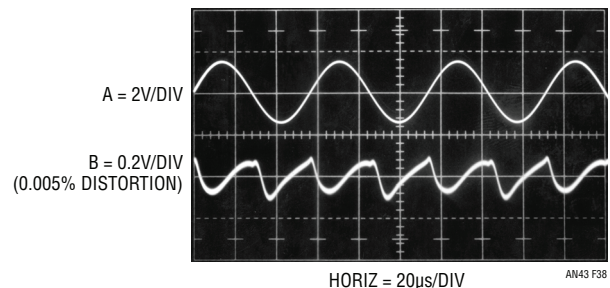


Figure 38. Distortion Measurements for Figure 37. Common Mode Suppression Permits 0.005% Distortion

Wien Bridge-Based Oscillators

Crystals are not the only resonant elements that can be stabilized in a gain-controlled bridge. Figure 39 is a Wien bridge (see References) based oscillator. The configuration shown was originally developed for telephony applications. The circuit is a modern adaptation of one described by a Stanford University student, William R. Hewlett,⁴ in his 1939 masters thesis (see Appendix C, “The Wien Bridge and Mr. Hewlett”).

The Wien network provides phase shift governed by the equation listed, and the lamp regulates amplitude in accordance with Figure 35’s description. Figure 40 is a variable frequency version of the basic circuit. Output frequency range spans 20Hz to 20kHz in three decade ranges, with 0.25dB amplitude flatness.

Note 4: History records that Hewlett and his friend David Packard made a number of these type oscillators. Then they built some other kinds of instruments.

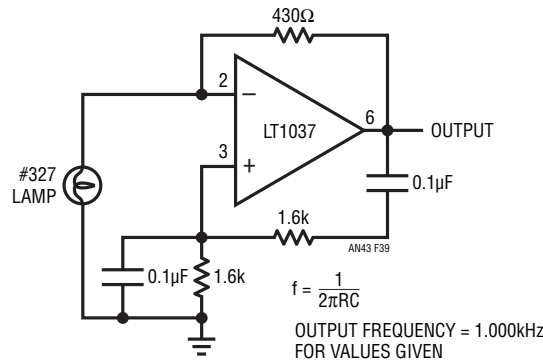


Figure 39. Wien Bridge-Based Sine Wave Oscillator. Simple, Modern Version of an Old Circuit Has 0.0025% Distortion

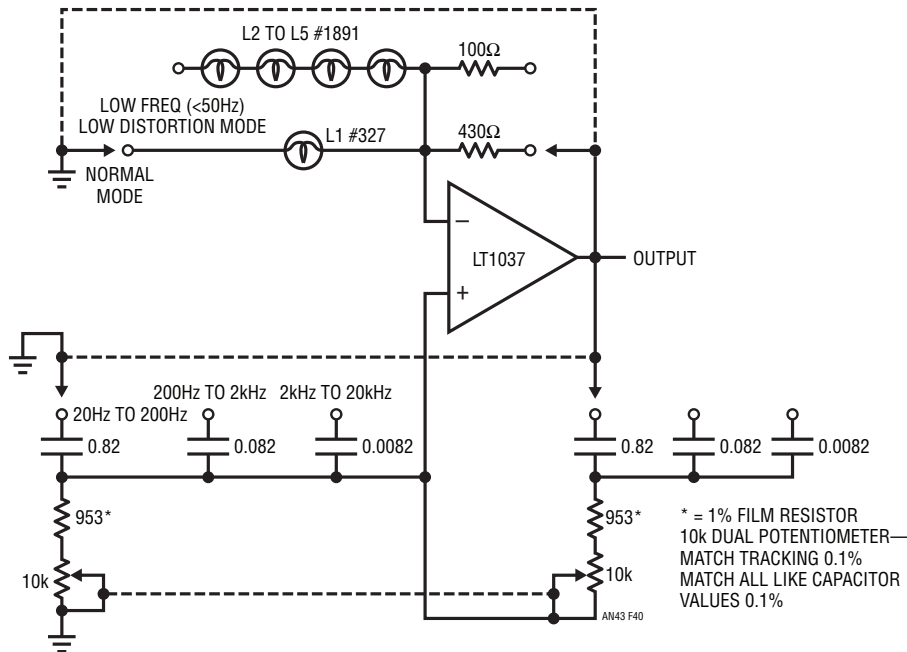


Figure 40. Multirange Wien Bridge-Based Oscillator. Multiple Lamps Provide Lowered Distortion at Low Frequencies

Application Note 43

The smooth, limiting nature of the lamp's operation, in combination with its simplicity, gives good results. Trace A, Figure 41, shows circuit output at 10kHz. Harmonic distortion, shown in Trace B, is below 0.003%. The trace shows that most of the distortion is due to second harmonic content and some crossover disturbance is noticeable. The low resistance values in the Wien network and the $3.8\text{nV}/\sqrt{\text{Hz}}$ noise specification of the LT1037 eliminate amplifier noise as an error term.

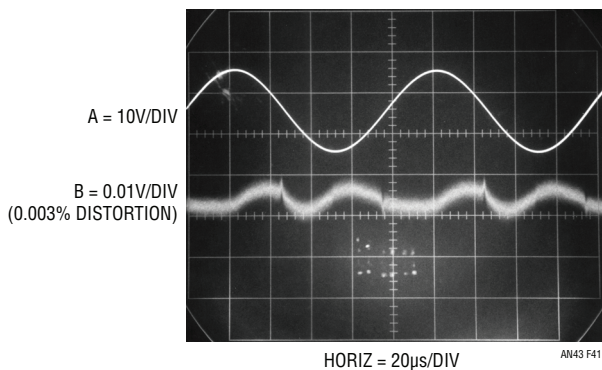


Figure 41. Figure 40's Distortion Characteristic at 10kHz

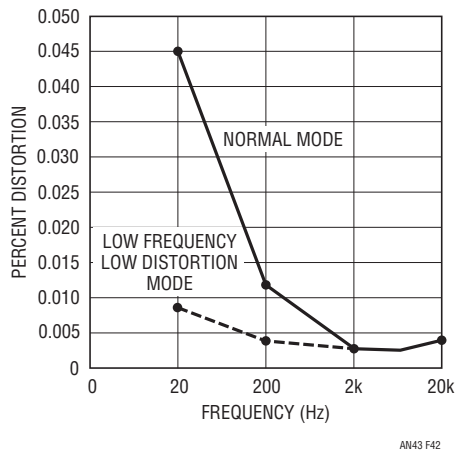


Figure 42. Figure 40's Distortion vs Frequency

At low frequencies, the thermal time constant of the small normal mode lamp begins to introduce distortion levels above 0.01%. This is due to "hunting" as the oscillator's frequency approaches the lamp thermal time constant. This effect can be eliminated, at the expense of reduced output amplitude and longer amplitude settling time, by switching to the low frequency, low distortion mode. The four large lamps give a longer thermal time constant and distortion is reduced. Figure 42 plots distortion versus frequency for the circuit.

Figure 43's version replaces the lamp with an electronic amplitude stabilization loop. The LT1055 compares the oscillator's positive output peaks with a DC reference. The diode in series with the LT1004 reference provides temperature compensation for the rectifier diode. The op amp biases Q1, controlling its channel resistance. This influences loop gain, which is reflected in oscillator output amplitude. Loop closure around the LT1055 occurs, stabilizing oscillator amplitude. The $15\mu\text{F}$ capacitor stabilizes the loop, with the 22k resistor settling its gain.

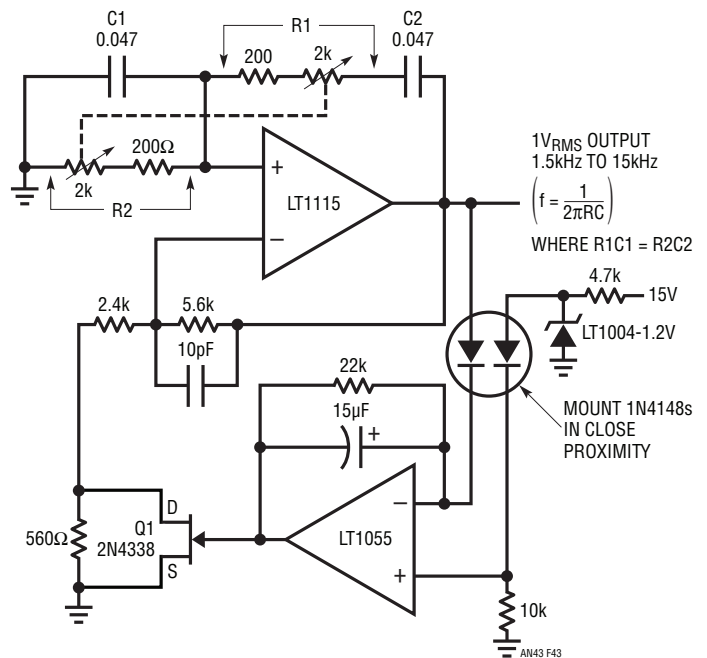


Figure 43. Replacing the Lamp with an Electronic Equivalent

Distortion performance for this circuit is quite disappointing. Figure 44 shows 0.15% 2f distortion (Trace B) in the output (Trace A), a huge increase over the lamp-based approach.⁵ This distortion does not correlate with the rectifier peaking residue present at Q1's gate (Trace C). Where is the villain in this scheme?

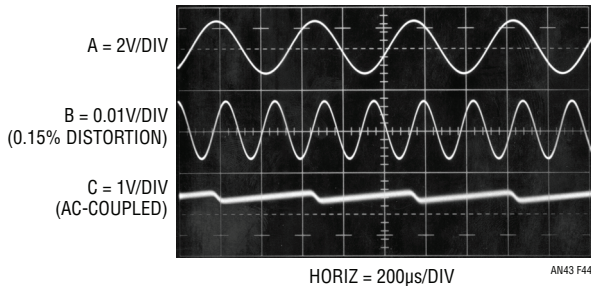


Figure 44. Figure 43 Produces Excessive Distortion Due to Q1's Channel Resistance Modulation

The culprit turns out to be Q1. In a FET, gate voltage theoretically sets channel resistance. In fact, channel voltage also slightly modulates channel resistance. In this circuit Q1's channel sees large swings at the fundamental. This swing combines with the channel voltage-resistance modulation effect, producing distortion.

The cure for this difficulty is local feedback around Q1. Properly scaled, this feedback nicely cancels out the

parasitic. Figure 45 shows the circuit redrawn with the inclusion of Q1's local loop. The 20k trimmer allows adjustment to optimize distortion performance. Figure 46 shows results. Distortion (Trace B) drops to 0.0018% and is composed of 2f, some gain loop rectification artifacts and noise. For reference the circuit's output (Trace A) and the LT1055 output (Trace C) are shown.

Figure 47 eliminates the trim, provides increased voltage and current output, and slightly reduces distortion. Q1 is replaced with an optically driven CdS photocell. This device has no parasitic resistance modulation effects. The LT1055 has been replaced with a ground sensing op amp

Note 5: What else should be expected when trying to replace a single light bulb with a bunch of electronic components? I can hear Figure 39's #327 lamp laughing.

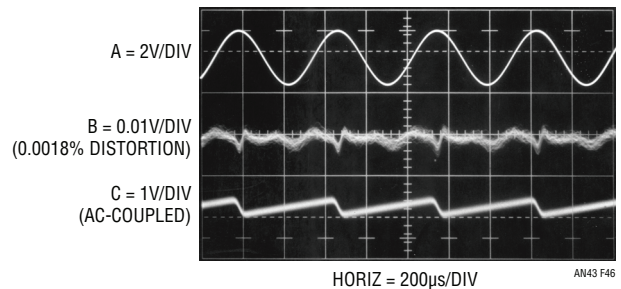


Figure 46. Figure 45's 0.0018% Distortion Characteristic

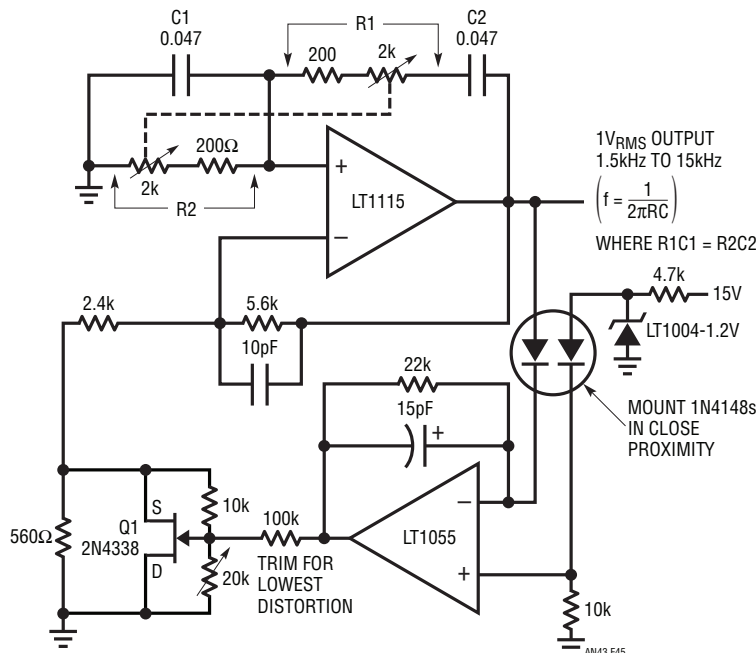


Figure 45. Local Feedback Around Q1 Cures Channel Resistance Modulation, Reducing Distortion to 0.0018%

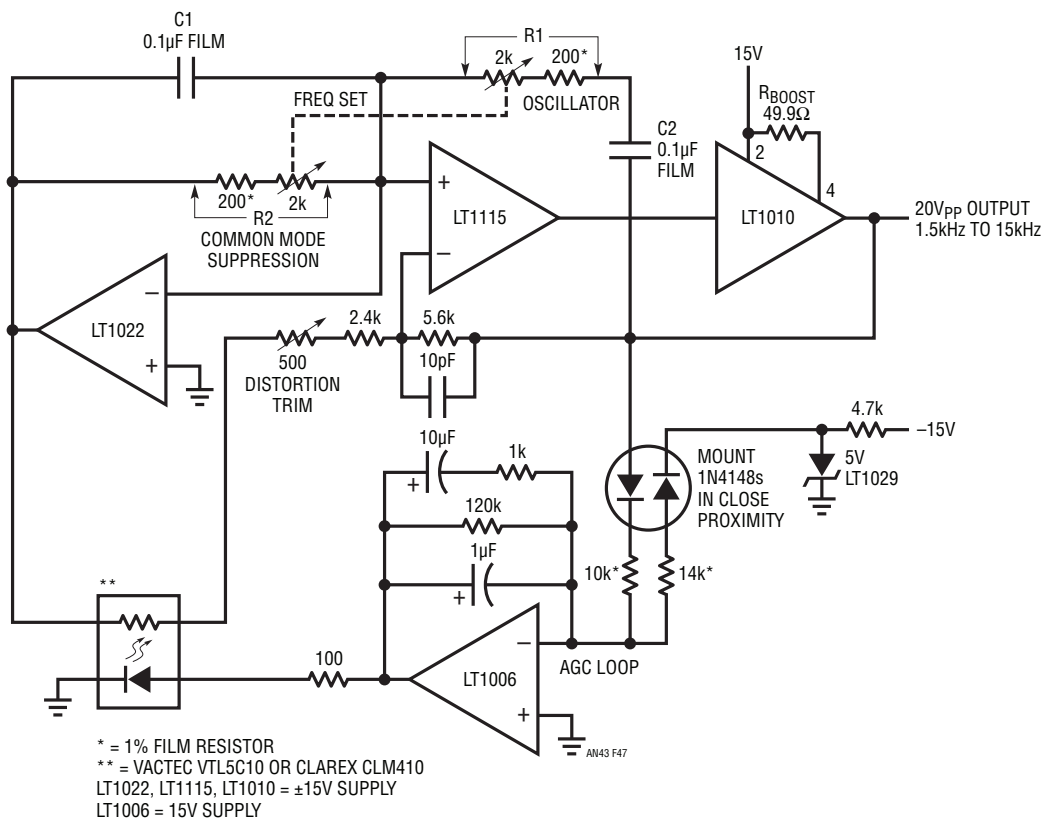


Figure 47. Replacing Q1 with an Optically Driven CdS Photocell Eliminates Resistance Modulation Trim

running in single supply mode. This permits true integrator operation and eliminates any possibility of reverse biasing the (downsized) feedback capacitor. Additional feedback components aid step response.⁶ Distortion performance improves slightly to 0.0015%.

The last Wien bridge-based circuit borrows Figure 37's common mode suppression technique (which is simply an AC version of Figure 6's DC common mode suppression loop) to reduce distortion to vanishingly small levels. The LT1022 amplifier appears in Figure 48. This amplifier forces the midpoint of the bridge to virtual ground by servo biasing the formerly grounded bridge legs. As in Figure 37, common mode swing is eliminated, reducing distortion. The circuit's output (Trace A, Figure 49) contains less than 0.0003% (3ppm) distortion (Trace B), with no

visible correlation to gain loop ripple residue (Trace C). This level of distortion is below the uncertainty floor of most distortion analyzers, requiring specialized equipment for meaningful measurement. (See Appendix D, guest written by Bruce Hofer of Audio Precision, Inc., for a discussion on distortion measurement considerations.)

Diode Bridge-Based 2.5MHz Precision Rectifier/AC Voltmeter

A final circuit shows a way to achieve low AC error switching with diode bridge techniques. Diode bridges provide faster, cleaner signal switching than any other technique.

Note 6: A much better scheme for a low ripple, fast response gain control loop is nicely detailed in the operating and service manual supplied with the Hewlett-Packard HP339A Distortion Analyzer.

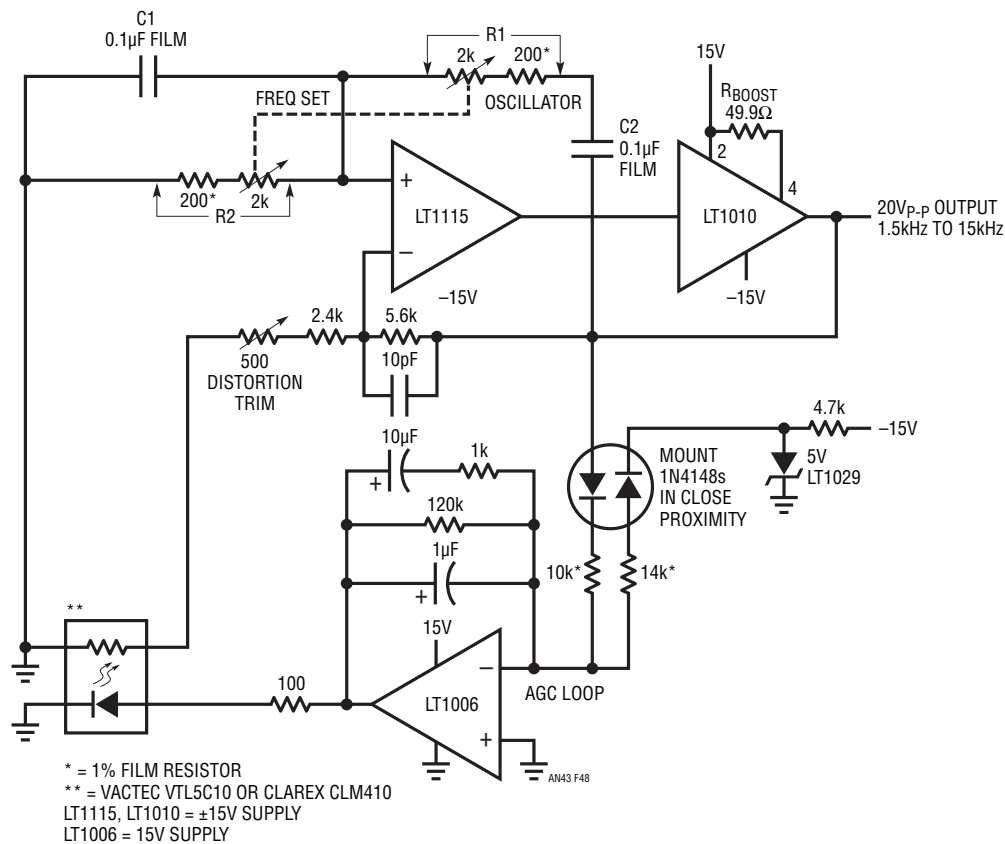


Figure 48. Adding Common Mode Suppression Lowers Distortion to 0.0003%

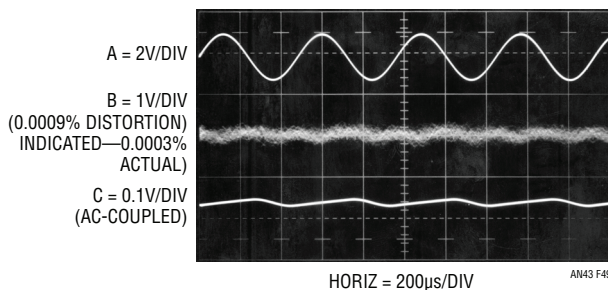


Figure 49. Figure 48's 3ppm Distortion is Below the Noise Floor of Most Analyzers

Most precision rectifier circuits rely on operational amplifiers to correct for diode drops. Although this scheme works well, bandwidth limitations usually restrict these circuits to operation below 100kHz. Figure 50 shows the LT1016 comparator in an open-loop, synchronous

rectifier configuration which has high accuracy out to 2.5MHz. An input 1MHz sine wave (Trace A, Figure 51) is zero cross detected by C1. Both of C1's outputs drive identical level shifters with fast (delay = 2ns to 3ns), ±5V outputs. These outputs bias a Schottky diode switching bridge (Traces B and C are the switched corners of the bridge). The input signal is fed to the left midsection of the bridge. Because C1 drives the bridge synchronously with the input signal, a half-wave rectified sine appears at the AC output (Trace D). The RMS value appears at the DC output. The Schottky bridge gives fast switching without charge pump-through. This is evident in Trace E, which is an expanded version of Trace D. The waveform is clean with the exception of very small disturbances where bridge switching occurs. To calibrate this circuit, apply a 1MHz to 2MHz 1V_{p-p} sine wave and adjust the

Application Note 43

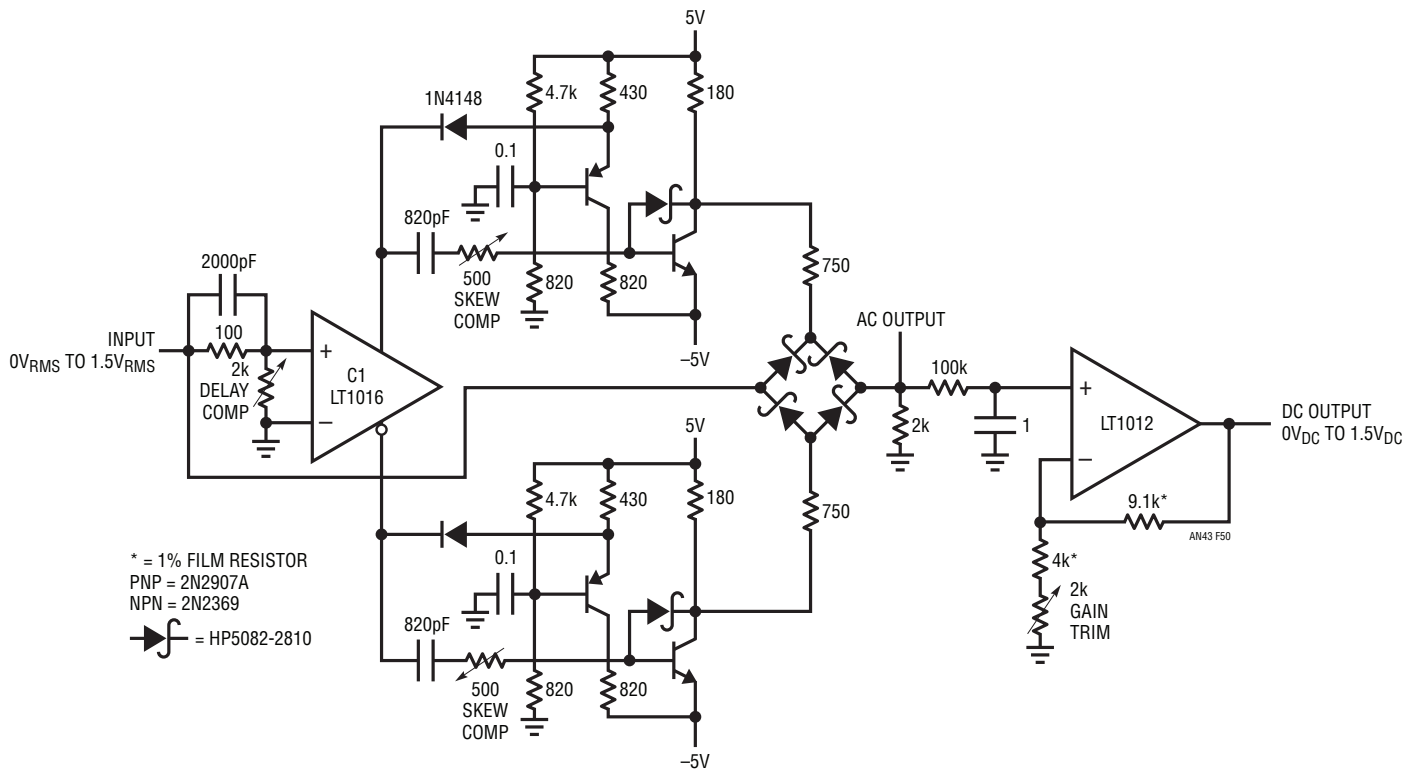


Figure 50. Fast, Bridge-Switched Synchronous Rectifier-Based AC/DC Converter

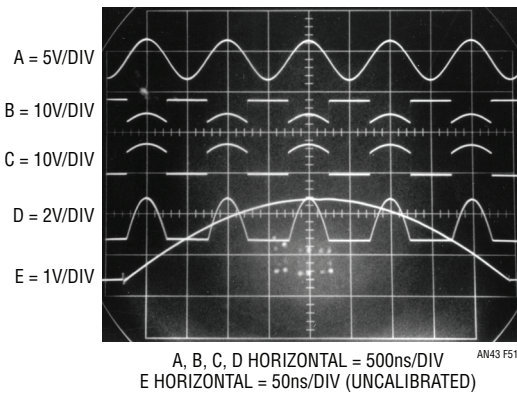


Figure 51. Fast AC/DC Converter Operating at 1MHz. Clean Switching is Due to Bridge Symmetry and Compensations for Delay and Switching Skew

delay compensation so bridge switching occurs when the sine crosses zero. The adjustment corrects for the small delays through the LT1016 and the level shifters. Next, adjust the skew compensation potentiometers for minimum aberrations in the AC output signal. These trims slightly shift the phase of the rising output edge of their respective level shifter. This allows skew in the complementary bridge drive signals to be kept within 1 ns to 2ns, minimizing output disturbances when switching occurs. A 100mV sine input will produce a clean output with a DC output accuracy of better than 0.25%.

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

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Application Note 43

APPENDIX A

STRAIN GAUGE BRIDGES

In 1856 Lord Kelvin discovered that applying strain to a wire shifted its resistance. This effect is repeatable, and is the basis for electrical output strain measurement. Early devices were simply wires suspended between two insulated points (Figure A1). The force to be measured mechanically biased the wire, changing its resistance. Modern devices utilize foil-based designs. The conductive material is deposited on an insulated carrier (Figure A2). Physically they take many forms, allowing for a variety of applications. The gages¹ are usually configured in a bridge and mounted on a beam (Figure A3), forming a transducer.

A useful transducer must be trimmed for zero and gain, and compensated for temperature sensitivity. Figure A4 shows a typical arrangement. Zero is set with a parallel trim, with similar treatment used to set gain. The gain trims include modulus gages to compensate beam material temperature sensitivity. Arranging these trims and completing the mechanical integration involves a fair amount of artistry, and is usually best left to specialists.²

Note 1: The correct spelling is gauge, but prolonged grammatical assaults have assassinated the “u.” Hence, “gage” assumes a claim to legitimacy.

Note 2: Those finding their sense of engineering prowess unalterably offended are referred to “SR-4 Strain Gage Handbook,” available from BLH Electronics, Canton, Massachusetts. Have fun.

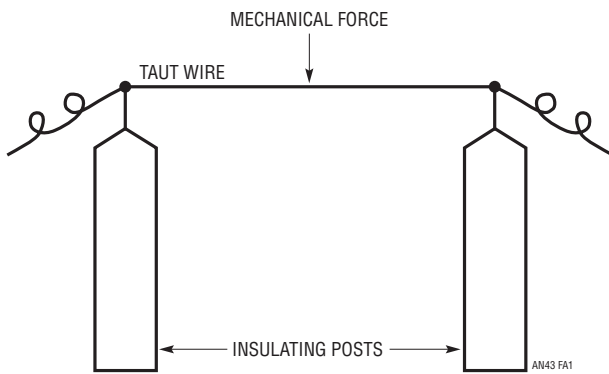


Figure A1. A Very Basic Strain Gauge

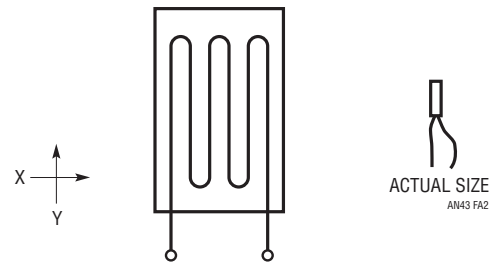


Figure A2. A Conceptual Strain Gage. Maximum Device Sensitivity is with Y-Axis Flexing Into the Page. Practical Devices Utilize Denser Patterns with Optimized Distribution of Conductive Material

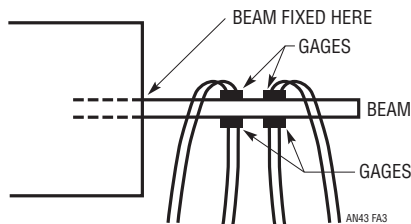


Figure A3. A Conceptual Strain Gauge Transducer. Bending Force On the Beam Causes Resistance Shifts

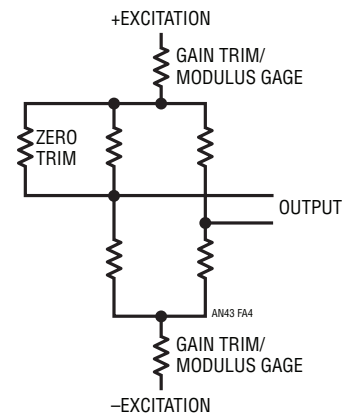


Figure A4. Simplified Strain Gauge Transducer Schematic

Semiconductor-based strain gage transducers utilize resistive shift in semiconducting materials. These devices, built in monolithic IC form, are considerably less expensive than manually assembled foil-based strain gage transducers. They have over ten times the sensitivity of foil-based devices, but are more sensitive to temperature and other effects. As such, they are best suited to somewhat less demanding applications than foil-based gages. Their monolithic construction and small size offer price and convenience advantages in many applications. Electrical form is similar to foil-based designs (e.g., a bridge configuration), although impedance levels are about ten times higher. The following guest written section details their characteristics.

SEMICONDUCTOR BASED STRAIN GAGES

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Strain gage technology, while based on a phenomena which dates back to the nineteenth century, has been of major importance in the areas of stress analysis, structural testing and transducer fabrication for more than 40 years.

First reports on semiconductor piezoresistive technology dates back to the observation by C.S. Smith³ in the early 1950's of large piezoresistive coefficients in Silicon and Germanium.

There are several advantages to implementing strain gages using semiconductor technology. The immediate one is the very high gage factors of approximately two orders of magnitude higher than metallic gages. These higher gage factors allow improved signal-to-noise ratios for the measurement of small dynamic stresses and simplifies the signal conditioning circuitry.

Another advantage is the precise control of the piezoresistive coefficients including magnitude, sign, and the possibility of transverse and shear responses. Additional advantages are low cost, small size, and compatibility with semiconductor processing technology which allows for integration of additional circuit elements (i.e., operational

amplifiers) on the same chip. The first phase of integration for silicon pressure sensors occurred when the strain gage and the diaphragm were combined into one monolithic structure. This was accomplished using the piezoresistive effect in semiconductors. A strain gage can be diffused or ion-implanted into a thin silicon diaphragm which has been chemically etched into a silicon substrate.

Piezoresistivity

In order to understand the implementation in silicon of strain gages, it is necessary to review the piezoresistive effect in silicon.

The analytic description of the piezoresistive effect in cubic silicon can be reduced to two equations which demonstrate the first order effects.

$$\Delta E_1 = P_0 I_1 (\pi_{11} X_1 + \pi_{12} X_2) \quad (1)$$

$$\Delta E_2 = P_0 I_2 \pi_{44} X_6 \quad (2)$$

where ΔE_1 and ΔE_2 are electric field flux density, P_0 is the unstressed bulk resistivity of silicon, I_s are the excitation current density, π_s are piezoresistive coefficients and X_s are stress tensors due to the applied force.

The effect described by equation (1) is that utilized in a pressure transducer of the Wheatstone bridge type. Regardless of whether the designer chooses N-type or P-type layers for the diffused sensing element, the piezoresistive coefficients π_{11} and π_{12} equation (1) will be oppose in sign.

This implies that through careful placement, and orientation with respect to the crystallographic axis, as well as a sufficiently large aspect ratio for the resistors themselves, it is possible to fabricate resistors on the same diaphragm which both increase and decrease respectively from their nominal values with the application of stress.

The effect described by equation (2) is typically neglected as a parasitic in the design of a Wheatstone bridge device. A closer look at its form, however, reveals that the incremental electrical field flux density, ΔE_2 , due to the applied stress, X_6 , is monotonically increasing for increasing X_6 .

Note 3: Smith C.S., "Piezoresistance Effect in Germanium and Silicon," Physical Review, Volume 94, November 1, 1954 Pages 42-49.

Application Note 43

In fact, equation (2) predicts an extremely linear output since it depends on only one piezoresistive coefficient and one applied stress. Furthermore, the incremental electric field can be measured by a single stress sensitive element. This forms the theoretical basis for the design of the transverse voltage or shear stress piezoresistive strain gage.

Shear Stress Strain Gage

Figure A5 shows the construction of a device which optimizes the piezoresistive effect of equation (2).⁴ The diaphragm is anisotropically etched from a silicon substrate. The piezoresistive element is a single, 4-terminal strain gage that is located at the midpoint of the edge of the square diaphragm at an angle of 45 degrees as shown in Figure A5. The orientation of 45 degrees and location at the center of the edge of the diaphragm maximizes the sensitivity to shear stress, X_6 , and the shear stress being sensed by the transducer by maximizing the piezoresistive coefficient, π_{44} .

Excitation current is passed longitudinally through the resistor (Pins 1 and 3) and the pressure that stresses

the diaphragm is applied at a right angle to the current flow. The stress establishes a transverse electric field in the resistor that is sensed as an output voltage at Pins 2 and 4, which are the taps located at the midpoint of the resistor. The single element shear-stress strain gage can be viewed as the mechanical analog of a Hall effect device. Figure A6 shows a cross section of a pressure transducer implemented in silicon and using the technique described. A differential pressure sensor chip is accomplished by opening the back side of the wafer.

Temperature Compensation and Calibration

The transverse voltage shear stress piezoresistive pressure transducer has been shown to present certain advantages over the Wheatstone bridge configuration. Specifically, improved linearity, and a more consistent reproducible offset (since it is defined by a single photolithographic step), as well as the added advantage of integrating stresses over a smaller percentage of the flexural element.

Very predictably, the transducer exhibits a negative temperature coefficient of span with a nominal value of 0.19%/°C, as well as a temperature coefficient of offset that can be in the range of $\pm 15\mu\text{V}/^\circ\text{C}$ or slightly larger before compensation. TC of span is due to the decrease of the piezoresistive coefficients with temperature due to increased thermal scattering in the lattice structure.

Note 4: J.E. Gragg, U.S. Patent 4,317,126

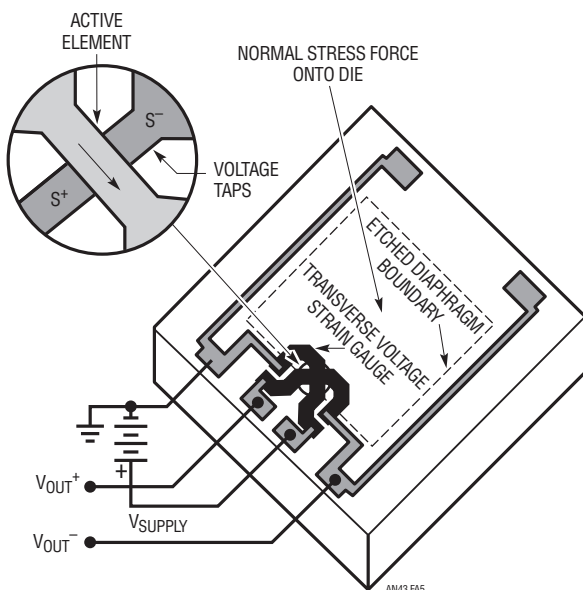


Figure A5. Basic Sensor Element—Top View

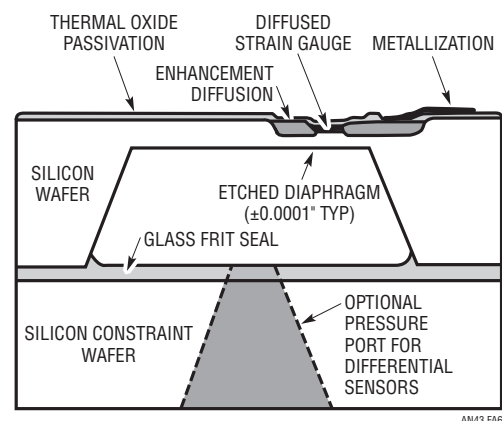


Figure A6. Cross Section of Pressure Transducer

First let's consider the relationship of output voltage, ΔV_O , with excitation voltage, V_{EX} , as predicted by equation (2).

$$\Delta V_O = w/l (\pi_{44} X_6) V_{EX} \quad (3)$$

It is apparent that the output voltage varies directly with excitation, by a factor $w/l(\pi_{44}X_6)$, or conversely that the output is ratiometric to the excitation, V_{EX} .

A typical output characteristic for an uncompensated transducer with a constant V_{EX} applied is shown in Figure A7. Hence, it is apparent that by increasing the supply voltage at the same rate that the full-scale span is decreasing, the undesired temperature dependence of span may be eliminated. This is accomplished by means of a very low TCR resistor placed in series with the transducer excitation legs which, by design, have a TCR of 0.24%/°C (Figure A8). If the value of the zero-TCR span resistor is appropriately chosen, it will decrease the "net" TCR of the combination to the ideal +0.19%/°C required to exactly compensate the negative TC of SPAN. This technique is known as "self-compensation," and can be utilized in the described manner or with a constant current excitation and a parallel TC span compensation resistor.

The passive circuit utilized to achieve calibration and temperature compensation is shown in Figure A8. Since the single element design uses only one resistor for both the input and the output, a self-compensation scheme can be employed. This technique utilizes the temperature

coefficient of the input resistance (TCR) to generate a temperature dependent voltage. The TCR of the strain gage has been specifically designed to be greater in absolute value than the temperature coefficient of the span, so placing additional passive resistive elements in series with the strain gage modifies the effective TCR and allows temperature compensation based on the input resistance value at room temperature. A constant voltage source is all that is necessary external to the device to ensure accurate operation over a wide temperature range.

The self-compensation technique eliminates the requirement for thermistors which are used in most externally compensated Wheatstone bridge pressure sensors. In addition to the cost and nonlinearity characteristics of thermistors, their negative temperature coefficient precludes their integration on silicon. Thin film resistors, on the other hand, are easily deposited on the strain gage substrate using techniques similar to those required for the metallization of wire bond pads used to make connection to external leads. The laser trimming technique is similar to that used in the manufacturing of high accuracy, monolithic, 16-bit analog-to-digital and digital-to-analog data converters, except that in the case of a pressure transducer, the silicon diaphragm is exercised over the pressure range during the trimming procedure.

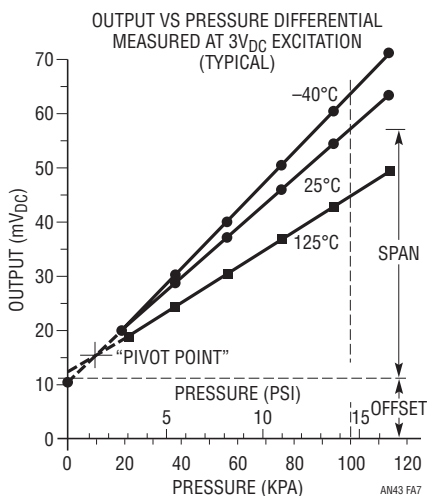


Figure A7. Output Span for Uncompensated Transducer

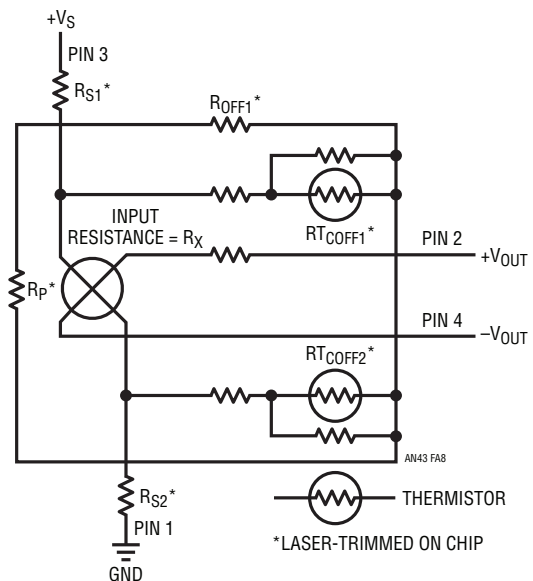


Figure A8. On-Chip Temperature Compensation and Calibration

Application Note 43

Four separate functions are accomplished by the laser trimming operation:

- 1) Zero calibration
- 2) Zero temperature compensation
- 3) Full-scale span temperature compensation
- 4) Full-scale span calibration

The sequence in which the trimming operation is performed is important to avoid interaction of components and the addition of several iterations to the trimming process. The main factor that allows high volume manufacturing techniques, however, is the ability to achieve temperature compensation in the single element sensor without the necessity to change the temperature during the trim operation. Measurements of the sensor parameters are made prior to the laser trim operation. Computer calculations determine which resistors must be trimmed and the amount of trimming required. Resistor R_{OFF1} and R_{OFF2} act as a part of a voltage divider used to calibrate the offset. The output voltage is set to zero with zero pressure applied by trimming either offset resistor R_{OFF1} or R_{OFF2} .

To temperature compensate the offset, thermistors RT_{COFF1} and RT_{COFF2} , a series of diffused silicon resistors with positive temperature coefficient and different values, are added as required to the circuit by cutting aluminum shorting links.

Full-scale span temperature compensation is accomplished by utilizing self temperature compensation—the addition of a single, series resistor to the input circuit when a constant voltage supply is used. The resistor is adjusted to compensate for changes in span with temperature by adjusting the magnitude of the excitation voltage applied to the active element. In order to minimize common mode errors, the “resistor” is actually split between the supply and ground side of the input so that $RS1 = RS2$. The span is adjusted to meet the specification by trimming resistor R_P , which is in parallel with the input resistance of the active element. The parallel resistor actually interacts with the series self-compensation network to provide a series-parallel temperature compensation which enhances the performance over the temperature range.

Performance of Compensated Sensors

The specification for key parameters of a 30PSI on-chip temperature compensated pressure sensor is shown in Figure A9. The excellent linearity is a result of the small active area of the single element strain gage—essentially a point condition. The temperature compensation which is achieved over 0°C to 85°C can be compared to commonly available alternatives.

PARAMETER	MIN	TYP	MAX
Pressure Range (in kPA)	—	—	100
Full-Scale Span (in mV)	38.5	40	41.5
Zero Pressure Offset (in mV)	—	+0.05	+1.0
Sensitivity (mV/PSI)	—	1.38	—
Linearity (% FS)	—	+0.1	+0.25
TEMPERATURE EFFECT FOR 0°C TO 85°C			
Full-Scale Span (% FS)	—	+0.5	+1.0
Offset (in mV)	—	+0.5	+1.0

Figure A9. Specifications for a Typical Pressure Transducer

APPENDIX B

BRIDGE READOUT—THEN AND NOW

The contemporary monolithic components used to read bridge signals are the beneficiaries of almost 150 years of dedicated work in bridge readout mechanisms. Some early schemes made fiendishly ingenious use of available technology to achieve remarkable performance. Figure B1 shows a light beam galvanometer. This device easily resolved currents in the nanoampere range. The unknown current passed through a coil, producing a magnetic field. The coil is mounted within a static magnetic field. The two field's interactions mechanically biased a small mirror, which was centrally mounted on a tautly suspended wire. The mirror may be thought of as the elastically constrained shaft of a DC motor. The amplitude and sign of the coil current produced corresponding torque—like mirror movements. A collimated light source was bounced off the mirror, and its reflection collected on a surface equipped with calibrated markings. The instruments high inherent sensitivity, combined with the gain in the optical angle, provided excellent results.

The tangent galvanometer (Figure B2) achieved similar nanoampere resolution. The actual meter movement was a compass, centrally mounted within a circular coil. Coil

current is measured by noting compass deflection from the earth's magnetic north. Current flow is proportional to the tangent of the measured deflection angle.

These and similar devices were referred to as “null detectors.” This nomenclature was well chosen, and reflected the fact that bridges were almost always read at null. This was so because the only technology available to accurately digitize electrical measurements was passive. “Bridge balances,” including variable resistors, resistance decade boxes and Kelvin-Varley dividers, were cornerstones of absolute measurements. No source of stable, calibrated gain was available; although the null detectors provided high sensitivity. As such, bridge measurement depended on highly accurate balancing technology and sensitive null detectors.

Lee DeForest's triode (1908) began the era of electronic gain. Harold S. Black attempted to patent negative feedback in 1928, but the U.S. Patent Office, in their governmental wisdom, treated him as a crackpot. Black published in the 1930s, and the notion of feedback stabilized gain was immediately utilized by more enlightened types.



Figure B1. The Light Beam Galvanometer is Essentially a Sensitive Meter Movement. It Takes Gain in the Optical Angle of a Mirror Reflected, Collimated Light Source (Courtesy the J. M. Williams Collection)



Figure B2. A Tangent Galvanometer Measures Small Currents by Indicating the Interaction Between Applied Current and the Earth's Magnetic Field. Absolute Current Value is Proportional to the Tangent of the Compass Deflection Angle (Courtesy the J. M. Williams Collection)

Application Note 43

The technology of the day did not permit development of feedback-based amplifiers which could challenge conventional bridge techniques. While Hewlett could use feedback to build a dandy sinewave oscillator, it simply was not good enough to replace Kelvin-Varley dividers and null detectors. Doing so required amplifiers with very high open-loop gains and low zero drift. The second requirement was notably difficult and elusive.

E.A. Goldberg invented the chopper-stabilized amplifier in 1948, finally making stable zero performance practical. Electronic analog computers quickly followed, and historic George A. Philbrick Researches produced the first commercially available general purpose op amps in the 1950s.

Null detectors were the first bridge components to feel the impact of all this. A number of notable chopper-stabilized bridge null detectors were produced during the 1950s and 1960s. All of these were essentially chopper-based operational amplifiers configured as complete instruments. Notable among these was the Julie Research Laboratories sub-microvolt sensitivity ND-103, which featured a 93Hz mechanical chopper (to avoid any interaction with 60Hz noise components). The Hewlett-Packard HP-425 had similar sensitivity, and used a small synchronous clock motor, photocells and incandescent lamps¹ in an elegantly simple photo-chopping scheme. Latter versions of this instrument (the HP-419A) were completely solid

state, although retaining a neon lamp-photocell chopping arrangement. Battery operation permitted floating the instrument across the bridge.

Concurrent to all this was the development of rackmounting-based devices called “instrumentation amplifiers.” These devices, designed to be applied at the system level, featured settable gain and bandwidth, differential inputs, and good zero point stability. Some were chopper stabilized while others utilized transistorized differential connections. Sold by a number of concerns, they were quite popular for transducer signal conditioning. These devices were the forerunners of modern IC instrumentation amplifiers. Their ability to supply low errors at zero and stable gain made accurate off-null bridge measurement possible.

The development of analog-digital converters during the 1960s² provided the last ingredient necessary for practical digitized output off-null bridge measurement. It had required over 100 years of technological progress to replace the null detectors and bridge balances. This is something to think about when soldering in IC instrumentation amps and A/D converters. What Lord Kelvin would have given for a single mini-DIP!

Note 1: The Hewlett-Packard Company and light bulbs have had a long and successful association.

Note 2: The first fully electronic analog-digital converter was developed by D.H. Wilkinson in 1949 (see References). The first analog-digital converters available as standard product were probably those produced by Pastoriza Electronics in the late 1960s.

APPENDIX C

THE WIEN BRIDGE AND MR. HEWLETT

The Wien bridge is easily the most popular basis for constructing sinewave oscillators. Circuits constructed around the Wien network offer wide dynamic range, ease of tuning, amplitude stability, low distortion and simplicity. Wien described his network (Figure C1) in 1891. Unfortunately, he had no source of electronic gain available, and couldn't have made it oscillate even if he wanted to. Wien developed the network for AC bridge measurement, and went off and used it for that.

Forty-eight years later William R. Hewlett combined Wien's network with controlled electronic gain in his masters thesis. The results were the now familiar "Wien bridge oscillator" architecture and the Hewlett-Packard Company. Hewlett's circuit (Figure C2) utilized the relatively new tools of feedback theory (see References) to support stable oscillation. Two loops were required. A positive feedback loop

from the amplifier's output (6F6 plate) back to its positive input (6J7 first grid) via the Wien bridge provided oscillation. Oscillation amplitude was stabilized by a second, negative, feedback loop. This loop was closed from the output (again, the 6F6 plate) back to the amplifier's negative input (the 6J7 cathode). The now famous lamp supplied a slight positive temperature coefficient to maintain gain at the proper value. For reference in interpreting the vacuum tube¹ configuration, a modern version (text Figure 39) of Hewlett's circuit appears as an insert.

Contemporary oscillators usually replace the lamps action with electronic equivalents to control loop settling time (see text).

Note 1: For those tender in years, "vacuum tubes" are thermionically activated FETs, descended from Lee DeForest.

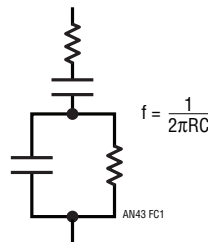


Figure C1. Wiens Network

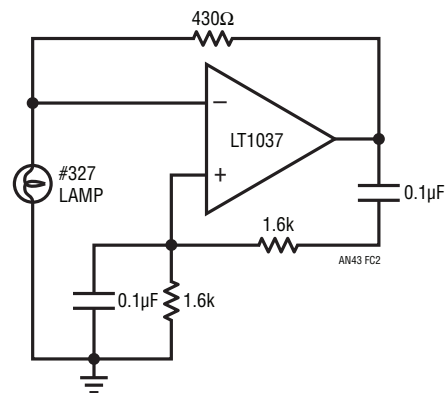
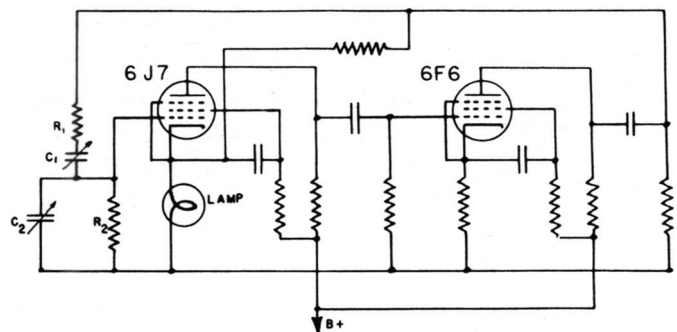


Figure C2. A Copy of Hewlett's Thesis "Figure 3" Showing His Original Circuit. Modern Version Shown for Reference (Hewlett's Figure Courtesy Stanford University Archives)

APPENDIX D

UNDERSTANDING DISTORTION MEASUREMENTS

Bruce E. Hofer
Audio Precision, Inc.

Introduction

Analog signal distortion is unavoidable in the real world. It can be defined as any effect or process that causes the signal to deviate from ideal. Because “distortion” means significantly different things to different people let us distinguish between two general categories based upon frequency domain effect.

A *linear* distortion changes the amplitude and phase relationship between the existing spectral components of a signal without adding new ones. Frequency and phase response errors are the most common examples. Both can cause significant alteration of the time domain waveform.

A *nonlinear* distortion adds frequency components to the signal that were never there, nor should be to begin with. Nonlinear distortion alters both the time and frequency domain representations of a signal. Noise can be considered a form of nonlinear distortion in some applications.

Nonlinear distortion is generally considered to be more serious than linear distortion because it is impossible to determine if a specific frequency component in the output signal was present in the input. This brief discussion will focus on the measurement and meaning of nonlinear distortion only. The word “distortion” shall hereinafter be used accordingly.

Measures of Distortion

One of the best and oldest methods of quantifying distortion is to excite a circuit or system with a relatively pure sine wave and analyze the output for the presence of signal components at frequencies other than the input sine wave. The sine wave is an ideal test signal for measuring nonlinear distortion because it is virtually immune to linear forms of distortions. With the exception of a perfectly tuned notch filter, the output of any linear distortion process will still be a sine wave!

“N-th” harmonic distortion is defined as the amplitude of any output signal at exactly N times the sine wave fundamental frequency. If the input sine wave is 400Hz any second harmonic distortion will show up at 800Hz, third harmonic at 1200Hz, etc. Spectrum analyzers, wave analyzers, and FFT analyzers are the typical instruments used to measure harmonic distortion. These instruments function by acting as highly selective voltmeters measuring the signal amplitude over a very narrow bandwidth centered at a specific frequency.

“THD” or Total Harmonic Distortion is defined as the RMS summation of the amplitudes of *all* possible harmonics, although it is often simplified to include only the second through the fifth (or somewhat higher) harmonics. The assumption that higher order harmonic content is insignificant in the computation of THD can be quite invalid. The sine wave distortion of many function generators is usually dominated by high order harmonic products with only relatively small amounts of products below the fifth harmonic. The crossover distortion characteristic of class AB and B amplifiers can often exhibit significantly high harmonic content above the fifth order.

A far better definition of THD is to include *all* harmonics up to some prescribed frequency limit. Usually the specific application will suggest a relevant upper harmonic frequency limit. In audio circuits a justifiable upper frequency limit might be 20kHz to 25kHz because few people can perceive signals above that range. In practice it has proven desirable to use a somewhat higher limit (typically 80kHz) because nonlinear distortion products above 20kHz can provoke intermodulation problems in subsequent audio stages. In the world of FM and TV broadcast measurements it is common practice to use a 30kHz bandwidth limit even though the signals are inherently limited to 15kHz.

“THD+N” or Total Harmonic Distortion plus Noise is defined as the RMS summation of *all signal components*, excluding the fundamental, over some prescribed bandwidth. Distortion analyzers perform this measurement by removing the fundamental sinewave with a notch filter and measuring the leftover signal. Unfortunately some popular analyzers have excessive measurement bandwidth (>1MHz) with no provision for limiting. For the vast majority of applications a measurement bandwidth of >500kHz serves little purpose other than to increase noise contribution and sensitivity to AM radio stations. Today’s better distortion analyzers offer a selection of measurement bandwidths typically including 20kHz to 22kHz, 30kHz, 80kHz, and wideband (300kHz to 500kHz).

At first glance it might appear that THD+N measurements are inferior to THD only measurements because of the sensitivity to wideband noise. Even with their noise contribution today’s distortion analyzers offer the lowest residual distortion, hence the most accuracy in making ultralow distortion measurements. The typical residual contribution of spectrum analyzers is usually limited by their internal mixer stages to about 0.003% (–90dB). FFT analyzers do not fare much better due to A/D converter nonlinearities. The very best 16-bit converters available today do not guarantee residual distortion below about 0.002% although future developments promise to improve this situation. Distortion analyzers offer the lowest residual performance with at least one manufacturer claiming 0.0001% (typical).

“IMD” or InterModulation Distortion is yet another technique for quantifying nonlinearity. It is a much more specialized form of testing requiring a multi-tone test signal. IMD tests can be more sensitive than THD or THD+N tests because the specific test frequencies, ratios, and analyzer measurement technique can be chosen to optimize response to only certain forms of nonlinearity. Unfortunately this is also one of the biggest disadvantages of IMD testing because there are so many tests that have been suggested: SMPTE, CCIF, TIM, DIM, MTM, to name a few.

Distortion Measurement Accuracy

Nonlinear distortion is not a traceable characteristic in the sense that an unbroken chain of comparisons can be made to a truly distortion-*less* standard. Such a standard does not exist! Real world distortion measurements will always include the non-zero contributions from both the sinewave source and the analyzer.

It is a truly challenging task to *accurately* measure distortion below about 0.01% (–80dB). Indeed, distortion measurement errors can become quite large near residual levels. Harmonic contributions from the original sinewave and the analyzer can add algebraically, vectorially, or even cancel depending upon their relative phase. There are no general assumptions that can be made regarding how two residual contributions will add or subtract.

In the following equation let “M” be the measured value of the N-th harmonic, let “X” be the magnitude of the distortion contributed by the analyzer, and let “D” be the true distortion magnitude of some signal. The measured distortion will be influenced by the residual analyzer contribution:

$$M \cdot \sin(2\pi Nft + \phi) = D \cdot \sin(2\pi Nft) + X \cdot \sin(2\pi Nft + \theta)$$

$$M = \begin{cases} (D + X) & \text{if } \theta = 0^\circ \\ (D^2 + X^2)^{1/2} & \text{if } \theta = \pm 90^\circ \\ (D - X) & \text{if } \theta = 180^\circ \end{cases} \quad (4)$$

Depending upon the relative phase between the distortion components (θ) a true distortion factor (D) of 0.0040% could be read as anything between 0.0025% to 0.0055% if the analyzer’s internal distortion contribution (X) was 0.0015%. Conversely a 0.0040% reading could have resulted from a true distortion factor of anything from 0.0025% to 0.0055% with the same 0.0015% analyzer contribution.

It is very important to understand this concept when making distortion readings near the specified residual levels of the test equipment. A lower reading may not always signify lower distortion. A low reading could be the result of a fortuitous cancellation of two larger contributions. It is also illogical to conclude that the true value of distortion is always less than the reading because the non-zero residual contributions of the analyzer and sinewave. The

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Application Note 43

service manual of one test equipment manufacturer incredibly states that a 0.0040% reading *verifies* their residual distortion guarantee of 0.0020% for both oscillator and analyzer!

All of the distortion measurement techniques give 0.5dB to 1.0dB (5% to 10%) reading accuracies at higher reading levels. Some distortion analyzers additionally provide average versus true RMS detection. Average detection is a carryover from the past and should be avoided because it will give erroneously low readings when multiple harmonics are present.

The Ultimate Meaning of THD and THD+N Measurements

Both THD and THD+N are measures of signal *impurity*. Distortion analyzers measure THD+N, not THD. Spectrum, wave, and FFT analyzers measure individual harmonic distortion from which THD can be calculated, but not THD+N. Is one better than the other?

For most applications THD+N is the more meaningful measurement because it quantifies total signal impurity. Particularly as we enter the age of A/D and D/A based

systems (for example, digital audio) the engineer is increasingly confronted with effects and imperfections that introduce non-harmonic components to a signal. Wideband noise itself can be viewed as an imperfection to be minimized. It is truly myopic to exclude other potentially serious and undesirable signal components in the determination of signal quality just because they do not happen to be a harmonic of the test signal. Why should a 60Hz component be acceptable in the calculation of 20Hz THD but be excluded when testing with a 1kHz fundamental?

On the other hand THD measurements are distinctly better than THD+N measurements if the application is to quantify a simple transfer function nonlinearity. Noise, hum, and other interference products are not introduced by these simple forms of nonlinearity and should not influence the measurement. Examples include the distortion due to component voltage coefficient effects and non-ohmic contact behavior.

Given that all real signals contain some distortion, how much THD or THD+N is acceptable? Only the designer can make that determination.

APPENDIX E

SOME PRACTICAL CONSIDERATIONS FOR BRIDGE INTERFACES

It is often desirable to route bridge outputs over considerable cable lengths. Cable driving should always be approached with caution. Even shielded cables are susceptible to noise pick-up, and input protection is often in order. Figure E1 shows some options. Simple RC filters often suffice for filtering. The upper limit on resistor value is set by amplifier bias current. FET input amplifiers allow large values, useful for minimizing capacitance size and input protection. Leakage eliminates electrolytic capacitors as candidates, and the largest practical non-electrolytic devices are about 1 μ F. Often, a single capacitor (dashed lines) is all that is required. Diode clamps prevent high

voltage spikes or faults (common in industrial environments) from damaging the amplifier. Figure E2 summarizes some clamp alternatives.

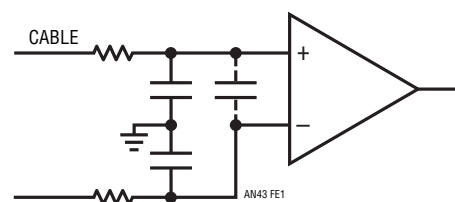


Figure E1. RC Filter Alternatives





CLAMP TYPE	FORWARD DROP	LEAKAGE AT 25°C (15V REVERSE)
 1N4148	≈0.6V	≈10 ⁻⁹ A
 HP5082-2810	≈400mV	≈10 ⁻⁷ A
 2N2222  2N4393	≈0.6V	≈10 ⁻¹¹ A

Figure E2. Various Devices Offer Different Clamp Characteristics

Figure E3 shows a high order switched-capacitor based filter. The LTC1062 has no DC error, and offers much better roll-off characteristics than the simple RC types. LTC Application Note 20, "Application Considerations for an Instrumentation Lowpass Filter," presents details.

Figure E4 shows a pre-amplifier used ahead of the remotely located instrumentation amplifier. The pre-amp raises cable signal level while lowering drive impedance. The asymmetrical bridge loading should be evaluated when using this circuit. Usually, the amplifiers input resistor can be made large enough to minimize its effect.

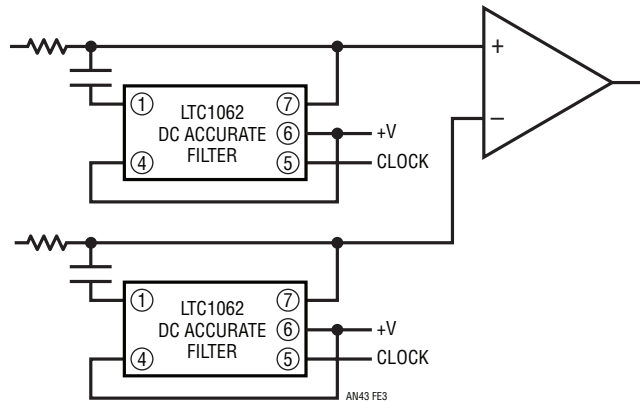


Figure E3. Switched-Capacitor Techniques Permit a DC Accurate 5th Order Lowpass Filter

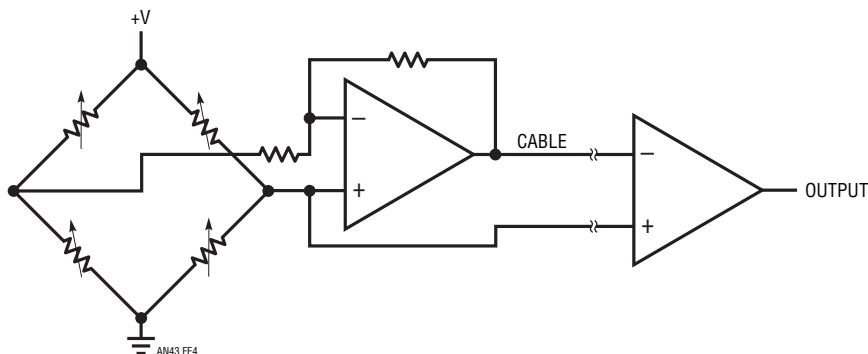
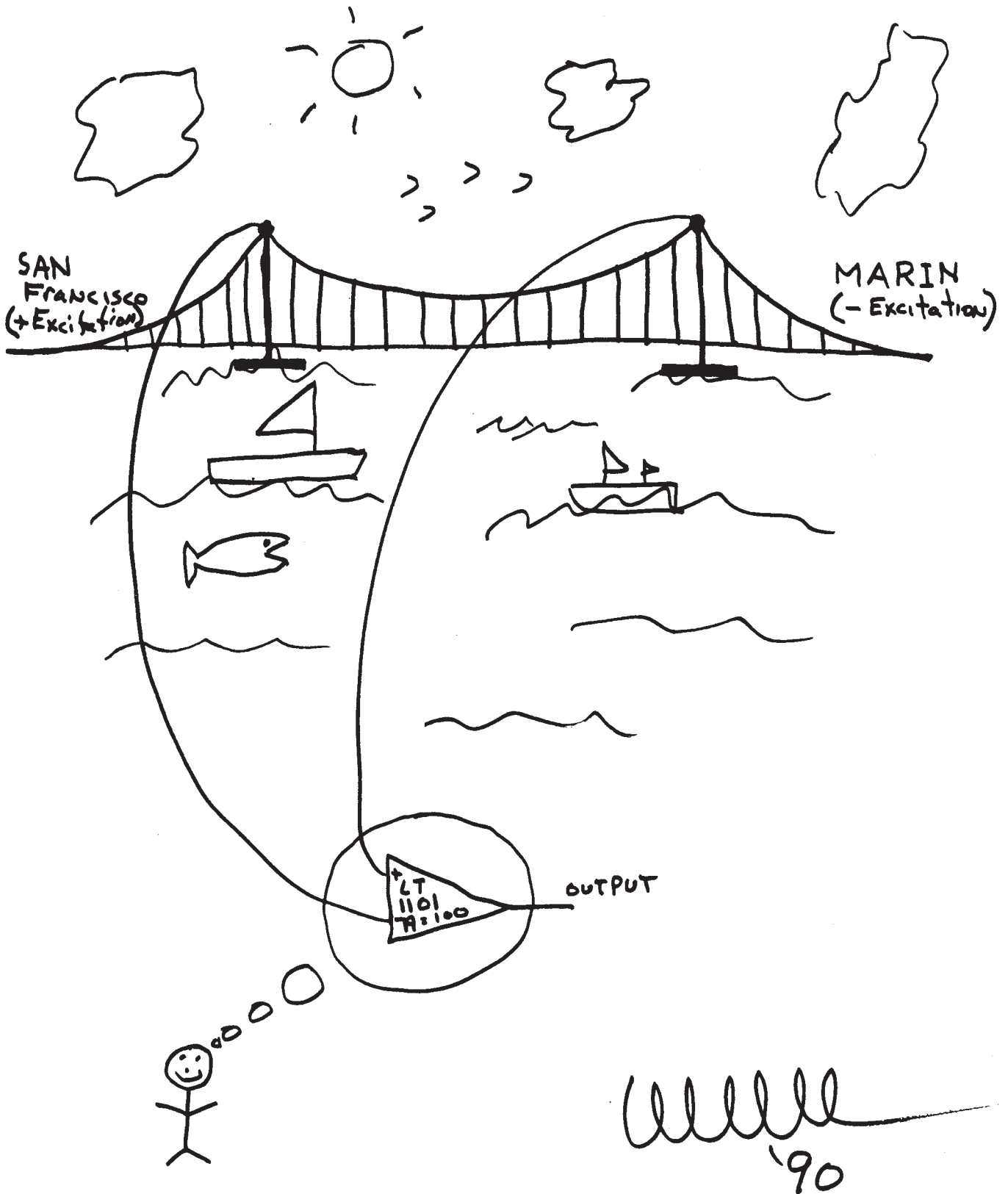


Figure E4. Pre-Amplifier Provides Gain and Low Impedance Drive to Cable

Application Note 43



Measurement and Control Circuit Collection

Diapers and Designs on the Night Shift

Jim Williams

Introduction

During my wife's pregnancy I wondered what it would *really* be like when the baby was finally born. Before that time, there just wasn't much mothering and fathering to do. As a consolation, we busied ourselves watching the baby's heartbeat (Figure 1) on a thrown-together fetal heart monitor (see References).

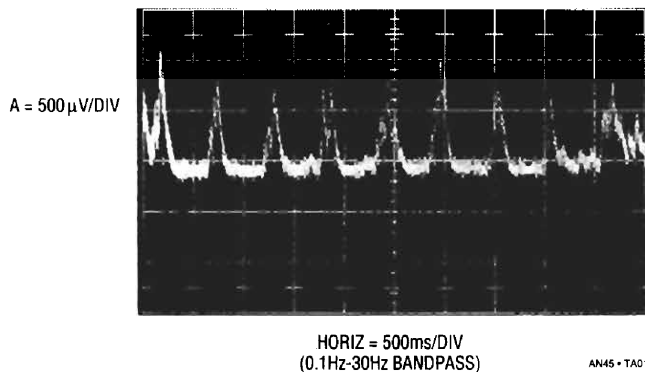


Figure 1. Michael's Fetal Heartbeat 4 1/2 Months into Pregnancy

When Michael was born things got noticeably busier in a hurry. My wife and I split up the evening duties. I got the night shift, 2 am to 7 am. After a few weeks, Michael and I got the hang of it and things began to go (relatively) smoothly. The two of us had mastered feedings, naps, crying jags, bottles, diapers and such and we began looking around for something to do. I decided to introduce Michael to the glories of late night circuit hacking. I first learned about wee hours circuit design at MIT in the 1970s. There was a subculture there that loaded up on pizza, soft drinks, and junk food, took it all into the lab, and closed the door until long after daylight. I was an enthusiastic convert.

Michael and I changed the rules just a bit. We loaded up on formula, diapers, and bottles and went into the lab.

The circuits in this collection represent our efforts, which stopped when he (more or less) began sleeping through the night. Most of the breadboarding occurred between

feedings, with design reviews and discussions during feedings. As such, the circuits are annotated with the number of feedings required for their completion; e.g. a "3-bottle circuit" took three feedings. The circuit's degree of difficulty, and Michael's degree of cooperation, combined to determine the bottle rating, which is duly recorded in each figure.

Low Noise and Drift Chopped Bipolar Amplifier

Figure 2's circuit combines the low noise of an LT1028 with a chopper based carrier modulation scheme to achieve an extraordinarily low noise, low drift DC amplifier. DC drift and noise performance exceed any currently available monolithic amplifier. Offset is inside $1\mu\text{V}$, with drift less than $0.05\mu\text{V}/^\circ\text{C}$. Noise in a 10Hz bandwidth is less than 40nV, far below monolithic chopper stabilized amplifiers.

Bias current, set by the bipolar LT1028 input, is about 25nA. These specifications suit demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The 74C04 inverters form a simple two-phase square wave clock running at about 350Hz. The oscillator provides complementary drive to S1 and S2, causing A1 to see a chopped version of the input voltage. A1 amplifies this AC signal. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because A1 is AC coupled, its DC offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift noted.

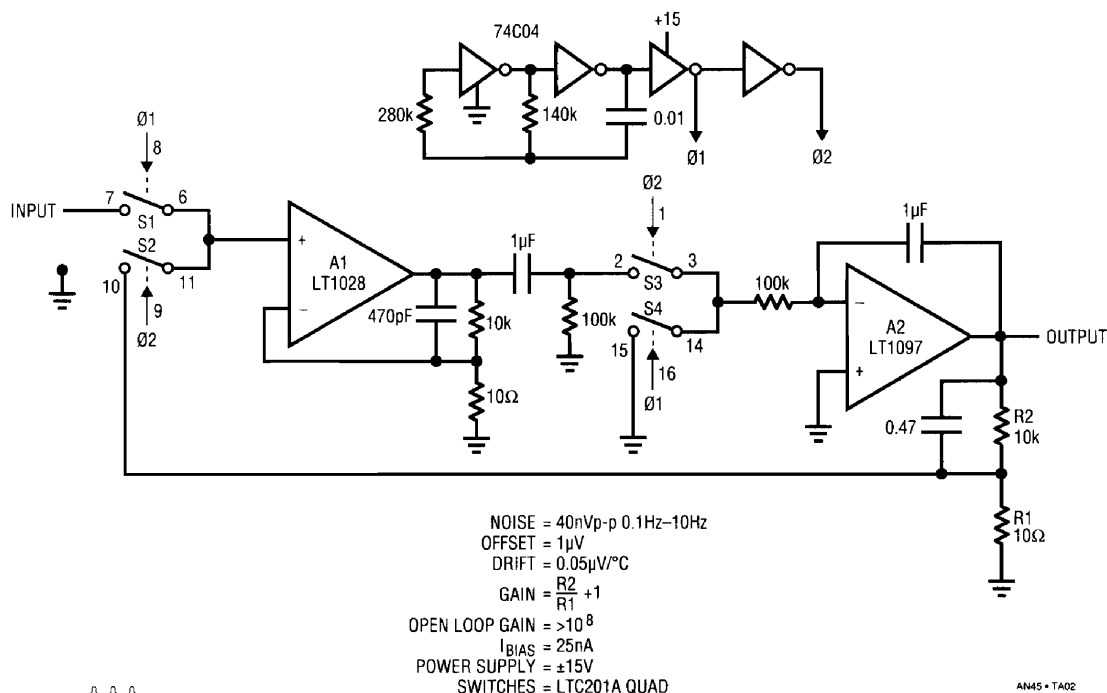


Figure 2. The Chopped Bipolar Amplifier. Noise is Inside 40nV with 0.05μV/°C Drift

Figure 3, a noise plot of the amplifier in a 0.1Hz-10Hz bandwidth, shows less than 40nV of peak-to-peak noise. A1 and the 60Ω resistance of S1-S2 contribute about equally to form this noise. When using this amplifier it is important to realize that A1's bias current flowing through the input source impedance causes additional noise. In general, to maintain low noise performance, source resistance should be kept below 500Ω. Fortunately, transducers such as strain gauge bridges, RTDs, and magnetic detectors are well below this figure.

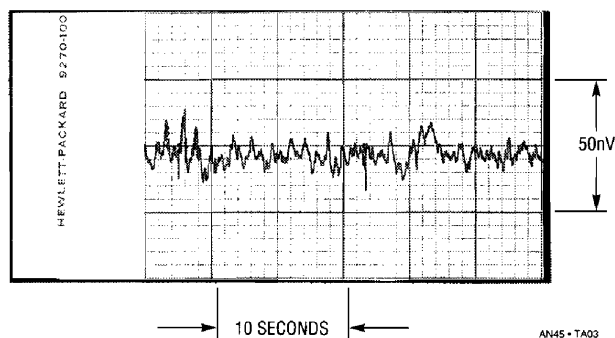


Figure 3. Noise in a 0.1Hz-10Hz Bandwidth is Less Than 40nV with 0.05μV/°C Drift

Low Noise and Drift Chopped FET Amplifier

Figure 4's circuit combines the low drift of a chopper stabilized amplifier with a pair of low noise FETs. The result is an amplifier with 0.05μV/°C drift, offset within 5μV, 50pA bias current, and 200nV noise in a 0.1Hz-10Hz bandwidth. The noise performance is especially noteworthy; it is almost eight times better than monolithic chopper stabilized amplifiers.

FET pair Q1 differentially feeds A2 to form a simple low noise op amp. Feedback, provided by R1 and R2, sets closed loop gain (in this case 1000) in the usual fashion. Although Q1 has extraordinarily low noise characteristics, its 15mV offset and 25μV/°C drift are poor. A1, a chopper stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1A's channel current to minimize the difference. Q1's skewed drain values ensure that A1 will be able to capture the offset. A1 supplies whatever current is required into Q1A's channel to force offset within 5μV. Additionally, A1's low bias current does not appreciably add to the overall 50pA amplifier bias current. As shown, the amplifier is set up for a non-inverting gain of 1000, although other gains and inverting operation are

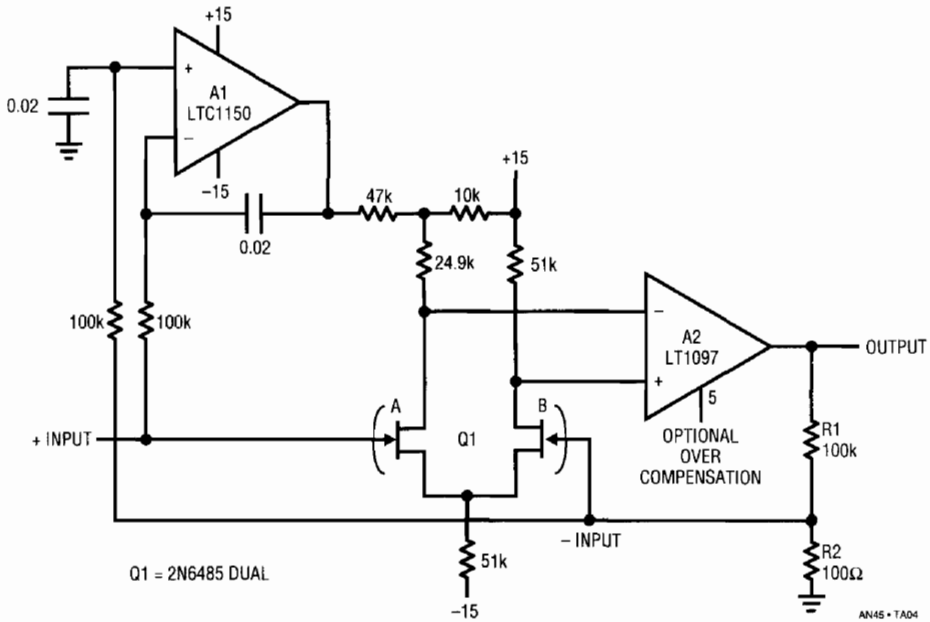


Figure 4. Chopper Stabilized FET Pair Combines Low Bias, Offset and Drift with 200nV Noise

possible. Figure 5 is a plot of noise measured in a 0.1Hz-10Hz bandwidth. The performance obtained is almost an order of magnitude better than any monolithic chopper stabilized amplifier, while retaining low offset and drift.

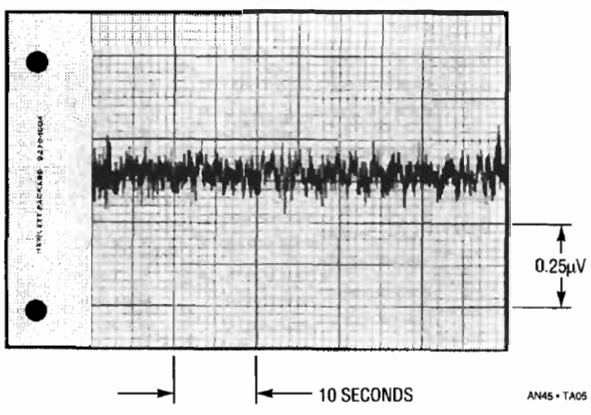


Figure 5. Noise Performance for Figure 4. A1's Low Offset and Drift are Retained, but Noise is Almost Ten Times Better

A2's optional overcompensation can be used (capacitor to ground) to optimize damping for low closed loop gains.

Stabilized, Wideband Cable Driving Amplifier with Low Input Capacitance

Figure 6's amplifier has over 20MHz of small signal bandwidth driving 100mA loads, capacitance or cable.

Input capacitance is below 1.5pF and bias current about 100pA. The output is fully protected. These features make this amplifier ideal as an ATE pin amplifier, video A-D input buffer, or cable driver. The amplifier also permits wideband probing when oscilloscope probe loading is not tolerable. The overall amplifier is composed of a low input capacitance FET, two LT1010 buffers, and a discrete gain stage. A3 acts as a DC restoration loop. The 33Ω resistors sense A1's operating current, biasing Q3 and Q4. These devices furnish complementary voltage gain to A2, which provides the circuit's output. Feedback is from A2's output to A1's output, which is a low impedance point. This "current mode" feedback permits fixed bandwidth over a wide range of closed loop gains. This contrasts with normal feedback schemes where bandwidth degrades as closed loop gain increases.

A3's stabilizing loop compensates large offsets in the signal path, which are dominated by mismatch in Q3 and Q4. A3 measures the DC difference between the amplifier's input and output and biases the signal path to correct for offset. Correction is implemented by controlling Q1's channel current via Q2. The channel current sets Q1's V_{GS}, allowing A3 to control overall circuit offset. The 9k-1k feedback divider feeding A3 is selected to equal the gain ratio of the circuit, in this case 10.

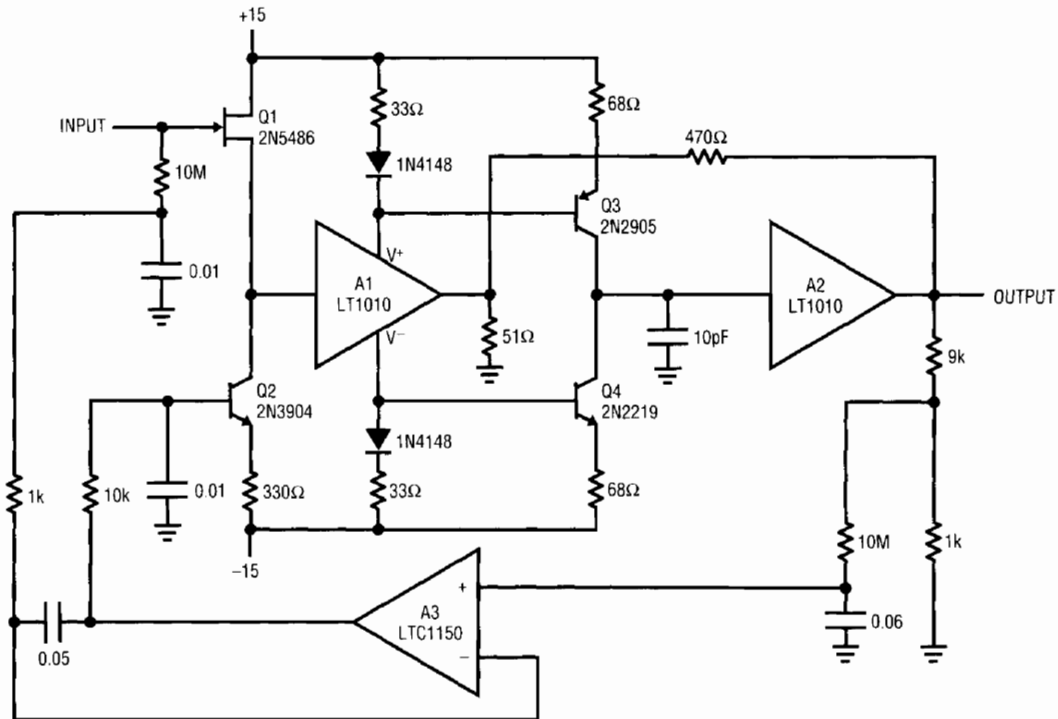


Figure 6. Stabilized, Wideband Cable Driving Amplifier with Low Input Capacitance

The feedback scheme makes A1's output look like the negative input of the amplifier, with closed loop gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that the bandwidth becomes relatively independent of closed loop gain over a reasonable range. For this circuit, small signal bandwidth exceeds 20MHz over gains of 1 to 20. The loop is quite stable, and the 10pF value at A2's input provides good damping over a wide range of gains.

Figure 7 shows large signal performance at a gain of 10 driving 10 feet of cable. A fast input pulse (trace A) produces the output shown (trace B). Response is quick and clean with no slew residue or poor dynamics.

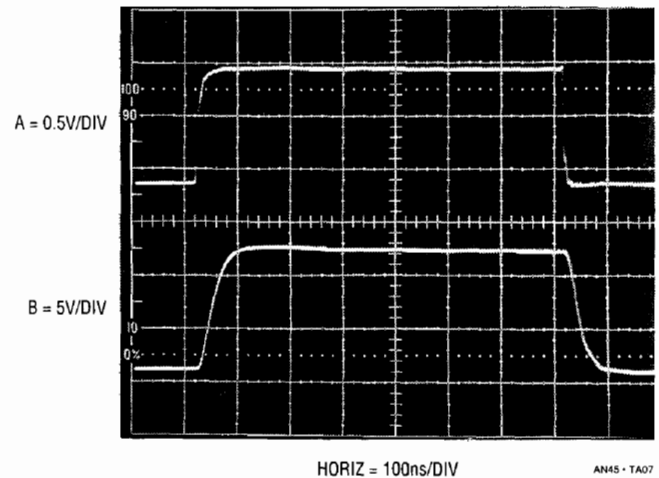


Figure 7. Wideband Amplifier's Response Driving A 10 Foot Cable

Voltage Programmable, Ground Referred Current Source

Precise, voltage programmable, ground referred current sources are usually complex and require trimming. Figure 8's simple, powerful configuration produces output current in strict accordance with the sign and magnitude of the control voltage. Dynamic response is well controlled,

and no trimming is required. The circuit's accuracy and stability are almost entirely dependent upon resistor R.

A1, biased by V_{IN} , drives current through R (in this case 10Ω) and the load. Instrumentation amplifier A2, operating at a gain of 100, senses across R. A2's output closes a loop back to A1. Because A1's loop forces a fixed voltage

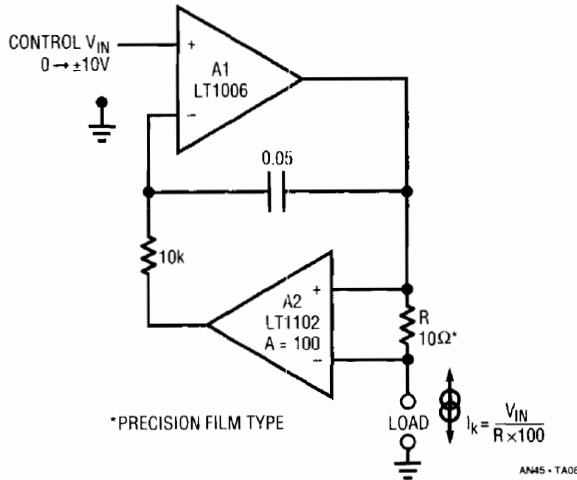


Figure 8. Voltage Programmable Current Source is Simple and Precise

across R, the current through the load is constant. The 10k-0.05µF combination sets A1's rolloff, and the circuit is stable.

Assuming an errorless component for R, the circuit's initial error is dominated by A2's 0.05% gain specification and its 5ppm/°C temperature coefficient. High grade film or wirewound resistors will maintain this level of performance.

Figure 9 shows dynamic response for a full scale input step. Trace A is the voltage control input while trace B shows the output current. Response is clean, with no slew residue or aberrations.

5V Powered, Fully Floating 4mA to 20mA Current Loop Transmitter

4mA to 20mA current loop transmitters are frequently required in industrial process control. Often, because of uncertain or dangerous common mode voltages, it is desirable that the generated 4mA to 20mA current be completely galvanically isolated from the transmitter's input. Figure 10's circuit does this while operating from a single 5V supply.

A2's positive input assumes a bias dependent upon the input and the 4mA trim setting. Under these conditions A2's output heads positive, turning on Q1 and Q2. Q2's collector drives T1's primary, which is chopped by Q3 and Q4. Complementary chopper drive comes from the 74C74 flip-flop outputs, with oscillator I1 setting a 25kHz clock

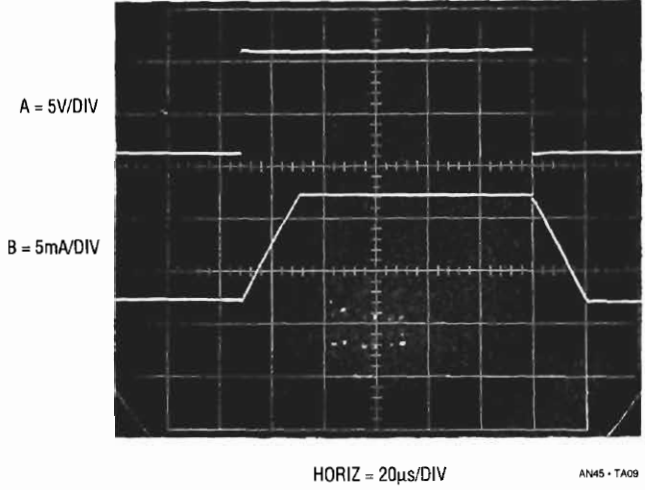


Figure 9. Current Source Dynamics are Clean, with No Slew Residue or Aberrations

rate. T1's output, producing voltage step-up, is rectified, filtered, and applied to the load. A3 senses load current across the 16Ω shunt and drives T2's center tap. Q9 and Q10, receiving complementary drive picked-off from T1's secondary, modulate T2's DC center tap voltage. T2's secondary receives this information, with flip-flop driven Q6-Q7 demodulating it back to DC at T2's center tap. T2's center tap voltage is fed A2, completing an isolated control loop. Changes in the circuit's input voltage cause this loop to adjust the load current accordingly. Conversely, load resistance changes have no effect, because the loop forces whatever voltage is necessary to maintain a constant 16Ω shunt voltage. Because T1 can supply up to 50V, load current remains fixed over load resistance swings from 0Ω to 2500Ω. Power supply shifts are similarly rejected by the loop, and the transformer modulation-demodulation scheme permits 0.05% accuracy and stability over temperature and a 250V common mode range. Greater common mode voltages are possible with increased transformer breakdown ratings.

Several subtleties aid circuit performance. I2-I3 and I4-I5 provide drive delays to Q6 and Q7. These delays approximate the delay through T1 to modulator pair Q9/Q10. This helps the four transistors switch simultaneously, aiding modulator-demodulator accuracy. Zener connected Q5 ensures that T1 produces enough voltage to power A3 and Q9/Q10, even when the load is 0Ω. Q8, similarly zener connected, clamps gate drive to Q9 and Q10, improving modulator linearity by preventing excessive gate drive variations over operating conditions. The diodes in A3's

Application Note 45

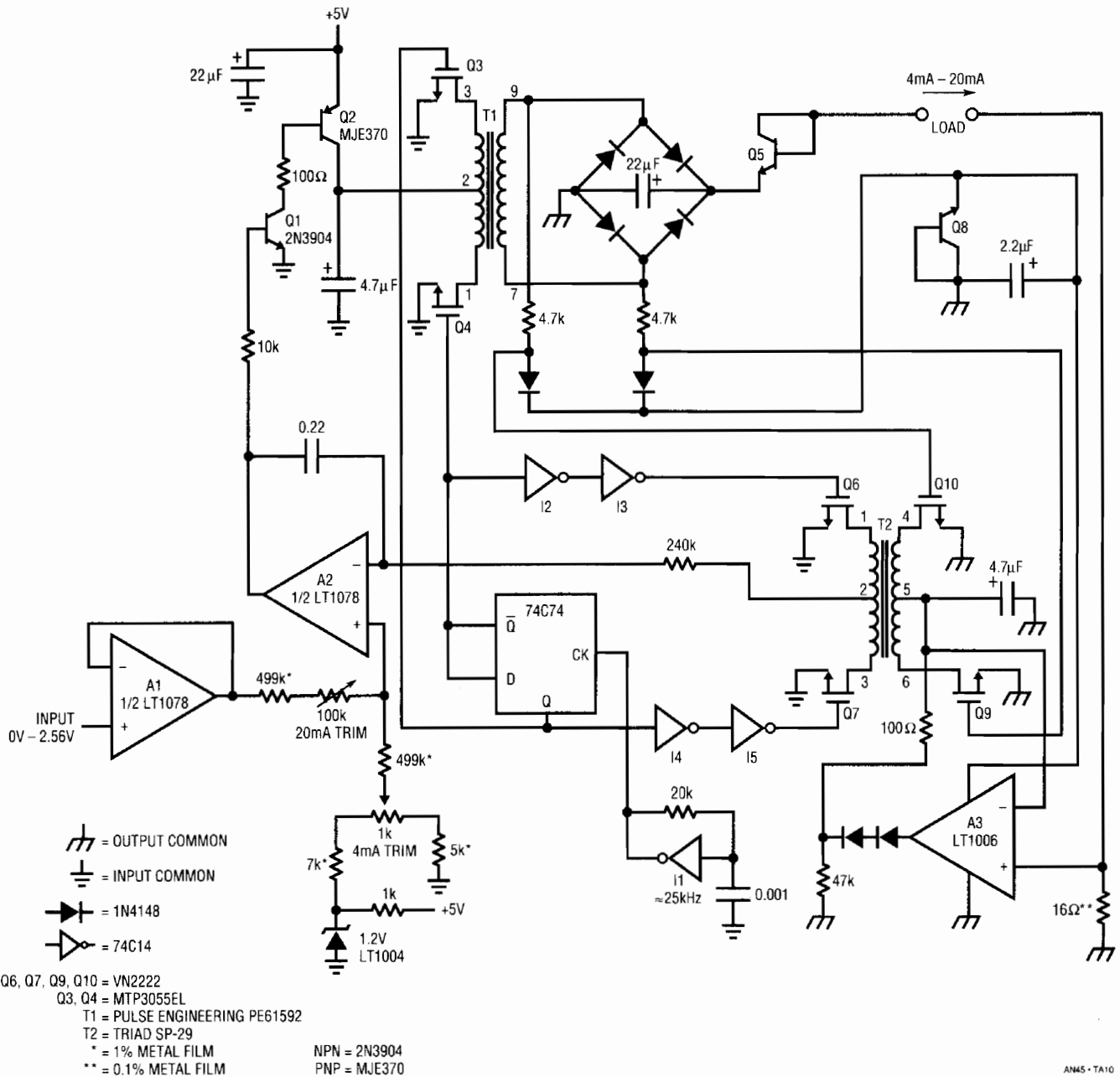


Figure 10. 5V Powered, Fully Floating 4mA-20mA Current Loop Transmitter

output ensure proper loop start-up. They prevent T2's center tap from receiving any bias until A3 has enough power supply voltage to function normally. To calibrate this circuit apply 0V input and adjust the 4mA trim for 4.00mA output (0.064V across the 16Ω shunt). Next,

apply 2.56V input and set the 20mA trimmer for 20.00mA output (0.3200V across the 16Ω shunt). Repeat this procedure until both points are fixed. Note that the 2.56V input range is directly compatible with D-A converter outputs, permitting digital control.

Application Note 45

(Q2) causes the theoretical 59.16mV (25°C) excursion (trace B) to appear across the V_{BE} junction. This signal is coupled to a switched demodulator via C1, which strips off Q2's DC bias. LTC1043 switch pin 2 (trace C) sees only the 59mV waveform, which is referenced to ground via demodulator action at pin 5 and pin 6. Pin 5, connected to capacitor C2, sits at pin 2's DC peak value. A1 amplifies this DC signal, with the LT1004 providing offset so 0°C equals 0V. The optional 10k resistor protects against ESD events, which may occur if Q2 is located at the end of a cable.

Using the components shown, the circuit achieves $\pm 1^\circ\text{C}$ accuracy over a sensed 0°C to 100°C range. Substituting randomly selected 2N3904s and 2N2222s for Q2 showed less than 0.4°C spread over 25 devices from various manufacturers.

Micropower, Cold Junction Compensated Thermocouple-to-Frequency Converter

Figure 13 is a complete, digital output, thermocouple signal conditioner. The circuit produces a 0kHz-1kHz output in response to a sensed 0°C to 100°C temperature

excursion. Cold junction compensation is included, and accuracy is within 1°C with stable 0.1°C resolution. Additionally, the circuit functions from a single supply, which may range from 4.75V to 10V. Maximum current consumption is 360µA.

The LT1025 provides an appropriately scaled cold junction compensation voltage to the type K thermocouple. As a result, the voltage at schematic point "A" varies from 0mV to 4.06mV over a sensed 0°C to 100°C range (type K slope is 40.6µV/°C). The remaining components form a voltage-to-frequency converter that directly converts this millivolt level signal without the usual DC gain stage. A1's negative input is biased by the thermocouple. A1's output drives a crude V-F converter, comprised of Q2, the 74C14 inverters, and associated components. Each V-F output pulse causes a fixed quantity of charge to be dispensed into C3 from C2 via the LTC201 based charge pump. C3 integrates the charge packets, producing a voltage at A1's positive input. A1's output forces the V-F converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action eliminates drift and nonlinearities in the V-F converter as an error term and the

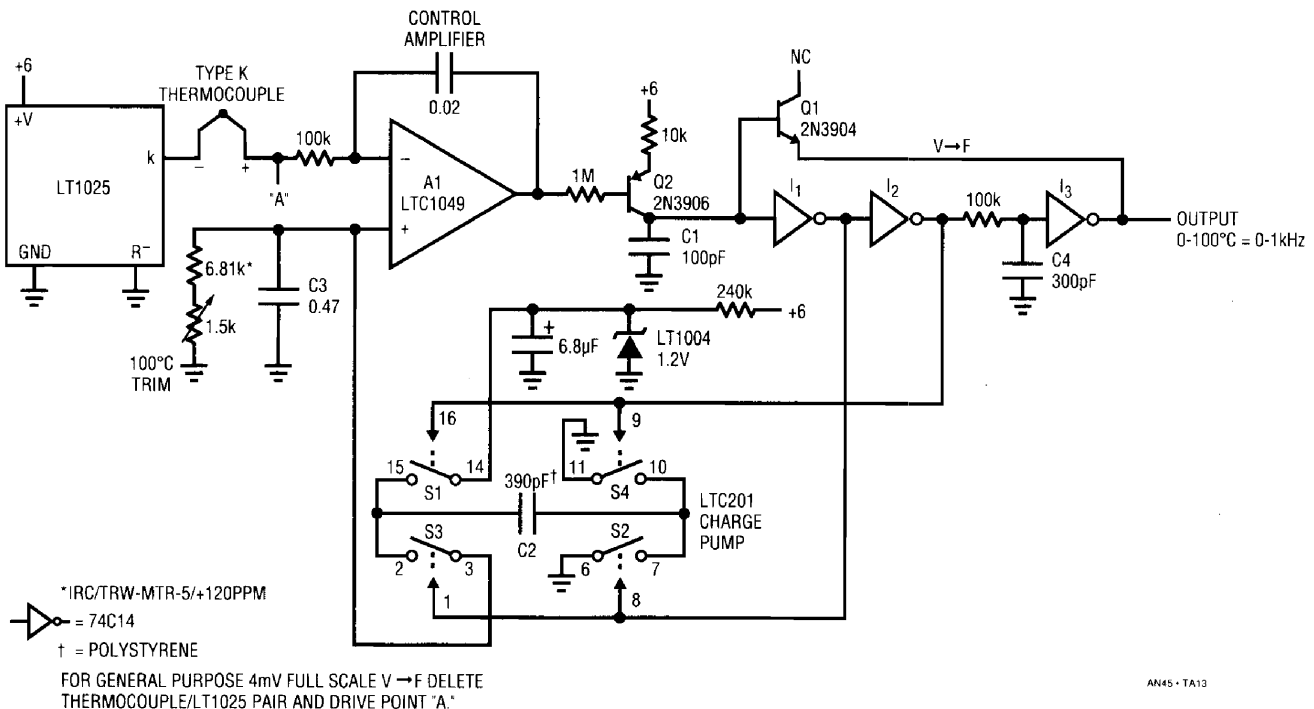


Figure 13. Thermocouple Sensed Temperature-to-Frequency Converter

output frequency is solely a function of the DC conditions at A1's inputs. The $0.02\mu\text{F}$ capacitor forms a dominant response pole at A1, stabilizing the loop. Chopper stabilized A1's low V_{OS} offset and drift eliminate offset error in the circuit, despite an output LSB value of only $4.06\mu\text{V}$ (0.1°C).

Figure 14 details circuit operation. A1's output biases current source Q2, producing a ramp (trace A, Figure 14) across C1. When the ramp crosses I1's threshold, the cascaded inverter chain switches, producing complementary outputs at I1 (trace B) and I2 (trace C). I3's RC delayed response (trace D) turns on diode connected Q1, discharging C1 and resetting the ramp. The ramp aberrations before the reset are due to transient I1 input currents during switching (near top of ramp). Q1's V_{BE} diode rounding and reverse charge transfer (bottom of ramp) account for the discontinuities during the ramp's low point.

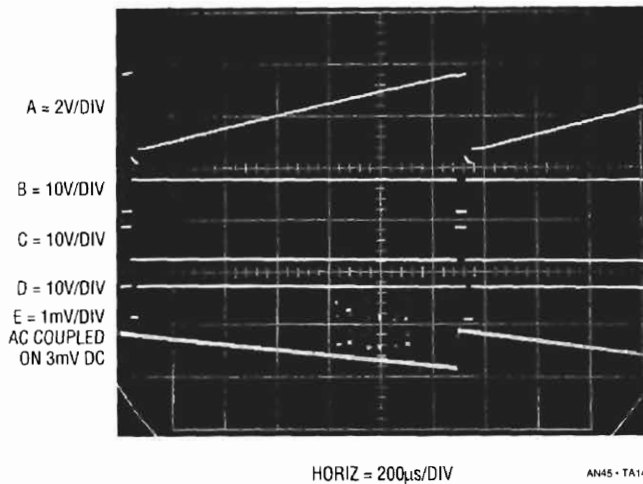


Figure 14. Waveforms for the Thermocouple-to-Frequency Converter

The complementary I1-I2 outputs clock the LTC201 switch based charge pump. C2 is alternately charged to the LT1004's reference voltage via S1 and S4 and discharged into C3 through S2 and S3. Each time this cycle occurs, C3's voltage is forced up (trace E). C3's average voltage is set by the $6.81\text{k}-1.5\text{k}$ trimmer resistance across it. A1 servo controls the repetition rate of the V-F to bring its inputs to the same value, closing a control loop. The $0.02\mu\text{F}$ capacitor smooths A1's response to DC.

To calibrate this circuit, disconnect the thermocouple and drive point "A" with 4.06mV . Next, set the 1.5k trimmer for

exactly 1000Hz output. Connect the thermocouple and the circuit is ready for use. Recalibration is not required if the thermocouple is replaced.

It is worth noting that this circuit can directly digitize any millivolt level signal by deleting the LT1025 thermocouple pair and directly driving point "A."

Relative Humidity Signal Conditioner

Relative humidity is a difficult physical parameter to transduce, and most transducers require fairly complex signal conditioning circuitry. Figure 15 combines simple circuitry with a capacitively based transducer to achieve good results. This circuit, which runs from a 9V battery, is accurate within 2% in the 5% to 90% relative humidity range.

The sensor specified has a nominal 500pF capacitance at $\text{RH} = 76\%$, with a slope of $1.7\text{pF}/\% \text{RH}$. The average voltage across the device must be zero. This prevents deleterious electrochemical migration in the sensor. LTC1043 section "A," driven by an internal oscillator, alternately charges the sensor from a resistively scaled portion of the LT1004 reference and discharges it into A1's summing point. Note that the switching is arranged so that sensor related current flows out of A1's summing point. The $0.1\mu\text{F}$ series capacitor ensures the sensor sees the required zero average voltage, with the $22\text{M}\Omega$ resistor preventing charge accumulation, which would stop current flow. The average current out of A1's summing point is balanced by packets of charge delivered by the LTC1043 switched capacitor section "C" in A1's feedback loop. The $0.1\mu\text{F}$ feedback capacitor gives A1 an integrator-like response, and its output is DC. As such, changes in sensor capacitance are seen as DC shifts in A1's output. A1 responds by raising its output positive to whatever DC potential is required to maintain its summing point at zero.

To allow 0% RH to equal 0V, offsetting is required. The signal and feedback terms biasing A1's summing point are expressed in charge form. Because of this, the offset must also be delivered to the summing point as charge, instead of a simple DC current. If this is not done, the circuit will be affected by drift in the LTC1043's internal oscillator. LTC1043 section "B" serves this function, delivering LT1004 referenced offsetting charge to A1.

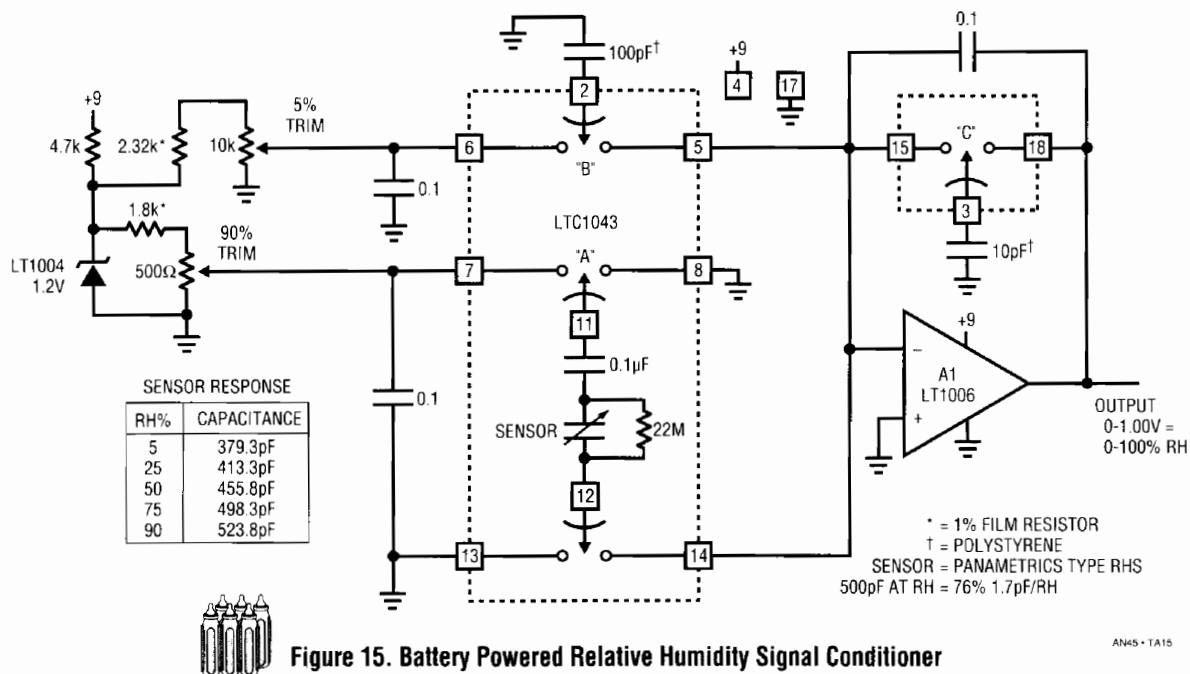


Figure 15. Battery Powered Relative Humidity Signal Conditioner

AN45-TA15

Drift terms in this circuit include the LT1004 and the ratio stability of the sensor and the polystyrene capacitors. These terms are well within the sensor's 2% accuracy specification, and temperature compensation is not required. To calibrate this circuit, place the sensor in a 5% RH environment and set the "5% RH trim" for 50mV output. Next, place the sensor in a 90% RH environment and set the "90% trim" for 900mV output. Repeat this procedure until both points are fixed. If known RH environments are unavailable, the capacitance versus RH table in Figure 15 may be utilized, although it applies for an ideal sensor. The capacitor values may be built-up or directly dialed out on a precision variable air capacitor (General Radio #722D).

Inexpensive Precision Electronic Barometer

Until recently, precision electronically based pressure measurements required expensive transducers. Capacitive and bonded strain gauge based approaches provide unmatched results, but costs are often prohibitive. Additionally, if low power operation is desired, signal conditioning for these devices can become complex.

Semiconductor based pressure transducers becoming available offer significant improvement over earlier devices. Figure 16's circuit utilizes such a device to form a low cost barometer. The LT1027 reference and A1 form a

current source to put precisely 1.5mA through transducer T1, in accordance with the manufacturer's specifications. Instrumentation amplifier A3 takes a differential gain of 10 from T1's bridge output. A2 provides additional gain to yield a calibrated output directly in inches of mercury.

T1's manufacturer specifies a nominal 115mV at full scale, although each device is supplied with precise calibration data. This information considerably simplifies calibration. To calibrate the circuit, simply adjust the potentiometer at A1 until the output corresponds to the scale factor supplied with the unit.

This circuit, compared to a long column mercury barometer, tracked ambient pressure variations from 29.75" to 30.32" over three months with only two counts of uncertainty. Additionally, over 50 turn-on/turn-off cycles had no measurable effect. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions.

1.5V Powered Radiation Detector

Figure 17's circuit provides an audible "tick" signal each time radiation or a cosmic ray passes through the detector. The LT1073 switching regulator pulses T1. T1 takes gain via its turns ratio and drives a voltage tripler, providing 500V bias to the detector. R1 and R2 provide scaled

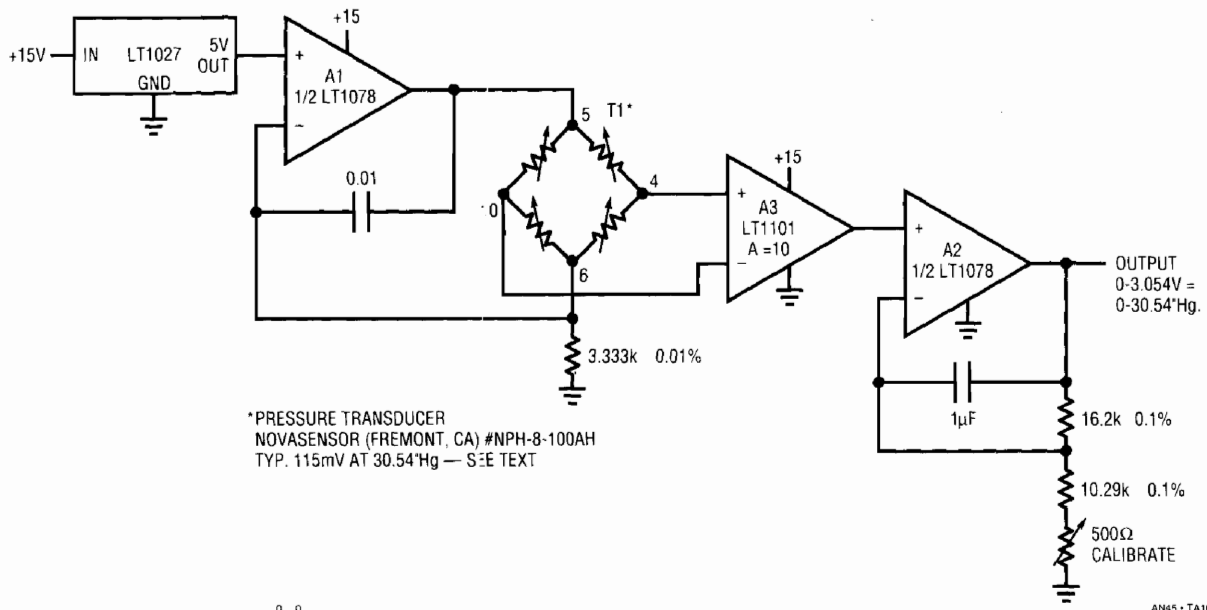


Figure 16. A Simple, Inexpensive Precision Barometer

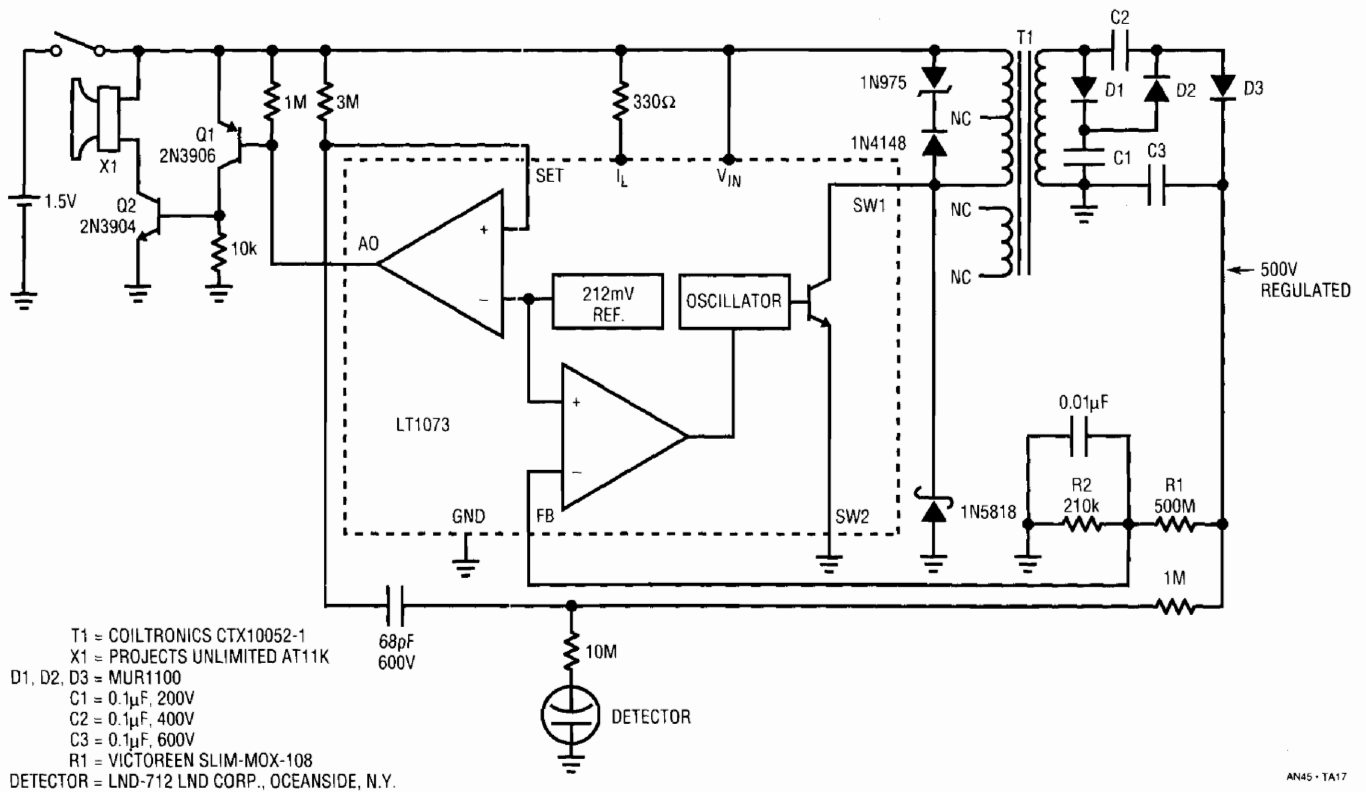


Figure 17. 1.5V Powered Radiation Detector

Application Note 45

feedback to the LT1073, closing a control loop. The $0.01\mu\text{F}$ lag adds AC hysteresis and the Schottky diode clamps negative going T1 excursions. When radiation or a cosmic ray strikes the detector, impedance drops briefly, transferring a quick negative going spike through the 68pF capacitor. This spike triggers the LT1073's auxiliary gain block, configured here as a comparator. Q1 and Q2 provide additional gain to drive the audible beeper. About 10 to 15 cosmic rays per minute are recorded in a normal environment.

9ppm Distortion, Quartz Stabilized Oscillator

A spectrally pure sine wave oscillator is required for data converter, filter and audio testing. Figure 18 provides a

stable frequency output with extremely low distortion. This quartz stabilized 4kHz oscillator has less than 9ppm (0.0009%) distortion in its 10Vp-p output.

To understand circuit operation, temporarily assume A2's output is grounded. With the crystal removed, A1 and the A3 power buffer form a non-inverting amplifier with a grounded input. The gain is set by the ratio of the 47k resistor to the 50k potentiometer — opto-isolator pair. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency, and oscillations occur. A4 compares A3's positive peaks with the LT1004 2.5V negative reference. The diode in series with the LT1004 provides temperature compensation for A3's rectifier diode. A4 biases the LED portion of the opto-isolator,

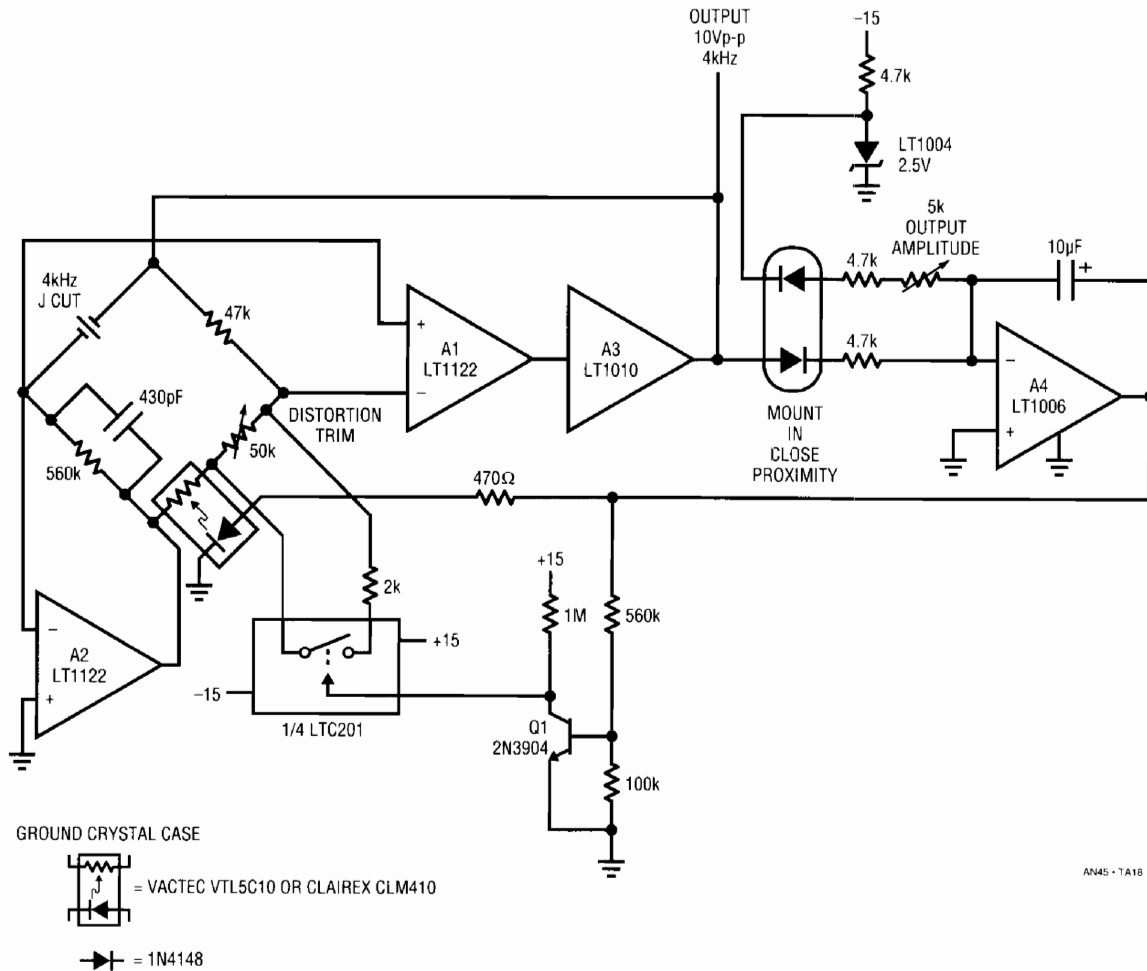


Figure 18. Quartz Stabilized 4kHz Oscillator with 9ppm Distortion

controlling the photoresistor's resistance. This sets loop gain to a value permitting stable amplitude oscillations. The 10 μ F capacitor stabilizes this amplitude control loop.

A2's function is to eliminate the common mode swing seen by A1. This dramatically reduces distortion due to A1's common mode rejection limitations. A2 does this by servo controlling the 560k Ω -photocell junction to maintain its negative input at 0V. This action eliminates common mode swing at A1, leaving only the desired differential signal.

Q1 and the LTC201 switch form a start-up loop. When power is first applied oscillations may build very slowly. Under these conditions A4's output saturates positive, turning on Q1. The LTC201 switch turns on, shunting the 2k Ω resistor across the 50k Ω potentiometer. This raises A1's loop gain, forcing a rapid build-up of oscillations. When oscillations rise high enough A4 comes out of saturation, Q1 and the switch go off and the loop functions normally.

The circuit is adjusted for minimum distortion by adjusting the 50k Ω potentiometer while monitoring A3's output with a distortion analyzer. This trim sets the voltage across the photocell to the optimum value for lowest distortion. The circuit's power supply should be well regulated and bypassed to ensure the distortion figures quoted.

After trimming, A3's output (trace A, Figure 19) contains less than 9ppm (0.0009%) distortion. Residual distortion components (trace B) include noise and second harmonic residue. Oscillation frequency, set by crystal tolerance, is typically within 50ppm with less than 2.5ppm/ $^{\circ}$ C drift.

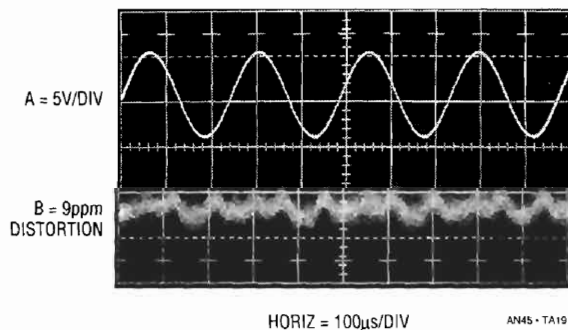


Figure 19. Oscillator Output and its 9ppm Distortion Residue

1.5V Powered Temperature Compensated Crystal Oscillator

Many single cell systems require a stable clock source. Crystal oscillators which run from 1.5V are relatively easy to construct. However, if good stability over temperature is required, things become more difficult. Ovenizing the crystal is one approach, but power consumption is excessive. An alternate method provides open loop, frequency correcting bias to the oscillator. The bias value is determined by absolute temperature. In this fashion, the oscillator's thermal drift, which is repeatable, is corrected. The simplest way to do this is by slightly varying the crystal's resonance point with a variable shunt or series impedance. Varactor diodes, the capacitance of which varies with reverse voltage, are commonly employed for this purpose. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shift, making direct 1.5V powered operation impossible.

Figure 20 improves the temperature stability of a 1.5V powered crystal oscillator by a factor of 20. It does this by slightly tuning the crystal's resonance as ambient temperature varies. Q1 and associated components form a 1MHz Colpitts oscillator which normally has a temperature coefficient of about 1ppm/ $^{\circ}$ C. The remainder of the circuit implements the temperature correction. The LM134 senses ambient temperature, converting it to a current which flows through the 30.1k resistor. This resistor's voltage is subtracted from a reference potential by A1. The stable subtraction voltage is derived from the LT1073's 212mV reference via Q2 and the 73.2k-27.4k resistors. Feedback from Q2's collector to the LT1073's auxiliary amplifier closes the reference loop, which also powers the Colpitts oscillator. The 47 μ F capacitor frequency compensates the loop.

A1's output controls the remaining portion of the LT1073, which is configured as a voltage step-up switching regulator. L1's high voltage inductive events are rectified and stored in the 47 μ F output capacitor, resulting in a stepped-up DC potential. This potential is fed back to A1, closing a control loop. Because A1 is biased by the temperature sensitive LM134, the loop's output varies with ambient temperature in a controlled manner. Q3's drop forces the step-up converter to always run, regardless of the loop's required output voltage. This permits smooth and continuous varactor bias from 0 to 3.9V over a 0-70 $^{\circ}$ C

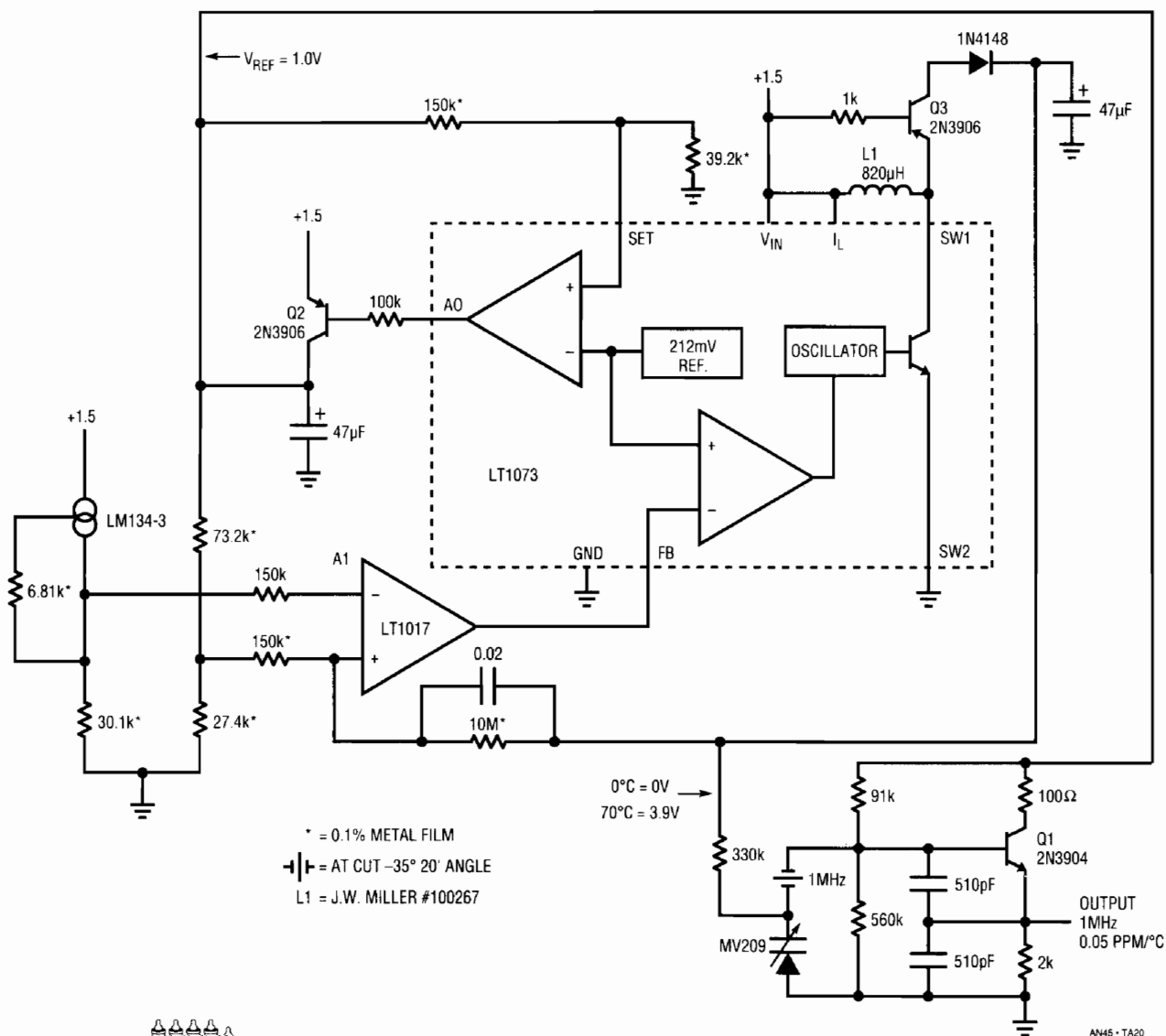


Figure 20. 1.5V Powered Temperature Compensated Crystal Oscillator

ambient operating environment. This output is applied to the varactor diode in the oscillator circuit. The varactor's capacitance, a function of its DC bias, thus varies with ambient temperature. This change in capacitance shifts the crystal's resonant frequency, opposing temperature induced crystal drift. For the values given in the circuit and the crystal cut specified, residual oscillator drift is only 0.05ppm/°C. This compares favorably with 1ppm/°C drift with no compensation used. The circuit functions from 1.7V down to 1.1V with no specification degradation. Current drain is only 230µA. Applications include portable high-accuracy clocks, survival radios, and secure communications.

90µA Precision Voltage-to-Frequency Converter

Figure 21 is a micropower voltage-to-frequency converter. A 0V-5V input produces a 0kHz-10kHz output with a linearity of 0.05%. Gain drift is 80ppm/°C. Maximum current consumption is only 90µA, almost 30 times lower than currently available V-F converters. To understand circuit operation, assume C1's positive input is slightly below its negative input (C2's output is low). The input voltage causes a positive going ramp at C1's positive input (trace A, Figure 22). C1's output is low, biasing the CMOS inverter output high. This allows current to flow from Q1's

Application Note 45

Q1's emitter voltage must be carefully controlled to get low drive. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE} . The two LT1034s are the actual voltage reference and the LM334 current source provides $35\mu\text{A}$ bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by utilizing the LM334's $0.3\%/^{\circ}\text{C}$ temperature coefficient to slightly temperature modulate the voltage drop in the Q2-Q4 trio. This correction's sign and magnitude directly oppose that of the $-120\text{ppm}/^{\circ}\text{C}$, 100pF polystyrene capacitor, aiding overall circuit stability.

The Q1 emitter-follower efficiently delivers charge to the 100pF capacitor. Both base and collector current end up in the capacitor. The CMOS inverter provides low loss SPDT reference switching without significant drive losses. The 100pF capacitor draws only small transient currents during its charge and discharge cycles. The 50pF - 47k positive feedback combination draws insignificantly small switching currents. Figure 23, a plot of supply current versus operating frequency, reflects the low power design. At zero frequency, the LT1017's quiescent current and the $35\mu\text{A}$ reference stack bias account for all current drain. There are no other paths for loss. As frequency scales-up, the charge/discharge cycle of the 100pF capacitor introduces the $1.5\mu\text{A}/\text{kHz}$ increase shown.

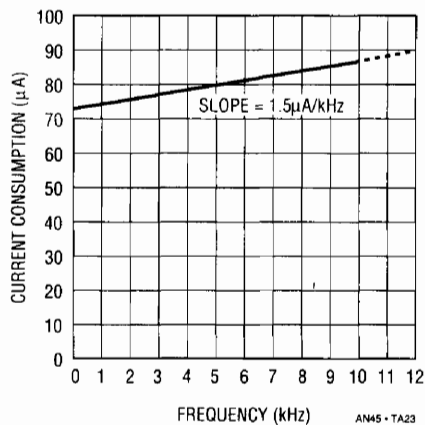


Figure 23. Current Consumption vs Frequency for the V to F Converter

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high. C2, detecting this via the inverter and the 2.7M - $0.1\mu\text{F}$ lag, also goes high. This lifts C1's negative input and

grounds the positive input with Q7, initiating normal circuit action.

Because the charge pump is directly coupled to C1's output, response is fast. The output settles within one cycle for a fast input step. To calibrate this circuit, apply 50mV and select the value at C1's input for a 100Hz output. Then, apply 5V and trim the input potentiometer for a 10kHz output.

Bipolar (AC) Input V-F Converter

No currently available V-F converter will accept bipolar (AC) inputs. This feature is desirable in power line monitoring and other applications. Figure 24's V-F converter accepts $\pm 10\text{V}$ inputs, producing a 0kHz - 10kHz output. Linearity is 0.04% , and temperature coefficient measures about $50\text{ppm}/^{\circ}\text{C}$. To understand circuit operation, assume a bipolar square wave (trace A, Figure 25) is applied to the input. During the input's positive phase, A1's output (trace B) swings negative, driving current through C1 via the full wave diode bridge. A1's current causes C1 to ramp linearly. Instrumentation amplifier A2, operating at a gain of 10, looks differentially across C1. A2's output (trace C) biases comparator A3's negative input. When A2's output crosses zero, A3 fires (trace D). AC positive feedback to A3's positive input (trace E) "hangs up" A3's output for about $20\mu\text{s}$. The Q1 level shifter drives ground referred inverters I1 and I2 to deliver biphasic drive (traces G and H) to the LTC201 switch. The LTC201, set-up as a charge pump, places C2 across C1 each time the inverters switch, resetting C1 to a lower voltage. The LT1004 reference, along with C2's value, determines how much charge is removed from C1 each time the charge pump cycles. Thus, each time A2's output tries to cross zero, C2 is switched across C1, resetting it to a small negative voltage and forcing A1 to begin recharging it. The frequency of this oscillatory behavior is directly proportional to the input derived current into A1. During the time C1 is ramping toward zero the LTC201 switches C2 across the LT1004, preparing it for the next discharge cycle. The action is the same for negative input excursions (see Figure 25), except that A1's output phasing is reversed. A2, looking differentially across A1's diode bridge, sees the same signal as for positive inputs and circuit action is identical. A4, detecting A1's output polarity, provides a sign bit output (trace F).

Application Note 45

output saturates positive, causing A3 to go negative. A3's prolonged negative state, detected by the R1-C3 filter, pulls its negative input toward -15V. When A3's negative input crosses zero, its output changes state and charges R1-C3 positively. A3's input rises above zero, causing output reversal and free-running oscillation commences. As in normal mode, the 100pF-33k RC aids transitions. A3's oscillations are transmitted to the LTC201 based charge pump via A1 and the inverters. C2 pumps charge out of C1, driving the voltage across it toward zero. A2 comes out of positive saturation and heads negative,

eliminating positive bias at A3's input. A3's free-running oscillation stops, and normal loop action begins.

To calibrate this circuit apply either a -10V or a +10V input and set the 10kΩ trimmer for exactly 10kHz output. The low offsets of A1 and A2 permit operation down to a few hertz with no zero trim required.

1.5V Powered, 350ps Rise Time Pulse Generator

Verifying the rise time limit of wideband test equipment set-ups is a difficult task. In particular, the "end-to-end" rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure 27's circuit does this, providing a 1ns pulse with rise and fall times inside 350ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage doubler network. L1 periodically receives charge, and its

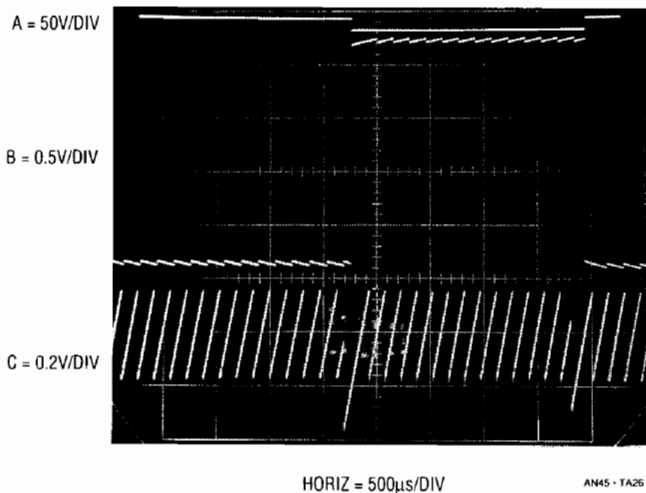
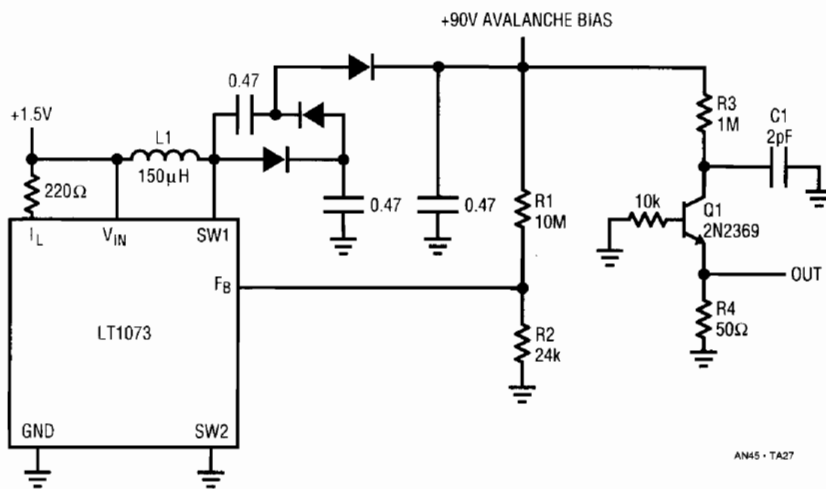


Figure 26. Detail of Integrator and Differential Amplifier Outputs



L1 = TOKO #262-LYF-0095K
 = MUR120
 SELECT Q1 AND 2pF VALUE — SEE TEXT



Figure 27. 350ps Rise Time Pulse Generator

flyback discharge delivers high voltage events to the doubler network. A portion of the doubler network's DC output is fed back to the LT1073 via the R1, R2 divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the R3-C1 combination. Q1, a 40V breakdown device, non-destructively avalanches when C1 charges high enough.³ The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free-running oscillation at about 200kHz. Figure 28 shows the output pulse. A 1GHz sampling oscilloscope (Tektronix 556 with 1S1 sampling plug-in) measures the pulse at 10V high with about a 1ns base. Rise time is 350ps, with fall time also indicating 350ps. The figures may actually be faster, as the 1S1 is specified with a 350ps rise time limit.⁴

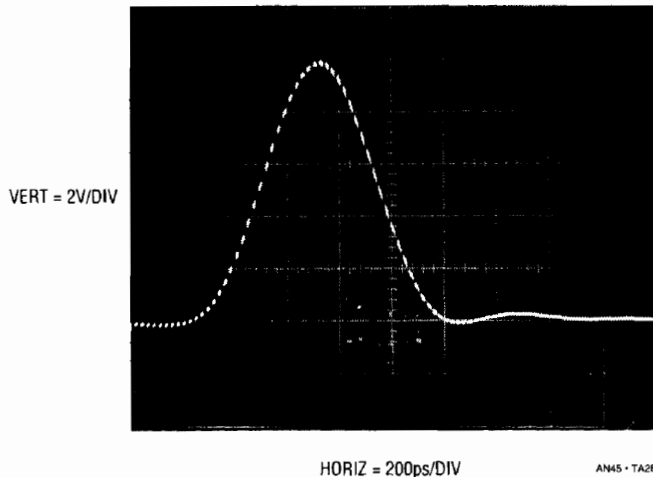


Figure 28. Avalanche Pulse Generator Output Pulse. Waveform Has 350ps Rise and Fall Times. Slightly Under Damped Turn-Off is Probably Due to Test Fixture Limitations

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All "good" devices switched in less than 600ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout techniques are essential for good results from this circuit. Current drain from the 1.5V battery version is about 5mA.

Note 3: See Reference 7.

Note 4: I'm sorry, but 1GHz is the fastest scope in my house.

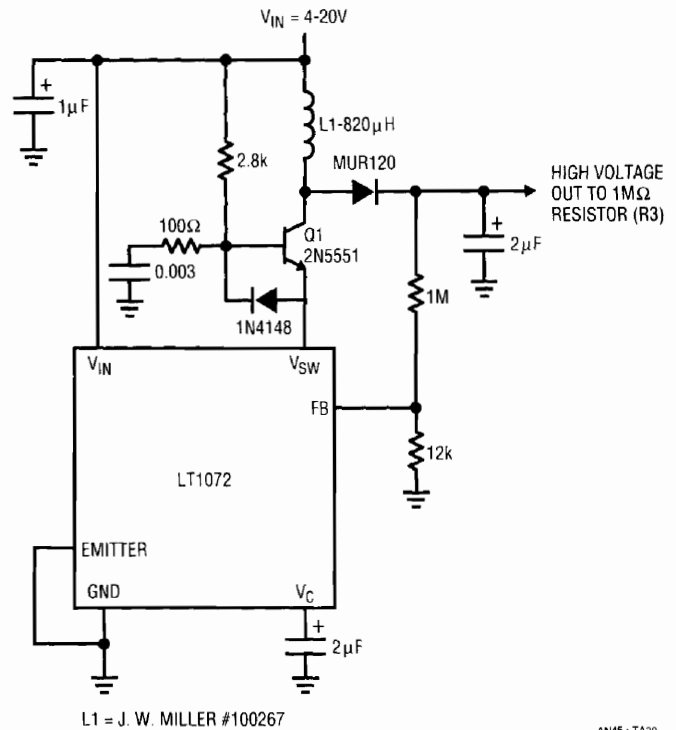


Figure 29. Alternate 90V DC-DC Converter

For those applications which must run from higher voltage inputs, Figure 29 is included. This circuit, which operates from inputs of 4V to 20V, will also power the avalanche stage. Cascoded high voltage transistor Q1 combines with the LT1072 switching regulator to form a high voltage switched mode control loop. The LT1072 pulse width modulates Q1 at its 40kHz clock rate. L1's inductive events are rectified and stored in the 2µF output capacitor. The 1MΩ-12kΩ divider provides feedback to the LT1072. The diode and RC at Q1's base damp inductor related parasitic behavior. The circuit's output drives the avalanche stage in similar fashion to the LT1073 based circuit.

A Simple Ultra-Low Dropout Regulator

Switching regulator post regulators, battery powered apparatus, and other applications frequently require low dropout linear regulators. Often, battery life is significantly affected by the regulator's dropout performance. Figure 30's simple circuit offers lower dropout voltage than any monolithic regulator. Dropout is below 50mV at 1A, increasing to only 450mA at 5A. Line and load regulation are within 5mV, and initial output accuracy is inside 1%.

Application Note 45

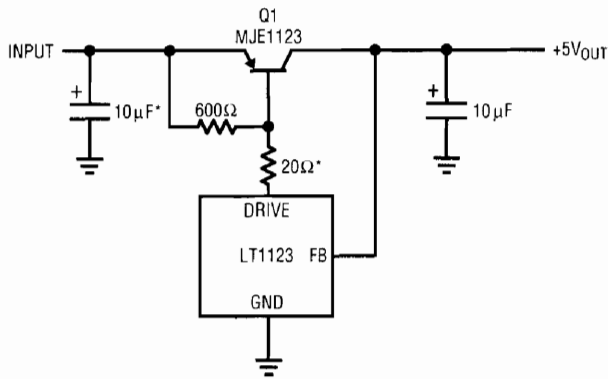
Additionally, the regulator is fully short circuit protected, and has a no load quiescent current of $600\mu\text{A}$.

Circuit operation is straightforward. The 3-pin LT1123 regulator (TO-92 package) servo controls Q1's base to maintain its feedback pin (FB) at 5V. The $10\mu\text{F}$ output capacitor provides frequency compensation. If the circuit is located more than six inches from the input source, the optional $10\mu\text{F}$ capacitor should bypass the input. The optional 20Ω resistor limits LT1123 power dissipation and is selected based upon the maximum expected input voltage (see Figure 31).

Normally, configurations of this type offer unpredictable short circuit protection. Here, the MJE1123 transistor

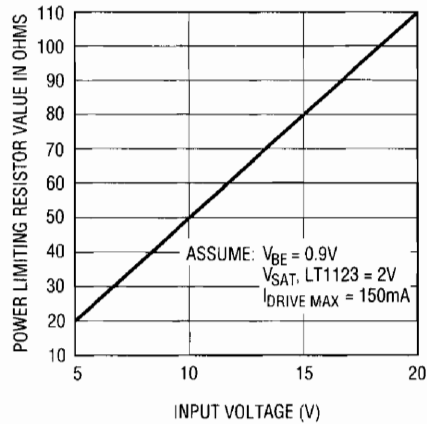
shown has been specially designed for use with the LT1123. Because of this, beta based current limiting is practical. Excessive output current causes the LT1123 to pull down harder on Q1 until beta limiting occurs. Under these conditions the controlled pull down current combines with Q1's beta and safe operating area characteristics to provide reliable short circuit limiting. Figure 32 details current limit characteristics for 30 randomly selected transistors.

Figure 33 shows dropout characteristics. Even at 5A, dropout is about 450mV, decreasing to only 50mV at 1A. Monolithic regulators cannot approach these figures, primarily because monolithic power transistors do not offer



* = OPTIONAL (SEE TEXT)
MJE1123 = MOTOROLA

AN45 - TA30

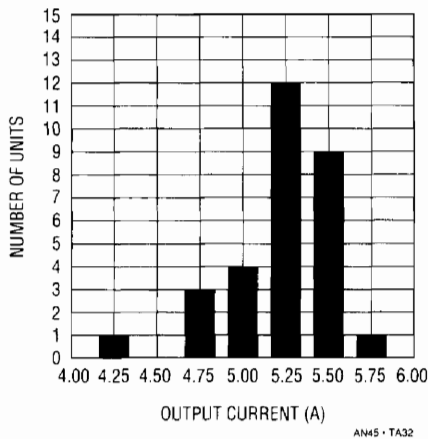


AN45 - TA31

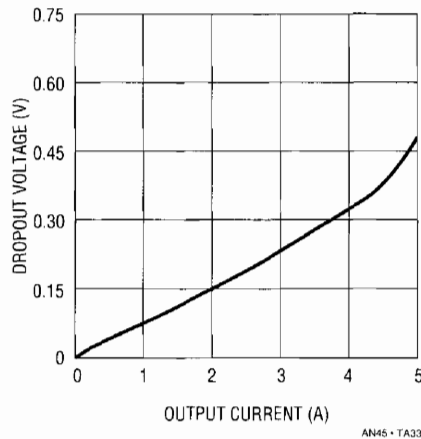


Figure 30. The Ultra-Low Dropout Regulator. LT1123 Combines with Specially Designed Transistor for Low Dropout and Short Circuit Protection

Figure 31. LT1123 Power Dissipation Limiting Resistor Value vs Input Voltage



AN45 - TA32



AN45 - TA33

Figure 32. Short Circuit Current for 30 Randomly Selected MJE1123 Transistors at $V_{IN} = 7\text{V}$

Figure 33. Dropout Voltage vs Output Current

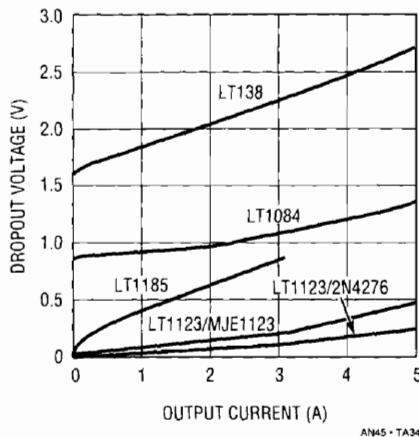


Figure 34. Dropout Voltage vs Output Current for Various Regulators

Q1's combination of high beta and excellent saturation. For comparison, Figure 34 compares the circuit's performance against some popular monolithic regulators. Drop-out is 10 times better than 138 types, and significantly better than the other types shown. Because of Q1's high beta, base drive loss is only 1%-2% of output current, even at full 5A output. This maintains high efficiency under the low $V_{IN} - V_{OUT}$ conditions the circuit will typically operate at. As an exercise, the MJE1123 was replaced with a 2N4276, a Germanium device. This combination provided even lower dropout performance, although current limit characteristics cannot be guaranteed.

Figure 35 shows a simple way to add shutdown to the regulator. A CMOS inverter or gate biases Q2 to control LT1123 bias. When Q2's base is driven, the loop functions normally. With Q2 unbiased, the circuit goes into shutdown and pulls no current.

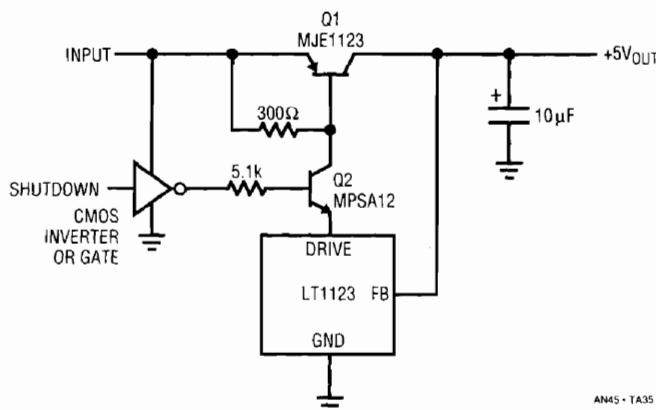
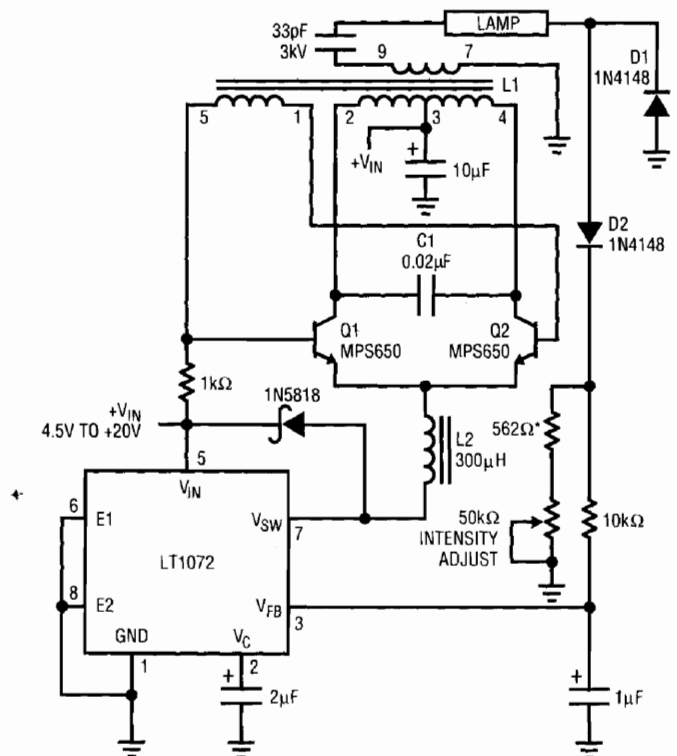


Figure 35. Shutdown for the Low Dropout Regulator

Cold Cathode Fluorescent Lamp Power Supply

Current generation portable computers utilize back-lit LCD displays. Cold Cathode Fluorescent Lamps (CCFL) provide the highest available efficiency for back-lighting the display. These lamps require high voltage AC to operate, mandating an efficient, high voltage DC-AC converter. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency.

Figure 36 meets these requirements. Efficiency is 78%, with an input voltage range of 4.5V-20V. 82% efficiency is possible if the LT1072 is driven from a low voltage (e.g., 3V-5V) source. Additionally, lamp intensity is continuously and smoothly variable from zero to full intensity.



- C1 = MUST BE A LOW LOSS CAPACITOR. METALIZED POLYCARB WIMA FKP2 (GERMAN) RECOMMENDED.
- L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1. PIN NUMBERS SHOWN FOR COILTRONICS UNIT
- L2 = COILTRONICS-CTX300-4
- * = 1% FILM RESISTOR
- DO NOT SUBSTITUTE COMPONENTS

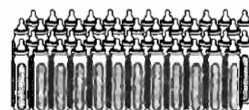


Figure 36. Cold Cathode Fluorescent Lamp Power Supply

Application Note 45

When power is applied the LT1072 switching regulator's feedback pin is below the device's internal 1.23V reference, causing full duty cycle modulation at the V_{SW} pin (trace A, Figure 37). L2 conducts current (trace B), which flows

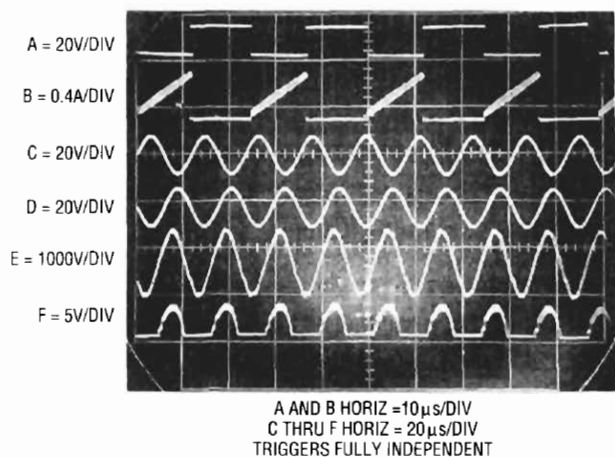


Figure 37. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B and C Through F.

from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

L1 and the transistors comprise a current driven Royer class converter⁵ which oscillates at a frequency primarily set by L1's characteristics and the 0.02µF capacitor. LT1072 driven L2 sets the magnitude of the Q1-Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1072 is off. The LT1072's 40kHz clock rate is asynchronous from the Royer converter's (~60kHz) rate, accounting for trace B's waveform thickening.

The 0.02µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (traces C and D, respectively). L1 furnishes voltage step-up, and about 1400Vp-p appears at its secondary (trace E). Current flows through the 33pF capacitor into the lamp. On negative waveform cycles the lamp's

current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across these resistors (trace F) represents 1/2 the lamp current. This signal is filtered by the 10k-1µF pair and presented to the LT1072's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1072's V_C pin provides stable loop compensation. The loop forces the LT1072 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0-100% intensity control with no lamp dead zones or "pop-on" at low intensities. Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

Several points should be kept in mind when observing this circuit's operation. L1's high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*⁶ Tektronix probe type P-6009 (acceptable) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

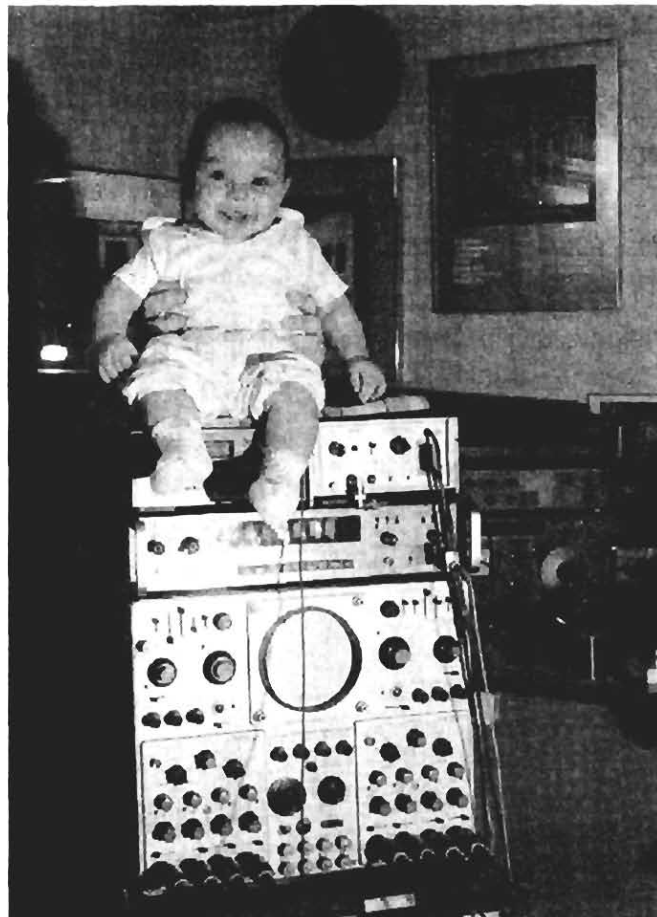
Another consideration involves observing waveforms. The LT1072's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 37 was obtained using a dual beam oscilloscope (Tektronix 556). LT1072 related traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Note 5: See Reference 8.

Note 6: Don't say we didn't warn you!

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High Speed Amplifier Techniques

A Designer's Companion for Wideband Circuitry

Jim Williams

PREFACE

This publication represents the largest LTC commitment to an application note to date. No other application note absorbed as much effort, took so long or cost so much. This level of activity is justified by our belief that high speed monolithic amplifiers greatly interest users.

Historically, monolithic amplifiers have represented packets of inexpensive, precise and controllable gain. They have partially freed engineers from the constraints and frustrations of device level design. Monolithic operational amplifiers have been the key to practical implementation of high level analog functions. As good as they are, one missing element in these devices has been speed.

Devices presently coming to market are addressing monolithic amplifiers' lack of speed. They bring with them the ease of use and inherent flexibility of op amps. When

Philbrick Researches introduced the first mass produced op amp in the 1950's (K2-W) they knew it would be used. What they couldn't possibly know was just how widely, and how many different types of applications there were. As good a deal as the K2-W was (I paid \$24.00 for mine - or rather, my father did), monolithic devices are far better. The combination of ease of use, economy, precision and versatility makes modern op amps just too good to be believed.

Considering all this, adding speed to op amps' attractions seems almost certain to open up new application areas. We intend to supply useful high speed products and the level of support necessary for their successful application (such high minded community spirit is, of course, capitalism's deputy). We hope you are pleased with our initial efforts and look forward to working together.

TABLE OF CONTENTS

PREFACE	AN47-1
INTRODUCTION	AN47-5
PERSPECTIVES ON HIGH SPEED DESIGN	AN47-5
MR. MURPHY'S GALLERY OF HIGH SPEED AMPLIFIER PROBLEMS	
Unterminated Pulse Generator	AN47-7
Poorly Terminated Line	AN47-8
Poor Probe Grounding	AN47-8
Undercompensated Probe	AN47-8
Overcompensated Probe	AN47-9
Mismatched Delay in Probes	AN47-9
Overdriven FET Probe	AN47-9
Probe at Amplifier Summing Point	AN47-10
Poor Quality Probe	AN47-10
Oscilloscope Overdriven	AN47-10
Poor or No Ground Plane	AN47-11
No Bypass Capacitors, Heavy Load	AN47-11
No Bypass Capacitors, No Load	AN47-11
Poor Quality Bypass Capacitors	AN47-12
Paralleled Bypass Capacitors Ring	AN47-12
Almost Good Enough Bypass Capacitors	AN47-12
2pF at Amplifier Summing Junction	AN47-12
Noise Due to Coupling Into Critical Nodes	AN47-13
1pF Coupling Path's Effects	AN47-13
Decompensated Amplifier at Too Low a Gain	AN47-13
Excessive Capacitive Load	AN47-13
Common Mode Overdrive	AN47-14
Booster Stage with Local Oscillations	AN47-14
Booster Stage with Loop Oscillations	AN47-14
Excessive Source Impedance	AN47-14
TUTORIAL SECTION	
About Cables, Connectors and Terminations	AN47-15
About Probes and Probing Techniques	AN47-16
About Oscilloscopes	AN47-20
About Ground Planes	AN47-24
About Bypass Capacitors	AN47-25
Breadboarding Techniques	AN47-26
Oscillation	AN47-29

APPLICATIONS SECTION I - AMPLIFIERS

Fast 12-Bit DAC Amplifier	AN47-32
2-Channel Video Amplifier	AN47-32
Simple Video Amplifier	AN47-32
Loop Through Cable Receivers	AN47-32
DC Stabilization – Summing Point Technique	AN47-33
DC Stabilization – Differentially Sensed Technique	AN47-34
DC Stabilization – Servo Controlled FET Input Stage	AN47-34
DC Stabilization – Full Differential Inputs with Parallel Paths	AN47-35
DC Stabilization – Full Differential Inputs, Gain-of-1000 with Parallel Paths	AN47-35
High Speed Differential Line Receiver	AN47-37
Transformer Coupled Amplifier	AN47-38
Differential Comparator Amplifier with Adjustable Offset	AN47-39
Differential Comparator Amplifier with Settable Automatic Limiting and Offset	AN47-40
Photodiode Amplifier	AN47-41
Fast Photo Integrator	AN47-41
Fiber Optic Receiver	AN47-43
40MHz Fiber Optic Receiver with Adaptive Trigger	AN47-43
50MHz High Accuracy Analog Multiplier	AN47-44
Power Booster Stage	AN47-45
High Power Booster Stage	AN47-47
Ceramic Bandpass Filters	AN47-48
Crystal Filter	AN47-48

APPLICATIONS SECTION II - OSCILLATORS

Sine Wave Output Quartz Stabilized Oscillator	AN47-48
Sine Wave Output Quartz Stabilized Oscillator with Electronic Gain Control	AN47-49
DC Tuned 1MHz-10MHz Wien Bridge Oscillator	AN47-49
Complete AM Radio Station	AN47-50

APPLICATIONS SECTION III - DATA CONVERSION

1Hz-1MHz Voltage-Controlled Sine Wave Oscillator	AN47-51
1Hz-10MHz V → F Converter	AN47-54
8-Bit, 100ns Sample-Hold	AN47-56
15ns Current Summing Comparator	AN47-57
50MHz Adaptive Threshold Trigger Circuit	AN47-58
Fast Time-to-Height (Pulsewidth-to-Voltage) Converter	AN47-58
True RMS Wideband Voltmeter	AN47-61

APPLICATIONS SECTION IV - MISCELLANEOUS CIRCUITS

RF Leveling Loop	AN47-63
Voltage Controlled Current Source	AN47-63
High Power Voltage Controlled Current Source	AN47-63
18ns Circuit Breaker	AN47-63

Application Note 47

REFERENCES..... AN47-67

APPENDICES

A. ABC's of Probes – Contributed by Tektronix, Inc.	AN47-69
B. Measuring Amplifier Settling Time	AN47-82
C. The Oscillation Problem – Frequency Compensation Without Tears	AN47-86
D. Measuring Probe-Oscilloscope Response	AN47-93
E. An Ultra Fast High Impedance Probe	AN47-96
F. Additional Comments on Breadboarding	AN47-98
G. FCC Licensing and Construction Permit Applications for Commercial AM Broadcasting Stations	AN47-123
H. About Current Mode Feedback	AN47-124
I. High Frequency Amplifier Evaluation Board	AN47-127
J. The Contributions of Edsel Murphy to the Understanding of the Behavior of Inanimate Objects, D.L. Klipstein (with permission of Cahners Publishing Co.)	AN47-130

INTRODUCTION

Most monolithic amplifiers have been relatively slow devices. Wideband operation has been the province of discrete and hybrid technologies. Some fast monolithic amplifiers have been available, but the exotic and expensive processing required has inflated costs, precluding widespread acceptance. Additionally, many of the previous monolithic designs were incapable of high precision and prone to oscillation or untoward dynamics, making them unattractive.

Recent processing and design advances have made inexpensive, precision wideband amplifiers practical. Figure 1 lists some amplifiers, along with a summary of their characteristics. Reviewing this information reveals extraordinarily wideband devices, with surprisingly good DC characteristics. All of these amplifiers utilize standard op amp architecture, except the LT1223 and LT1228, which are so-called current mode feedback types (see Appendix H, "About Current Mode Feedback"). It is clear that the raw speed capabilities of these devices, combined with their inherent flexibility as op amps, permit a wide range of applications. What is required of the user is a familiarity with the devices and respect for the requirements of high speed circuitry.

This effort's initial sections are devoted to familiarizing the reader with the realities and difficulties of high speed circuit work. The mechanics and subtleties of achieving precision circuit operation at DC and low frequency have been well documented. Relatively little has appeared which discusses, in practical terms, how to get fast circuitry to work. In developing such circuits, even veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high speed circuits can only work if negotiated compromises with nature are arranged. Ignorance of, or contempt for, physical law is a direct route to frustration. Mother Nature laughs at dilettantism and crushes arrogance without even knowing she did it. Even without Einstein's revelations, the world of high speed is full of surprises. Working with events measured in nanoseconds requires the greatest caution, prudence and respect for Mother Nature. Absolutely nothing should be taken for granted, because nothing is. Circuit design is very much the art of compromise with parasitic effects. The "hidden

schematic" (this descriptive was originated by Charly Gullett of Intel Corporation) usually dominates the circuit's form, particularly at high speed.

In this regard, much of the text and appendices are directed at developing awareness of, and respect for, circuit parasitics and fundamental limitations. This approach is maintained in the applications section, where the notion of negotiated compromises is expressed in terms of resistor values and compensation techniques. Many of the application circuits use the amplifier's speed to improve on a standard circuit. Some utilize the speed to implement a traditional function in a non-traditional way, with attendant advantages. A (very) few operate at or near the state-of-the-art for a given circuit type, regardless of approach. Substantial effort has been expended in developing these examples and documenting their operation. The resultant level of detail is justified in the hope that it will be catalytic. The circuits should stimulate new ideas to suit particular needs, while demonstrating fast amplifiers' capabilities in an instructive manner.

PERSPECTIVES ON HIGH SPEED DESIGN

A substantial amount of design effort has made Figure 1's amplifiers relatively easy to use. They are less prone to oscillation and other vagaries than some much slower amplifiers. Unfortunately, laws of physics dictate that the circuit's *environment* must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns, delays and memory access times in terms of nanoseconds. Figure 2's test circuit provides valuable perspective on just how fast these amplifiers are. Here, the pulse generator (Trace A, Figure 3) drives a 74S04 Schottky TTL inverter (Trace B), an LT1223 op amp connected as an inverter (Trace C), and a 74HC04 high speed CMOS inverter (Trace D). The LT1223 doesn't fare too badly. Its delay and fall times are about 2ns slower than the 74S04, but significantly faster than the 74HC04. In fact, the LT1223 has completely finished its transition before the 74HC04 even begins to move! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in

PARAMETER	LT1122	LT1190	LT1191	LT1192	LT1193	LT1194	LT1220	LT1221	LT1222	LT1223	LT1224
Slew Rate	60V/ μ s	450V/ μ s	450V/ μ s	450V/ μ s	450V/ μ s	DIFFERENTIAL 450V/ μ s	250V/ μ s	250V/ μ s	200V/ μ s	1000V/ μ s	300V/ μ s
Bandwidth	14MHz	50MHz	90MHz	400MHz	70MHz	70MHz	45MHz	150MHz	350MHz	100MHz	45MHz
Delay-Rise Time	15ns-65ns	4ns-7ns	3.5ns-1.6ns	5ns-7ns	4ns-7ns	4ns-7ns	4ns-4ns	5ns-5ns	5ns-5ns	3.5ns-3.5ns	4ns-4ns
Settling Time	340ns-0.01%	100ns-0.1%	100ns-0.1%	80ns-0.1%	100ns-0.1%	100ns-0.1%	90ns-0.1%	90ns-0.1%	90ns-0.1%	75ns-0.1%	90ns-0.1%
Output Current	6mA	50mA	50mA	50mA	50mA	50mA	24mA	24mA	24mA	50mA	40mA
Offset	600 μ V	4mV	2mV	2mV	3mV	3mV	2mV	1mV	1mV	3mV	1mV
Drift	6 μ V/ $^{\circ}$ C						20 μ V/ $^{\circ}$ C	15 μ V/ $^{\circ}$ C	10 μ V/ $^{\circ}$ C		20 μ V/ $^{\circ}$ C
Bias Current	75pA	500nA	500nA	500nA	500nA	500nA	300nA	300nA	300nA	3 μ A	6 μ A
Gain	500,000	22,000	45,000	200,000	Adjustable	10	20,000	50,000	100,000	90dB	80dB
Gain Error (Minimum Gain)				$A_{V_{MIN}} = 10$	0.1%	0.1%		$A_{V_{MIN}} = 4$	$A_{V_{MIN}} = 10$		$A_{V_{MIN}} = 1$
Gain Drift											
Power Supply	40V	18V _{MAX}	18V _{MAX}	18V _{MAX}	18V _{MAX}	18V _{MAX}	36V	36V	36V	36V _{MAX}	36V

Figure 1. Characteristics of Some Different Fast IC Amplifiers

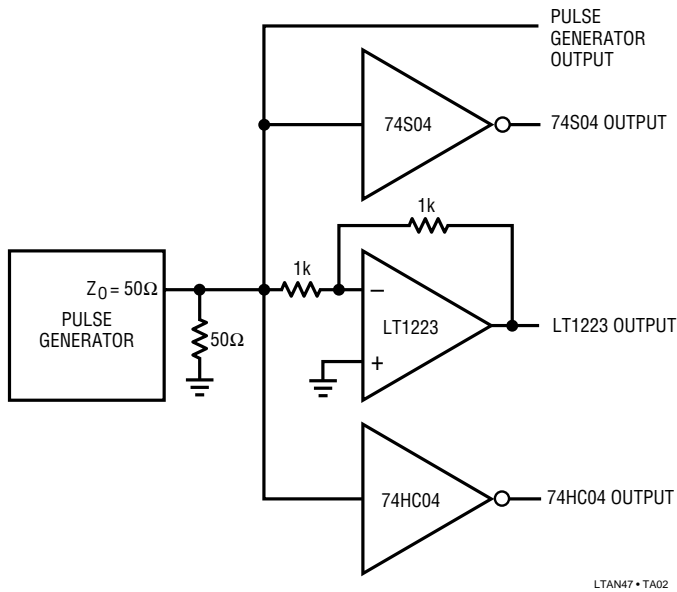


Figure 2. A Race Between the LT1223 Amplifier and Some Fast Logic Inverters

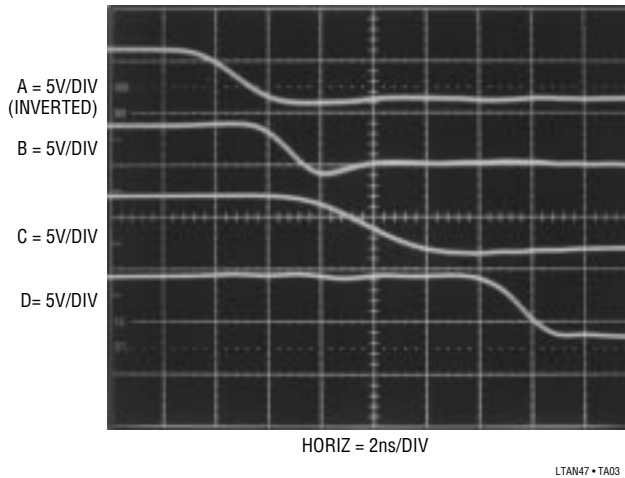


Figure 3. The Amplifier (Trace C) is 3ns Slower than 74S Logic (Trace B), but 5ns Faster than High Speed HCMOS (Trace D)!

circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses, and dissimilar operation between two identical circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit environment. To learn how to do this

requires studying the causes of the aforementioned difficulties.

The following segments, “Mr. Murphy’s Gallery of High Speed Amplifier Problems” and the “Tutorial Section”, address this. The “Problems” section alerts the reader to trouble areas, while the “Tutorial” highlights theory and techniques which may be applied towards solving the problems shown. The tutorials are arranged in roughly the same order as the problems are presented.

MR. MURPHY’S GALLERY OF HIGH SPEED AMPLIFIER PROBLEMS

It sometimes seems that Murphy’s Law dominates all physical law. For a complete treatise on Murphy’s Law, see Appendix J, “The Contributions of Edsel Murphy to the Understanding of the Behavior of Inanimate Objects”, by D.L. Klipstein. The law’s consequences weigh heavily in high speed design. As such, a number of examples are given in the following discussion. The average number of phone calls we receive per month due to each “Murphy” example appears at the end of each figure caption.

Problems can start even before power is applied to the amplifier. Figure 4 shows severe ringing on the pulse edges at the output of an unterminated pulse generator cable. This is due to reflections and may be eliminated by terminating the cable. *Always terminate the source in its characteristic impedance when looking into cable or long PC traces. Any path over 1 inch long is suspect.*

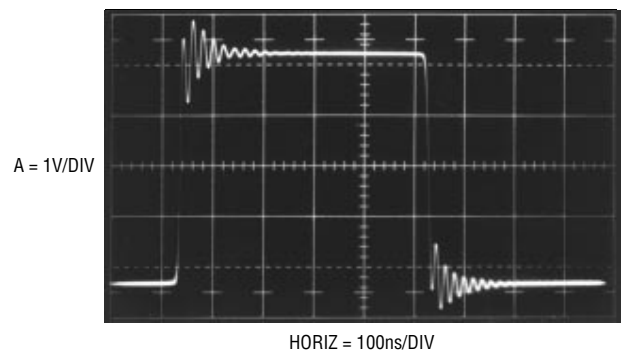


Figure 4. An Unterminated Pulse Generator Cable Produces Ringing Due to Reflections – 3 ☎

In Figure 5 the cable is terminated, but ripple and aberration are still noticeable following the high speed edge transitions. In this instance the terminating resistor’s leads are lengthy ($\approx 3/4"$), preventing a high integrity wideband termination.

Application Note 47

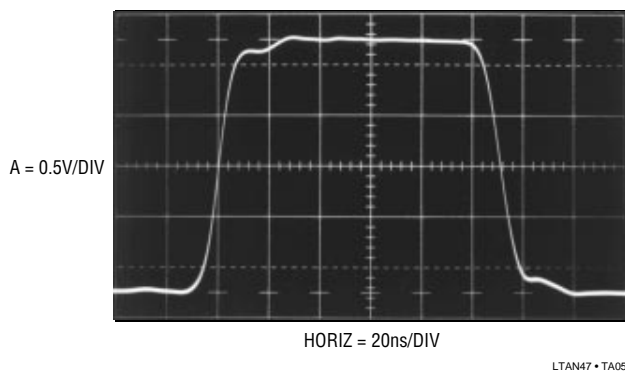


Figure 5. Poor Quality Termination Results in Pulse Corner Aberrations – 1 📞

The best termination for 50Ω cable is the BNC coaxial type. These devices should not simply be resistors in an enclosure. Good grade 50Ω terminators maintain true coaxial form. They use a carefully designed 50Ω resistor with significant effort devoted to connections to the actual resistive element. In particular, the largest possible connection surface area is utilized to minimize high speed losses. While these type terminators are practical on the test bench, they are rarely used as board level components. In general, the best termination resistors for PC board use are carbon or metal film types with the shortest possible lead lengths. These resistor's end-cap connections provide better high speed characteristics than the rod-connected composition types. Wirewound resistors, because of their inherent and pronounced inductive characteristics, are completely unsuitable for high speed work. This includes so-called non-inductive types.

Another termination consideration is disposal of the current flowing through the terminator. The terminating resistor's grounded end should be placed so that the high speed currents flowing from it do not disrupt circuit operation. For example, it would be unwise to return terminator current to ground near the grounded positive input of an inverting op amp. The high speed, high density (5V pulses through a 50Ω termination generates 100mA current spikes) current flow could cause serious corruption of the desired zero volt op amp reference. This is another reason why, for bench testing, the coaxial BNC terminators are far preferable to discrete, breadboard mounted resistors. With BNC types in use the termination current returns directly to the source generator and never flows in the breadboard. (For more information see the Tutorial section.) *Select terminations carefully and evaluate the effects of their placement in the test set-up.*

Figure 6 shows an amplifier output which rings and distorts badly after rapid movement. In this case, the probe ground lead is too long. For general purpose work, most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. (Probes are covered in the Tutorial section; also see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.). *Keep the probe ground connection as short as possible. The ideal probe ground connection is purely coaxial. This is why probes mated directly to board mounted coaxial connectors give the best results.*

In Figure 7 the probe is properly grounded, but a new problem pops up. This photo shows an amplifier output

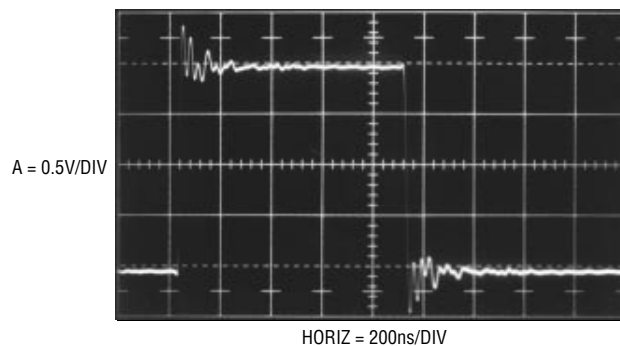


Figure 6. Poor Probe Grounding Badly Corrupts the Observed Waveform – 53 📞

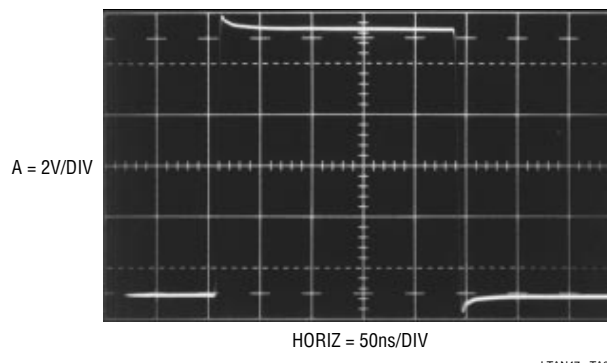


Figure 7. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error – 12 📞

excursion of 11V — quite a trick from an amplifier running from $\pm 5V$ rails. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly.* (For discussions on probes, see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc. and the Tutorial section.) Figure 8 shows another probe-induced problem. Here the amplitude seems correct but the amplifier appears slow with pronounced edge rounding. In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or straight probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

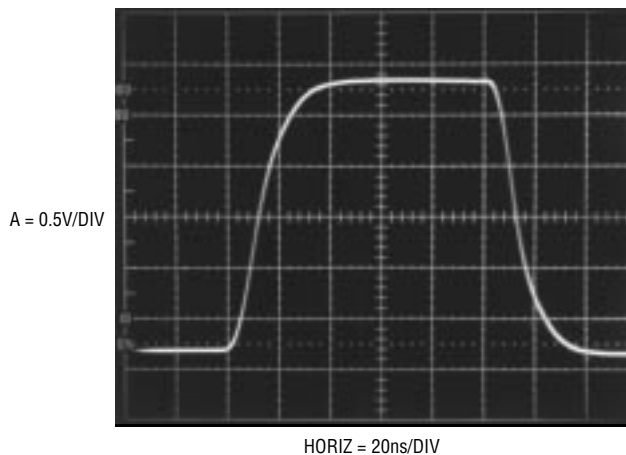


Figure 8. Overcompensated or Slow Probes Make Edges Look Too Slow – 2 📞

Mismatched probes account for the apparent excessive amplifier delay in Figure 9. Delay of almost 12ns (Trace A is the input, Trace B the output) is displayed for an amplifier specified at 6ns. Always keep in mind that various types of probes have different signal transit delay times. At high sweep speeds, this effect shows up in multi-trace displays as time skewing between individual channels. Using similar probes will eliminate this problem, but measurement requirements often dictate dissimilar probes. In such cases the differential delay should be measured and then mentally factored in to reduce error when interpreting the display. It is worth noting that active probes,

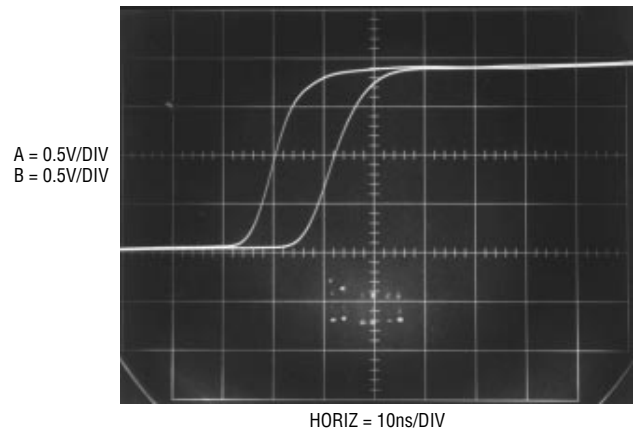


Figure 9. Probes with Mismatched Delays Produce Apparent Time Skewing in the Display – 4 📞

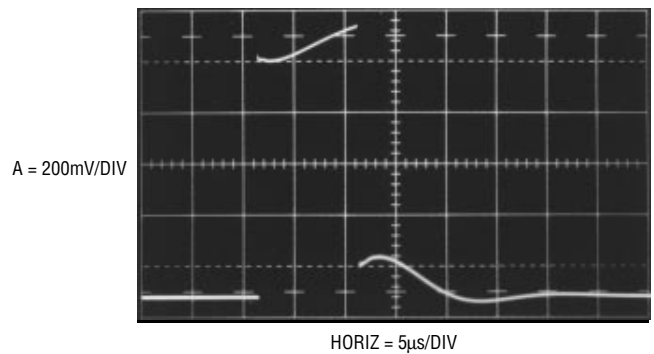


Figure 10. Overdriven FET Probe Produces Excessive Waveform Distortion and Tailing. Saturation Effects can Also Cause Delayed Response – 1 📞

such as FET and current probes, have signal transit times as long as 25ns. A fast 10X or 50Ω probe delay can be inside 3ns. *Account for probe delays in interpreting oscilloscope displays.*

The difficulty shown in Figure 10 is a wildly distorted amplifier output. The output slews quickly, but the pulse top and bottom recoveries have lengthy, tailing responses. Additionally, the amplifier output seems to clip well below its nominal rated output swing. A common oversight is responsible for these conditions. A FET probe monitors the amplifier output in this example. The probe's common-mode input range has been exceeded, causing it to overload, clip and distort badly. When the pulse rises, the probe is driven deeply into saturation, forcing internal circuitry away from normal operating points. Under these conditions the displayed pulse top is illegitimate. When the output falls, the probe's overload recovery is lengthy and uneven, causing the tailing. More subtle forms of FET

Application Note 47

probe overdrive may show up as extended delays with no obvious signal distortion. *Know your FET probe. Account for the delay of its active circuitry. Avoid saturation effects due to common-mode input limitations (typically $\pm 1V$). Use 10X and 100X attenuator heads when required.*

Figure 11's probe-caused problem results in amplifier output peaking and ringing. In other respects the display is acceptable. This output peaking characteristic is caused by a second 10X probe connected to the amplifier's summing junction. Because the summing point is so central to analyzing op amp operation, it is often monitored. At high speed the 10pF probe input capacitance causes a significant lag in feedback action, forcing the amplifier to overshoot and hunt as it seeks the null point. Minimizing this effect calls for the lowest possible probe input capacitance, mandating FET types or special passive probes. (Probes are covered in the Tutorial section; also see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.). *Account for the effects of probe capacitance, which often dominates its impedance characteristics at high speeds. A standard 10pF 10X probe forms a 10ns lag with a 1K Ω source resistance.*

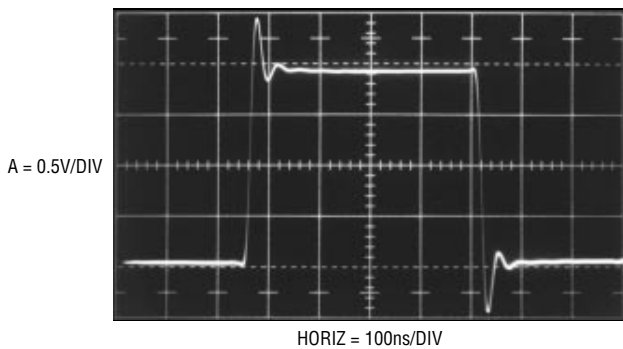


Figure 11. Effect of a 10X, 10pF 'Scope Probe at the Summing Point – 2 📞

A peaked, tailing response is Figure 12's characteristic. The photo shows the final 40mV of a 2.5V amplifier excursion. Instead of a sharp corner which settles cleanly, peaking occurs, followed by a lengthy tailing decay. This waveform was recorded with an inexpensive off-brand 10X probe. Such probes are often poorly designed, and constructed from materials inappropriate for high speed work. The selection and integration of materials for wideband probes is a specialized and difficult art. Sub-

stantial design effort is required to get good fidelity at high speeds. *Never use probes unless they are fully specified for wideband operation. Obtain probes from a vendor you trust.*

Figure 13 shows the final movements of an amplifier output excursion. At only 1mV per division the objective is to view the settling residue to high resolution. This response is characterized by multiple time constants, non-linear slew recovery and tailing. Note also the high speed event just before the waveform begins its negative going transition. What is actually being seen is the oscilloscope recovering from excessive overdrive. Any observation that requires off-screen positioning of parts of the waveform should be approached with the greatest caution. Oscilloscopes vary widely in their response to overdrive, bringing displayed results into question. Complete treatment of high resolution settling time measurements and oscilloscope overload characteristics is given in the Tutorial section, "About Oscilloscopes" and Appendix B "Measuring Amplifier Settling Time". *Approach all oscilloscope*

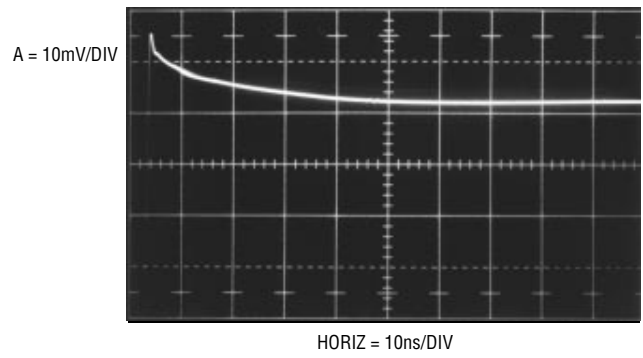


Figure 12. Poor Quality 10X Probe Introduces Tailing – 2 📞

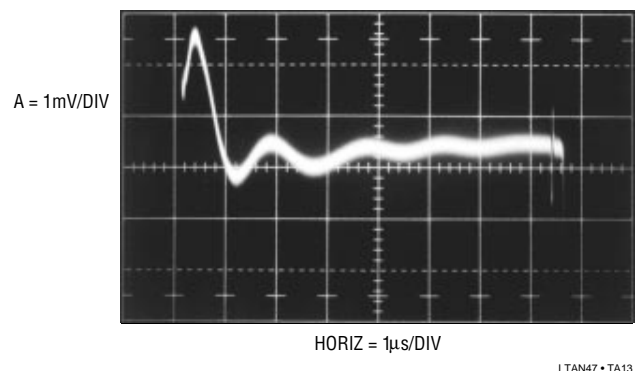


Figure 13. Overdriven Oscilloscope Display Says More About the Oscilloscope than the Circuit it's Connected to – 6 📞

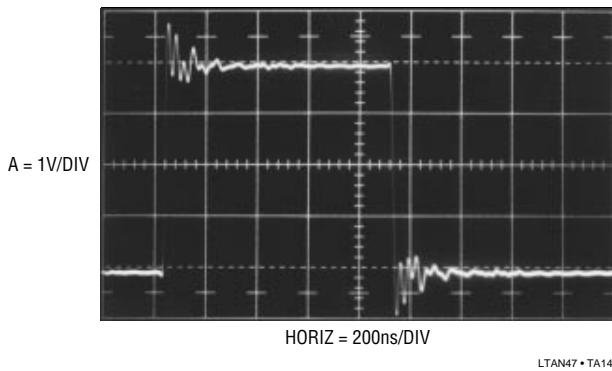


Figure 14. Instabilities Due to No Ground Plane Produce a Display Similar to a Poorly Grounded Probe – 62 📞

measurements which require off-screen activity with caution. Know your instrument's capabilities and limitations.

Sharp eyed readers will observe that Figure 14 is a duplicate of Figure 6. Such lazy authorship is excusable because almost precisely the same waveform results when no ground plane is in use. A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. (The theory behind ground planes is discussed in the Tutorial section). The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with high speed circuitry.*

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can “communicate” through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts as an electrical flywheel to keep supply impedance low at high

frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully (see Tutorial, “About Bypass Capacitors”). An unbypassed amplifier with a 100Ω load is shown in Figure 15. The power supply the amplifier sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the amplifier and its load, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. *Always use bypass capacitors.*

In Figure 16 the 100Ω load is removed, and a pulse output is displayed. The unbypassed amplifier responds surprisingly well, but overshoot and ringing dominate. *Always use bypass capacitors.*

Figure 17's settling is noticeably better, but some ringing remains. This response is typical of lossy bypass capacitors, or good ones placed too far away from the amplifier. *Use good quality, low loss bypass capacitors, and place them as close to the amplifier as possible.*

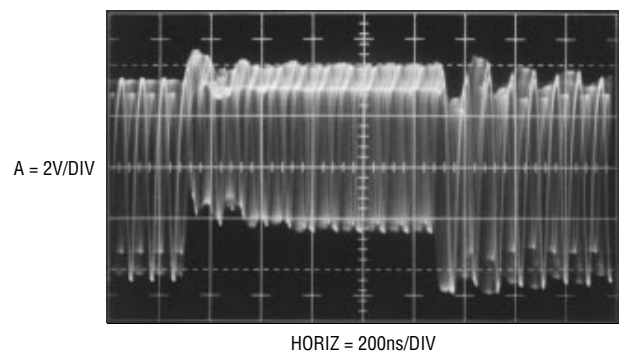


Figure 15. Output of an Unbypassed Amplifier Driving a 100Ω Load Without Bypass Capacitors – 58 📞

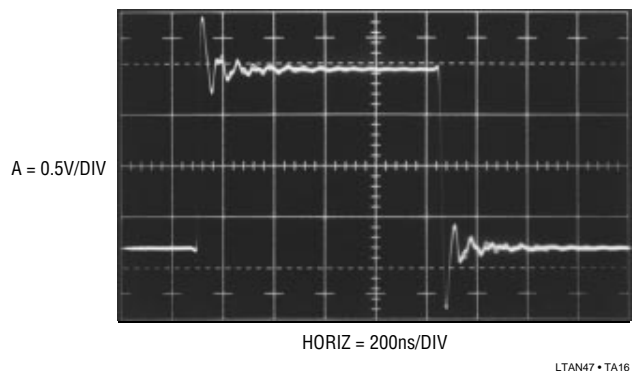


Figure 16. An Unbypassed Amplifier Driving No Load is Surprisingly Stable...at the Moment – 49 📞

Application Note 47

The multiple time constant ringing in Figure 18 often indicates poor grade paralleled bypassing capacitors or excessive trace length between the capacitors. While paralleling capacitors of different characteristics is a good way to get wideband bypassing, it should be carefully considered. Resonant interaction between the capacitors can cause a waveform like this after a step.

This type response is often aggravated by heavy amplifier loading. *When paralleling bypass capacitors, plan the layout and breadboard with the units you plan to use in production.*

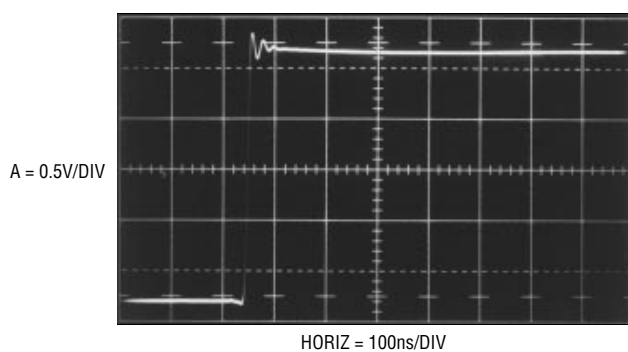


Figure 17. Poor Quality Bypass Capacitor Allows Some Ringing – 28 📞

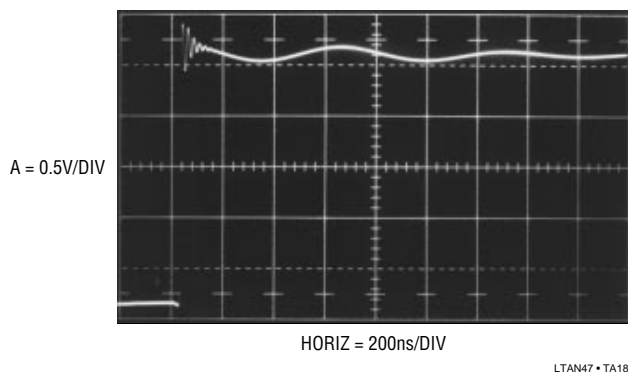


Figure 18. Paralleled Bypass Capacitors Form a Resonant Network and Ring – 2 📞

Figure 19 addresses a more subtle bypassing problem. The trace shows the last 40mV excursion of a 5V step almost settling cleanly in 300ns. The slight overshoot is due to a loaded (500Ω) amplifier without quite enough bypassing. Increasing the total supply bypassing from 0.1μF to 1μF cured this problem. *Use large value paralleled bypass capacitors when very fast settling is required, particularly if the amplifier is heavily loaded or sees fast load steps.*

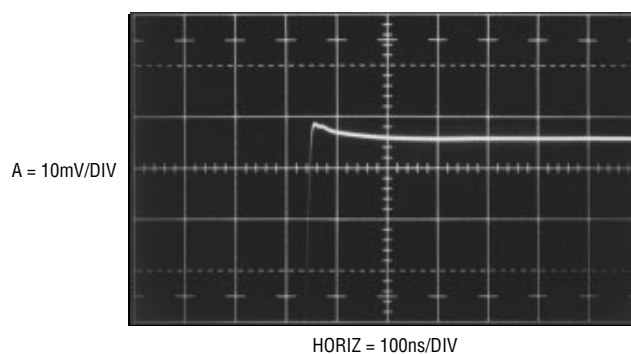


Figure 19. A More Subtle Bypassing Problem. Not-Quite-Good-Enough Bypassing Causes a Few Millivolts of Peaking – 1 📞

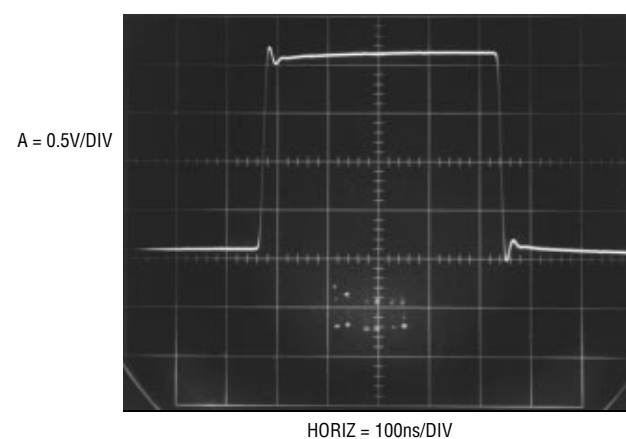
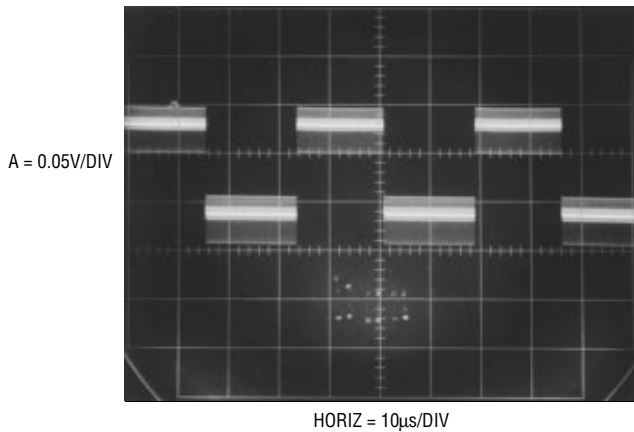


Figure 20. 2pF Stray Capacitance at the Summing Point Introduces Peaking – 4 📞

The problem shown in Figure 20, peaking on the leading and trailing corners, is typical of poor layout practice (see Tutorial section on “Breadboarding Techniques”). This unity gain inverter suffers from excessive trace area at the summing point. Only 2pF of stray capacitance caused the peaking and ring shown. *Minimize trace area and stray capacitance at critical nodes. Consider layout as an integral part of the circuit and plan it accordingly.*

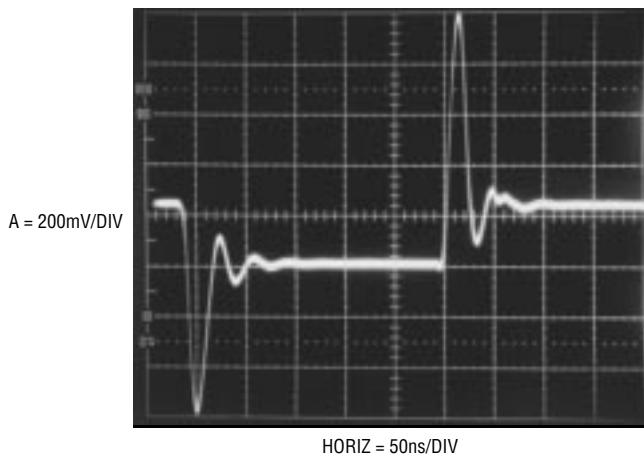
Figure 21’s low level square wave output appears to suffer from some form of parasitic oscillation. In actuality, the disturbance is typical of that caused by fast digital clocking or switching regulator originated noise getting into critical circuit nodes. *Plan for parasitic radiative or conductive paths and eliminate them with appropriate layout and shielding.*

Figure 22 underscores the previous statement. This output was taken from a gain-of-ten inverter with 1kΩ input



LTAN47 • TA21

Figure 21. Clock or Switching Regulator Noise Corrupts Output Due to Poor Layout – 3 📞



LTAN47 • TA22

Figure 22. Output of an X10 Amplifier with 1pF Coupling from the Summing Point to the Input. Careful Shielding of the Input Resistor Will Eliminate the Peaked Edges and Ringing – 2 📞

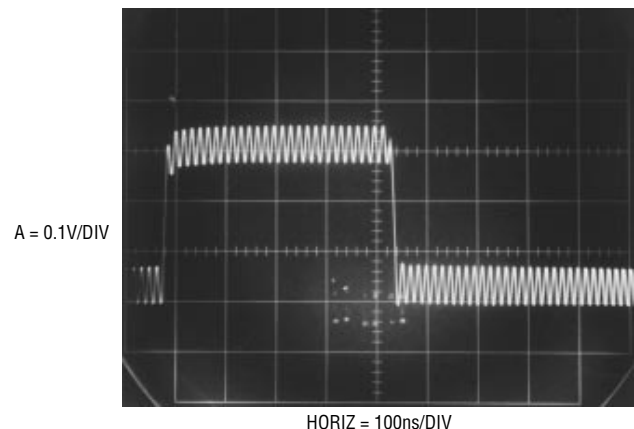
resistance. It shows severe peaking induced by *only 1pF* of parasitic capacitance across the 1k resistor. The 50Ω terminated input source provides only 20mV of drive via a divider, but that’s more than enough to cause problems, even with only 1pF stray coupling. In this case the solution was a ground referred shield at a right angle to, and encircling, the 1kΩ resistor. *Plan for parasitic radiative paths and eliminate them with appropriate shielding.*

A decompensated amplifier running at too low a gain produced Figure 23’s trace. The price for decompensated amplifiers’ increased speed is restrictions on minimum allowable gain. Decompensated amplifiers are simply not stable below some (specified) minimum gain, and no amount of ignorance or wishing will change this. This is a

common applications oversight with these devices, although the amplifier never fails to remind the user. *Observe gain restrictions when using decompensated amplifiers.*

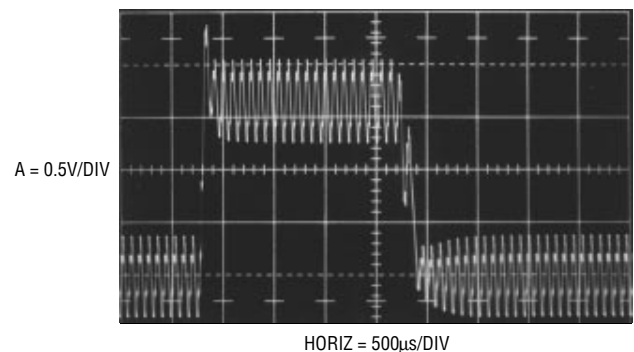
Oscillation is also the problem in Figure 24, and it is due to excessive capacitive loading (see Tutorial section on “Oscillation”). Capacitive loading to ground introduces lag in the feedback signal’s return to the input. If enough lag is introduced (e.g., a large capacitive load) the amplifier may oscillate. Even if a capacitively loaded amplifier doesn’t oscillate, it’s always a good idea to check its response with step testing. It’s amazing how close to the edge of the cliff you can get without falling off, except when you build 10,000 production units. *Avoid capacitive loading. If such loading is necessary, check performance margins and isolate or buffer the load if necessary.*

Figure 25 appears to contain one cycle of oscillation. The output waveform initially responds, but abruptly reverses direction, overshoots and then heads positive again. Some



LTAN47 • TA23

Figure 23. Decompensated Amplifier Running at Too Low a Gain – 22 📞



LTAN47 • TA24

Figure 24. Excessive Capacitive Load Upsets the Amplifier – 165 📞

Application Note 47

overshoot again occurs, with a long tail and a small dip well before a non-linear slew returns the waveform to zero. Ugly overshoot and tailing completes the cycle. This is certainly strange behavior. What is going on here? The input pulse is responsible for all these anomalies. Its amplitude takes the amplifier outside its common-mode limits, inducing the bizarre effects shown. *Keep inputs inside specified common-mode limits at all times.*

Figure 26 shows an oscillation laden output (Trace B) trying to unity gain invert the input (Trace A). The input's form is distinguishable in the output, but corrupted with very high frequency oscillation and overshoot. In this case the amplifier includes a booster within its loop to provide increased output current. The disturbances noted are traceable to local instabilities within the booster circuit. (See Appendix C, "The Oscillation Problem — Frequency Compensation Without Tears"). *When using output booster stages, insure they are inherently stable before placing them inside an amplifier's feedback loop. Wideband booster stages are particularly prone to device level parasitic high frequency oscillation.*

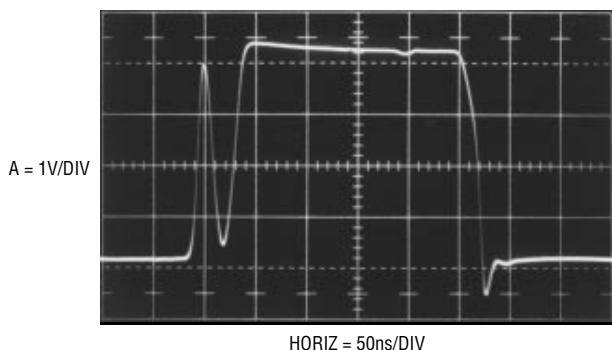


Figure 25. Input Common Mode Overdrive Generates Odd Outputs – 3 📞

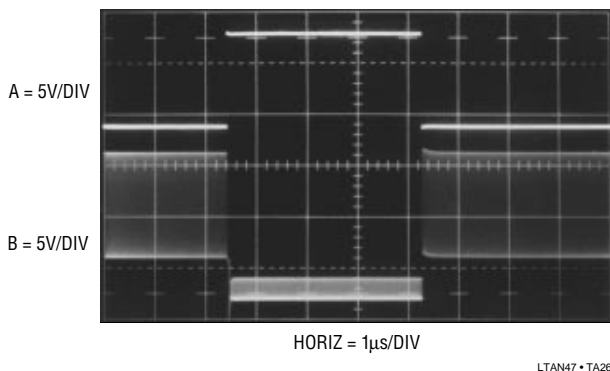


Figure 26. Local Oscillations in a Booster Stage. Frequency is Typically High – 12 📞

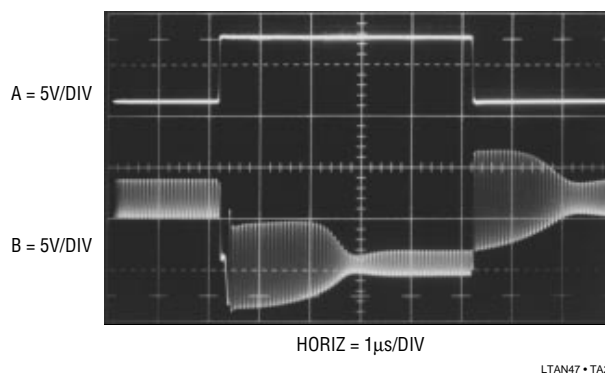


Figure 27. Loop Oscillations in a Booster Stage. Note Lower Frequency than Local Oscillations in Previous Example – 28 📞

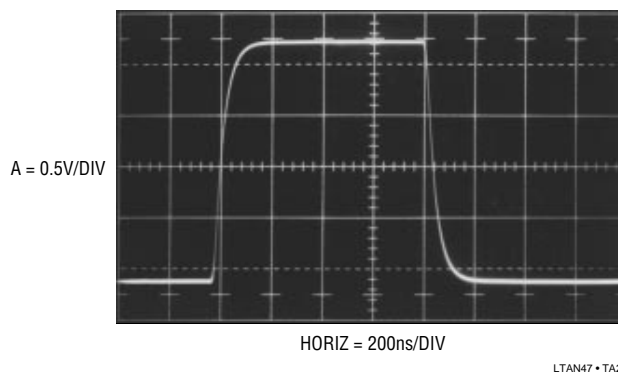


Figure 28. Excessive Source Impedance Gives Serene But Undesired Response – 6 📞

Figure 27's booster augmented unity gain inverting op amp also oscillates, but at a much lower frequency. Additionally, overshoot and non-linear recovery dominate the waveform's envelope. Unlike the previous example, this behavior is not due to local oscillations within the booster stage. Instead, the booster is simply too slow to be included in the op amp's feedback loop. It introduces enough lag to force oscillation, even as it hopelessly tries to maintain loop closure. *Insure booster stages are fast enough to maintain stability when placed in the amplifier's feedback loop.*

The serene rise and fall of Figure 28's pulse is a welcome relief from the oscillatory screaming of the previous photos. Unfortunately, such tranquilized behavior is simply too slow. This waveform, reminiscent of Figure 8's bandlimited response, is due to excessive source impedance. The high source impedance combines with amplifier input capacitance to band limit the input and the output reflects this action. *Minimize source impedance to levels*

which maintain desired bandwidth. Keep stray capacitance at inputs down.

TUTORIAL SECTION

An implied responsibility in raising the aforementioned issues is their solution or elimination. What good is all the rabble-raising without suggestions for fixes? It is in this spirit that this tutorial section is presented. Theory, techniques, prejudice and just plain gossip are offered as tools which may help avoid or deal with difficulties. As previously mentioned, the tutorials appear in roughly the same order as the problems were presented.

About Cables, Connectors and Terminations

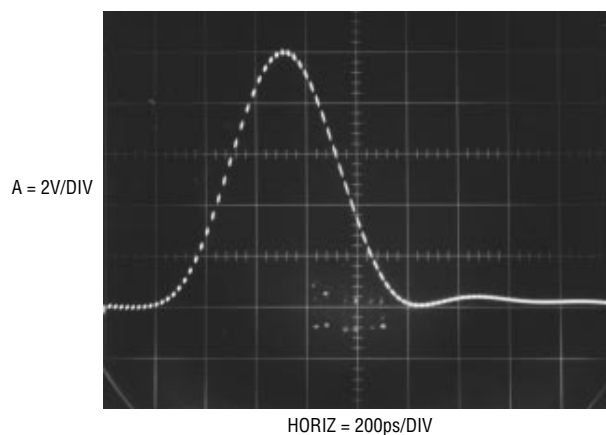
Routing of high speed signals to and from the circuit board should always be done with good quality coaxial cable. The cable should be driven and terminated in the system's characteristic impedance at the drive and load points. The driven end is usually an instrument (e.g., pulse or signal generator), presumably endowed with proper characteristics by its manufacturer. It is the cable and its termination, selected by the experimenter, that often cause problems.

All coaxial cable is not the same. Use cable appropriate to the system's characteristic impedance and of good quality. Poorly chosen cable materials or construction methods can introduce odd effects at very high speeds, resulting in observed waveform distortion. A poor cable choice can adversely effect 0.01% settling in the 100ns-200ns region. Similarly, poor cable can preclude maintenance of even the cleanest pulse generator's 1ns rise time or purity. Typically, inappropriate cable can introduce tailing, rise time degradation, aberrations following transitions, non-linear impedance and other undesirable characteristics.

Termination choice is equally important. Good quality BNC coaxial type terminators are usually the best choice for breadboarding. Their impedance vs frequency is flat into the GHz range. Additionally, their construction insures that the (often substantial) drive current returns directly to the source, instead of being dumped into the breadboard's

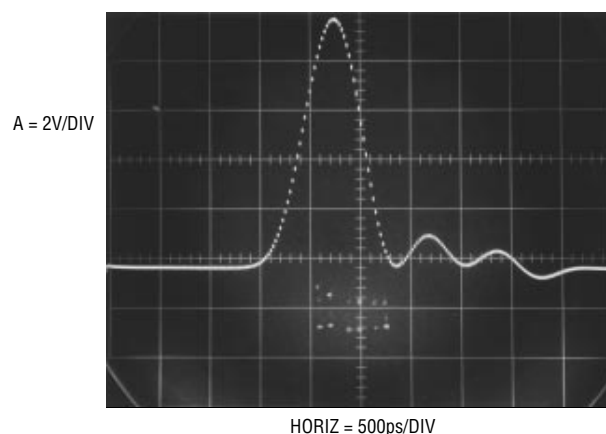
Note 1: The ability to generate such a pulse proves useful for a variety of tasks, including testing terminators, cables, probes and oscilloscopes for response. The requirements for this pulse generator are surprisingly convenient and inexpensive. For a discussion and construction details see Appendix D "Measuring Probe - Oscilloscope Response".

ground system. As previously discussed, BNC coaxial terminators are not simply resistors in a can. Special construction techniques insure optimum wideband response. Figures 29 and 30 demonstrate this nicely. In Figure 29 a 1ns pulse with 350ps rise and fall times¹ is monitored on a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in and P6032 probe). The waveform is clean, with only a slight hint of ring after the falling edge. This photo was taken with a high grade BNC coaxial type terminator in use. Figure 30 does not share these attributes. Here, the generator is terminated with a 50Ω carbon composition resistor with lead lengths of about 1/8 inch. The waveform rings and tails badly on turn-off before finally settling. Note that the sweep speed required a 2.5X reduction to capture these unwanted events.



LTAN47 • TA29

Figure 29. 350ps Rise and Fall Times are Preserved by a Good Quality Termination



LTAN47 • TA30

Figure 30. Poor Grade Termination Produces Pronounced Ringing and Tailing in the GHz Range

Application Note 47

Connectors, such as BNC barrel extensions and tee-type adaptors, are convenient and frequently employed. Remember that these devices represent a discontinuity in the cable, and can introduce small but undesirable effects. In general it is best to employ them as close as possible to a terminated point in the system. Use in the middle of a cable run provides minimal absorption of their mismatch and reflections. The worst offenders among connectors are adaptors. This is unfortunate, as these devices are necessitated by the lack of connection standardization in wideband instrumentation. The mismatch caused by a BNC-to-GR874 adaptor transition at the input of a wideband sampling 'scope is small, but clearly discernible in the display. Similarly, mismatches in almost all adaptors, and even in "identical" adaptors of different manufacture, are readily measured on a high-frequency network analyzer such as the Hewlett-Packard 4195A² (for additional wisdom and terror along these lines see Reference 1).

BNC connections are easily the most common, but not necessarily the most desirable, wideband connection mechanism. The ingenious GR874 connector has notably superior high frequency characteristics, as does the type N. Unfortunately, it's a BNC world out there.

About Probes and Probing Techniques

The choice of which oscilloscope probe to use in a measurement is absolutely crucial. The probe must be considered as an inherent part of the circuit under test. Rise time, bandwidth, resistive and capacitive loading, delay and other limitations must be kept in mind.

Sometimes, the best probe is no probe at all. In some circumstances it is possible and preferable to connect critical breadboard points *directly* to the oscilloscope (see Figure 31). This arrangement provides the highest possible grounding integrity, eliminates probe attenuation, and maintains bandwidth. In most cases this is mechanically inconvenient, and often the oscilloscope's electrical characteristics (particularly input capacitance) will not permit it. This is why oscilloscope probes were developed, and why so much effort has been put into their development (Reference 42 is excellent). In addition to the mate-

Note 2: Almost no one believes any of this until they see it for themselves. I didn't. Photos of the network analyzer's display aren't included in the text because no one would believe them. I wouldn't.

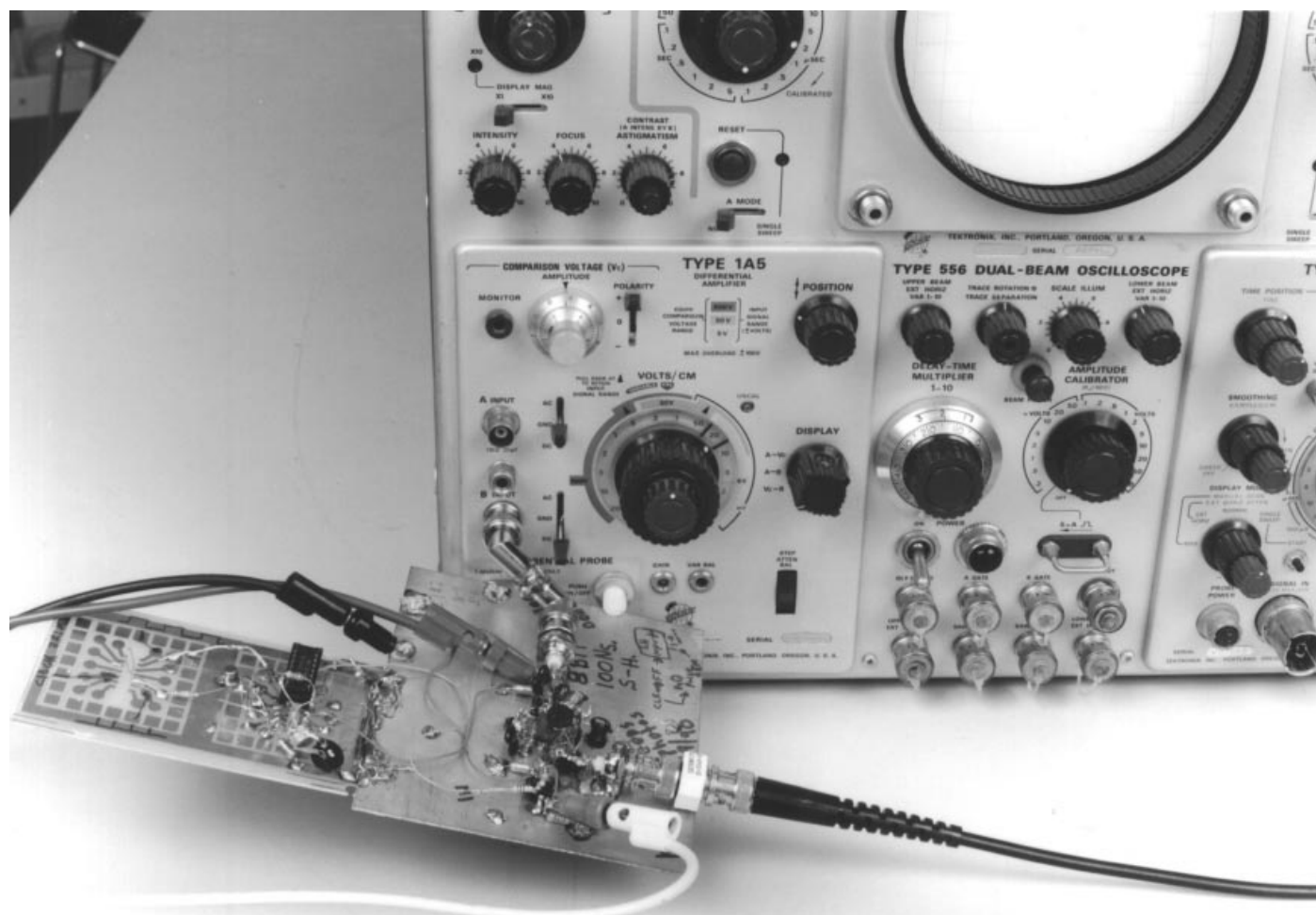
rial presented here, an in-depth treatment of probes appears in Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.

Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the point they are measuring. The most obvious is input resistance, but input capacitance usually dominates in a high speed measurement. Much time can be lost chasing circuit events which are actually due to improperly selected or applied probes. An 8pF probe looking at a 1k Ω source impedance forms an 8ns lag — substantially longer than a fast amplifier's delay time! Pay particular attention to the probe's input capacitance. Standard 10M Ω , 10X probes typically have 8pF-10pF of input capacitance, with 1X types being much higher. In general, 1X probes are not suitable for fast work because their bandwidth is limited to about 20MHz. Remember that all 10X probes cannot be used with all oscilloscopes; the probe's compensation range must match the oscilloscope's input capacitance. Low impedance probes (with 500 Ω to 1k Ω resistance), designed for 50 Ω inputs, usually have input capacitance of 1pF or 2pF. They are a very good choice if you can stand the low resistance. FET probes maintain high input resistance and keep capacitance at the 1pF level but have substantially more delay than passive probes. FET probes also have limitations on input common-mode range which must be adhered to or serious measurement errors will result. Contrary to popular belief, FET probes *do not* have extremely high input resistance — some types are as low as 100k Ω . It is possible to construct a wideband FET probe with very high input impedance, although input capacitance is somewhat higher than standard FET probes. For measurements requiring these characteristics, such a probe is useful. See Appendix E, "An Ultra Fast High Impedance Probe".

Regardless of which type probe is selected remember that they all have bandwidth and rise time restrictions. The displayed rise time on the oscilloscope is the vector sum of source, probe and 'scope rise times.

$$t_{RISE} = \sqrt{(t_{RISE} \text{ Source})^2 + (t_{RISE} \text{ Probe})^2 + (t_{RISE} \text{ Oscilloscope})^2}$$

This equation warns that some rise time degradation must occur in a cascaded system. In particular, if probe and oscilloscope are rated at the same rise time, the system response will be slower than either.



LTAN47 • TA31

Figure 31. Sometimes the Best Probe is No Probe. Direct Connection to the Oscilloscope Eliminates a 10X Probe's Attenuation and Possible Grounding Problems in a Sample-Hold (Figure 124) Settling Time Measurement

Current probes are useful and convenient.³ The passive transformer-based types are fast and have less delay than the Hall effect-based versions. The Hall types, however, respond at DC and low frequency and the transformer types typically roll off around 100Hz to 1kHz. Both types have saturation limitations which, when exceeded, cause odd results on the CRT which will confuse the unwary. The Tektronix type CT-1 current probe, although not nearly as versatile as the clip-on probes, bears mention. Although this is not a clip-on device, it may be the least electrically intrusive way of extracting wideband signal information. Rated at 1GHz bandwidth, it produces 5mV/mA output with only 0.6pF loading. Decay time constant of this AC current probe is $\approx 1\%/50\text{ns}$, resulting in a low frequency limit of 35kHz.

Note 3: A more thorough discussion of current probes is given in LTC Application Note 35, "Step Down Switching Regulators". See Reference 2.

A very special probe is the differential probe. A differential probe may be thought of as two matched FET probes contained within a common probe housing. This probe literally brings the advantage of a differential input oscilloscope to the circuit board. The probes matched, active circuitry provides greatly improved high frequency common mode rejection over single ended probing or even matched passive probes used with a differential amplifier. The resultant ability to reject common-mode signals and ground noise at high frequency allows this probe to deliver exceptionally clean results when monitoring small, fast signals. Figure 32 shows a differential probe being used to verify the waveshape of a 2.5mV input to a wideband, high gain amplifier (Figure 76 of the Applications section).

When using different probes, remember that they all have different delay times, meaning that apparent timing errors

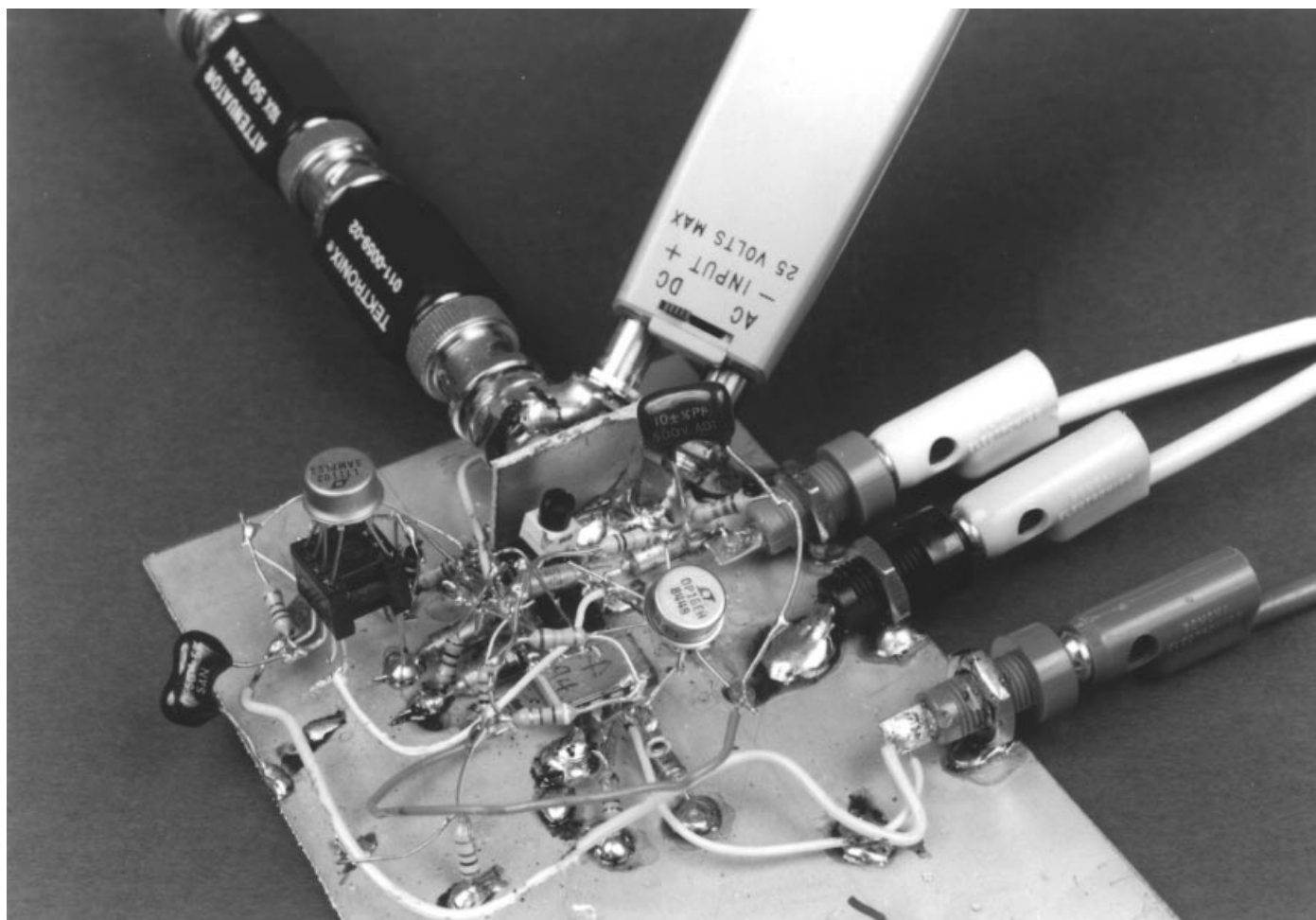
Application Note 47

will occur on the CRT. Know what the individual probe delays are and account for them in interpreting the CRT display.

By far the greatest source of error in probe use is grounding. Poor probe grounding can cause ripples and discontinuities in the waveform observed. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is due to parasitic inductance in the probe's ground connection. In most oscilloscope measurements this is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in making the lowest possible inductive connection to ground. Most of these attachments

assume a ground plane is in use, which it should be. Always try to make the shortest possible connection to ground – anything longer than 1 inch may cause trouble. Sometimes it's difficult to determine if probe grounding is the cause of observed waveform aberrations. One good test is to disturb the grounding set-up and see if changes occur. Nominally, touching the ground plane or jiggling probe ground connectors or wires should have no effect. If a ground strap wire is in use try changing its orientation or simply squeezing it together to change and minimize its loop area. *If any waveform change occurs while doing this the probe grounding is unacceptable, rendering the oscilloscope display unreliable.*

The simple network of Figure 33 shows just how easy it is for poorly chosen or used probes to cause bad results. A 9pF input capacitance probe with a 4 inch long ground



LTAN47 • TA32

Figure 32. Using a Differential Probe to Verify the Integrity of a 2.5mV High Speed Input Pulse (Figure 76's X1000 Amplifier)

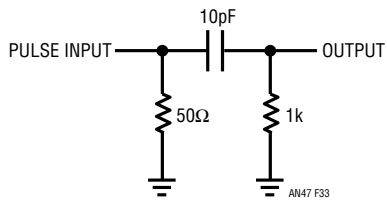
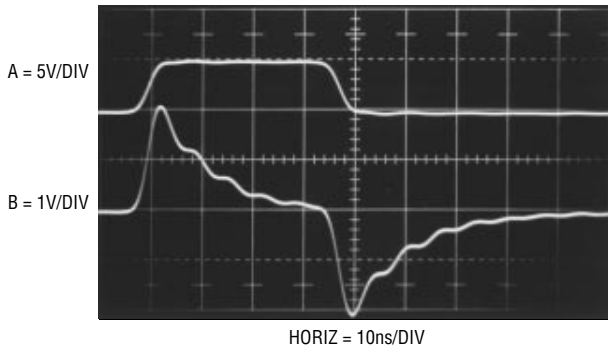
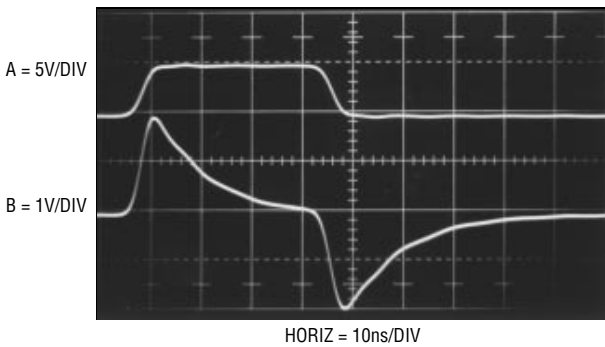


Figure 33. Probe Test Circuit



LTAN47 • TA34

Figure 34. Test Circuit Output with 9pF Probe and 4 Inch Ground Strap



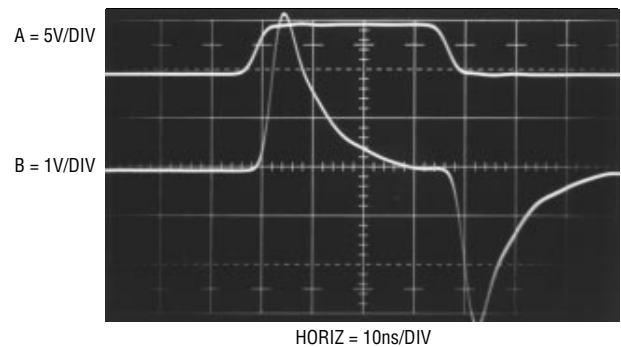
LTAN47 • TA35

Figure 35. Test Circuit Output with 9pF Probe and 0.25 Inch Ground Strap

strap monitors the output (Trace B, Figure 34). Although the input (Trace A) is clean, the output contains ringing. Using the same probe with a 1/4 inch spring tip ground connection accessory seemingly cleans up everything (Figure 35). However, substituting a 1pf FET probe (Figure 36) reveals a 50% output amplitude error in Figure 35! The FET probe's low input capacitance allows a more accurate version of circuit action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5ns due to delay in its active circuitry. Hence, separate measurements with each probe are required to determine the output's amplitude and timing parameters.

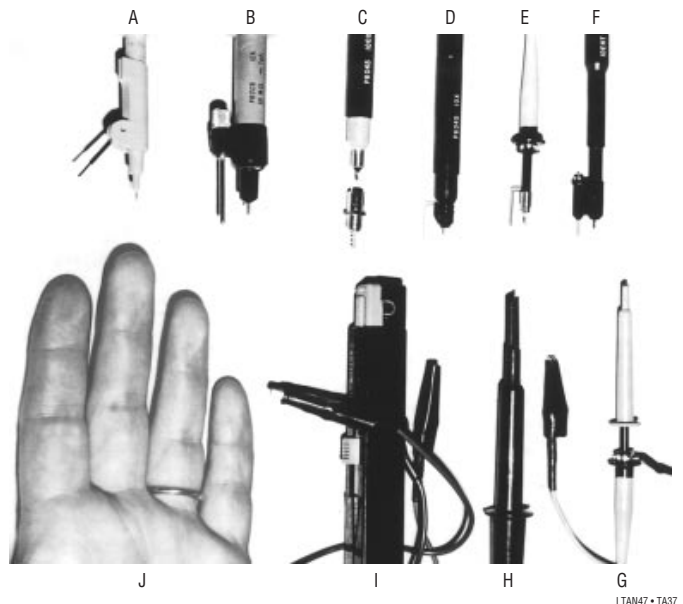
A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can be used to introduce stray capacitance to a suspected circuit node while observing results on the CRT. Two fingers, lightly moistened, can be used to provide an experimental resistance path. Some high speed engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

Examples of some of the probes discussed, along with different forms of grounding implements, are shown in Figure 37. Probes A, B, E, and F are standard types equipped with various forms of low impedance grounding attachments. The conventional ground lead used on G is more convenient to work with but will cause ringing and



LTAN47 • TA36

Figure 36. Test Circuit Output with FET Probe



LTAN47 • TA37

Figure 37. Various Probe-Ground Strap Configurations

Application Note 47

other effects at high frequencies, rendering it useless. H has a very short ground lead. This is better, but can still cause trouble at high speeds. D is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. C is a separated FET probe attenuator head. Such heads allow the probe to be used at higher voltage levels (e.g., $\pm 10\text{V}$ or $\pm 100\text{V}$). The miniature coaxial connector shown can be mounted on the circuit board and the probe mated with it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended. I is a current probe. A ground connection is not usually required. However, at high speeds the ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible. J is typical of the finger probes described in the text. Note the ground strap on the third finger.

The low inductance ground connectors shown are available from probe manufacturers and are always supplied with good quality, high frequency probes. Because most oscilloscope measurements do not require them, they invariably become lost. There is no substitute for these devices when they are needed, so it is prudent to take care of them. This is especially applicable to the ground strap on the finger probe.

About Oscilloscopes

The modern oscilloscope is one of the most remarkable instruments ever constructed. The protracted and intense development effort put toward these machines is perhaps equaled only by the fanaticism devoted to timekeeping.⁴ It is a tribute to oscilloscope designers that instruments manufactured over 25 years ago still suffice for over 90% of today's measurements. The oscilloscope-probe combination used in high speed work is the most important equipment decision the designer must make. Ideally, the oscilloscope should have at least 150MHz bandwidth, but

Note 4: In particular, the marine chronometer received ferocious and abundant amounts of attention. See References 4, 5, and 6. For an enjoyable stroll through the history of oscilloscope vertical amplifiers, see Reference 3. See also Reference 41.

Note 5: See Appendix D, "Measuring Probe - Oscilloscope Response", for complete details on this pulse generator.

Note 6: This sequence of photos was shot in my home lab. I'm sorry, but 1GHz is the fastest 'scope in my house.

slower instruments are acceptable if their limitations are well understood. Be certain of the characteristics of the probe-oscilloscope combination. Rise time, bandwidth, resistive and capacitive loading, delay, noise, channel-to-channel feedthrough, overdrive recovery, sweep nonlinearity, triggering, accuracy and other limitations must be kept in mind. High speed linear circuitry demands a great deal from test equipment and countless hours can be saved if the characteristics of the instruments used are well known. Obscene amounts of time have been lost pursuing "circuit problems" which in reality are caused by misunderstood, misapplied or out-of-spec equipment. Intimate familiarity with your oscilloscope is invaluable in getting the best possible results with it. In fact, it is possible to use seemingly inadequate equipment to get good results if the equipment's limitations are well known and respected. All of the circuits in the Applications section involve rise times and delays well above the 100MHz-200MHz region, but 90% of the development work was done with a 50MHz oscilloscope. Familiarity with equipment and thoughtful measurement technique permit useful measurements seemingly beyond instrument specifications. A 50MHz oscilloscope cannot track a 5ns rise time pulse, but it can measure a 2ns delay between two such events. Using such techniques, it is often possible to deduce the desired information. There are situations where no amount of cleverness will work and the right equipment (e.g., a faster oscilloscope) must be used. Sometimes, "sanity-checking" a limited bandwidth instrument with a higher bandwidth oscilloscope is all that is required. For high speed work, brute force bandwidth is indispensable when needed, and no amount of features or computational sophistication will substitute. Most high speed circuitry does not require more than two traces to get where you are going. Versatility and many channels are desirable, but if the budget is limited, spend for bandwidth!

Dramatic differences in displayed results are produced by probe-oscilloscope combinations of varying bandwidths. Figure 38 shows the output of a very fast pulse⁵ monitored with a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in). At this bandwidth the 10V amplitude appears clean, with just a small hint of ringing after the falling edge. The rise and fall times of 350ps are suspicious, as the sampling oscilloscope's rise time is also specified at 350ps.⁶

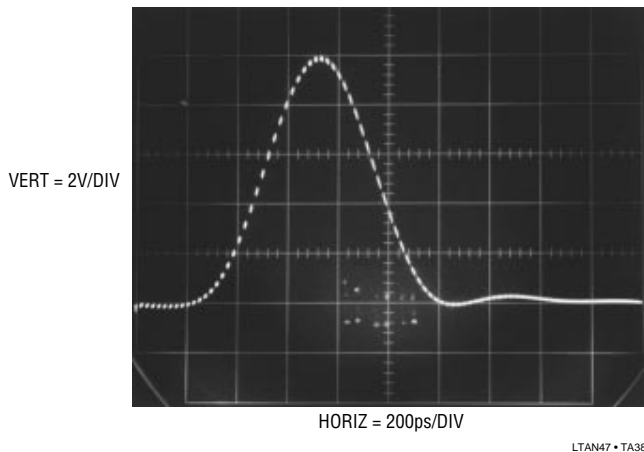


Figure 38. A 350ps Rise/Fall Time 10V Pulse Monitored on 1GHz Sampling Oscilloscope. Direct 50Ω Input Connection is Used

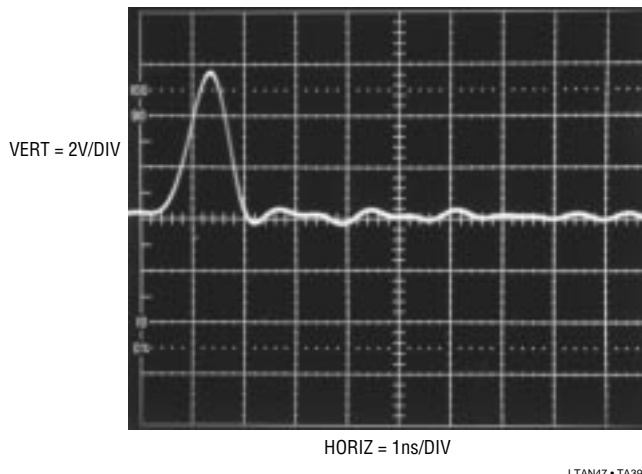


Figure 39. The Test Pulse Appears Smaller and Slower On a 350MHz Instrument ($t_{RISE} = 1ns$). Deliberate Poor Grounding Creates Rippling After the Pulse Falls. Direct 50Ω Connection is Used

Figure 39 shows the same pulse observed on a 350MHz instrument with a direct connection to the input (Tektronix 485/50Ω input). Indicated rise time balloons to 1ns, while displayed amplitude shrinks to 6V, reflecting this instrument's lesser bandwidth. To underscore earlier discussion, poor grounding technique (1 1/2" of ground lead to the ground plane) created the prolonged rippling after the pulse fall.

Figure 40 shows the same 350MHz (50Ω input) oscilloscope with a 3GHz 10X probe (Tektronix P6056). Displayed results are nearly identical, as the probe's high bandwidth contributes no degradation. Again, deliberate poor grounding causes overshoot and rippling on the pulse fall.

Figure 41 equips the same oscilloscope with a 10X probe specified at 290MHz bandwidth (Tektronix P6047). Additionally, the oscilloscope has been switched to its 1MΩ input mode, reducing bandwidth to a specified 250MHz. Amplitude degrades to less than 4V and edge times similarly increase. The deliberate poor grounding contributes the undershoot and underdamped recovery on pulse fall.

In Figure 42 a 100MHz 10X probe (Hewlett-Packard Model 10040A) has been substituted for the 290MHz unit. The oscilloscope and its set-up remain the same. Amplitude shrinks below 2V, with commensurate rise and fall times. Cleaned up grounding eliminates aberrations.

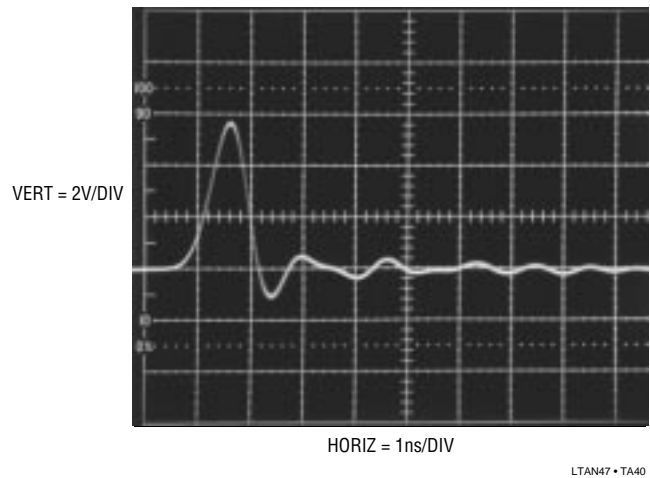


Figure 40. Test Pulse on the Same 350MHz Oscilloscope Using a 3GHz 10X Probe. Deliberate Poor Grounding Maintains Rippling Residue

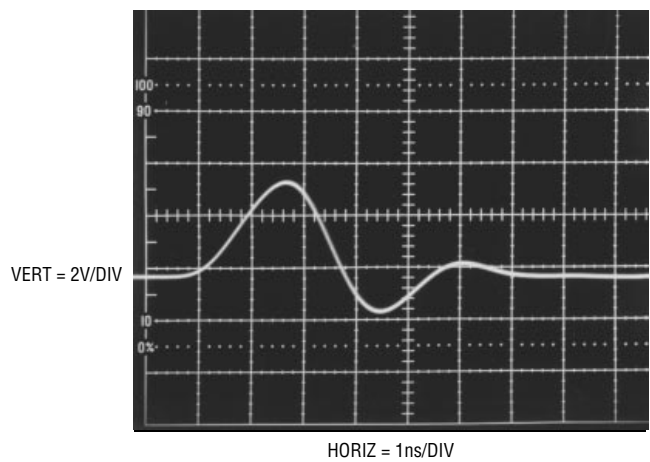


Figure 41. Test Pulse Measures Only 3V High on a 250MHz 'Scope with Significant Waveform Distortion. 250MHz 10X Probe Used

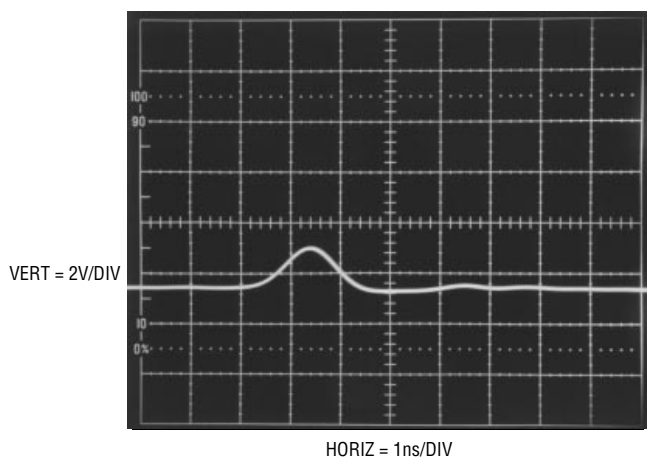


Figure 42. Test Pulse Measures Under 2V High Using 250MHz 'Scope and a 100MHz Probe

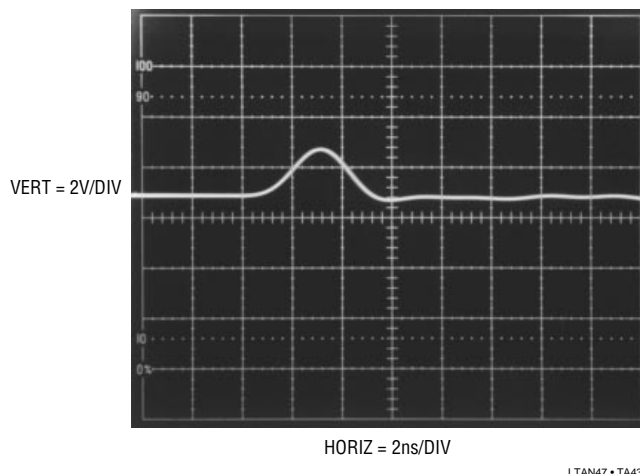


Figure 43. 150MHz Oscilloscope ($t_{RISE} = 2.4ns$) with Direct Connection Responds to the Test Pulse

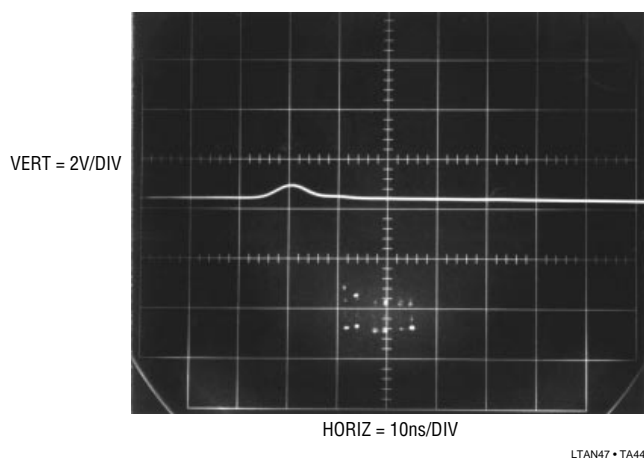


Figure 44. A 50MHz Instrument Barely Grunts. 10V, 350ps Test Pulse Measures Only 0.5V High with 7ns Rise and Fall Times!

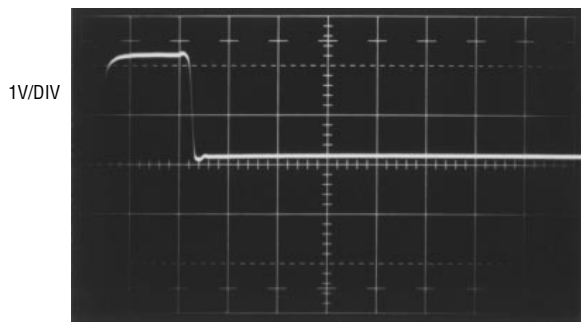
A Tektronix 454A (150MHz) produced Figure 43's trace. The pulse generator was directly connected to the input. Displayed amplitude is about 2V, with appropriate 2ns edges. Finally, a 50MHz instrument (Tektronix 556 with 1A4 plug-in) just barely grunts in response to the pulse (Figure 44). Indicated amplitude is 0.5V, with edges reading about 7ns. That's a long way from the 10V and 350ps that's really there!

A final oscilloscope characteristic is overload performance. It is often desirable to view a small amplitude portion of a large waveform. In many cases the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overload before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude, and other considerations. Oscilloscope response to overload varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100X overload at 0.005V/division may be very different than at 0.1V/division. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overload must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

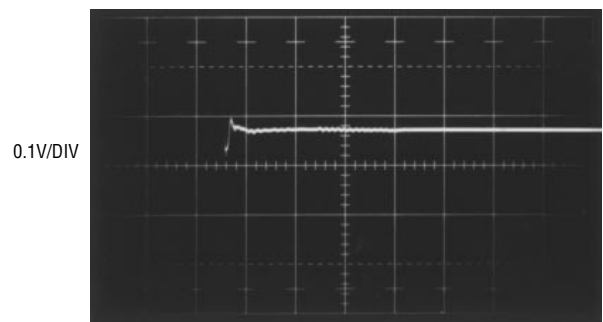
The waveform to be expanded is placed on the screen at a vertical sensitivity which eliminates all off-screen activity. Figure 45 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure 46) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure 47, gain has been further increased and all the features of Figure 46 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure 48 brings some unpleasant surprises. This increase in gain

causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure 47. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure 49 the gain remains the same, but the vertical position knob has

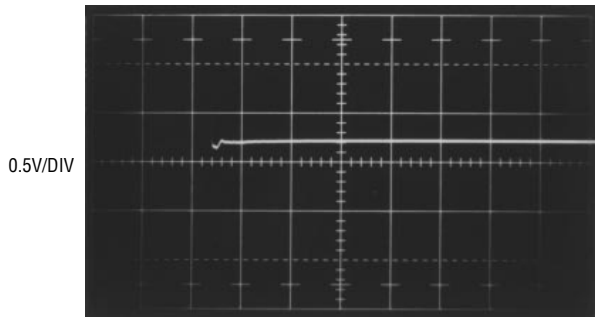
been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure 50). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.



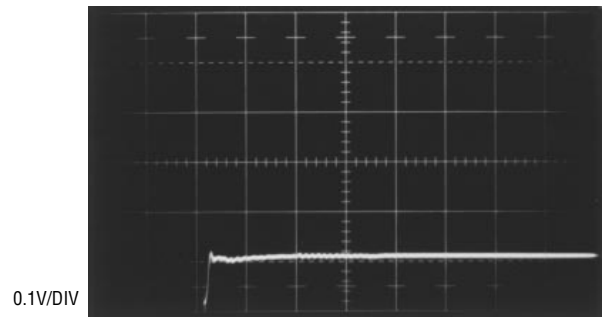
100ns/DIV
Figure 45 LTAN47 • TA45



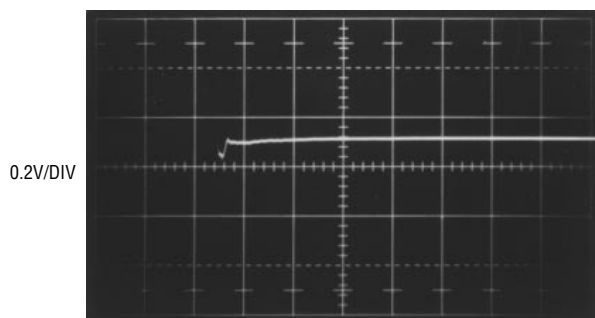
0.1V/DIV
100ns/DIV
Figure 48 LTAN47 • TA48



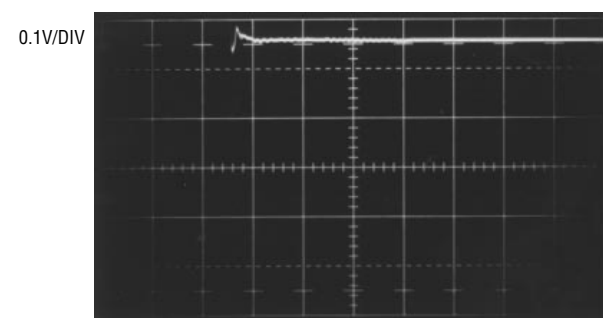
100ns/DIV
Figure 46 LTAN47 • TA46



0.1V/DIV
100ns/DIV
Figure 49 LTAN47 • TA49



100ns/DIV
Figure 47 LTAN47 • TA47



0.1V/DIV
100ns/DIV
Figure 50 LTAN47 • TA50

Figures 45-50. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

Application Note 47

Differential plug-ins can address some of the issues associated with excessive overdrive, although they cannot solve all problems. Two differential plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7, 1A7A and 7A22 feature $10\mu\text{V}$ sensitivity, although bandwidth is limited to 1MHz. The units also have selectable high and low pass filters and good high frequency common-mode rejection. Tektronix type 1A5, W and 7A13 are differential comparators. They have calibrated DC nulling (slideback) sources, allowing observation of small, slowly moving events on top of common-mode DC or fast events riding on a waveform.

A special case is the sampling oscilloscope. By nature of its operation, a sampling 'scope in proper working order is inherently immune to input overload, providing essentially instantaneous recovery between samples. Appendix B, "Measuring Amplifier Settling Time", utilizes this capability. See Reference 8 for additional details.

The best approach to measuring small portions of large waveforms, however, is to eliminate the large signal swing seen by the oscilloscope. Appendix B, "Measuring Amplifier Settling Time" shows ways to do this when measuring DAC-amplifier settling time to very high accuracy at high speed.

In summary, while the oscilloscope provides remarkable capability, its limitations must be well understood when interpreting results.⁷

About Ground Planes

Many times in high frequency circuit layout, the term "ground plane" is used, most often as a mystical and ill-defined cure to spurious circuit operation. In fact, there is little mystery to the usefulness and operation of ground planes, and like many phenomena, their fundamental operating principle is surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus,

Note 7: Additional discourse on oscilloscopes will be found in References 1 and 7 through 11.

we can visualize a wire carrying current (Figure 51) surrounded by radii of magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the wire's current. To compute the wire's inductance requires integrating the field over the wire's length and the total radial area of the field. This implies integrating on the radius from $R = R_W$ to infinity, a very large number. However, consider the case where we have two wires in space carrying the same current in either direction (Figure 52). The fields produced cancel.

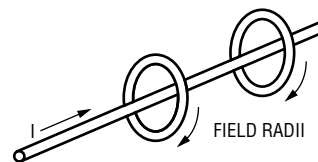


Figure 51. Single Wire Case

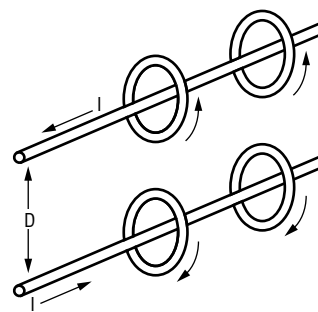


Figure 52. Two Wire Case

In this case, the inductance is much smaller than in the simple wire case and can be made arbitrarily smaller by reducing the distance between the two wires. This reduction of inductance between current carrying conductors is the underlying reason for ground planes. In a normal circuit, the current path from the signal source through its conductor and back to ground includes a large loop area. This produces a large inductance for this conductor which can cause ringing due to LRC effects. It is worth noting that 10nH at 100MHz has an impedance of 6Ω . At 10mA a 60mV drop results.

A ground plane provides a return path directly under the signal carrying conductor through which return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents will always flow through the return path of lowest impedance. In a properly designed

ground plane, this path is directly under the signal conductor. In a practical circuit, it is desirable to ground plane one whole side of the PC card (usually the component side for wave solder considerations) and run the signal conductors on the other side. This will give a low inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to AC skin effect (AC currents travel along a conductor's surface). Additionally, they aid the circuit's high frequency stability by referring stray capacitances to ground.

Some practical hints for ground planes are:

1. Ground plane as much area as possible on the component side of the board, especially under traces that operate at high frequency.
2. Mount components that conduct substantial fast rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
3. Where common ground potential is important (i.e., at comparator inputs), try to single point the critical components into the ground plane to avoid voltage drops.

For example, in Figure 53's common A/D circuit, good practice would dictate that grounds 2, 3, 4 and 6 be as close to single point as possible. Fast, large currents must flow through R1, R2, D1 and D2 during the DAC settle time. Therefore, D1, D2, R1 and R2 should be mounted close to the ground plane to minimize their inductance. R3 and C1 don't carry any current, so their inductance is less important; they could be vertically

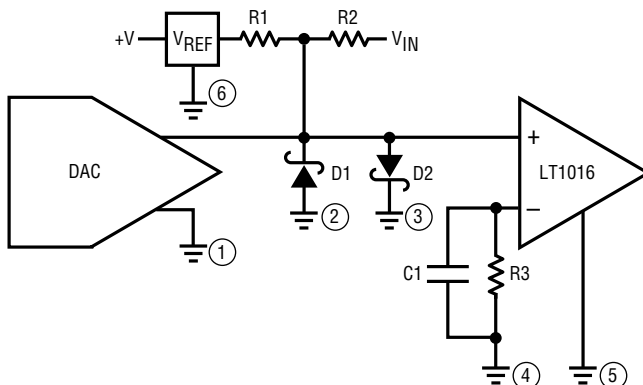


Figure 53. Typical Grounding Scheme

inserted to save space and to allow point 4 to be single point common with 2, 3 and 6. In critical circuits, the designer must often trade off the beneficial effects of lowered inductance versus the loss of single point ground.

4. Keep trace length short. Inductance varies directly with length and no ground plane will achieve perfect cancellation.

About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure 54. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values so they can absorb long transients, necessitating electrolytic types which have large series R and L.

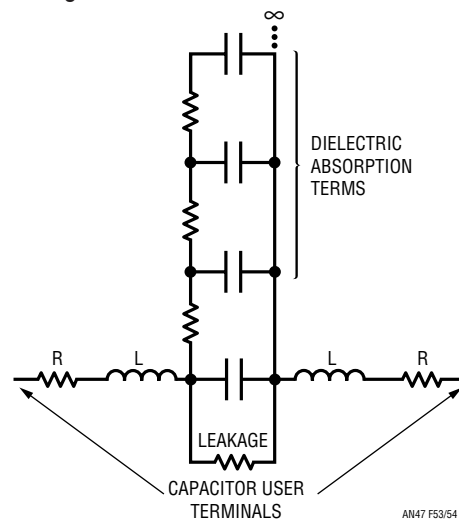


Figure 54. Parasitic Terms of a Capacitor

Application Note 47

Different types of electrolytics and electrolytic-non-polar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure 55) and accompanying photos are useful. The photos show the response of 5 bypassing methods to the transient generated by the test circuit. Figure 56 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure 57 uses an aluminum $10\mu\text{F}$ electrolytic to considerably cut the disturbance, but there is still plenty of potential trouble. A tantalum $10\mu\text{F}$ unit offers cleaner response in Figure 58 and the $10\mu\text{F}$ aluminum combined with a $0.01\mu\text{F}$ ceramic type is even better in Figure 59. Combining electrolytics with non-polarized capacitors is a popular way to get good response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in Figure 60. Caveat!

Breadboarding Techniques

The breadboard is both the designer's playground and proving ground. It is there that Reality resides, and paper (or computer) designs meet their ruler. More than anything else, breadboarding is an iterative procedure, an odd amalgam of experience guiding an innocent, ignorant,

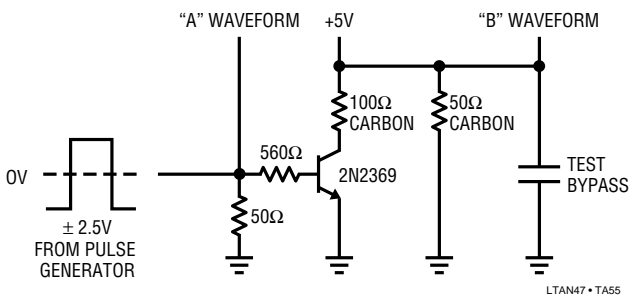


Figure 55. Bypass Capacitor Test Circuit

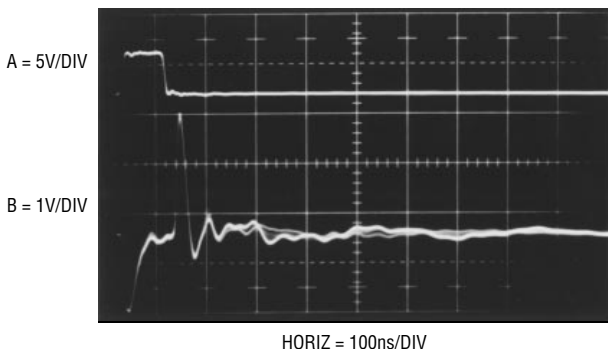


Figure 56. Response of Unbypassed Line

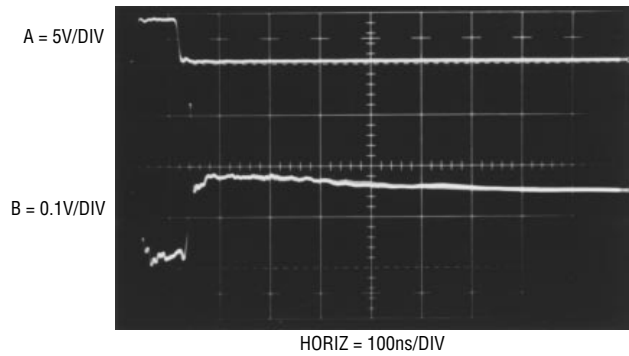


Figure 57. Response of $10\mu\text{F}$ Aluminum Capacitor

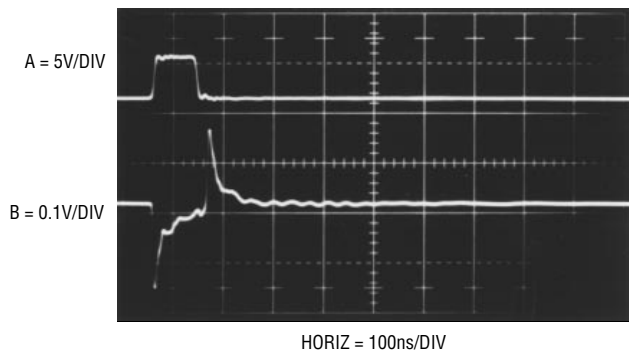


Figure 58. Response of $10\mu\text{F}$ Tantalum Capacitor

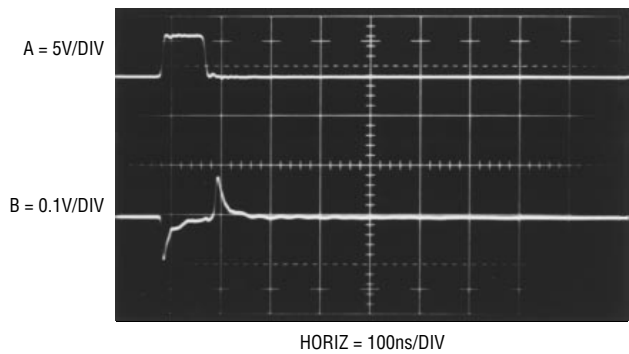


Figure 59. Response of $10\mu\text{F}$ Aluminum Paralleled by $0.01\mu\text{F}$ Ceramic

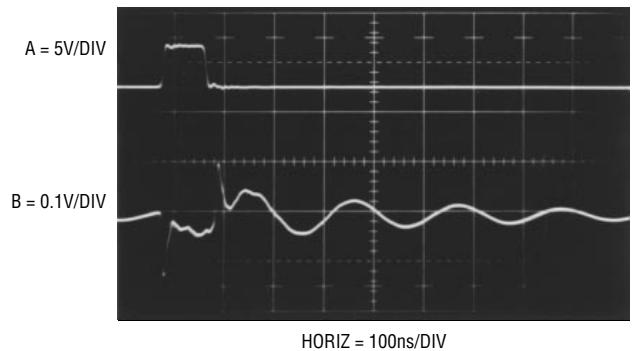


Figure 60. Some Paralleled Combinations can Ring. Try before Specifying!

explorative spirit. A key is to be willing to try things out, sometimes for not very good reasons. Invent problems and solutions, guess carefully and wildly, throw rocks and see what comes loose. Invent and design experiments, and follow them wherever they lead. Reticence to try things is probably the number one cause of breadboards that “don’t work”.⁸ Implementing the above approach to life begins with the physical construction methods used to build the breadboard.

A high speed breadboard must start with a ground plane. Additionally, bypassing, component layout and connections should be consistent with high speed operations. Because of these considerations there is a common misconception that breadboarding high speed circuits is time consuming and difficult. This is simply not true. For high speed circuits of moderate complexity a complete and electrically correct breadboard can be assembled in 10 minutes if all necessary components are on hand. The key to rapid breadboarding is to identify critical circuit nodes and design the layout to suit them. This permits most of the breadboard’s construction to be fairly sloppy, saving time and effort. Additionally, use all degrees of freedom in making connections and mounting components. Don’t be bashful about bending I.C. pins to suit desired low capacitance connections, or air wiring components to achieve rapid or electrically optimum layout. Save time by using components, such as bypass capacitors, as mechanical

supports for other components, such as amplifiers. It is true that eventual printed circuit construction is required, but when initially breadboarding forget about PC and production constraints. Later, when the circuit works, and is well understood, PC adaptations can be taken care of.

Figure 61’s amplifier circuit is a good working example. This circuit, excerpted from the Applications section (where its electrical operation is more fully explained) is a high impedance, wideband amplifier with low input capacitance. Q1 and A1 form the high frequency path, with the 900Ω-100Ω feedback divider setting gain. A2 and Q2 close a DC stabilization loop, minimizing DC offset between the circuit’s input and output. Critical nodes in this circuit include Q1’s gate (because of the desired low input capacitance) and A1’s input related connections (because of their high speed operation). Note that the connections associated with A2 serve at DC and are much less sensitive to layout. These determinations dominate the breadboard’s construction.

Figure 62 shows initial breadboard construction. The copper clad board is equipped with banana type connectors. The connector’s mounting nuts are simply soldered to the clad board, securing the connectors. Figure 63 adds A1 and the bypass capacitors. Observe that A1’s leads have been bent out, permitting the amplifier to sit down on the ground plane, minimizing parasitic capacitance. Also, the bypass capacitors are soldered to the amplifier power pins right at the capacitor’s body. The capacitor’s lead lengths are returned to the banana power jacks. This connection method provides good amplifier bypassing

Note 8: A much more eloquently stated version of this approach is found in Reference 12.

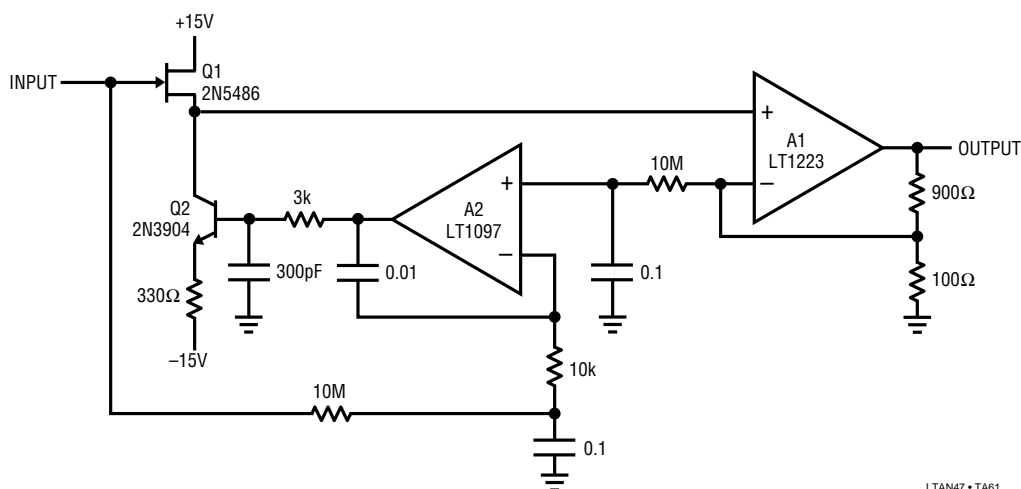


Figure 61. The Stabilized FET Input Amplifier (Applications Figure 73) to be Breadboarded

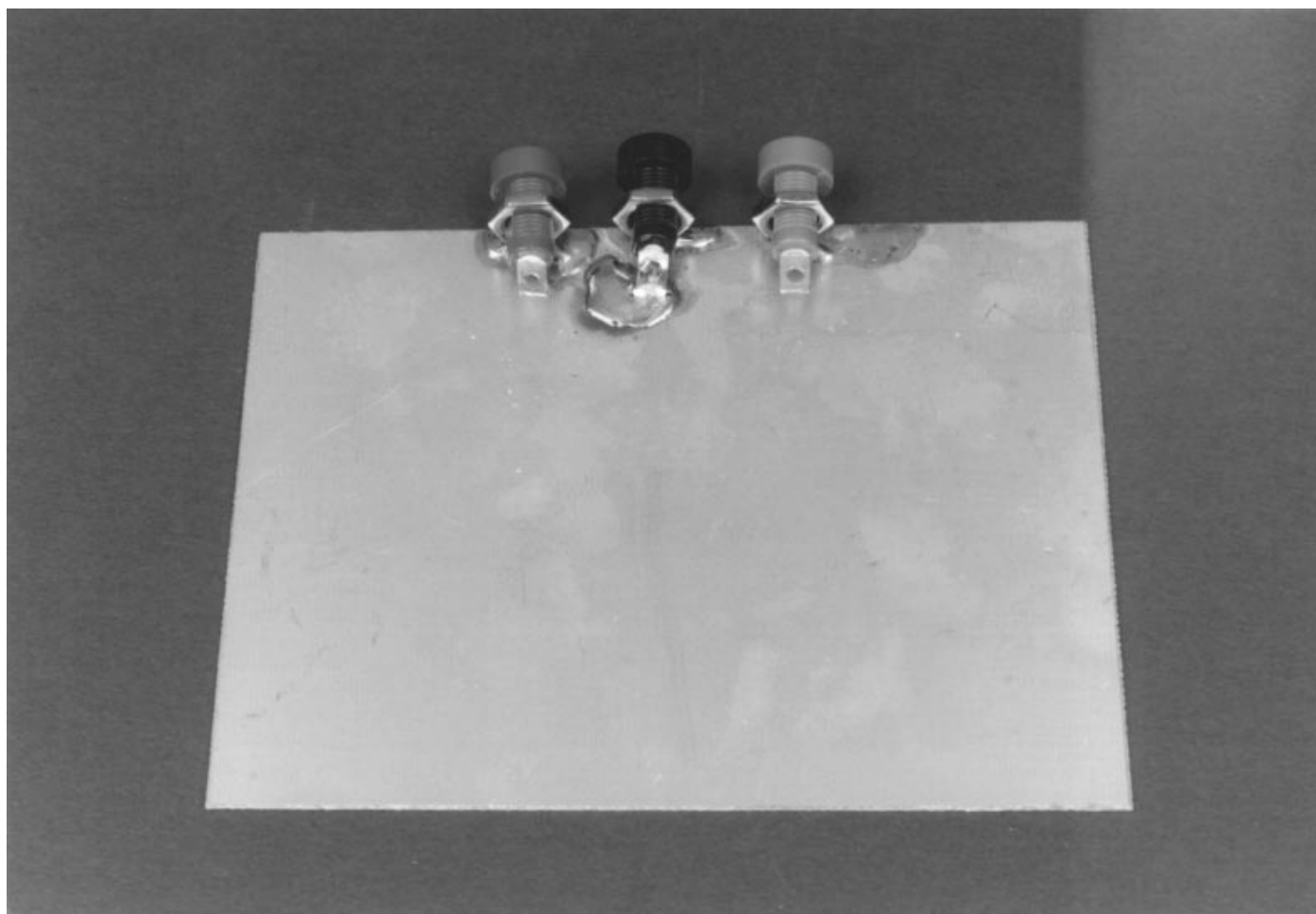


Figure 62. The Banana Jacks are Soldered to the Copper Clad Board

LTAN47 • TA62

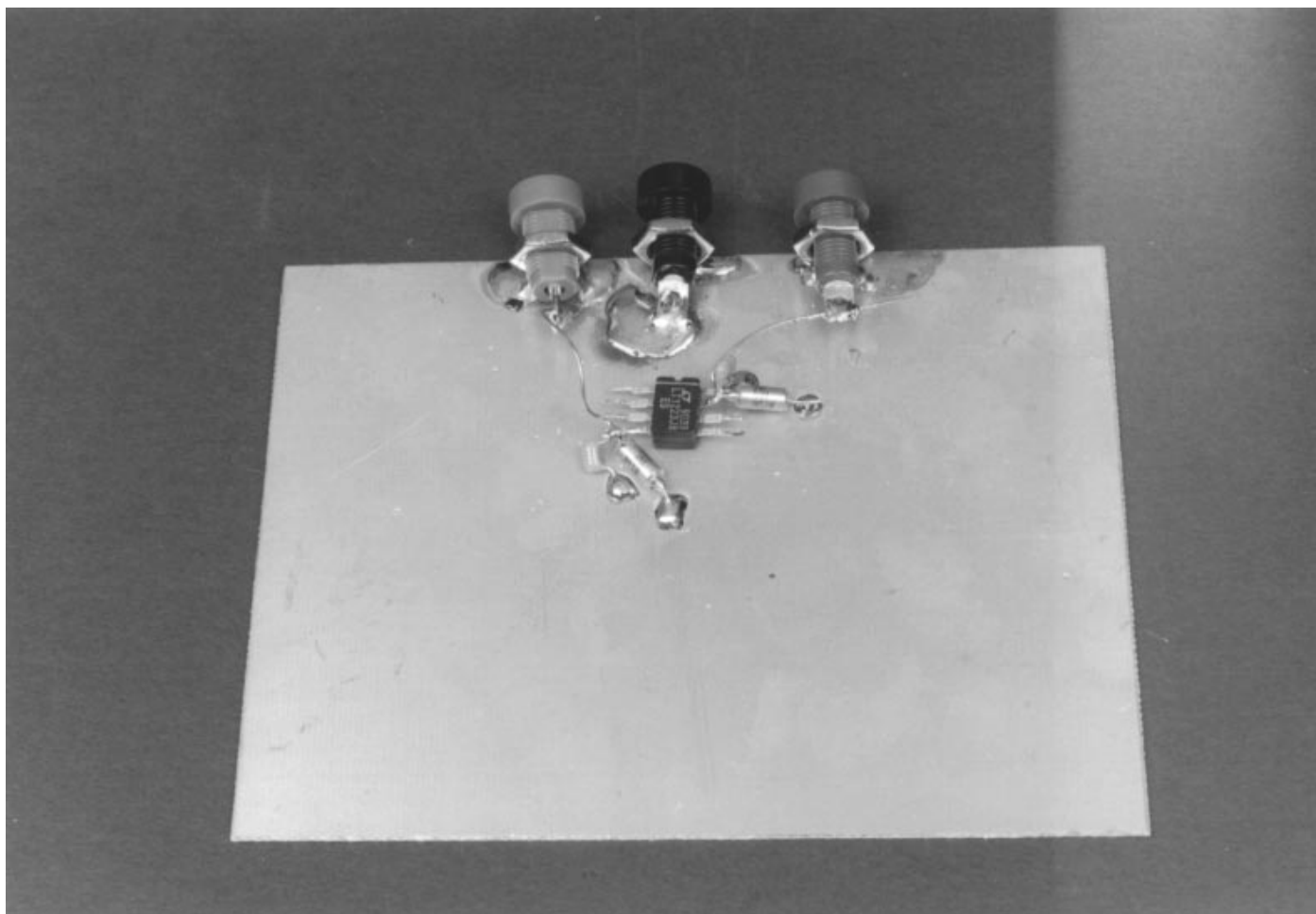
while mechanically supporting the amplifier. It also eliminates separate wire runs to the power pins.

Figure 64 adds the discrete components in the high speed path. Q1's gate is connected directly to the input BNC, as is the $10\text{M}\Omega$ resistor associated with A2's negative input. Note that the end of this resistor that sees high frequency is cut very short, while the other end is left uncut. The 900Ω - 100Ω divider is installed at A1, with very short connections to A1's negative input. A1's $10\text{M}\Omega$ resistor receives similar treatment to the BNC connected $10\text{M}\Omega$ unit; the high frequency end is cut short, while the end destined for connection to A2 remains uncut. Q2's collector and Q1's source, high speed points, are tied closely together with A1's positive input.

Finally, DC amplifier A2 and its associated components are air wired into the breadboard (Figure 65). Their DC opera-

tion permits this, while the construction technique makes connections to the previously wired nodes easy. The previously uncommitted ends of the $10\text{M}\Omega$ resistors may be bent in any way necessary to make connections. All other components associated with A2 receive similar treatment and the circuit is ready for experimentation.

Despite the breadboard's seemingly haphazard construction, the circuit worked well. Input capacitance measured a few pF (including BNC connector) with bias current of about 100pA . Slew rate was $1000\text{V}/\mu\text{s}$, with bandwidth approaching 100MHz . Output, even with 50mA loading, was clean, with no sign of oscillation or other instabilities. Full details on this circuit appear in the Applications section. Additional examples of breadboard construction techniques appear in Appendix F, "Additional Comments on Breadboarding".



LTAN47 • TA63

Figure 63. High Speed Amplifier A1 is Connected to Power. Bypass Capacitors Provide Support. Bending Amplifier Pins Eases Connections and Minimizes Distance to the Ground Plane

Once the breadboard seems to work, it's useful to begin thinking about PC layout and component choice for production. Experiment with the existing layout to determine just how sensitive nominally critical points are. Add controlled parasitic terms (e.g., resistors, capacitors and physical layout changes) to test for sensitivity. Gentle touching of suspect points with a finger can yield preliminary indication of sensitivity, giving clues that can be quite valuable.

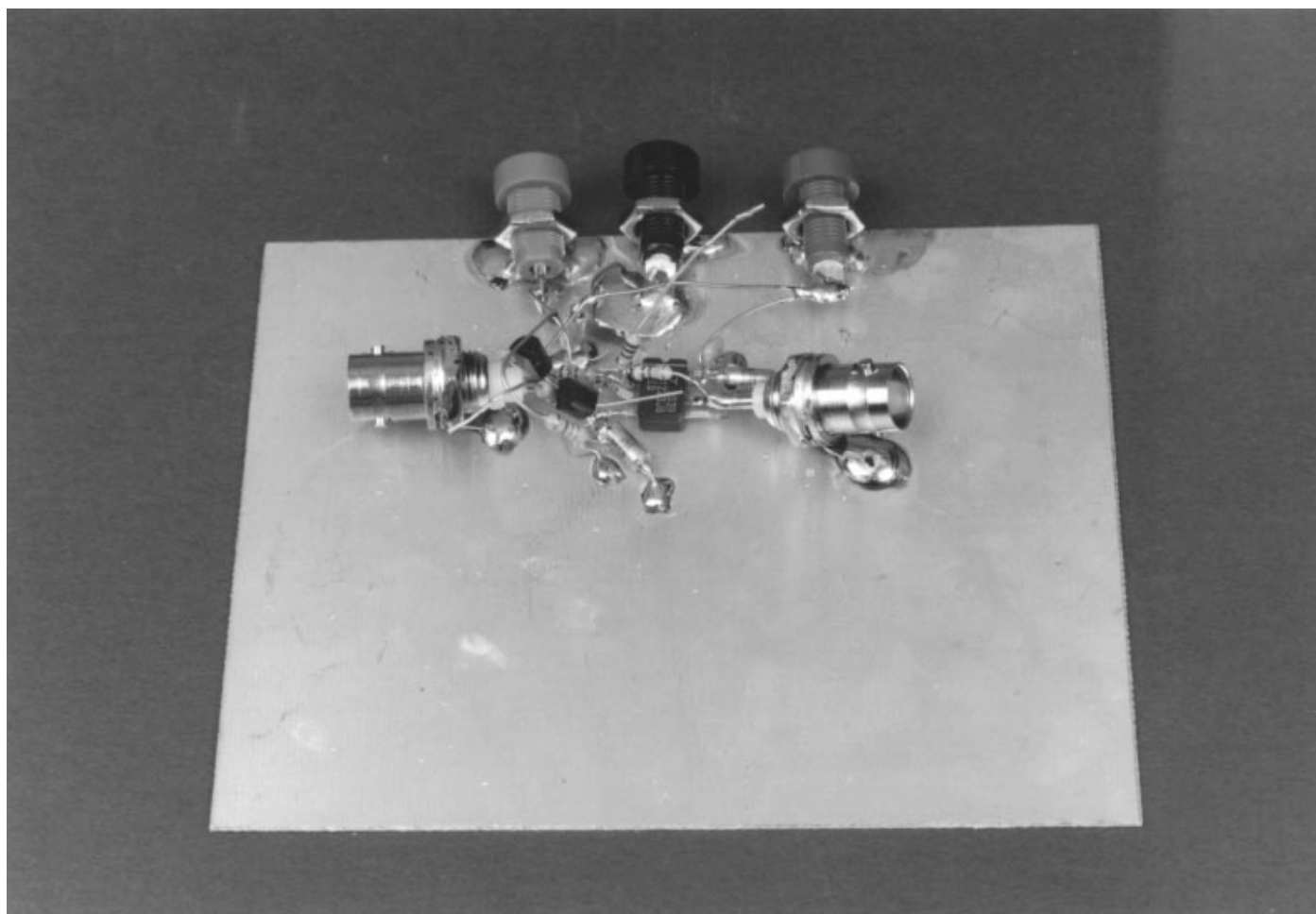
In conclusion, when breadboarding, design the breadboard to be quick and easy to build, work with and modify. Observe the circuit and listen to what it is telling you before trying to get it to some desired state. Finally, don't hesitate to try just about anything; that's what the breadboard is for. Almost anything you do will cause some result —

whether it's good or bad is almost irrelevant. Anything you do that enhances your ability to correlate events occurring on the breadboard can only be beneficial.

Oscillation

The forte of the operational amplifier is negative feedback. It is feedback which stabilizes the operating point and fixes the gain. However, positive feedback or delayed negative feedback can cause oscillation. Thus, a properly functioning amplifier constantly lives in the shadow of oscillation.

When oscillation occurs, several major candidates for blame are present. Power supply impedance must be low. If the supply is unbypassed, the impedance the amplifier sees at its power terminals is high, particularly at high



LTAN47 • TA64

Figure 64. Additional High Speed Discrete Components and Connectors are Added. Note Short Connections at Amplifier Input Pins (Left Side of Package). 10M Resistors Uncommitted Ends are Just Visible

frequency. This impedance forms a voltage divider with the amplifier, allowing the supply to move as internal conditions in the amplifier change. This can cause local feedback and oscillation occurs. The obvious cure is to bypass the amplifier.

A second common cause of oscillation is positive feedback. In most amplifier circuits feedback is negative, although controlled amounts of positive feedback may be used. In a circuit that nominally has only negative feedback unintended positive feedback may occur with poor layout. Check for possible parasitic feedback paths and unwanted or overlooked feedback action. Always minimize (to the extent possible) impedances seen by amplifier inputs. This helps attenuate the effects of parasitic feedback paths to the inputs. Similarly, minimize exposed input trace area. Route amplifier outputs and other signals well away from

sensitive nodes. Sometimes no amount of layout finesse will work and shielding is required. Use shielding only when required — extensive shielding is a sloppy substitute for good layout practice.

A final cause of oscillation is negative feedback arriving well delayed in time. Under these conditions the amplifier hopelessly tries to servo a feedback signal which consistently arrives too late. The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point. The most common causes of this problem are reactive loading of the amplifier (most notably capacitive loads such as cable) and circuitry, such as power amplifiers, placed within the amplifier's feedback path. Reactive loads should be isolated from the amplifier's output (and feedback path) with a resistor or power amplifier. Sometimes rolling off the amplifier's frequency

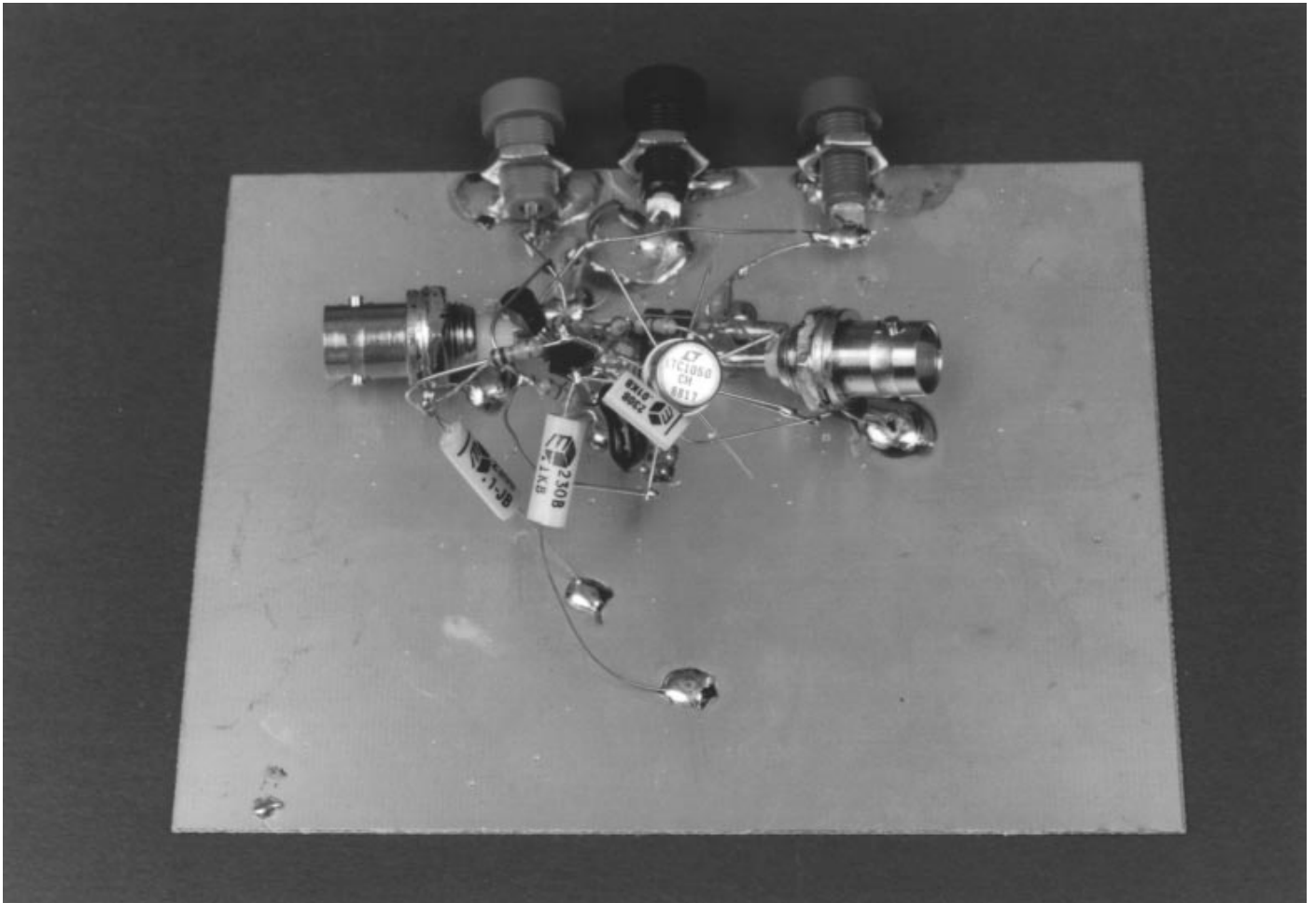


Figure 65. DC Servo Amplifier is Wired In and Connections to 10M Resistors Completed. This Part of the Circuit is Not Layout Sensitive

LTAN47 • TA65

response will fix the problem, but in high speed circuits this may not be an option.

Placing power gain or other type stages within the amplifier's feedback path adds time delay to the stabilizing feedback. If the delay is significant, oscillation commences. Stages operating within the amplifier's loop must contribute minimum time lag compared to the amplifier's speed capability. At lower speeds this is not too difficult, but something destined for operation within a 100MHz amplifier's loop must be *fast*. As mentioned before, rolling off the amplifier's frequency response eases the job, but is usually undesirable in a wideband circuit. Every effort should be expended to maximize the added stages bandwidth before resorting to roll-off of the amplifier. In this way the fastest overall bandwidth is achieved while maintaining stability. Appendix C, "The Oscillation Problem –

Frequency Compensation Without Tears", discusses considerations surrounding operating power gain and other type stages within amplifier loops.

This completes the tutorial section. Hopefully, several notions have been imparted. First, in any measurement situation, test equipment characteristics are an integral part of the circuit. At high speed and high precision this is particularly the case. As such, it is imperative to know your equipment and how it works. There is no substitute for intimate familiarity with your tool's capabilities and limitations.⁹

In general, use equipment you trust and measurement techniques you understand. Keep asking questions and

Note 9: Further exposition and *kvetching* on this point is given in Reference 13.

Application Note 47

don't be satisfied until everything you see on the oscilloscope is accounted for and makes sense.

Fast monolithic amplifiers, combined with the precautionary notes listed above, permit fast linear circuit functions which are difficult or impractical using other approaches. Some of the applications presented represent the state-of-the-art for a particular circuit function. Others show simplified and/or improved ways to implement standard functions by utilizing the amplifier's easily accessed speed. All have been carefully (and painfully) worked out and should serve as good idea sources for potential users of the device. Have fun. I did.

APPLICATIONS SECTION I - AMPLIFIERS

Fast 12-Bit Digital-to-Analog Converter (DAC) Amplifier

One of the most common applications for a high speed amplifier, transforming a 12-bit DAC's current output into a voltage, is also one of the most difficult. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns or less, but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, in the 100pF-150pF range, and it varies with code. Bipolar DACs typically have 20pF-30pF of capacitance, stable over all codes. As such, bipolar DACs are almost always used where high speed is required. Figure 66 shows the popular AD565A 12-bit DAC with an LT1220 output op amp. Figure 67 shows clean 0.01% settling in 280ns (Trace B) to an all-bits-on input step (Trace A). The requirements for obtaining Trace B's display are not trivial, and are fully detailed in Appendix B, "Measuring Amplifier Settling Time".

2-Channel Video Amplifier

Figure 68 shows a simple way to multiplex two video amplifiers onto a single 75Ω cable. The appropriate ampli-

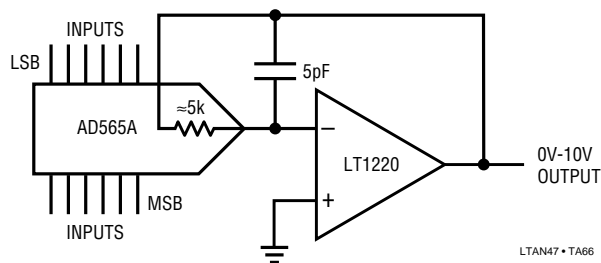


Figure 66. Typical Output Amplifier Configuration for a 12-Bit D-to-A Converter

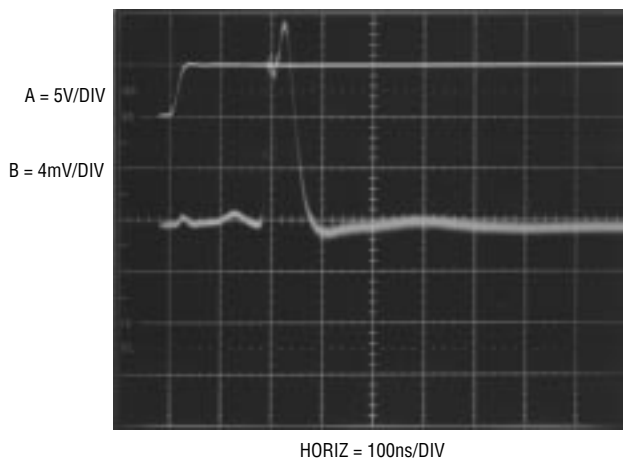


Figure 67. Settling Residue (Trace B) for All Bits Switched On (Trace A). Output is Fully Settled in 280ns

fier is activated in accordance with the truth table in the figure¹⁰. Amplifier performance includes 0.02% differential gain error and 0.1° differential phase error. The 75Ω back termination looking into the cable means the amplifiers must swing 2Vp-p to produce 1Vp-p at the cable output, but this is easily handled.

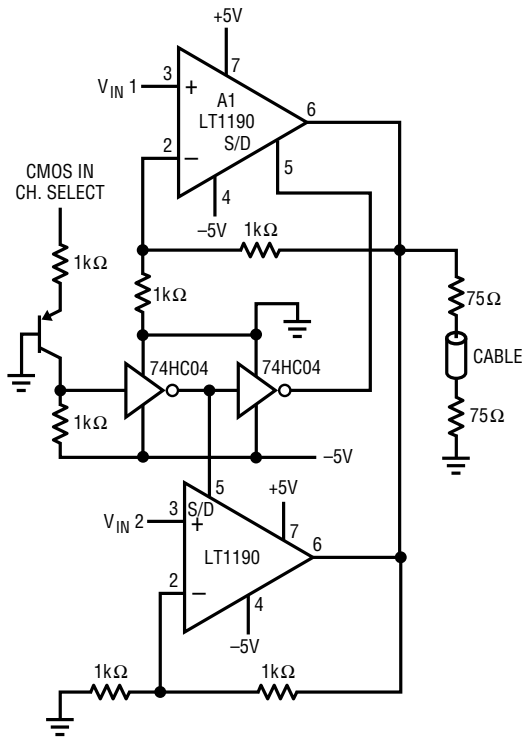
Simple Video Amplifier

Figure 69 is a simpler version of Figure 68. This is a single channel video amplifier, arranged (in this case) for a gain of ten. The double cable termination is retained and the circuit delivers a bandwidth of 55MHz.

Loop Through Cable Receivers

Figure 70 is another cable related circuit. Here, the LT1193 differential amplifier simply hangs across a distribution cable, extracting the signal. The amplifier's true differential inputs reject common-mode signals. As in the previous

Note 10: A truth table in an op amp circuit! Et tu, LTC!!



TRUTH TABLE

INPUT SELECT	A1 OUTPUT	A2 OUTPUT
5V	ACTIVE	INACTIVE
0V	INACTIVE	ACTIVE

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Figure 68. 2-Channel Multiplexed Video Amplifier

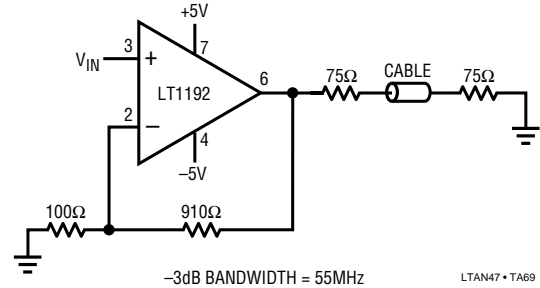
circuit, differential gain and phase errors measure 0.2% and 0.1°, respectively. A separate input permits DC level adjustment.

DC Stabilization – Summing Point Technique

Often it is desirable to obtain the precision offset of a DC amplifier with the bandwidth of a fast device. There are a variety of techniques for doing this. Which method is best is heavily application dependent, so several configurations are presented.

Figure 71 shows a composite made up of an LT1097 low drift device and an LT1191 high speed amplifier. The overall circuit is a unity gain inverter with the summing node located at the junction of the two 1k resistors. The LT1097 monitors this summing node, compares it to ground and drives the LT1191's positive input, completing a DC stabilizing loop around the LT1191. The 100kΩ-0.01μF time constant at the LT1097 limits its response to

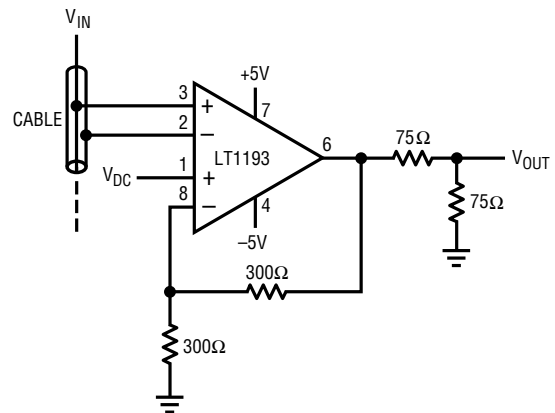
low frequency signals. The LT1191 handles high frequency inputs while the LT1097 stabilizes the DC operating point. The 4.7k-220Ω divider at the LT1191 prevents excessive input overdrive during start-up. This circuit combines the LT1097's 35μV offset and 1.5V/°C drift with the LT1191's 450V/μs slew rate and 90MHz bandwidth. Bias current, dominated by the LT1191, is about 500nA.



-3dB BANDWIDTH = 55MHz

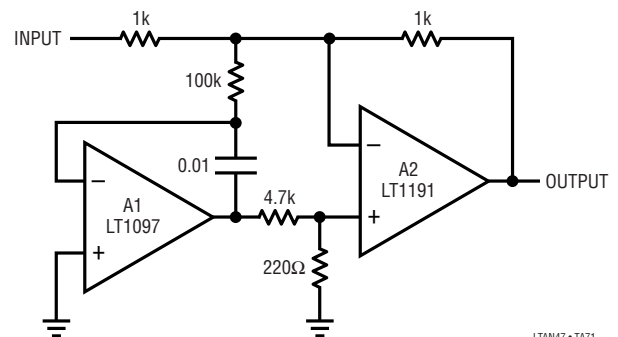
LTAN47 • TA69

Figure 69. Double Terminated Cable Driver



LTAN47 • TA70

Figure 70. Cable Sense Amplifier for Loop Through Connections with DC Adjust



LTAN47 • TA71

Figure 71. A1 DC Stabilizes A2 by Forcing the Summing Point to Zero

Application Note 47

DC Stabilization – Differentially Sensed Technique

Figure 72 is similar to Figure 71, except that the sensing is done differentially, preserving access to both fast amplifier inputs. The LT1097 measures the DC error at the LT1220's input terminals and biases its offset pins to force offset within $50\mu\text{V}$. The offset pin biasing at the LT1220 is arranged so the LT1097 will always be able to find the servo point. The $0.01\mu\text{F}$ capacitor rolls off the LT1097 at low frequency and the LT1220 handles high frequency signals. The combined characteristics of these amplifiers yield the following performance:

- Offset Voltage $50\mu\text{V}$
- Offset Drift $1\mu\text{V}/^\circ\text{C}$
- Slew Rate $250\text{V}/\mu\text{s}$
- Gain-Bandwidth 45MHz

DC Stabilization – Servo Controlled FET Input Stage

Figure 73 shows a wideband, highly stable gain-of-ten with high input impedance. Input capacitance is about 3pF . Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1223 provides a 100MHz bandwidth gain of ten. Normally, this open loop configuration would be quite drifty because there is no DC feedback. The LT1097 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly

filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction.

This circuit constitutes an extremely wideband (Q1 does not degrade A2's 100MHz performance), high input impedance amplifier. With an input capacitance of 3pF and

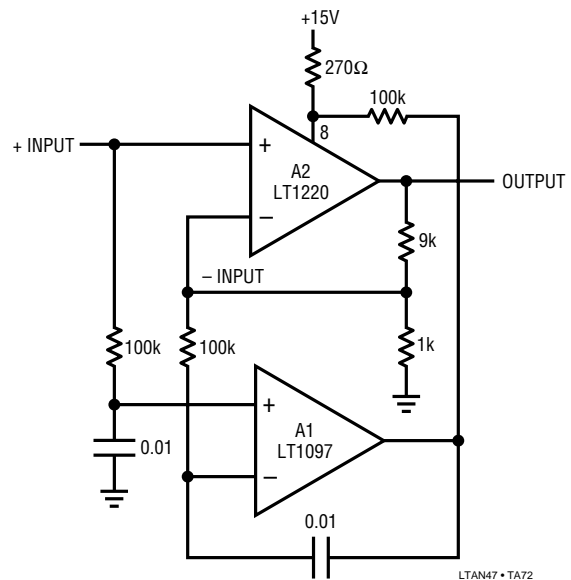


Figure 72. A1 DC Stabilizes A2 by Forcing the Offset Pins to Produce a 0V Difference at A2's Inputs

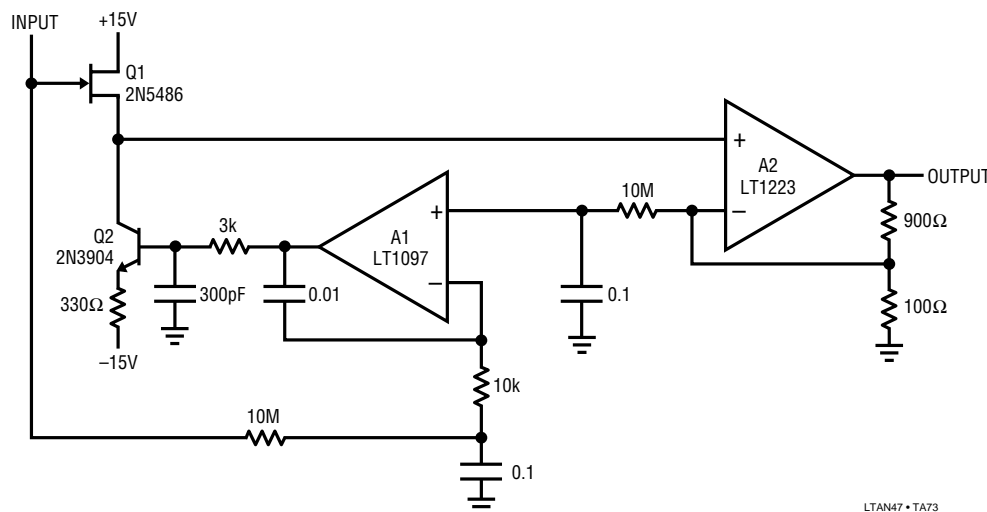


Figure 73. A1 DC Stabilizes the Circuit by Controlling Q1's Channel Current

bias current of 100pA, it is well suited for probing or as an ATE pin amplifier. As shown, gain is ten, but other gains are possible by varying the feedback ratio.

DC Stabilization – Full Differential Inputs with Parallel Paths

Figure 74 shows a way to get full differential inputs with DC stabilized operation. This circuit combines the output of two differential input amplifiers for overall DC corrected wideband operation. A1 and A2 both differentially sense the input at gains of ten. Wideband A1 feeds output amplifier A3 via a highpass network, while the slower A2 contributes DC and low frequency information to A3. A2 does not see high frequency inputs, because they are filtered by the 2k-200pF lowpass networks at its inputs. If the gain and bandwidth of the high and low frequency paths complement each other, A3's output should be an undistorted, amplified version (in this case $\times 10$) of the input. Figure 75 shows this to be the case. Trace A is one side of a differential input applied to the circuit. Trace B is A1's output taken at the 500 Ω potentiometer - 0.001 μ F junction. Trace C is A2's output. With the AC gain and DC gain match trims properly adjusted, the two paths' contributions match up and Trace D is singularly clean, with no residue. The adjustments are optimized by trimming the AC gain for the squarest corners and the DC gain match for a flat top. Bandwidth for this circuit exceeds 35MHz, slew rate is 450V/ μ s and DC offset about 200 μ V.

Note 11: For assistance in following circuit signal flow, the schematic of this device is included in the figure.

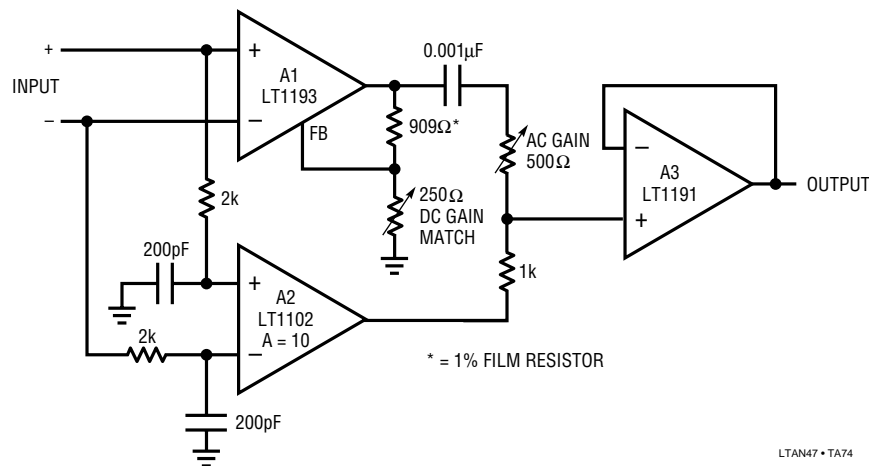


Figure 74. A Parallel Path DC Stabilized Differential Amplifier. High Frequency Signals Go through A1, while A2 Handles DC and Low Frequency. A3 Sums Both Paths

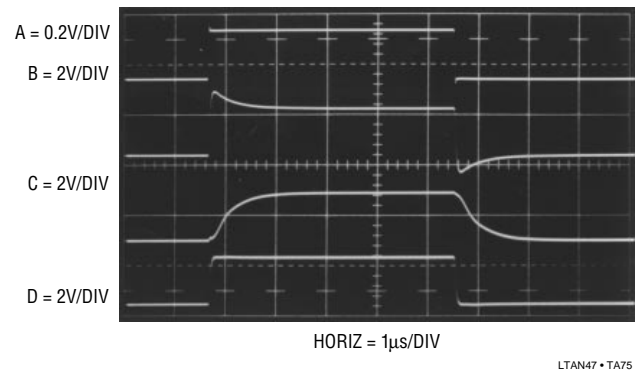


Figure 75. Waveforms for the Parallel Path Differential Amplifier. Trace A is the Input; B, C and D are the High Pass, Low Pass and Output Nodes, Respectively

DC Stabilization – Full Differential Inputs, Gain-of-1000 with Parallel Paths

Figure 76 is a very powerful extension of the previous circuit. Operation is similar, but gain is increased to 1000. Bandwidth is about 35MHz, rise time equals 7ns and delay is inside 7.5ns. Full power response is available to 10MHz, with input noise about 15 μ V broadband. This kind of speed, coupled with full differential inputs, the gain of 1000, DC stability, and low cost make the circuit broadly applicable in wideband instrumentation. As before, two differential amplifiers, A1 and A2, simultaneously sense the inputs. In this case A1 is the popular and economical 592-733 type, operating at a gain of 100.¹¹ A1's differential outputs feed output amplifier A3 via 1 μ F-1k Ω high pass networks which strip off A1's DC content. A2, a precision DC differential type, operates in similar fashion to the previous circuit, supplying DC and low frequency

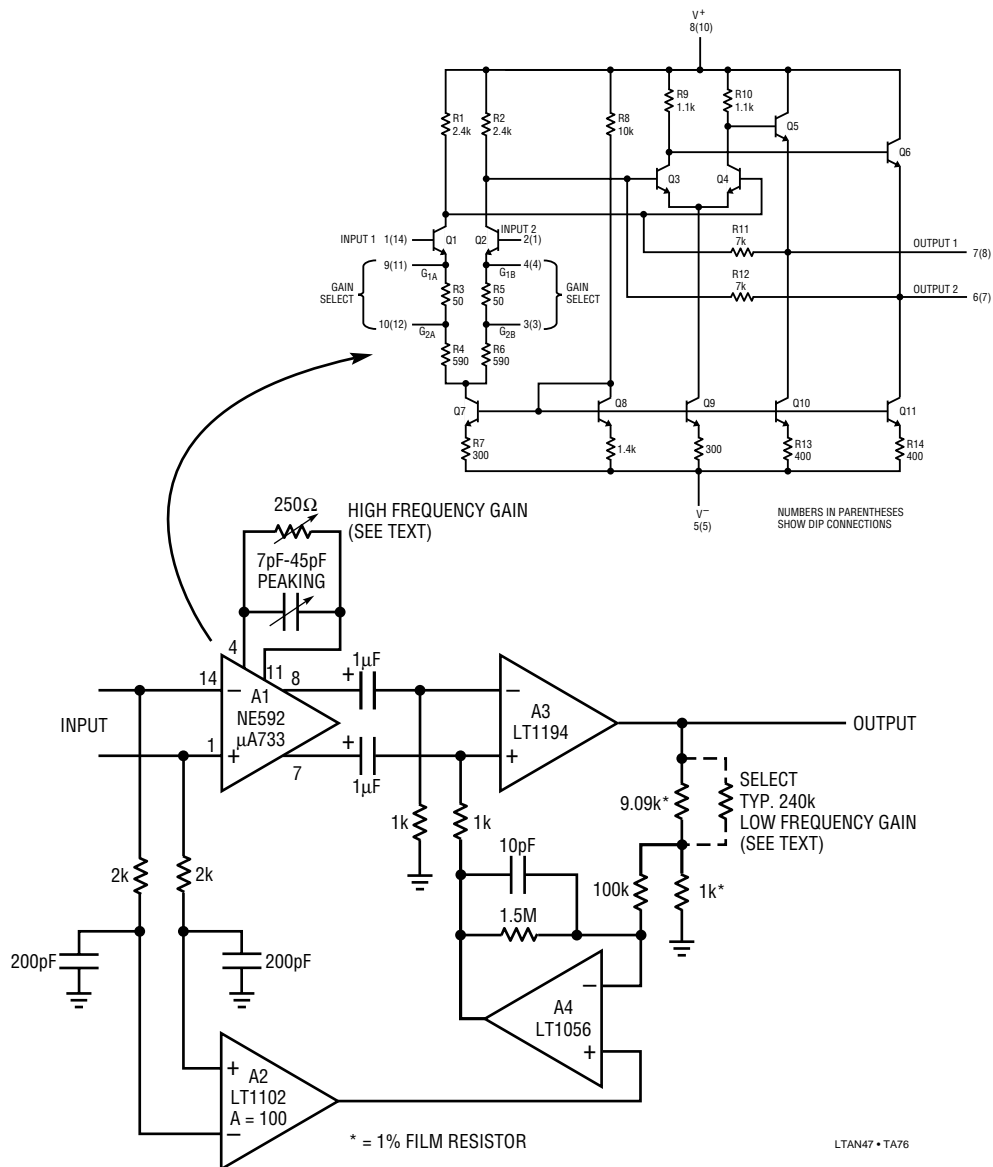


Figure 76. A Full Differential, Parallel Path Amplifier. Gain is 1000, with 38MHz Bandwidth. Delay is Inside 7.5ns and Rise Time Under 7ns

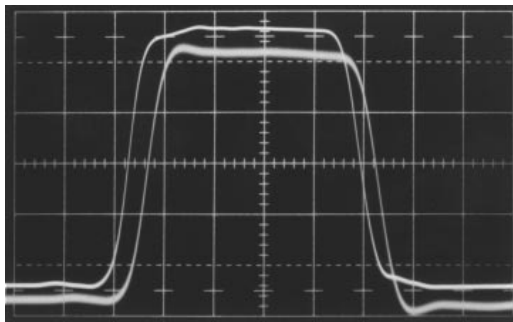
information to A3 at a trimmed gain of 100. In this case output amplifier A3 is a differential gain block with a nominal committed gain of 10. This change is necessitated by A1's differential output, which must be single-ended to obtain the circuit's output. As such A2 does not directly apply its low frequency information to A3 as it did before. Instead, A4 measures the difference between A2's output and a divided down portion of A3's output. A4's output, biasing A3's positive input via the 1kΩ resistor, closes a loop around the circuit's DC-low frequency path. The divider feeding A4's negative input is adjusted so that the circuit's DC gain is known and equal to its AC gain.

Figure 77 shows the circuit's response to a 60ns, 2.5mV amplitude pulse (Trace A). The X1000 output (Trace B) responds cleanly, with delay and rise time in the 5ns-7ns range. Some small amount of peaking is evident, although it may be trimmed with the peaking adjustment at A1. Figure 78 plots the circuit's gain vs frequency. Gain is flat within 1/2dB to 20MHz, with the -3dB point at 38MHz. Figure 77's edge peaking shows up here as a very slight gain increase starting around 1MHz and continuing out to about 15MHz. The peaking trim will eliminate this effect.

To use this circuit, put in a low frequency or DC signal of known amplitude and adjust the low frequency gain for a

X1000 output after the output has settled. Next, adjust the high frequency gain so that the signal's front and rear corners have amplitudes identical to the settled portion. Finally, trim the peaking adjustment for best settling of the output pulse's front and rear corners.

Figure 79 shows input (Trace A) and output (Trace B) waveforms with all adjustments properly set. Fidelity is excellent, with no aberrations or other artifacts of the parallel path operation evident. Figure 80 shows the effects of too much AC gain; excessive peaking on the edges with proper amplitude indicated only after the AC channel transitions through its highpass cut off. Similarly, excessive DC gain produces Figure 81's traces. The AC gain path



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Figure 77. Pulse Response for the X1000 Differential Amplifier. Fidelity is Quite Good, with Only Slight Output Peaking (Trace B)

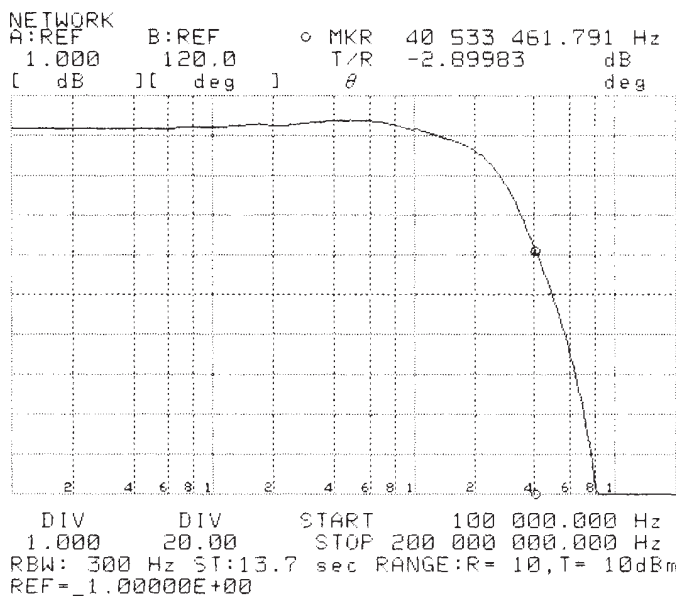
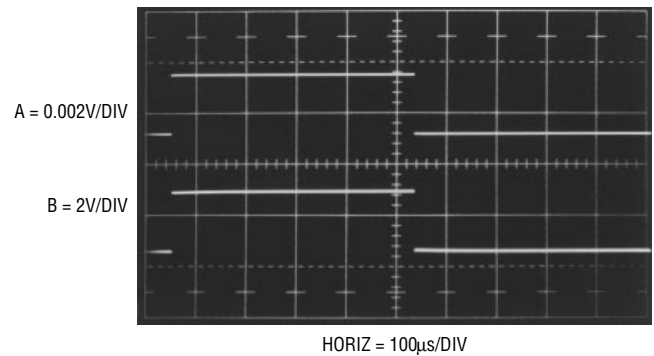
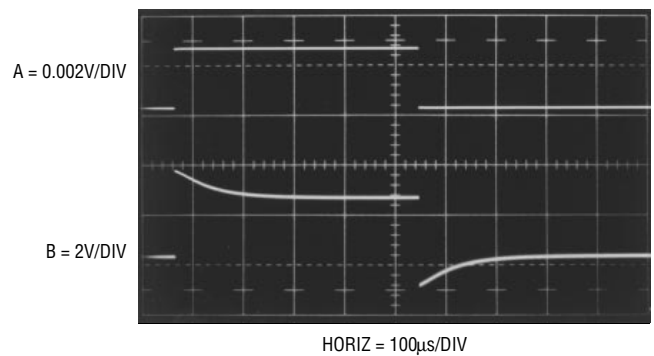


Figure 78. Gain vs Bandwidth for the X1000 Differential Amplifier. Peaking Noted in Figure 77 Shows up as 0.25dB Peak at 5MHz, Which Could be Trimmed Out



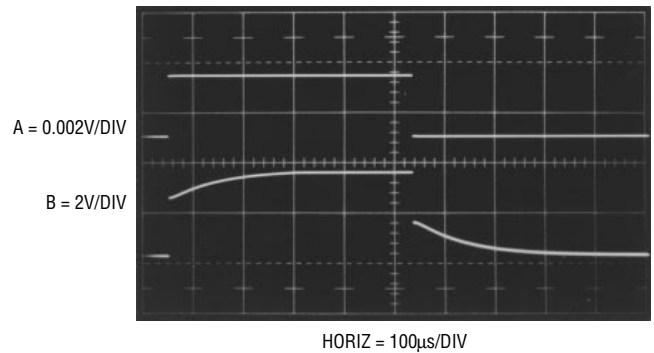
LTAN47 • TA79

Figure 79. Response of X1000 Amplifier with Bandwidth Crossover Points Properly Adjusted. A = Input; B = Output



LTAN47 • TA80

Figure 80. Response of X1000 Amplifier with Excessive AC Gain. A = Input; B = Output



LTAN47 • TA81

Figure 81. Response of X1000 Amplifier with Too Much DC Gain. A = Input; B = Output

provides proper initial response, but too much DC gain forces a long, tailing response to an incorrect amplitude.

High Speed Differential Line Receiver

High speed analog signals transmitted on a line often pick up substantial common-mode noise. Figure 82 shows a simple, fast differential line receiver using the LT1194

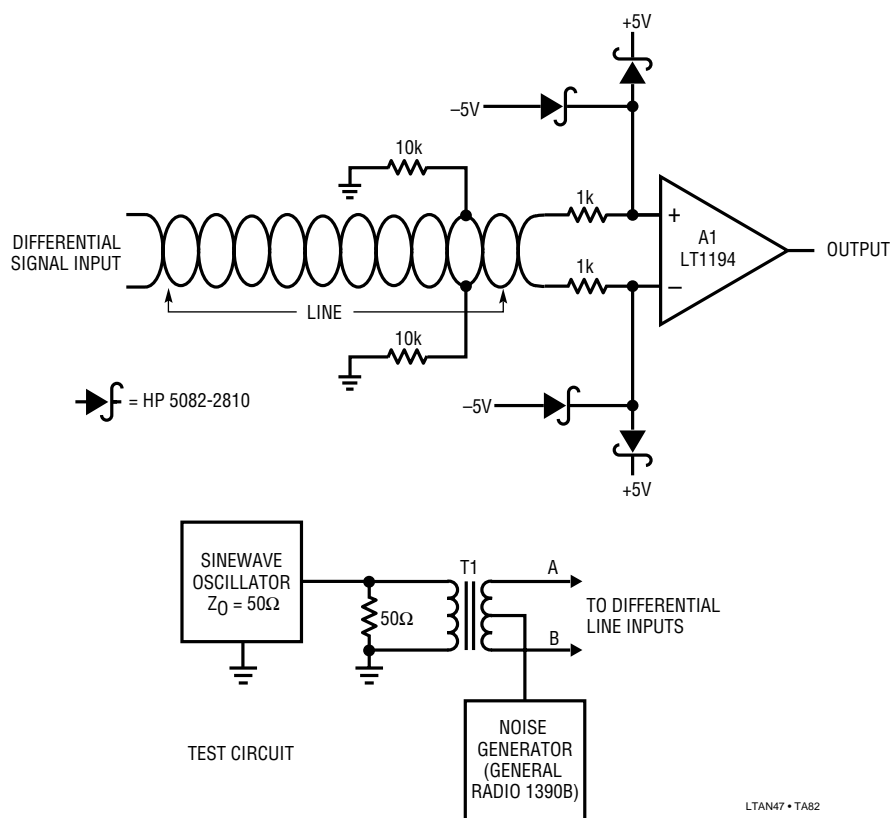


Figure 82. Simple, Full Differential Line Receiver

gain-of-ten differential amplifier. The differential line is fed to A1. The resistor-diode networks prevent overload and insure input bias for A1 under all conditions. A1's output represents the difference of the two line input times a gain of ten. In theory, all common-mode noise should be rejected. The test circuit shown in the figure confirms this. The sinewave oscillator drives T1 (Trace A, Figure 83), producing a differential line output at its secondary. T1's secondary is returned to ground through a broadband noise generator, flooding the line inputs with common-mode noise (traces B and C are A1's inputs). Trace D, A1's X10 version of the differential signal at its inputs, is clean with no visible noise or disturbances. This circuit will easily provide a clean output with DC-5MHz noise dominating signal by a 100:1 ratio.

Transformer Coupled Amplifier

Figure 84 shows another way to achieve high common-mode rejection. Additionally, this circuit has the advantage of true 3 port isolation. The input, gain stage, and output are all galvanically isolated from each other. As such, this

configuration is useful where large common-mode differences are encountered or where ground integrity is uncertain. A1 is set up in a simple gain of 11. T1 feeds its input, and the output is taken from T2. Figure 85 shows results for a 4MHz input, with all "•" designated transformer leads referred to ground. The input (Trace A, Figure 85) is applied to T1, whose output (Trace B) feeds A1. A1 takes gain, and its output (Trace C) feeds T2. T2's output

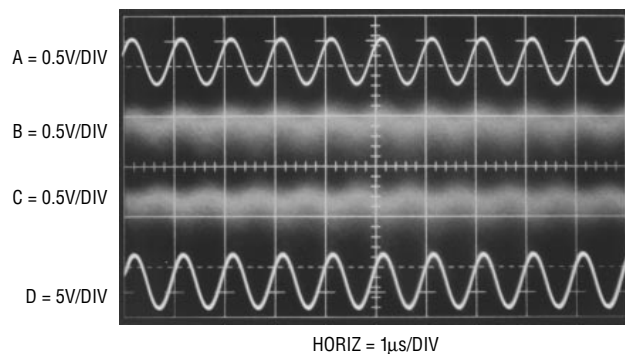
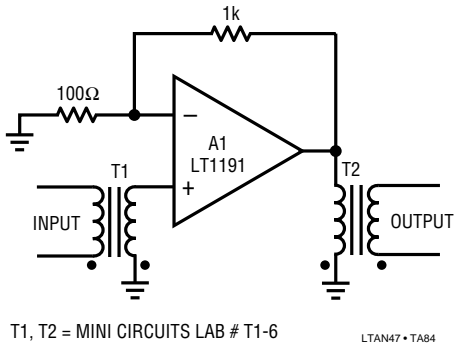


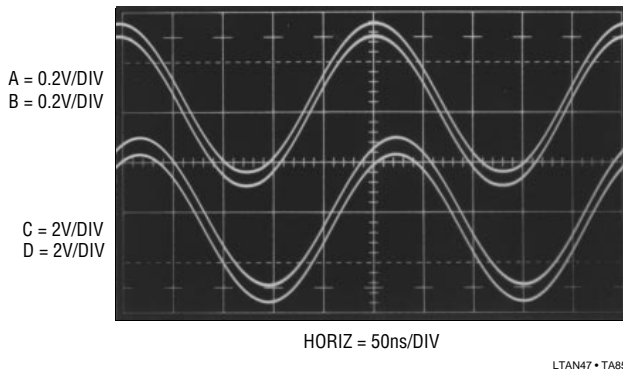
Figure 83. Differential Line Receiver Easily Pulls Out a Signal Buried in Common-Mode Noise. Output is Clean, Despite 100:1 Noise-to-Signal Ratio

(Trace D) is the circuit's output. Phase shift is evident, although tolerable. T1 and T2 are very wideband devices, with low phase shift. Note the negligible phase difference between the A-B and C-D trace pairs. A1 contributes essentially the entire phase error. Using the transformers specified, the circuit's low frequency cut-off is about 10kHz.



T1, T2 = MINI CIRCUITS LAB # T1-6
LTAN47 • TA84

Figure 84. Transformer Coupled Amplifier. Note That A1 is Galvanically Isolated From Input and Output Nodes



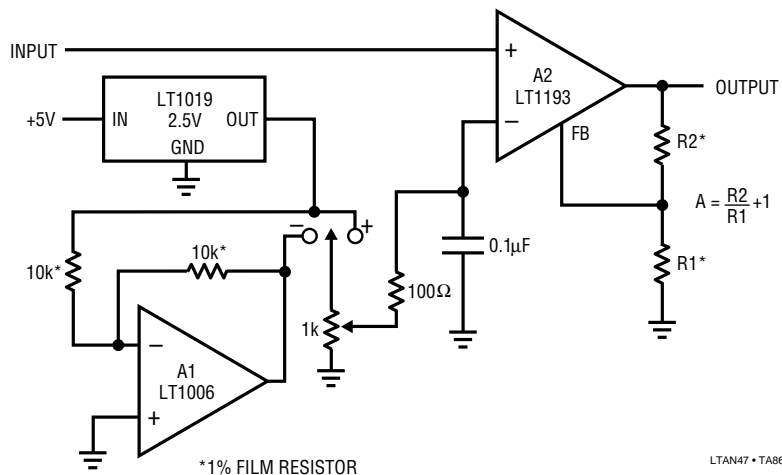
LTAN47 • TA85

Figure 85. Transformer Coupled Amplifier Responds to an Input (Trace A) with a Slightly Phase Shifted Output (Trace D). Traces B and C are T1 Secondary and T2 Primary, Respectively

Differential Comparator Amplifier with Adjustable Offset

It is often desirable to examine or amplify one particular portion of a signal while rejecting all other portions. At high speed this can be difficult, because the amplifier may see fast, large common-mode swings. Recovery from such activity usually is dominated by saturation effects, making the amplifier's output questionable. The LT1193's differential amplifier's fast overload recovery permits this function, maintaining output fidelity to the input signal. Additionally, the input level amplitude at which amplification begins is settable, allowing any amplitude defined point to be selected. In Figure 86, A1, the LT1019 reference and associated components form an adjustable, bipolar voltage source which is coupled to differential amplifier A2's negative input. The input signal biases A2's positive input with A2's gain set by R1 and R2, in accordance with the equation given.

Input signals below A2's negative input levels maintain A2's output in saturation, and no signal is seen at the output. When the positive input rises above the negative input's bias point A2 becomes active, providing an amplified version of the instantaneous difference between its inputs. Figure 87 shows what happens when the output of a triangle wave generator (Trace A) is applied to the circuit. Setting the bias level just below the triangle peak permits high gain, detailed operation of the turnaround at the peak. Switching residue in the generator's output is clearly observable in Trace B. Appropriate variations in the voltage source setting would permit more of the triangle



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Figure 86. Fast Differential Comparator Amplifier with Settable Offset

Application Note 47

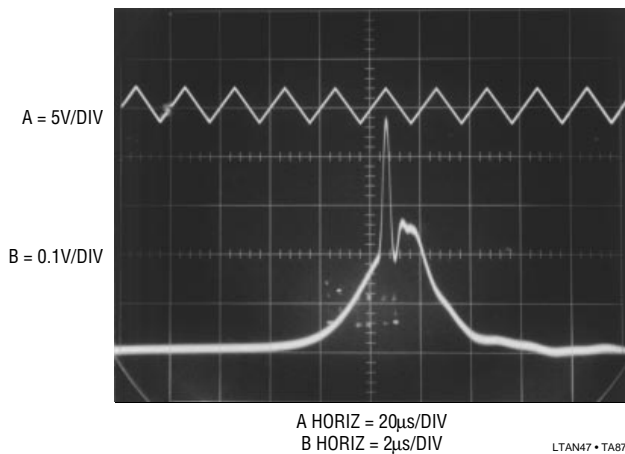


Figure 87. The Differential Comparator Amplifier Extracting Signal Detail From a Triangle Waveform's Peak. Triangle Generator's Switching Artifacts are Clearly Evident

slopes to be observed, with attendant loss of resolution due to oscilloscope overload limitations. Similarly, increasing A2's gain allows more amplitude detail while placing restrictions on how much of the waveform can be displayed. It is worth noting that this circuit performs the same function as differential plug-in units for oscilloscopes. This circuit's output is accurate and settled to 0.1% 100ns after it enters its linear region.

Differential Comparator Amplifier with Settable Automatic Limiting and Offset

Figure 88 extends the previous circuit's operation, allowing amplified observation of information between two settable, amplitude defined points. The amplitude setpoints are settable in both magnitude and sign. In this circuit the polarity of the offset applied to A2's negative input is

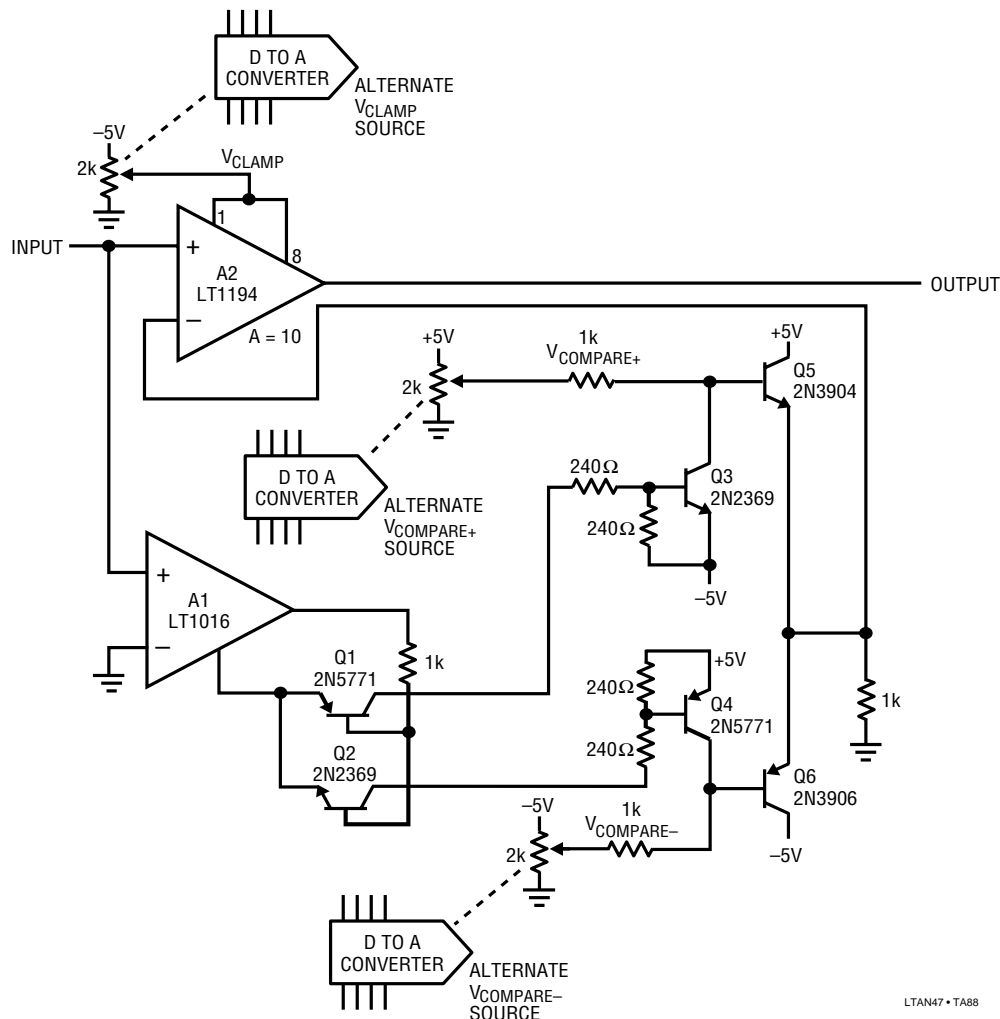


Figure 88. Differential Comparator Amplifier with Settable Automatic Limiting and Offset

determined by comparator A1's output state. A1 compares the circuit's input to ground, generating polarity information at its outputs. Level shifters Q1-Q3 and Q2-Q4 bias followers Q5 and Q6. Positive circuit inputs result in Q5 supplying the "V_{COMPARE+}" potential to A2, while negative inputs route "V_{COMPARE-}" to A2. This eliminates the previous circuit's manual polarity switch, permitting automatic selection of the differencing polarity and amplitude. Additionally, this circuit takes advantage of A2's input clamp feature. This feature (See LT1194 Data Sheet) limits the dynamic range of the input, clamping the amplifier's input operating range. Signals inside the clamp limit are processed normally, while signals outside the limit are precluded from influencing the amplifier. This combination of circuit controls allows very tightly defined windows on a waveform to be selected for accurate amplification without overload restrictions.

Figure 89 shows the circuit output for a sine input (Trace A) from the same function generator used to test the previous circuit. The V⁺ and V⁻ compare voltages are set just below the sinewave peaks, with "V_{clamp}" programmed to restrict amplification to the peak's excursion. Trace B, the circuit's output, simultaneously shows amplitude detail of *both* sine peaks. The observed distortion is directly traceable to this generator's imperfect internal triangle waveform (see Figure 87), as well as its sine shaper characteristics.

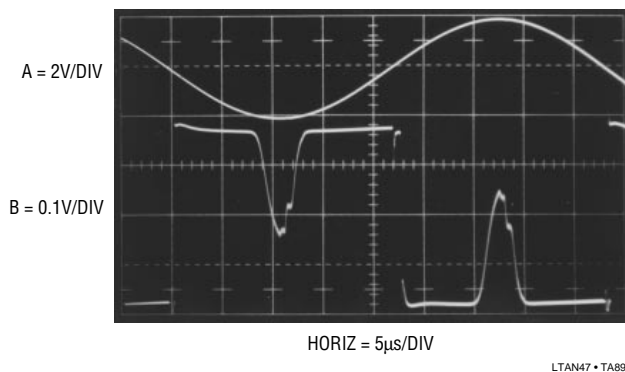


Figure 89. The Automatic Differential Comparator Amplifier Finds Triangle Wave and Switching Residuals (Trace B) in Trace A's Peaks

Photodiode Amplifier

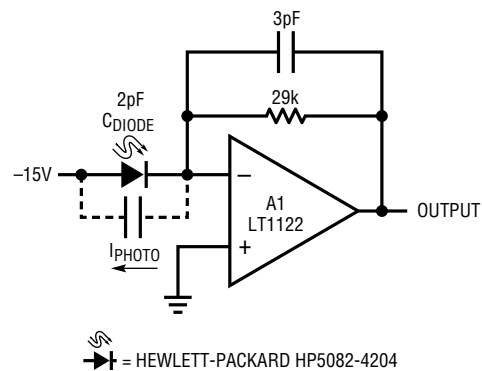
Amplification of fast photodiode signals over a wide range of intensity is a common requirement. Figure 90's fast FET amplifier serves well, giving wideband operation with 5

decades of photocurrent. The photodiode is set up in the conventional manner. Photocurrent is fed directly to A1's summing point, causing A1's output to move to the level required to maintain virtual ground at the negative input. The -15V diode bias aids diode response. The table in the figure details circuit operating characteristics with the diode specified.

Some care in frequency compensating this configuration is required. The diode has about 2pF of parasitic capacitance, forming a significant lag at A1's summing point. If no feedback capacitor is used, high speed dynamics are poor. Figure 91 shows circuit response to a photo input (Trace A) with the indicated 3pF feedback capacitor removed. A1's output overshoots and saturates before finally ringing down to final value. In contrast, replacing the 3pF capacitor provides Figure 92's results. The same input pulse (Trace A, Figure 92) produces a cleanly damped output (Trace B). The capacitor imposes a 50% speed penalty (note faster horizontal scale for Figure 92). This is unavoidable because suppressing the parasitic ringing's relatively low frequency mandates significant roll-off.

Fast Photo Integrator

A related circuit to the photodiode amplifier is Figure 93's photo integrator. Here, the output represents the integral of the diode's photocurrent over some period of time. This



→ = HEWLETT-PACKARD HP5082-4204

RESPONSE DATA

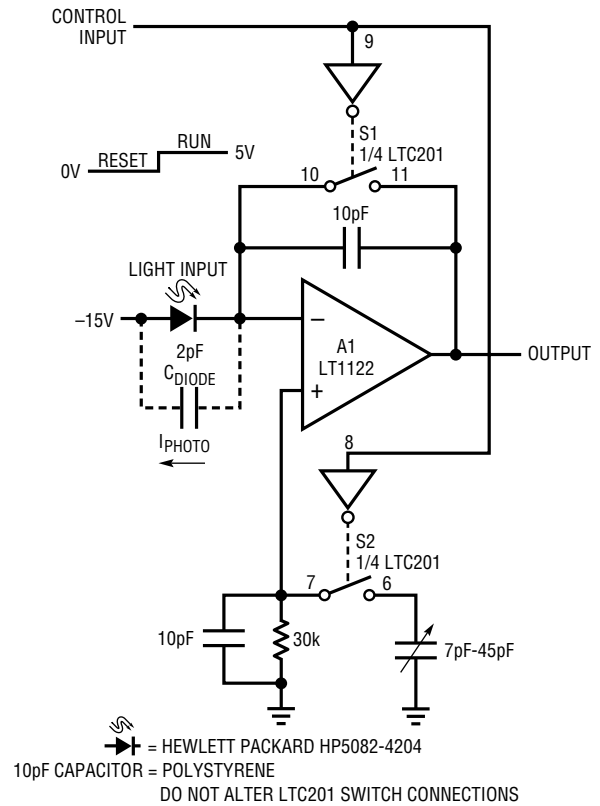
LIGHT (900nm)	DIODE CURRENT	CIRCUIT OUTPUT
1mW	350µA	10.0V
100µW	35µA	1V
10µW	3.5µA	0.1V
1µW	350nA	0.01V
100nW	35nA	0.001V

LTAN47 • TA89

Figure 90. A Simple Photodiode Amplifier

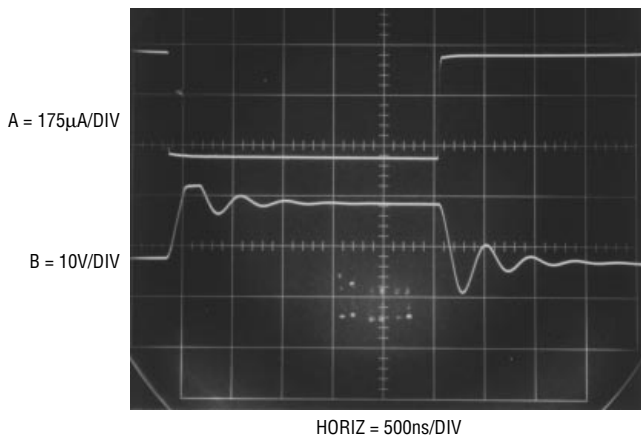
Application Note 47

circuit is particularly applicable in situations where the total energy in a light pulse (or pulses) must be measured. The circuit is a very fast integrator, with S1 used as a reset switch. S2, switched simultaneously with S1, compensates S1's charge injection error. With the control input (Trace A, Figure 94) low and no photocurrent, S1 is closed and A1 looks like a grounded follower. Under these conditions A1's output (Trace C) sits at 0V. When the control input goes high, A1 becomes an integrator as soon as S1 opens. Due to switch delay, this occurs about 150ns after the control input goes high. When S1 opens it delivers some parasitic charge to A1's summing point. S2 provides a compensatory charge based pulse at A1's positive terminal to cancel the effects of S1's charge error. This action shows up as a fast, small amplitude event in A1's output which settles rapidly back to 0V.



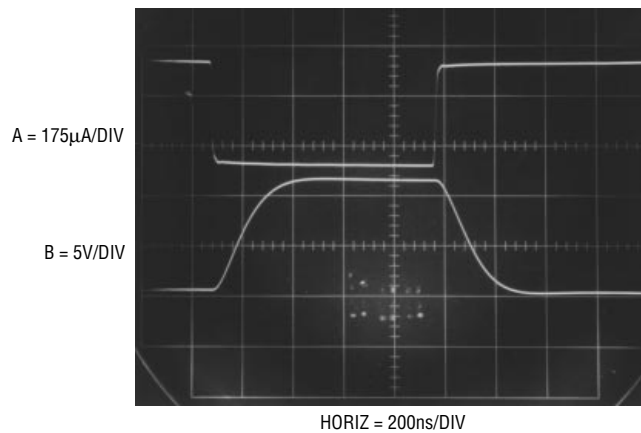
LTAN47 • TA93

Figure 93. A Very Fast Photo Integrator. S2 Compensates Reset Switch S1's Small Charge Injection



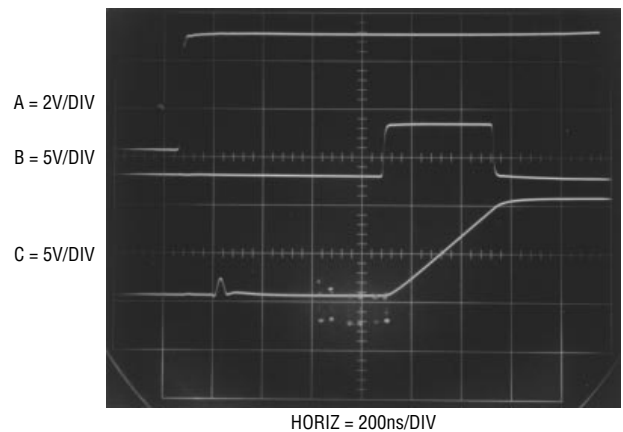
LTAN47 • TA91

Figure 91. Response of Figure 90 Without a Feedback Capacitor



LTAN47 • TA92

Figure 92. Figure 90 Responding with a Feedback Capacitor



LTAN47 • TA94

Figure 94. The Photo Integrator Acquires (Trace C) an Input Light Pulse (Trace B) with the Control Line (Trace A) in the Run Mode. Charge Cancellation Action is Evident at Trace C's 400ns Point

At this point in time the integrator is ready to receive and record a photo pulse. When light falls on the photodiode (Trace B triggers a light pulse seen by the photodiode) A1 responds by integrating. In this case A1's output integrates rapidly until the light pulse ceases. A1's voltage after the light event is over is related to the total energy seen by the diode during the event. A monitoring A-D converter can acquire A1's output. In typical operation the control line returns low, resetting A1 until the next event is to be integrated.

With only 10pF of integration capacitor, the circuit has an output droop rate of about 0.2V/μs. This can be increased, although integration speed will suffer accordingly. Integration times of nanoseconds to milliseconds and photocurrents ranging from nanoamperes to hundreds of microamperes are accommodated by the circuit as shown. Thus, light intensities spanning microwatts to milliwatts over wide ranges of duration are practical inputs. The primary accuracy restrictions are A1's 75pA bias current, its 12V output swing and the effectiveness of the charge cancellation network. Typically, full-scale accuracy of several percent is achievable if the charge cancellation network is trimmed. To do this, assure that the diode sees no light while repetitively pulsing the control line. Adjust the trimmer capacitor for 0V output at A1 immediately after the disturbance associated with the S1-S2 switching settles.

Fiber Optic Receiver

A simple high speed fiber optic receiver appears in Figure 95. A1, a photocurrent-to-voltage converter similar to Figure 90, feeds comparator A2. A2 compares A1's output

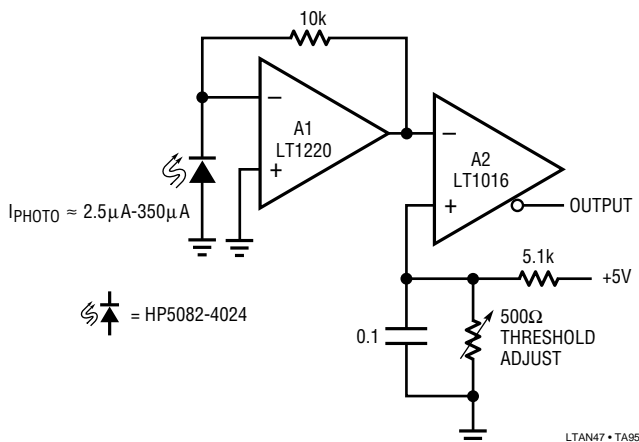


Figure 95. A Simple Fiber Optic Receiver

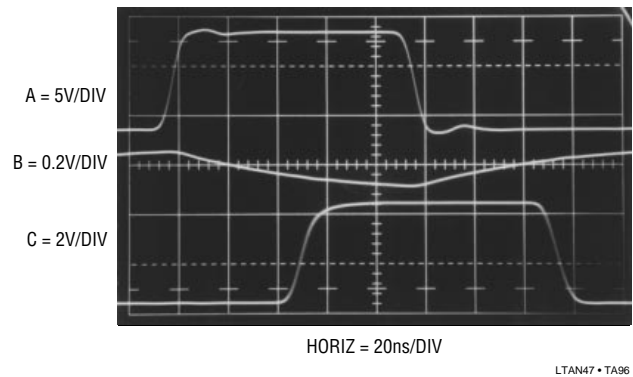


Figure 96. Waveforms for the Simple Fiber Optic Receiver. A1 (Trace B) Lags the Input (Trace A), but Output (Trace C) is Clean

to a DC level established by the threshold adjust setting, producing a logic compatible output. Figure 96 shows typical waveforms. Trace A is a pulse associated with a photo input. Trace B is A1's response and Trace C is A2's output. The phase shift between the photo input and A2's output is due to A1's delay in reaching the threshold level. Reducing the threshold level will help, but moves operation closer to the noise floor. Additionally, the fixed threshold level cannot account for response changes in the emitter and detector diodes and fiber optic line over time and temperature.

40MHz Fiber Optic Receiver with Adaptive Trigger

Receiving high speed fiber optic data with wide input amplitude variations is not easy. The high speed data and uncertain intensity of the light level can cause erroneous results unless the receiver is carefully designed. Figure 97 addresses the previous circuit's limitations, offering significant performance advantages. This receiver will reliably condition fiber optic inputs of up to 40MHz with input amplitude varying by >40dB. Its digital output features an adaptive threshold trigger which accommodates varying signal intensities due to component aging and other causes. An analog output is also available to monitor the detector output. The optical signal is detected by the PIN photodiode and amplified by A1. A second stage, A2, gives further amplification. The output of this stage biases a 2-way peak detector (Q1-Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of A2's output signal's mid-point appears at the junction of the 500pF capacitor and the 22MΩ units. This point will always sit midway between the signal's excursions, re-

Application Note 47

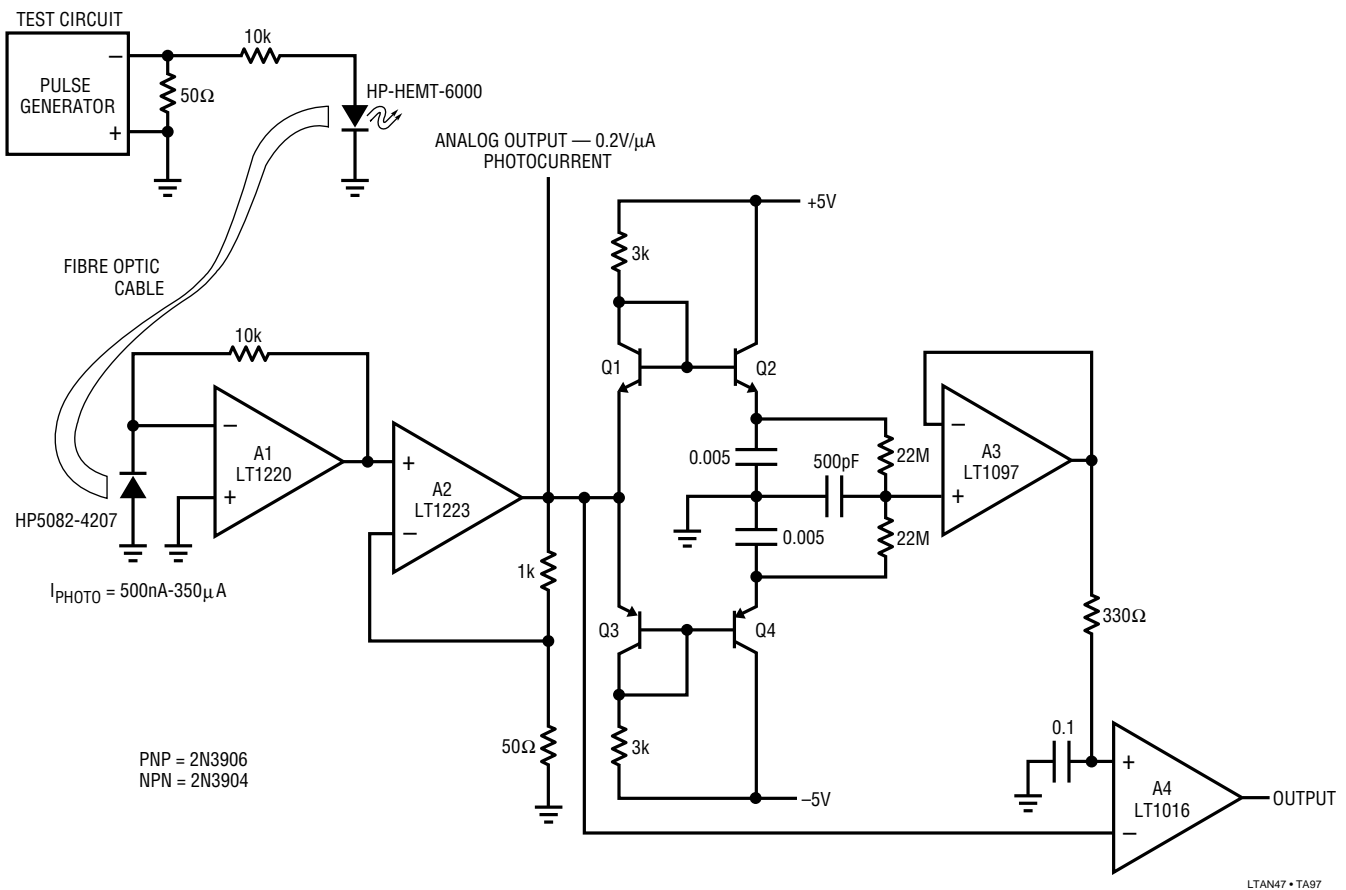


Figure 97. Adaptively Triggered 40MHz Fiber Optic Receiver is Immune to Shifts in Operating Point

ardless of absolute amplitude. This signal-adaptive voltage is buffered by the low bias LT1097 to set the trigger voltage at the LT1016's positive input. The LT1016's negative input is biased directly from A2's output. Figure 98 shows the results using the test circuit indicated in Figure 97. The pulse generator's output is Trace A, while A2's output (analog output monitor) appears in Trace B. The LT1016 output is Trace C. The waveforms were recorded with a $5\mu\text{A}$ photocurrent at about 20MHz. Note that A4's output transitions correspond with the midpoint of A2's output (plus A4's 10ns propagation delay) in accordance with the adaptive trigger's operation.

50MHz High Accuracy Analog Multiplier

Although highly accurate, very wideband analog multipliers are available, their output takes a differential form. These differential outputs, which have substantial common mode content, are frequently inconvenient to work with. RF transformers can be used to single end the outputs, but DC and low frequency information is lost.

Figure 99 uses the LT1193 differential amplifier to accomplish the differential-to-single ended transition. The AD834 is set up in the recommended configuration (see Analog Devices AD834 Data Sheet, Reference 26). The LT1193 takes the differential signal from the AD834's 50Ω terminated output and provides a single ended output. The gain of two yields a $\pm 1\text{V}$ output at full-scale.

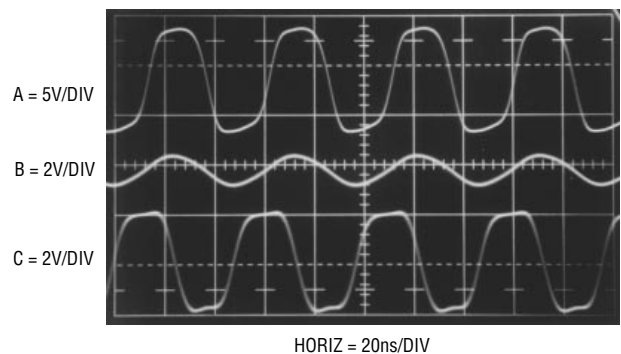


Figure 98. Adaptively Triggered Fiber Optic Receiver's Waveforms at 20MHz with $5\mu\text{A}$ Diode Current

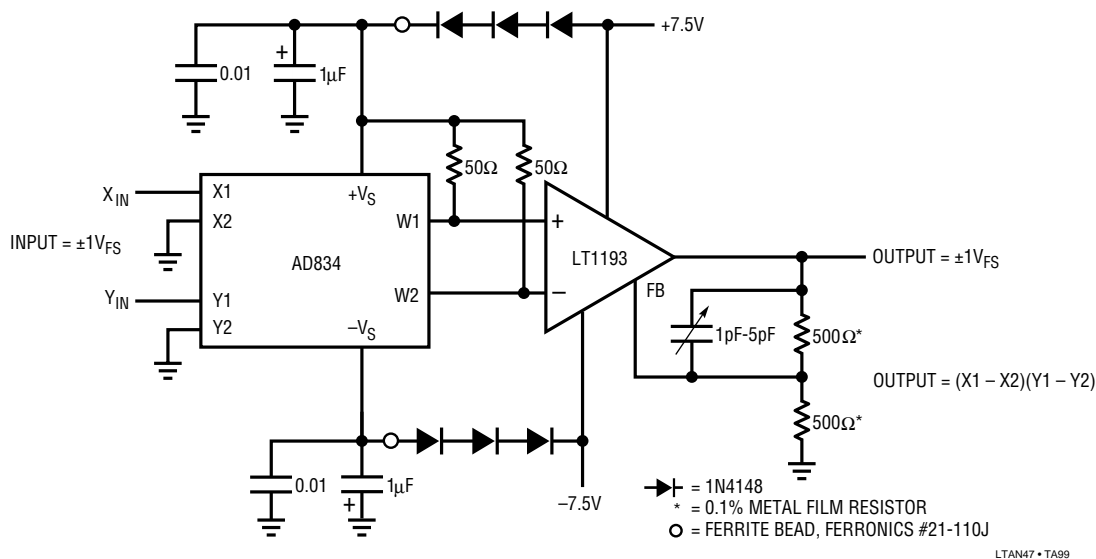


Figure 99. Analog Multiplier with 2% Accuracy Over DC to 50MHz Has a Single Ended Output

The AD834 outputs come out riding on a common-mode level very close to the device's positive supply. This common-mode level falls outside the LT1193's input common-mode range. The diodes in the 7.5V supply rails drop the supply at the AD834, biasing its outputs within the LT1193's input range. This scheme avoids the attenuation and matching problems presented by placing a level shift between the multiplier and amplifier. The ferrite beads combine with the diode's impedance to ensure adequate bypassing for the multiplier, a very wideband device.

Performance for this circuit is quite impressive. Error remains within 2% over DC-50MHz, with feedthrough below -50dB. Trimming the circuit involves adjusting the variable capacitor at the amplifier for minimal output square wave peaking. Figure 100 shows performance when a 20MHz sine input is multiplied by Trace A's waveform. The output (Trace B) is a singularly clean instantaneous representation of the X•Y input products, with strict fidelity to their components.

Power Booster Stage

Occasionally, it is necessary to supply larger output currents than an amplifier is capable of delivering. The power gain stage, sometimes called a booster, is usually placed within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics.

Because the output stage resides in the amplifier's feedback path, loop stability is a concern. This is particularly the case with high speed amplifiers. The output stage's gain and AC characteristics must be considered if good dynamic performance is to be achieved. Overall circuit frequency response and dynamic load handling capabilities are issues that cannot be ignored when designing a power gain stage for a monolithic amplifier. The output stage's added gain and phase shift can cause poor AC response or outright oscillation. Judicious application of frequency compensation methods is needed for good results (see Appendix C, "The Oscillation Problem – Frequency Compensation Without Tears", for discussion and details on compensation methods).

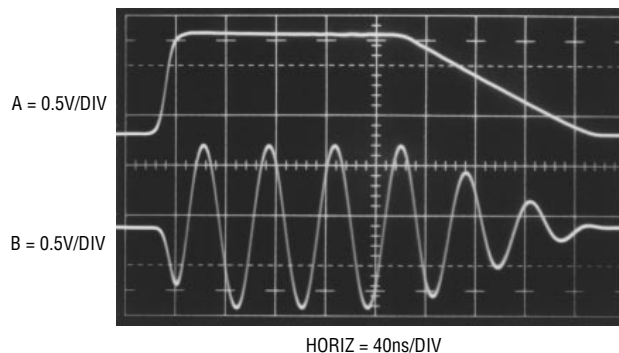


Figure 100. The Multiplier Produces a Modulated Sine Output (Trace B) in Accordance with Trace A's Envelope

Application Note 47

Figure 101 shows a 200mA power booster used with an LT1220 amplifier. Complementary emitter followers Q1-Q5 provide current gain for positive signals, with Q2 and Q6 handling negative excursions. Q3 and Q4 are V_{BE} based current limits, coming on and robbing drive from the appropriate output transistor when current exceeds about 300mA. The diodes prevent Q1 and Q2 from seeing reverse V_{BE} during current limit. The 100Ω resistor and ferrite beads prevent the low impedance amplifier output from causing oscillation in Q1 and Q2 (see Appendix C).

To be effective, the booster must be exceptionally fast. A slow design will obviate the AC performance of the amplifier controlling it, or in the worst case, cause oscillation (again, see Appendix C). Figure 102 shows booster performance with the LT1220 removed from the circuit. The input pulse (Trace A) is applied to the booster input, with the output (Trace B) taken at the indicated spot. Evaluation of the photograph shows that booster rise and fall times are limited by the input pulse generator. Additionally, delay is in the 1ns range. This kind of speed makes the circuit a good candidate for acceptable AC performance within a fast amplifier's loop.

Figure 103 shows pulse response with the LT1220 installed in the circuit with a 50Ω load. The booster's high speed contributes negligible delay and overall response is clean and predictable. The local 3pF roll-off at the LT1220 optimizes response, but is not absolutely necessary in this circuit. The input (Trace A) produces a nicely shaped LT1220 slew-limited output (Trace B).

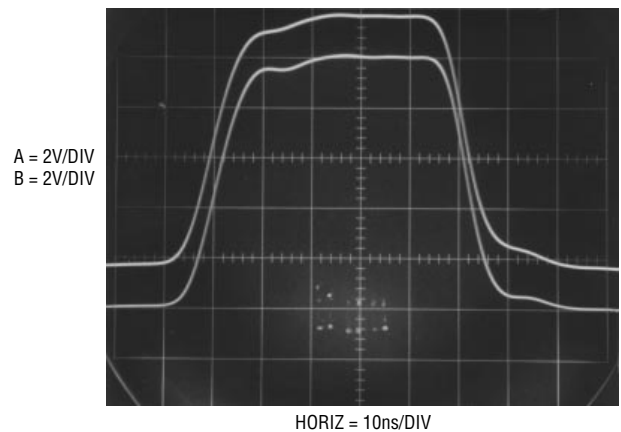


Figure 102. Response of Figure 101's Booster Stage

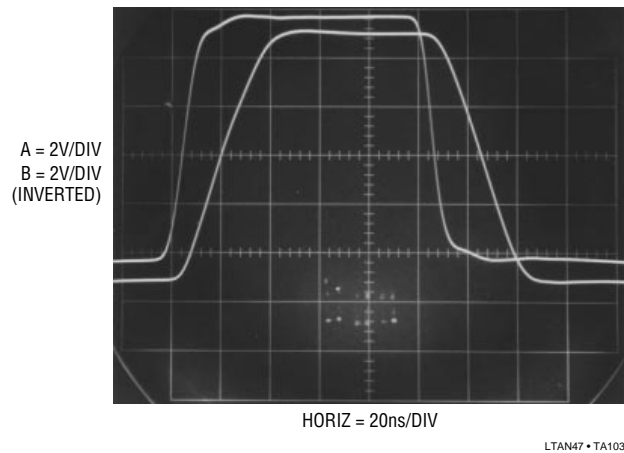


Figure 103. The Booster's Response When Inside an Amplifier's Loop

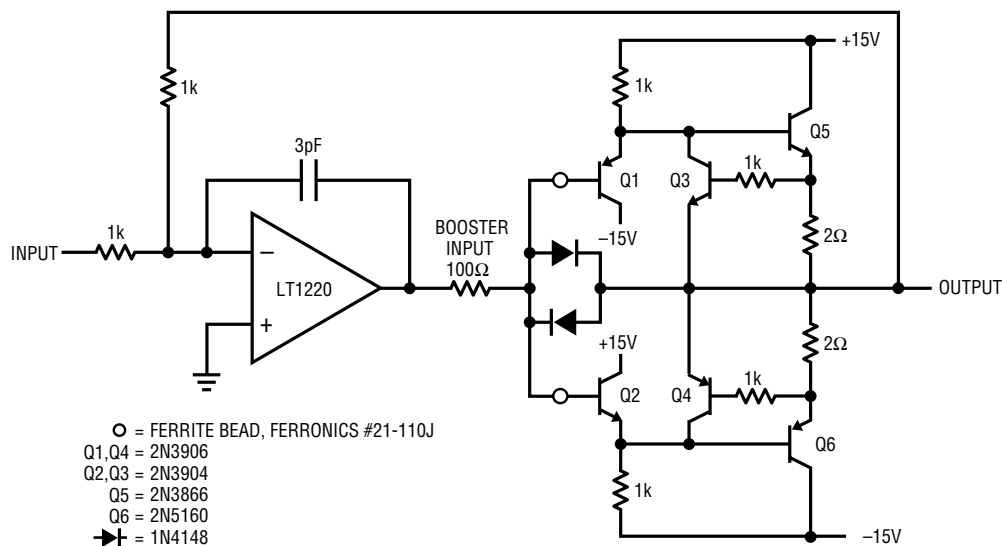


Figure 101. A 200mA Output Wideband Booster Stage

LTAN47 • TA101

High Power Booster Stage

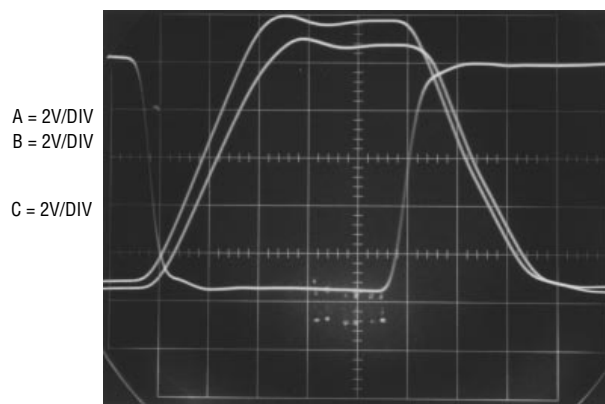
In theory, higher power booster stages should be achievable by utilizing bigger devices. This is partly the case, but lack of availability of wideband PNP power transistors is an issue. Figure 104 shows a way around this problem.

The circuit is essentially a 1A output version of Figure 101, with several differences. In the positive signal path output transistor Q4 is an RF power type, driven by Darlington connected Q3. The diode in Q1's emitter compensates the additional V_{BE} introduced by Q3, preventing crossover distortion.

The negative signal path substitutes the Q5-Q6 connection to simulate a fast PNP power transistor. Although this configuration acts like a fast PNP follower, it has voltage gain and tends to oscillate. The local 2pF feedback capacitor suppresses these parasitic oscillations and the composite transistor is stable.

This circuit also includes a feedback capacitor trim to optimize AC response. This difference from the previous circuit is necessitated by this circuit's slightly slower characteristics and much heavier loading. Current limit operation and other characteristics are similar to the lower power circuit.

Figure 105 shows waveforms for a 10V negative input step (Trace A) with a 10Ω load. The amplifier responds (Trace B), driving the booster to the voltage required to close the loop. For this positive step, the amplifier provides about 1.5V overdrive to overcome Q3 and Q4's V_{BE} drops. The booster output, lagging by a few nanoseconds (Trace C), drives the load cleanly, with only minor peaking. This peaking may be minimized with the feedback capacitance trimmer.



LTAN47 • TA105

Figure 105. The Boosted Op Amp Drives a 1A Load to 10V in 50ns

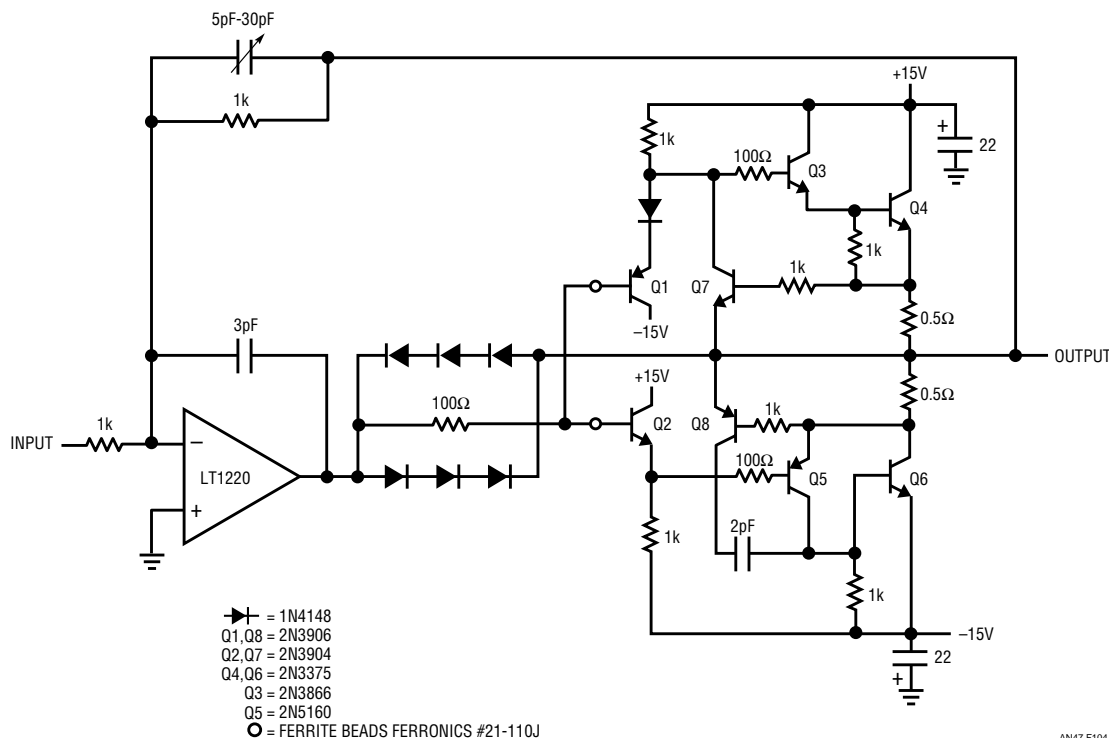


Figure 104. Fast, 1A Booster Stage

Application Note 47

Ceramic Bandpass Filters

Figure 106 is a highly selective bandpass filter using a resonant ceramic element and a single amplifier. The ceramic element nominally looks like a high impedance off its resonant frequency, in this case 400kHz. For off resonance inputs, A1 acts like a grounded follower, producing no output. At resonance, the ceramic element has a low impedance and A1 responds as an inverter with gain. The 100Ω resistor isolates the ceramic element's capacitance from A1's summing point. This capacitance is quite substantial and limits the circuit's out of band rejection capability. Figure 107 shows this. This plot shows very steep rejection, with A1's output down almost 20dB at 300kHz and 40dB at 425kHz. The device's stray parasitic capacitance causes the gentle rise in output at higher frequencies and also sets the -20dB floor at 300kHz.

Figure 108 partially corrects this problem with a nulling technique. This circuit is similar to the previous one, except that a portion of the input is fed to A1's positive input. The RC network at this input is scaled to look like the ceramic resonator's off null impedance. As such, A1's inputs see similar signals for out of band components,

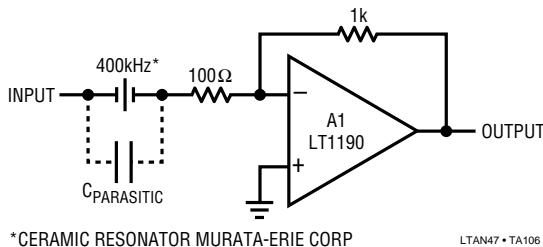


Figure 106. A Piezo-Ceramic Based Filter

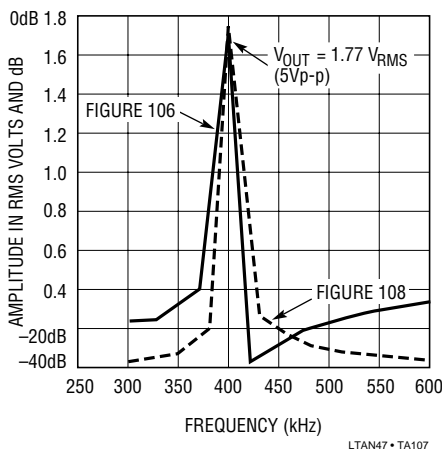


Figure 107. Response of Both Piezo-Ceramic Filters. Differential Network's Activity is Evident in Figure 108's Performance

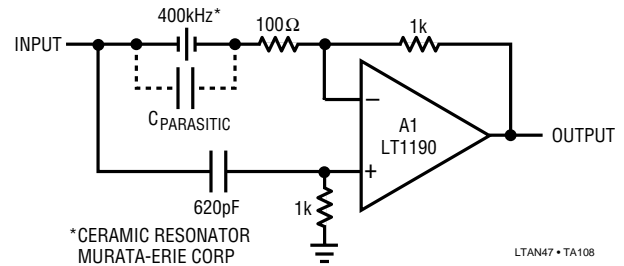


Figure 108. Differential Network Nulls Parasitic Capacitance of Ceramic Element

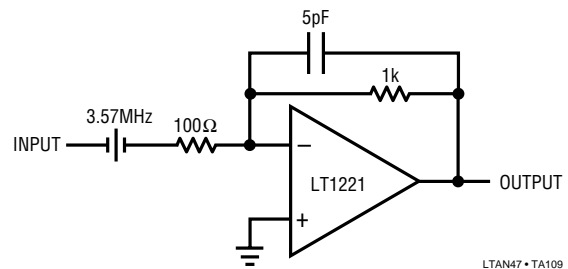


Figure 109. Crystal Filter

resulting in attenuation via A1's common-mode rejection. At resonance, the added RC network appears as a much higher impedance than the ceramic element and filter response is similar to Figure 106's circuit. Figure 107 shows that this circuit has much better out of band rejection than Figure 106. The high frequency roll-off is smooth, and over 20dB deeper than Figure 106 at 475kHz. The low frequency side of resonance has similar characteristics at 375kHz and below.

Crystal Filter

Quartz crystals can also be used to make even higher selectivity filters at higher frequencies. Figure 109 replaces Figure 106's ceramic element with a 3.57MHz quartz crystal. Figure 110 shows almost 30dB attenuation only a few kHz on either side of resonance! The differential nulling technique used with the ceramic elements is less effective with quartz crystals. Crystals have significantly lower parasitic terms, making the cancellation less effective.

APPLICATIONS SECTION II - OSCILLATORS

Sine Wave Output Quartz Stabilized Oscillator

Figure 111 places a crystal within the amplifier's feedback path, creating an oscillator. With the crystal removed, the

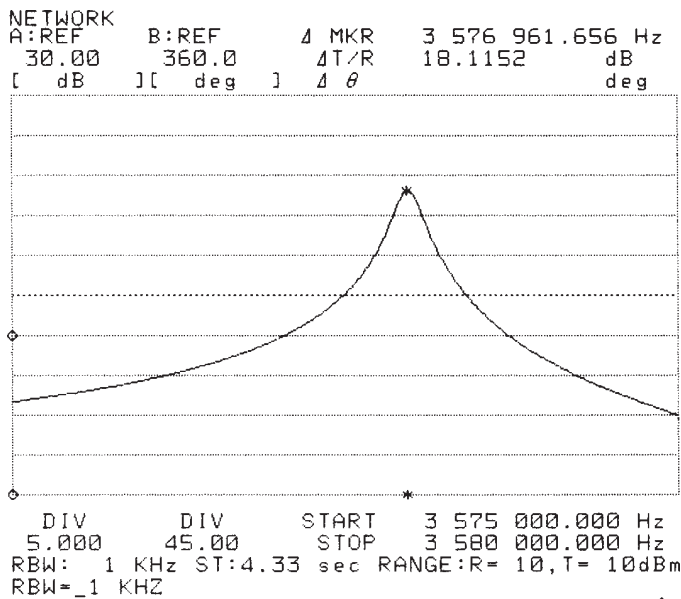


Figure 110. The Crystal Filter's Response

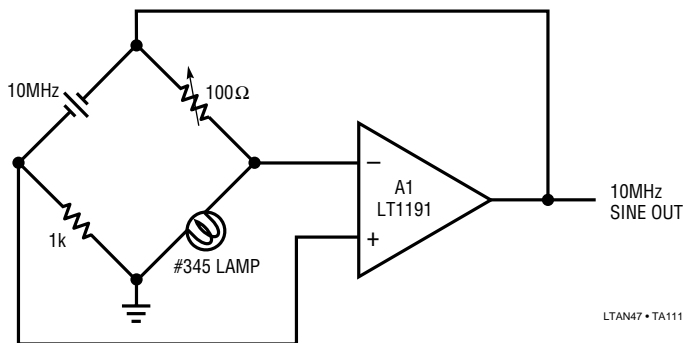


Figure 111. 10MHz Quartz Stabilized Sine Wave Oscillator

circuit is a familiar non-inverting amplifier with a grounded input. Gain is set by the impedance ratio of the elements associated with A1's negative input. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency and oscillations commence.

In any oscillator it is necessary to control the gain as well as the phase shift at the frequency of interest. If gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting. Here, gain control comes from the positive temperature coefficient of the lamp at A1's negative input. When power is applied, the lamp is at a low resistance value, gain is high and oscillation amplitude builds. As amplitude builds, lamp current increases, heating occurs, and the lamp's resistance goes up. This causes a reduction in amplifier gain and the circuit finds a

stable operating point. This circuit's sine wave output has all the stability advantages associated with quartz crystals. Although shown at 10MHz, it works well with a wide variety of crystal types over a 100kHz-20MHz range. The use of the lamp to control amplifier gain is a classic technique, first described by Meacham in 1938.¹² Electronic gain control, while more complex, offers more precise control of amplitude.

Sine Wave Output Quartz Stabilized Oscillator with Electronic Gain Control

Figure 112's quartz stabilized oscillator replaces the lamp with an electronic amplitude stabilization loop. A2 compares the A1 oscillator's positive output peaks with a DC reference. The diode in the DC reference path temperature compensates the rectifier diode. A2 biases Q1, controlling its channel resistance. This influences loop gain, which is reflected in oscillator output amplitude. Loop closure around A1 occurs, stabilizing oscillator amplitude. The 1μF capacitor compensates the gain control loop.

The DC reference network is set up to provide optimum temperature compensation for the rectifier diode, which sees a 2Vp-p 20MHz waveform out of A1. A1's small amplitude swing minimizes distortion introduced by channel resistance modulation in Q1. To use this circuit, adjust the 50Ω trimmer until 2Vp-p oscillations appear at A1's output.

Figure 113 is a spectrum analysis of the oscillator's output. The fundamental sits at 20MHz, with the second harmonic 47dB down at 40MHz. A third harmonic, 50dB down, occurs at 60MHz. Resolution bandwidth for the spectrum analysis is 1kHz.

DC Tuned 1MHz-10MHz Wien Bridge Oscillator

In Figure 114 the quartz crystal is replaced with a Wien network at A2's positive input. A1 controls Q1 to amplitude stabilize A2's oscillations in identical fashion to the previous figure. Although the Wien network is not nearly as stable as a quartz crystal, it has the advantage of a variable frequency output. Normally, this is facilitated by varying either R, C, or both. Usually, manually adjustable elements such as dual potentiometers and two section variable

Note 12: See Reference 20, as well as References 19 and 21 for supplemental information.

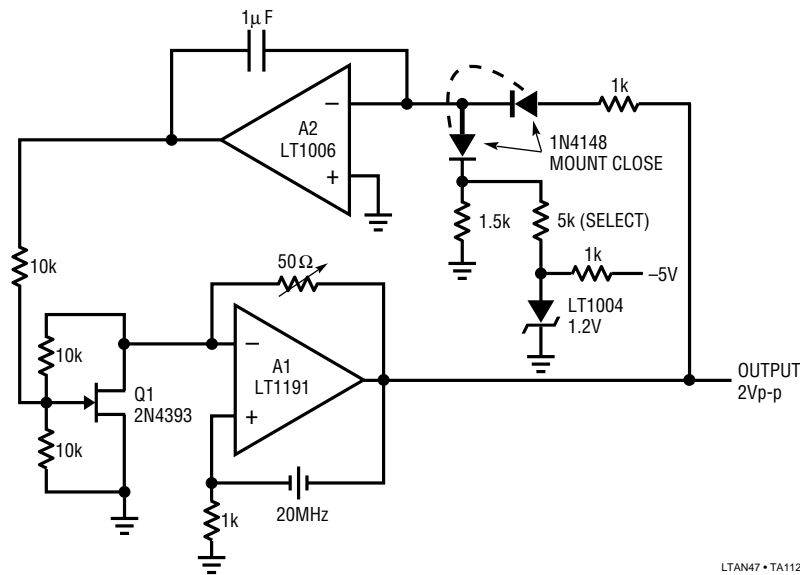


Figure 112. 20MHz Quartz Stabilized Sine Wave Oscillator with Electronic AGC

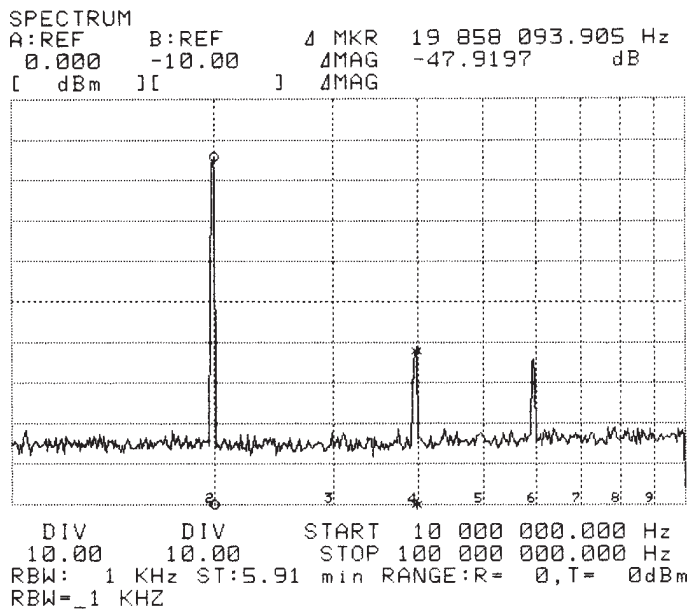


Figure 113. Spectrum Analysis of the 20MHz Quartz Oscillator. Harmonic Content is at Least 47dB Down

capacitors are used. Here, the Wien network resistors are fixed at 360Ω , while the capacitive elements are realized with varactor diodes. The varactor diodes voltage-variable-capacitance characteristic allows DC tuning of the oscillator. DC inputs of 0V-10V to the varactors result in a 1MHz to 10MHz shift in oscillation frequency. The $0.1\mu\text{F}$ capacitor blocks the DC bias from A2's positive input while permitting the Wien network to function normally. A2's 2Vp-p output minimizes the varactor's junction effects, aiding distortion.

This $\pm 5\text{V}$ powered circuit requires voltage step-up to develop adequate varactor drive. A3 and the LT1172 switching regulator form a simple voltage step-up regulator. A3 controls the LT1172 to produce the output voltage required to close a loop at A3's negative input. L1's high voltage inductive flyback events, rectified by the diode and zener connected Q2, are stored in the $22\mu\text{F}$ output capacitor. The 7.5k-2.5k divider provides a sample of the output's value to A3's negative input, closing the loop. The $0.1\mu\text{F}$ capacitor stabilizes this feedback action. Q2's zener drop allows the circuit to produce controlled outputs all the way down to 0V. This arrangement permits a 0V-2.5V input at A3 to produce a corresponding 0V-10V varactor bias. Figure 115, a spectral plot of the circuit running at 7.6MHz, shows the second harmonic down 35dB, with the third harmonic down almost 60dB. Resolution bandwidth is 3kHz.

Complete AM Radio Station

A complete microphone-to-antenna AM radio station appears in Figure 116.¹³ The carrier is generated by A1, set up as a quartz stabilized oscillator similar to the one described in Figure 111. A1's output feeds A2, functioning as a modulated RF power output stage. A2's input signal range is restricted by the bias applied to offset pins 1 and

Note 13: The construction and operation of this apparatus may require Federal Communications Commission review and/or licensing. See Appendix G for FCC licensing and application information.

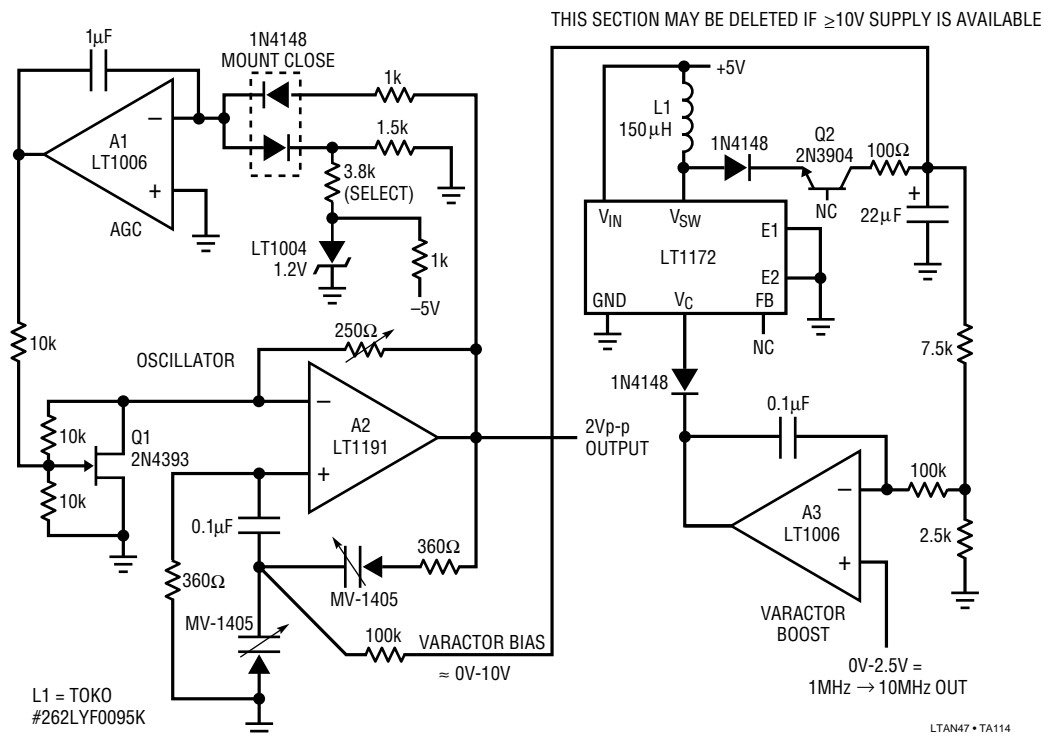


Figure 114. Varactor Tuned 1MHz-10MHz Wien Bridge Oscillator

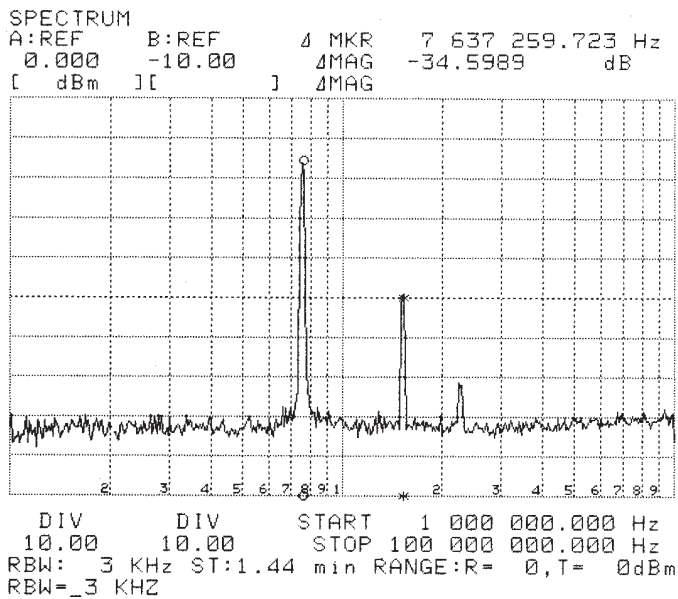


Figure 115. Spectrum Analysis for the Varactor Tuned Wien Bridge. Harmonics are at Least 34dB Down From Fundamental

8 (see LT1194 data sheet for details). A3, a microphone amplifier, supplies bias to these pins, resulting in an amplitude modulated RF carrier at A2's output. The DC term summed with the microphone biases A3's output to the appropriate level for good quality modulation characteristics. Calibration of this circuit involves trimming the

100Ω potentiometer in the oscillator for a stable 1Vp-p 1MHz A1 output.¹⁴

Figure 117 shows typical AM carrier output at the antenna. In this case the modulation is supplied by Mr. Chuck Berry, singing "Johnny Be Goode".

APPLICATIONS SECTION III - DATA CONVERSION

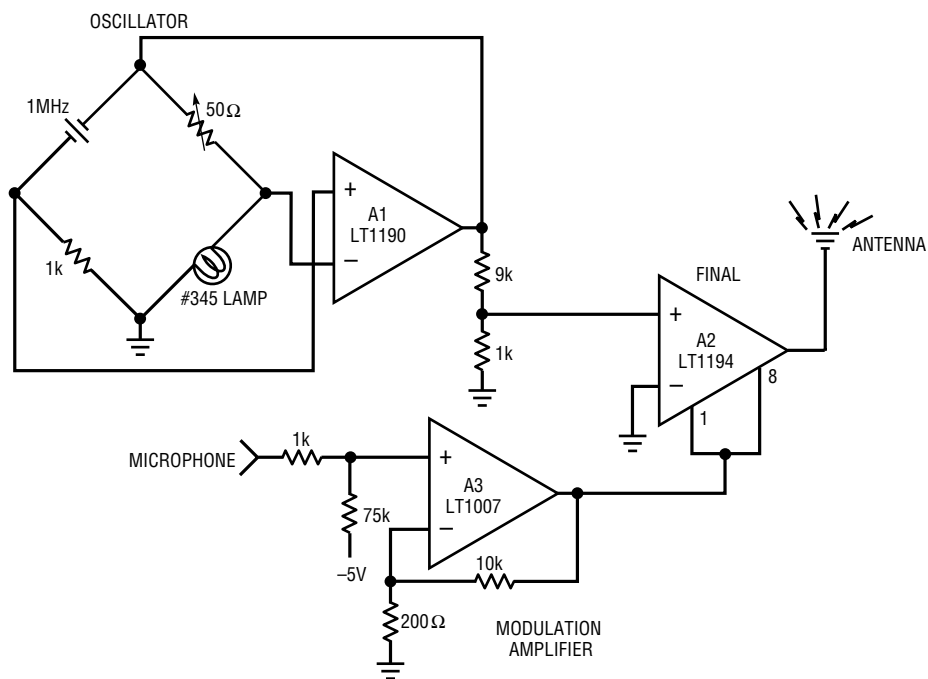
1Hz-1MHz Voltage-Controlled Sine Wave Oscillator

The oscillators presented to this point have limited frequency tuning range. Although Figure 118 is not a true oscillator, it produces a synthesized sine wave output over a wide dynamic range. Many applications such as audio, shaker table driving and automatic test equipment require voltage-controlled oscillators (VCO) with a sine wave output. This circuit meets this need, spanning a 1Hz-1MHz range (120dB or 6 decades) for a 0V to 10V input. It maintains 0.25% frequency linearity and 0.40% distortion specifications.¹⁵ To understand the circuit, assume Q5 is

Note 14: Operating frequency subject to FCC approval and assignment. See Footnote 13 and Appendix G.

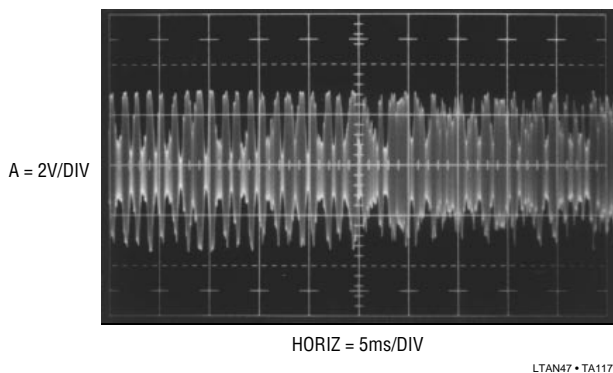
Note 15: Seasoned readers of LTC literature, a hardened corps, may recognize this and other circuits in this publication as updated versions of previous LTC applications. The partial repetition is justified based on improved specifications and/or simplification of the original circuit.

Application Note 47



LTAN47 • TA116

Figure 116. A Complete AM Radio Station. Don't Forget Your Advertisers and FCC License (See Appendix G)



LTAN47 • TA117

Figure 117. Chuck Berry Lays a Little Modulation on the 1MHz Carrier

on and its collector (Trace A, Figure 119) is at $-15V$, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 3.6k resistor and the self-biased FETs. A current, $-I$, is pulled from the summing point. A2, a precision op amp, DC stabilizes A1. A1's output (Trace B, Figure 119) integrates positive until C1's input (Trace C) crosses 0V. When this happens, C1's inverting output goes negative, the Q4-Q5 level shifter turns off, and Q5's collector goes to $+15V$. This allows Q1 to come on. The resistors in Q1's path are scaled to produce a current, $+2I$, exactly twice the absolute magnitude of the current, $-I$, being removed from the

summing node. As a result, the net current into the junction becomes $+I$ and A1 integrates negatively at the same rate as its positive excursion.

When A1 integrates far enough in the negative direction, C1's "+" input crosses zero and its outputs reverse. This switches the Q4-Q5 level shifter's state. Q1 goes off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 1MHz with a 0V-10V input. The LT1009 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's "+" input, assuring it clean recovery from overdrive.

The AD639 trigonometric function generator, biased via A4, converts A1's triangle output into a sine wave (Trace D).

The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At higher frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If these delays are not minimized, triangle amplitude will increase with frequency, causing distortion level to also increase with frequency. The total delay generated by the LT1016,

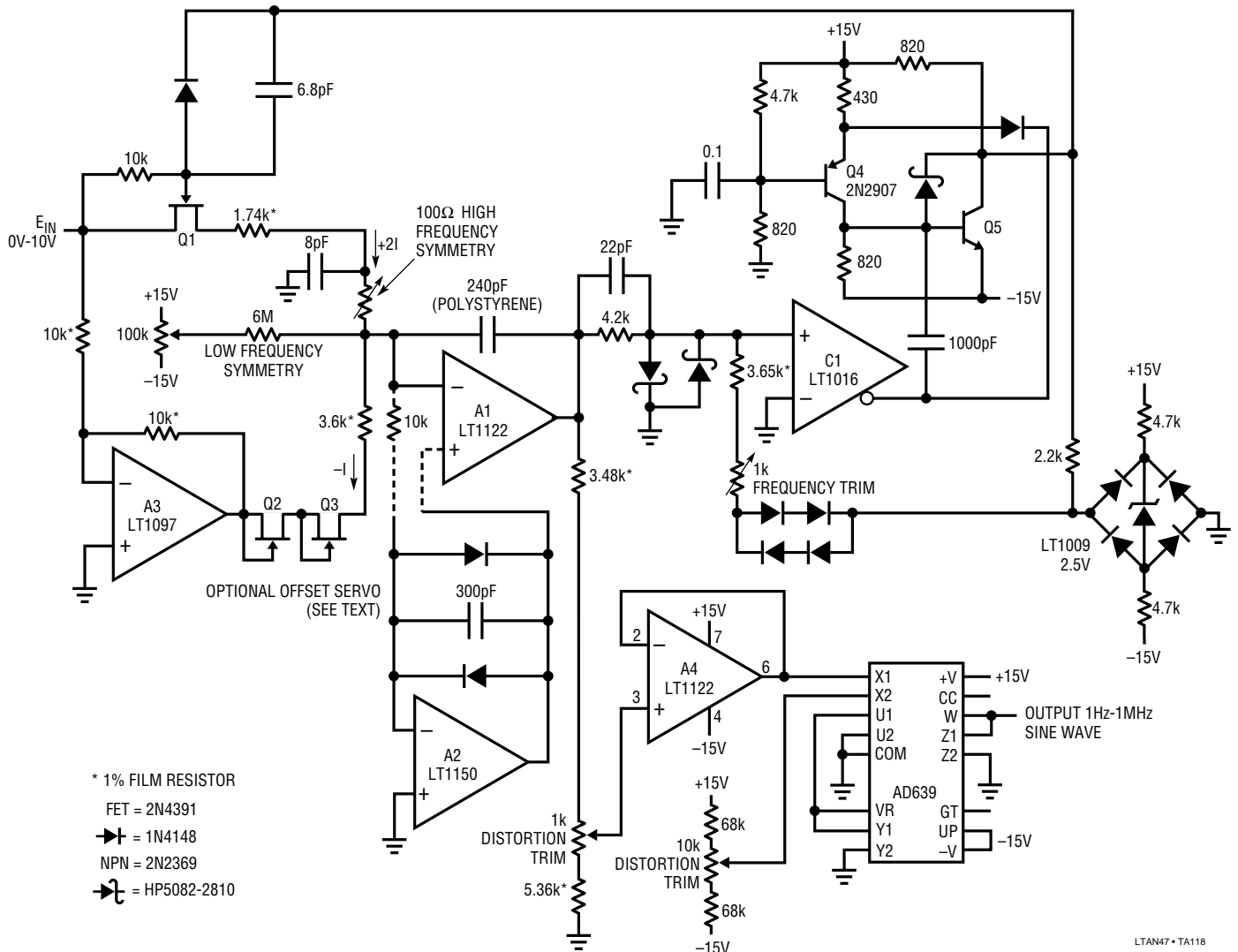


Figure 118. 1Hz-1MHz Sine Wave Output VCO Has 0.25% Linearity and 0.4% Distortion

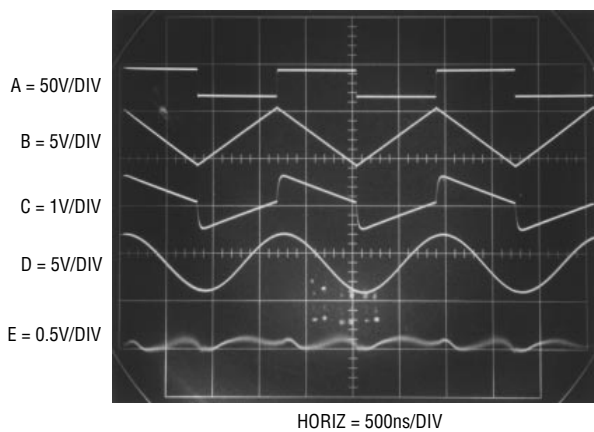


Figure 119. Sine Wave VCO Waveforms

the Q4-Q5 level shifter, and Q1 is 14ns. This small delay, combined with the 22pF feedforward network at the LT1016's input, keeps distortion to just 0.40% over the entire 1MHz range. At 100kHz, distortion is typically inside 0.2%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 8pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature-dependent on-resistance of Q1, keeping the +21/-1 relationship constant with temperature.

This circuit features extremely fast response to input changes, something most sine wave circuits cannot do.

Application Note 47

Figure 120 shows what happens when the input switches between two levels (Trace A). A1's triangle output (Trace B) shifts frequency immediately, with no glitching or poor dynamics. The sine output (Trace C), reflecting this action, is similarly clean. To adjust this circuit, put in 10.00V and trim the 100Ω pot for a symmetrical triangle output at A1.

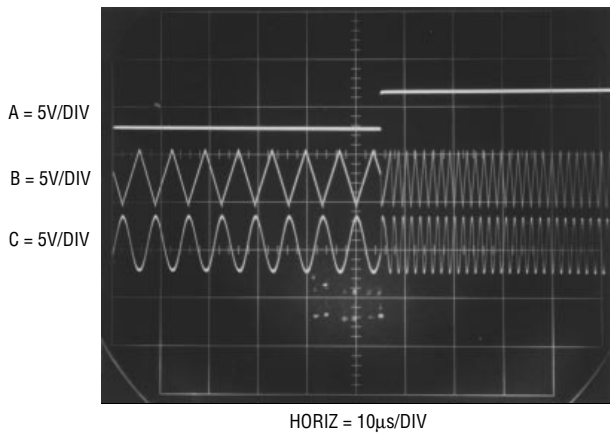


Figure 120. Sine Wave Output VCO Step Response is Quick and Clean

Next, put in 100μV and trim the 100k pot for triangle symmetry. Then, put in 10.00V again and trim the 1k frequency trim adjustment for a 1MHz output frequency. Finally, adjust the distortion trim potentiometers for minimum distortion as measured on a distortion analyzer (Trace E, Figure 119). Slight readjustment of the other potentiometers may be required to get lowest possible distortion. If operation below 100Hz is not required, the A2 based DC stabilization stage may be deleted. If this is done, A1's positive input should be grounded.

1Hz-10MHz V → F Converter

The LT1016 and the LT1122 high speed FET amplifier combine to form a high speed V → F converter in Figure 121. A variety of circuit techniques are used to achieve a 1Hz to 10MHz output. Overrange to 12MHz ($V_{IN} = 12$) is provided. This circuit has a wider dynamic range (140dB or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V → Fs. The theory of operation is based on the identity $Q = CV$.

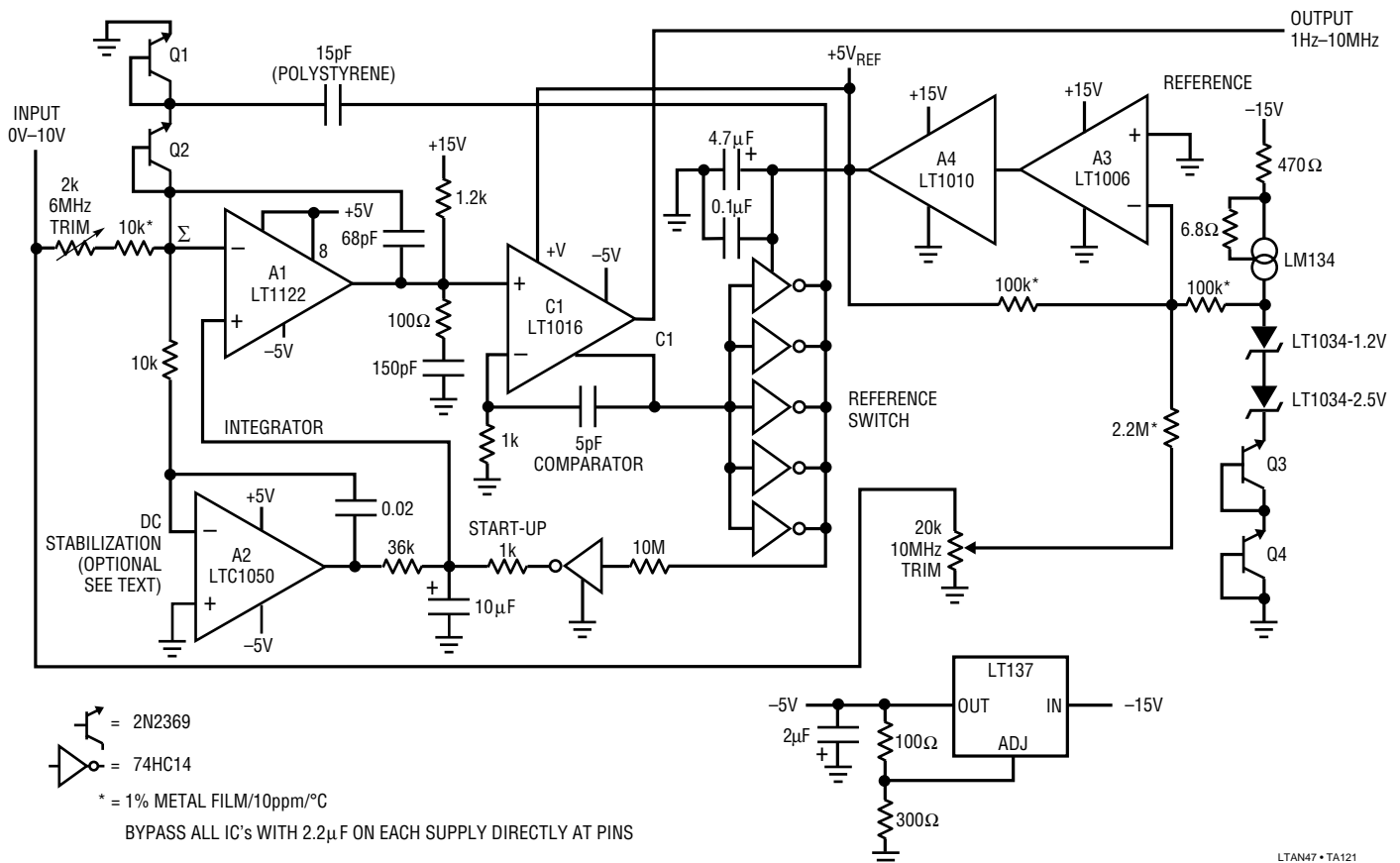


Figure 121. 1Hz-10MHz V-to-F Converter. Linearity is 0.03% with 50ppm/°C Drift

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

$0.05\mu\text{V}/^\circ\text{C}$ offset drift performance is obtained by stabilizing A1 with A2, a chopper stabilized op amp. A2 measures the DC value of the negative input, compares it to ground, and forces the positive input to maintain offset balance in A1. Note that A2 is configured as an integrator and cannot see high frequency signals. It functions only at DC and low frequency.

A1 is arranged as an integrator with a 68pF feedback capacitor. When a positive voltage is applied to the input, A1's output integrates in a negative direction (Trace A, Figure 122). During this period, C1's inverting output is low. The paralleled HCMOS inverters form a reference voltage switch. The reference voltage is established by the LM134 current source driven LT1034's and the Q3-Q4 combination. Additionally, a small input voltage related term is summed into the reference, improving overall circuit linearity. A3-A4 provides low drift buffering, presenting a low impedance reference to the paralleled inverter's supply pin. The HCMOS outputs give low resistance, essentially errorless switching. The reference switch's output charges the 15pF capacitor via Q1's path.

When A1's output crosses zero, C1's inverting output goes high and the reference switch (Trace B) goes to ground. This causes the 15pF unit to dispense charge into the summing node via Q2's V_{BE} . The amount of charge dispensed is a direct function of the voltage the 15pF unit was charged to ($Q = CV$). Q1 and Q2 are temperature compensated by Q3 and Q4 in the reference string. The current through the 15pF unit (Trace C) reflects the charge pumping action. The removal of current from A1's summing junction (Trace D) causes the junction to be driven very quickly negative. The initial negative-going 15ns

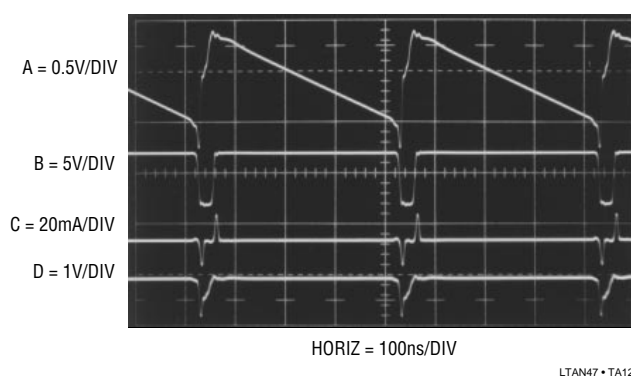


Figure 122. 10MHz V-to-F's Operating Waveforms. LT1122 Integrator is Completely Reset in 60ns

transient at A1's output is due to amplifier delay. The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (Trace A) slew limits as it attempts to regain control of the summing node. The class A $1.2\text{k}\Omega$ pull-up and the RC damper at A1's output minimizes erroneous output movement, enhancing this slew recovery. The amount of time the reference switch remains at ground depends on how long it takes A1 to recover and the 5pF - 1000Ω hysteresis network at C1. This 60ns interval is long enough for the 15pF unit to fully discharge. After this, C1 changes state, the reference switch swings positive, the capacitor is recharged and the entire cycle repeats. The frequency at which this oscillation occurs is directly related to the voltage-input-derived current into the summing junction. Any input current will require a corresponding oscillation frequency to hold the summing point at an average value of 0V .

Maintaining this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to achieving 10MHz full-scale operating frequency is the ability to transmit information around the loop as quickly as possible. The discharge-reset sequence is particularly critical and is detailed in Figure 123. Trace A is the A1 integrator output. Its ramp output crosses 0V at the first left vertical graticule division. A few nanoseconds later, C1's inverting output begins to rise (Trace B), switching the reference switch to ground (Trace C). The reference switch begins to head towards ground about 16ns after A1's output crosses 0V . 2ns later, the summing point (Trace D) begins to go negative as current is pulled from it through the 15pF capacitor. At 25ns , C1's inverting

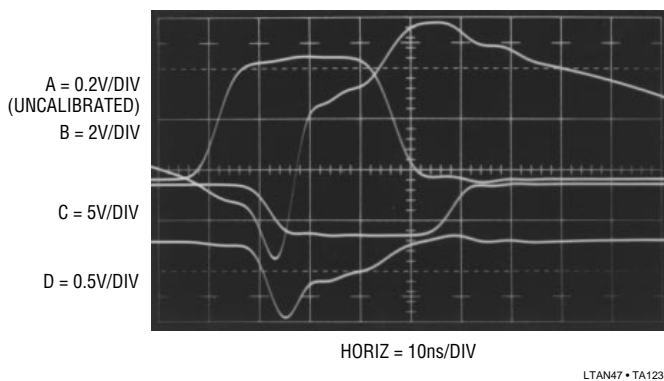


Figure 123. Detail of 60ns Reset Sequence (Whoosh!)

output is fully up, the reference switch is at ground, and the summing point has been pulled to its negative extreme. Now, A1 begins to take control. Its output (Trace A) slews rapidly in the positive direction, restoring the summing point. At 60ns, A1 is in control of the summing node and the integration ramp begins again.

Start-up and overdrive conditions could force A1's output to go to the negative rail and stay there. The AC-coupled nature of the charge dispensing loop can preclude normal operation and the circuit may latch. The remaining HCMOS inverter provides a watchdog function for this condition. If A1's output rails negative the reference switch tries to stay at ground. The remaining inverter goes high, lifting A1's positive input. This causes A1's output to slew positive, initiating normal circuit action. The 1k-10 μ F combination and the 10M-inverter input capacitance limit start-up loop bandwidth, preventing unwanted outputs.

The LM134 current source driving the reference string has a built in 0.33%/ $^{\circ}$ C thermal coefficient, causing slight voltage modulation in the Q3-Q4 pair over temperature. This small change ($\approx +120$ ppm/ $^{\circ}$ C) opposes the -120 ppm/ $^{\circ}$ C drift in the 15pF polystyrene capacitor, aiding overall circuit tempo.

To trim this circuit, apply exactly 6V at the input and adjust the 2k Ω potentiometer for 6.000MHz output. Next, put in exactly 10V and trim the 20k unit for 10.000MHz output. Repeat these adjustments until both points are fixed. A2's low drift eliminates a zero adjustment. If operation below 600Hz is not required, A2 and its associated components may be deleted.

Linearity of this circuit is 0.03% with full-scale drift of 50ppm/ $^{\circ}$ C. Zero point error, controlled by A2, is 0.05Hz/ $^{\circ}$ C.

8-Bit, 100ns Sample-Hold

Figure 124 shows a simple, very fast sample-hold circuit. This circuit will acquire a ± 5 V input to 8-bit accuracy in 100ns. Hold step is inside 1/4 LSB with hold settling inside 25ns. Aperture time is 4ns and droop rate about 1/2 LSB/ μ s.

The input is fed to a Schottky switching bridge via inverting buffer A1. The Schottky bridge, similar to types used in sampling oscilloscopes¹⁶, gives 1ns switching and eliminates the charge pump-through that a FET switch would contribute. The switching bridge's output feeds output amplifier A2. A2, configured as an integrator, is the actual hold amplifier. Its output is fed back to the switching bridge's input, forming a summing point with A1's output resistor. This feedback loop places the bridge within a loop, enhancing accuracy.

The bridge is switched by driving the sample-hold input line. Q1 and Q2 drive L1's primary. L1's secondaries provide complementary drive to the bridge with almost no time skewing.

Figure 125 shows the circuit acquiring a full scale step. Trace A is the input command while Trace B is A2's output. The aberration visible in A2's output when switching into hold (hold step) is due to minute residual AC imbalances in the bridge. Figure 126 studies this effect in high resolution detail, with the hold step trim deliberately disconnected. After A2's output nominally settles at final value, the circuit is switched into hold. The bridge imbalance allows a small parasitic charge to be displaced into A2's summing point, causing A2 to step 10mV higher (in this case). If the trim is connected and properly adjusted, it supplies a small compensatory charge during switching. Figure 127 shows the effect of this on the output. The settled hold output is the same as the acquired value. To trim this circuit, ground the input while pulsing the sample-hold control line. Next, adjust the trim for minimal amplitude step between the sample and hold states.

In contrast to low frequency sample-hold circuits this design cannot pass signal if left in the sample mode. The transformer's inherent AC coupling precludes such operation. Similarly, extended sample mode duration (e.g., >500ns) will cause transformer saturation, resulting in erroneous outputs and excessive Q1-Q2 dissipation. If

Note 16: See References 7, 8 and 28.

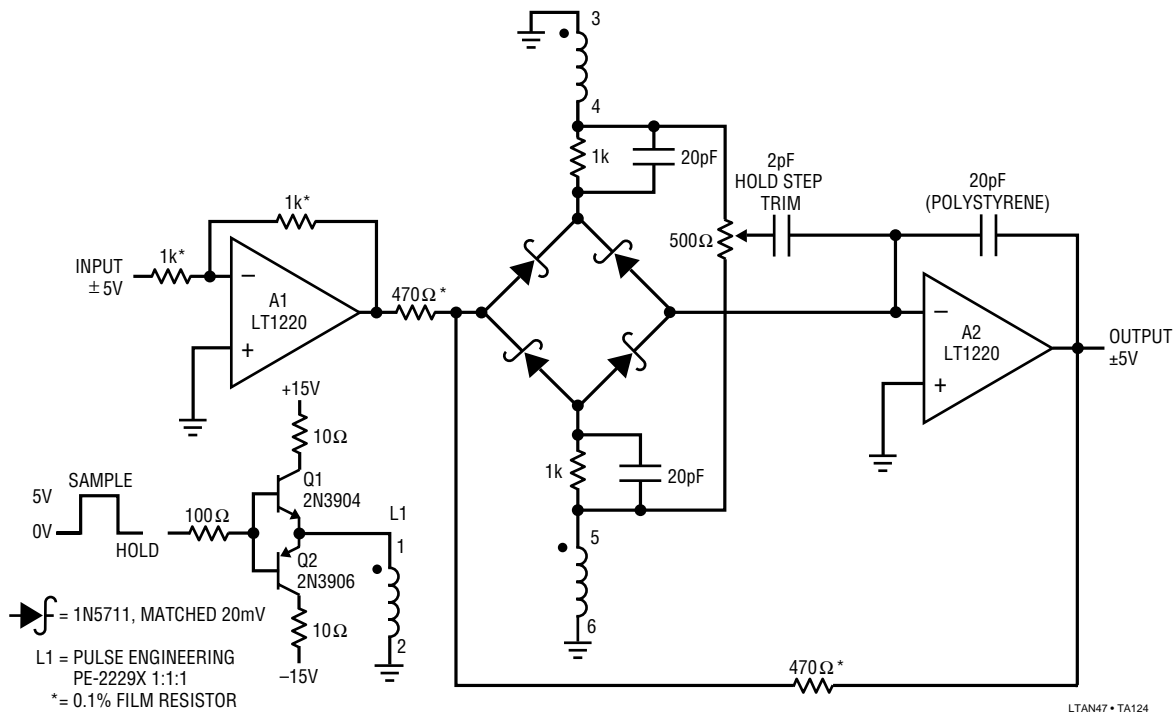


Figure 124. 8-Bit, 100ns Sample-Hold

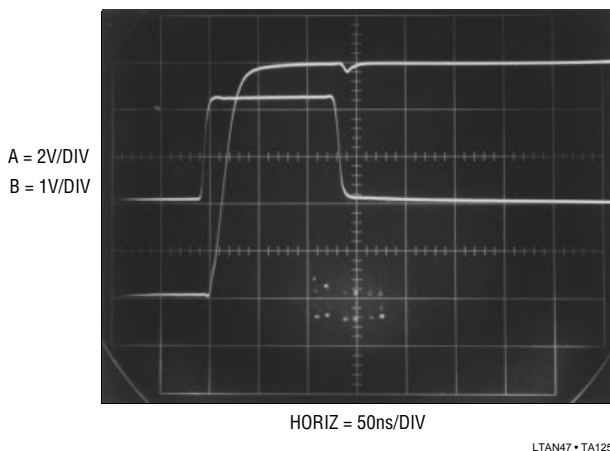


Figure 125. Fast Sample-Hold Acquiring a Full-Scale Input

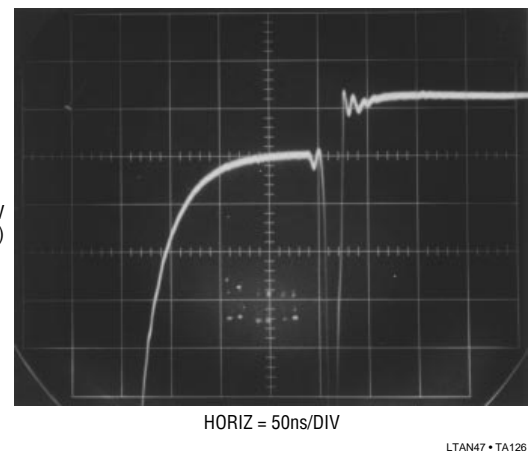


Figure 126. Hold Step with Mis-Adjusted Compensation

extended logic high durations are possible at the control input, it should be AC coupled.

15ns Current Summing Comparator

Figure 128 shows a way to build a high speed current comparator with resolution in the 12-bit range. Current comparison, the fastest way to compare D→A outputs and analog values, is commonly used in high speed A→D converters and instrumentation. A1 is set up as a Schottky bounded amplifier. The bound diodes prevent A1 from

saturation due to excessive summing point overdrive, aiding response time. The 3pF capacitor, a typical value, compensates DAC output capacitance and is selected for best amplifier damping. The 10k feedback resistor, also typical, is chosen for best gain-bandwidth performance. Voltage gains of 4 to 10 are common. Figure 129 shows output performance. Trace A, a test input, causes A1's output (Trace B) to slew through zero (screen center horizontal line). When A1 crosses zero, C1's input biases negative and it responds (C1's output is Trace C) 10ns later with a TTL

Application Note 47

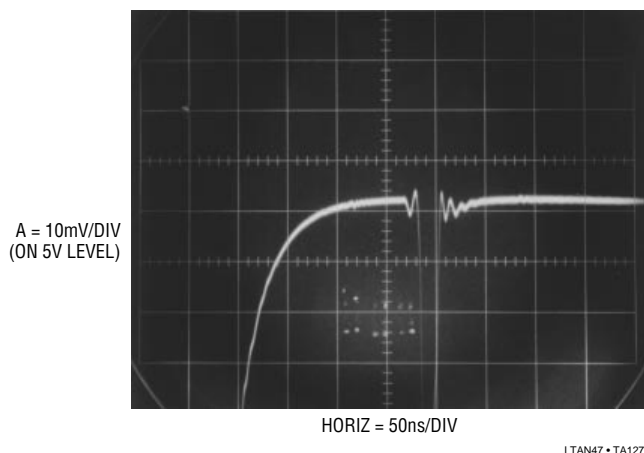


Figure 127. Hold Step with Properly Adjusted Compensation

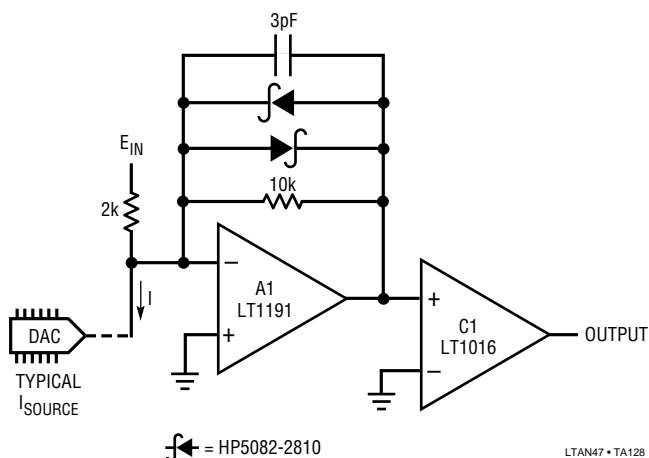


Figure 128. Fast Summing Comparator

output. Total elapsed time from the test input arriving at a TTL high until the comparator output achieves a TTL high is inside 15ns.

50MHz Adaptive Threshold Trigger Circuit

Figure 130 is an extremely versatile trigger circuit. Designing a fast, stable trigger is not easy and often entails a considerable amount of discrete circuitry. This circuit reliably triggers from DC-50MHz over a 2mV-300mV input range with no level adjustment required.

A1, a gain of ten preamplifier, feeds an adaptive trigger configuration identical to the one described in Figure 97's fiber optic receiver. The adaptive trigger maintains the A3 output comparator's trip point at 1/2 input signal amplitude, regardless of its magnitude. This insures reliable automatic triggering over a wide input amplitude range, even for very low level inputs. As an option, the network

shown in dashed lines permits changing the trip threshold. This allows any point on the input waveform edge to be selected as the actual trigger point.¹⁷

Figure 131 shows performance for a 40MHz input sine wave (Trace A). A1's output (Trace B) takes gain and the A3 comparator gives a clean logic output (Trace C). At the highest frequencies, any bandwidth limiting in A1 is irrelevant; the adaptive trigger threshold will simply vary ratiometrically to maintain circuit output.

Fast Time-to-Height (Pulsewidth-to-Voltage) Converter

The circuit of Figure 132 allows very short pulsewidths (in this case 250ns full-scale) to be determined to a typical accuracy of 1%. Digital methods of achieving similar results dictate clock speeds of 1GHz, which is cumbersome. In addition, processor based approaches using averaging techniques require repetitive pulses which this circuit does not. Circuits of this type are frequently required in automatic test equipment and nuclear and high energy physics work where determination of short pulsewidths is a common requirement.

The circuit functions by charging a capacitor during the period of a pulsewidth. When the pulse ends, charging ceases and the voltage across the capacitor is proportional to the width of the pulse.

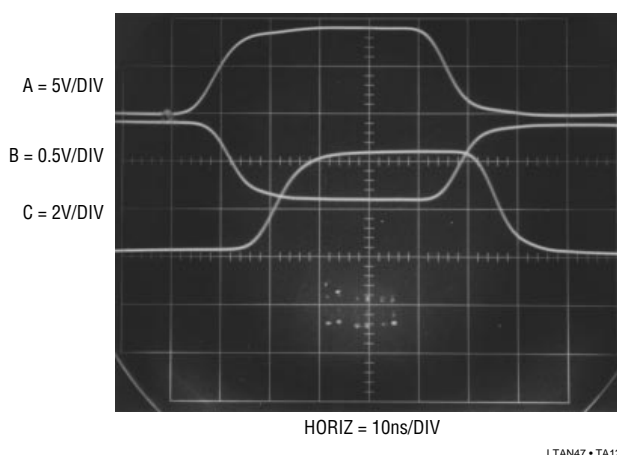


Figure 129. Fast Summing Comparator's Waveforms. Total Delay is 15ns

Note 17: This technique is borrowed from oscilloscope trigger circuitry. See Reference 29.

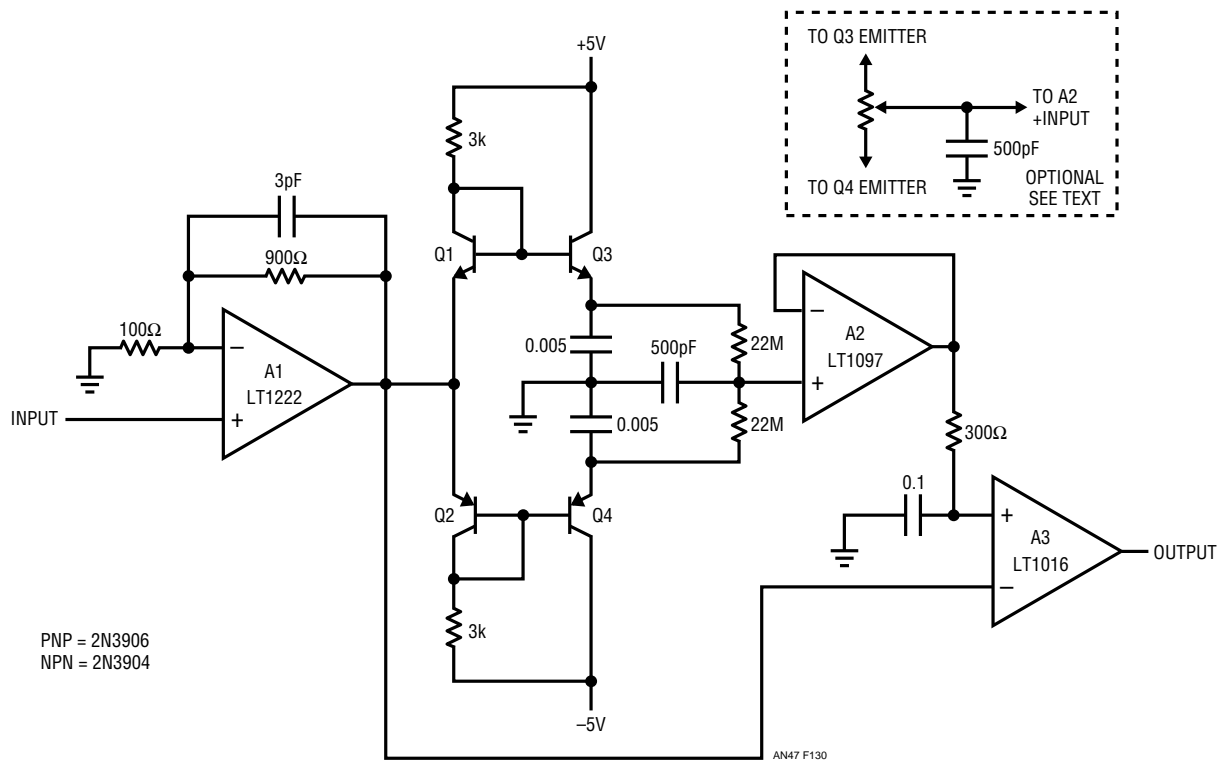


Figure 130. 50MHz Trigger with Adaptive Threshold

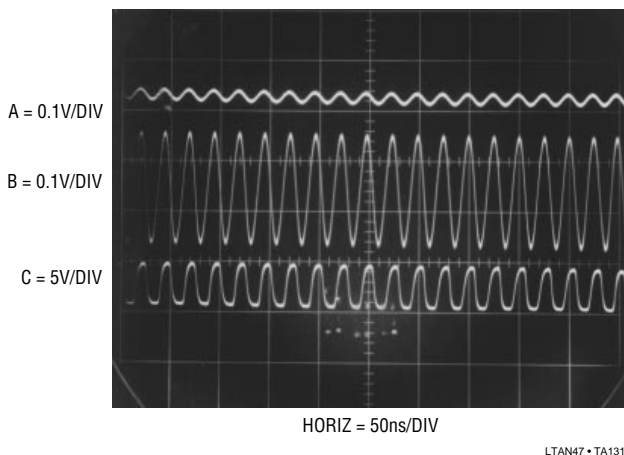


Figure 131. The Trigger Responds to a 40MHz Input. Input Amplitude Variations from 2mV-300mV Have No Effect

The input pulse to be measured (Trace A, Figure 133) simultaneously biases the 74C221 dual one shot and Q3. Q3, aided by Baker¹⁸ clamping, capacitive feedforward and optimized DC base biasing, turns off in a few nanoseconds. Current source Q2's emitter forward biases and Q2

supplies constant current to the 100pF integrating capacitor. Q1 supplies temperature compensation for Q2, with the 2.5V LT1009 referencing the current source. Q2's collector (e.g., the 100pF capacitor) charges in ramp fashion (Trace B). A1 supplies a buffered output (Trace C). When the input pulse ends, Q3 rapidly turns on, reverse biasing Q2's emitter and turning off the current source. A1's voltage is directly proportional to the input pulse width. A monitoring A → D converter can acquire this data.

After a time set by the 74C221's RC programmed delay, a pulse appears at its Q2 output (Trace D). This pulse turns on Q4, discharging the 100pF capacitor to zero and readying the circuit for the next input pulse.

This circuit's accuracy and resolution are crucially dependent on minimizing delay in switching the Q1-Q2 current source. Figure 134 provides amplitude and time expanded versions of critical circuit waveforms. Trace A is the input pulse and Trace B is A1's input, showing the beginning of the ramp's ascent. Trace C, A1's output, shows about 13ns delay from A1's input. Traces D and E, A1's input and

Note 18: See Reference 45.

Application Note 47

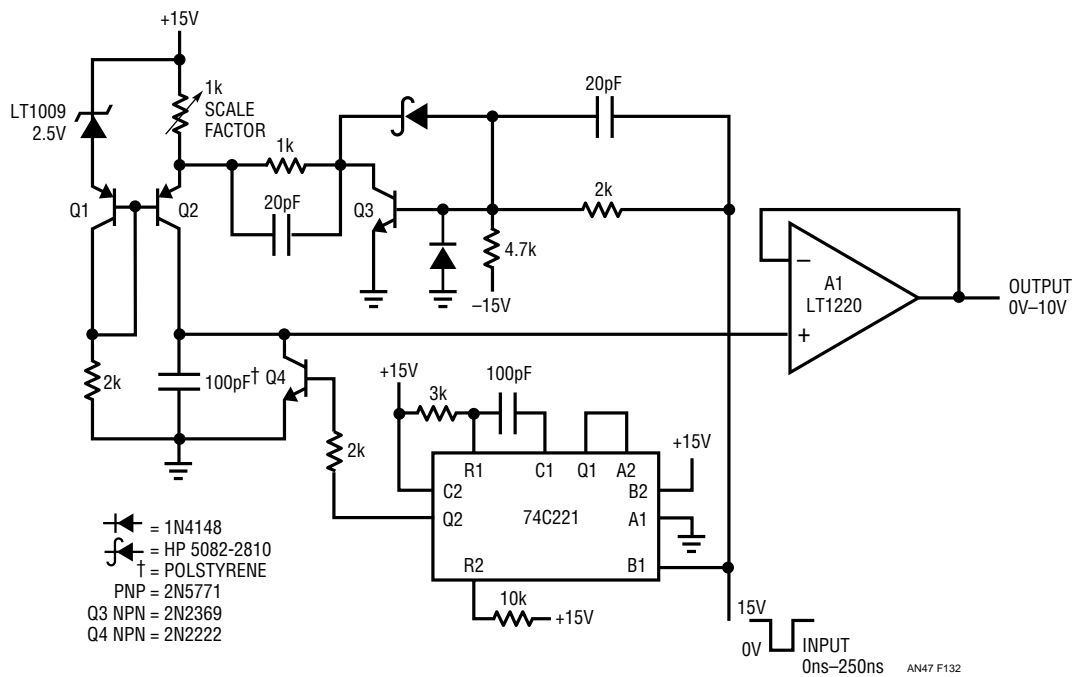


Figure 132. Fast Time-to-Height Converter

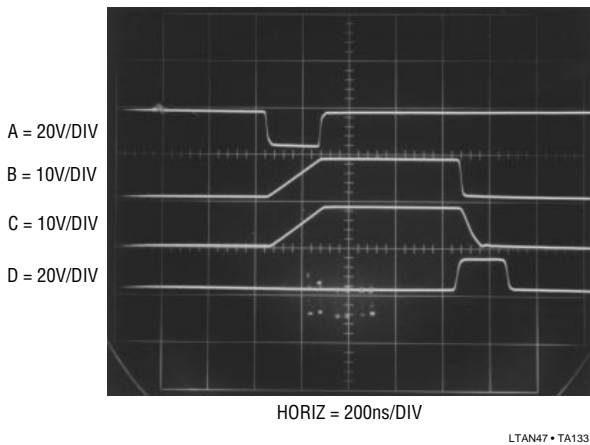


Figure 133. Time-to-Height Converter Acquires a 250ns Pulse

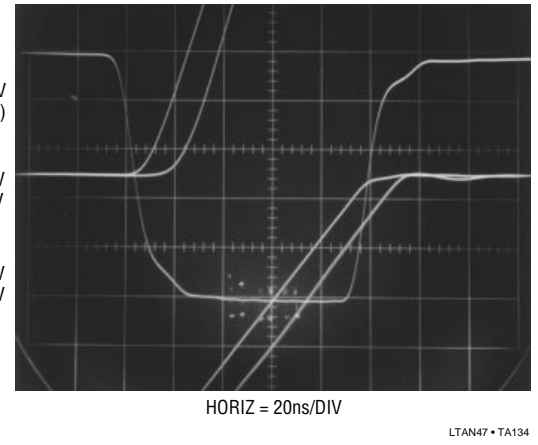


Figure 134. Detail of Time-to-Height Converter's Ramp Switching

output respectively, record similar A1 delays for ramp turn-off. The photo reflects the extremely fast current source switching; the vast majority of delay is due to A1's delay. A1's delay is far less critical than current source switching delays; A1 will always settle to the correct value well before the one shot resets the circuit. In practice, a monitoring A → D converter should not be triggered until about 50ns after the circuit's input pulse has ceased. This gives A1 plenty of time to catch up to the 100pF capacitor's settled value.

As mentioned, current source switching speed is essential for good results. Figure 135 details current source turn off. Trace A is the circuit's input pulse rising edge and Trace B shows the top of the ramp. Turn off occurs in a few nanoseconds. Similar speed is characteristic of the input's falling edge (current source turn on). Additionally, it is noteworthy that circuit accuracy and resolution limits are set by the *difference* in current source turn on and off delays. As such, the *effective* overall delay is extremely small.

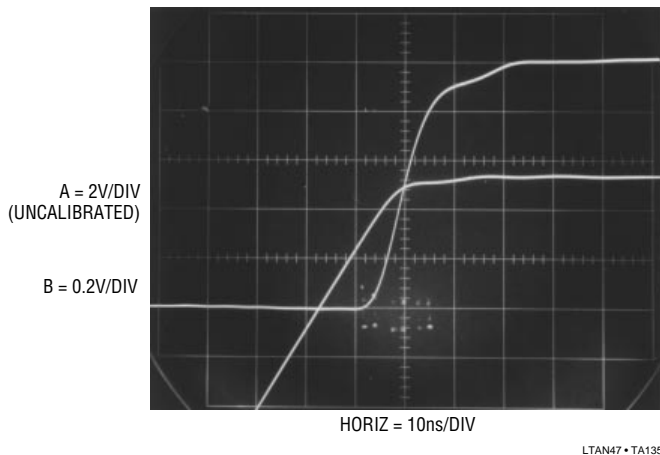


Figure 135. Current Source Turn-Off Detail for the Time-to-Height Converter

To calibrate this circuit, put in a 250ns width pulse and trim the 1k Ω potentiometer for 10V output. The circuit will convert pulse widths from 20ns to 250ns to a typical accuracy of 1%. The 20ns minimum measurable width is due to inability to fully discharge the 100pF capacitor. If this is objectionable, Q4 can be replaced with a lower saturation device or A1's output can be offset.

True RMS Wideband Voltmeter

Most AC RMS measurements use logarithmic techniques to compute the waveform's RMS value. This method limits bandwidth to below 1MHz and crest factor performance to about 10:1. Practically speaking, a waveform's RMS value is defined as its heating value in the load. Specialized instruments employ thermally based assemblies that compute the RMS value of the input. The thermal method provides substantially improved bandwidth and crest factor capability compared to logarithmically based converters.

Thermal RMS-DC converters are direct acting, thermo-electronic analog computers. The thermal technique is explicit, relying on first principles. The simple operation permits wideband performance unattainable with implicit, indirect methods based on logarithmic computing.

Figure 136 shows a classic scheme for implementing a thermally based RMS-DC converter. Here, the DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal

interaction is non-linear, the input-output voltage relationship is linear with unity gain. The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier will reject this common-mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range. Figure 136's output is linear because the matched thermal pair's non-linear voltage-temperature relationships cancel each other.

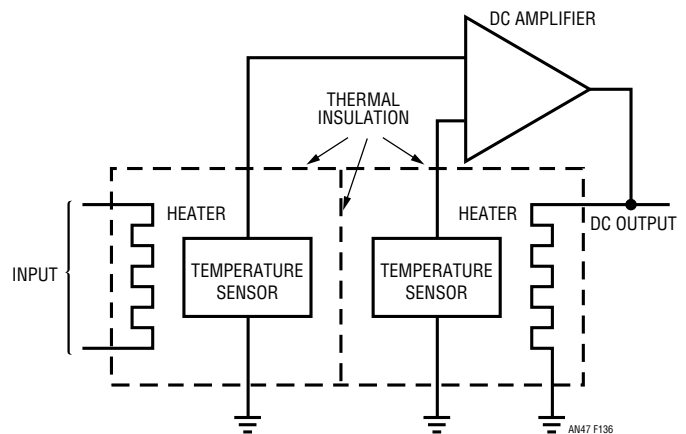


Figure 136. Conceptual Thermal RMS-DC Converter

The advantages of this approach have made its use popular in thermally based RMS-DC measurements. Typically, the assembly is composed of matched heater resistors, sensors and thermal insulation. These assemblies are relatively large and expensive to produce. Figure 137's economical wideband thermally based voltmeter is based on a monolithic thermal converter. The LT1223 provides gain, and drives the LT1088 RMS-DC thermal converter.¹⁹ The LT1088's temperature sensing diodes are biased from the supply. A1, set up as a differential servo amplifier with a gain of 9000, extracts the diode's difference signal and biases Q1. Q1 drives one of the LT1088's heaters, completing a loop. The 3300pF capacitor gives a stable roll-off.

Note 19: Complete details on this device and a discussion on thermal conversion considerations are found in Reference 40.

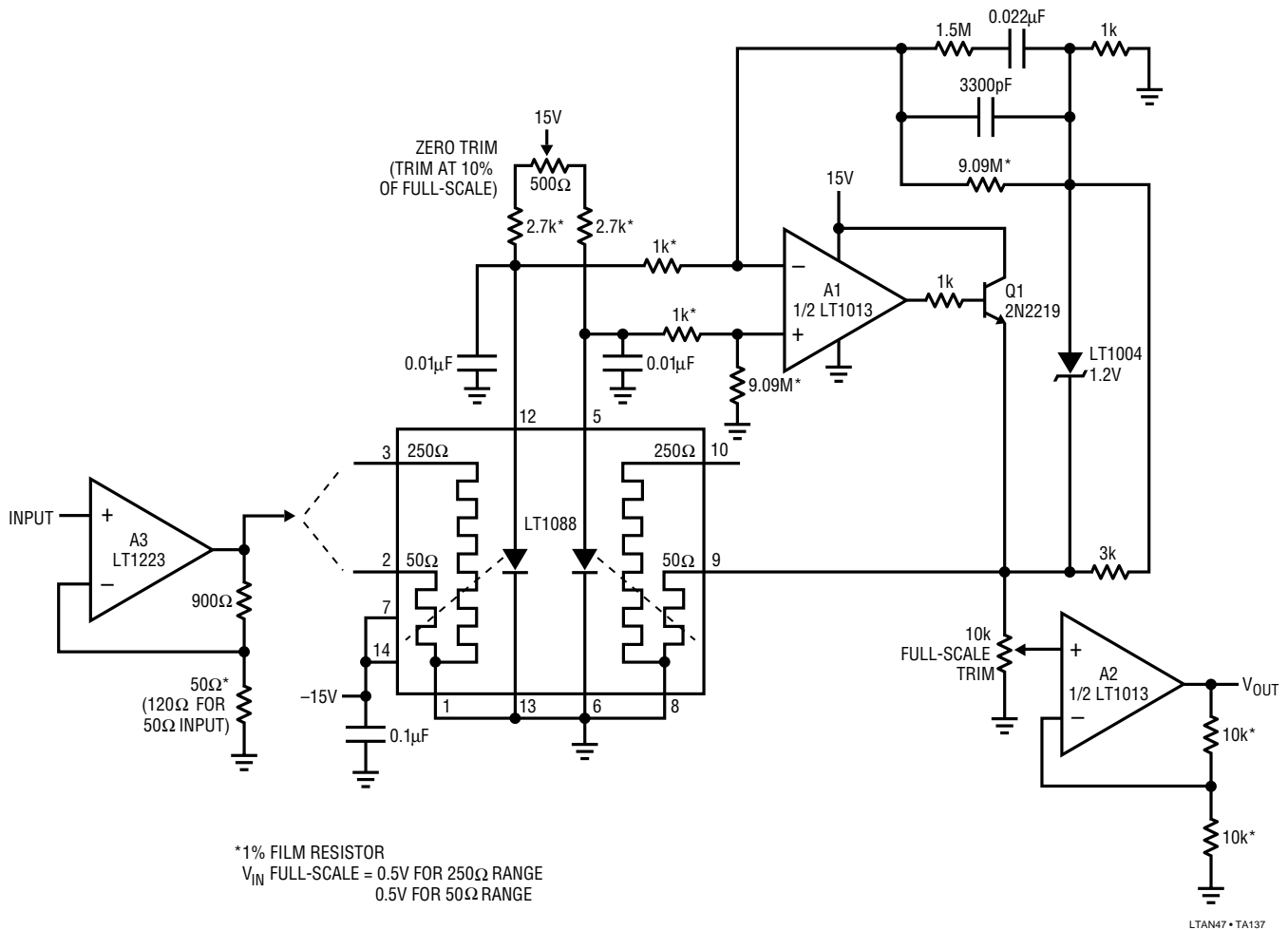


Figure 137. Wideband True RMS Voltmeter

The 1.5M-0.022μF combination improves settling by reducing gain during output slew. The LT1088's square-law thermal gain means overall loop gain is lower for small inputs. Normally, this would result in slow settling for values below about 10%-20% of scale. The LT1004 1k-3k network is a simple breakpoint, boosting amplifier gain in this region to improve settling. A2, a gain trimmable output stage, serves to compensate for gain variations in the two sides of the LT1088. To trim the circuit, put in about a 10% scale DC signal (e.g., 0.05V). Adjust the zero trim so that $V_{OUT} = V_{IN}$. Next, apply a full-scale DC input and set the full-scale trim to that value at the output. Repeat the trims until both are fixed well within 1% of full-scale. An alternate trim scheme involves applying no input, grounding Q1's base and setting the zero trim until A1's output is active. Then, unground Q1's base, apply a full-scale input and trim the full-scale adjustment for that value at the output.

Figure 138 is a plot of error vs input frequency. The LT1088 is specified at 2% to 100MHz (50Ω heater) or 1% to 20MHz (250Ω heater). As such, most of the error shown is due to bandwidth restrictions in A3, but performance is still impressive. The plots include data taken at various input levels into both heaters. A 500mV input into 250Ω dips to 1% at 8MHz and 2.5% at 14MHz before peaking badly beyond 17MHz. This input level forces a 9.5 V_{RMS} output at A3, introducing large signal bandwidth limitations. The 400mV input to the 250Ω heater shows essentially flat results to 20MHz, the LT1088's 250Ω heater specification limit.

The 50Ω heater provides significantly wider bandwidth, although A3's 50mA output limits maximum input to about 100mV_{RMS} (1.76V_{RMS} at the LT1088).

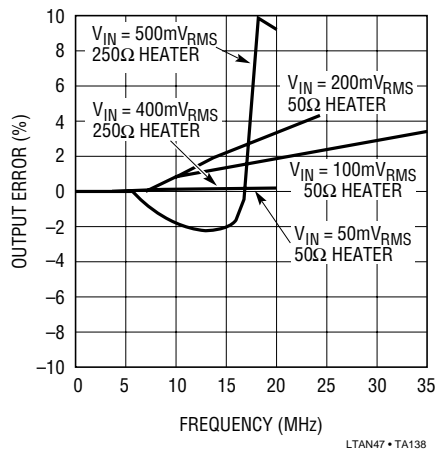


Figure 138. Accuracy Plot for the RMS Voltmeter

APPLICATIONS SECTION IV - MISCELLANEOUS CIRCUITS

RF Leveling Loop

Figure 137's wideband AC conversion can be applied in other areas. A common RF requirement is to stabilize the amplitude of a waveform against variations in input, time and temperature. Instruments and transmitters frequently require this function, which is not easy if waveform purity must be maintained. Figure 139A shows a 25MHz RF leveling loop. The RF input is applied to the AD539 wideband multiplier. The multiplier's output drives A1. A1's output is converted to DC by the LT1088 based RMS-DC converter (see previous circuit). A servo amplifier compares this output with a settable DC reference and biases the multiplier's control channel, completing a loop. The 0.33 μ F capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo. The loop maintains the output's 25MHz RMS amplitude at the DC reference's value. Changes in load, input, power supply and other variables are rejected.

Figure 139B, a similar circuit, offers significantly lower cost although performance is not quite as good. The RF input is applied to LT1228 A1, an operational transconductance amplifier. A1's output feeds LT1228 A2, a current feedback amplifier. A2's output, the circuit's output, is sampled by the A3 based gain control configuration. This arrangement, similar to the gain control loops described in Figures 112 and 114, closes a gain control loop back at A1. The 4pF capacitor compensates rectifier diode

capacitance, enhancing output flatness vs frequency. A1's I_{SET} input current controls its gain, allowing overall output level control. This approach to RF leveling is simple and inexpensive, although output drift, distortion and regulation are somewhat higher than in the previous circuit.

Voltage Controlled Current Source

Figure 140 shows a voltage controlled current source with load and control voltage referred to ground. This simple, powerful circuit produces output current in accordance with the sign and magnitude of the control voltage. The circuit's scale factor is set by resistor R. A1, biased by V_{IN} , drives current through R (in this case 10 Ω) and the load. A2, sensing differentially across R, closes a loop back to A1. The load current is constant because A1's loop forces a fixed voltage across R. The 2k-100pF combination sets roll off and the configuration is stable. Figure 141 shows dynamic response. Trace A is the voltage control input while Trace B is the output current. Response is quick and clean, with delay of 5ns and no slew residue or aberration.

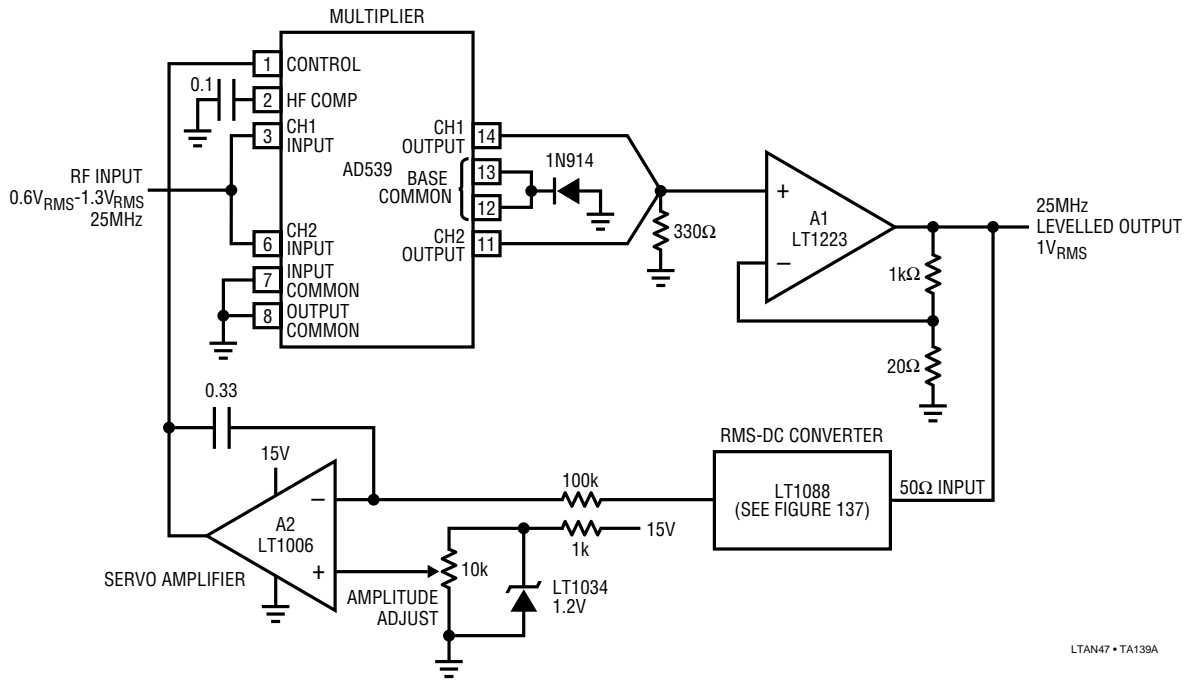
High Power Voltage Controlled Current Source

Figure 142 is identical to the basic current source, except that it adds a 1A booster stage (adapted from Figure 104) for increased output power. Including the booster inside A1's feedback loop eliminates its DC errors. Note that the booster's current limiting features have been removed, because of this circuit's inherent current limiting nature of operation. Figure 143 shows this circuit's response to be as clean as the lower power version, although delay is about 20ns slower. It is worth mentioning that the loop stability considerations involved in placing A2 and the booster in A1's feedback path are significant. This circuit receives treatment in Appendix C, "The Oscillation Problem - Frequency Compensation Without Tears".

18ns Circuit Breaker

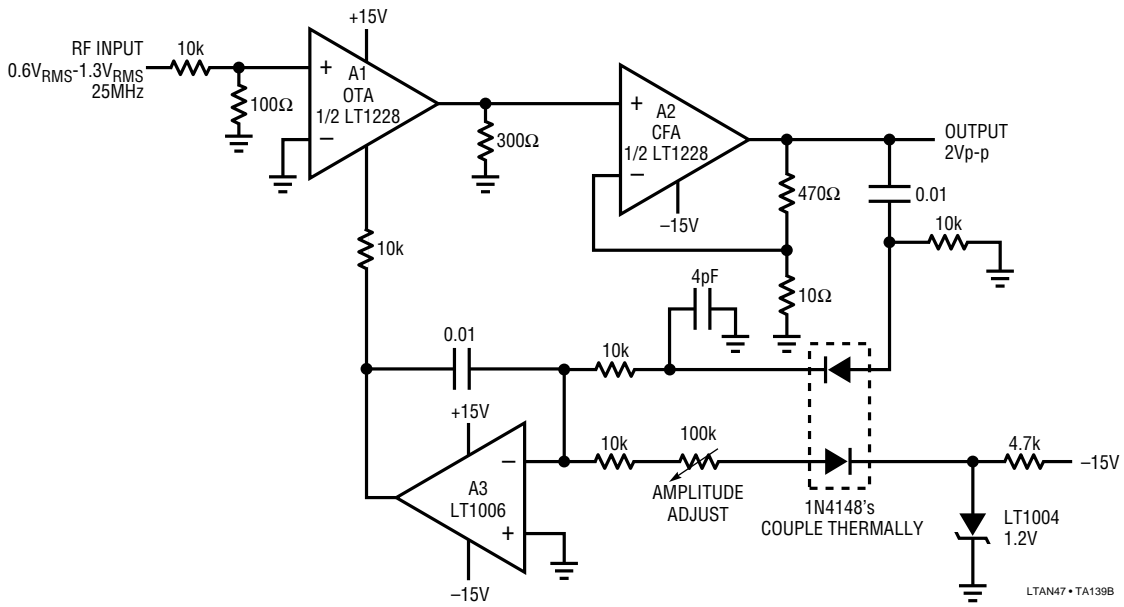
Figure 144 shows a simple circuit which will turn off current in a load 18ns after it exceeds a preset value. This circuit has been used to protect integrated circuits during developmental probing and is also useful for protecting expensive loads during trimming and calibration. The circuit's versatility is enhanced because one side of the load is grounded. Under normal conditions, Q1's emitter (Trace A, Figure 145, is Q1's current, and Trace C is its

Application Note 47



LTAN47 • TA139A

Figure 139A. RF Leveling Loop



LTAN47 • TA139B

Figure 139B. Simple RF Leveling Loop

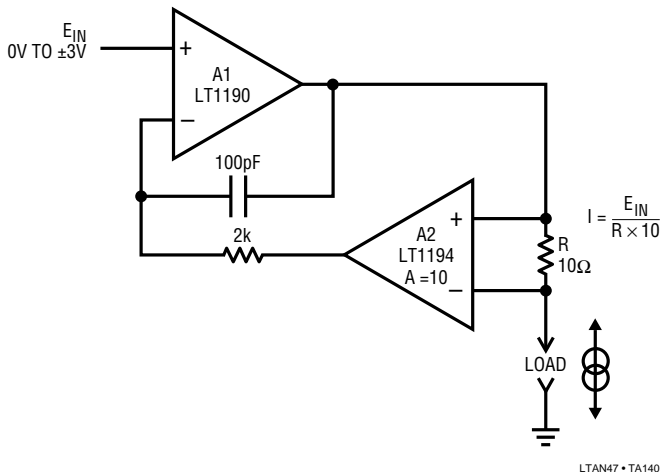


Figure 140. Fast, Precise, Voltage Controlled Current Source with Grounded Load

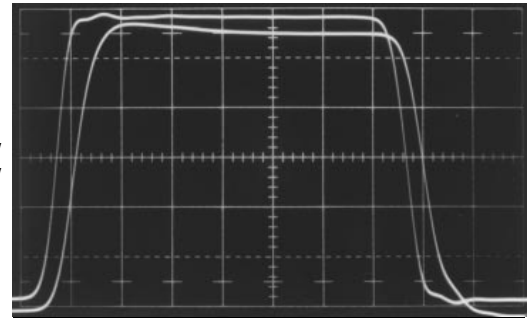


Figure 141. Dynamic Response of the Current Source. Delay is 4ns, with Clean Settling

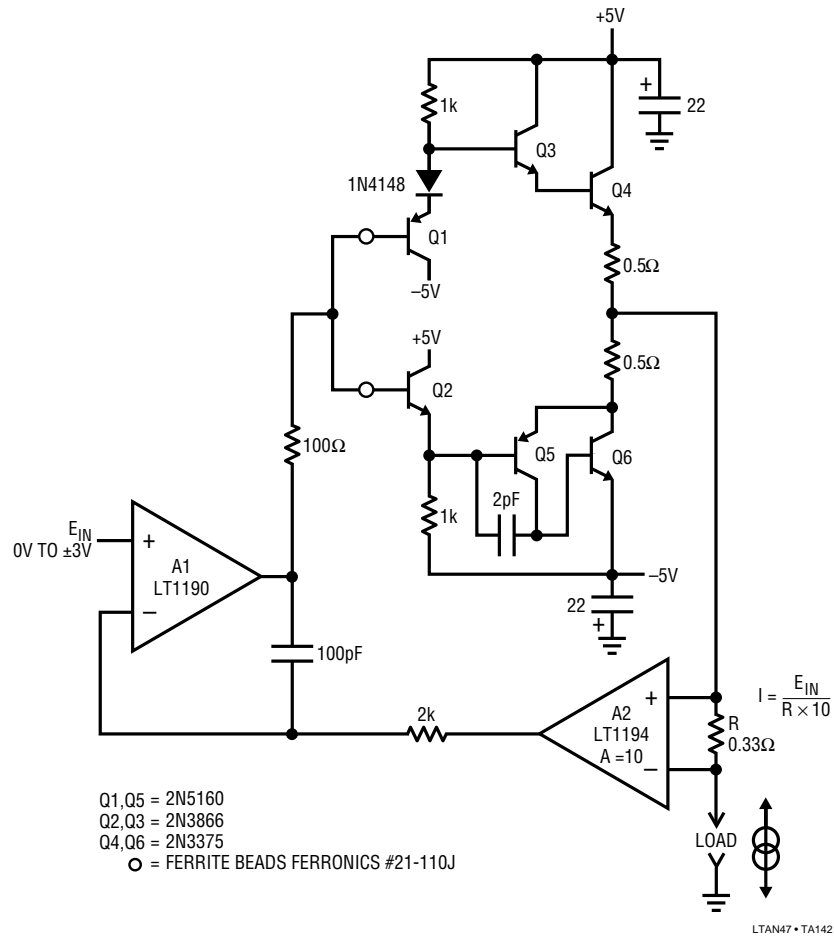


Figure 142. High Power, Wideband Voltage Controlled Current Source

Application Note 47

voltage) is biased on, supplying power to the load via the 10Ω current shunt. Differential amplifier A1's output resides below comparator A2's voltage programmed trip point and Q2 is off. When an overload occurs, Q1's emitter current begins to increase (Trace A, just prior to the third vertical division). A1's output (Trace B) begins to rise as it tracks the increase in the 10Ω shunt's voltage. The 9k-1k dividers keep A1 inputs inside their common-mode range. Simultaneously, Q1's emitter voltage (Trace C) begins to drop as it beta limits. When A1's version of the load current exceeds A2's trip point, A2 (Trace D) goes high, turning on Q2. Q2's turn on steals Q1's base drive, turning off the load

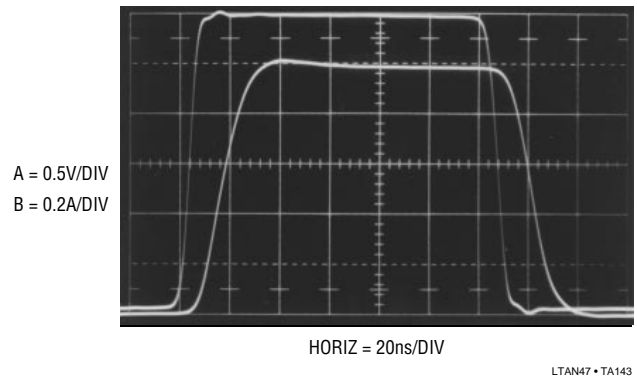


Figure 143. 1A Pulse Response of the High Power Current Source

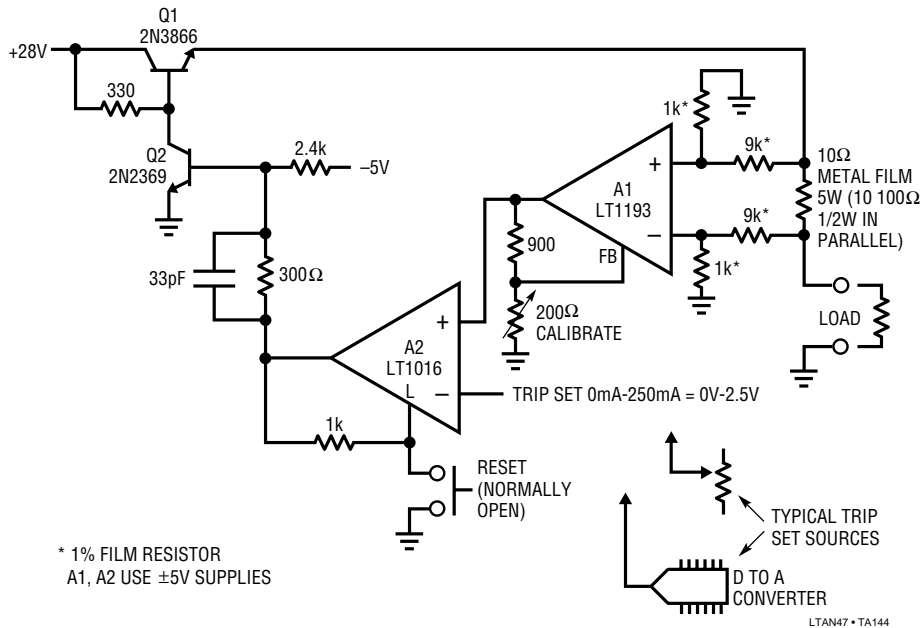


Figure 144. 18ns Circuit Breaker with Voltage Programmable Trip Point

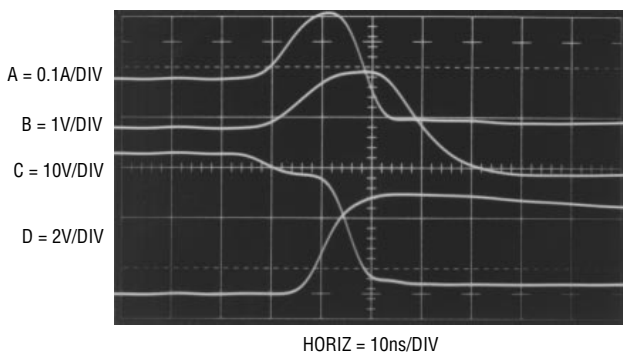


Figure 145. Operating Waveforms for the 18ns Circuit Breaker. Circuit Output (Trace C) is Shut Down 18ns After Output Current (Trace A) Begins to Rise

current. Local positive feedback at A2's latch pin causes it to latch in this off state. When the load fault has been cleared, the pushbutton can be used to reset the circuit. The delay from the onset of excessive load current to complete shutdown is inside 18ns. The 4ns delay of Trace A's current probe should be factored in when interpreting waveforms. To calibrate this circuit, ground Q2's base and install a 250mA load. Adjust the 200Ω trim for a 2.5V output at A1. Next, remove the load, unground Q2's base and press the reset button. Finally, put in the desired trip set voltage and the circuit is ready for use.

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Application Note 47

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Note: *This application note was derived from a manuscript originally prepared for publication in EDN Magazine.*

APPENDIX A

ABC's of Probes – Tektronix, Inc.

This appendix, guest written by the engineering staff of Tektronix, Inc., is a distillation of their booklet, "ABC's of Probes". The complete booklet is available, at no charge,

through any Tektronix sales office or call 800-835-9433 ext. 170. For excellent technical background on probe theory see Reference 42.

PART I: UNDERSTANDING PROBES

The vital link in your measurement system

Probes connect the measurement test points in a DUT (device under test) to the inputs of an oscilloscope. Achieving optimized system performance depends on selecting the proper probe for your measurement needs.

Though you could connect a scope and DUT with just a wire, this simplest of connections would not let you realize the full capabilities of your scope. By the same token, a probe that is not right for your application can mean a significant loss in measurement results, plus costly delays and errors.

Why not use a piece of wire?

Good question: There are legitimate reasons for using a piece of wire or, more correctly, two pieces of wire; some low bandwidth scopes and special purpose plug-in amplifiers only provide binding post input terminals, so they offer a convenient means of attaching wires of various lengths.

DC levels associated with battery operated equipment could be measured. Low frequency (audio) signals from the same equipment could also be examined. Some high output transducers could also be monitored. However, this type of connection should be kept away from line-operated equipment for two basic reasons, safety and risk of equipment damage.

Safety: Attachment of hookup wires to line-operated equipment could impose a health hazard, either because the "hot" side of the line itself could be accessed, or because internally generated high voltages could be contacted. In both cases, the hookup wire offers virtually no operator protection, either at the equipment source or at the scope's binding posts.

Risk of Equipment Damage:

Two unidentified hookup wires, one signal lead and one ground, could cause havoc in line-operated equipment. If the "ground" wire is attached to **any** elevated signal in line-operated equipment, various degrees of damage will result simply because both the scope and the equipment are (or should be) on the same three-wire outlet system, and short-circuit continuity is completed through one common ground.

Performance Considerations:

In addition to the hazards just mentioned, there are two major performance limitations associated with using hookup wires to transfer the signal to the scope: circuit loading and susceptibility to external pickup.

Circuit Loading: This subject will be discussed in detail later, but circuit loading by the test equipment (scope-probe) is a combination of resistance and capacitance. Without the benefit of using an attenuator (10X) probe, the loading on the device under test (DUT) will be 1M ohm (the scope input resistance) and more than 15 picofarad (15pF), which is the typical scope input capacitance plus the stray capacitance of the hookup wire.

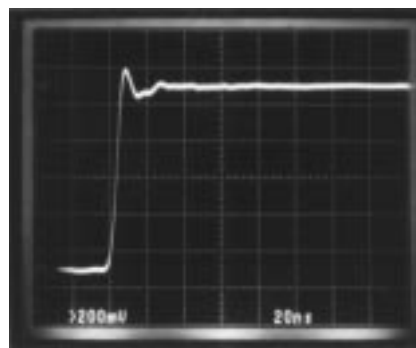


Figure 1-1

Figure 1-1 shows what a "real world" signal from a 500 ohm impedance source looks like when loaded by a 10M ohm, 10 pF probe:

the scope-probe system is 300MHz. Observed risetime is 6 nSec.

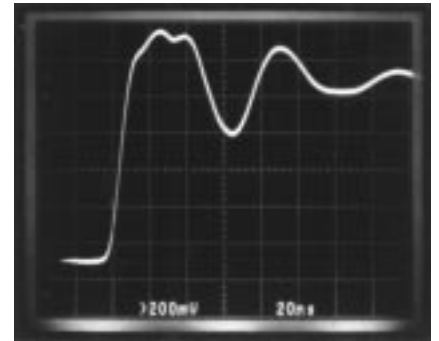


Figure 1-2

Figure 1-2 shows what happens to the same signal when it is accessed by two 2-meter lengths of hookup wire: loading is 1M ohm (the scope input resistance) and about 20 pF (the scope input capacitance, plus the stray capacitance of the wires). Observed risetime has slowed to 10 nSec and the transient response of the system has become unusable.

Susceptibility to External Pickup: An unshielded piece of wire acts as an antenna for the pickup of external fields, such as line frequency interference, electrical noise from fluorescent lamps, radio stations and signals from nearby equipment. These signals are not only injected into the scope along with the wanted signal, but can also be injected into the device under test (DUT) itself.

The source impedance of the DUT has a major effect on the level of interference signals developed in the wire. A very low source impedance would tend to shunt any induced voltages to ground, but high frequency signals could still appear at the scope input and mask the wanted signal. The answer, of course, is to use a probe which, in addition to its other features, provides coaxial shielding of the center conductor and virtual elimination of external field pickup.

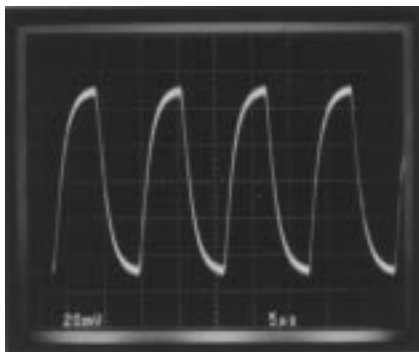


Figure 1-3

Figure 1-3 shows what a low level signal from a high impedance source (100mV from 100K ohm) looks like when accessed by a 300MHz scope-probe system. Loading is 10M ohm and 10 pF. This is a true representation of the signal, except that probe resistive loading has reduced the amplitude by about 1%; the observed high frequency noise is part of the signal at the high impedance test point and would normally be removed by using the BW (bandwidth) limit button on the scope. (See Figure 1-4.)

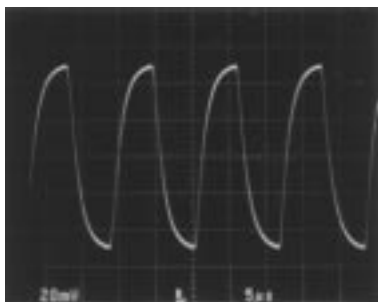


Figure 1-4

If we look at the same test point with our pieces of wire, two things happen. The amplitude drops due to the increased resistive and capacitive loading, and noise is added to the signal because the hookup wire is completely unshielded. (See Figure 1-5)

Most of the observed noise is line frequency interference from fluorescent lamps in the test area.

Probably the most annoying effect of using hookup wire to observe high frequency signals is its unpredictability. Any touching or rearrangement of the leads can produce different and nonrepeatable effects on the observed display.

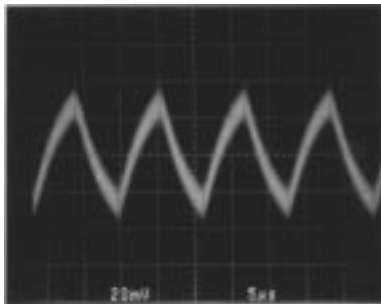


Figure 1-5

Benefits of using probes

Not all probes are alike and, for any specific application, there is no one ideal probe; but they share common features and functions that are often taken for granted.

Probes are convenient. They bring a scope's vertical amplifier to a circuit. Without a probe, you would either need to pick up a scope and attach it to a circuit, or pick up the circuit and attach it to the scope. Properly used, probes are convenient, flexible and safe extensions of a scope.

Probes provide a solid mechanical connection. A probe tip, whether it's a clip or a fine solid point, makes contact at just the place you want to examine.

Probes help minimize loading. To a certain extent, all probes load the DUT—the source of the signal you are measuring. Still, probes offer the best means of making the connections needed. A simple piece of wire, as we have just seen, would severely load the DUT; in fact, the DUT might stop functioning altogether.

Probes are designed to minimize loading. Passive, non-attenuating 1X probes offer the highest capacitive loading of any probe type—even these, however, are designed to keep loading as low as possible.

Probes protect a signal from external interference. A wire connection, as described earlier, in addition to loading the circuit, would act as an antenna and pick up stray signals such as 60Hz power, CBers, radio and TV stations. The scope would display these stray signals as well as the signal of interest from the DUT.

Probes extend a scope's signal amplitude-handling ability. Besides reducing capacitive and resistive loading, a standard passive 10X

(ten times attenuation) probe extends the on-screen viewability of signal amplitudes by a factor of ten.

A typical scope minimum sensitivity is 5V/division. Assuming an eight-division vertical graticule, a 1X probe (or a direct connection) would allow on-screen viewing of 40V p-p maximum. The standard 10X passive probe provides 400V p-p viewing. Following the same line, a 100X probe should allow 4kV on-screen viewing. However, most 100X probes are rated at 1.5kV to limit power dissipation in the probe itself.

Check the specs. Bandwidth is the probe specification most users look at first, but plenty of other features also help to determine which probe is right for your application. Circuit loading, signal aberrations, probe dynamic range, probe dimensions, environmental degradation and ground-path effects will all impact the probe selection process, as discussed in the pages that follow.

By giving due consideration to probe characteristics that your application requires, you will achieve successful measurements and derive full benefit from the instrument capabilities you have at hand.

How probes affect your measurements

Probes affect your measurements by loading the circuit you are examining. The loading effect is generally stated in terms of impedance at some specific frequency, and is made up of a combination of resistance and capacitance.

Source Impedance. Obviously, source impedance will have a large impact on the net effect of any specific probe loading. For example, a device under test with a near zero output impedance would not be affected in terms of amplitude or risetime to any significant degree by the use of a typical 10X passive probe. However, the same probe connected to a high impedance test point, such as the collector of a transistor, could affect the signal in terms of risetime and amplitude.

Capacitive Loading. To illustrate this effect, let's take a pulse generator with a very fast risetime. If the initial risetime was assumed to be zero ($t_r = 0$), the output t_r of the generator would be limited by the

associated resistance and capacitance of the generator. This integration network produces an output rise time equal to $2.2 RC$. This limitation is derived from the universal time-constant curve of a capacitor.

Figure 1-6 shows the effect of internal source resistance and capacitance on the equivalent circuit. At no time can the output risetime be faster than $2.2 RC$ or 2.2 nSec .

If a typical probe is used to measure this signal, the probe's specified input capacitance and resistance is added to the circuit as shown in Figure 1-7.

Because the probe's $10 \text{ M}\Omega$ resistance is much greater than the generator's 50 ohm output resistance, it can be ignored.

Figure 1-8 shows the equivalent circuit of the generator and probe, applying the $2.2 RC$ formula again. The actual risetime has slowed from 2.2 n Sec. to 3.4 nSec.

Percentage change in risetime due to the added probe tip capacitance:

$$\% \text{ change} = \frac{tr_2 - tr_1}{tr_1} \times 100 = \frac{3.4 - 2.2}{2.2} \times 100 = 55\%$$

Another way of estimating the affect of probe tip capacitance on a source is to take the ratio of probe tip capacitance (marked on the probe compensation box) to the known or estimated source capacitance.

Using the same values:

$$\frac{C_{\text{probe tip}}}{C_1} \times 100 = \frac{11 \text{ pF}}{20 \text{ pF}} \times 100 = 55\%$$

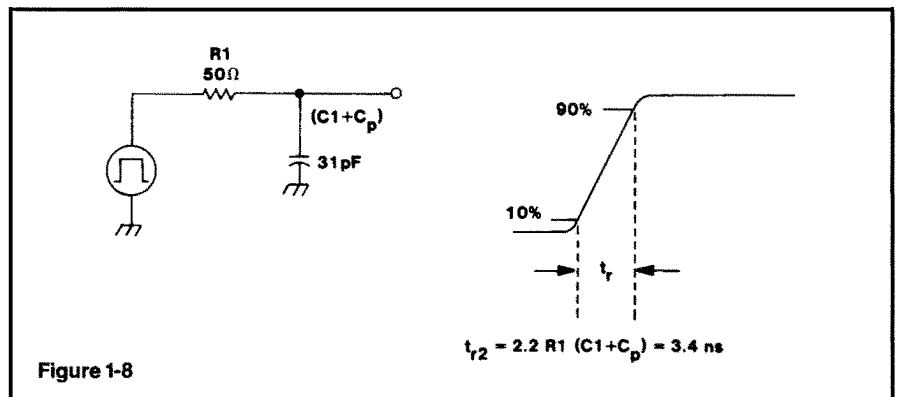
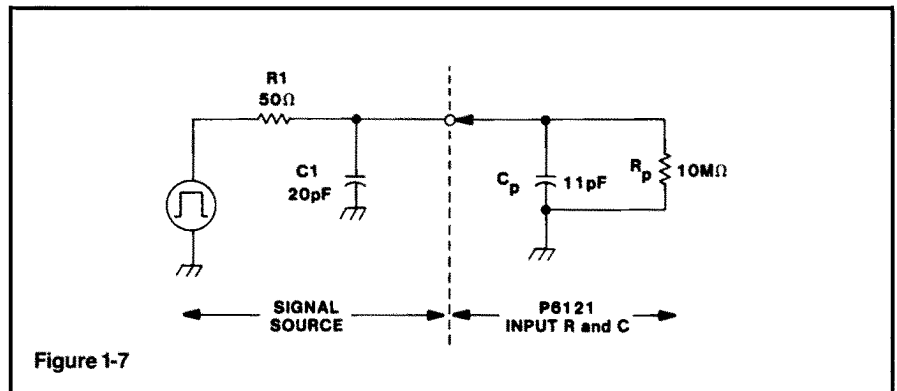
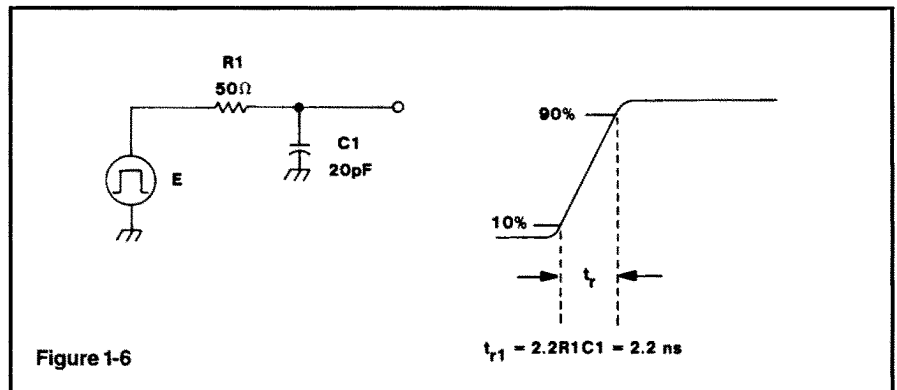
To summarize, any added capacitance slows the source risetime when using high impedance passive probes. In general, the greater the attenuation ratio, the lower the tip capacitance. Here are some examples:

Probe	Attenuation	Tip Capacitance
Tektronix P6101A	X1	54 pF
Tektronix P6105A	X10	11.2 pF
Tektronix P6007	X100	2 pF

Capacitive Loading: Sinewave.

When probing continuous wave (CW) signals, the probe's capacitive reactance at the operating frequency must be taken into account.

The total impedance, as seen at the probe tip, is designated R_p and is a function of frequency. In addition to the capacitive and resistive elements, designed-in inductive elements serve to offset the pure capacitive loading to some degree.



Curves showing typical input impedance vs frequency, or typical X_p and R_p vs frequency are included in most Tektronix probe instruction manuals. Figure 1-9A shows the typical input impedance and phase relationship vs frequency of the Tektronix P6203 Active Probe. Note that the $10 \text{ K}\Omega$ input impedance is maintained to almost 10 MHz by careful design of the associated resistive, capacitive and inductive elements.

Figure 1-9B shows a plot of X_p and R_p vs frequency for a typical $10 \text{ M}\Omega$ passive probe. The dotted line (X_p) shows capacitive reactance vs frequency. The total loading is again offset by careful design of the associated R, C and L elements.

If you do not have ready access to the information and need a worst-case guide to probe loading, use the following formula:

$$X_p = \frac{1}{2\pi FC}$$

X_p = Capacitive reactance (ohms)
 F = Operating frequency
 C = Probe tip capacitance (marked on the probe body or compensation box.)

For example, a standard passive $10 \text{ M}\Omega$ probe with a tip capacitance of 11 pF will have a capacitive reactance (X_p) of about 290 ohm at 50 MHz .

Depending, of course, on the source impedance, this loading could have a major effect on the

Application Note 47

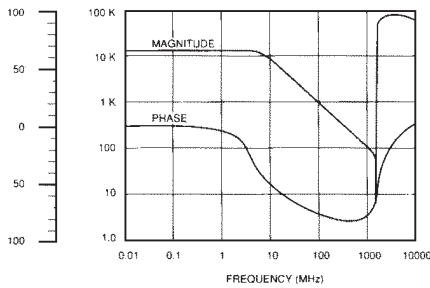


Figure 1-9A. Typical Input Impedance vs Frequency for the Tektronix P6203 Active Probe

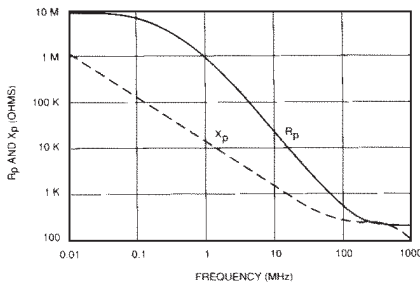


Figure 1-9B. Xp and Rp vs Frequency for a Typical 10 MΩ Passive Probe

signal amplitude (by simple divider action), and even on the operation of the circuit itself.

Resistive Loading. For all practical purposes, a 10X, 10M ohm passive probe has little effect on today's circuitry in terms of resistive loading, however, they do carry a trade-off in terms of relatively high capacitive loading as we have previously discussed.

Low Z Passive Probes. A "Low Z" passive probe offers very low tip capacitance at the expense of relatively high resistive loading. A typical 10X "50 ohm" probe has an input C of about 1 pF and a resistive loading of 500 ohm: Figure 1-10 shows the circuit and equivalent model of this type of probe.

This configuration forms a high frequency 10X voltage divider because, from transmission line theory, all that the 450 ohm tip resistor "sees" looking into the cable is a pure 50 ohm resistance, no C or L component. No low frequency compensation is necessary because it is not a capacitive divider. Low Z probes are typically high bandwidth (up to 3.5GHz and risetimes to 100 pS) and are best suited for making risetime and transit-time measurements. They can, however, affect the pulse amplitude by simple resistive divider action between the source and the load (probe). Because of its resistive loading effects, this type of probe

performs best on 50 ohm or lower impedance circuits under test.

Note also that these probes operate into 50 ohm scope inputs only. They are typically teamed up with fast (500MHz to 1GHz) real time scopes or with scopes employing the sampling principle.

Bias-Offset Probes. A Bias/Offset probe is a special kind of Low Z design with the capability of providing a variable bias or offset voltage at the probe tip.

Bias/Offset probes like the Tektronix P6230 or P6231 are useful for probing high speed ECL circuitry, where resistive loading could upset the operating point. These special probes are fully described in Part 3; under Advanced Probing Techniques.

The Best of Both Worlds. From the foregoing, it can be seen that the totally "non-invasive" probe does not exist. However, one type of probe comes close—the active probe.

Active probes are discussed in the Tutorial section, but in general, they provide low resistance loading (10M ohm) with very low capacitive loading (1 to 2 pF). They do have trade-offs in terms of limited dynamic range, but under the right conditions, do indeed offer the best of both worlds.

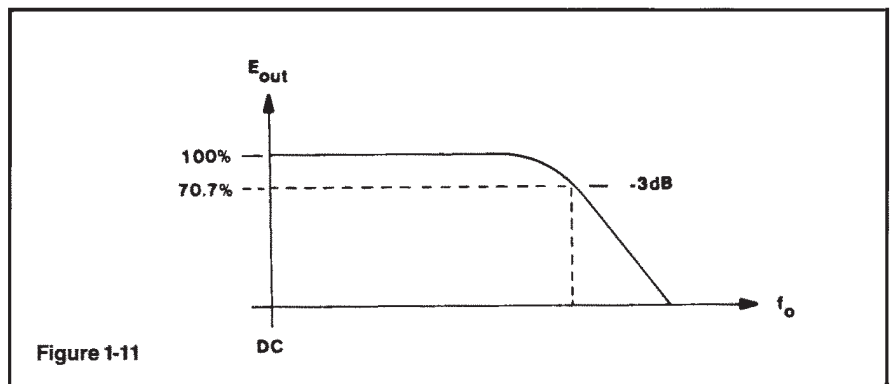
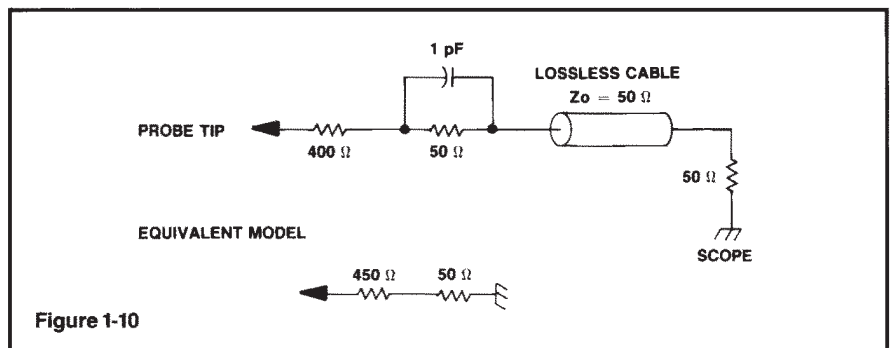
Bandwidth. Bandwidth is the point on an amplitude versus frequency curve where the measurement system is down 3dB from a starting (reference) level. Figure 1-11 shows a typical response curve of an oscilloscope system.

Scope vertical amplifiers are designed for a Gaussian roll-off at the high end (a discussion of Gaussian response is beyond the scope of this primer). With this type of response, risetime is approximately related to bandwidth by the following equation:

$$Tr = \frac{.35}{BW} \quad \text{or, for convenience:} \\ \text{Risetime (nanoseconds)} = \frac{350}{\text{Bandwidth (MHz)}}$$

It is important to note that the measurement system is -3dB (30%) down in amplitude at the specified bandwidth limit.

Figure 1-12 shows an expanded portion of the -3dB area. The horizontal scale shows the input frequency derating factor necessary to obtain accuracies better than 30% for a specific bandwidth scope. For example, with no derating, a "100MHz" scope will have up to a 30% amplitude error at 100MHz (1.0 on the graph). If this scope is to have an amplitude accuracy better than 3%, the input frequency must be limited to about 30MHz (100MHz X .3).



For making amplitude measurements within 3% at a specific frequency, choose a scope with at least four times the specified bandwidth as a general rule of thumb.

Probe Bandwidth. All probes are ranked by bandwidth. In this respect, they are like scopes or other amplifiers that are ranked by bandwidth. In these cases we apply the square root of the sum of the squares formula to obtain the "system risetime." This formula states that:

$$\text{Risetime system} = \sqrt{\text{Tr}^2_{\text{displayed}} + \text{Tr}^2_{\text{source}}}$$

Passive probes do not follow this rule and should not be included in the square root of the sum of the squares formula.

Tektronix provides a probe bandwidth ranking system that specifies "the bandwidth (frequency range) in which the probe performs within its specified limits. These limits include: total aberrations, risetime and swept bandwidth."

Both the source and the measurement system shall be specified when checking probe specifications (see Test Methods, this page).

In general, a Tektronix "100MHz" probe provides 100MHz performance (-3dB) when used on a compatible 100MHz scope. In other words, it provides full scope bandwidth **at the probe tip.**

However, not all probe/scope systems can follow this general rule. Refer to the sidebar, "Scope Bandwidth at the Probe Tip?."

Figure 1-13 shows examples of Tektronix scopes and their recommended passive probes.

Test Methods: As with all specifications, matching test methods must be employed to obtain specified performance. In the case of bandwidth and risetime measurements, it is essential to connect the probe to a properly terminated source. Tektronix specifies a 50 ohm source terminated in 50 ohm, making this a 25 ohm source impedance. Furthermore, the probe must be connected to the source via a proper probe tip to BNC adaptor. (Figure 1-14).

Figure 1-14 shows an equivalent circuit of a typical setup. The displayed risetime should be a 3.5 nSec or faster.

Figure 1-15 shows an equivalent circuit of a typical passive probe connected to a source.

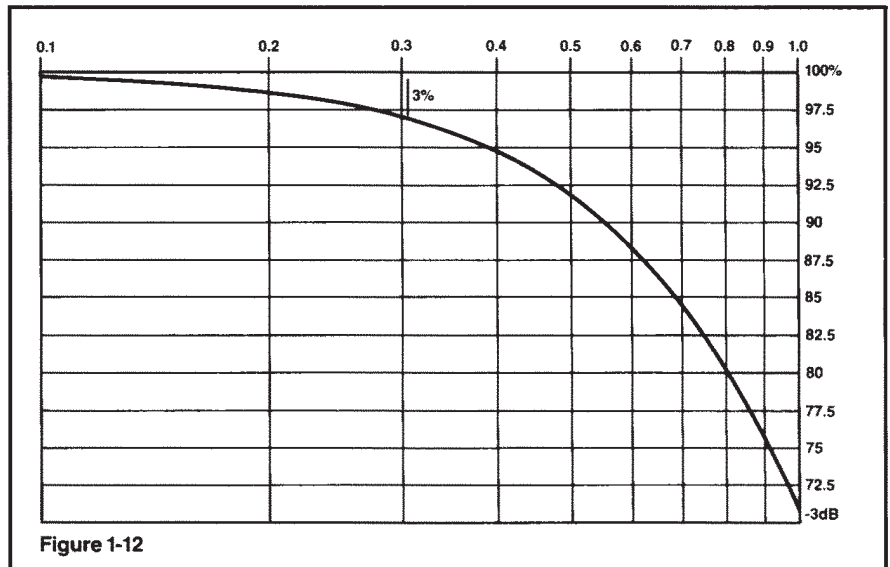


Figure 1-12

SCOPE	BW (1 MΩ input)	PROBE	BW	SYSTEM
2235	100	P6109	150	100
2245A	100	P6109	150	100
2246A	100	P6109	150	100
2445B	150	P6133	150	150
		Opt 25		
485	350	P6106A	250	250
2465B	400	P6137	400	400
2467B	400	P6137	400	400

Figure 1-13

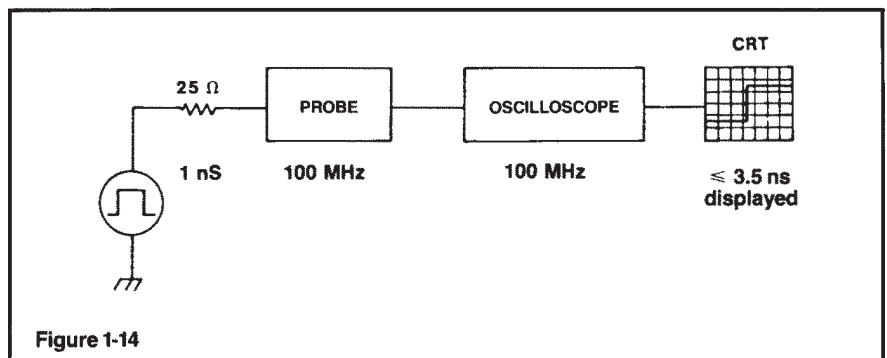


Figure 1-14

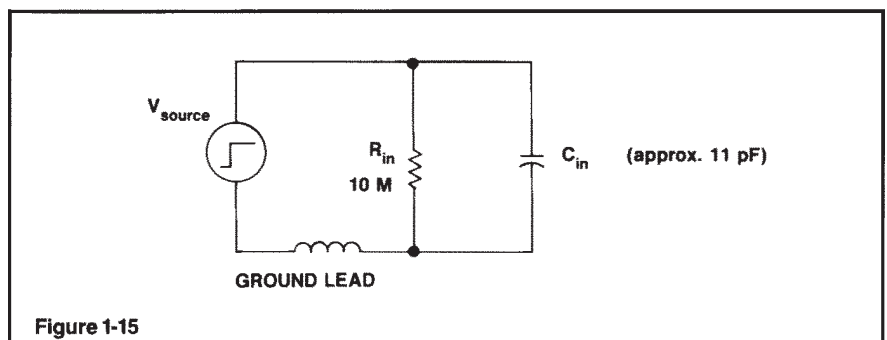


Figure 1-15

Scope Bandwidth at the Probe Tip ?

Most manufacturers of general-purpose oscilloscopes that include standard accessory probes in the package, promise and deliver the advertised scope bandwidth **at the probe tip**.

For example, the Tektronix 2465B 400 MHz Portable Oscilloscope and its standard accessory P6137 Passive Probes deliver 400 MHz (-3db) at the probe tip.

However, not all high performance scopes can offer this feature, even when used with their recommended passive probes. For example, the Tektronix 11A32 400 MHz plug-in has a system bandwidth of 300 MHz when used with its recommended P6134 passive probe. This is simply because even the highest impedance passive probes are limited to about 300 to 350 MHz, while still meeting their other specifications.

It is important to note that the above performance is only obtainable under strictly controlled, and industry recognized conditions; which states that the signal must originate from a 50 Ω back-terminated source (25 Ω), and that the probe must be connected to the source by means of a probe tip to BNC (for other) adaptor.

This method ensures the shortest ground path and necessary low impedance to drive the probe's input capacitance, and to provide the specified bandwidth at the signal acquisition point, the probe tip.

Real-world signals rarely originate from 25 Ω sources, so less than optimum transient response and bandwidth should be expected when measuring higher impedance circuits.

How ground leads affect measurements

A ground lead is a wire that provides a local ground-return path when you are measuring any signal. An inadequate ground lead (one that is too long or too high in inductance) can reduce the fidelity of the high frequency portion of the displayed signal.

What grounding system to use.
When making **any** measurement, some form of ground path is required to make a basic two-terminal connection to the DUT. If you want to check the presence or absence of signals from low-frequency equipment, **and** if the equipment is line-powered and plugged into the same outlet system as the scope, then the common 3-wire ground system provides the signal ground return. However, this indirect route adds inductance in the signal path—it can also produce ringing and noise on the displayed signal and is not recommended.

When making any kind of absolute measurement, such as amplitude, risetime or time delay measurements, you should use the shortest grounding path possible, consistent with the need to move the probe among adjacent test points. The ultimate grounding system is an in-circuit ECB (etched circuit board) to probe tip adaptor. Tektronix can supply these for either miniature, compact or subminiature probe configurations.

Figure 1-15 shows an equivalent circuit of a typical passive probe connected to a source. The ground lead L and C_{in} form a series resonant circuit with only 10M ohm for damping. When hit with a pulse, it will ring. Also, excessive L in the ground lead will limit the changing current to C_{in} , limiting the risetime.

Without going into the mathematics, an 11pF passive probe with a 6-inch ground lead will ring at about 140MHz when excited by a fast pulse. As the ring frequency increases, it tends to get outside the passband of the scope and is greatly attenuated. So to increase the ring frequency, use the shortest ground lead possible and use a probe with the lowest input C .

Probe Ground Lead Effects. The effect of inappropriate grounding methods can be demonstrated several ways. Figs. 1-16A, B and C show the effect of a 12-inch ground lead when used on various bandwidth scopes.

In Figure 1-16A, the display on the 15MHz scope looks OK because the ringing aberrations are beyond the passband of the instrument and are greatly attenuated. Figs. 1-16B and C show what the same signal looks like on 50MHz and 100MHz scopes.

Even with the shortest ground lead, the probe-DUT interface has the **potential** to ring. The potential to ring depends on the **speed** of the step function. The ability to **see** the resultant ringing oscillation depends on the scope system bandwidth.

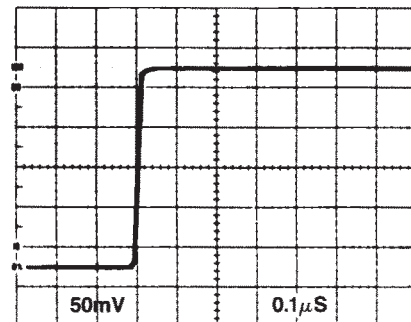


Figure 1-16A

Scope BW = 15MHz
Ground lead 12 inches

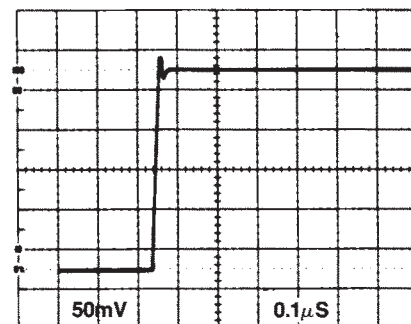


Figure 1-16B

Scope BW = 50MHz
Ground lead 12 inches

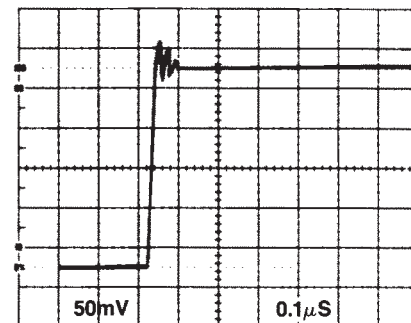


Figure 1-16C

Scope BW = 100MHz
Ground lead 12 inches

Figs. 1-17A through F show the effects of various grounding methods and ground lead lengths on the display of a very fast pulse. This is the most critical way of looking at ground lead effects: we used a fast pulse, with a risetime of about 70 pico seconds and a fast (400 MHz) scope with a matching P6137 probe.

Fig. 1-17A shows the input pulse under the most optimum conditions when using 50 ohm coax cable. Scope: the Tektronix 2465B with 50 ohm input and 50 ohm cable from a 50 ohm source. Displayed risetime is < 1 nSec.

Fig. 1-17B shows the same signal when using the scope-probe combination under the most optimum conditions. A BNC to probe adaptor or an in-circuit test jack provides a coaxial ground that surrounds the probe ground ring. This system provides the shortest probe ground connection available. Displayed risetime is < 1 nSec.

Figures 1-17C through E show the effects of longer ground leads on the displayed signal. Fig. 1-17C shows the effect of a short semi-flexible

ground connection, called a "Z" lead. Finally, Fig. 1-17F shows what happens when no probe ground lead is used.

How probe design affects your measurements

Probes are available in a variety of sizes, shapes and functions, but they do share several main features: a probe head, coaxial cable and either a compensation box or a termination.

The probe head contains the signal-sensing circuitry. This circuitry may be passive (such as a 9-M ohm resistor shunted by an 11 pF capacitor in a passive voltage probe or a 125-turn transformer secondary in a current probe); or active (such as a source follower or Hall generator) in a current probe or active voltage probe.

The coaxial cable couples the probe head output to the termination. Cable types vary with probe types.

The termination has two functions:

- to terminate the cable in its characteristic impedance.
- to match the input impedance of the scope.

The termination may be passive or active circuitry. For easy connection to various test points, many probes feature interchangeable tips and ground leads.

A unique feature of most Tektronix probes is the Tektronix-patented coaxial cable that has a resistance-wire center conductor. This distributed resistance suppresses ringing caused by impedance mismatches between the cable and its terminations when you're viewing fast pulses on wideband scopes.

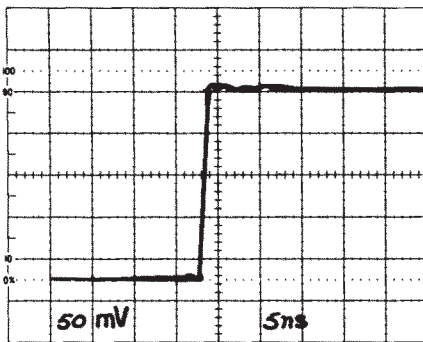


Figure 1-17A
50 ohm Source/Cable/2465B/50 ohm input

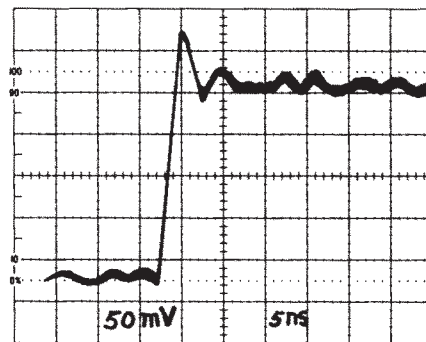


Figure 1-17C
P6137 - Probe/Z Ground Tr = 1.5 nS

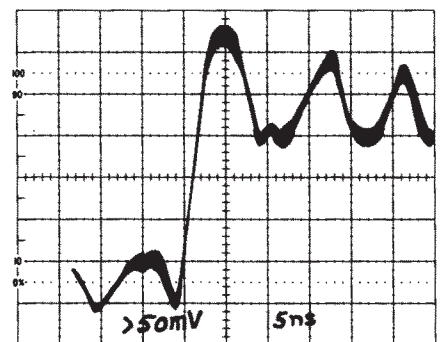


Figure 1-17E
P6137 - Probe/6" Gnd Lead Tr = 4 nS

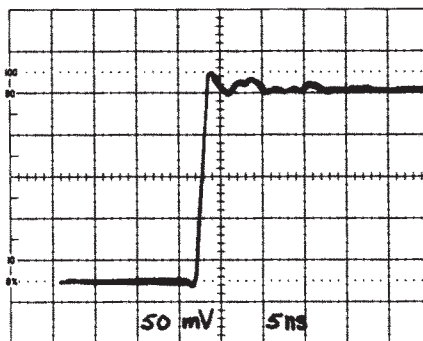


Figure 1-17B
P6137-BNC/Probe Adaptor Tr = < 1 nS

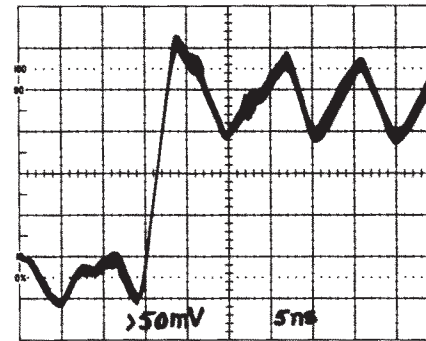


Figure 1-17D
P6137 - Probe/3" Gnd Lead Tr = 4 nS

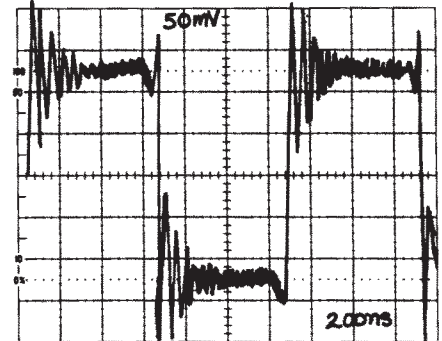


Figure 1-17F
No Ground Lead

Application Note 47

PART II: EFFECTS OF PROBE COMPENSATION — UNDERSTANDING PROBES

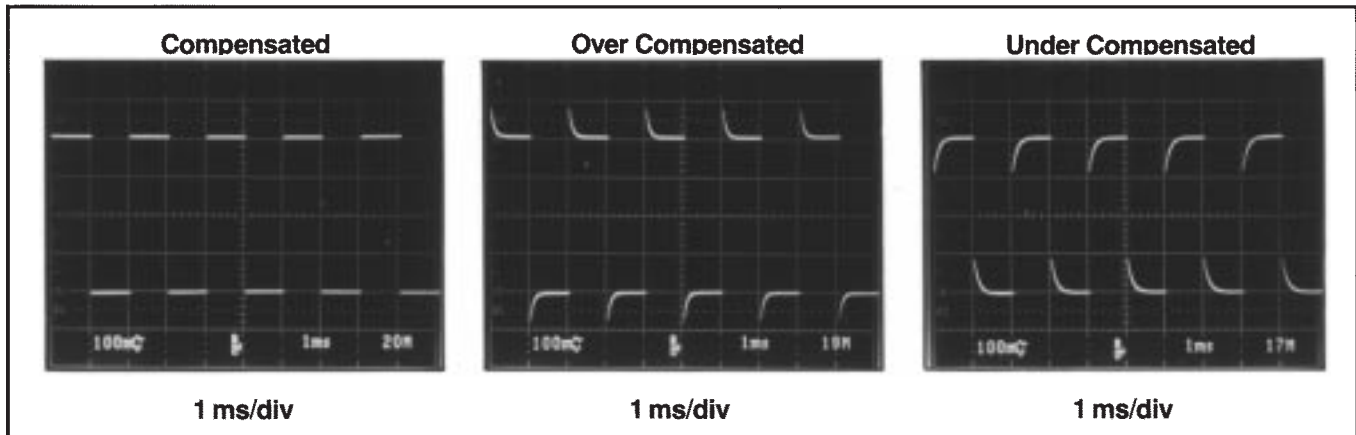


Figure 2-1. Shows the display associated with correctly and incorrectly compensated probes.

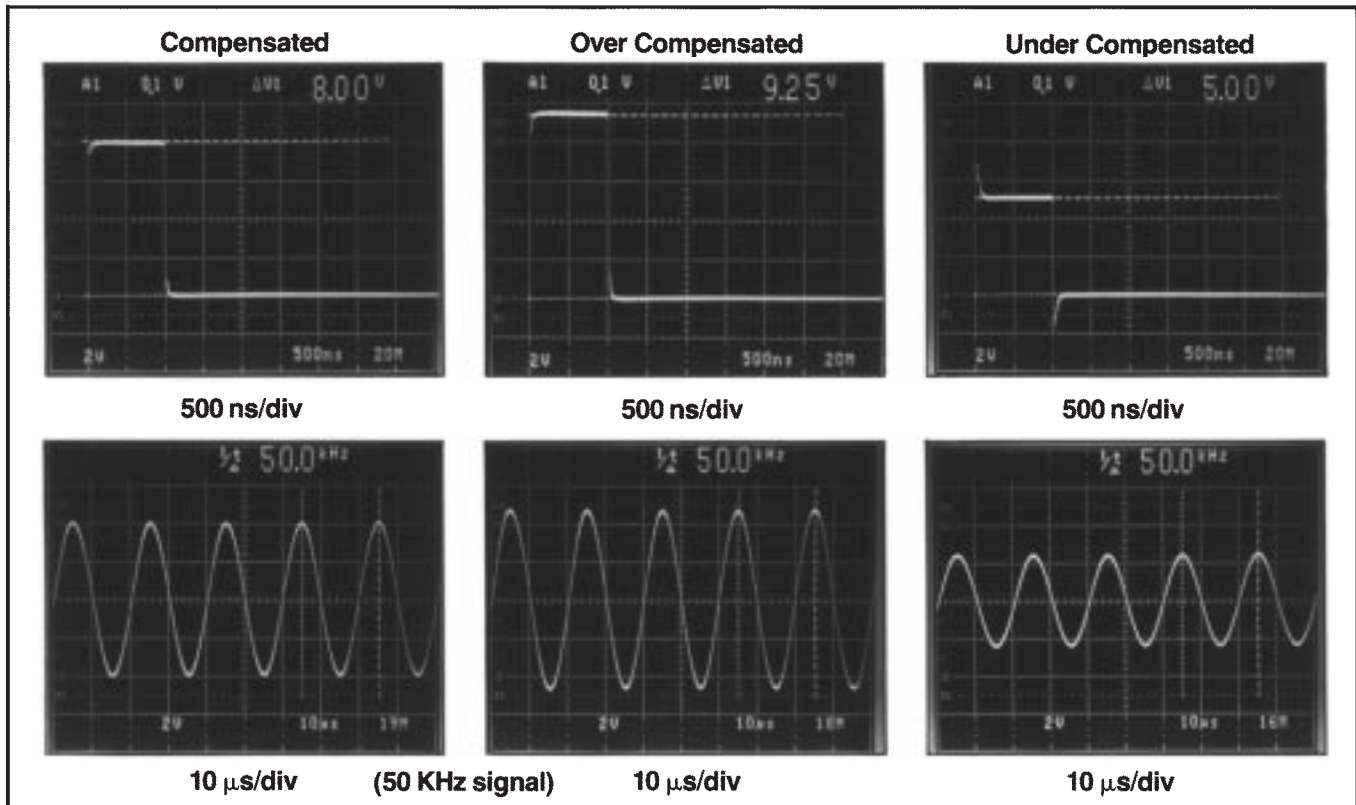


Figure 2-2. Shows the effects on faster pulses and sinewaves when an incorrectly compensated probe is used. Note that the much faster sweep rates used to correctly view these waveforms does not warn the user of an adjustment problem.

Tips on using probes

Compensating the probe. The most common mistake in making scope measurements is forgetting to compensate the probe. Improperly compensated probes can distort the waveforms displayed on the scope. The probe should be compensated as it will be used when you make the measurement.

The basic low frequency compensation (L.F. comp.) procedure is simple:

- Connect the probe tip to the scope CALIBRATOR (refer to Scope Calibrator Outputs.)
- Switch the channel 1 input coupling to dc.
- Turn on the scope and move the CH1 VOLTS/DIV switch to pro-

duce about four divisions of vertical display.

- Set the sweep rate to 1mSec/div. (for line-driven calibrators see Scope Calibrators Outputs.)
- Use a non-metallic alignment tool to turn the compensation adjust until the tops and bottoms of the square-wave are flat.

PART III: ADVANCED PROBING TECHNIQUES

Introduction:

In Part III we will examine some of the more advanced probing techniques associated with accessing high frequency and complex signals, such as fast ECL, waveforms offset from ground, and true differential signals.

Most of the techniques to be described follow recommended practices outlined throughout this Booklet, and to a large extent involve proper grounding techniques.

Workers in the audio and relatively low frequency fields may wonder what all the fuss is about, and may comment "I don't have any of these problems," or "I can't see any difference when I use different ground lead lengths, or even when I leave the ground lead completely off?"

In order to see aberrations caused by poor grounding techniques, two conditions must exist:

1. The scope system bandwidth must be great enough to handle the high frequency content existing at the probe tip.
2. The input signal must contain enough high frequency information (fast risetime) in order to cause ringing and aberrations due to poor grounding techniques.

To illustrate these points, a 20 MHz scope was used to access a 1.7 nS pulse by using a standard passive probe with a 6" ground lead.

NOTE: A fast scope can be made into a slow scope simply by pushing the Bandwidth Limit (B/W Limit) button ?.

We used a 350 MHz scope with a 20 MHz B/W Limit function.

Figure 3-1 shows the resultant clean displayed pulse with a risetime of about 20 nS (17.5 MHz).

This display does not represent conditions actually existing at the probe tip, because the 20 MHz measurement system cannot "see" what's really happening.

Figure 3-2 shows what the probe tip signal really looks like when a 350 MHz scope is used under the same conditions (B/W Limit off).

The observed risetime has improved to about 2 nS, but we have serious problems with ringing and aberrations, caused by incorrect grounding techniques.

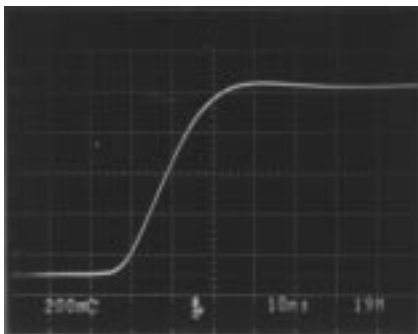


Figure 3-1. Resultant clean, but incorrect display caused by inadequate scope system bandwidth.

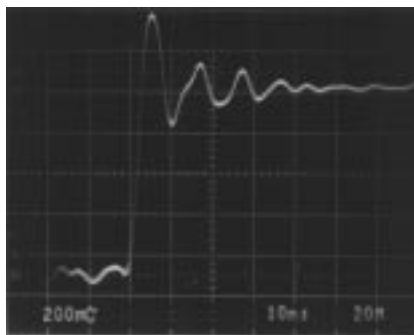


Figure 3-2. The same input signal as shown in figure 3-1, but accessed by a 350 MHz system bandwidth scope (same 6" ground lead).

The problem can now be seen because the scope system bandwidth is great enough to pass and display all the frequency content existing at the probe tip.

To further stress the points about high frequency content and scope system bandwidth, let's assume an input pulse with a risetime of about 20 nS. If the signal is accessed by the same probe /6" ground lead /350 MHz system, it would look very much like the display in figure 3-1.

There would be no frequency content higher than 17.5 MHz (20 nS Tr). The 6" ground lead would not ring, and would therefore be the correct choice for accessing this relatively slow signal.

In the following sections we discuss how to recognize signal acquisition problems, and how to avoid them.

Techniques for probing ECL, high speed 50 Ω environments, and accessing true differential signals are also discussed.

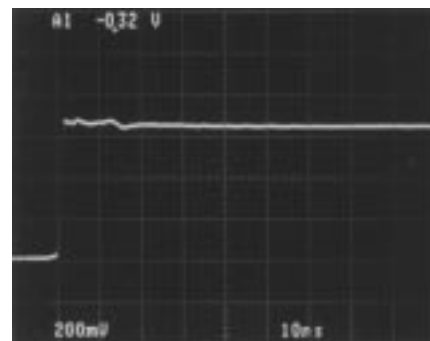


Figure 3-3. 1 nS Tr pulse accessed via an ECB to Probe Tip Adaptor (test point)

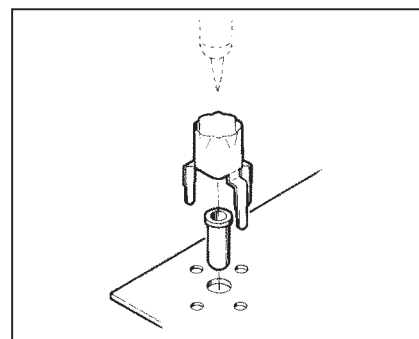


Figure 3-4. Typical ECB to Probe Tip Adaptor installation

Probe Ground Lead Effects. In Part I we discussed the basic need for probe grounding, and showed several different ways of looking at the effects of correct, and incorrect probe grounding.

In this section, we will expand upon these techniques and show how to identify problem areas.

When a probe (high Z, low Z, passive or active) is connected to the circuit under test via an ECB to Probe Tip Adaptor (test point), the coaxial environment existing at the probe tip is extended through the adaptor to the signal pick-off point, and to the ECB ground plane (or device ground).

Figure 3-3 shows what a typical 1 nS Tr pulse looks like when a suitable probe is connected to the circuit via an ECB to Probe Tip Adaptor.

Figure 3-4 shows a typical ECB to Probe Tip Adaptor (test point) installation.

These test points are available in three sizes to accept miniature, compact or sub-miniature series probes.

Application Note 47

If a flexible ground lead is used in place of the ECB to Probe Tip Adaptor, the 1 nS Tr input step (with high frequency content up to 350 MHz) will cause the ground lead to ring at a frequency determined by the ground lead inductance and the probe tip and source capacitance.

Figure 3-5 shows the effect of using a 6" ground lead to make the ground connection.

The ring frequency for the 6" ground lead/probe tip C combination is 87.5 MHz. This signal is injected in series with the wanted signal and appears at the probe tip, as shown in figure 3-6.

Unfortunately, the problem is not this simple.

The probe's coaxial environment has been disrupted at the signal acquisition point by ground lead inductance, and is no longer correctly terminated (for high speed signal acquisition).

This abrupt transition leaves the probe's outer shield susceptible to ring frequency injection (the ground lead inductance is in series with the outer braid)

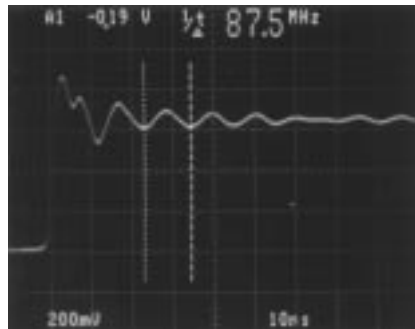


Figure 3-5. Effect of a 6" ground lead on a 1 nS Tr input step.

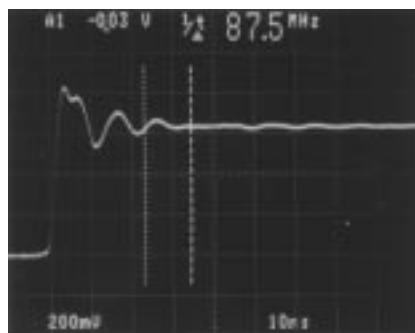


Figure 3-7. The same setup as in figure 3-5, except that the probe cable has been repositioned, and a hand has been placed over part of the probe cable.

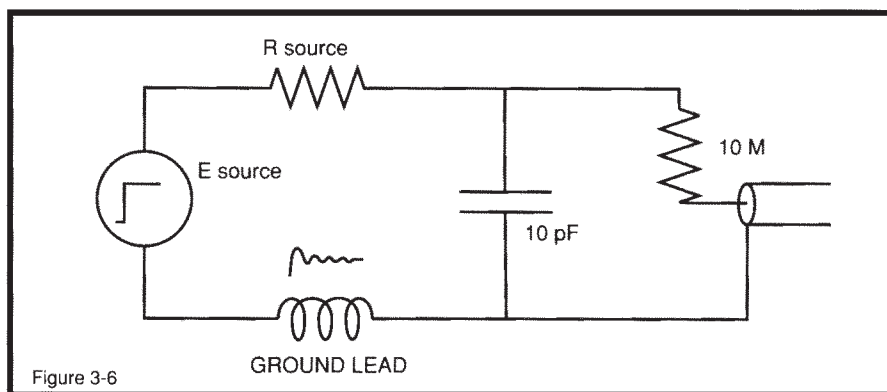


Figure 3-6. Equivalent circuit, ground lead inductance (excess inductance).

The now unterminated probe cable system develops reflections, which intermix with the ring frequency and the signal to produce a multitude of problems and unpredictable results.

Herein lies the key to the identification of ground lead problems.

Figure 3-7 shows exactly the same setup as in figure 3-5, except that the probe cable has been moved, and a hand has been placed over part of the probe cable.

KEY: If touching or moving the probe cable produces changes in the display, you have a probe grounding problem.

A correctly grounded (terminated) probe should be completely insensitive to cable positioning or touch.

Ground Lead Length. All things being equal, the shortest ground lead produces the highest ring frequency.

If the lead is very short, the ring frequency might be high enough to be outside the passband of the scope, and/or the input frequency content may not be high enough to stimulate the ground lead's resonant circuit.

In all cases, the shortest ground lead should be used, consistent with the need for probe mobility.

If possible, use 3" or shorter ground leads, such as the Low Impedance Contact (Z Lead). These are supplied with the Tektronix P613X and P623X family of probes.

One final note. The correct probe grounding method depends on the signal's high frequency content, the scope system bandwidth, and the need for mobility between test points.

A 12" ground lead may be perfect for many lower frequency applica-

tions. It will provide you with extra mobility, and nothing will be gained by using shorter leads.

If in doubt, apply the cable touch test outlined previously.

Ground Loop Noise Injection.

Another form of signal distortion can be caused by signal injection into the grounding system.

This can be caused by unwanted current flow in the ground loop existing between the common scope and test circuit power line grounds, and the probe ground lead and cable.

Normally, all these points are, or should be at zero volts, and no ground current will flow.

However, if the scope and test circuit are on different building system grounds, there could be small voltage differences, or noise on one of the building ground systems.

The resulting current flow (at line frequency or noise frequency) will develop a voltage drop across the probe cable's outer shield, and be injected into the scope in series with the desired signal.

Inductive Pickup in Ground Loops. Noise can enter a common ground system by induction into long 50 Ω signal acquisition cables, or into standard probe cables.

Proximity to power lines or other current-carrying conductors can induce current flow in the probe's outer cable, or in standard 50 Ω coax. The circuit is completed through the building system common ground.

Prevention of Ground Loop Noise Problems. Keep all signal acquisition probes and/or cables away from sources of potential interference.

Verify the integrity of the building system ground.

If the problem persists, open the ground loop:

1. By using a Ground Isolation Monitor like the Tektronix A6901.
2. By using a power line isolation transformer on either the test circuit or on the scope.
3. By using an Isolation Amplifier like the Tektronix A6902B.
4. By using differential probes (see Differential Measurements).

NOTE: Never defeat the safety 3-wire ground system on either the scope or on the test circuit.

Do not "float" the scope, except by using an approved isolation transformer, or preferably, by using the Tektronix A6901 Ground Isolation Monitor.

The A6901 automatically reconnects the ground if scope ground voltages exceed ± 40 V.

Induced Noise in Probe Ground Leads. The typical probe ground lead resembles a single-turn loop antenna when it is connected to the test circuit.

The relatively low impedance of the test circuit can couple any induced voltages into the probe, as shown in figure 3-8.

High speed logic circuits can produce significant electro-magnetic (radiated) noise at close quarters.

If the probe ground lead is positioned too close to certain areas on the board, interference signals could be picked up by the loop antenna formed by the probe ground lead, and mix with the probe tip signal.

Question: Is this what my signal really looks like?

Moving the probe ground lead around will help identify the problem.

If the **noise level** changes, you have a ground lead induced noise problem.

A more positive way of identification is to disconnect the probe from the signal source and clip the ground lead to the probe tip.

Now use the probe/ground lead as a loop antenna and search the board for radiated noise.

Figure 3-9 shows what can be found on a logic board, **with the probe tip shorted to the ground lead.**

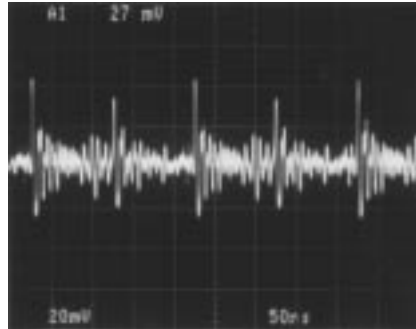


Figure 3-9. Induced noise in the probe ground loop (tip shorted to the ground clip).

This is radiated noise, induced in the single-turn loop and fed to the probe tip.

The significance of any induced or injected noise increases with reduced working signal levels, because the signal to noise ratio will be degraded. This is especially true with ECL, where signal levels are 1 V or less.

Prevention: If possible, use an ECB to Probe Tip Adaptor (test point). If not, use a Z Lead or short flexible ground lead.

Also, bunch the ground lead together to make the loop area as small as possible.

Bias Offset Probes. A Bias/Offset probe is a special kind of Low Z design with the capability of providing a variable bias or offset voltage at the probe tip.

Bias/Offset probes like the Tektronix P6230 and P6231 are useful for probing high speed ECL circuitry, where resistive loading could upset the operating point.

They are also useful for probing higher amplitude signals (up to ± 5 V), where resistive loading could affect the DC level at some point on the waveform.

Bias/Offset probes are designed with a tip resistance of 450Ω (10X). When these probes are connected into a 50Ω environment, this loading results in a 10% reduction in peak to peak source amplitude. This round-figure loading is more convenient to handle than that produced by a standard 500Ω (10 X) Low Z probe, which would work out at 9.09% under the same conditions.

It is important to note that bias/offset probes always present a 450Ω resistive load to the source, regardless of the bias/offset voltage selected.

The difference between bias/offset and standard Low Z probes lies in their ability to null current flow **at some specific and selectable point** on the input waveform (within ± 5 V).

To see how bias/offset probes work, let's take a typical $10 \times 500 \Omega$ Low Z probe and connect it in the circuit shown in figure 3-10.

By taking a current flow approach we find that at one point on the waveform the source voltage is -4 V, therefore the load current will be;

$$I = ER = 4/RS + Rp + R_{scope} = 4/550 = 7.27 \text{ mA.}$$

Therefore the voltage drop across the 50Ω source resistance (R_s) will be;

$$E = IR = 7.27 \times 10^{-3} \times 50 = 0.363 \text{ V}$$

And the measured pulse amplitude will be $-4 - 0.363 = 3.637$ V (E dut), or about 9% down from its unloaded state.

If we substitute the 500Ω Low Z probe with a 450Ω bias/offset probe, the circuit will look like figure 3-11.

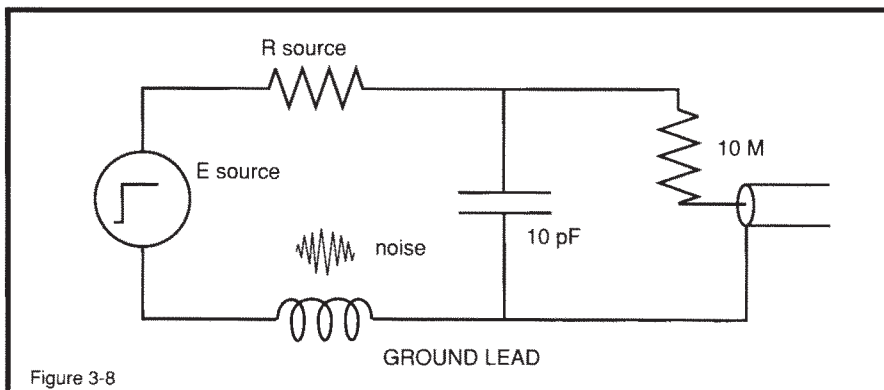


Figure 3-8

Figure 3-8. Equivalent Circuit. Ground Lead Induced Noise.

Application Note 47

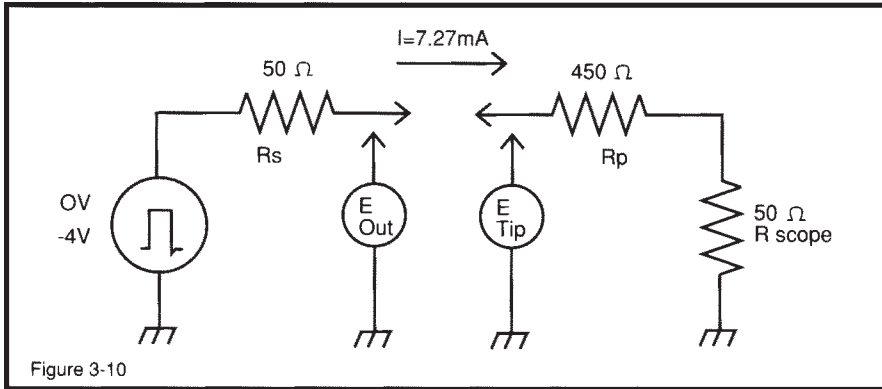


Figure 3-10

Figure 3-10. Low Z 10X 500 Ω probe connected to a 50 Ω source.

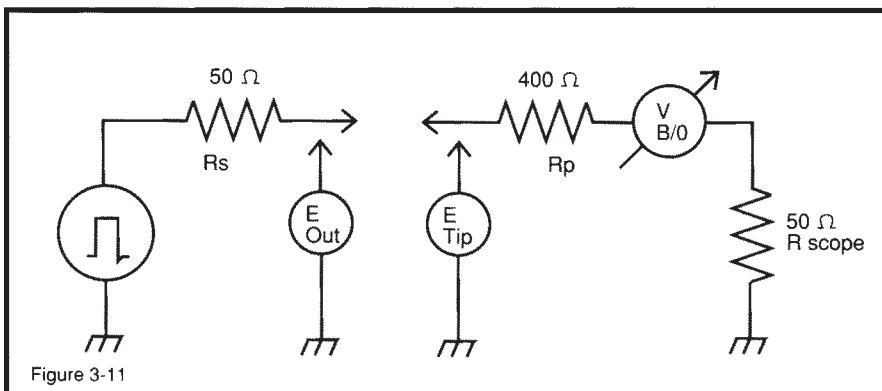


Figure 3-11

Figure 3-11. A 450 Ω Bias/Offset probe connected to a 50 Ω source.

With the bias/offset adjusted for 0 V, the effect on the circuit will be similar to a 500 Ω Low Z probe, except for the small resistive change.

Figure 3-12 shows the source waveform acquired by a 10 M Ω probe.

Figure 3-13 shows the effect on the waveform when the 450 Ω probe is added.

As expected, the pulse amplitude has reduced from -4 V to 3.60 V , or exactly 10% down.

Figure 3-14 shows the effect of adjusting the offset to -4 V . The -4 V bias opposes the signal at the -4 V level and results in zero current flow, and the source is effectively unloaded **at this point**.

However, when the signal returns to ground level, there is a 4 V differential between the top of the pulse and the bias/offset source. Current will flow, and Ohms Law will dictate that the top of the pulse will go negative by -40 mV (10%).

Sometimes it is desirable to adjust the offset mid-way between the peak to peak excursions. This distributes the effect of resistive loading between the two voltage swings.

Figure 3-15 shows the effect of adjusting the bias/offset to -2 V . Current flow will be the same for both signal swings, and they will be equally down by 5%, for a total of 10%.

Summary:

1. Bias/Offset probes can be adjusted (within $\pm 5\text{ V}$) to provide zero resistive (effective) loading at one selected point on the input waveform.
2. Bias/Offset probes can be used to simulate the effect of pull-up or pull-down voltages (within $\pm 5\text{ V}$) on the circuit under test (voltage source impedance is $450\ \Omega$).
3. Bias/Offset probes always present a total resistive load of $450\ \Omega$, and reduce the peak to peak amplitude of $50\ \Omega$ sources by 10%.
4. For simplicity, we have ignored the effects of capacitive loading. Typically, Bias/Offset probes have less than 2 pF tip C.

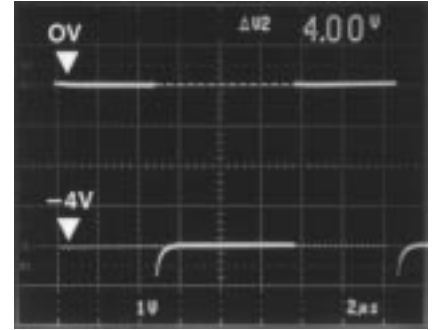


Figure 3-12. Unloaded negative-going 4 V pulse acquired by a 10 M Ω probe.

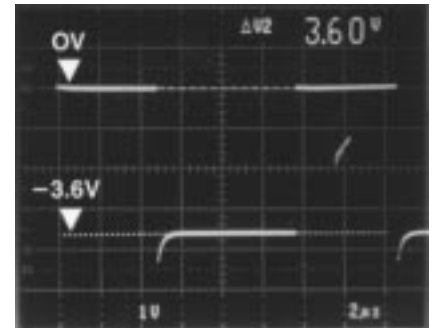


Figure 3-13. Effect of connecting a 450 Ω Bias/Offset probe (offset = 0 V). Minus level has been reduced by 10%.

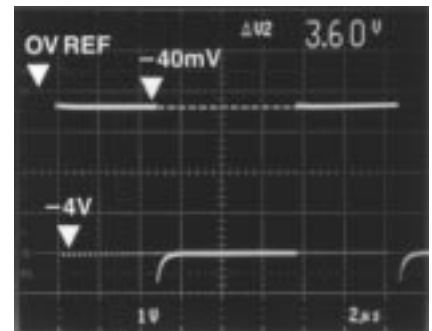


Figure 3-14. Bias/Offset adjusted for -4 V . Signal current at the -4 V level is zero. Current flow at ground level is maximum. Peak to peak amplitude remains the same (10% down).

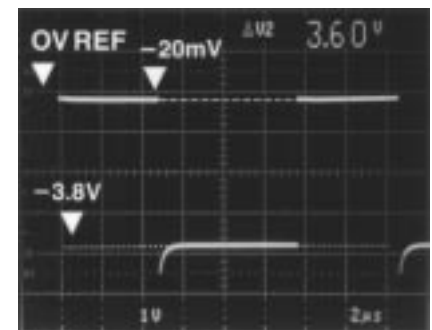


Figure 3-15. Bias/Offset adjusted for -2 V . Load current distributed between the negative and positive-going swings. Peak to peak amplitude remains the same (10% down).

Bias/Offset probes like the Tektronix P6230 or P6231 have bandwidths to 1.5 GHz, 450 Ω input R, and 1.3 pF (P6230), or 1.6 pF (P6231) input C.

They provide offset voltages of ± 5 V DC, and function with 1 M Ω or 50 Ω input systems (P6231, 50 Ω only).

The P6230 obtains operating power, either from the scope itself, or from the Tektronix 1101A or 1102 Power Supply.

The P6231 is designed to operate with the Tektronix 11000 Series scopes, and obtains operating power and bias/offset from the scope. Offset is selectable from the mainframe touch screen.

Differential Probing Techniques.

Accessing small signals elevated from ground, either at an AC level or a combination of AC and DC, requires the use of differential probes and a differential amplifier system.

One of the problems associated with differential measurements is the maintenance of high common mode rejection ratio (CMRR) at high common mode frequencies.

Poor common mode performance allows a significant portion of the common (elevated) voltage to appear across the differential probe's inputs. If the common mode voltage is pure DC, the result may only be a displayed baseline shift. However, if the common mode voltage is AC, or a combination of AC and DC, a significant portion may appear across the differential input and will mix with the desired signal.

Figure 3-16 shows the basic items necessary to make a differential measurement.

In this example two similar but un-matched passive probes are used. The probe ground leads are usually either removed or clipped together. They are **never** connected to the elevated DUT (device under test).

CMRR depends upon accurate matching of the probe-pair's electrical characteristics, including cable length. System CMRR can be no better than the differential amplifier's specifications, and in all cases, CMRR degrades as a function of frequency.

Figure 3-17 shows a simplified diagram of a DUT with a pulsed output of 1 V p-p floating on a 5 V p-p 20 MHz sinewave.

CMRR at 20 MHz is a poor 10:1 because of the un-matched probes.

Observed signal. (referred to probe input) = 1 V p-p pulse + (5 V p-p sine/10) = 1 V p-p pulse + 0.5 V p-p sine.

Figure 3-18a shows what the displayed waveform might look like under the conditions shown in figure 3-17.

In comparison, figures 3-18b and 3-18c show what the displayed signal might look like at CMRR's of 100:1 and 1000:1.

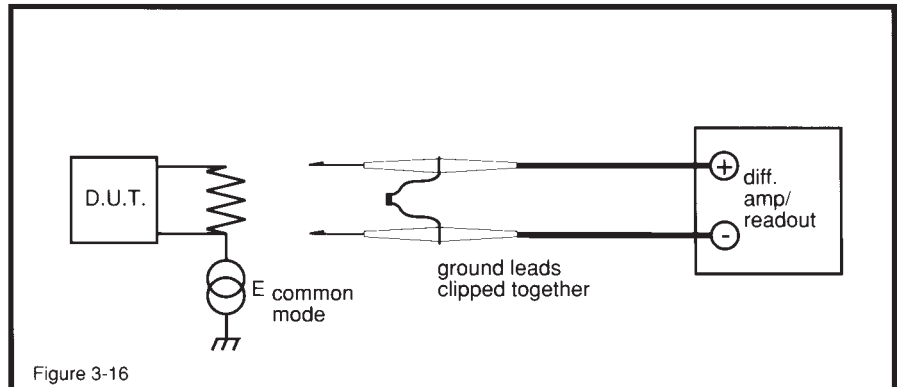


Figure 3-16. Basic connections to a device under test to make a differential measurement.

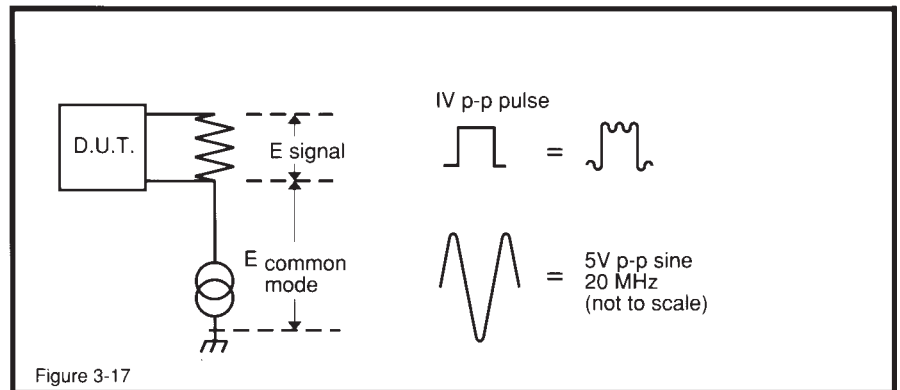
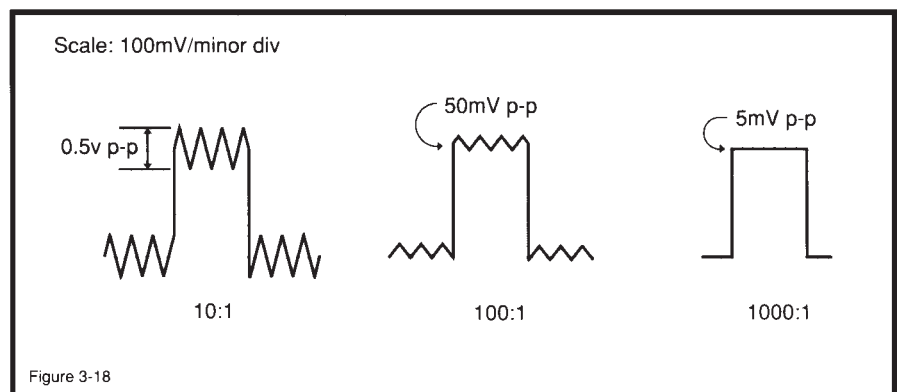


Figure 3-17. Simplified diagram. Elevated DUT. Common mode rejection is 10:1 at 20 MHz.



Figures 3-18, a, b and c. Displayed waveforms from the circuit shown in figure 3-17 at CMRR's of 10:1, 100:1 and 1000:1.

APPENDIX B

Measuring Amplifier Settling Time

High resolution measurement of amplifier settling at high speed is often necessary. Frequently, the amplifier is driven from a digital-to-analog converter (DAC). In particular, the time required for the DAC-amplifier combination to settle to final value after an input step is especially important. This specification allows setting a circuit's timing margins with confidence that the data produced is accurate. The settling time is the total length of time from input step application until the amplifier output remains within a specified error band around the final value.

Figure B1 shows one way to measure DAC amplifier settling time. The circuit uses the false sum node technique. The resistors and amplifier form a summing network. The amplifier output will step positive when the DAC moves. During slew, the oscilloscope probe is bounded by the diodes, limiting voltage excursion. When settling occurs, the summing node is arranged so the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. Several flaws exist. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction will influence observed settling waveforms. The 20pF probe shown alleviates this problem but its 10X attenuation

sacrifices oscilloscope gain. 1X probes are not suitable because of their excessive input capacitance. An active 1X FET probe might work, but another issue remains.

The clamp diodes at the probe point are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The diodes' 600mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question (for a discussion of oscilloscope overdrive considerations, see the Tutorial Section on Oscilloscopes). With the oscilloscope set at 1mV per division, the diode bound allows a 600:1 overdrive. Schottky diodes can cut this in half, but this is still much more than any real-time vertical amplifier is designed to accommodate.¹ The oscilloscope's overdrive recovery will completely dominate the observed waveform and all measurements will be meaningless.

One way to achieve reliable settling time measurements is to clip the incoming waveform in *time*, as well as amplitude. If the oscilloscope is prevented from seeing the waveform until settling is nearly complete, overload is avoided. Doing this requires placing a switch at the settle circuit's output and controlling it with an input-triggered, variable delay. FET switches are not suitable because of their gate-source capacitance. This capacitance will allow gate drive artifacts to corrupt the oscilloscope display,

Note 1: See Reference 3 for history and wisdom about vertical amplifiers.

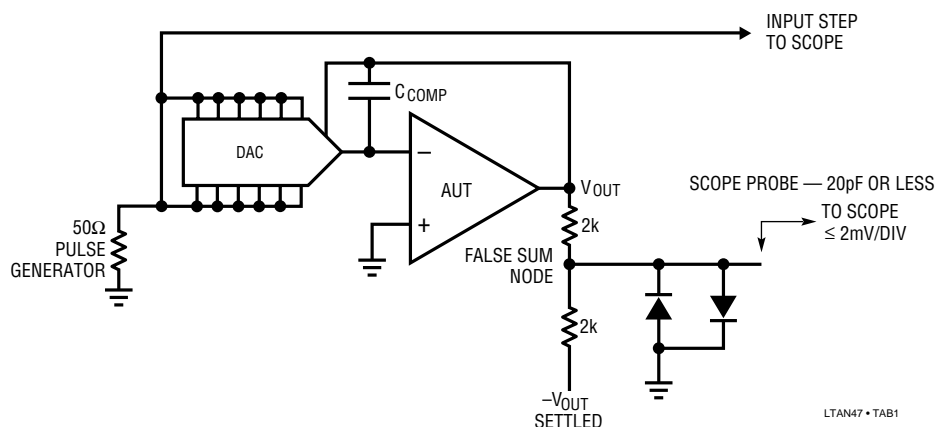


Figure B1. One (Not Very Good) Way to Measure DAC-Op Amp Settling Time

producing confusing readings. In the worst case, gate drive transients will be large enough to induce overload, defeating the switch's purpose.

Figure B2 shows a way to implement the switch which largely eliminates these problems. This circuit allows settling within 1mV to be observed. The Schottky sampling bridge is the actual switch. The bridge's inherent balance, combined with matched diodes and very high speed complementary bridge switching, yields a clean switched output. An output buffer stage unloads the settle node and drives the diode bridge.

The operation of the DAC-amplifier is as before. The additional circuitry provides the delayed switching function, eliminating oscilloscope overdrive. The settle node is buffered by A1, a unity gain broadband FET input buffer with 3pF input capacitance and 350MHz bandwidth. A1 drives the Schottky bridge. The pulse generator's output fires the 74123 one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way the oscilloscope's output is reliable and meaningful data may be taken. The one shot's output is level shifted by the Q1-Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1-Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.² The bridge's output may be observed directly (by oscilloscopes with adequate sensitivity) or A2 provides a times 10 amplified version. A2's gain of 20 (and the direct output's $\div 2$ scaling) derives from the 2k-2k settle node dividers attenuation. A third output, taken directly from A1, is also available. This output, which bypasses the entire switching circuitry, is designed to be monitored by a sampling oscilloscope. Sampling oscilloscopes are inherently immune to overload.³ As such, a good test of this settling time test fixture (and the above statement) is to compare the signals displayed by the sampling 'scope and the Schottky-bridge-aided real time 'scope. As an *additional* test, a completely different method of measuring settling time (albeit considerably more complex) described by Harvey⁴ was also employed. If all three approaches

represent good measurement technique and are constructed properly, results should be identical.⁵ If this is the case, the identical data produced by the three methods has a high probability of being valid. Figures B3, B4 and B5 show settling time details of an AD565A DAC and an LT1220 op amp. The photos represent the sampling bridge, sampling 'scope and Harvey methods, respectively. Photos B3 and B5 display the input step for convenience in ascertaining elapsed time. Photo B4, taken with a single trace sampling oscilloscope (Tektronix 1S1 with P6032 cathode follower probe in a 556 mainframe) uses the leftmost vertical graticule line as its zero time reference. All methods agree on 280ns to 0.01% settling (1mV on a 10V step). Note that Harvey's method inherently adds 30ns, which must be subtracted from the displayed 310ns to get the real number.⁶ Additionally, the shape of the settling waveform, in every detail, is identical in all three photographs. This kind of agreement provides a high degree of credibility to the measured results.

Some poorly designed amplifiers exhibit a substantial thermal tail after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking settling at high speed, it is always a good idea to slow the oscilloscope sweep down and look for thermal tails. Often the thermal tail's effect can be accentuated by loading the amplifier's output. Such a tail can make an amplifier appear to have settled in a much shorter time than it actually has.

To get the best possible settling time from any amplifier, the feedback capacitor, C_F , should be carefully chosen. C_F 's purpose is to roll-off amplifier gain at the frequency which permits best dynamic response. The optimum value for C_F will depend on the feedback resistor's value and the characteristics of the source. DAC's are one of the most common sources and also one of the most difficult. DAC's current outputs must often be converted to a

Note 2: The Q1-Q4 bridge switching scheme, a variant of one described in Reference 14, was developed at LTC by George Feliz.

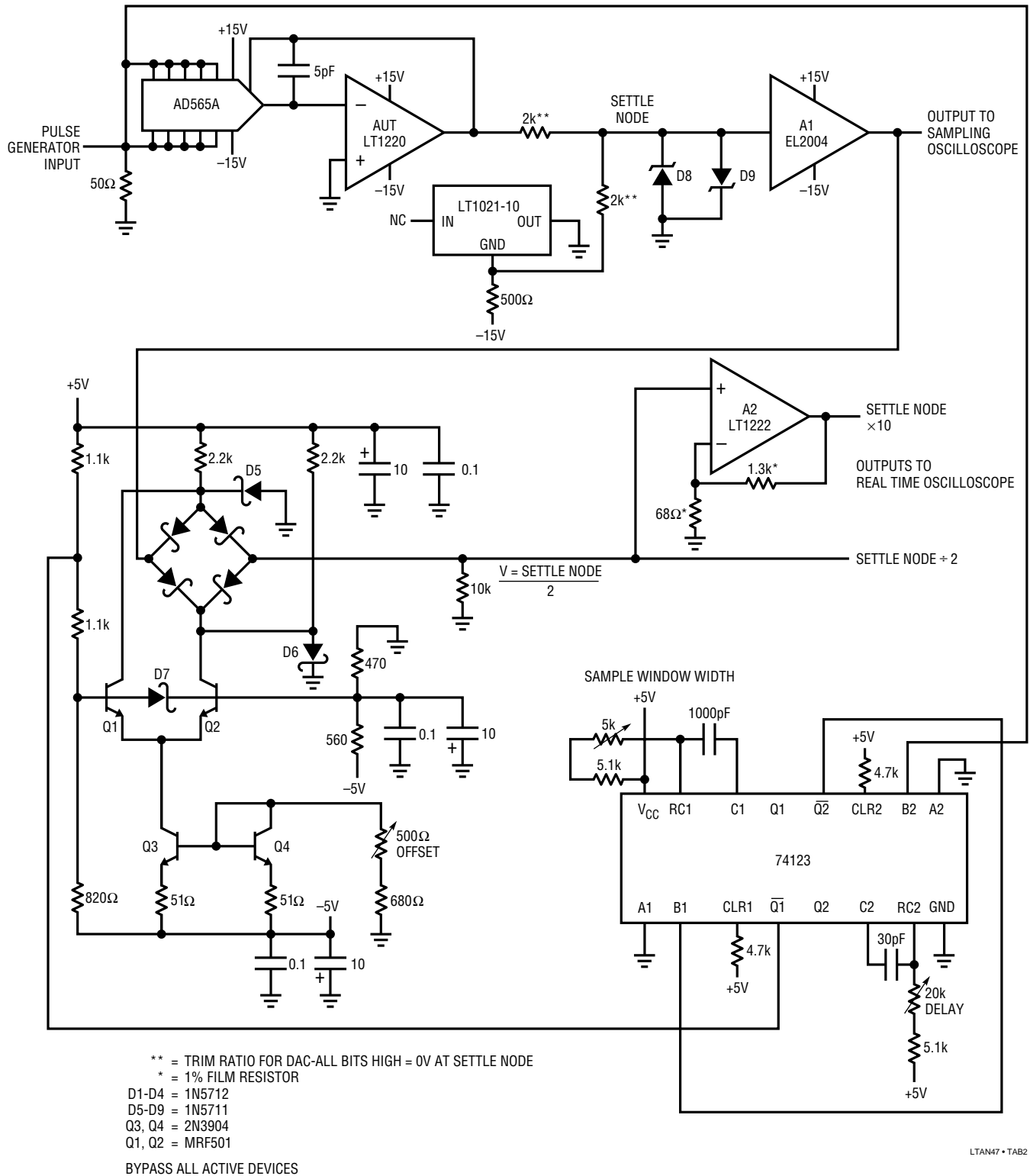
Note 3: See References 7, 8 and 18.

Note 4: See Reference 17.

Note 5: Construction details of the settling time fixture discussed here appear (literally) in Appendix F, "Additional Comments on Breadboarding". Also see the Tutorial Section on Breadboarding Techniques.

Note 6: See Reference 17.

Application Note 47



LTAN47 • TAB2

Figure B2. Settling Time Test Circuit Using a Sampling Bridge Eliminates Oscilloscope Overdrive

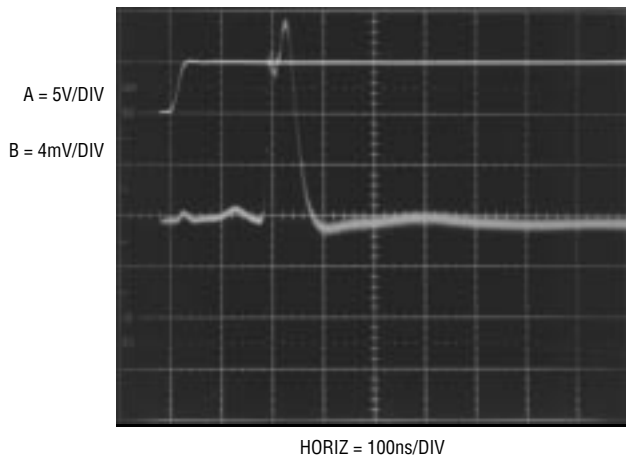


Figure B3. 280ns Settling Time as Measured by Figure B2's Circuit. Sampling Switch Closes Just Before Third Vertical Division, Allowing Settling Detail to be Observed Without Overdriving the Oscilloscope

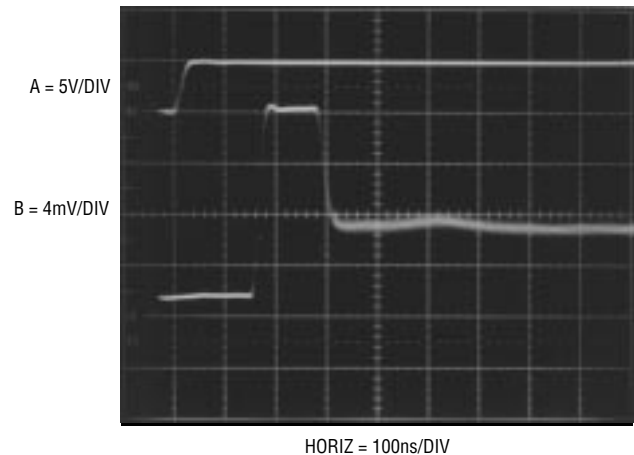


Figure B5. 280ns Settling Time as Measured by Harvey's Method. After Subtraction of this Method's Inherent 30ns Delay, Settling Time and Waveform Shape are Identical to Figures B3 and B4

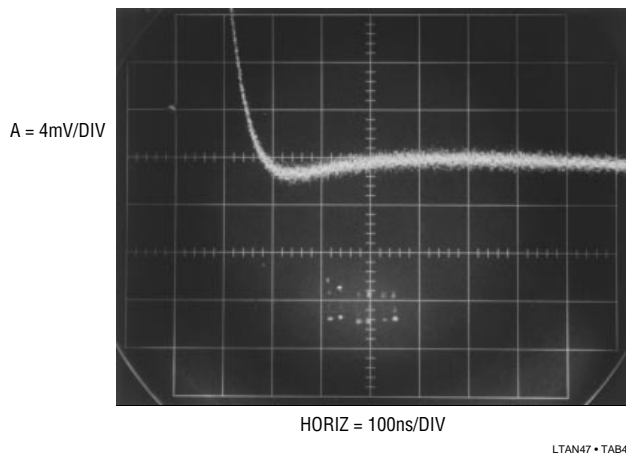


Figure B4. 280ns Settling Time as Measured at Figure B2's Sampling Oscilloscope Output by a Sampling 'Scope. Settling Time and Waveform Shape is Identical to Figure B3

voltage. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns or less but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the

amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance and it varies with code. Bipolar DACs typically have 20pF-30pF of capacitance, stable over all codes. Because of their output capacitance, DAC's furnish an instructive example in amplifier compensation. Figure B6 shows the response of an industry standard DAC-80 type and a relatively slow (for this publication) op amp. Trace A is the input, while Traces B and C are the amplifier and settle outputs, respectively. In this example no compensation capacitor is used and the amplifier rings badly before settling. In Figure B7, an 82pF unit stops the ringing and settling time goes down to 4 μ s. The overdamped response means that C_F dominates the capacitance at the AUT's input and stability is assured. If fastest response is desired, C_F must be reduced. Figure B8 shows critically damped behavior obtained with a 22pF unit. The settling time of 2 μ s is the best obtainable for this DAC-amplifier combination. Higher speed is possible with faster amplifiers and DACs but the compensation issues remain the same.

Application Note 47

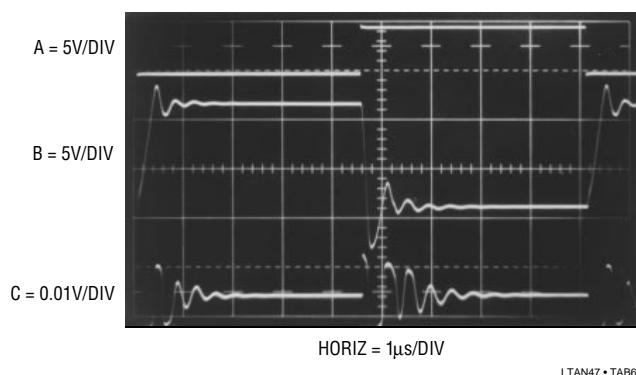


Figure B6. No Feedback Capacitor

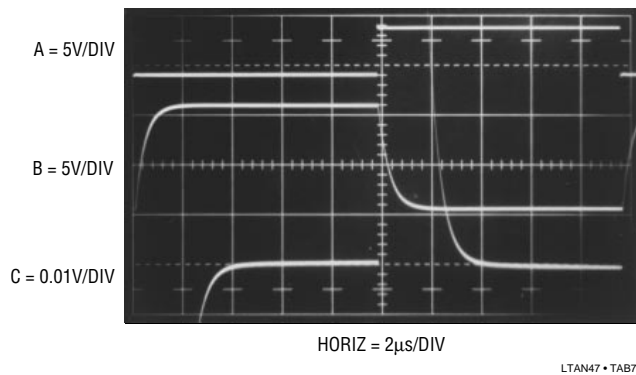


Figure B7. Relatively Large Feedback Capacitor

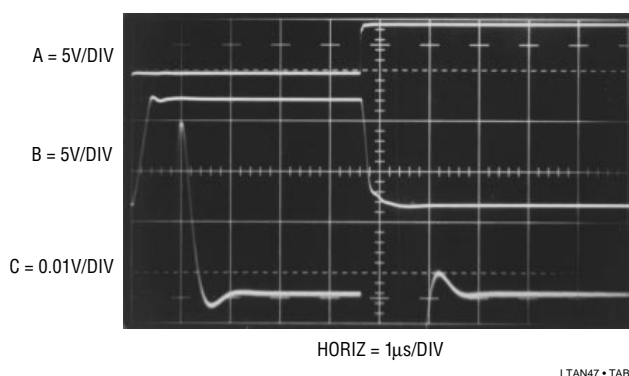


Figure B8. Reduced Feedback Capacitor Gives Fastest Settling

Figures B6-B8. Effects of Different Feedback Capacitors on a DAC-Op Amp Combination

APPENDIX C

The Oscillation Problem – Frequency Compensation Without Tears

All feedback systems have the propensity to oscillate. Basic theory tells us that gain and phase shift are required to build an oscillator. Unfortunately, feedback systems, such as operational amplifiers, have gain and phase shift. The close relationship between oscillators and feedback amplifiers requires careful attention when an op amp is designed. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when feedback is applied. Further, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This is why feedback loop enclosed stages can cause oscillation.

A large body of complex mathematics is available which describes stability criteria and can be used to predict stability characteristics of feedback amplifiers. For the most sophisticated applications, this approach is required to achieve optimum performance.

However, little has appeared which discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. Specifically, a practical approach to stabilizing amplifier-power gain stage combinations is discussed here, although the considerations can be generalized to other feedback systems.

Oscillation problems in amplifier-power booster stage combinations fall into two broad categories; local and loop

oscillations. *Local* oscillations can occur in the boost stage, but should not appear in the IC op amp, which presumably was debugged prior to sale. These oscillations are due to transistor parasitics, layout and circuit configuration-caused instabilities. They are usually relatively high in frequency, typically in the 0.5MHz to 100MHz range. Usually, local booster stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation. Text Figure 101, repeated here as Figure C1 for reader convenience, furnishes an instructive example. The Q1, Q2 emitter follower pair has reasonably high f_t . These devices will oscillate if driven from a low impedance source (see insert, Figure C1 and References 43 and 44). The 100Ω resistor and the ferrite beads are included to make the op amps output look like a higher impedance to prevent problems. Q5 and Q6, also followers, have even higher f_t , but are driven from 330Ω sources, eliminating the problem. The photo in Figure C2 shows Figure C1 following an input with the 100Ω resistor and ferrite beads removed. Trace A is the input, while Trace B is the output. The resultant high frequency oscillation is typical of locally caused disturbances. Note that the major loop is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high f_t transistors unless they are needed. When high frequency devices are in use, plan layout carefully. In very stubborn cases, it may be necessary to

lightly bypass transistor junctions with small capacitors or RC networks. Circuits which use local feedback can sometimes require careful transistor selection and use. For example, transistors operating in a local loop may require different f_t s to achieve stability. Emitter followers are notorious sources of oscillation and should never be directly driven from low impedance sources (again, see References 43 and 44).

Loop oscillations are caused when the added gain stage supplies enough delay to force substantial phase shift. This causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain combined with the added delay causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10Hz-1MHz.

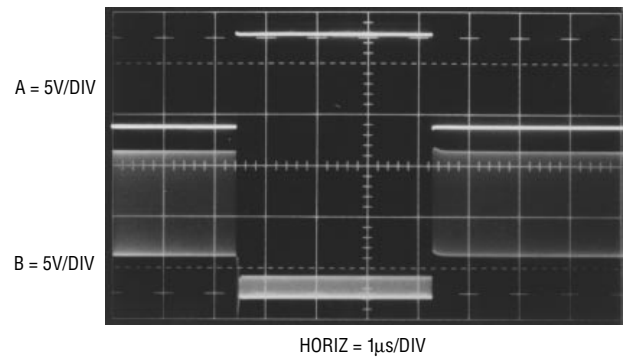


Figure C2. Local Oscillations Due to Booster Stage Instabilities

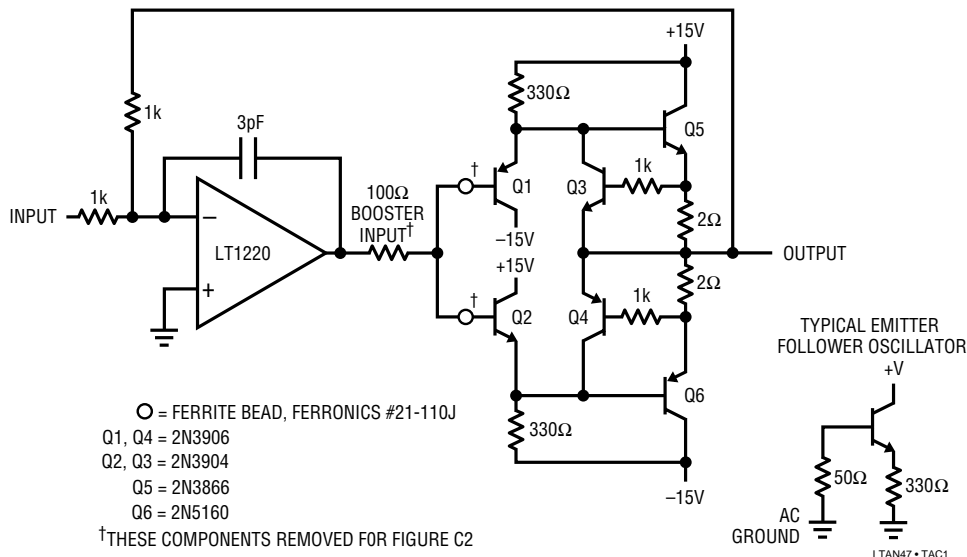


Figure C1. Figure 101's Booster Circuit with a Few Components Removed Begins Our Study of Loop Stability

Application Note 47

A good way to eliminate loop-caused oscillations is to limit the gain-bandwidth of the control amplifier. If the booster stage has higher gain-bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When control amplifier gain-bandwidth dominates, oscillation is assured. Under these conditions, the control amplifier hopelessly tries to servo a feedback signal which consistently arrives too late. The servo action takes the form of an electronic tail chase with oscillation centered around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations it is preferable to brute force compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling off control amplifier gain-bandwidth. The feedback capacitor serves only to trim step response and should not be relied on to stop outright oscillation.

Figures C3 and C4 illustrate these issues. The LT1006 amplifier used with the LT1010 current buffer produces the output shown in Figure C4. As before, Trace A is the input and Trace B the output. The LT1006 has less than

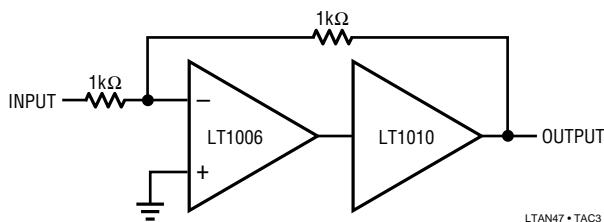


Figure C3. A Slow Op Amp and a Medium Speed Booster

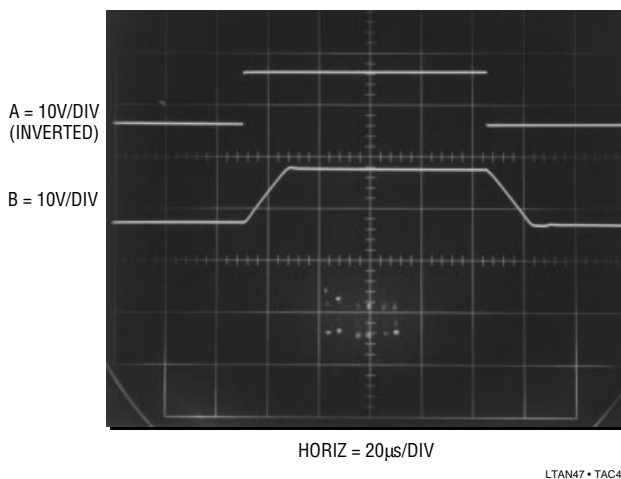


Figure C4. Loop Stability is “Free” When the Op Amp is Much Slower than the Booster

1MHz gain-bandwidth. The LT1010’s 20MHz gain-bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1006’s internal roll-off is well below that of the output stage and stability is achieved with no external compensation components. Figure C5 uses a 100MHz bandwidth LT1223 as the control amplifier. The associated photo (Figure C6) shows the results. Here, the control amplifier’s roll-off is well beyond the output stage’s, causing problems. The phase shift through the LT1010 is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the control amplifier’s gain-bandwidth.

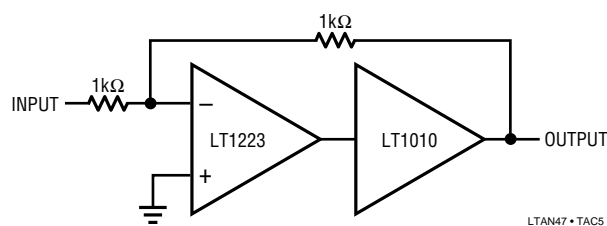


Figure C5. A Fast Op Amp and a Medium Speed Booster

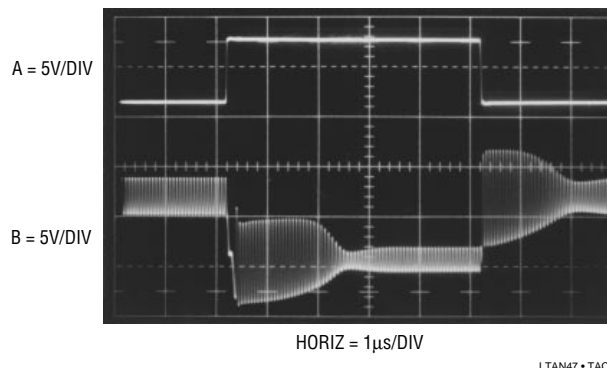


Figure C6. Loop Oscillation is “Free” When the Op Amp is Much Faster than the Booster

The fact that the slower op amp circuit doesn’t oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is free. The faster amplifier makes the AC characteristics of the output stage become significant and requires roll-off components for stability. Practically, the LT1223’s speed is simply too much for the LT1010. A somewhat slower amplifier is the way to go. Alternately, a faster booster may be employed. Figure C7 attempts this, but doesn’t quite make it. Photo C8 is less corrupted, but 100MHz oscillation indicates the booster stage (borrowed from text Figure 101) is still too slow for the LT1223. Attempts to use another booster design in Figure C9 (similarly purloined from text Figure

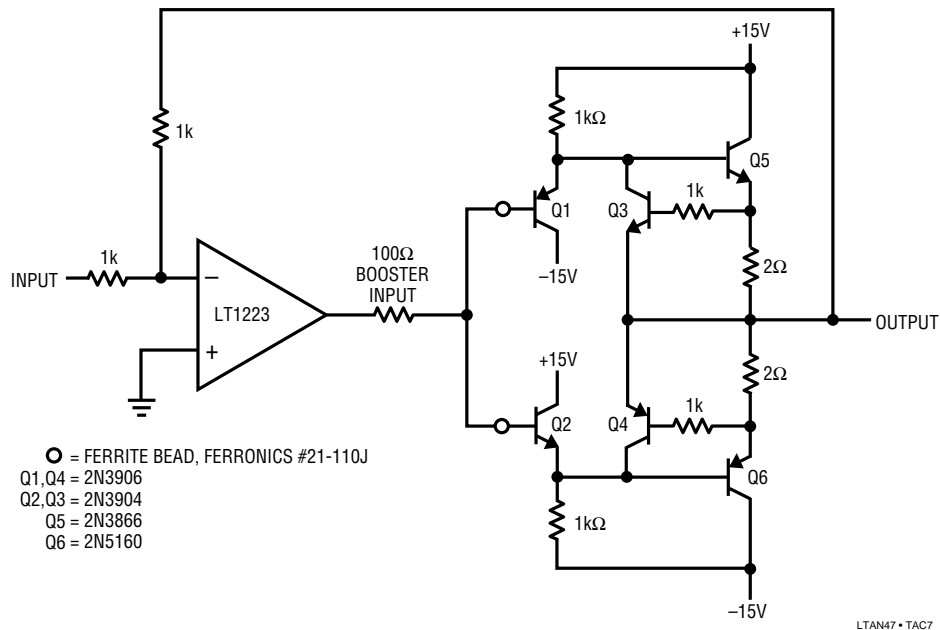


Figure C7. A Very Fast Amplifier with a Fast Booster

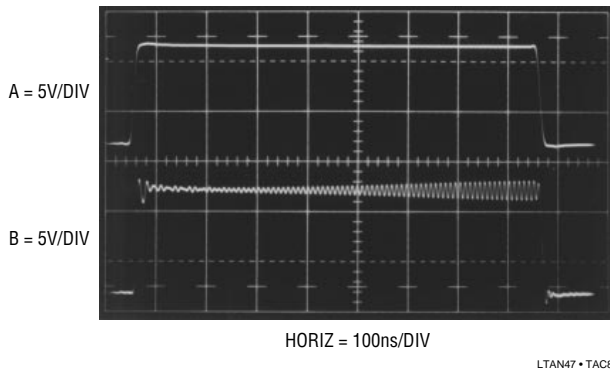


Figure C8. Figure C7's Booster is Not Quite Quick Enough to Prevent Loop Oscillation

104) fail for the same reason. Figure C10 shows 40MHz oscillation, indicative of this high power booster's slower speed.

Figure C11 has much more pleasant results. Here a 45MHz gain-bandwidth LT1220 has been substituted for the 100MHz LT1223 in Figure C7's circuit. The slower amplifier, combined with light local compensation, works well with the booster stage in its loop. Figure C12 shows a well controlled high speed output, nicely damped, with no sign of oscillations.

Power boosters are not the only things that can be placed within an amplifier's feedback loop. Text Figure 140's

current source, reproduced here as Figure C13, is an interesting variation. There is no power booster in the loop, but rather a 40MHz differential amplifier with a gain of 10. To stabilize the circuit the slowest amplifier in the 1190 family, the 50MHz LT1190, is chosen. The local 100pF feedback slows it down a bit more and the loop is fast and stable (Figure C14). What happens if we remove the 100pF feedback path? Figure C15 shows that the loop is no longer stable under this condition because the LT1190 control amplifier cannot servo the phase shifted feedback at higher frequency. Put that 100pF capacitor back in!

It's worth mentioning that similar results to those obtained back in Figure C3 are obtainable by substituting a very slow control amplifier (e.g., an LT1006 which has less than 1MHz gain-bandwidth). The slower amplifier would give "free" compensation, eliminating the necessity for the 100pF unit. However, the circuit's frequency response would be severely degraded.

Text Figure 142's high power current source furnishes further instruction. This loop contains the differential amplifier *and* a booster, seemingly making things even more difficult. Figure C16, recognizable as text Figure 142's high power current source with the 100pF local compensation removed, oscillates above 10MHz. Replacing the compensation restores proper response. Figure

Application Note 47

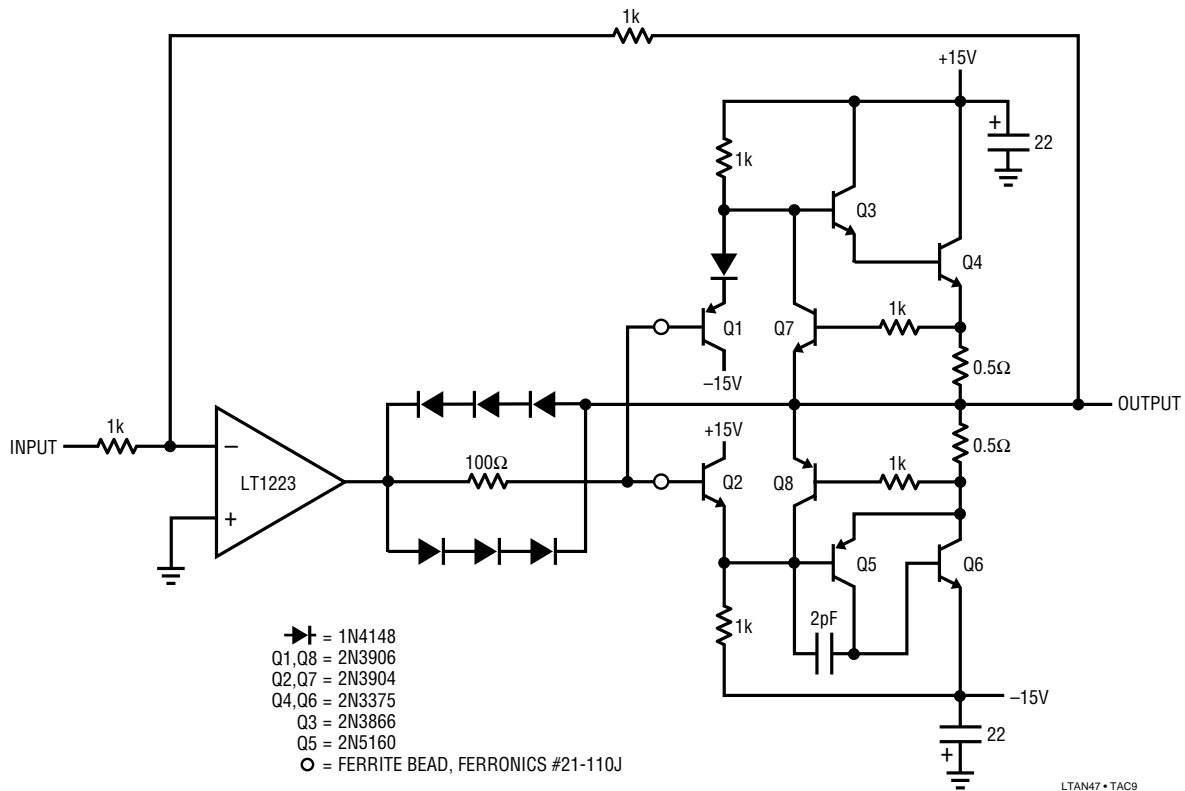


Figure C9. A Very Fast Amplifier with a Fast High Power Booster

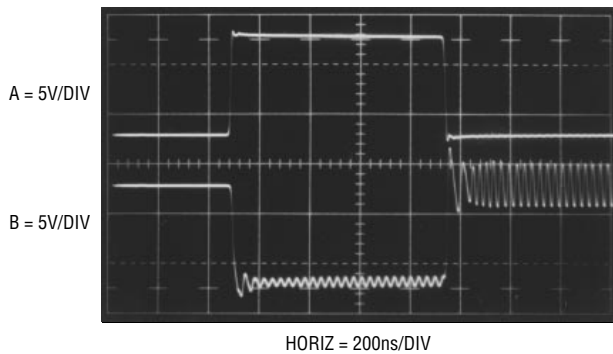


Figure C10. C9's High Power Booster is Fast But Causes Loop Oscillations

C17 shows the loop has no oscillations. What this tells us is that the control amplifier doesn't care just what generates the causal feedback between its input and output, so long as there isn't excessive delay. This circuit has a fairly busy feedback loop, but the control amplifier is oblivious to its bustling nature....unless you leave that 100pF feedback capacitor out!

When compensating loops like these, remember to investigate the effects of various loads and operating conditions. Sometimes a compensation scheme which appears fine gives bad results for some conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

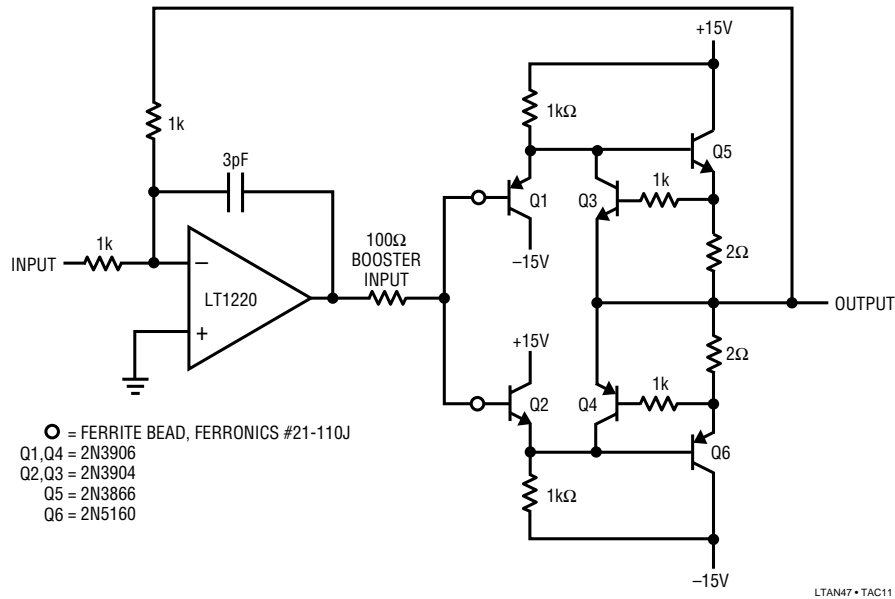


Figure C11. Figure 101 (Again) with 100Ω Resistor and Beads Reinstalled

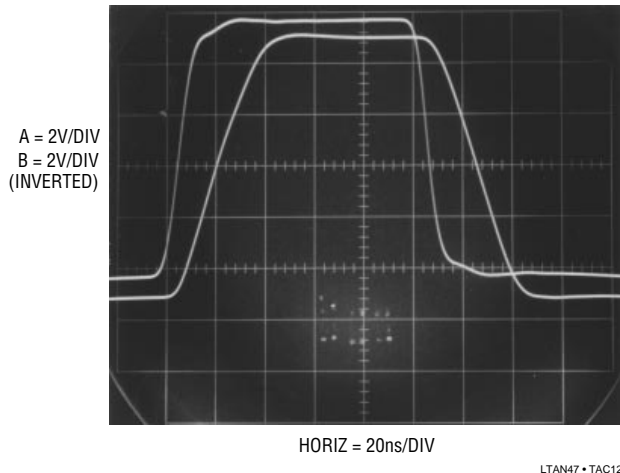


Figure C12. Lovely!

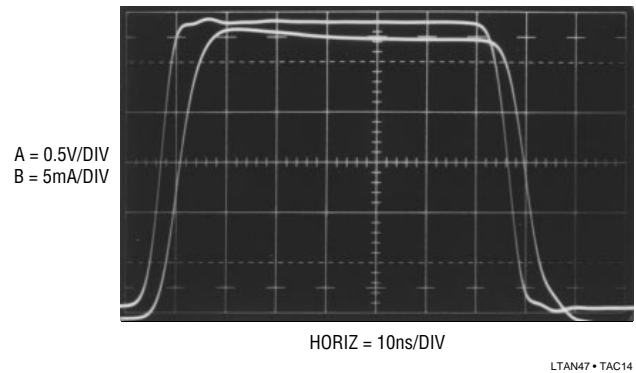


Figure C14. Response of the Current Source with the RC Components in Place

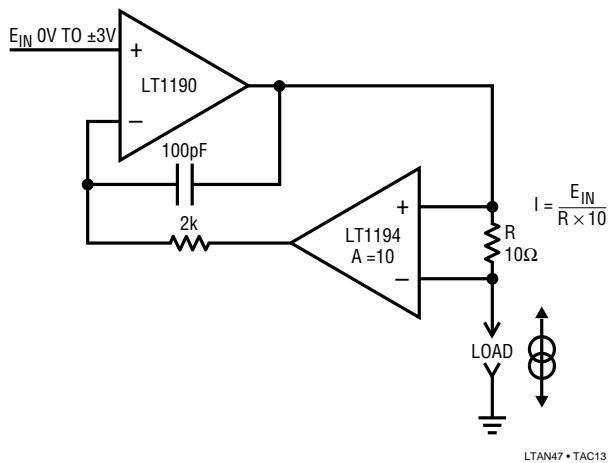


Figure C13. Figure 140's Current Source. What Do the RC Components Do?

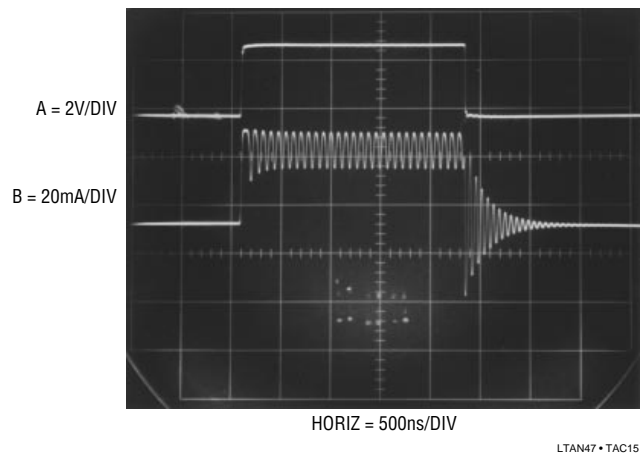


Figure C15. Removing the 100pF Capacitor Allows the Op Amp to See Phase Shifted Feedback, Causing Oscillation. Put that 100pF Back In!

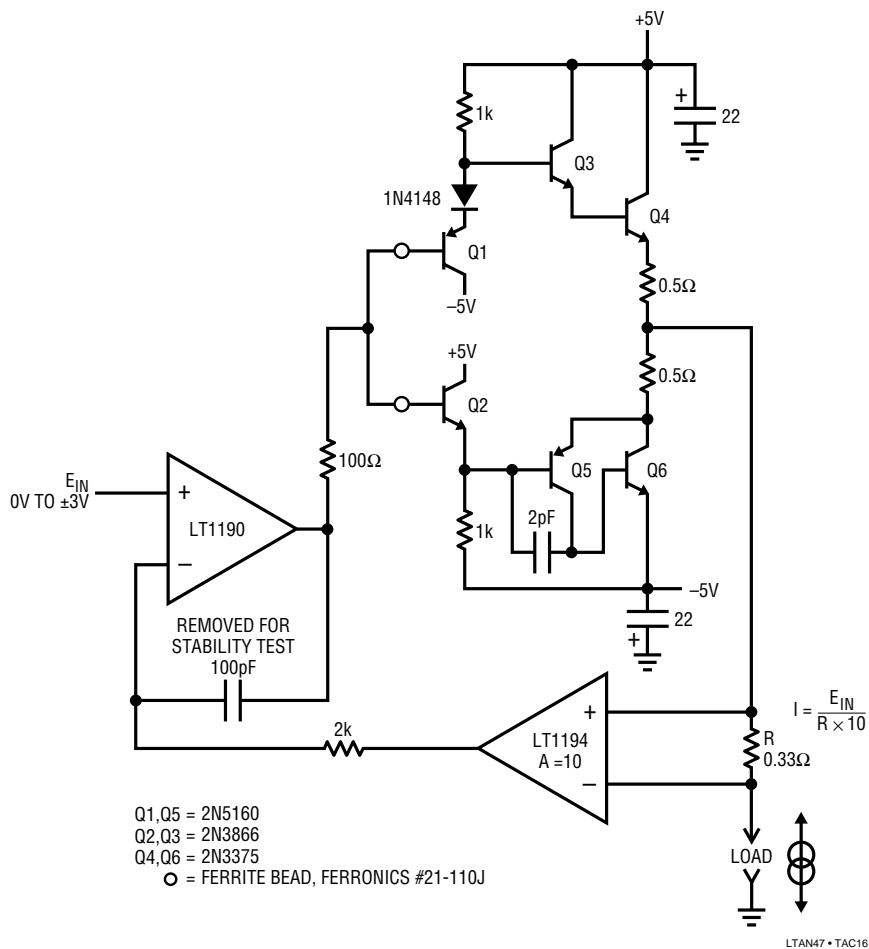


Figure C16. Text Figure 142's High Power Current Source. When the 100pF Capacitor is Removed, 10MHz Loop Oscillations Result

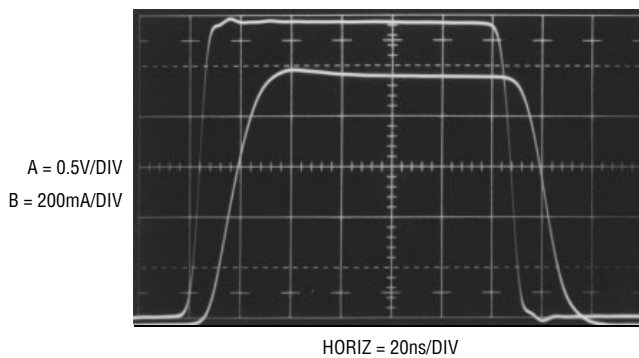


Figure C17. Much Better. Leave that 100pF Capacitor in There!

APPENDIX D

Measuring Probe-Oscilloscope Response

Verifying the rise time limit of wideband test equipment set-ups is a difficult task. In particular, the end-to-end rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure D1's circuit does this, providing a 1ns pulse with rise and fall times inside 350ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage step-up network. L1 periodically receives charge and its flyback discharge delivers high voltage events to the step-up network. A portion of the step-up network's DC output is fed back to the LT1073 via the 10M, 24k divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the 1M- 2pF combination. Q1, a 40V breakdown device, non-destructively avalanches when C1 charges high enough. The result is a quickly rising, very fast pulse across R4. C1

discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free running oscillation at about 200kHz.^{1,2} Figure D2 shows the output pulse. A 1GHz sampling oscilloscope (Tektronix 556 with 1S1 sampling plug-in) measures the pulse at 10V high with about a 1ns base. Rise time is 350ps, with fall time also indicating 350ps. There is a slight hint of ring after the falling edge, but it is well controlled. The figures may actually be faster, as the 1S1 is specified with a 350ps limit.³

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All good devices switched in less than 650ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF-4pF. Ground plane type construction with

Note 1: This method of generating fast pulses borrows heavily from the Tektronix type 111 Pretrigger Pulse Generator. See References 8 and 25.

Note 2: This circuit replaces the tunnel diode based arrangement shown in AN13, Appendix D. While AN13's circuit works well, it generates a smaller, more irregularly shaped pulse and the tunnel diodes have become quite expensive.

Note 3: Just before going to press the pulse was measured at Hewlett-Packard Laboratories with a HP-54120B 12GHz sampling oscilloscope. Rise and fall times were 216ps and 232ps, respectively. Photo available on request.

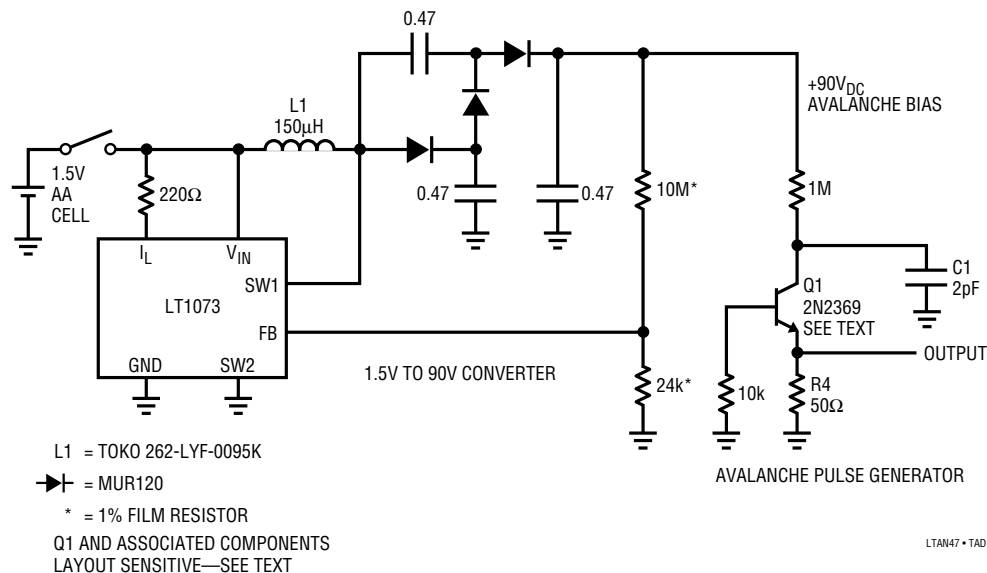


Figure D1. 350ps Rise/Fall Time Avalanche Pulse Generator

Application Note 47

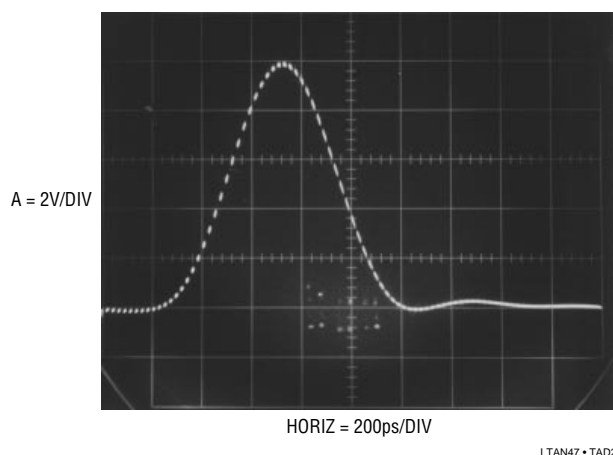


Figure D2. The Avalanche Pulse Generator's Output Monitored on a 1GHz Sampling Oscilloscope

high speed layout techniques are essential for good results from this circuit. Current drain from the 1.5V battery is about 5mA.

Figure D3 shows the physical construction of the actual generator. Power, supplied from a separate box, is fed into the generator's enclosure via a BNC connector. Q1 is mounted *directly* at the output BNC connector, with grounding and layout appropriate for wideband operation. Lead lengths, particularly Q1's and C1's, should be experimented with to get best output pulse purity. Figure D4 is the complete unit.

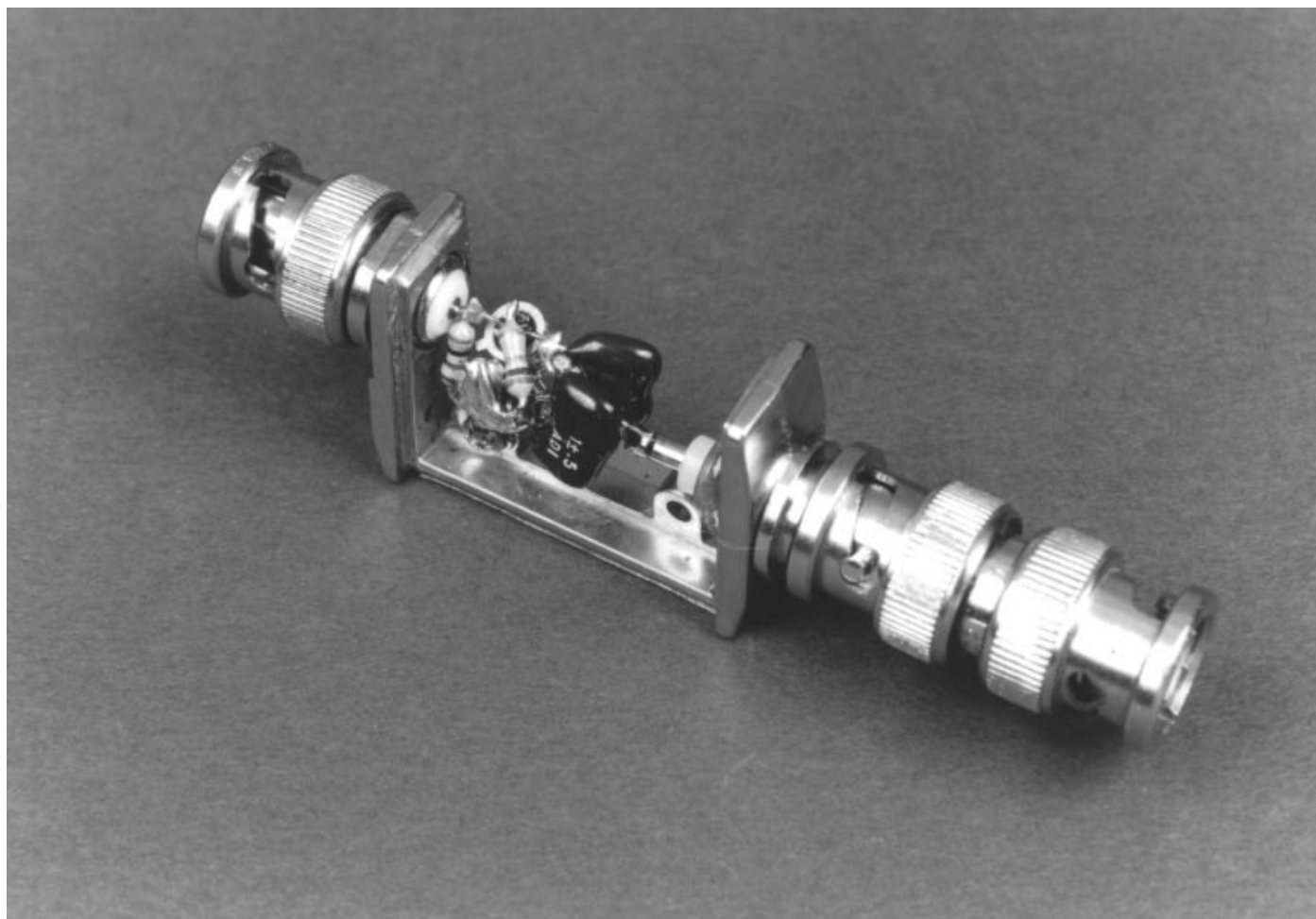


Figure D3. Details of the Avalanche Pulse Generator's Head. 90V_{DC} Enters at Lower Right BNC, Pulse Exits at Top Left BNC. Note Short Lead Lengths Associated with Output



LTAN47 • TAD4

Figure D4. The Packaged Avalanche Pulser. 1.5V-90V Converter is in the Black Box. Avalanche Head is at Left

APPENDIX E

An Ultra-Fast High Impedance Probe

Under most circumstances the 1pF-2pF input capacitance and 10M Ω resistance of FET probes is more than adequate for difficult probing situations. Occasionally, however, very high input resistance with high speed is needed. At some sacrifice in speed and input capacitance compared to commercial probes, it is possible to construct such a probe. Figure E1 shows schematic details. A1, a 350MHz hybrid FET buffer, forms the electrical core of the probe. This device is a low input capacitance, wideband FET source follower driving a fast bipolar output stage. The input of the probe goes to this device via a 51 Ω resistor, reducing the possibility of oscillations in the follower input stage when the probe sees low AC impedance. A1's output drives a guard shield around the probe's input line, reducing effective input capacitance to about 4pF. A ground referred shield encircles the guard shield, reducing pickup and making high quality ground connections to the circuit under test easy. A1 drives the output BNC cable to feed the oscilloscope. Normally, it is undesirable to back terminate the cable at A1 because the oscilloscope will see only half of A1's output. While a back termination provides the best signal dynamics, the resulting attenuation is a heavy penalty. The RC damper shown can be trimmed for best edge response while maintaining an unattenuated output.

What can't be seen in the schematic is the probe's physical construction. Very careful construction is required to

maintain low input capacitance, low bias current and wide bandwidth. The probe head is particularly critical. Every effort should be made to minimize the length of wire between A1's input and the probe tip. In our lab, we have found that discarded pieces of broken 10X probes, particularly attenuator boxes and probe heads, provide an excellent packaging basis for this probe.¹ Figure E2 shows the probe head. Note the compact packaging. Additionally, A1's package is arranged so that it's (not insubstantial) dissipated heat is transferred to the probe case body when the snap-on cover (shown in photo) is in place. This reduces A1's substrate temperature, keeping bias current down. A1's input is directly connected to the probe head to minimize parasitic capacitance. The power supply for A1, located in a separate enclosure, is fed in through separate wires. A1's output is delivered to the oscilloscope via conventional BNC hardware.

Figure E3 shows the probe output (Trace B) responding to an input (Trace A) as monitored on a 350MHz oscilloscope (Tektronix 485). Measured specifications for our version of this probe include a rise time of 6ns, 6ns delay and 58MHz bandwidth. The delay time contribution is about evenly split between the amplifier and cable. Input capacitance is about 4pF without the probe hook tip and 7pF with the hook tip. Input bias current measured 400pA and gain error about 5%. (A1 is an open loop device.)

Note 1: This is not to encourage or even accept the breakage of probes. The author regards the breakage of oscilloscope probes as the lowest possible human activity. The sole exception to this condemnation is poor quality probes, which should be destroyed as soon as their deficiencies are discovered.

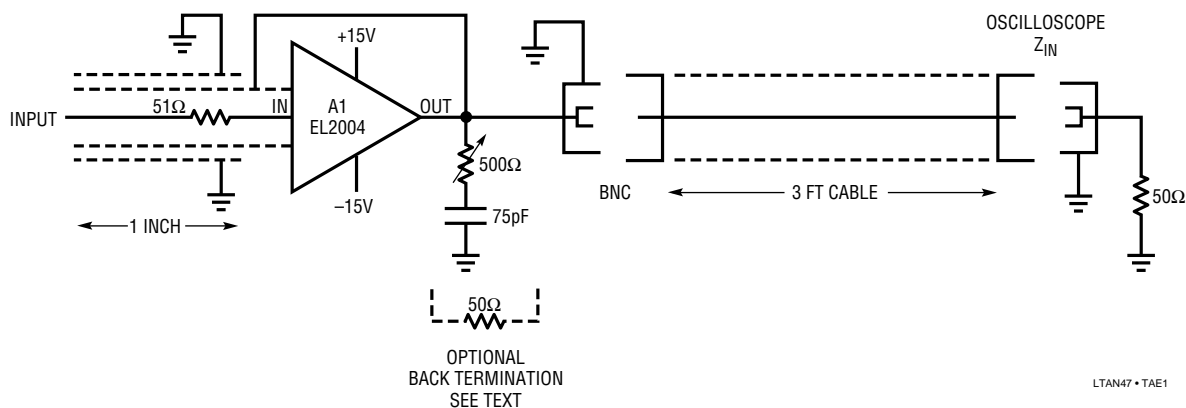
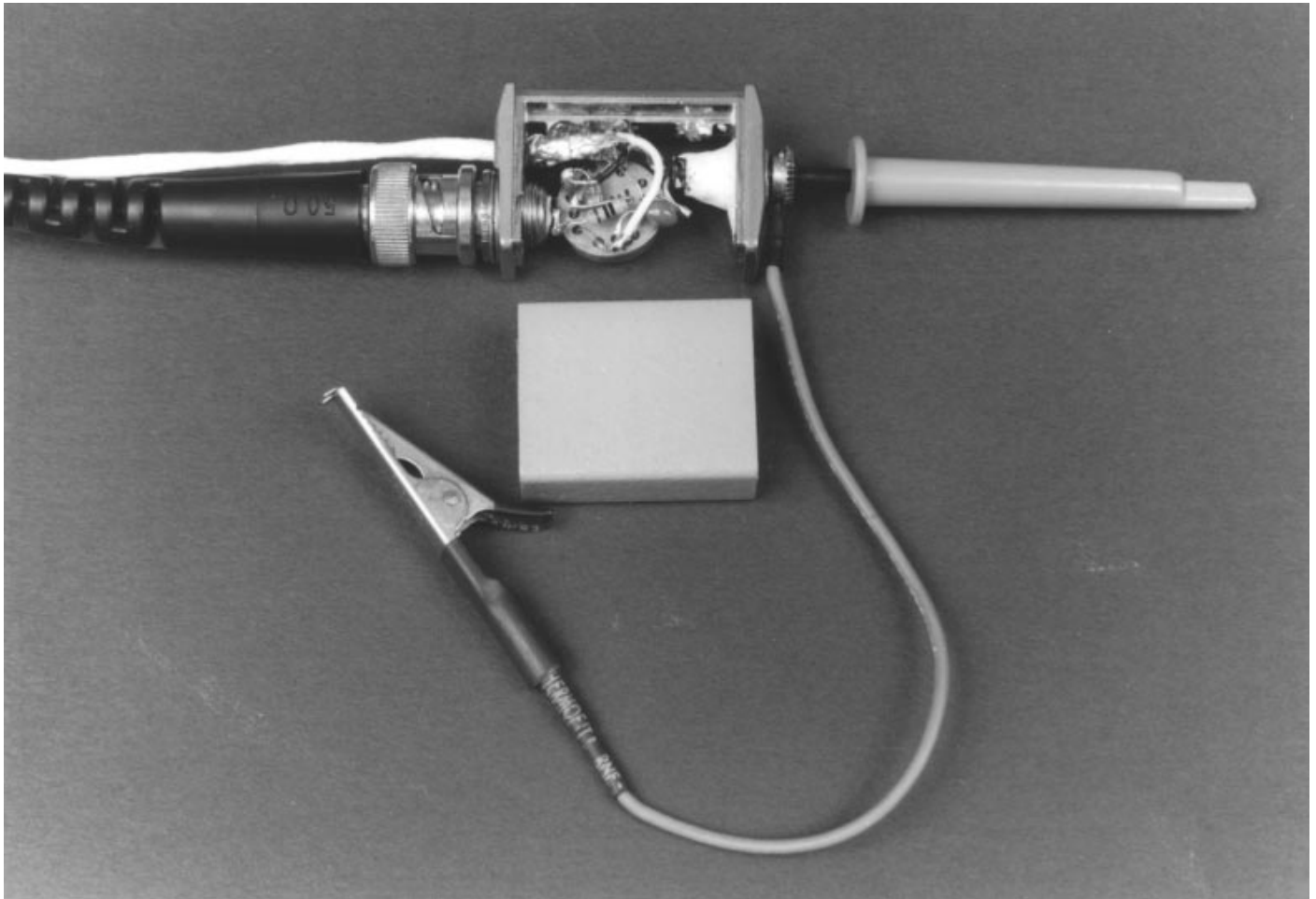
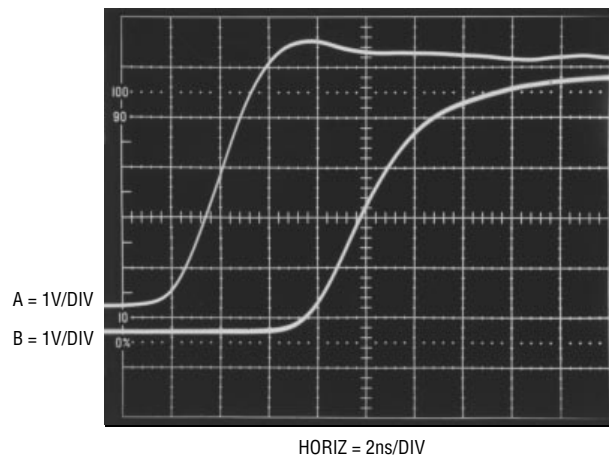


Figure E1. Ultra Fast Buffer Probe Schematic



LTAN47 • TAE2

Figure E2. Physical Layout of Ultra Fast Buffer Probe



LTAN47 • TAE3

Figure E3. Probe Response (Trace B) to Input Pulse (Trace A)

Application Note 47

APPENDIX F

Additional Comments on Breadboarding

This section contains, in visual form, commentary on some of the breadboards of the circuits described in the text. The breadboards appear in roughly corresponding

order to their text presentation and comments are brief but hopefully helpful. The bit pushers have commented software; why not commented hardware?

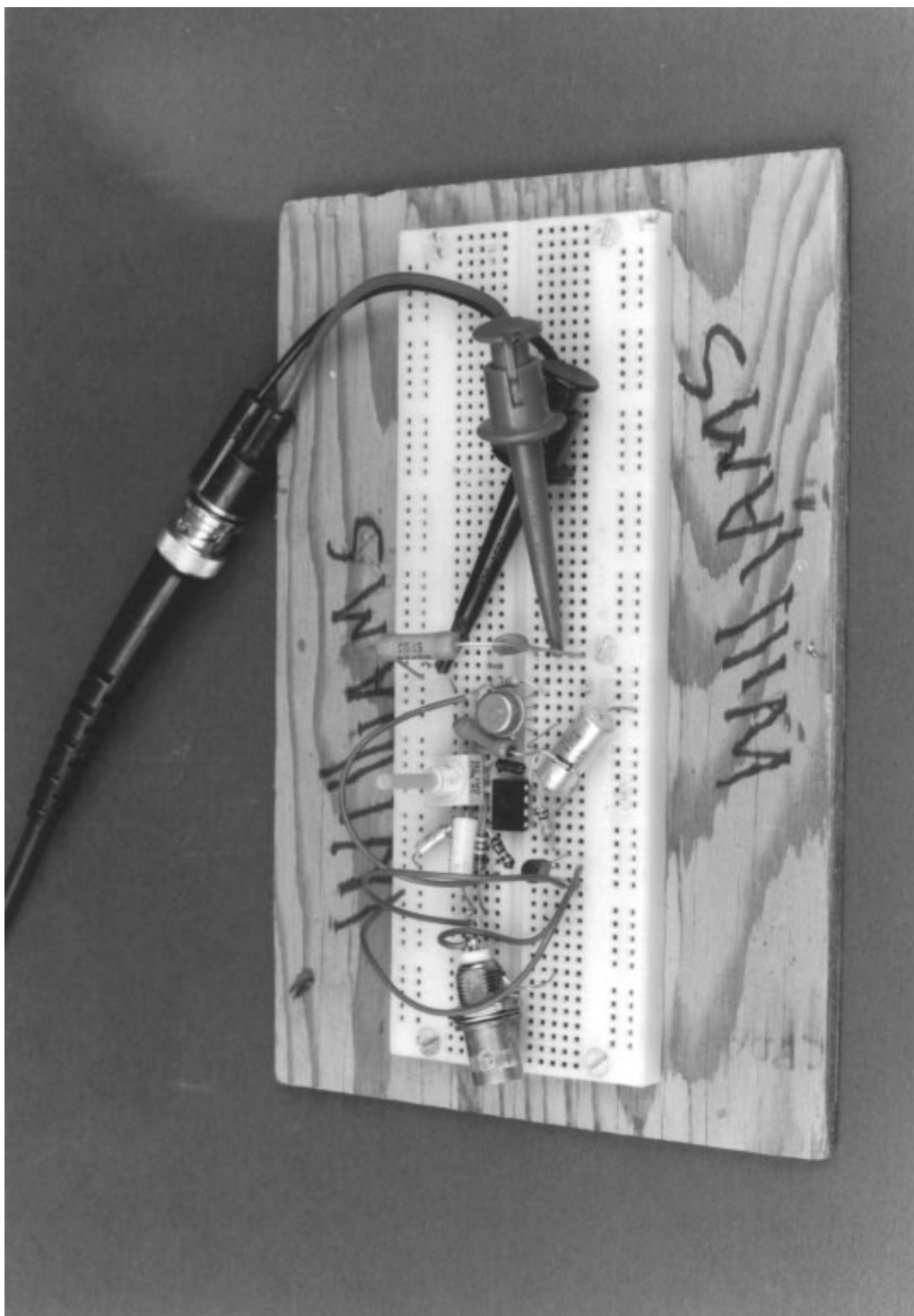
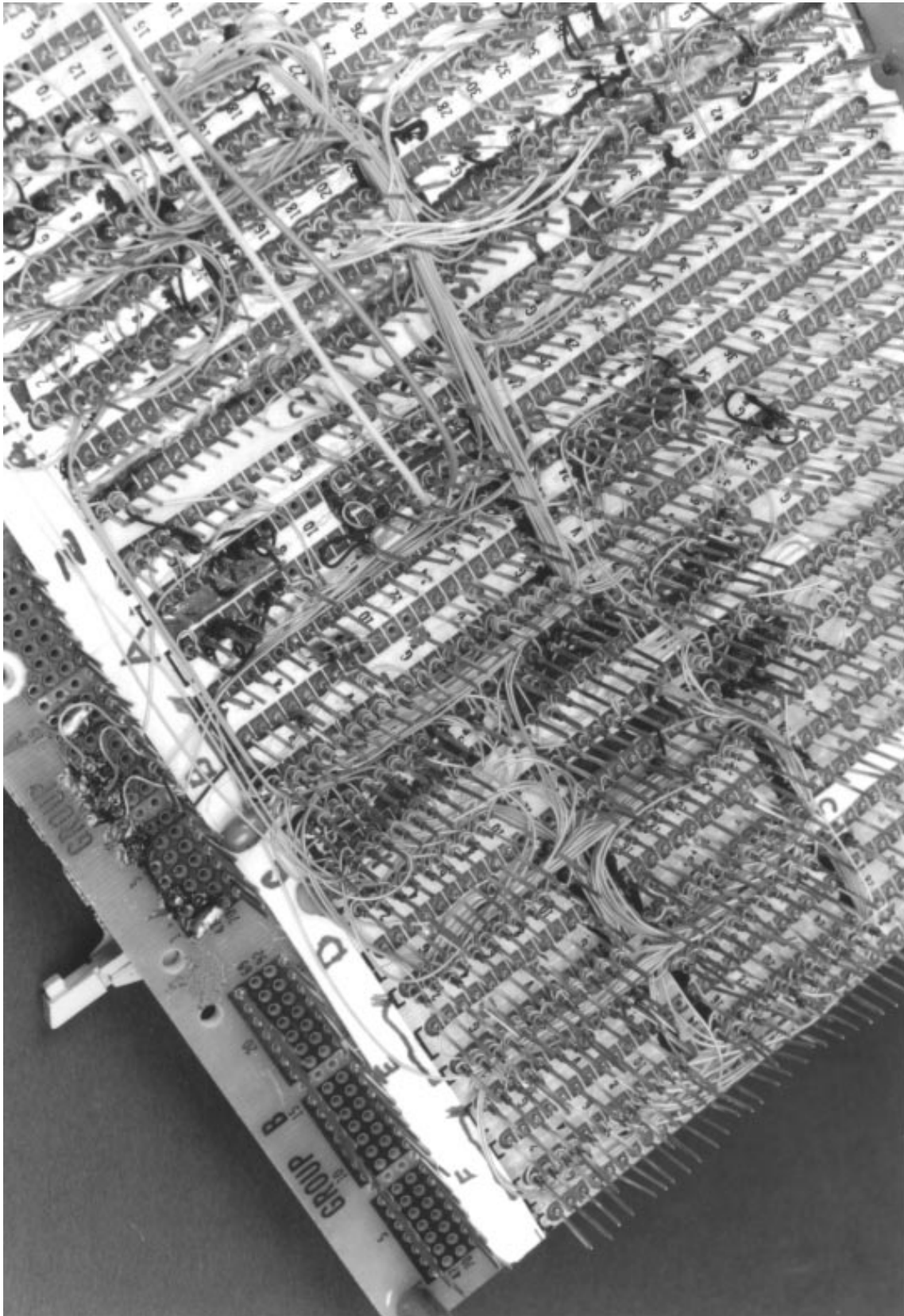
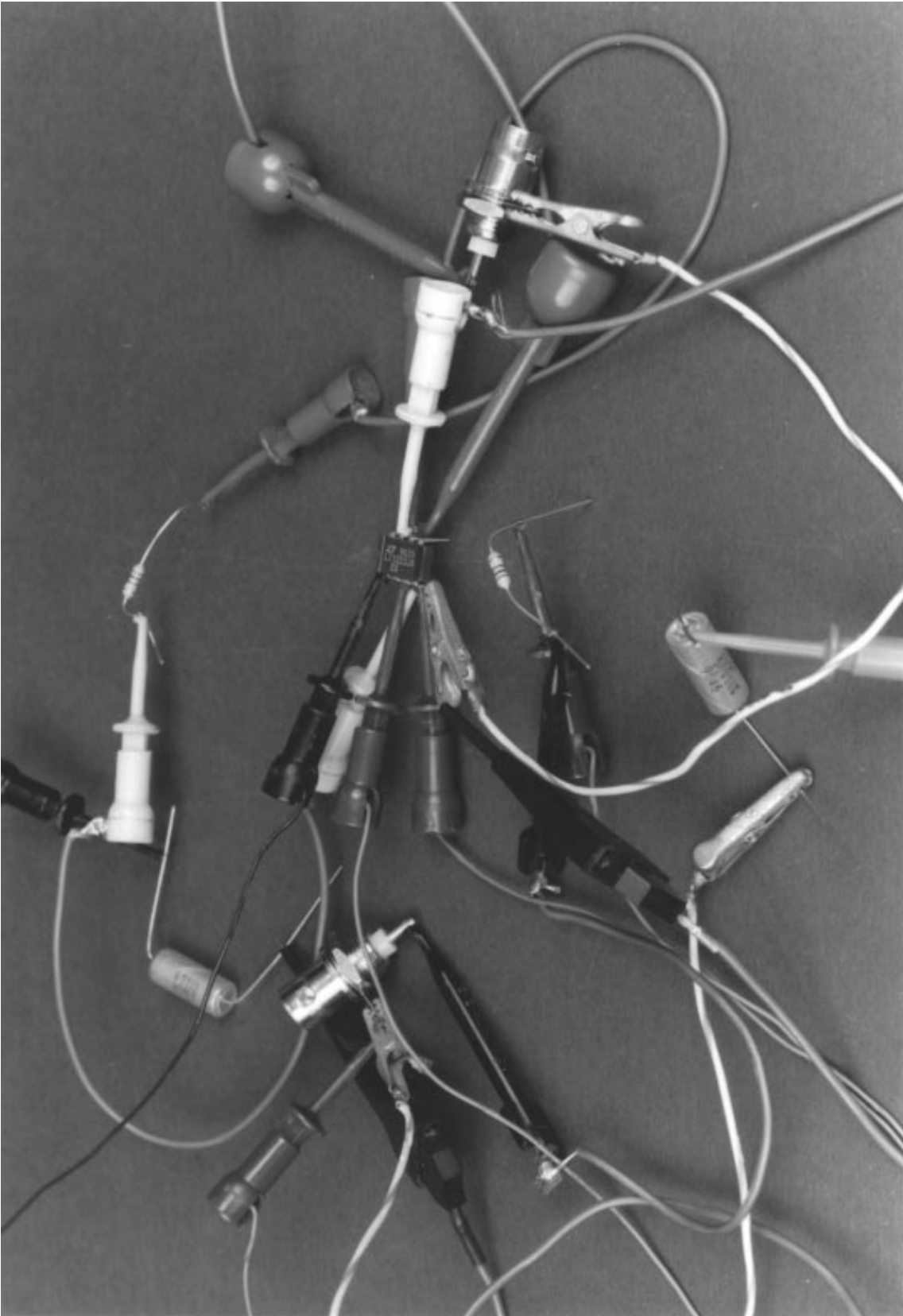


Figure F1. No



LTAN17 • TAF2

Figure F2. No



LTAN47-TAF3

Figure F3. No

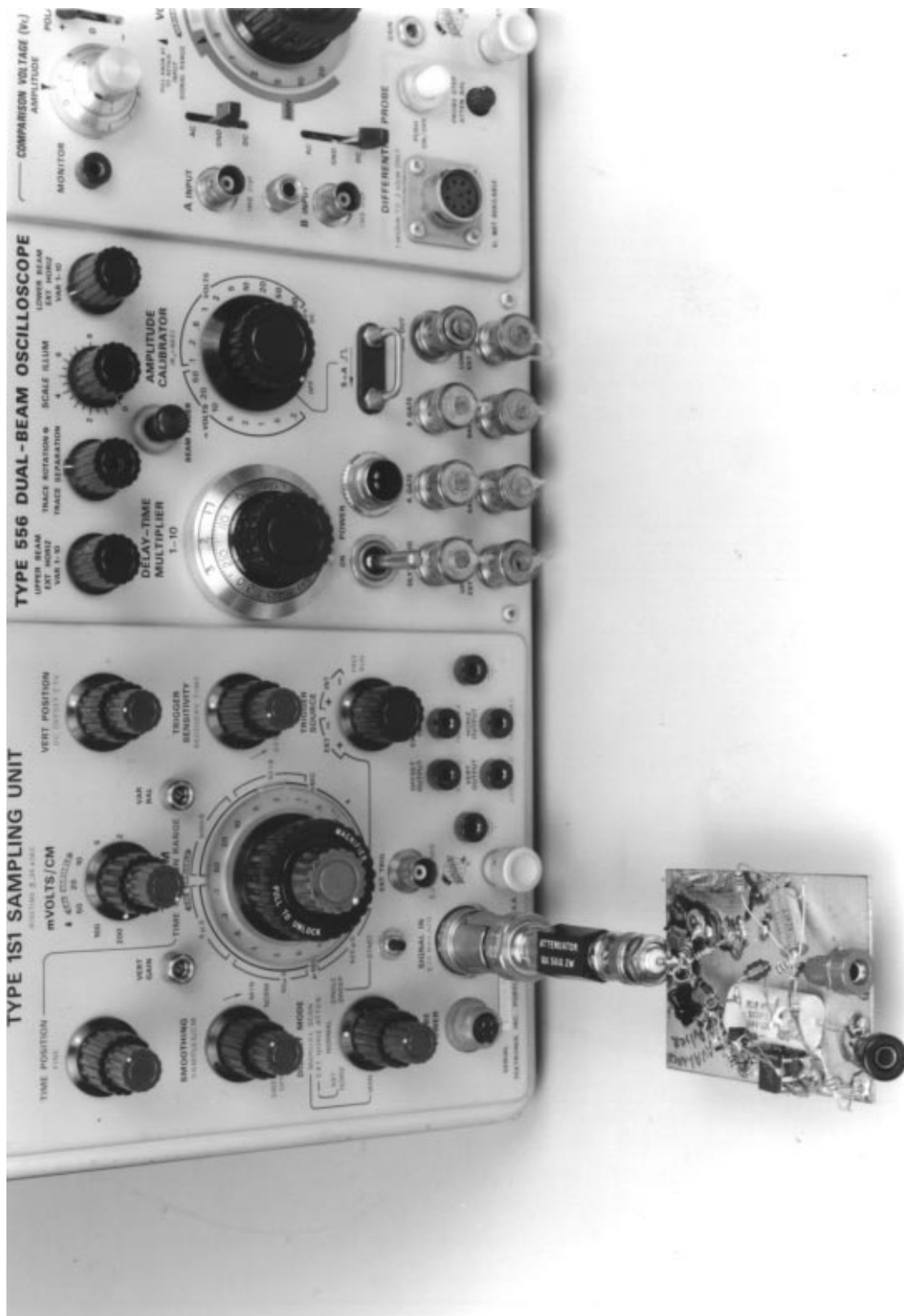
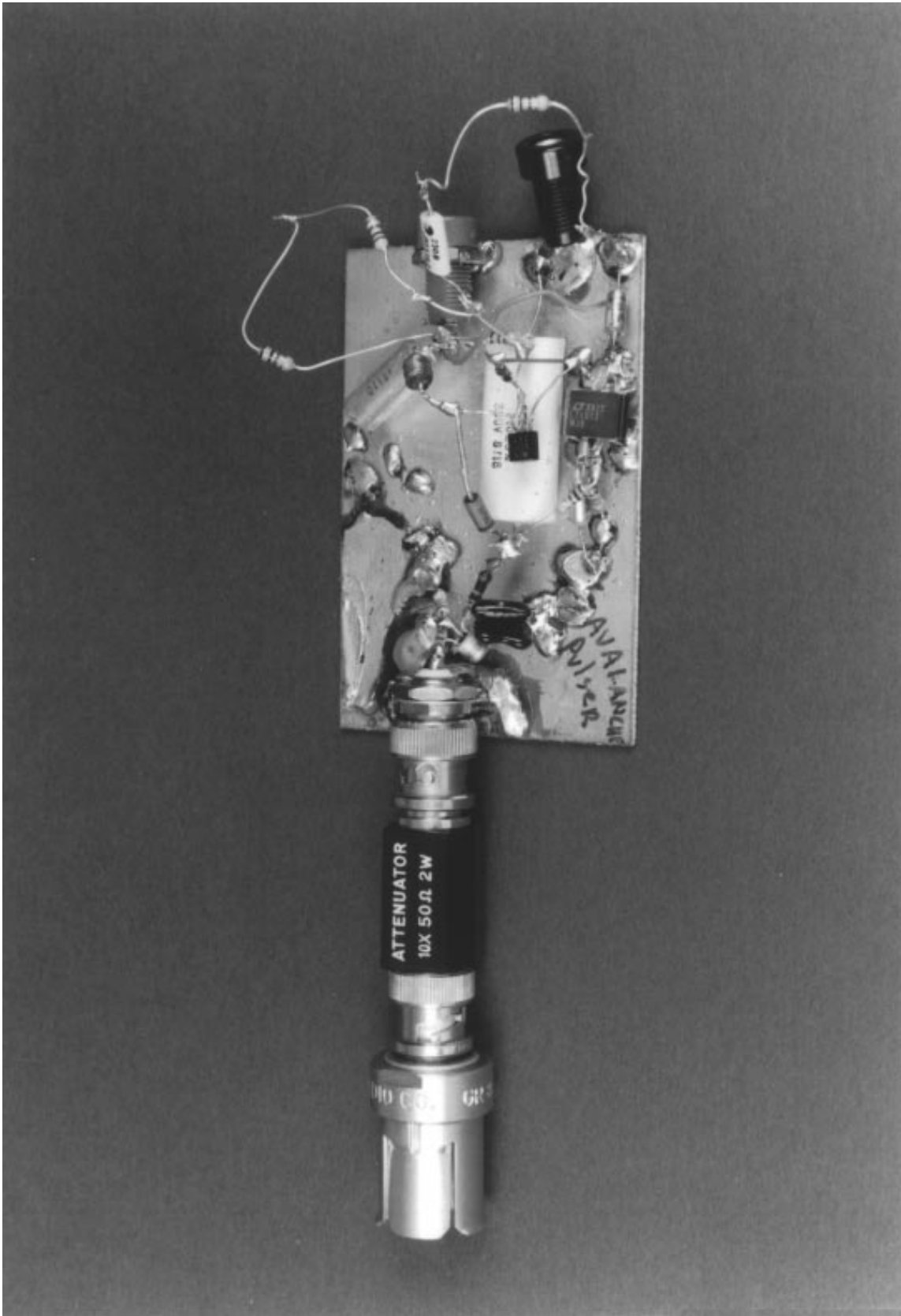
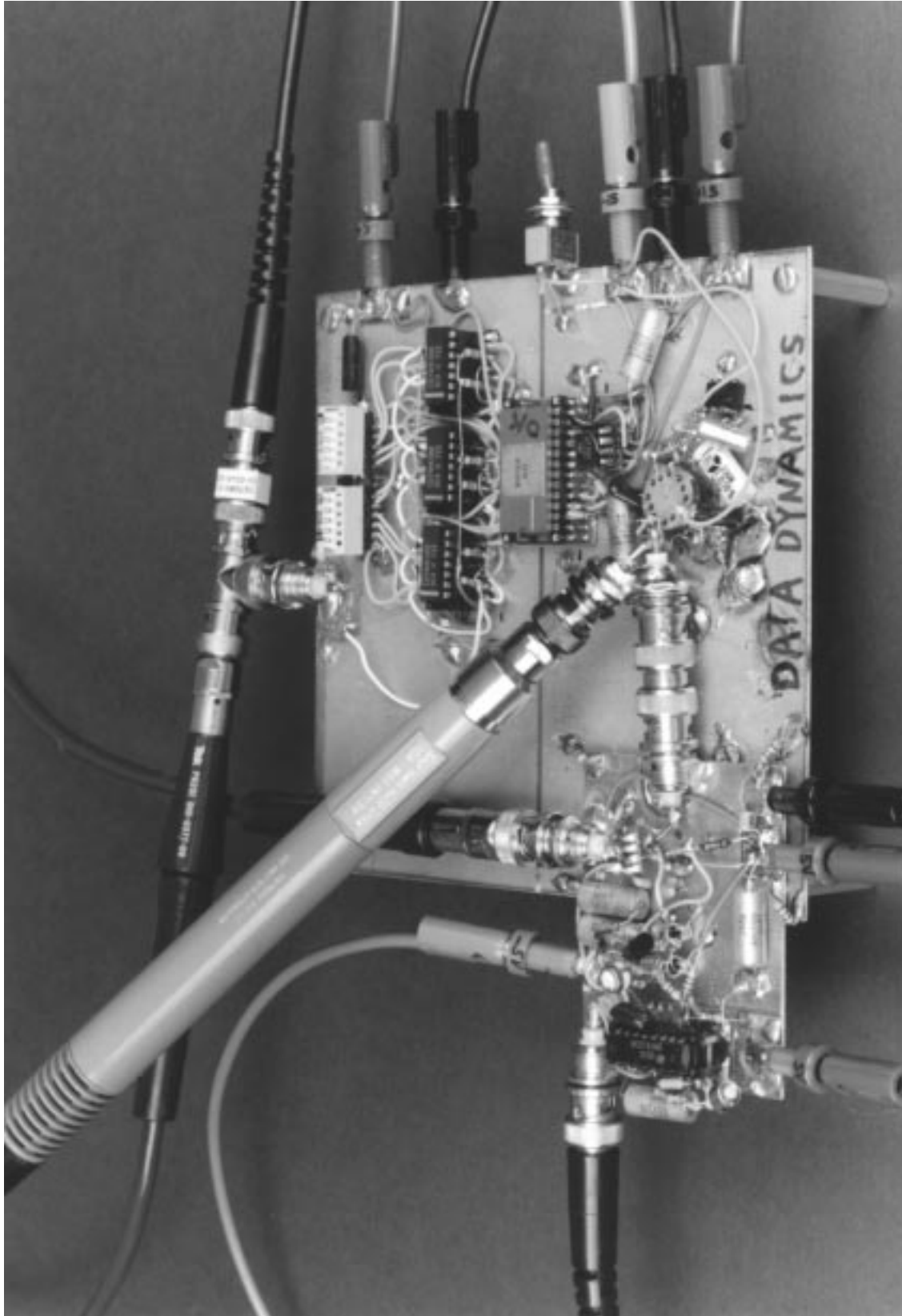


Figure F4. Prototype Avalanche Pulser Under Test. Direct Connection to Oscilloscope Eliminates Cable or Probe Effects



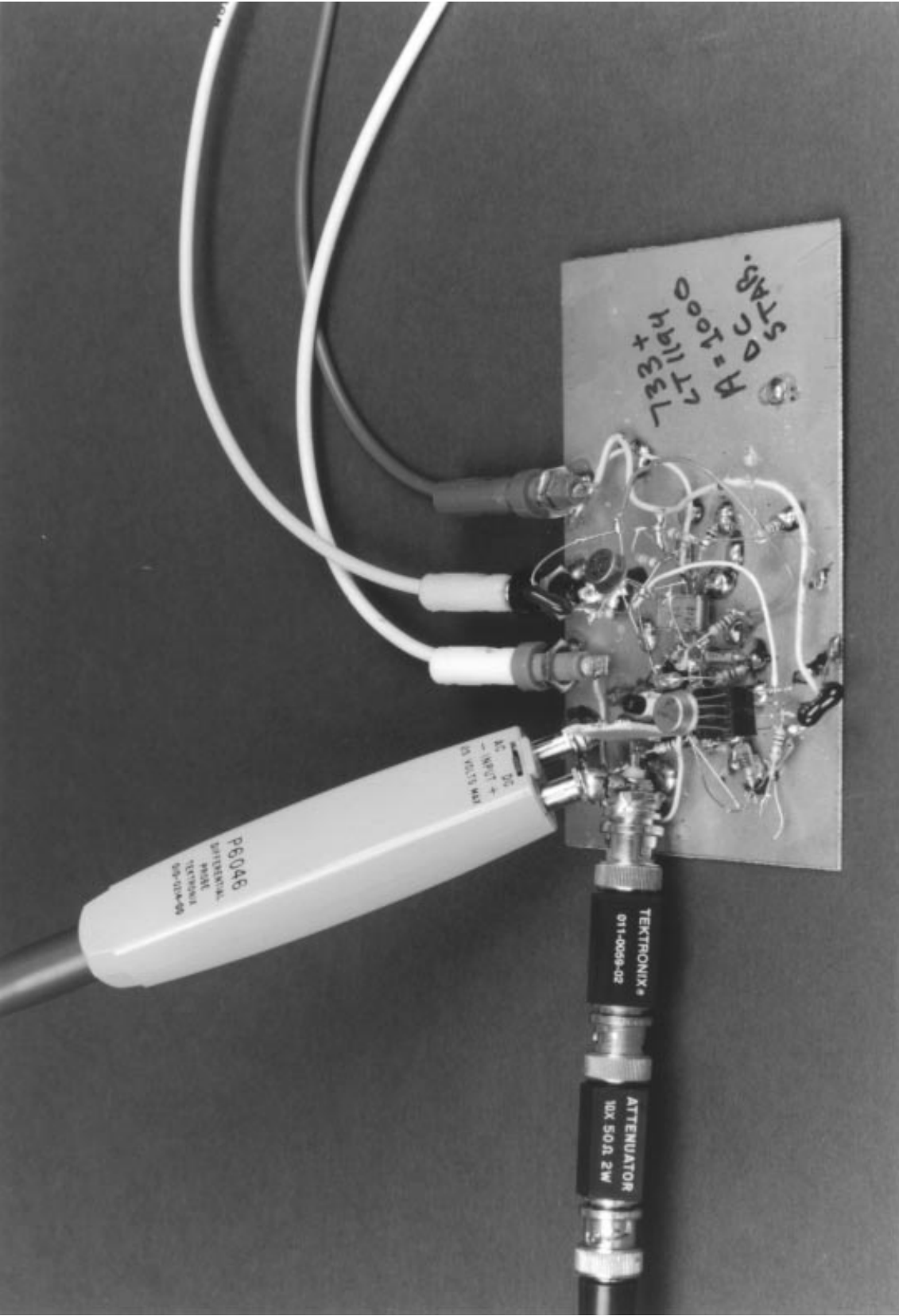
LTAN47-TAF5

Figure F5. Close-Up of Prototype Avalanche Pulse Generator. DC Bias Generator (Right Side of Board) is Carelessly Wired, but Pulse Forming Circuitry (Left Side of Board, by BNC Connector) is Carefully and Tightly Wired



LTAN17-TAF6

Figure F6. The Settling Time Test Fixture Described in Appendix B. DAC and Amplifier are in Center Right of Photo. Note Break in Clad Separating Analog and Digital Grounds and Attention to Layout in Switching Bridge (Lower Left). Switching Bridge is Returned Separately to Ground — Its Board is Mechanically Stood-Off From Main Board by 10M Ω Resistors. Output Section, Driving the Large P6032 Follower Probe, is at Lower Right



LTANF7 • TAF7

Figure F7. The X1000 38MHz Differential Amplifier. DC and Low Frequency Electronics use Sockets (Foreground) and Air Wire Techniques (Center Right) for Easy and Fast Breadboarding. Wideband Circuitry Hugs the Ground Plane, and is Clustered Near the Input BNC

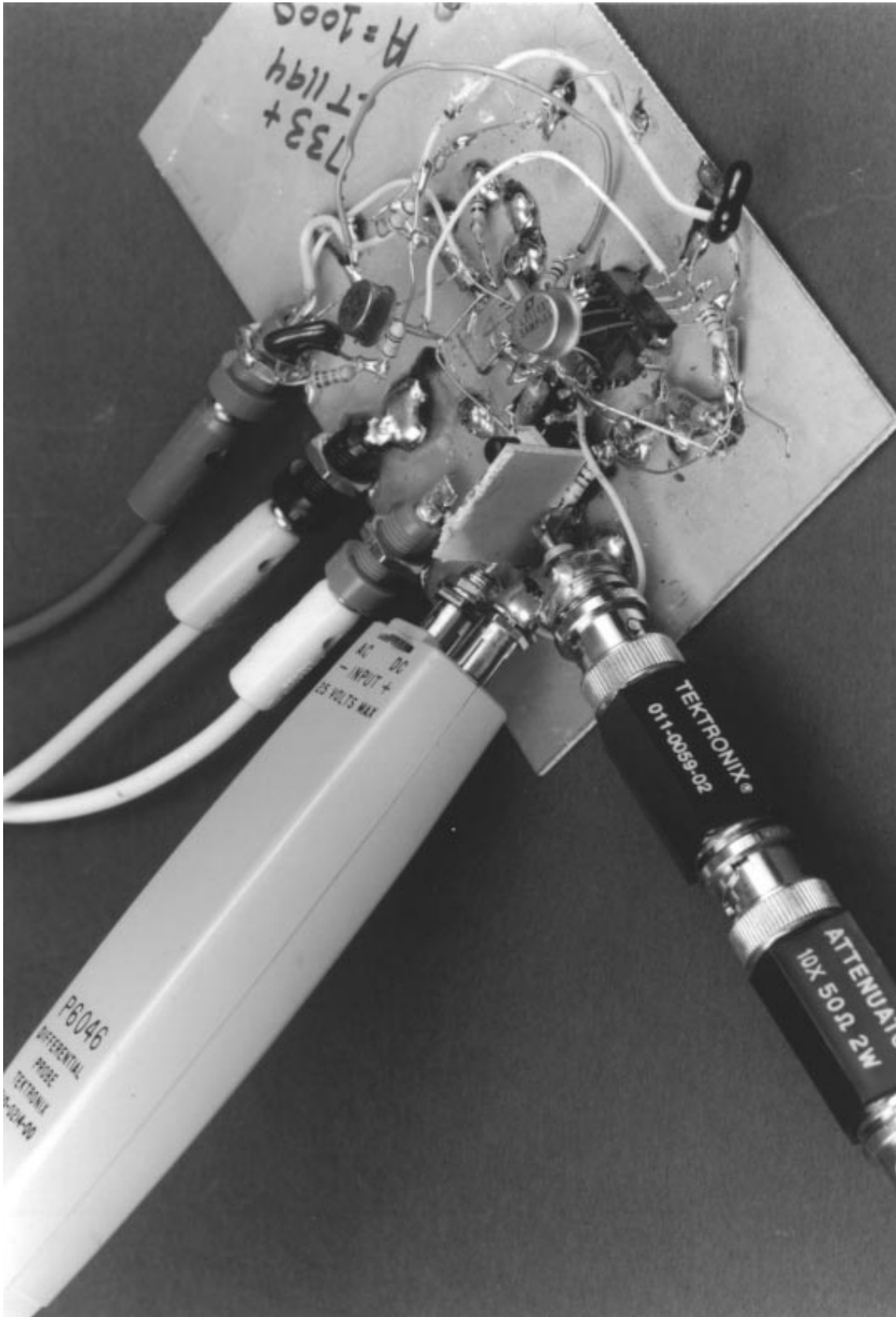
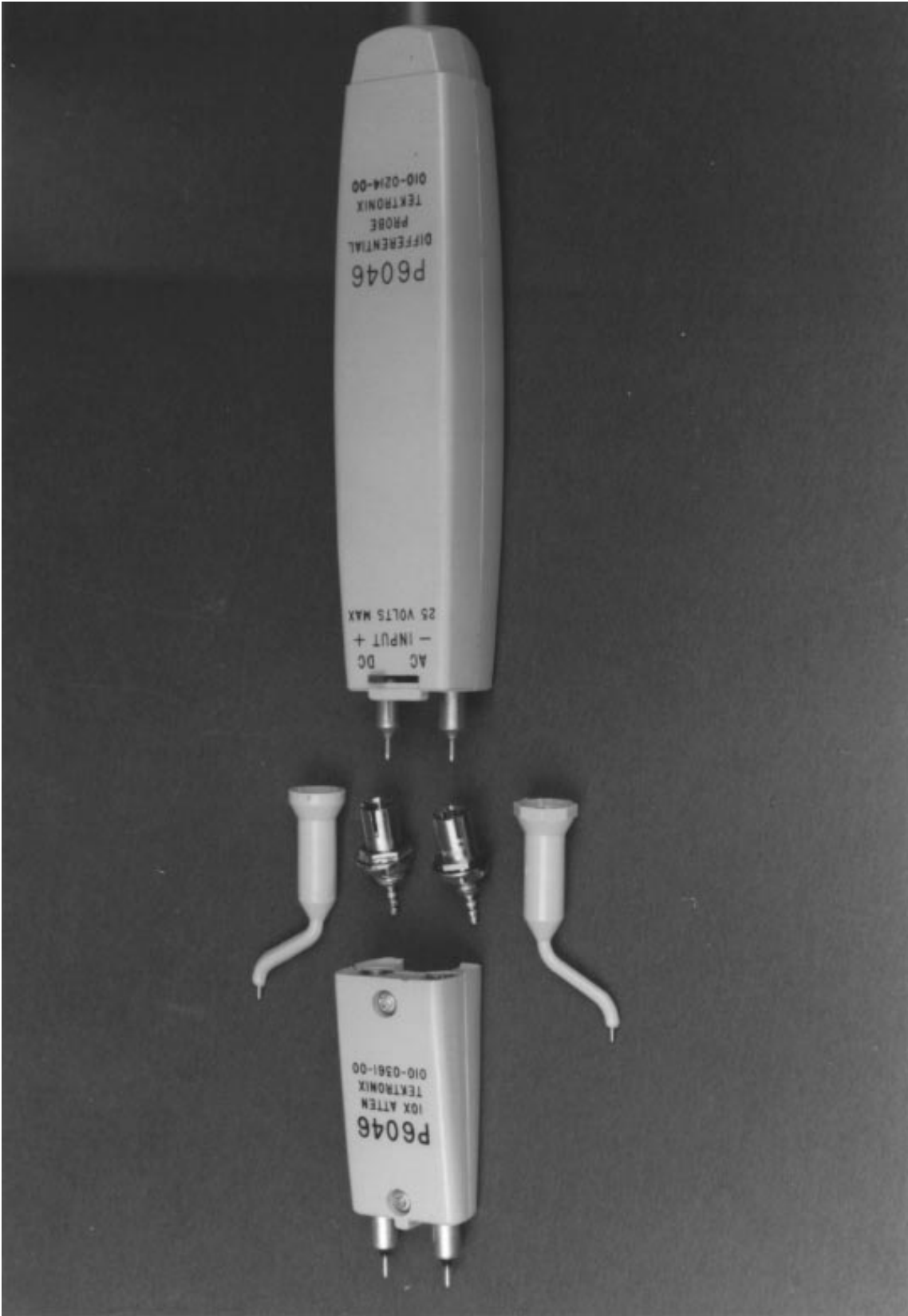


Figure F8. Input Detail of X1000 Differential Amplifier. Clad Shield (Center Right) Prevents BNC Radiation from Corrupting Low Level Circuitry. Differential Probe Verifies Fidelity of 2.5mV Pulse Out of the X100 Attenuator Stacked Sections. Note DIP Packages Hugging Ground Plane, While Cans Operating at Low Frequency are Carelessly Wired



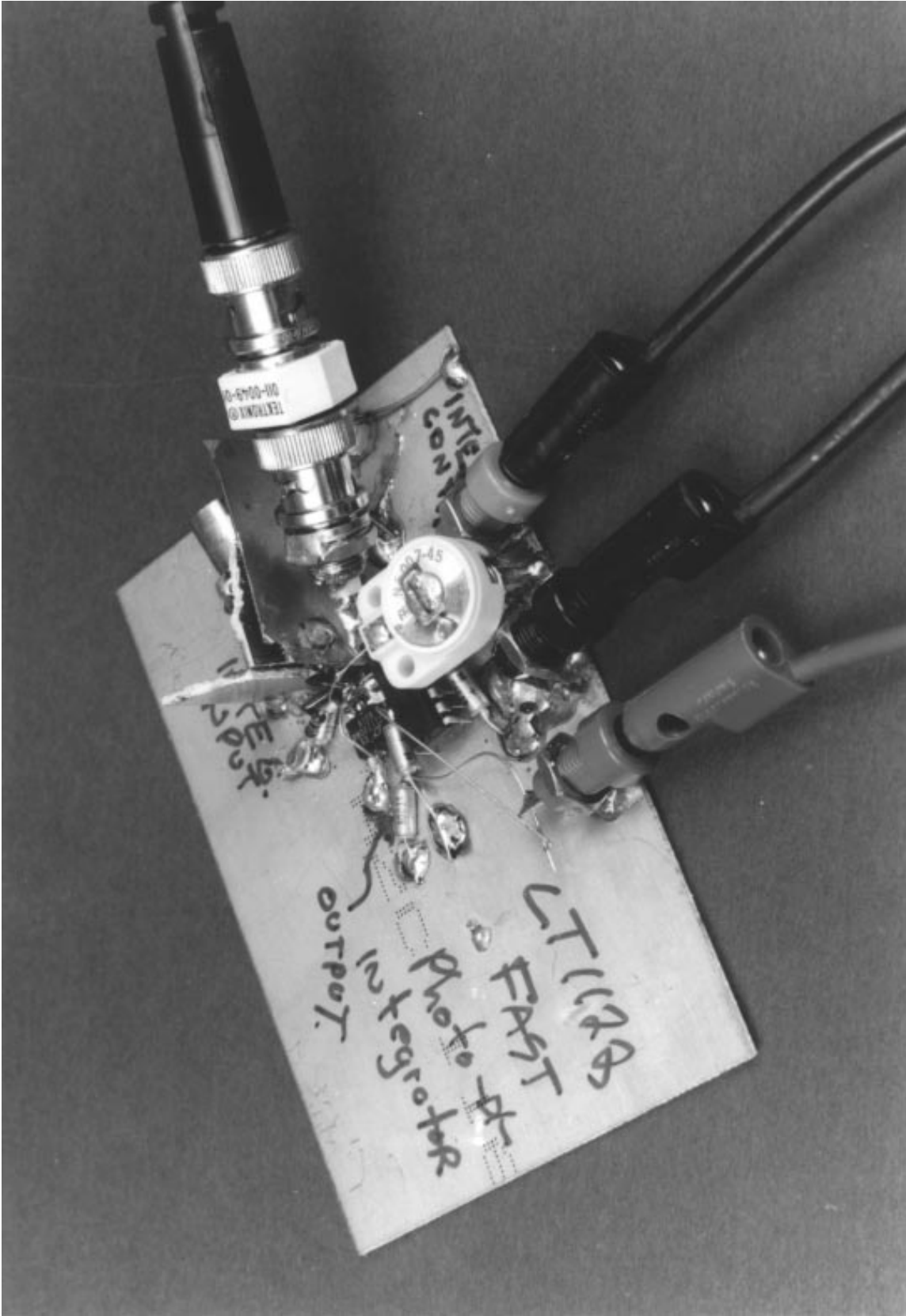
LTAN17 • TAF9

Figure F9. The Differential Probe and Its 10X Attenuator. Offset Probe Tips are Convenient for Making Differential Connections, but Sockets Maintain a True Coaxial Environment and are Preferred



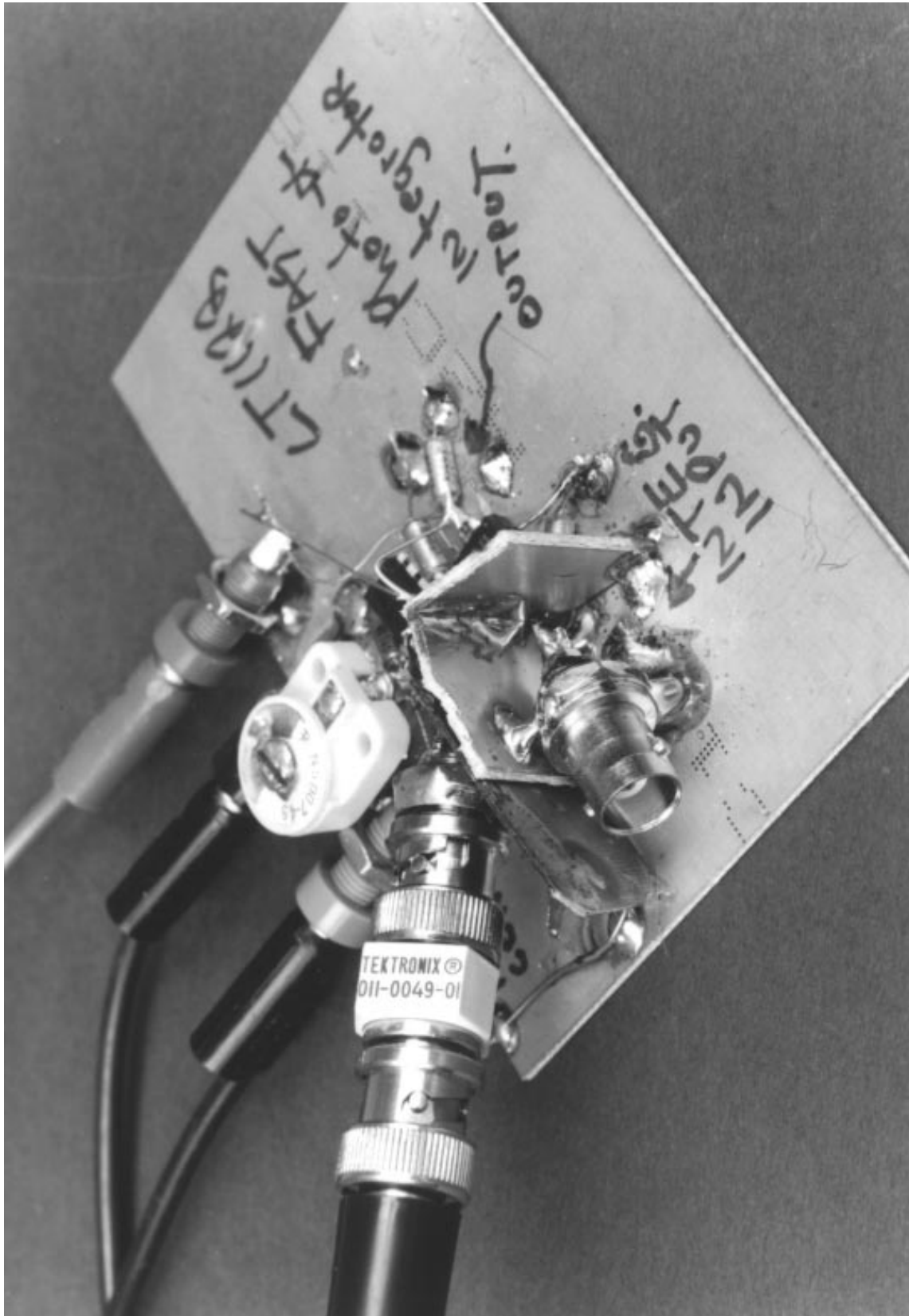
LTAN47-TAF10

Figure F10. The Photodiode Amplifier Layout Emphasizes Low Capacitance at Amplifier (Located Below Trimmer Capacitor, Photo Center Upper Left). Vertical Guard Shield Breaks Up BNC Radiation; was Used When Photo Input was Simulated with a Pulse Generator



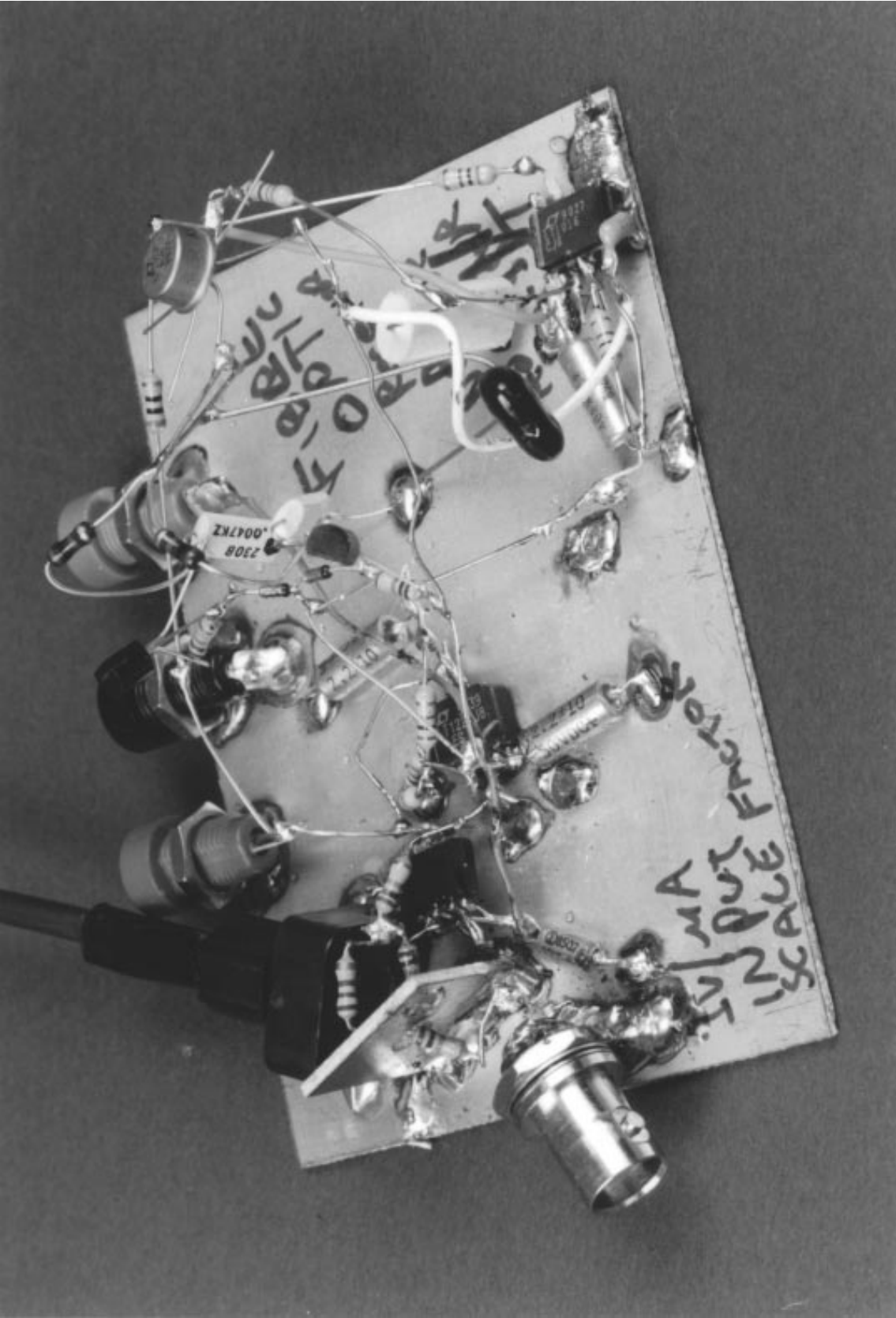
LTAN47-TAF11

Figure F11. Fast Photo Integrator Under Test with Pulse Generator Simulating a Photo Input. BNC Radiation is Controlled with Extensive Shielding at Integrator Input (Just Visible Upper Center). Control Input (Cable Connected BNC) is Less Critical; Does Not Require Shielding



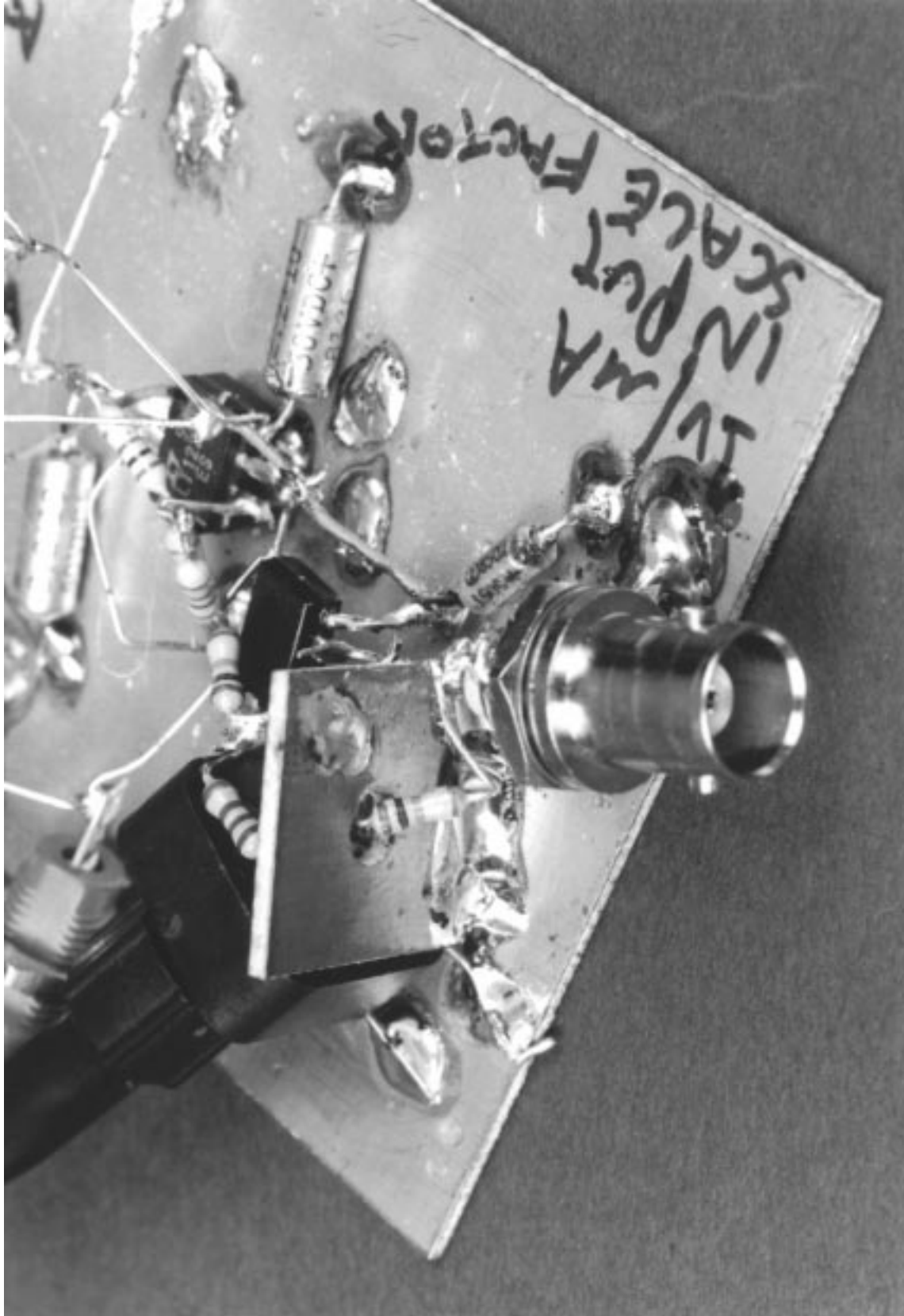
LTAN47-TAF12

Figure F12. Photo Integrator Details. Integrator Input BNC is Fully Shielded From Integrator Amp — 1pF Coupling From BNC Output to Summing Point will Cause Excessive Peaking. Amplifier and Switch ICs are Just Visible



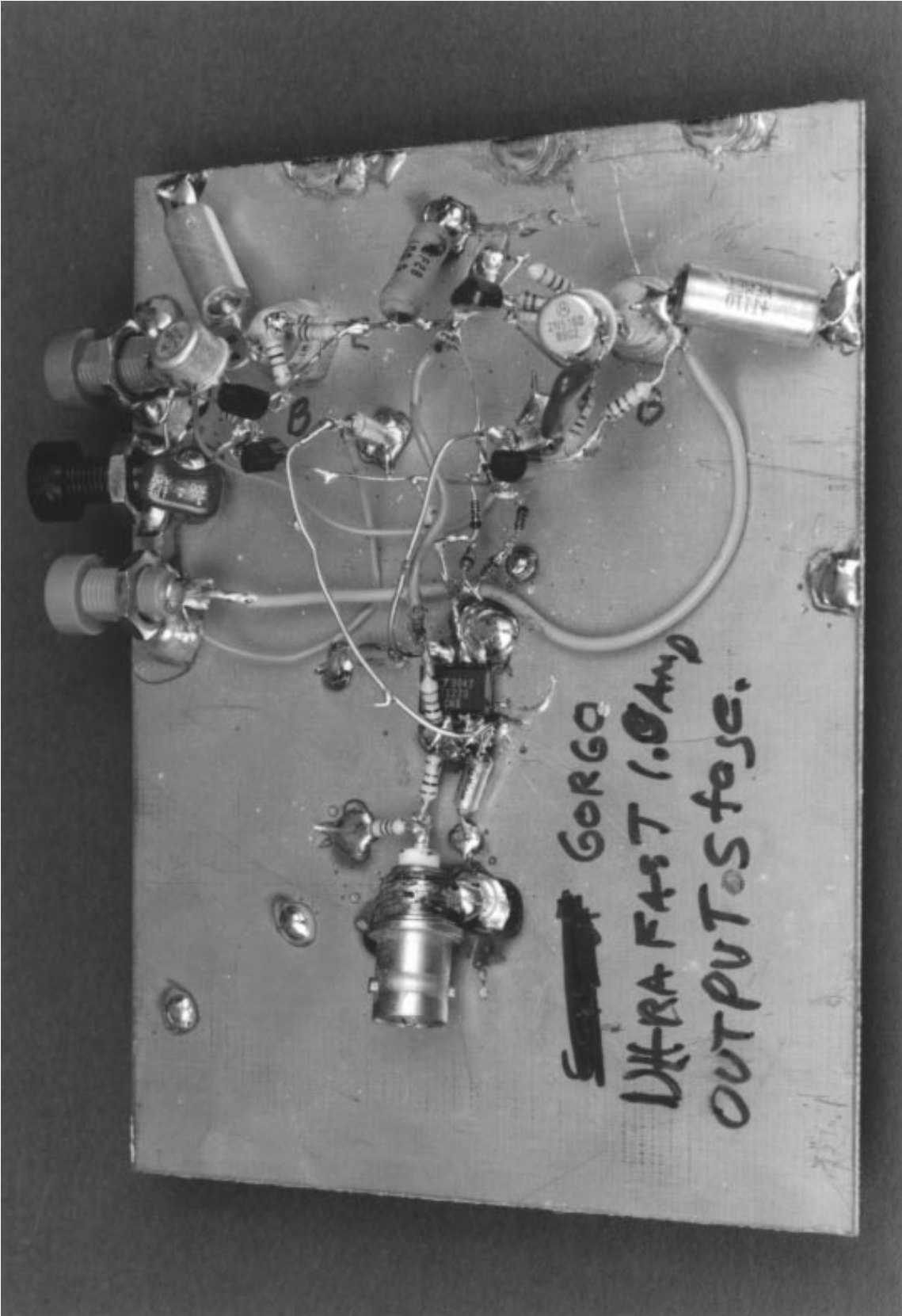
LTAN47-TAF13

Figure F13. The Adaptive Trigger Fiber Optic Receiver. BNC Photo-Simulation Input and Fiber Optic Line Both Connected. Low Frequency Wiring is Haphazardly Constructed While High Frequency Sections are Tight and Hug the Ground Plane. Note Vertical Shield at Photo-Simulation Input BNC



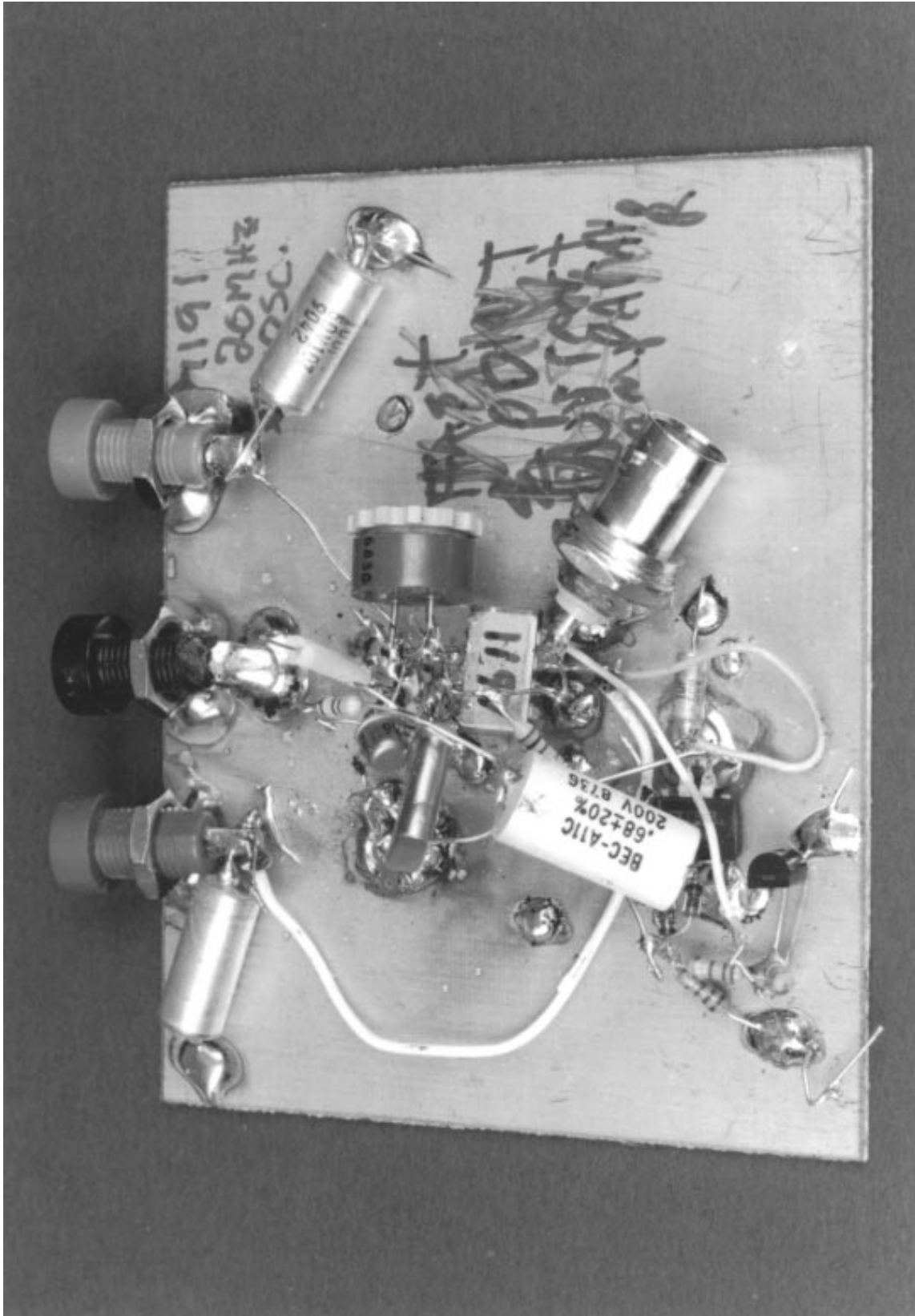
LTAN47-TAF14

Figure F14. Detail of the Fiber Optic Receiver's Photo-Simulation BNC Input. Resistor From BNC is Routed Through a Small Hole in Vertical Shield, Minimizing Capacitance. Another Resistor on the Shield's Other Side Divides Effects of Residual Capacitance to Keep Summing Point Clean



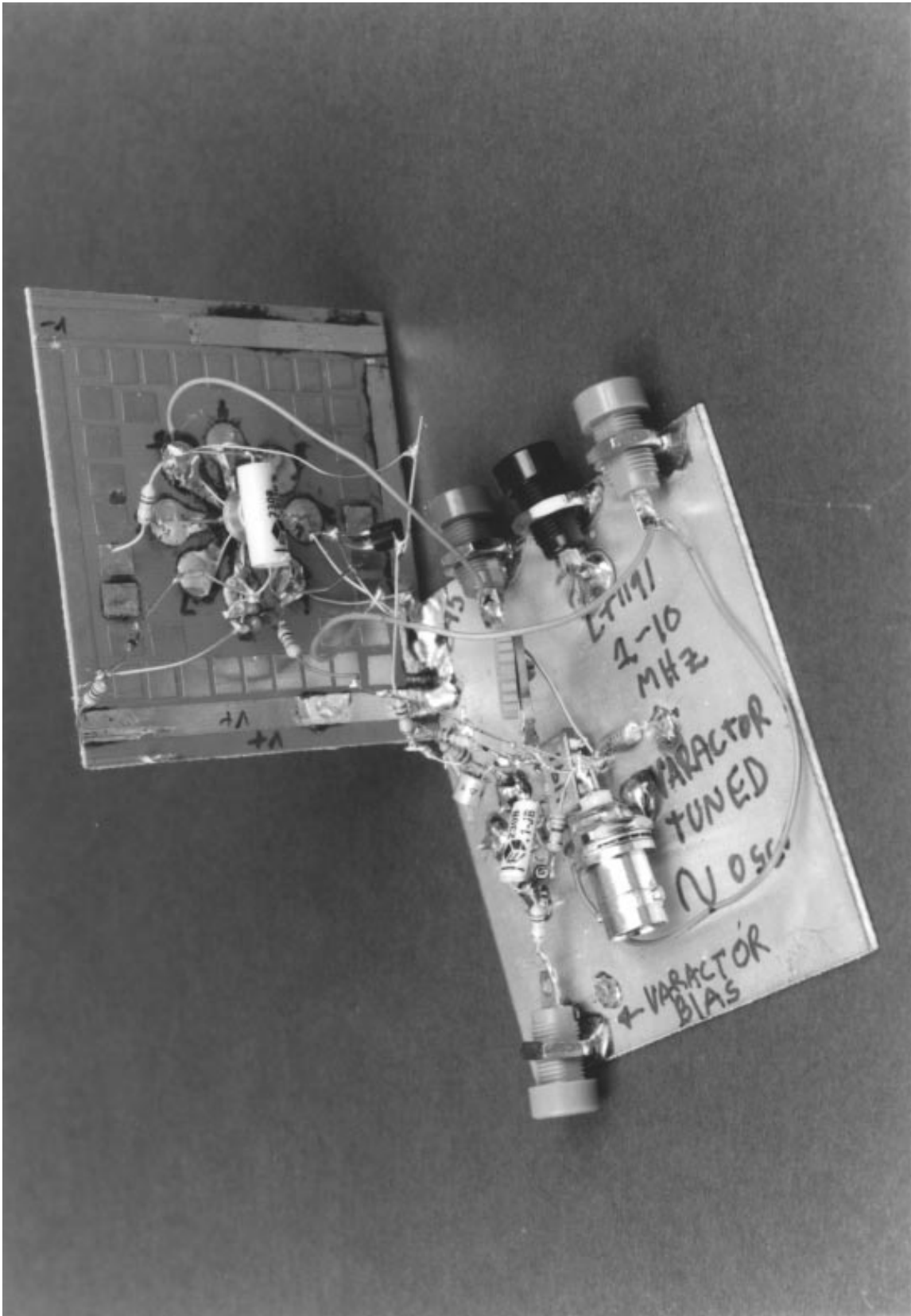
LTAN47-1A15

Figure F15. The 1A Booster. Note Heavy Bypassing Right at the Output Power Transistors (Both Stud-Mounted to Clad). Local Compensation Capacitors (Right Side Upper and Lower) Have Short Leads



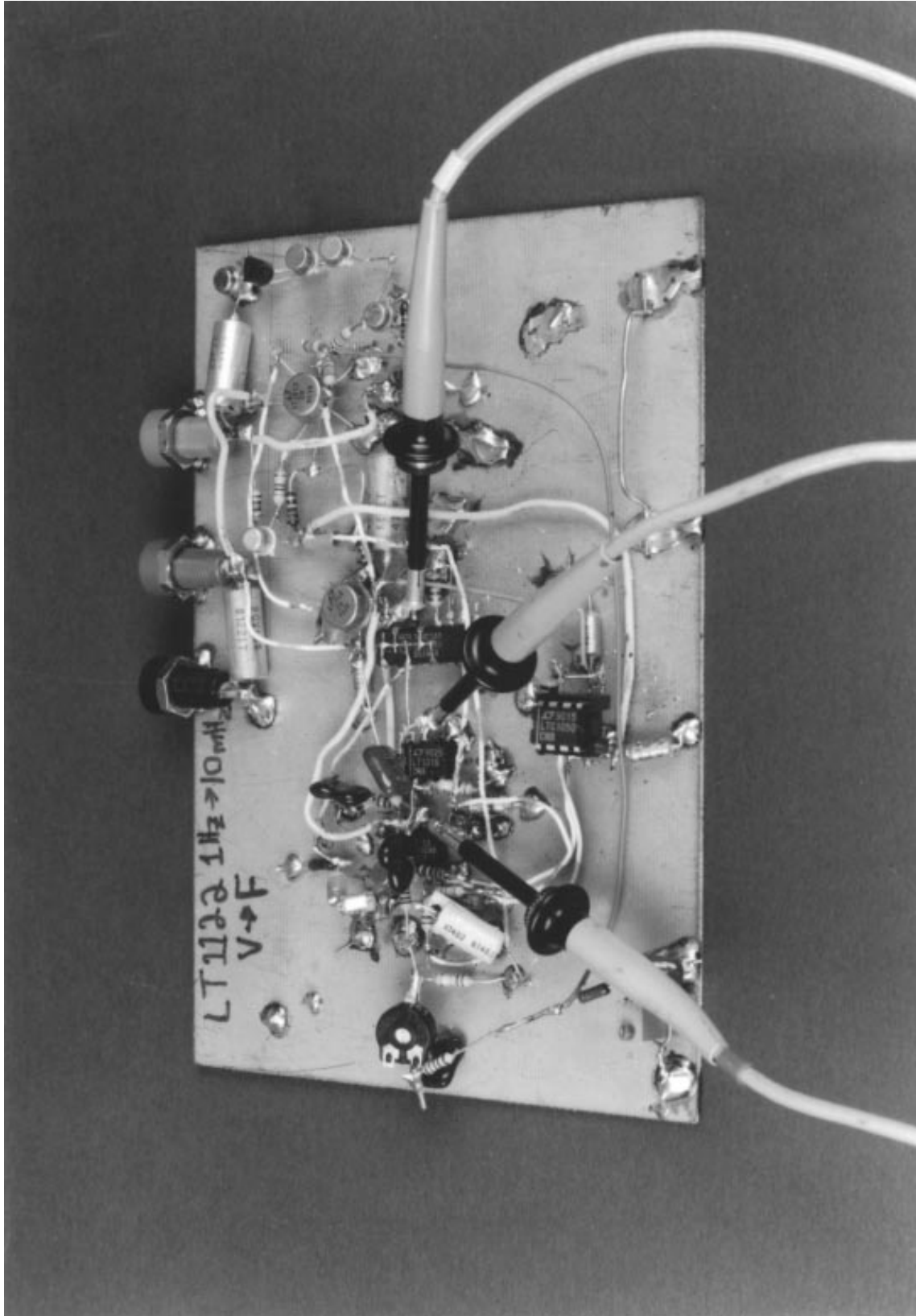
LTAN47-TAF16

Figure F16. 20MHz Sine Wave Crystal Oscillator. DC-AGC Section is at Lower Left, Oscillator is in Center. Control FET is Located at Oscillator Amplifier. Slow Gate Control Signal Arrives via Long-Leaded Resistor, (Photo Center Upper Left)



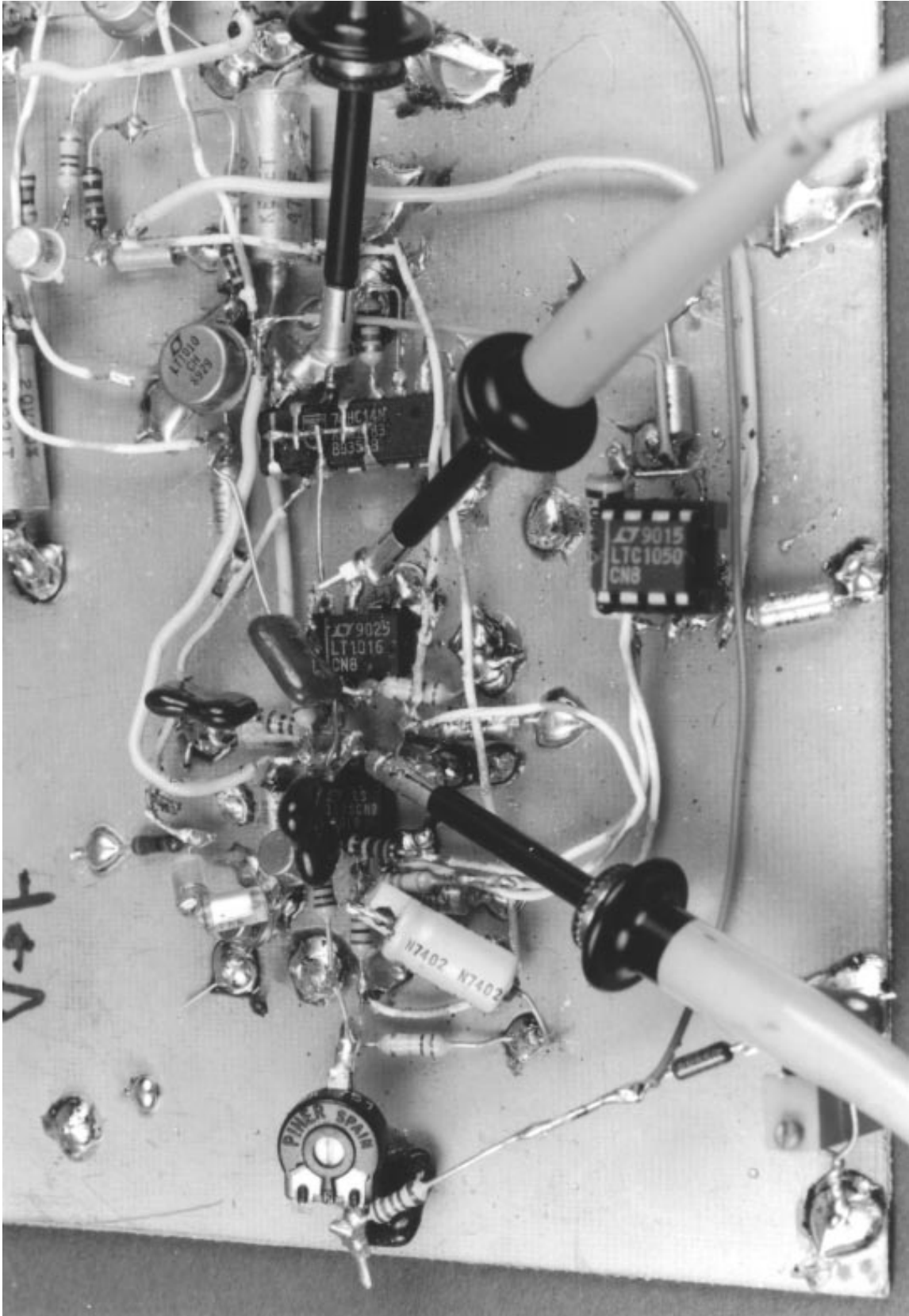
LTAN47-TAF17

Figure F17. The Varactor Tuned Wien Bridge, DC-AGC Section is on Vertical Board — High Frequency Section Hugs the Ground Plane. Control FET (Center Left), Located at Oscillator, is Biased From a Long Line Originating on AGC Board. Note FET Gate Resistor is Located at FET, Not DC Board. Oscillator Output Receives Reverse Treatment



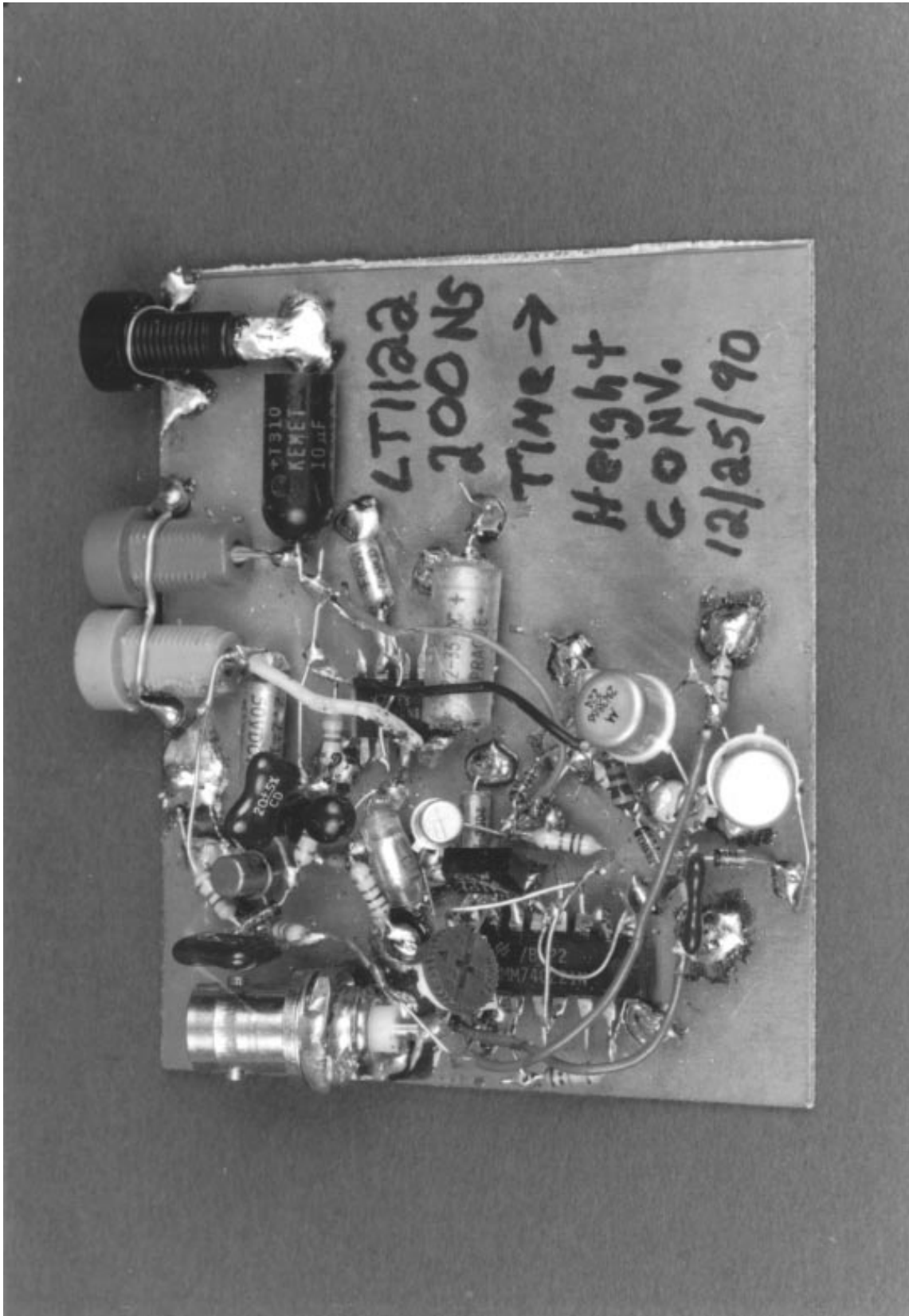
LTAN47-TAF18

Figure F18. The 1Hz-10MHz V to F Breadboard with Probes Attached. DC Servo Amplifier is Socketed, with Long Leads. Reference Section, Starting at Breadboard (Upper Right), Works Toward Reference Switch (Large DIP at Board Center). Note Very Tight Layout in Amplifier-Comparator Region (Board Left Center)



LTAN47-TAF19

Figure F19. Details of 1Hz-10MHz V to F High Speed Section. LT1122 Integrator is Just Visible Under its Associated Discrete Components. Summing Point (Left Side of Amplifier) is Layout's Electrical Center. LT1016 Wiring is Also Very Tight Except for its Output Which Goes to Reference Switch. DC Servo Amplifier Sleeps in its Socket. Note Probe Tip Connectors



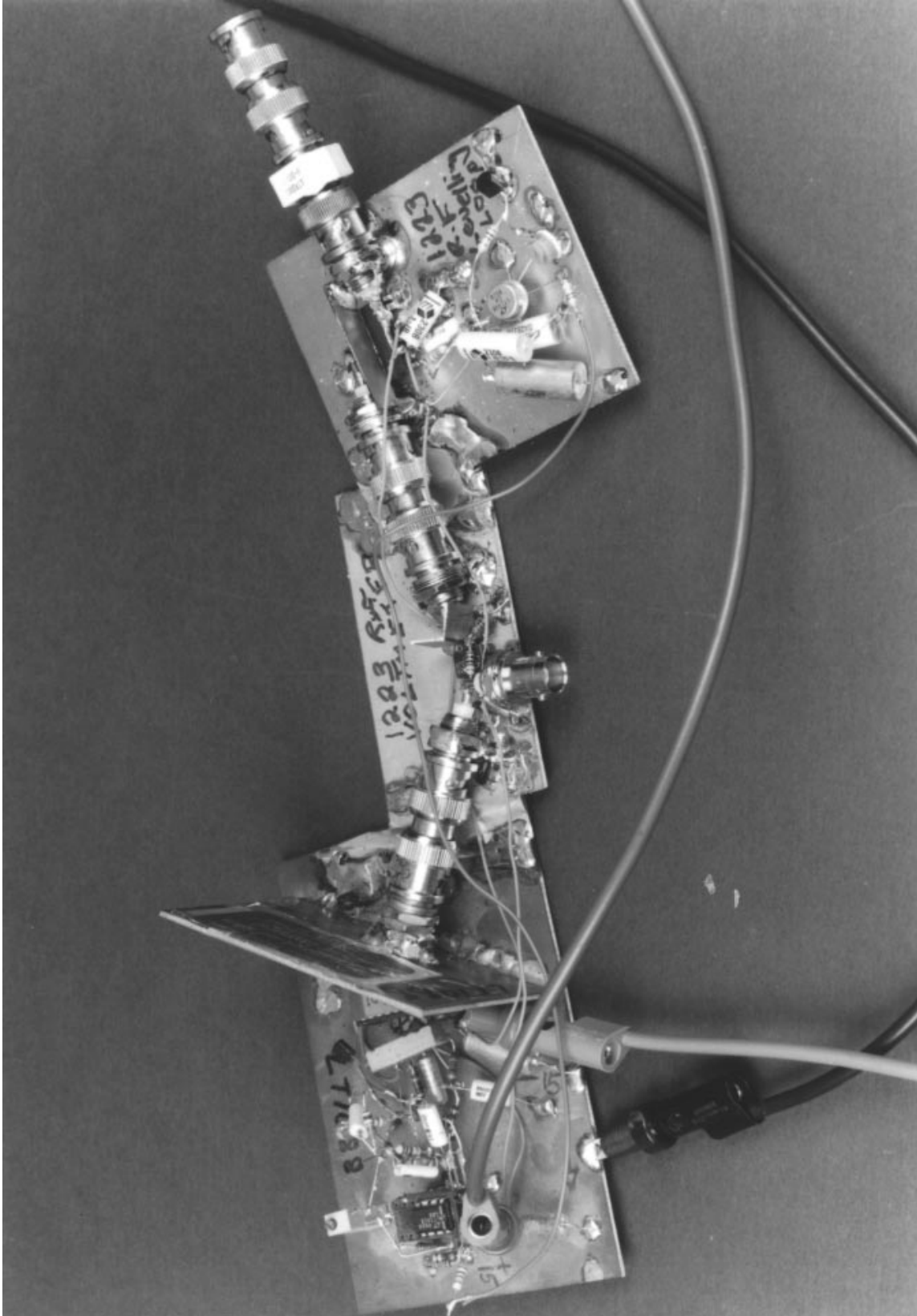
LT1AN47-TAF20

Figure F20. The Time-to-Height Converter. Switched Current Source, (Board Center Left), has Very Tight Layout. Follower Amplifier is at Board Upper Center. Major Components (in Order from Top to Bottom), Include Current Source Switch Transistor, Current Source Transistor (Black Case), Integrator Capacitor (Silver) and Reset Transistor. Note Short Connection to Amplifier Input Pin



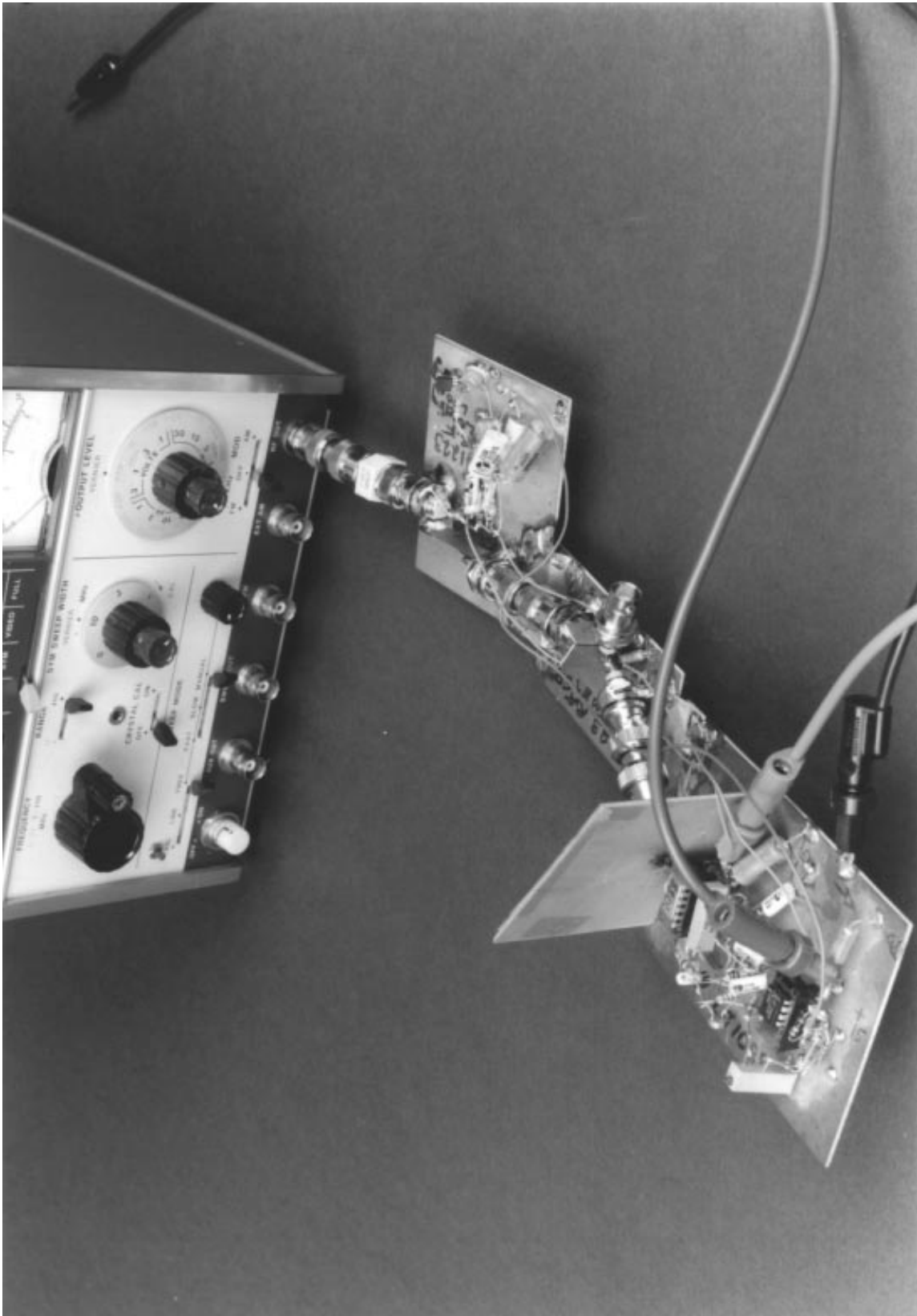
LTAN47-TAF21

Figure F21. The Automatic Trigger. Low Frequency Automatic Level Section is Spread Out, (Right Side of Board). Wideband Circuitry Hugs Ground Plane and is Located Near Input BNC. Amplifier's Low Impedance, Fast Output Feeds LT1016 Output Comparator Over a Relatively Long Wire Run, Routed Through Insensitive Section of DC Circuitry



LTAN47-TAF22

Figure F22. The RF Leveling Loop. The RMS to DC Converter (Left Board) was Built First, Then the RF Pre-Amp (Center Board) and Finally the Multiplier-Servo Board. Each Board's Performance was Verified Before Joining Them. Note Copper Tape Maintaining Ground Plane Integrity Between Boards



LTAN47-TAF23

Figure F23. RF Leveling Loop Attached Directly to the Test Generator. Cable Uncertainties are Eliminated Because There is No Cable



LTAN47-TAF24

Figure F24. The Voltage Controlled Current Source. Vertical Shield (Upper Left) Absorbs Input BNC Radiation. Amplifier-Loop Compensation Components are Located Directly at Amplifier (Behind Shield)

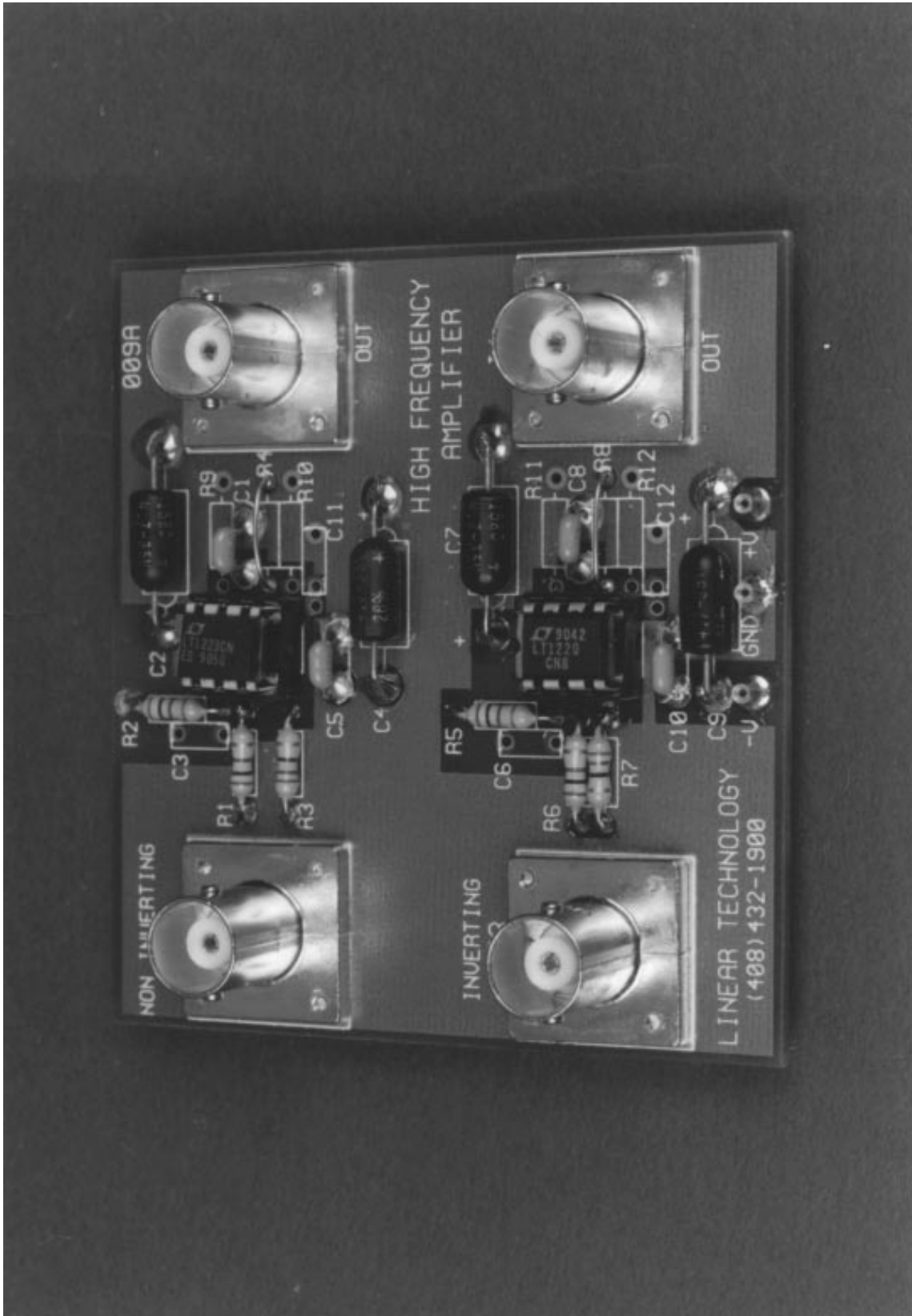


Figure F25. The Good Life. The High Frequency Amplifier Demonstration Board Discussed in Appendix I. Sockets are a Compromise Between Best Performance and Flexibility

APPENDIX G

FCC Licensing and Construction Permit Applications for Commercial AM Broadcasting Stations

In accordance with the application for Figure 116's circuit, and our law-abiding nature, find facsimiles of the appropriate FCC applications below. The complete forms are available by writing to:

Federal Communications Commission
Washington, D.C. 20554

Approved by OMB
3090-0027
Expires 2/29/92
See Page 25 for information
regarding public burden estimate

FCC 301

APPLICATION FOR CONSTRUCTION PERMIT FOR COMMERCIAL BROADCAST STATION

For COMMISSION Fee Use Only FEE NO: FEE TYPE: FEE AMT: ID SEQ:	For APPLICANT Fee Use Only Is a fee submitted with this application? <input type="checkbox"/> Yes <input type="checkbox"/> No If fee exempt (see 47 C.F.R. Section 1.1112), indicate reason therefor (check one box): <input type="checkbox"/> Noncommercial educational licensee <input type="checkbox"/> Governmental entity FOR COMMISSION USE ONLY FILE NO.
--	---

Section I - GENERAL INFORMATION

1. Name of Applicant Street Address or P.O. Box City State ZIP Code Telephone No. (include Area Code)	Send notices and communications to the following person at the address below: Name Street Address or P.O. Box City State ZIP Code Telephone No. (include Area Code)
--	---

2. This application is for: AM FM TV

(a) Channel No. or Frequency	(b) Principal Community
	City State

(c) Check one of the following boxes:

Application for NEW station

MAJOR change in licensed facilities; call sign: _____

MINOR change in licensed facilities; call sign: _____

MAJOR modification of construction permit; call sign: _____
File No. of construction permit: _____

MINOR modification of construction permit; call sign: _____
File No. of construction permit: _____

AMENDMENT to pending application; Application file number: _____

NOTE: It is not necessary to use this form to amend a previously filed application. Should you do so, however, please submit only Section I and those other portions of the form that contain the amended information.

3. Is this application mutually exclusive with a renewal application? Yes No

If Yes, state:

Call letters	Community of License
	City State

Figure G1

Approved by OMB
3090-0028
Expires 9/30/90

APPLICATION FOR NEW BROADCAST STATION LICENSE
(Carefully read instructions before filling out Form)
RETURN ONLY FORM TO FCC

For Commission Fee Use Only FEE NO: FEE TYPE: FEE AMT: ID SEQ:	For Applicant Fee Use Only Is a fee submitted with this application? <input type="checkbox"/> Yes <input type="checkbox"/> No If No, indicate reason therefor (check one box): <input type="checkbox"/> Nonfeeable application Fee Exempt (See 47 C.F.R. Section 1.1112) <input type="checkbox"/> Noncommercial educational licensee <input type="checkbox"/> Governmental entity
--	---

SECTION I - GENERAL DATA

Legal Name of Applicant City State Zip Code Telephone No. (include area code)	For Commission Use Only File No.
---	-------------------------------------

1. Facilities authorized by construction permit

This application is for: Commercial Noncommercial

AM Directional AM Non-Directional FM Directional FM Non-Directional TV

Call Letters	Community of License	Construction Permit File No.	Modification of Construction Permit File No(s).	Expiration Date of Last Construction Permit
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2. Is the station now operating pursuant to automatic program test authority in accordance with 47 C.F.R. Section 73.1620? Yes No

If No, explain.

3. Have all the terms, conditions, and obligations set forth in the above described construction permit been fully met? Yes No

If No, state exceptions.

4. Apart from the changes already reported, has any cause or circumstance arisen since the grant of the underlying construction permit which would result in any statement or representation contained in the construction permit application to be now incorrect? Yes No

If Yes, explain.

5. Has the permittee filed its Ownership Report (FCC Form 323) or ownership certification in accordance with 47 C.F.R. Section 73.3015(b)? Yes No

If No, explain. Does not apply

Figure G2

Figure G1-G2. The FCC Forms Appropriate for Figure 116's Circuit

APPENDIX H

About Current Feedback

Contrary to some enthusiastic marketing claims, current feedback isn't new. In fact, it is much older than "normal" voltage feedback, which has been so popularized by op amps. The current feedback connection is *at least* 50 years old, and probably much older. William R. Hewlett used it in 1939 to construct his now famous sine wave oscillator.¹ "Cathode feedback" was widely applied in RF and wideband instrument design throughout the 30's, 40's and 50's. It was a favorite form of feedback, if for no other reason than there wasn't any place else left to feed back to!

In the early 1950's G.A. Philbrick Researches introduced the K2-W, the first commercially available packaged operational amplifier. This device, with its high impedance differential inputs, permitted the voltage type feedback so common today. Although low frequency instrumentation types were quick to utilize the increased utility afforded by high impedance feedback nodes, RF and wideband designers hardly noticed. They continued to use cathode feedback, called (what else?) emitter feedback in the new transistor form.

Numerous examples of the continued use of current feedback in RF and wideband instruments are found in designs dating from the 1950's to the present.² With ostensibly easier to use voltage type feedback a reality during this period, particularly as monolithic devices became cheaper, why did discrete current feedback continue to be used? The reason for the continued popularity of current techniques was (and is) bandwidth. Current feedback is simply much faster. Additionally, within limits, a current feedback based amplifier's bandwidth does not degrade as closed loop gain is increased. This is a significant advantage over voltage feedback amplifiers, where bandwidth falls as closed loop gain is increased.

Note 1: See Appendix C, "The Wien Bridge and Mr. Hewlett", in Reference 19. See also References 20 through 24 and 46.

Note 2: See the "General Electric Transistor Manual", published by G.E. in 1964. See also operating and service manuals for the Hewlett-Packard 3400A RMS Voltmeter, 1120A FET probe, and the Tektronix P6042 current probe.

Relatively recently, current based designs have become available as general purpose, easy to use monolithic and hybrid devices. This brings high speed capability to a much wider audience, hopefully opening up new applications. So, while the technique is not new, marketing claims notwithstanding, the opportunity is. Although current based designs have poorer DC performance than voltage amplifiers, their bandwidth advantage is undeniable. What's the magic?

Current Feedback Basics

William H. Gross

The distinctions of how current feedback amplifiers differ from voltage feedback amplifiers are not obvious at first, because, from the outside, the differences can be subtle. Both amplifier types use a similar symbol, and can be applied on a first order basis using the same equations. However, their behavior in terms of gain bandwidth trade-offs and large signal response is another story.

Unlike voltage feedback amplifiers, small signal bandwidth in a current feedback amplifier isn't a straight inverse function of closed loop gain, and large signal response is closer to ideal. Both benefits are because the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor (R_f) from output to inverting input works with internal junction capacitances to set the closed loop bandwidth. Even though the gain set resistor (R_g) from inverting input to ground works with the R_f to set the voltage gain, just as in a voltage feedback op amp, the closed loop bandwidth does not change. The explanation of this is fairly straightforward. The equivalent gain bandwidth product of the CFA is set by the Thevenin equivalent resistance at the inverting input and the internal compensation capacitor. If R_f is held constant and gain changed with R_g , the Thevenin resistance changes by the same amount as the gain. From an overall loop standpoint, this change in feedback attenuation will produce a change in noise gain, and a proportionate reduction of open loop bandwidth (as in a conventional op amp). With current feedback, however, the key point is that changes in Thevenin resistance also produce compensatory changes

in open loop bandwidth, unlike a conventional fixed gain bandwidth amplifier. As a result, the net closed loop bandwidth of a current-fed-back amplifier remains the same for various closed loop gains.

Figure H1 shows the LT1223 voltage gain vs frequency for five gain settings driving 100Ω . Shown for comparison is a plot of the fixed 100MHz gain bandwidth limitation that a voltage feedback amplifier would have. It is obvious that for gains greater than one, the LT1223 provides 3-20 times more bandwidth.

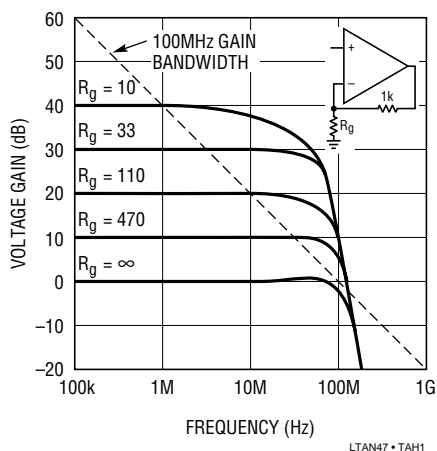


Figure H1. Voltage Gain vs Frequency for Current Feedback Amplifier (Family of Curves) and a Conventional Voltage Amplifier (Straight Line)

Because the feedback resistor determines the compensation of the LT1223, bandwidth and transient response can be optimized for almost every application. When operating on $\pm 15V$ supplies, R_f should be $1k\Omega$ or more for stability, but on $\pm 5V$, the minimum value is 680Ω , because the junction capacitors increase with lower voltage. For either case, larger feedback resistors can also be used, but will slow down the LT1223 (which may be desirable in some applications).

The LT1223 delivers excellent slew rate and bandwidth with better DC performance than previous current feed-

back amplifiers (CFAs). On $\pm 15V$ supplies with a $1k$ feedback resistor, the small signal bandwidth is $100MHz$ into a 400Ω load and $75MHz$ into 100Ω . The input will follow slew rates of $250V/\mu s$ with the output generating over $500V/\mu s$, and output slew rate is well over $1000V/\mu s$ for large input overdrive. Input offset voltage is $3mV$ (max), and input bias current is $3\mu A$ (max). A $10k\Omega$ pot, connected to pins 1 and 5 with wiper to V^+ , provides optional offset trimming. This trim shifts inverting input current about $\pm 10\mu A$, effectively producing input voltage offset.

The LT1223 also has shutdown control, available at pin 8. Pulling more than $200\mu A$ from pin 8 drops the supply current to less than $3mA$, and puts the output into a high impedance state. The easy way to force shutdown is to ground pin 8 using an open collector (drain) logic stage. An internal resistor limits current, allowing direct interfacing with no additional parts. When pin 8 is open, the LT1223 operates normally.

The difference in operating characteristics between op amps and CFAs result in slight differences in common circuit configurations. Figure H2 summarizes some popular circuit types, showing differences between op amps and CFAs. Gain can be set with either R_{IN} or R_f in an op amp, while a CFA's feedback resistor (R_f) is fixed. Op amp bandwidth is controllable with a feedback capacitor; for a CFA, bandwidth must be limited at the input. A feedback capacitor is never used. In an integrator, the $1k$ resistor must be included in the CFA so its negative input sees the optimal impedance. Finally, (not shown) there is no correlation between bias currents of a CFA's inputs. Because of this, source impedance matching will not improve DC accuracy. Matching input source impedances aids offset performance in op amps that do not have internal bias current cancellation.

Application Note 47

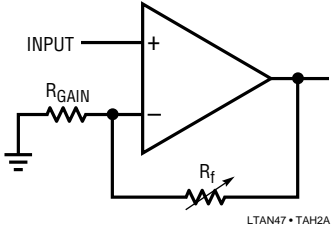
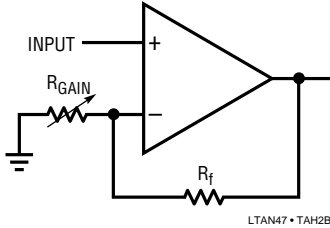
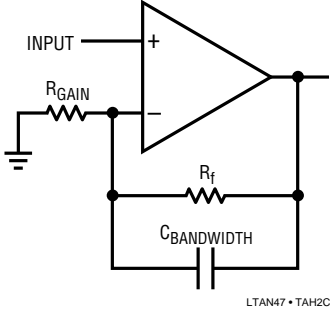
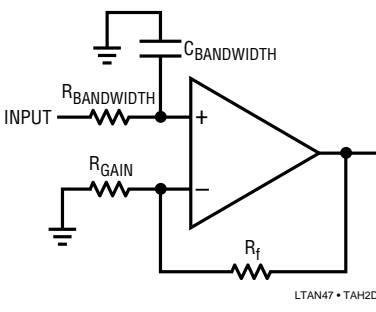
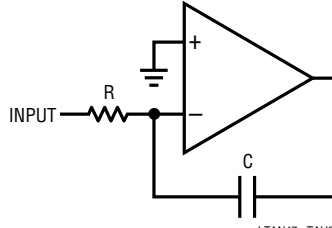
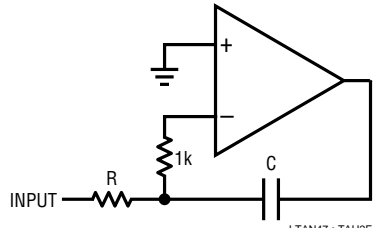
CIRCUIT TYPE	VOLTAGE FEEDBACK OP AMP	CURRENT FEEDBACK AMPLIFIER
SETTING GAIN	 <p style="text-align: right; font-size: small;">LTAN47 • TAH2A</p>	 <p style="text-align: right; font-size: small;">LTAN47 • TAH2B</p>
LIMITING BANDWIDTH	 <p style="text-align: right; font-size: small;">LTAN47 • TAH2C</p>	 <p style="text-align: right; font-size: small;">LTAN47 • TAH2D</p>
INTEGRATOR	 <p style="text-align: right; font-size: small;">LTAN47 • TAH2E</p>	 <p style="text-align: right; font-size: small;">LTAN47 • TAH2F</p>

Figure H2. Some Practical Differences in Applying Current and Voltage Amplifiers

APPENDIX I

High Frequency Amplifier Evaluation Board

LTC demo board 009 (photo, Figure I1, schematic, Figure I2) is designed to simplify the evaluation of high speed operational amplifiers. It includes both an inverting and non-inverting circuit, and extra holes are provided to allow the use of board-mounted BNC or SMA connectors. The two circuits are independent with the exception of shared power supply and ground connections.

Layout is a primary contributor to the performance of any high speed amplifier. Poor layout techniques adversely affect the behavior of a finished circuit. Several important layout techniques, all used in demo board 009, are described below:

1. Top side ground plane. The primary task of a ground plane is to lower the impedance of ground connections. The inductance between any two points on a uniform sheet of copper is less than the inductance of a thin, straight trace of copper connecting the same two points. The ground plane approximates the characteristics of a copper sheet and lowers the impedance at key points in the circuit, such as the grounds of connectors and supply bypass capacitors.
2. Ground plane voids. Certain components and circuit nodes are very sensitive to stray capacitance. Two good examples are the summing node of the op amp and the feedback resistor. Voids are put in the ground plane in these areas to reduce stray ground capacitance.
3. Input/output matching. The width of the input and output traces is adjusted to a stripline impedance of 50Ω . Note that the terminating resistors (R3 and R7) are connected to the end of the input lines, not at the connector. While stripline techniques aren't absolutely necessary for the demo board, they are important on larger layouts where line lengths are longer. The short lines on the demo board can be terminated in 50Ω , 75Ω , or 93Ω without adversely affecting performance.

4. Separation of input and output grounds. Even though the ground plane exhibits a low impedance, input and output grounds are still separated. For example, the termination resistors (R3 and R7) and the gain-setting resistor (R1) are grounded in the vicinity of the input connector. Supply bypass capacitors (C1, C2, C4, C5, C7, C8, C9 and C10) are returned to ground in the vicinity of the output connectors.

The circuit board is designed to accommodate standard 8-pin miniDIP, single operational amplifiers such as the LT1190 and LT1220 families. Both voltage and current feedback types can be used. Pins 1, 5 and 8 are outfitted with extra holes for use in adjusting DC offsets, compensation, or, in the case of the LT1223 and LT1190/1/2, for shutting down the amplifier.

If a current feedback amplifier such as the LT1223 is being evaluated, omit C3/C6. R4 and R6 are included for impedance matching when driving low impedance lines. If the amplifier is supposed to drive the line directly, or if the load impedance is high, R4 and R8 can be replaced by jumpers. Similarly R10 and R12 can be used to establish a load at the output of the amplifier.

Low profile sockets may be used for the op amps to facilitate changing parts, but performance may be affected above 100MHz.

High speed operational amplifiers work best when their supply pins are bypassed with R_f-quality capacitors. C1, C5, C8 and C10 should be 10nF disc ceramic or other capacitors with a self-resonant frequency greater than 10MHz. The polarized capacitors (C2, C4, C7, and C9) should be 1 μ F to 10 μ F tantalums. Most 10nF ceramics are self-resonant well above 10MHz and 4.7 μ F solid tantalums (axial leaded) are self-resonant at 1MHz or below. Lead lengths are critical; the self-resonant frequency of a 4.7 μ F tantalum drops by a factor of 2 when measured through 2" leads. Although a capacitor may become inductive at high frequencies, it is still an effective bypass component above resonance because the impedance is low.

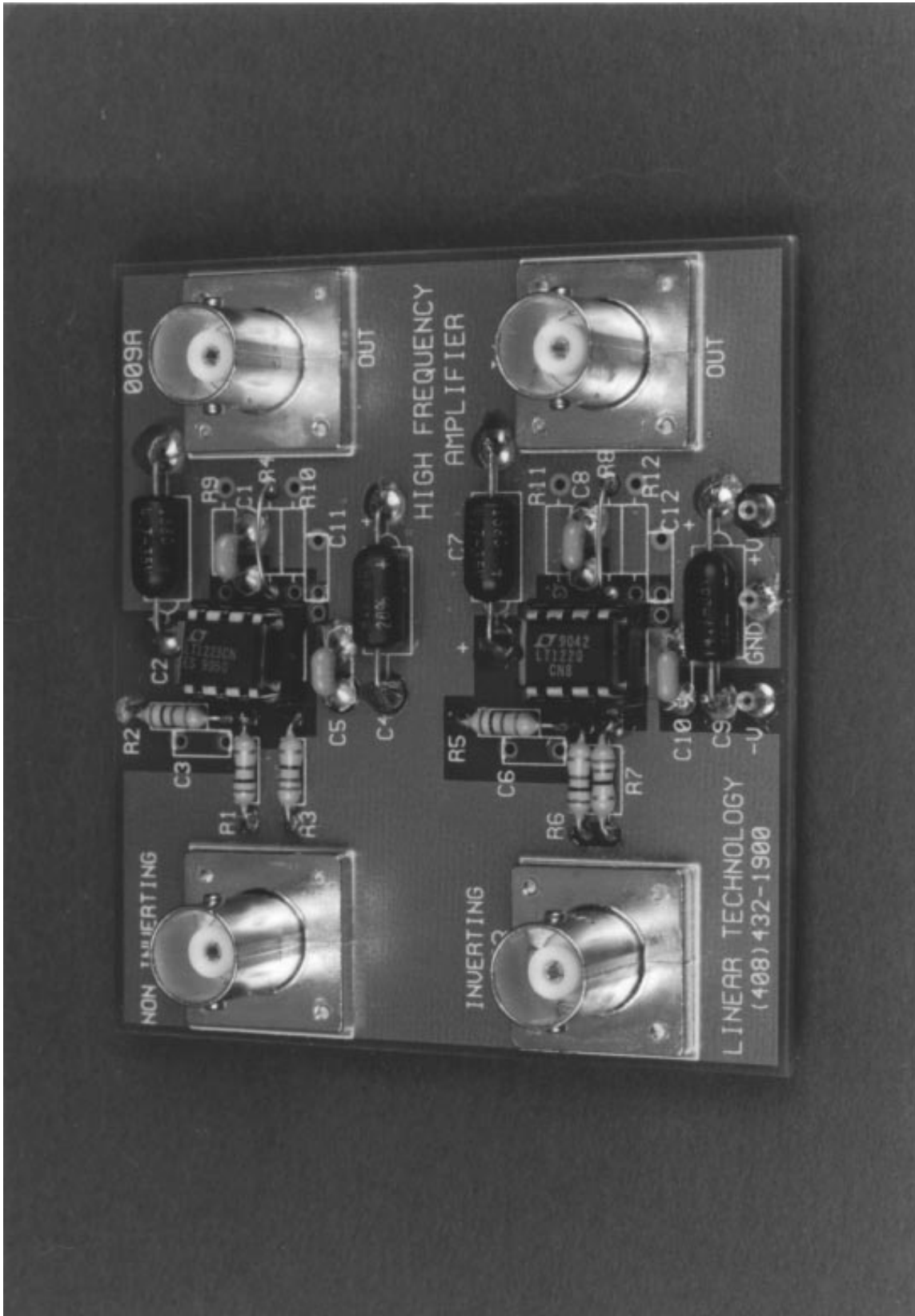
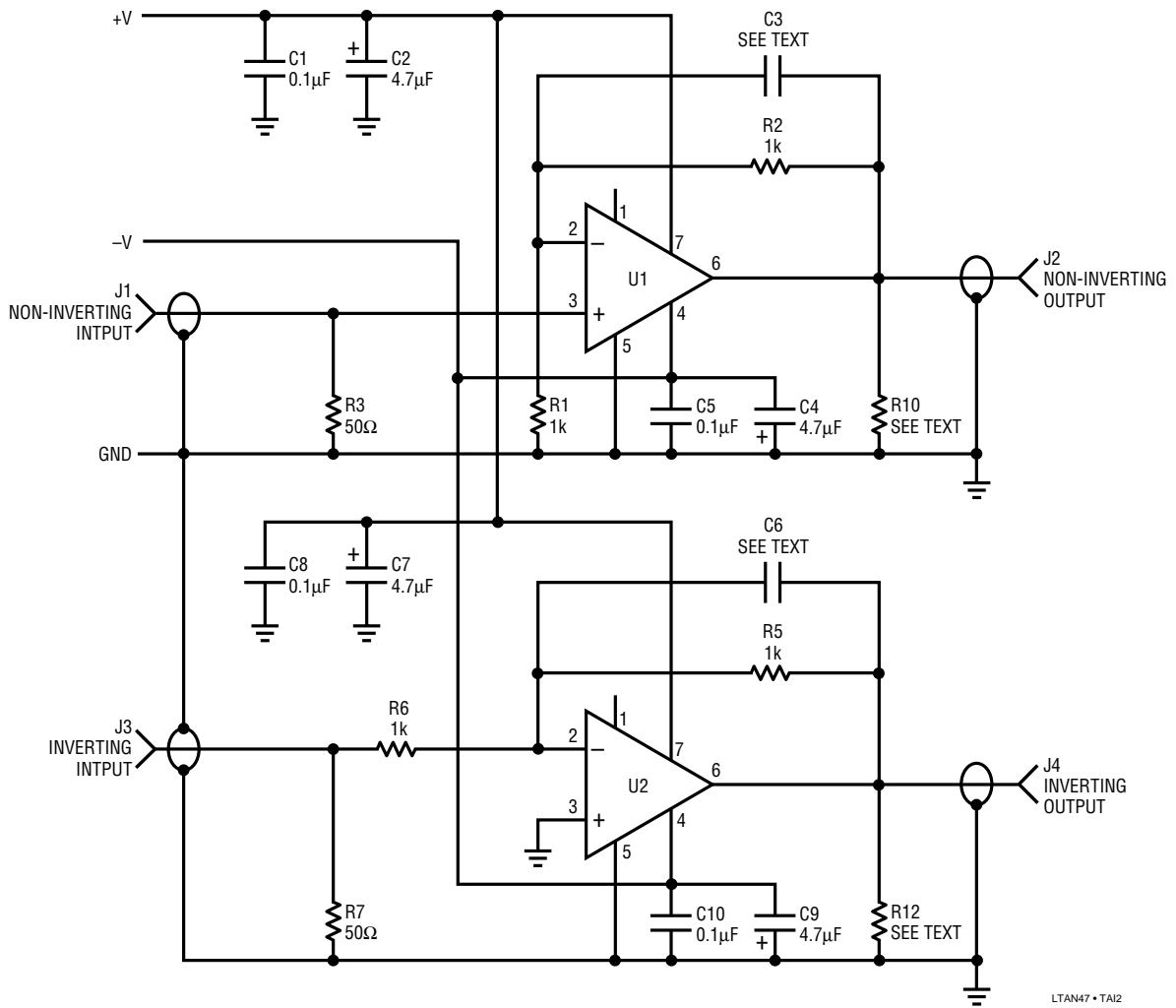


Figure 1. The Enticing LTC High Frequency Amplifier Demonstration Board. Sockets are Not Optimal, but Allow Trying Different Amplifiers



LTAN47 • TA12

Figure 12. High Frequency Amplifier Demonstration Board Schematic

APPENDIX J

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The Contributions of Edsel Murphy to the Understanding of the Behavior of Inanimate Objects

D. L. KLIPSTEIN

Abstract—Consideration is given to the effects of the contributions of Edsel Murphy to the discipline of electronics engineering. His law is stated in both general and special form. Examples are presented to corroborate the author's thesis that the law is universally applicable.

I. INTRODUCTION

IT HAS LONG BEEN the consideration of the author that the contributions of Edsel Murphy, specifically his general and special laws delineating the behavior of inanimate objects, have not been fully appreciated. It is deemed that this is, in large part, due to the inherent simplicity of the law itself.

It is the intent of the author to show, by references drawn from the literature, that the law of Murphy has produced numerous corollaries. It is hoped that by noting these examples, the reader may obtain a greater appreciation of Edsel Murphy, his law, and its ramifications in engineering and science.

As is well known to those versed in the state-of-the-art, Murphy's Law states that "If anything can go wrong, it will." Or, to state it in more exact mathematical form:

$$1 + 1^{*n} = 2 \quad (1)$$

where *n is the mathematical symbol for hardly ever.

Some authorities have held that Murphy's Law was first expounded by H. Cohen¹ when he stated that "If anything can go wrong, it will — during the demonstration." However, Cohen has made it clear that the broader scope of Murphy's general law obviously takes precedence.

To show the all-pervasive nature of Murphy's work, the author offers a small sample of the application of the law in electronics engineering.

II. GENERAL ENGINEERING

II.1. A patent application will be preceded by one week by a similar application made by an independent worker.

II.2. The more innocuous a design change appears, the further its influence will extend.

II.3. All warranty and guarantee clauses become void upon payment of invoice.

II.4. The necessity of making a major design change

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increases as the fabrication of the system approaches completion.

II.5. Firmness of delivery dates is inversely proportional to the tightness of the schedule.

II.6. Dimensions will always be expressed in the least usable term. Velocity, for example, will be expressed in furlongs per fortnight.²

II.7. An important Instruction Manual or Operating Manual will have been discarded by the Receiving Department.

II.8. Suggestions made by the Value Analysis group will increase costs and reduce capabilities.

II.9. Original drawings will be mangled by the copying machine.³

III. MATHEMATICS

III.1. In any given miscalculation, the fault will never be placed if more than one person is involved.

III.2. Any error that can creep in, will. It will be in the direction that will do the most damage to the calculation.

III.3. All constants are variables.

III.4. In any given computation, the figure that is most obviously correct will be the source of error.

III.5. A decimal will always be misplaced.

III.6. In a complex calculation, one factor from the numerator will always move into the denominator.

IV. PROTOTYPING AND PRODUCTION

IV.1. Any wire cut to length will be too short.

IV.2. Tolerances will accumulate unidirectionally toward maximum difficulty of assembly.

IV.3. Identical units tested under identical conditions will not be identical in the field.

IV.4. The availability of a component is inversely proportional to the need for that component.

IV.5. If a project requires n components, there will be $n-1$ units in stock.⁴

IV.6. If a particular resistance is needed, that value will not be available. Further, it cannot be developed with any available series or parallel combination.⁵

IV.7. A dropped tool will land where it can do the most damage. (Also known as the law of selective gravitation.)

IV.8. A device selected at random from a group having 99% reliability, will be a member of the 1% group.

IV.9. When one connects a 3-phase line, the phase

sequence will be wrong.⁶

IV.10. A motor will rotate in the wrong direction.⁷

IV.11. The probability of a dimension being omitted from a plan or drawing is directly proportional to its importance.

IV.12. Interchangeable parts won't.

IV.13. Probability of failure of a component, assembly, subsystem or system is inversely proportional to ease of repair or replacement.

IV.14. If a prototype functions perfectly, subsequent production units will malfunction.

IV.15. Components that must not and cannot be assembled improperly will be.

IV.16. A dc meter will be used on an overly sensitive range and will be wired in backwards.⁸

IV.17. The most delicate component will drop.⁹

IV.18. Graphic recorders will deposit more ink on humans than on paper.¹⁰

IV.19. If a circuit cannot fail, it will.¹¹

IV.20. A fail-safe circuit will destroy others.¹²

IV.21. An instantaneous power-supply crowbar circuit will operate too late.¹³

IV.22. A transistor protected by a fast-acting fuse will protect the fuse by blowing first.¹⁴

IV.23. A self-starting oscillator won't.

IV.24. A crystal oscillator will oscillate at the wrong frequency — if it oscillates.

IV.25. A pnp transistor will be an npn.¹⁵

IV.26. A zero-temperature-coefficient capacitor used in a critical circuit will have a TC of -750 ppm/ $^{\circ}$ C.

IV.27. A failure will not appear till a unit has passed Final Inspection.¹⁶

IV.28. A purchased component or instrument will meet its specs long enough, and only long enough, to pass Incoming Inspection.¹⁷

IV.29. If an obviously defective component is replaced in an instrument with an intermittent fault, the fault will reappear after the instrument is returned to service.¹⁸

IV.30. After the last of 16 mounting screws has been removed from an access cover, it will be discovered that the wrong access cover has been removed.¹⁹

IV.31. After an access cover has been secured by 16 hold-down screws, it will be discovered that the gasket has been omitted.²⁰

IV.32. After an instrument has been fully assembled, extra components will be found on the bench.

IV.33. Hermetic seals will leak.

V. SPECIFYING

V.1. Specified environmental conditions will always be exceeded.

V.2. Any safety factor set as a result of practical experience will be exceeded.

V.3. Manufacturers' spec sheets will be incorrect by a factor of 0.5 or 2.0, depending on which multiplier gives the most optimistic value. For salesmen's claims these factors will be 0.1 or 10.0.

V.4. In an instrument or device characterized by a number of plus-or-minus errors, the total error will be the sum of all errors adding in the same direction.

V.5. In any given price estimate, cost of equipment will exceed estimate by a factor of 3.²¹

V.6. In specifications, Murphy's Law supersedes Ohm's.

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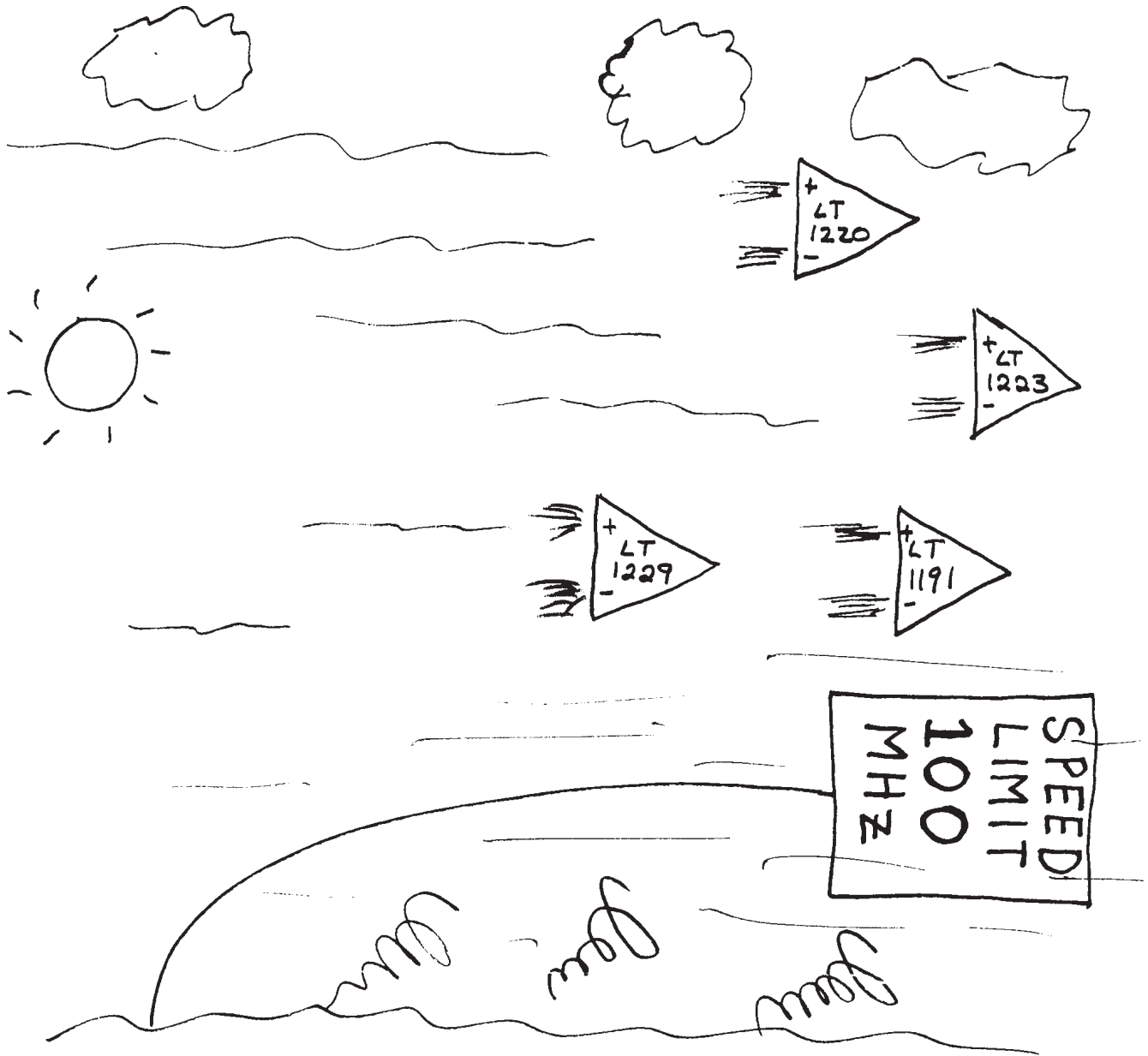
*In some cases where no reference is given, the source material was misplaced during preparation of this paper (another example of Murphy's Law). In accordance with the law, these misplaced documents will turn up on the date of publication of this paper.



The man who developed one of the most profound concepts of the twentieth century is practically unknown to most engineers. He is a victim of his own law. Destined for a secure place in the engineering hall of fame, something went wrong.

His real contribution lay not merely in the discovery of the law but more in its universality and in its impact. The law itself, though inherently simple, has formed a foundation on which future generations will build.

Application Note 47



(I WISH This App Note WENT AS FAST AS LTC Amplifiers)

W. L. L.
-91

Illumination Circuitry for Liquid Crystal Displays

Tripping the Light Fantastic . . .

Jim Williams

Current generation portable computers and instruments utilize back-lit liquid crystal displays (LCDs). Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps require high voltage AC to operate, mandating an efficient high voltage DC-AC converter. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

The LCD also requires a bias supply for contrast control. The supply's negative output should be regulated, and variable over a considerable range.

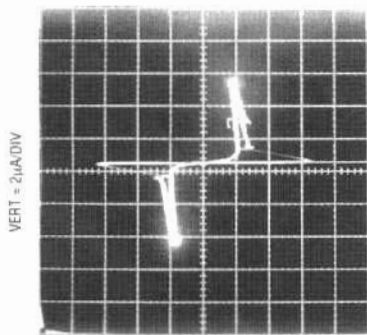
The small size and battery powered operation associated with LCD equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture, and long battery life is usually a priority. Laptop and hand held portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50%

of the battery drain. Additionally, these components, including PC board and all hardware, usually must fit within the LCD enclosure with a height restriction of 0.25".

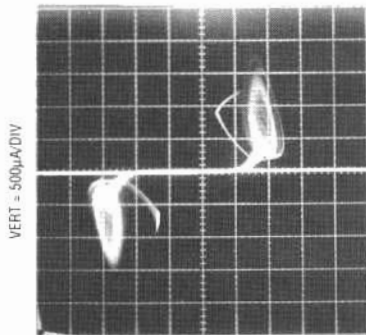
Cold Cathode Fluorescent Lamp (CCFL) Power Supplies

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are a difficult load to drive, particularly for a switching regulator. They have a "negative resistance" characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the start voltage is about 1000V, although higher and lower voltage bulbs are common. Operating voltage is usually 300V to 400V, although other bulbs may require different potentials (see Appendix E for a comparison of various backlights). The bulbs will operate from DC, but migration effects within the bulb will quickly damage it. As such, the waveform must be AC. No DC content should be present.

Figure 1A shows an AC driven bulb's characteristics on a curve tracer. The negative resistance induced "snap back" is apparent. In Figure 1B another bulb, acting against the curve tracer's drive, produces oscillation.



1A.



1B.

Figure 1. Negative Resistance Characteristic for Two CCFL Bulbs. "Snap Back" is Readily Apparent, Causing Oscillation in 1B. These Characteristics Complicate Power Supply Design

Application Note 49

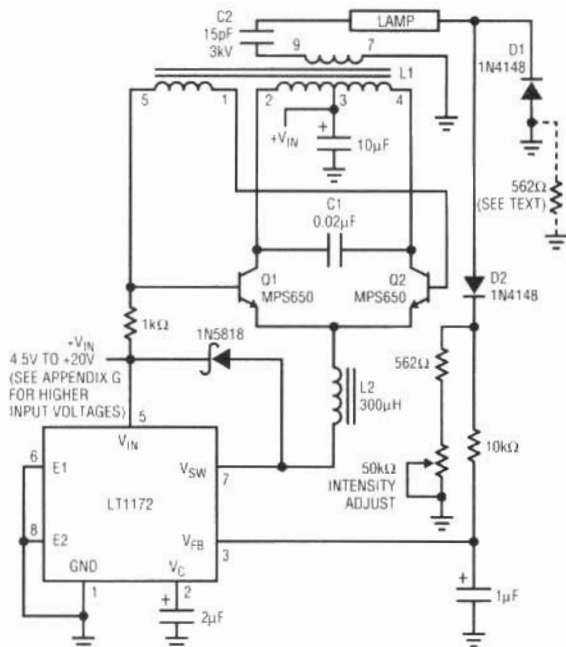
These tendencies, combined with the frequency compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on start-up. Once the lamp is in its operating region it assumes a linear load characteristic, easing stability criteria.

Bulb operating frequencies are typically 20kHz to 100kHz, and a sine-like waveform is preferred. The sine drive's low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.¹

Figure 2's circuit meets CCFL drive requirements. Efficiency is 78% with an input voltage range of 4.5V to 20V. 82% efficiency is possible if the LT1172 is driven from a low voltage (e.g., 3V-5V) source. Additionally, lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied the LT1172 switching regulator's feedback pin is below the device's internal 1.23V reference, causing full duty cycle modulation at the V_{SW} pin (trace A, Figure 3). L2 conducts current (trace B), which flows from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

L1 and the transistors comprise a current driven Royer class converter² which oscillates at a frequency primarily set by L1's characteristics (including its load) and the 0.02 μ F capacitor. LT1172 driven L2 sets the magnitude of the Q1-Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1172 is off. The LT1172's 100kHz clock rate is asynchronous with respect to the push-pull converter's (60kHz) rate, accounting for trace B's waveform thickening.

The 0.02 μ F capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (traces C and D respectively). L1 furnishes voltage step-up, and about 1400Vp-p appears at its secondary (trace E). Current flows through the 15pF capacitor into the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562 Ω -50k potentiometer chain. The positive half-sine appearing across these resistors (trace F) represents 1/2 the lamp current. This signal is filtered by the 10k-1 μ F pair and presented to the LT1172's feedback pin. This connection closes a control loop which regulates lamp current. The 2 μ F capacitor at the LT1172's V_C pin provides stable loop



- C1 = MUST BE A LOW LOSS CAPACITOR METALIZED POLYCARB WIMA FKP2 (GERMAN) RECOMMENDED
 - L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1. PIN NUMBERS SHOWN FOR COILTRONICS UNIT
 - L2 = COILTRONICS-CTX300-4
 - Q1, Q2 = AS SHOWN OR BCP 56 (PHILLIPS SO PACKAGE) **DO NOT SUBSTITUTE COMPONENTS**
- COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure 2. Cold Cathode Fluorescent Lamp (CCFL) Power Supply

compensation. The loop forces the LT1172 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0%-100% intensity control with no lamp dead zones or "pop-on" at low intensities.³ Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

Several points should be kept in mind when observing this circuit's operation. L1's high voltage secondary can only

Note 1: Many of the characteristics of CCFLs are shared by so called "Hot" cathode fluorescent lamps. See Appendix A, "Hot" Cathode Fluorescent Lamps.

Note 2: See Reference 3.

Note 3: Controlling a non-linear load's current, instead of its voltage, permits applying this circuit technique to a wide variety of nominally evil loads. See Appendix D, "A Related Circuit."

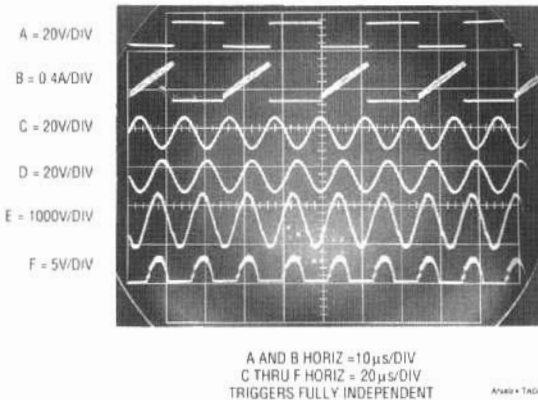


Figure 3. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B, and C through F

be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*⁴ Tektronix probe types P-6007 and P-6009 (acceptable) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1172's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 3 was obtained using a dual beam oscilloscope (Tektronix 556). LT1172 related traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Obtaining and verifying high efficiency⁵ requires some amount of diligence. The optimum efficiency values given for C1 and C2 are typical, and will vary for specific types of lamps. C1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristic. C2 ballasts the lamp, effectively buffering its negative resistance characteristic. Small values of C2 provide the most load isolation, but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage, but degrade load buffering. Also, C1's "best" value is somewhat dependent on the type of

lamp used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but generalized guidelines are possible. Typical values for C1 are 0.01µF to 0.047µF. C2 usually ends up in the 10pF to 47pF range. C1 *must* be a low loss capacitor and substitution of the recommended device is not recommended. A poor quality dielectric for C1 can easily degrade efficiency by 10%. C1 and C2 are selected by trying different values for each and iterating towards minimum input supply current. During this procedure insure that loop closure is maintained by monitoring the LT1172's feedback pin, which should be at 1.23V. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q1, Q2 and the output.

Other issues influencing efficiency include bulb wire length and energy leakage from the bulb. The high voltage side of the bulb should have the smallest practical lead length. Excessive length results in radiative losses which can easily reach 3% for a 3 inch wire. Similarly, no metal should contact or be in close proximity to the bulb. This prevents energy leakage which can exceed 10%.⁶

These considerations should be made with knowledge of other LCD issues. See Appendix B, "Mechanical Design Considerations for Liquid Crystal Displays." This section was guest written by Charles L. Guthrie of Sharp Electronics Corporation.

Special attention should be given to the layout of the circuit board since high voltage is generated at the output. The

Note 4: Don't say we didn't warn you!

Note 5: The term "efficiency" as used here applies to *electrical efficiency*. In fact, the ultimate concern centers around the efficient conversion of power supply energy into light. Unfortunately, lamp types show considerable deviation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life and history of any particular lamp. As such, this publication treats "efficiency" on an electrical basis; the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp has been selected the ratio of primary supply power to emitted lamp light energy may be measured with the aid of a photometer.

Note 6: A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the bulb at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb-forefinger combination towards the high voltage (higher field intensity) bulb end produces progressively greater input currents. Don't touch the high voltage lead or you may receive an electrical shock. Repeat: Don't touch the high voltage lead or you may receive an electrical shock.

output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination build-up can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. It is good practice for minimization of leakage to break the silk screen line which outlines transformer T1. This prevents leakage from the high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk screen ink for its ability to withstand high voltages.

Once these procedures have been followed efficiency can be measured. Efficiency may be measured by determining bulb current and voltage. Measuring current involves measuring RMS voltage across the 562Ω resistor (short the potentiometer). The bulb current is:

$$I_{\text{BULB}} = \left(\frac{E}{R} \right) \times 2$$

The X2 factor is necessitated because the diode steering dumps the current to ground on negative cycles. The shunting effects of the 10K-1μF RC across the 562Ω resistor introduce a small current measurement error. Because of this, best accuracy is obtained by measuring across a temporarily inserted 562Ω 1% unit in the ground lead of the negative current steering diode. Once this measurement is complete this second 562Ω resistor may be deleted and the negative current steering diode again returned directly to ground. Bulb RMS voltage is measured at the bulb with a properly compensated high voltage probe. Multiplying these two results gives power in watts, which may be compared to the DC input supply $E \times I$ product. In practice, the lamp's current and voltage contain small out of phase components but their error contribution is negligible.

Both the current and voltage measurements require a wideband True RMS voltmeter. The meter must employ a thermal type RMS converter—the more common logarithmic computing type based instruments are inappropriate because their bandwidth is too low.

The previously recommended high voltage probes are designed to see a 1MΩ-10pF-22pF oscilloscope input.

The RMS voltmeters have a 10MΩ input. This difference necessitates an impedance matching network between the probe and the voltmeter. Details on this and other efficiency measurement issues appear in Appendix C, "Achieving Meaningful Efficiency Measurements."

Two Tube Designs

Some displays require two tubes instead of the more popular single tube approach. These two tube designs usually require more power. Accommodating two tubes involves separate ballast capacitors (see Figure 4), but circuit operation is similar. Higher power may require a different transformer rating. Figure 2's transformer can supply 7.5mA, although more current is possible with appropriate transformer types. For reference, an 11mA capability transformer appears in Figure 4.

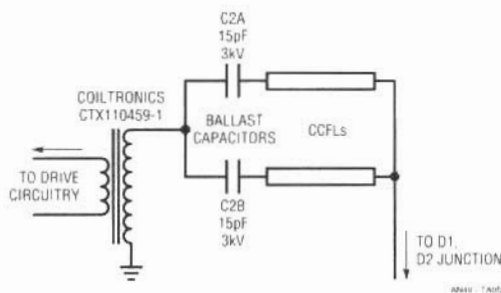


Figure 4. Driving Two Tubes. Capacitors Provide Ballast, Isolating the Tubes

The two tube designs reflect slightly different loading back through the transformer's primary. C2 usually ends up in the 10pF to 47pF range. Note that C2A and B appear with their lamp loads in parallel across the transformer's secondary. As such C2's value is often smaller than in a single tube circuit using the same type lamp. Ideally, the transformer's secondary current splits evenly between the C2-lamp branches, with the total load current being regulated. In practice, differences between C2A and B and differences in lamp wiring layout preclude a perfect current split. Practically, these differences are small, and the lamps appear to emit equal amounts of light.

Low Power CCFL Supply

Figure 5 is the other extreme. This design, the so-called "dim backlight," is optimized for single tube operation at very low currents. The circuit is meant for use at low input voltages, typically 2V to 6V. Figure 2's circuit drives 5mA maximum, but this design tops out at 1mA. This circuit maintains control down to tube currents of $1\mu\text{A}$, a very dim light! It is intended for applications where the longest possible battery life is desired. Primary supply drain ranges from hundreds of microamperes to 100mA with tube currents of microamps to 1mA. In shutdown the circuit pulls only $110\mu\text{A}$. Maintaining high efficiency at low tube currents requires modifying the basic design.

Achieving high efficiency at low operating current requires lowering Figure 2's quiescent power drain. To do this the LT1172, a pulse width modulator based device, is replaced with an LT1173. The LT1173 is a "burst mode" type regulator. When this device's feedback pin is too low it

delivers a burst of output current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground referred diode at the V_{SW} pin prevents substrate turn-on due to excessive L2 ring-off.

During the off periods the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, Figure 2's LT1172 pulse width modulator type regulator maintains "housekeeping" current between cycles. This results in more available output power but higher quiescent currents.

Figure 6 shows operating waveforms. When the regulator comes on (trace A, Figure 6) it delivers bursts of output current to the L1-Q1-Q2 high voltage converter. The converter responds with bursts of ringing at its resonant frequency. The circuit's loop operation is similar to Figure 2.⁷

Some bulbs may display non-uniform light emission at very low excitation currents. See Appendix F, "The Thermometer Effect."

LCD Bias Supplies

LCD's also require a bias supply for contrast control. The supply's variable negative output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. The logic sections of display drivers operate from single 5V supplies, but the actual driver outputs swing between +5V and a negative bias potential. Varying this bias causes the contrast of the display to vary.

An LCD bias generator, developed by Steve Pietkiewicz of LTC, is shown in Figure 7. In this circuit U1 is an LT1173 micropower DC to DC converter. The 3V input is converted to +24V by U1's switch, L2, D1, and C1. The switch pin (SW1) also drives a charge pump composed of C2, C3, D2, and D3 to generate -24V. Line regulation is less than 0.2%

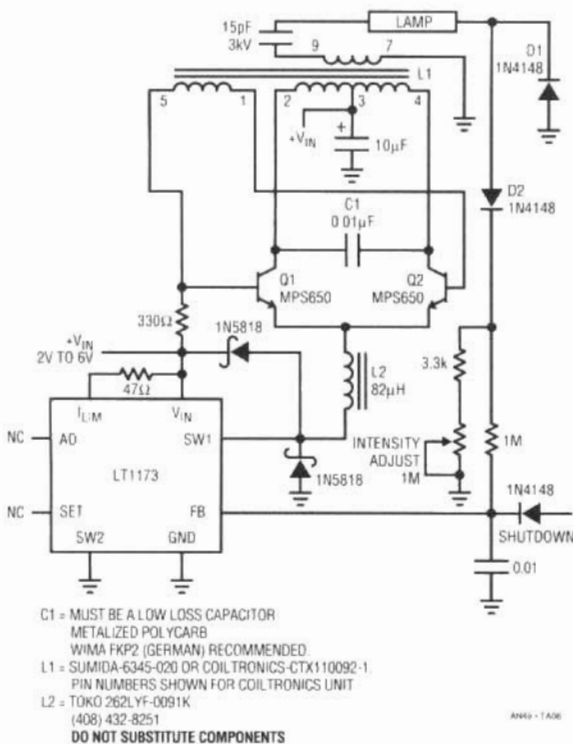


Figure 5. Low Power CCFL Power Supply. Circuit Controls Lamp Current over a $1\mu\text{A}$ to 1mA Range

Note 7: The discontinuous energy delivery to the loop causes substantial jitter in the burst repetition rate, although the high voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" mode region of most oscilloscopes, precluding a detailed display. "Alternate" mode operation causes waveform phasing errors, producing an inaccurate display. As such, waveform observation requires special techniques. Figure 6 was taken with a dual beam instrument (Tektronix 556) with both beams slaved to one time base. Single sweep triggering eliminated jitter artifacts. Most oscilloscopes, whether analog or digital, will have trouble reproducing this display.

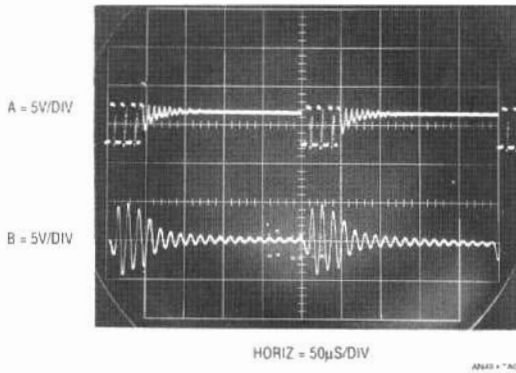


Figure 6. Waveforms for the Low Power CCFL Power Supply. LT1173 Burst Type Regulator (Trace A) Periodically Excites the Resonant High Voltage Converter (Q1 Collector is Trace B)

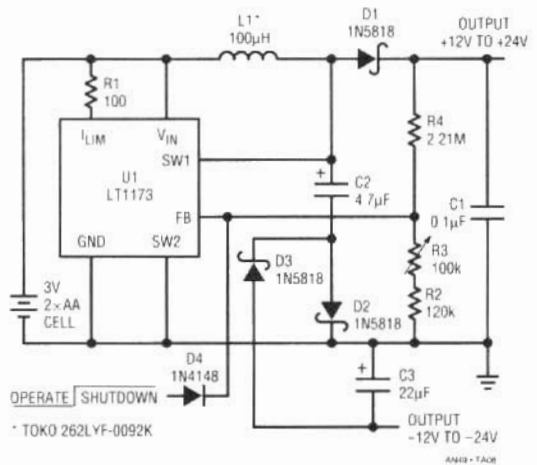


Figure 7. DC to DC Converter Generates LCD Bias

from 3.3V to 2V inputs. Load regulation, although suffering somewhat since the $-24V$ output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2V input at 75% efficiency.

If greater output power is required, Figure 7's circuit can be driven from a +5V source. R1 should be changed to 47Ω and C3 to $47\mu F$. With a 5V input, 40mA are available at 75% efficiency. Shutdown is accomplished by bringing the anode of D4 to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage.

Shutdown current is $110\mu A$ from the input source and $36\mu A$ from the shutdown signal.

A similar modification of a boost converter can provide negative bias from a 5V supply is shown in Figure 8. The converter, developed by Jon Dutra of LTC, is half switcher and half charge pump. The charge pump (C1, C2, D2, and D3) is driven by the flying node at V_{SW} . The output is variable from $-12V$ to $-24V$, providing contrast control for the display.

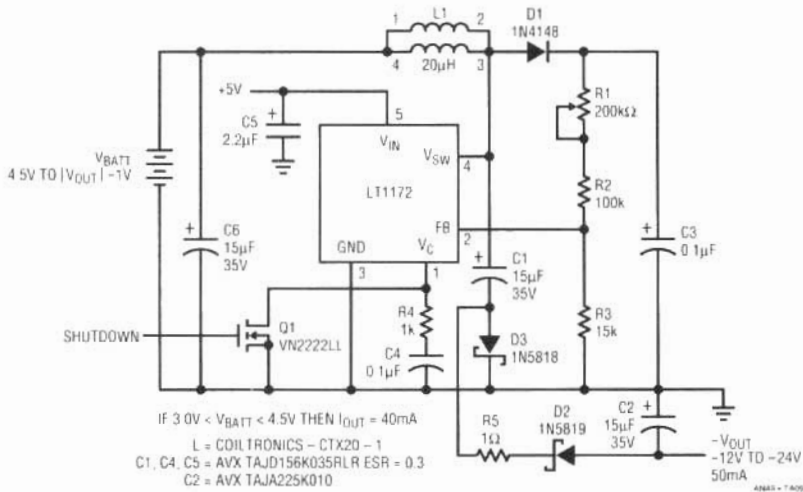


Figure 8. The Dutra Configuration Combines Switching Regulator and Charge Pump Techniques to Generate Negative Bias for LCD Drivers

On low voltage supplies (6V or less) V_{IN} and V_{BATT} can be tied together. With higher battery voltages, high efficiency is obtained by running the LT1172 V_{IN} pin from 5V. Shutting off the 5V supply automatically turns off the LT1172. The maximum value for V_{BATT} is equal to the negative output +1V. Also, the difference between V_{BATT} and V_{IN} must not exceed 16V. R1, R2, and R3 are made large to minimize battery drain in shutdown, since they are permanently connected to the battery via L1 and D1. Efficiency is about 80% at $I_{OUT} = 25mA$.

Note: This application note was derived from a manuscript originally prepared for publication in EDN Magazine.

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APPENDIX A

"HOT" CATHODE FLUORESCENT LAMPS

Many CCFL characteristics are shared by so-called "Hot" Cathode Fluorescent Lamps (HCFLs). The most significant difference is that HCFLs contain filaments at each end of the tube (see Figure A1). When the filaments are powered they emit electrons, lowering the tube's ionization potential. This means a significantly lower voltage will start the tube. Typically the filaments are turned on, a relatively modest high voltage impressed across the tube, and start-up occurs. Once the tube starts filament power is removed. Although HCFLs reduce the high voltage requirement they require a filament supply and sequencing circuitry. The CCFL circuits shown in the text will start and run HCFLs without using the filaments. In practice this involves simply driving the filament connections at the HCFL tube ends as if they were CCFL electrodes.

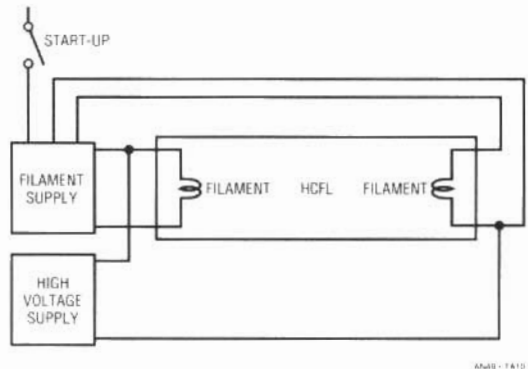


Figure A1. A Conceptual Hot Cathode Fluorescent Lamp Power Supply. Heated Filaments Liberate Electrons, Lowering the Tube's Start-Up Voltage Requirement. CCFL Supply Discussed in Text Eliminates Filament Supply

APPENDIX B

MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS

Charles L. Guthrie, Sharp Electronics Corporation

Introduction

As more companies begin the manufacturing of their next generation of computers, there is a need to reduce the overall size and weight of the units to improve their portability. This has sparked the need for more compact designs where the various components are placed in closer proximity, thus making them more susceptible to interaction from signal noise and heat dissipation. The following is a summary of guidelines for the placement of the display components, and a summary of suggestions for overcoming difficult design constraints associated with component placement.

In notebook computers, the thickness of the display housing is important. The design usually requires the display to be in a pivotal structure so that the display may be folded down over the keyboard for transportation. Also, the outline dimensions must be minimal so that the package will remain as compact as possible. These two constraints drive the display housing design and placement of the display components. This discussion surveys each of the problems facing the designer in detail and offers suggestions for overcoming the difficulties to provide a reliable assembly.

The problems facing the pen based computer designer are similar to those realized in notebook designs. In addition, however, pen based designs require protection for the face of the display. In pen based applications, as the pen is moved across the surface of the display, the pen has the potential for scratching the front polarizer. For this reason, the front of the display must be protected. Methods for protecting the display face while minimizing effects on the display image are given.

Additionally, the need to specify the flatness of the bezel is discussed. Suggestions for acceptable construction techniques for sound design are included. Further, display components likely to cause problems due to heat buildup are identified and methods for minimization of the heat's effects are presented.

The ideas expressed here are not the only solutions to the various problems, and have not been assessed as to whether they may infringe on any patents issued or applied for.

Flatness and Rigidity of the Bezel

In the notebook computer, the bezel has several distinct functions. It houses the display, the inverter for the backlight, and in some instances, the controls for contrast and brightness of the display. The bezel is usually designed to tilt to set the optimum viewing angle for the display.

It is important to understand that the bezel must provide a mechanism to keep the display flat, particularly at the mounting holds. Subtle changes in flatness place uneven stress on the glass which can cause variations in contrast across the display. Slight changes in pressure may cause significant variation in the display contrast. Also, at the extreme, significantly uneven pressures can cause the display glass to fail.

Because the bezel must be functional in maintaining the flatness of the display, consideration must be made for the strength of the bezel. Care must be taken to provide structural members, while minimizing the weight of the unit. This may be executed using a parallel grid, normal to the edges of the bezel, or angled about 45° off of the edges of the bezel. The angled structure may be more desirable in that it provides resistance to torquing the unit while lifting the cover with one hand. Again, the display is sensitive to stresses from uneven pressure on the display housing.

Another structure which will provide excellent rigidity, but adds more weight to the computer, is a "honeycomb" structure. This "honeycomb" structure resists torquing from all directions and tends to provide the best protection for the display.

With each of these structures it is easy to provide mounting assemblies for the display. "Blind nuts" can be molded

into the housing. The mounting may be done to either the front or rear of the bezel. Attachment to the rear may provide better rigidity for placement of the mounting hardware.

One last caution is worth noting in the development of a bezel. The bezel should be engineered to absorb most of the shock and vibration experienced in a portable computer. Even though the display has been carefully designed, the notebook computer presents extraordinary shock and abuse problems.

Avoiding Heat Buildup in the Display

Several of the display components are sources for heat problems. Thermal management must be taken into account in the design of the display bezel. A heated display may be adversely affected; a loss of contrast uniformity usually results. The Cold Cathode Fluorescent Tube (CCFT) itself gives off a small amount of heat relative to the amount of current dissipated in its glow discharge. Likewise, even though the inverters are designed to be extremely efficient, there is some heat generated. The buildup of heat in these components will be aggravated by the typically "tight" designs currently being introduced. There is little ventilation designed into most display bezels. To compound the problem, the plastics used are poor thermal conductors, thus causing the heat to build up which may affect the display.

Some current designs suffer from poor placement of the inverter and/or poor thermal management techniques. These designs can be improved, even where redesign of the display housing, with improved thermal management, is impractical.

One of the most common mistakes in current designs is that there has been no consideration for the build up of heat from the CCFT. Typically, the displays for notebook applications have only one CCFT to minimize display power requirements. This lamp is usually placed along the right edge of the display. Since the lamp is placed very close to the display glass, it can cause a temperature rise in the liquid crystal. It is important to note that variations in temperature of as little as 5°C can cause an apparent non-uniformity in display contrast. Variations caused by slightly higher temperature variations will cause objectionable variations in the contrast and display appearance.

To further aggravate the situation, some designs have the inverter placed in the bottom of the bezel. This has a tendency to cause the same variations in contrast, particularly when the housing does not have any heat sinking for the inverter. This problem manifests itself as a "blooming" of the display, just above the inverter. This "blooming" looks like a washed out area where, in the worst case, the characters on the display fade completely.

The following section discusses the recommended methods for overcoming these design problems.

Placement of the Display Components

One of the things that can be done is to design the inverter into the base of the computer with the mother board. In some applications this is impractical because this requires the high voltage leads to be mounted within the hinges connecting the display bezel to the main body. This causes a problem with strain relief of the high voltage leads, and thus with U.L. Certification.

One mistake, made most often, is placing the inverter at the bottom on the bezel next to the lower edge of the display. It is a fact that heat rises, yet this is one of the most overlooked problems in new notebook designs. Even though the inverters are very efficient, some energy is lost in the inverter in the form of heat. Because of the insulating properties of the plastic materials used in the bezel construction, heat builds up and affects the display contrast.

Designs with the inverter at the bottom can be improved in one of three ways. The inverter can be relocated away from the display; heat sinking materials can be placed between the display and the inverter; or ventilation can be provided to remove the heat.

In mature designs, it may be impractical to do what is obvious and move the inverter up to the side of the display towards the top of the housing. In these cases, the inverter may be insulated from the display with a "heat dam". One method of accomplishing this would be to use a piece of mica insulator die cut to fit tightly between the inverter and the display. This heat dam would divert the heat around the end of the display bezel to rise harmlessly to the top of the housing. Mica is recommended in this application because of its thermal and electrical insulating properties.

The last suggestion for removing heat is to provide some ventilation to the inverter area. This has to be done very carefully to prevent exposing the high voltage. Ventilation may not be a practical solution because resistance to liquids and dust is compromised.

The best solution for the designer of new hardware is to consider the placement of the inverter to the side of the display and at the top of the bezel. In existing designs of this type the effects of heat from the inverter, even in tight housings, has been minimal or non-existent.

One problem which is aggravated by the placement of the inverter at the bezel is heat dissipated by the CCFT. In designs where the inverter is placed up and to the side of the display, fading of the display contrast due to CCFT heat is not a problem. However, when the inverter is placed at the bezel bottom, some designs experience a loss of contrast aggravated by the heat from the CCFT and inverter.

In cases where the inverter must be left at the bottom, and the CCFT is causing a loss of contrast, the problem can be minimized by using an aluminum foil heat sink. This does not remove the heat from the display, but dissipates it over the entire display area, thus normalizing the display contrast. The aluminum foil is easy to install and in some present designs has successfully improved the display contrast.

Remember that the objection to the contrast variation stems more from non-uniformity than from a total loss of contrast.

Protecting the Face of the Display

One of the last considerations in the design of notebook and pen based computers is protection of the display face.

The front polarizer is made of a mylar base and thus is susceptible to scratching. The front protection for the display, along with providing scratch protection, may also provide an anti-glare surface.

There are several ways that scratch resistance and anti-glare surfaces can be incorporated. A glass or plastic cover may be placed over the display, thus providing protection. The material should be placed as close to the display as possible to minimize possible parallax problems due to reflections off of the cover material. With anti-glare materials, the further the material is from the front of the display the greater the distortion.

In pen applications, the front anti-scratch material is best placed in contact with the front glass of the display. The cover glass material normally needs to be slightly thicker to protect the display from distortion when pressure is being exerted on the front.

There are several methods for making the pen input devices. Some use the front surface of the cover glass to provide input data and some use a field effect to a printed wiring board on the back of the display. When the pen input is on the front of the display, the input device is usually on a glass surface.

To limit specular reflection in this application, the front cover glass should be bonded to the display. Care must be taken to insure that the coefficient of thermal expansion is matched for all of the materials used in the system. Because of the difficulties encountered with the bonding of the cover glass, and the potential to destroy the display through improper workmanship, consulting an expert is strongly recommended.

APPENDIX C

ACHIEVING MEANINGFUL EFFICIENCY MEASUREMENTS

Efficiency measurement is difficult. The most important points for getting good efficiency measurements are:

- Use proper equipment.
- Measure carefully.
- Measure with the CCFL you intend to use. Simple resistive loads or substitute lamps can cause 5-10% errors.

- Measure with the circuit components and layout you intend to use.

Obtaining reliable efficiency data for the CCFL circuits requires attention to measurement technique. The combination of high frequency, harmonic laden waveforms and high voltage makes meaningful results difficult to obtain.

The choice, understanding and use of test instrumentation is crucial. Clear thinking is needed to avoid unpleasant surprises!¹

Probes

The probes employed must faithfully respond over a variety of conditions. Measuring across the resistor in series with the CCFL is the most favorable circumstance. This low voltage, low impedance measurement allows use of a standard 1X probe. The probe's relatively high input capacitance does not introduce significant error. A 10X probe may also be used, but frequency compensation issues (discussion to follow) must be attended to.

The high voltage measurement across the lamp is considerably more demanding on the probe. The waveform fundamental is at 20kHz to 100kHz, with harmonics into the MHz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects which would corrupt the measurement. The design and construction of such a probe requires significant attention. Figure C1 lists some recommended probes along with their characteristics. As stated in the text, almost all

standard oscilloscope probes *will fail*² if used for this measurement. Attempting to circumvent the probe requirement by resistively voltage dividing the lamp voltage also creates problems. Large value resistors often have significant voltage coefficients and their shunt capacitance is high and uncertain. As such, simple voltage dividing is not recommended. Similarly, common high voltage probes intended for DC measurement will have large errors because of AC effects. The P6013A and P6015 are the favored probes; their 100M Ω input and small capacitance introduces low loading error. The penalty for their 1000X attenuation is reduced output, but the recommended voltmeters (discussion to follow) can accommodate this.

All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1M Ω paralleled by (typically) 10pF-22pF. The recommended voltmeters, which will be discussed, have significantly different input characteristics. Figure C2's table shows higher input resistances and a range of capacitances. Because of this the probe must be compensated for the

Note 1: It is worth considering that various constructors of text Figure 2 have reported efficiencies ranging from 8% to 115%.

Note 2: That's twice we've warned you nicely.

TEKTRONIX PROBE TYPE	ATTENUATION FACTOR	ACCURACY	INPUT RESISTANCE	INPUT CAPACITANCE	RISE TIME	BANDWIDTH	MAXIMUM VOLTAGE	DERATED ABOVE	DERATED TO AT FREQUENCY	COMPENSATION RANGE	ASSUMED TERMINATION RESISTANCE
P6007	100X	3%	10M Ω	2.2pF	14ns	25MHz	1.5kV	200kHz	700V _{RMS} at 10MHz	15-55pF	1M
P6009	100X	3%	10M Ω	2.5pF	2.9ns	120MHz	1.5kV	200kHz	450V _{RMS} at 40MHz	15-47pF	1M
P6013A	1000X	Adjustable	100M Ω	3pF	7ns	50MHz	12kV	100kHz	800V _{RMS} at 20MHz	12-60pF	1M
P6015	1000X	Adjustable	100M Ω	3pF	1.4ns	250MHz	20kV	100kHz	2000V _{RMS} at 20MHz	12-47pF	1M

Figure C1. Characteristics of Some Wideband High Voltage Probes. Output Impedances are Designed for Oscilloscope Inputs

MANUFACTURER AND MODEL	FULL SCALE RANGES	ACCURACY AT 1MHz	ACCURACY AT 100kHz	INPUT RESISTANCE AND CAPACITANCE	MAXIMUM BANDWIDTH	CREST FACTOR
Hewlett-Packard 3400 Meter Display	1mV to 300V, 12 Ranges	1%	1%	0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF	10MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Hewlett-Packard 3403C Digital Display	10mV to 1000V, 6 Ranges	0.5%	0.2%	10mV and 100mV Range = 20M and 20pF $\pm 10\%$, 1V to 1000V Range = 10M and 24pF $\pm 10\%$	100MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Fluke 8920A Digital Display	2mV to 700V, 7 Ranges	0.7%	0.5%	10M and < 30pF	20MHz	7:1 At Full Scale, 70:1 At 0.1 Scale

Figure C2. Pertinent Characteristics of Some Thermally Based RMS Voltmeters. Input Impedances Necessitate Matching Network and Compensation for High Voltage Probes

Application Note 49

voltmeter's input characteristics. Normally, the optimum compensation point is easily determined and adjusted by observing probe output on an oscilloscope. A known amplitude square wave is fed in (usually from the oscilloscope calibrator) and the probe adjusted for correct response. Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct.

The impedance mismatch occurs at low and high frequency. The low frequency term is corrected by placing an appropriate value resistor in shunt with the probe's output. For a 10M Ω voltmeter input a 1.1M Ω resistor is suitable. This resistor should be built into the smallest possible BNC equipped enclosure to maintain a coaxial environment. No cable connections should be employed; the enclosure should be placed *directly* between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low frequency impedance mismatch.

Correcting the high frequency mismatch term is more involved. The wide range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. How is the experimenter to know where to set the high frequency probe compensation adjustment? One solution is to feed a known value RMS signal to the probe-voltmeter combination and adjust compensation for a proper reading. Figure C3 shows a simple way to generate a known RMS voltage. This scheme takes advantage of the recommended voltmeter's insensitivity to waveform shape. The CMOS flip-flop is driven from a stable 10.00V source.

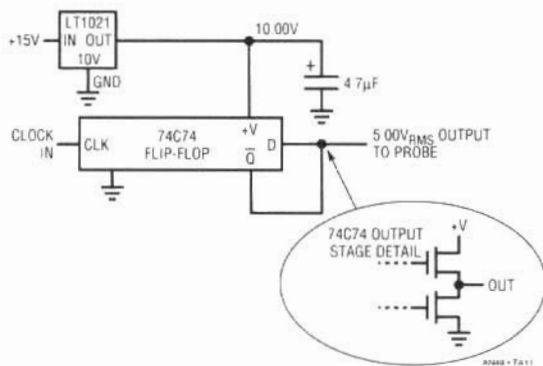


Figure C3. The RMS Calibrator. MOSFET Output Stage Detail Shows Purely Ohmic Switching to Power Rails

The CMOS output stage, which is purely ohmic, produces essentially errorless switching between the power supply rails. Clocking the flip-flop produces a square wave output with a 10.00V amplitude. The result is a known 5.00V_{RMS} output. Now, the probe's compensation is adjusted for a 5.00V voltmeter reading. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If the probe compensation is altered (e.g., for proper response on an oscilloscope) the voltmeter's reading will be erroneous.³

RMS Voltmeters

The efficiency measurements require an RMS responding voltmeter. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all AC voltmeters, including DVMs with AC ranges.

There are a number of ways to measure RMS AC voltage. Three of the most common include *average*, *logarithmic*, and *thermally* responding. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true RMS value. Although these instruments are "real time" analog computers their 1% error bandwidth is well below 300kHz and crest factor capability is limited. Almost all general purpose DVMs use such a logarithmically based approach and, as such, are not suitable for CCFL efficiency measurements. Thermally based RMS voltmeters are direct acting thermo-electronic analog computers. They respond to the input's RMS heating value. This technique is explicit, relying on the very definition of RMS (e.g., the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques.⁴ Additionally, they are insensitive to waveform shape and easily

Note 3: The translation of this statement is to hide the probe when you are not using it. If anyone wants to borrow it, look straight at them, shrug your shoulders, and say you don't know where it is. This is decidedly dishonest, but eminently practical. Those finding this morally questionable may wish to re-examine their attitude after producing a days worth of worthless data with a probe that was unknowingly readjusted.

Note 4: Those finding these descriptions intolerably brief are commended to References 5, 6 and 7.

accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

Figure C4 shows a conceptual thermal RMS-DC converter. The input waveform warms a heater, resulting in increased output from its associated temperature sensor. A DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common mode term, eliminating their effect. Also, although the voltage and thermal interaction is non-linear, the input-output RMS voltage relationship is linear with unity gain.

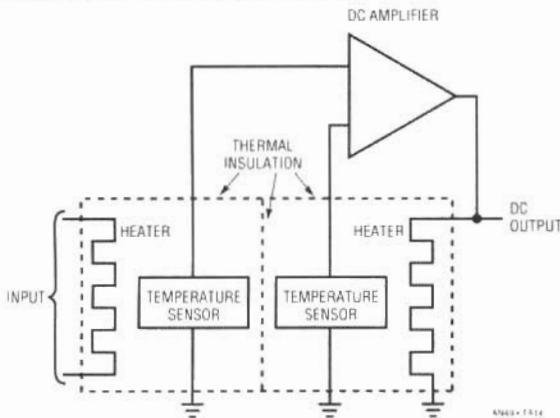


Figure C4. Conceptual Thermal RMS-DC Converter

The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier will reject this common mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure C4's output is linear because the matched thermal pair's non-linear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS-DC measurements.

The instruments listed in Figure C2, while considerably more expensive than other options, are typical of what is required for meaningful results. The HP3400A and the Fluke 8920A are currently available from their manufacturers. The HP3403C, an exotic and highly desirable instrument, is no longer produced but readily available on the secondary market.

APPENDIX D

A RELATED CIRCUIT

The high voltage compliance current loop approach of the CCFL power supply suits other applications. The current sensing permits precise high efficiency control of a wide variety of difficult loads. A HeNe Laser represents such a load. Lasers are negative impedances operating at very high voltages. Typically, they require 6kV-10kV to start, with an operating voltage in the 1kV-3kV region. Best optical characteristics are achieved by controlling the current through the laser. Simple high voltage drive does not provide this. Figure D1 adapts the CCFL circuitry to control a laser. Both tube current stability and electrical efficiency are improved over the more conventional voltage mode drive.

The start-up and sustaining functions have been combined into a single closed loop current source with over 10kV of compliance. When power is applied, the Laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.48μF capacitor resonates with L1, providing boosted, sine wave drive. L2 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L2's secondary

Application Note 49

form a voltage tripler, producing over 10kV across the Laser. The Laser breaks down and current begins to flow through it. The 47k Ω resistor ballasts the Laser, limiting current. The current flow causes a voltage to appear across the 190 Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts its pulse width drive to L2 to maintain the FB pin at 1.23V regardless of changes in operating conditions. In this fashion the Laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by varying the 190 Ω value. The 1N4002 diode string clamps excessive voltages when Laser conduction first begins, protecting the LT1170. The 10 μ F capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting.

The circuit will start and run the Laser over a 9V–35V input range with an electrical efficiency of about 75%.

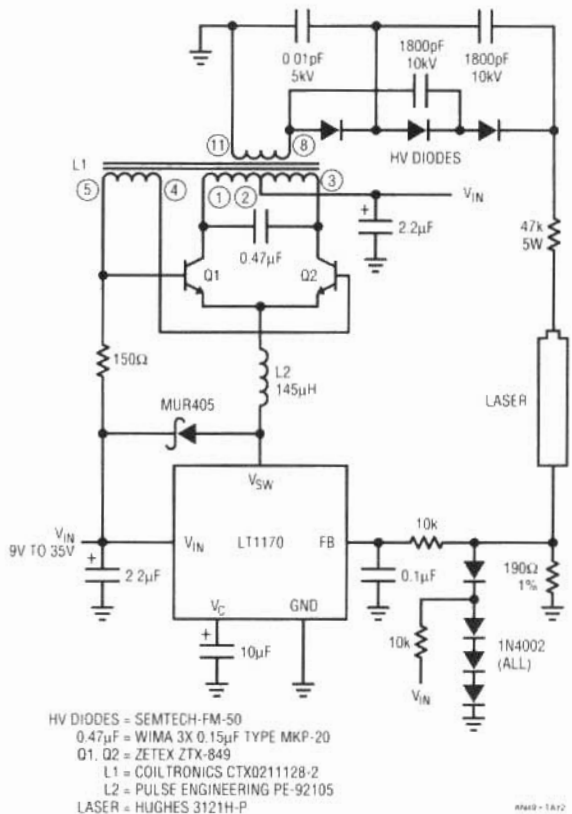


Figure D1. Laser Power Supply is Essentially a 10kV Compliance Current Source

APPENDIX E

BACKLIGHT CHARACTERISTICS

DISPLAY TYPE	RUN VOLTAGE	START VOLTAGE	DISCHARGE CURRENT IN mA	BRIGHTNESS IN nt	POWER CONSUMPTION IN WATTS
CXA-M10M	480 \pm 80	1200 MIN	4-6	5000 TYP	2.4
EMI-1231	355 \pm 60	1200 TYP	5 \pm 1	10,000	1.8
LM000105	340 \pm 60	1200 MIN	5 \pm 1	5000 MIN	1.7
CXA-1301	335 \pm 25	1000 TYP	5 \pm 1	2300 MIN	1.7
CXA-M10M	300 \pm 30	1300 MIN	5.3 TYP	8000 MIN	1.8
CSA-0113	290 \pm 60	1000 TYP	3.0	4500	.87
EHI-1231	280 TYP	1100 MIN	3.5-7	10,000 TYP	2

Figure E1. Characteristics of Some Sharp Corporation LCD Backlights

APPENDIX F

THE THERMOMETER EFFECT

Bulbs operating at very low currents may display the "thermometer effect"; that is, light intensity may be non-uniformly distributed along the bulb's length. Although bulb current density is uniform, the associated electromagnetic field is not. The field's low intensity, combined with its gradient, means that there is not enough energy to maintain uniform phosphor glow beyond some point.

Bulbs displaying the thermometer effect emit most of their light near the high voltage electrode, with rapid emission fall-off as distance from the electrode increases. Placing a conductor along the bulb's length largely alleviates "thermometering." The trade-off is decreased efficiency due to energy leakage (see footnote 6 and associated text). It is worth noting that various bulb types have different degrees of susceptibility to the thermometer effect.

APPENDIX G

OPERATION FROM HIGH VOLTAGE INPUTS

Some applications require higher input voltages. The 20V maximum input specified in Figures 2 and 4 is set by the LT1172 going into its isolated flyback mode (see LT1072 and LT1172 data sheets), not breakdown limits. If the LT1172 is driven from a low voltage source (e.g., 5V) the 20V limit may be extended by using Figure G1's network. If the LT1172 is driven from the same supply as L1's center tap the network is unnecessary.

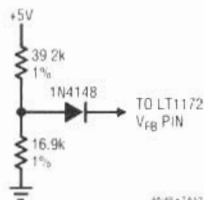

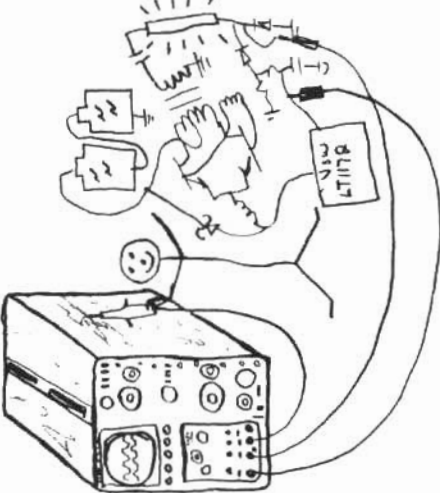
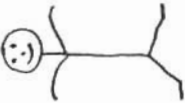


Figure G1. Network Allows CCFL Operation Beyond 20V Inputs

<p>When I WAS 4 Years Old I PLAYED WITH LIGHT BULBS AND BATTERIES. I Loved it.</p>  <p>A simple stick figure is shown with a light bulb above its head. To the right of the figure are two battery symbols, one above the other.</p>	<p>Now, I'm 44 Years Old & I STILL Play With light Bulbs & batteries. I Love it.</p>  <p>The stick figure is shown interacting with a complex circuit board. The circuit includes a light bulb, several batteries, and various electronic components like resistors and capacitors. Wires connect the components, and some are labeled with 'V', 'A', and 'mA'.</p>	<p>I Guess I Matured Early</p>  <p>A simple stick figure with a smiling face is shown in the top right panel.</p>
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CALL ME ABOUT YOUR BACKLIGHT APPLICATION

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Techniques for 92% Efficient LCD Illumination

Waste Not, Want Not . . .

Jim Williams

INTRODUCTION

In August of 1992 LTC published Application Note 49, "Illumination Circuitry for Liquid Crystal Displays." One notable aspect of this event is that it generated more response *than all previous LTC application notes combined*. This level of interest, along with significant performance advances since AN-49's appearance, justifies further discussion of LCD backlighting circuitry.

This publication includes pertinent information from the previous effort in addition to updated sections and a large body of new material. The partial repetition is a small penalty compared to the benefits of text flow, completeness and time efficient communication. The most noteworthy performance advance is achievement of 92% efficiency for the backlight power supply. Additional new benefits include low voltage operation, synchronizing capability, higher output power for color displays, and extended dimming range.

A practical 92% efficient LCD backlight design is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and the physical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing and other items has a major effect on electrical characteristics. The greatest care in every detail is required to achieve a practical high efficiency LCD backlight. Getting the lamp to light is just the beginning!

Current generation portable computers and instruments utilize back-lit liquid crystal displays (LCDs). These displays have also appeared in applications ranging from medical equipment to automobiles, gas pumps and retail terminals. Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps require high voltage AC to operate, mandating an efficient high voltage DC-AC converter. In addition to good efficiency, the converter should deliver

the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency. The sine wave excitation also provides optimal current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

The LCD also requires a bias supply for contrast control. The supply's output should be regulated, and variable over a considerable range.

The small size and battery powered operation associated with LCD equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is usually a priority. Laptop and hand held portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including PC board and all hardware, usually must fit within the LCD enclosure with a height restriction of 0.25".

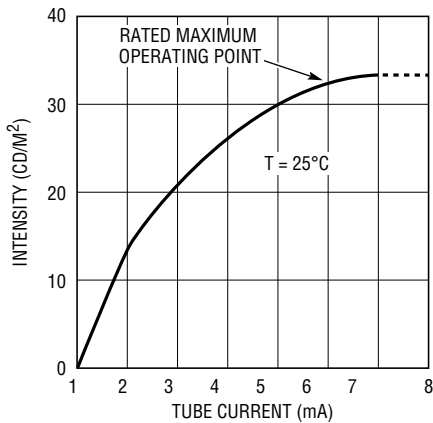
Cold Cathode Fluorescent Lamps (CCFLs)

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are complex transducers, with many variables affecting their ability to convert electrical current to light. Factors influencing conversion efficiency include the lamp's current, temperature, drive waveform characteristics, length, width, gas constituents and the proximity to nearby conductors.

These and other factors are interdependent, resulting in a complex overall response. Figures 1 through 4 show some typical characteristics. A review of these curves hints at the difficulty in predicting lamp behavior as operating conditions vary. The lamp's current and temperature are

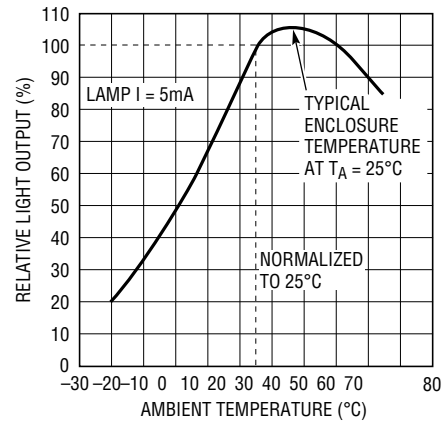
CCFL backlight application circuits contained in this Application Note are covered by U.S. patent number 5408162 and other patents pending.

Application Note 55



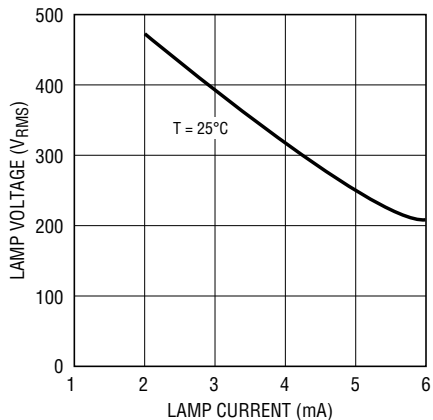
AN55 • TA01

Figure 1. Emissivity for a Typical 6mA Lamp. Curve Flattens Badly Above 6mA



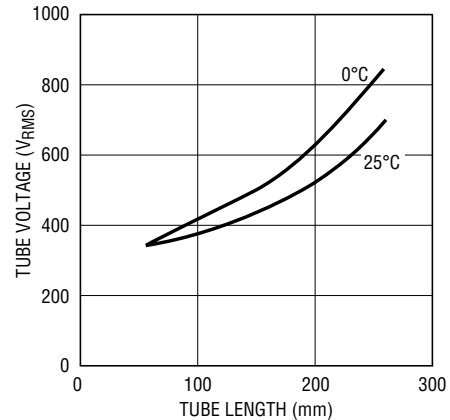
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Figure 2. Ambient Temperature Effects on Emissivity of a Typical 5mA Lamp. Lamp and Enclosure Must Come to Thermal Steady State Before Measurements are Made



AN55 • TA03

Figure 3. Current vs Voltage for a Lamp in the Operating Region



AN55 • TA04

Figure 4. Running Voltage vs Lamp Length at Two Temperatures. Start-Up Voltages are Usually 50% to 200% Higher Over Temperature

clearly critical to emission, although electrical efficiency may not necessarily correspond to the best optical efficiency point. Because of this, both electrical and photometric evaluation of a circuit is often required. It is possible, for example, to construct a CCFL circuit with 94% electrical efficiency which produces less light output than an approach with 80% electrical efficiency (see Appendix J, “A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas.” Similarly, the performance of a very well matched lamp-circuit combination can be severely degraded by a lossy display enclosure or excessive high voltage wire lengths. Display enclosures with too much conducting material near the lamp have huge losses due to capacitive coupling. A poorly designed display

enclosure can easily degrade efficiency by 20%. High voltage wire runs typically cause 1% loss per inch of wire.

CCFL Load Characteristics

These lamps are a difficult load to drive, particularly for a switching regulator. They have a “negative resistance” characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the start voltage is about 1000V, although higher and lower voltage lamps are common. Operating voltage is usually 300V to 400V, although other lamps may require different potentials. The lamps will operate from DC, but migration effects within the lamp will quickly damage it. As such, the waveform must be AC. No DC content should be present.

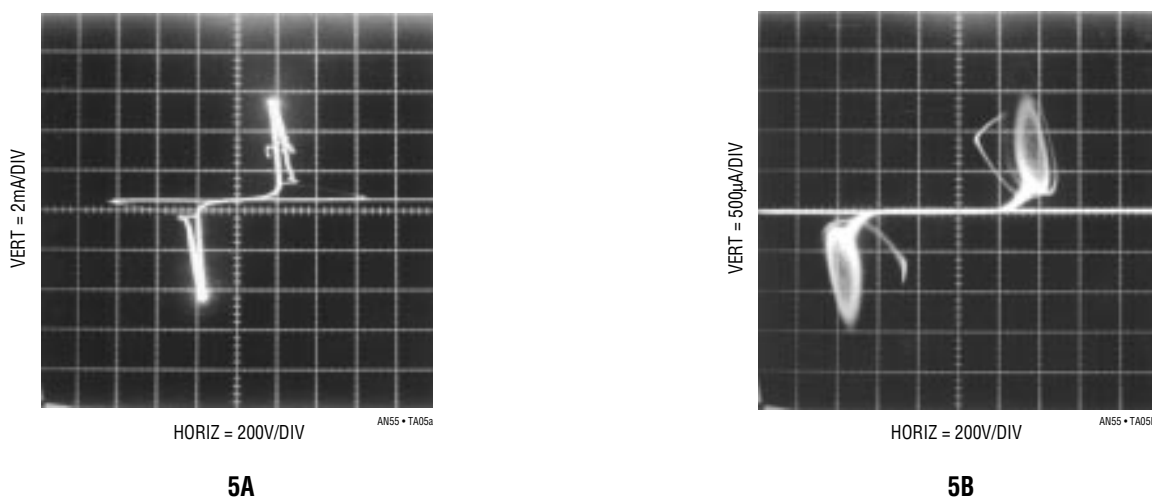


Figure 5. Negative Resistance Characteristic for Two CCFL Lamps. “Snap-Back” is Readily Apparent, Causing Oscillation in 5B. These Characteristics Complicate Power Supply Design

Figure 5A shows an AC driven lamp’s characteristics on a curve tracer. The negative resistance induced “snap-back” is apparent. In Figure 5B another lamp, acting against the curve tracer’s drive, produces oscillation. These tendencies, combined with the frequency compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on start-up. Once the lamp is in its operating region it assumes a linear load characteristic, easing stability criteria. Lamp operating frequencies are typically 20kHz to 100kHz and a sine-like waveform is preferred. The sine drive’s low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.¹ A further benefit to the continuous sine drive is its low crest factor and controlled rise times, which are easily handled by the CCFL. CCFL’s RMS current-to-light output efficiency is degraded by fast rise high crest factor drive waveforms.²

CCFL Power Supply Circuits

Figure 6’s circuit meets CCFL drive requirements. Efficiency is 88% with an input voltage range of 4.5V to 20V. This efficiency figure can be degraded by about 3% if the LT1172 V_{IN} pin is powered from the same supply as the main circuit V_{IN} terminal. Lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied the LT1172 switching regulator’s feedback pin is below the device’s internal 1.2V reference, causing full duty cycle modulation at the V_{SW} pin (Trace A, Figure 7). L2 conducts current (Trace B) which flows from

L1’s center tap, through the transistors, into L2. L2’s current is deposited in switched fashion to ground by the regulator’s action.

L1 and the transistors comprise a current driven Royer class converter³ which oscillates at a frequency primarily set by L1’s characteristics (including its load) and the 0.033 μ F capacitor. LT1172 driven L2 sets the magnitude of the Q1-Q2 tail current, hence L1’s drive level. The 1N5818 diode maintains L2’s current flow when the LT1172 is off. The LT1172’s 100kHz clock rate is asynchronous with respect to the push-pull converter’s (60kHz) rate, accounting for Trace B’s waveform thickening.

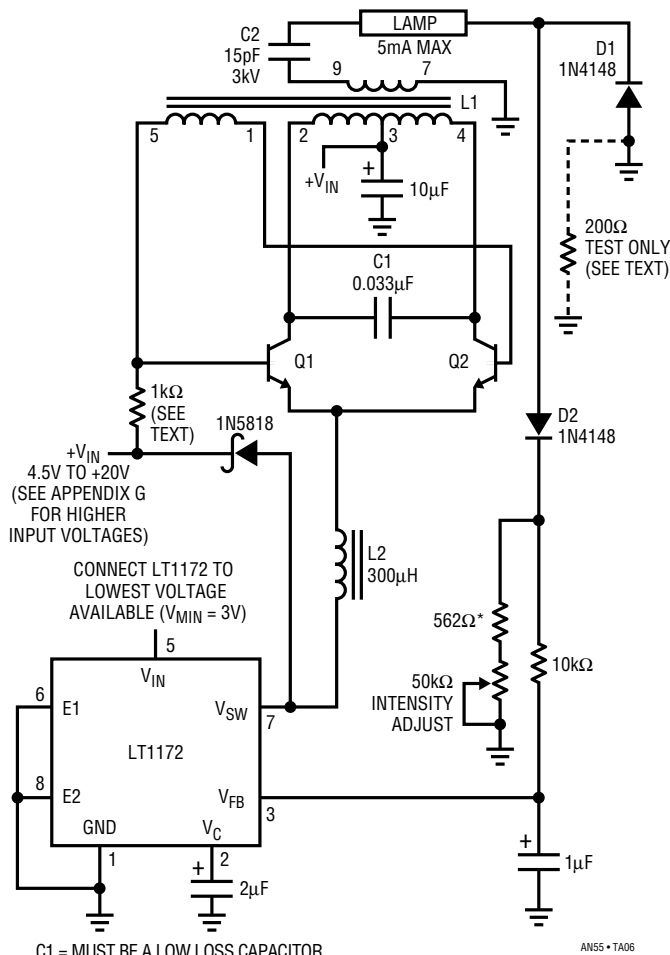
The 0.033 μ F capacitor combines with L1’s characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (Traces C and D respectively). L1 furnishes voltage step-up, and about 1400V_{P-P} appears at its secondary (Trace E). Current flows through the 15pF capacitor into the lamp. On negative waveform cycles the lamp’s current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562 Ω -50k potentiometer chain. The positive half-sine appearing across the resistors (Trace F) represents 1/2 the lamp

Note 1: Many of the characteristics of CCFLs are shared by so-called “Hot” cathode fluorescent lamps. See Appendix A, “Hot” Cathode Fluorescent Lamps.

Note 2: See Appendix J, “A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas.”

Note 3: See Appendix I, “Who Was Royer and What Did He Design?” See also reference 2.

Application Note 55



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS CTX300-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

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Figure 6. An 88% Efficiency Cold Cathode Fluorescent Lamp (CCFL) Power Supply

current. This signal is filtered by the 10k-1µF pair and presented to the LT1172's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1172's V_C pin provides stable loop compensation. The loop forces the LT1172 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0%-100% intensity control with no lamp dead zones or "pop-on" at low intensities.⁴ Additionally, lamp

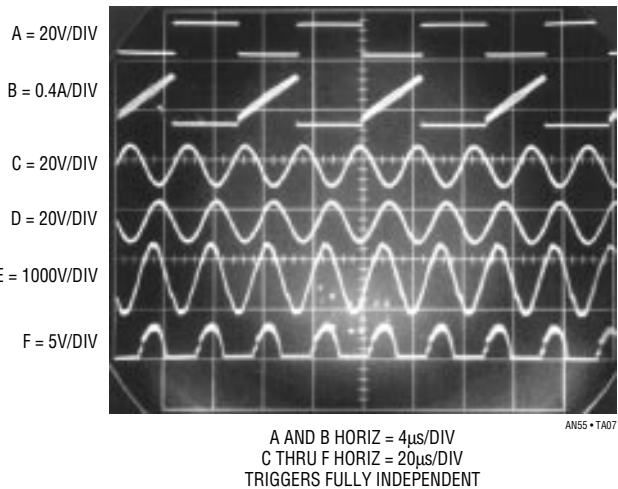


Figure 7. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B, and C through F

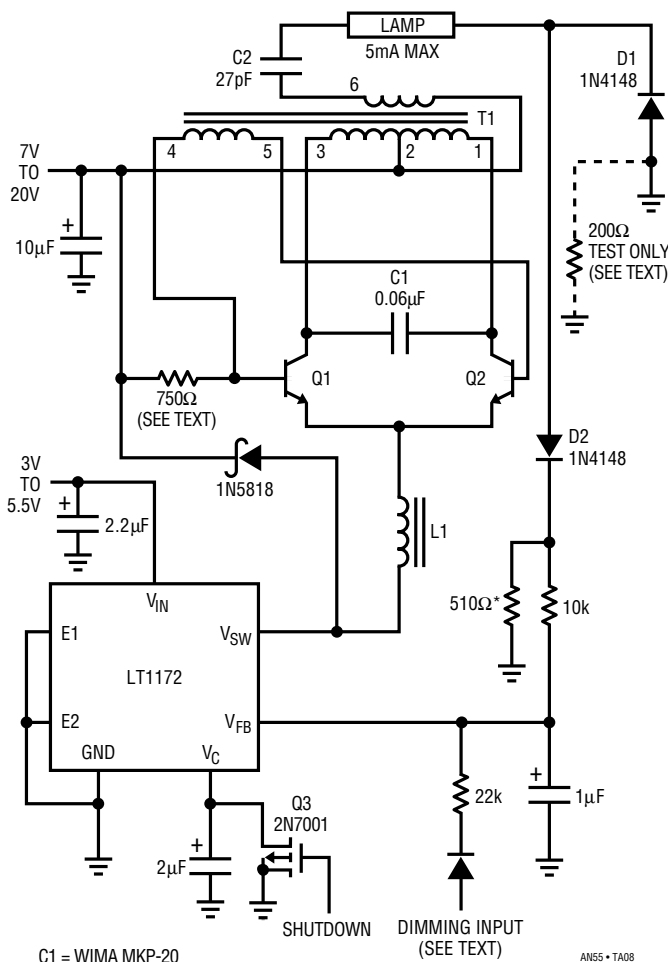
life is enhanced because current cannot increase as the lamp ages.

This circuit's 0.1% line regulation is notably better than some other approaches. This tight regulation prevents lamp intensity variation when abrupt line changes occur. This typically happens when battery powered apparatus is connected to an AC powered charger. The circuit's excellent line regulation derives from the fact that L1's drive waveform never changes shape as input voltage varies. This characteristic permits the simple 10kΩ-1µF RC to produce a consistent response. The RC averaging characteristic has serious error compared to a true RMS conversion, but the error is constant and "disappears" in the 562Ω shunt's value.

This circuit is similar to one previously described⁵ but its 88% efficiency is 6% higher. The efficiency improvement is primarily due to the transistor's higher gain and lower saturation voltage. The base drive resistor's value (nominally 1kΩ) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. A procedure for doing this is described in the following section, "General Measurement and Optimization Considerations."

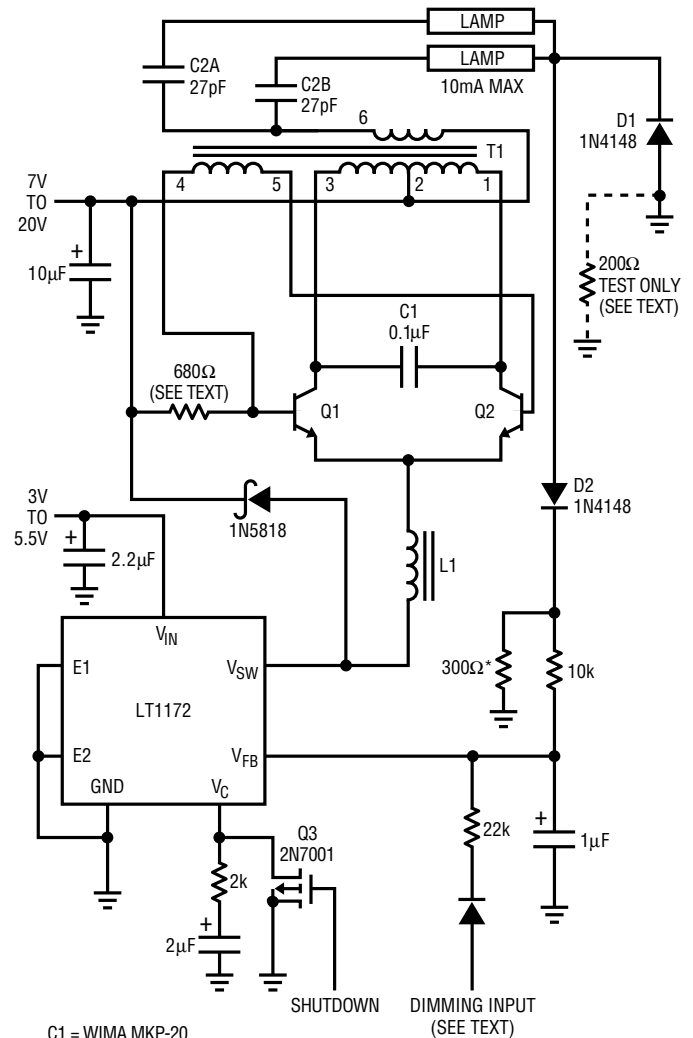
Note 4: Controlling a nonlinear load's current, instead of its voltage, permits applying this circuit technique to a wide variety of nominally evil loads. See Appendix H, "Related Circuits."

Note 5: See "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, Application Note 49, August 1992.



C1 = WIMA MKP-20
 L1 = COILTRONICS CTX150-4
 Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
 T1 = COILTRONICS CTX110600-1 OR SUMIDA EPS-207
 PIN NUMBERS SHOWN FOR COILTRONICS UNIT
 * = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS
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Figure 8. A 91% Efficient CCFL Supply for 5mA Loads Features Shutdown and Dimming Inputs



C1 = WIMA MKP-20
 L1 = COILTRONICS CTX150-4
 Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
 T1 = COILTRONICS CTX110600-1 OR SUMIDA EPS-207
 PIN NUMBERS SHOWN FOR COILTRONICS UNIT
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Figure 9. A 92% Efficient CCFL Supply for 10mA Loads Features Shutdown and Dimming Inputs. Two Lamps are Typical of Color Displays

Figure 8's circuit is similar, but uses a transformer with lower copper and core losses to increase efficiency to 91%. The trade-off is slightly larger transformer size. Value shifts in C1, L2 and the base drive resistor reflect different transformer characteristics. This circuit also features shutdown via Q3 and a DC or pulse width controlled dimming input. Appendix F, "Intensity Control and Shutdown Methods," details operation of these features. Figure 9, directly derived from Figure 8, produces 10mA output to drive color LCD's at 92% efficiency. The slight efficiency improvement comes from a reduction in LT1172 "housekeeping" current as a percentage of total current

drawn. Value changes in components are the result of higher power operation. The most significant change involves driving two lamps. Accommodating two lamps involves separate ballast capacitors but circuit operation is similar. Two lamp designs reflect slightly different loading back through the transformer's primary. C2 usually ends up in the 10pF to 47pF range. Note that C2A and B appear with their lamp loads in parallel across the transformer's secondary. As such, C2's value is often smaller than in a single lamp circuit using the same type lamp. Ideally the

Application Note 55

transformer's secondary current splits evenly between the C2-lamp branches, with the total load current being regulated. In practice, differences between C2A and B and differences in lamps and lamp wiring layout preclude a perfect current split. Practically, these differences are small, and the lamps appear to emit equal amounts of light. Layout and lamp matching can influence C2's value. Some techniques for dealing with these issues appear in the text section, "Layout Issues."

General Measurement and Optimization Considerations

Several points should be kept in mind when observing operation of these circuits. L1's high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*⁶ Tektronix probe types P-6007 and P-6009 (acceptable in some cases) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1172's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 7 was obtained using a dual beam oscilloscope (Tektronix 556). LT1172 related Traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Obtaining and verifying high efficiency⁷ requires some amount of diligence. The optimum efficiency values given for C1 and C2 are typical, and will vary for specific types of lamps. An important realization is that the term "lamp" includes the *total* load seen by the transformer's secondary. This load, reflected back to the primary, sets transformer input impedance. The transformer's input impedance forms an integral part of the LC tank that produces the high voltage drive. Because of this, circuit efficiency must be optimized with the wiring, display housing and physical layout arranged *exactly* the same way they will be built in production. Deviations from this procedure will result in

lower efficiency than might otherwise be possible. In practice, a "first cut" efficiency optimization with "best guess" lead lengths and the intended lamp in its display housing usually produces results within 5% of the achievable figure. Final values for C1 and C2 may be established when the physical layout to be used in production has been decided on. C1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristic. C2 ballasts the lamp, effectively buffering its negative resistance characteristic. Small values of C2 provide the most load isolation, but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage, but degrade load buffering. Also, C1's "best" value is somewhat dependent on the lamp type used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but generalized guidelines are possible. Typical values for C1 are 0.01 μ F to 0.15 μ F. C2 usually ends up in the 10pF to 47pF range. C1 *must* be a low loss capacitor and substitution of the recommended devices is not recommended. A poor quality dielectric for C1 can easily degrade efficiency by 10%. Before capacitor selection the Q1-Q2 base drive resistor should be set to a value which insures saturation, e.g., 470 Ω . Next, C1 and C2 are selected by trying different values for each and iterating towards best efficiency. During this procedure insure that loop closure is maintained by monitoring the LT1172's feedback pin, which should be at 1.23V. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q1, Q2 and the output. Finally, the base drive resistor's value should be optimized.

Note 6: Don't say we didn't warn you!

Note 7: The term "efficiency" as used here applies to electrical efficiency. In fact, the ultimate concern centers around the efficient conversion of power supply energy into light. Unfortunately, lamp types show considerable deviation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life and history of any particular lamp. As such, this publication treats "efficiency" on an electrical basis; the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp has been selected the ratio of primary supply power to lamp emitted light energy may be measured with the aid of a photometer. This is covered in Appendix D, "Photometric Measurement." See also Appendix K, "Perspectives on Efficiency."

The base drive resistor's value (nominally $1\text{k}\Omega$) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. This point may be established for any lamp type by determining the peak collector current at full lamp power.

The base resistor should be set at the largest value that ensures saturation for worst case transistor beta. This condition may be verified by varying the base drive resistor about the ideal value and noting small variations in input supply current. The minimum obtainable current corresponds to the best beta vs saturation trade-off. In practice, supply current rises slightly on either side of this point. This "double value" behavior is due to efficiency degradation being caused by either excessive base drive or saturation losses.

Other issues influencing efficiency include lamp wire length and energy leakage from the lamp. The high voltage side of the lamp should have the smallest practical lead length. Excessive length results in radiative losses which can easily reach 3% for a 3 inch wire. Similarly, no metal should contact or be in close proximity to the lamp. This prevents energy leakage which can exceed 10%.⁸

It is worth noting that a custom designed lamp affords the best possible results. A jointly tailored lamp-circuit combination permits precise optimization of circuit operation, yielding highest efficiency.

These considerations should be made with knowledge of other LCD issues. See Appendix B, "Mechanical Design Considerations for Liquid Crystal Displays." This section was guest written by Charles L. Guthrie of Sharp Electronics Corporation.

Special attention should be given to the layout of the circuit board since high voltage is generated at the output. The output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination build-up can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. It is good practice for minimization of leakage to break the silk screen line which outlines transformer T1. This prevents leakage

from the high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk screen ink for its ability to withstand high voltages.

Efficiency Measurement

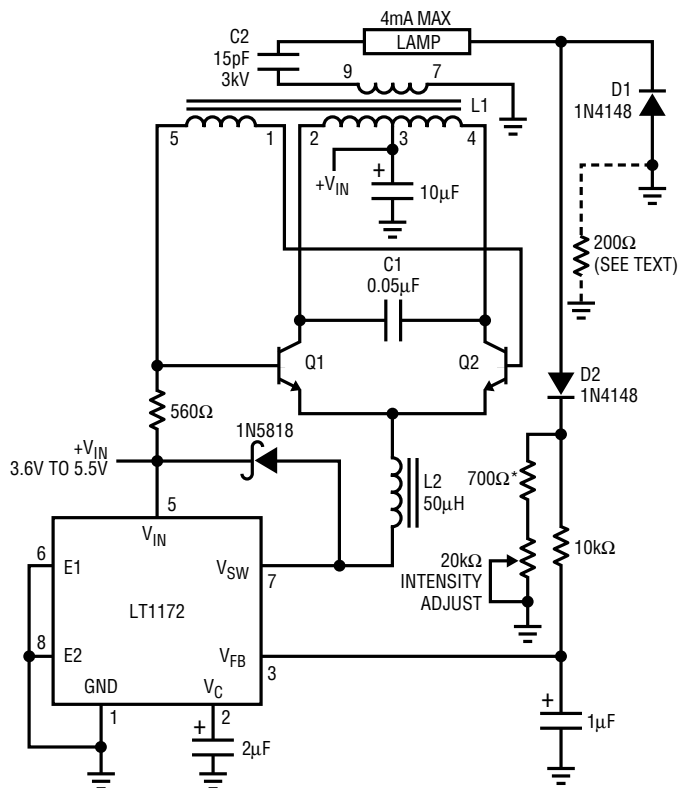
Once these procedures have been followed efficiency can be measured. Efficiency may be measured by determining lamp current and voltage. Measuring current involves measuring RMS voltage across a temporarily inserted 200Ω , 0.1% resistor in the ground lead of the negative current steering diode. The lamp current is: $I_{LAMP} = E_{RMS}/200\Omega \times 2$. The $\times 2$ factor is necessitated because the diode steering dumps the current to ground on negative cycles. The 200Ω value allows the RMS meter to read with a scale factor numerically identical to the total current. Once this measurement is complete the 200Ω resistor may be deleted and the negative current steering diode again returned directly to ground. Lamp RMS voltage is measured at the lamp with a properly compensated high voltage probe. Multiplying these two results gives power in watts, which may be compared to the DC input supply(s) $E \times I$ product(s). In practice, the lamp's current and voltage contain small out of phase components but their error contribution is negligible.

Both the current and voltage measurements require a wideband True RMS voltmeter. The meter must employ a thermal type RMS converter—the more common logarithmic computing type based instruments are inappropriate because their bandwidth is too low.

The previously recommended high voltage probes are designed to see a $1\text{M}\Omega$ - 10pF - 22pF oscilloscope input. The RMS voltmeters have a $10\text{M}\Omega$ input. This difference necessitates an impedance matching network between the probe and the voltmeter. Details on this and other efficiency measurement issues appear in Appendix C, "Achieving Meaningful Efficiency Measurements."

Note 8: A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the lamp at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb-forefinger combination towards the high voltage (higher field intensity) lamp end produces progressively greater input currents. Don't touch the high voltage lead or you may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.

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- L2 = COILTRONICS CTX50-4
- Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
- * = 1% FILM RESISTOR
- DO NOT SUBSTITUTE COMPONENTS**

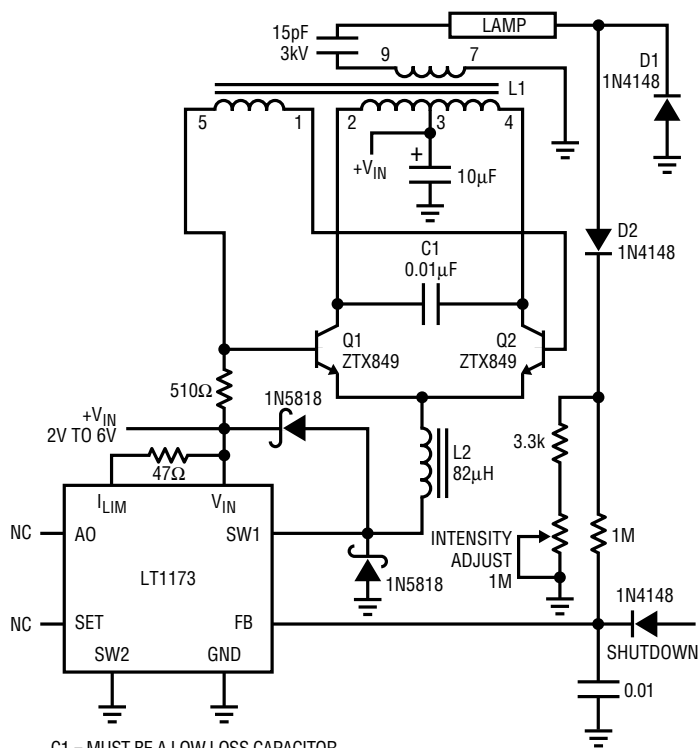
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Figure 10. A 4mA Design Intended for Low Voltage Operation. L1's Modified Turns Ratio Allows Operation Down to 3.6V

Low Power CCFL Supplies

Many applications require relatively low power CCFL backlighting. Figure 10's variation, optimized for low voltage inputs, produces 4mA output. Circuit operation is similar to the previous examples. The fundamental difference is L1's higher turns ratio, which accommodates the reduced available drive voltage. The circuit values given are typical, although some variation occurs with various lamps and layouts.

Figure 11's design, the so-called "dim backlight," is optimized for single lamp operation at very low currents. The circuit is meant for use at low input voltages, typically 2V to 6V with a 1mA maximum lamp current. This circuit maintains control down to lamp currents of 1μA, a very



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- PIN NUMBERS SHOWN FOR COILTRONICS UNIT
- L2 = TOKO 262LYF-0091K
(408) 432-8251
- DO NOT SUBSTITUTE COMPONENTS**

Figure 11. Low Power CCFL Power Supply. Circuit Controls Lamp Current Over a 1μA to 1mA Range

dim light! It is intended for applications where the longest possible battery life is desired. Primary supply drain ranges from hundreds of microamperes to 100mA with lamp currents of microamps to 1mA. In shutdown the circuit pulls only 100μA. Maintaining high efficiency at low lamp currents requires modifying the basic design.

Achieving high efficiency at low operating current requires lowering quiescent power drain. To do this the LT1172, a pulse width modulator based device, is replaced with an LT1173. The LT1173 is a Burst Mode™ operation regulator. When this device's feedback pin is too low it delivers a burst of output current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground referred diode at the V_{SW} pin prevents substrate turn-on due to excessive L2 ring-off.

Burst Mode is a trademark of Linear Technology Corporation.

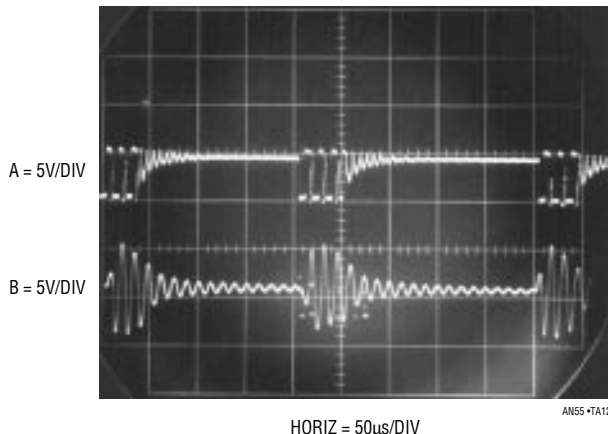


Figure 12. Waveforms for the Low Power CCFL Power Supply. LT1173 Burst Type Regulator (Trace A) Periodically Excites the Resonant High Voltage Converter (Q1 Collector is Trace B)

During the off periods the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, the other circuit's LT1172 pulse width modulator type regulator maintains "housekeeping" current between cycles. This results in more available output power but higher quiescent currents.

Figure 12 shows operating waveforms. When the regulator comes on (Trace A, Figure 12) it delivers bursts of output current to the L1-Q1-Q2 high voltage converter. The converter responds with bursts of ringing at its resonant frequency.⁹ The circuit's loop operation is similar to the previous designs except that L1's drive waveform varies with supply. Because of this, line regulation suffers and the circuit is not recommended for wide ranging inputs.

Some lamps may display non-uniform light emission at very low excitation currents. See the text section, "Extending Illumination Range."

Note 9: The discontinuous energy delivery to the loop causes substantial jitter in the burst repetition rate, although the high voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" mode region of most oscilloscopes, precluding a detailed display. "Alternate" mode operation causes waveform phasing errors, producing an inaccurate display. As such, waveform observation requires special techniques. Figure 12 was taken with a dual beam instrument (Tektronix 556) with both beams slaved to one time base. Single sweep triggering eliminated jitter artifacts. Most oscilloscopes, whether analog or digital, will have trouble reproducing this display.

LCD Bias Supplies

LCDs also require a bias supply for contrast control. The supply's variable output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. The logic sections of display drivers operate from single 5V supplies, but the actual driver outputs swing between +5V and a negative bias potential. Varying this bias causes the display contrast to vary.

An LCD bias generator, developed by Steve Pietkiewicz of LTC, is shown in Figure 13. In this circuit U1 is an LT1173 micropower DC to DC converter. The 3V input is converted to +24V by U1's switch, L2, D1, and C1. The switch pin (SW1) also drives a charge pump composed of C2, C3, D2, and D3 to generate -24V. Line regulation is less than 0.2% from 3.3V to 2V inputs. Load regulation, although suffering somewhat since the -24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2V input at 75% efficiency.

If greater output power is required, Figure 13's circuit can be driven from a +5V source. R1 should be changed to 47Ω and C3 to 47µF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing D4's anode to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage.

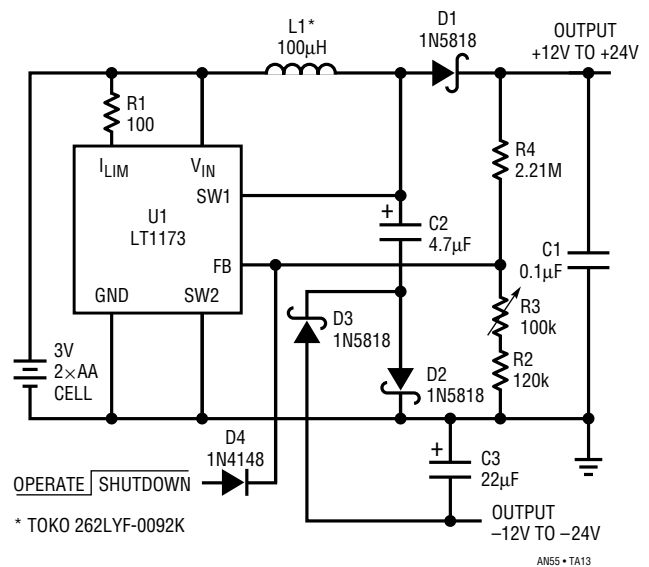


Figure 13. DC to DC Converter Generates LCD Bias

Application Note 55

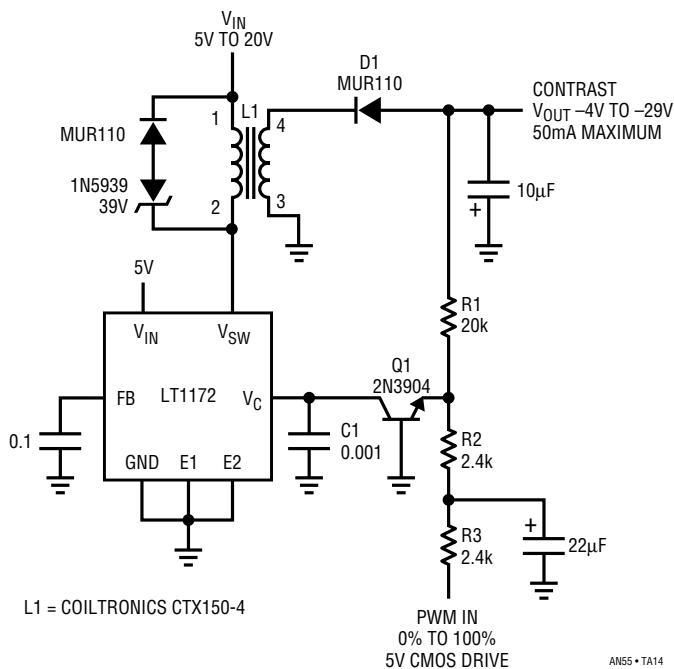


Figure 14. A Transformer Based LCD Contrast Supply. Q1 Level Shifts the Feedback Signal and Functions as a Reference Amplifier

Shutdown current is $110\mu\text{A}$ from the input source and $36\mu\text{A}$ from the shutdown signal.

Figure 14 is a transformer based approach to generating LCD bias. The LT1172 drives L1, producing negative flyback events at pin 4. D1 rectifies these events, producing a negative DC output. The R1-R2-R3 string sets feedback at Q1's emitter. Q1, acting as a reference amplifier, biases the LT1172, closing a control loop. C1 provides frequency compensation, stabilizing the loop. In this case, a pulse width modulated signal biases the feedback string, setting operating point and contrast. A 0V to 5V DC signal could also be used. The use of Q1's V_{BE} as a reference introduces a $-0.3\%/^{\circ}\text{C}$ temperature coefficient, but this is not deleterious to system operation. Maximum output current is 50mA and efficiency measures about 82%.

Dual Output LCD Bias Voltage Generator

The many different kinds of LCD displays available make programming LCD bias voltage at the time of manufacture attractive. Figure 15's circuit, developed by Jon Dutra of

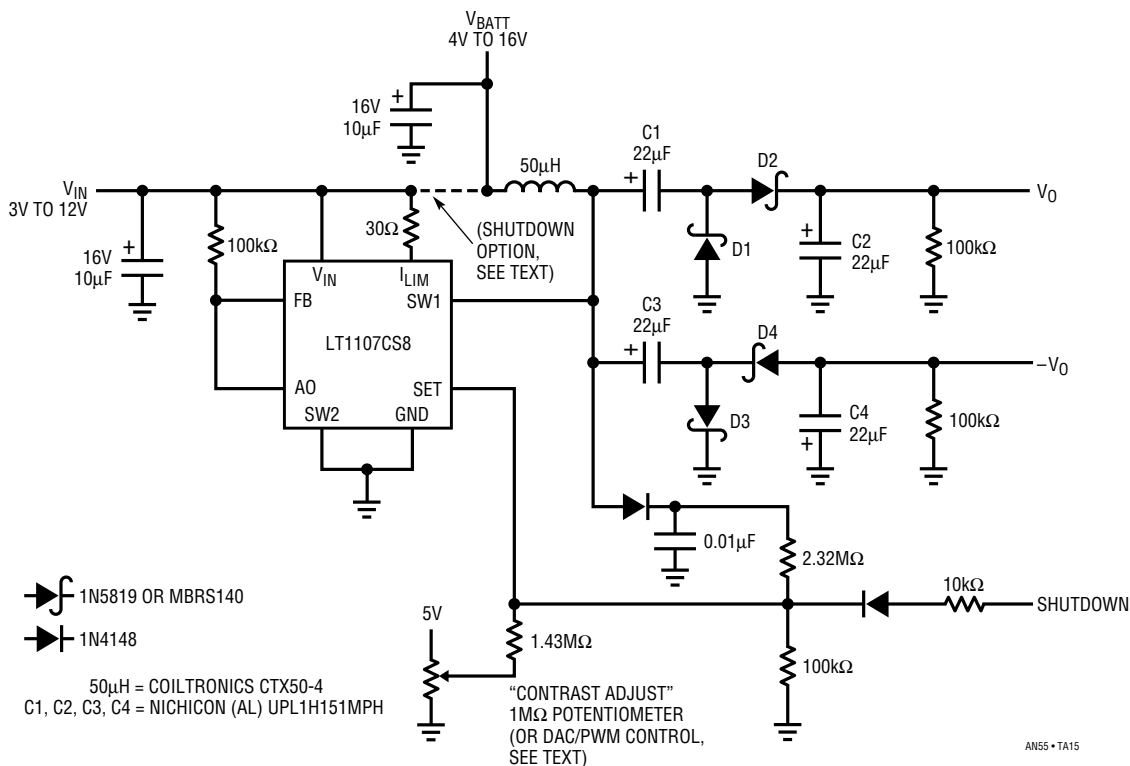


Figure 15. Dual Output LCD Bias Voltage Generator

LTC is an AC coupled boost topology. The feedback signal is derived separately from the outputs, so loading does not affect loop compensation, although load regulation is somewhat compromised. With 28V out, from 10% to 100% load (4mA to 40mA), the output voltage sags about 0.65V. From 1mA to 40mA load the output voltage drops about 1.4V. This is acceptable for most displays.

Output noise is reduced by using the auxiliary gain block within the LT1107 (see LT1107 data sheet) in the feedback path. This added gain effectively reduces comparator hysteresis and tends to randomize output noise. Output noise is below 30mV over the output load range. Output power increases with V_{BATT} , from about 1.4W with 5V in to about 2W with 8V or more. Efficiency is 80% over a broad output power range. If only a positive or negative output voltage is required, the diodes and capacitors associated with the unused output can be eliminated. The 100k Ω resistor is required on each output to load a parasitic voltage doubler created by D2-D4 shunt capacitance. Without this minimum load, the output voltage can rise to unacceptable levels.

The voltage at the switch pin (SW1) swings from 0V to V_{OUT} plus 2 diode drops. This voltage is AC coupled to the positive output through C1 and D1, and to the negative output through C3 and D3. C1 and C3 have the full RMS output current flowing through them. Most tantalum capacitors are not rated for current flow. Use of a rated tantalum or electrolytic is recommended for reliability. At lower output currents monolithic ceramics are also an option.

The circuit may be shut down in several ways. The easiest is to pull the set pin above 1.25V. This approach consumes 200 μ A in shutdown. A lower power method is to turn off V_{IN} to the LT1107 by a high side switch or simply disable the input supply (see option in schematic). This drops quiescent current from the V_{BATT} input below 10 μ A. In both cases V_{OUT} drops to zero volts. In the event $+V_{OUT}$ does not need to drop to zero, C1 and D1 can be eliminated. The output voltage can be adjusted from any voltage above V_{BATT} to 46V. Output voltage can be controlled by the user with DAC, PWM or potentiometer control. Summing currents into the feedback node allows downward adjustment of output voltage.

Layout

The physical layout of the lamp, its leads, the display housing and other high voltage components is an integral part of the circuit. Poor layout can easily degrade efficiency by 25%, and higher layout induced losses have been observed. Producing an optimal layout requires attention to how losses occur. Figure 16 begins our study by examining potential parasitic paths between the transformer's output and the lamp. Parasitic capacitance to AC ground from any point between the transformer output and the lamp creates a path for undesired current flow. Similarly, stray coupling from any point along the lamp's length to AC ground induces parasitic current flow. All parasitic current flow is wasted, causing the circuit to produce more energy to maintain the desired current flow

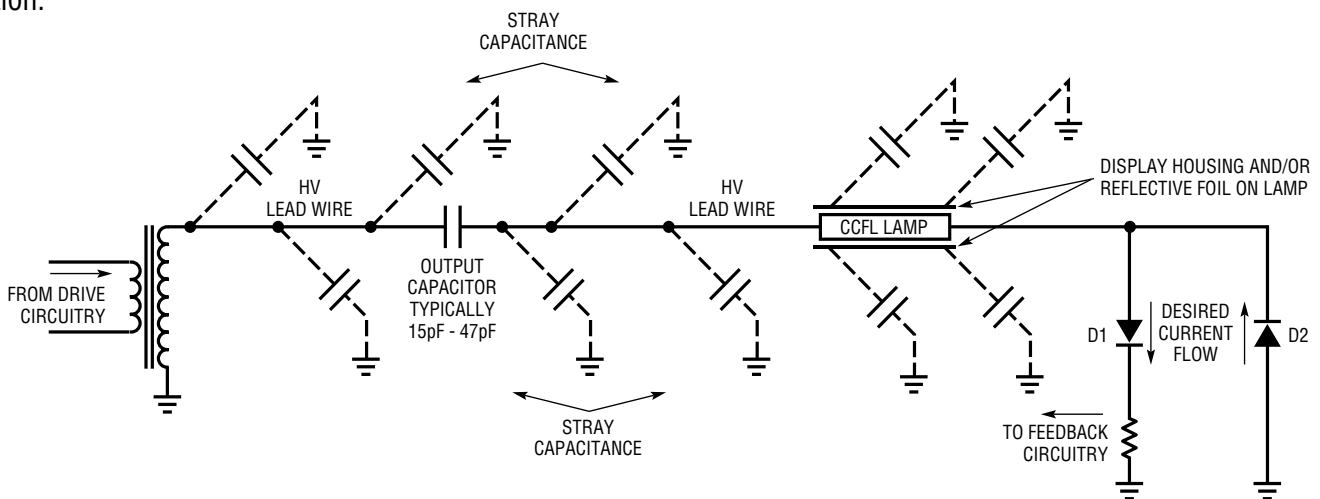


Figure 16. Loss Paths Due to Stray Capacitance in a Practical LCD Installation. Minimizing these Paths is Essential for Good Efficiency

AN55-1A16

Application Note 55

in D1 and D2. The high voltage path from the transformer to the display housing should be as short as possible to minimize losses. A good rule of thumb is to assume 1% efficiency loss per inch of high voltage lead. Any PC board ground or power planes should be relieved by at least 1/4" in the high voltage area. This not only prevents losses, but eliminates arcing paths.

Parasitic losses associated with lamp placement within the display housing require attention. High voltage wire length within the housing must be minimized, particularly for displays using metal construction. Insure that the high voltage is applied to the shortest wire(s) in the display. This may require disassembling the display to verify wire length and layout. Another loss source is the reflective foil commonly used around lamps to direct light into the actual LCD. Some foil materials absorb considerably more field energy than others, creating loss. Finally, displays supplied in metal enclosures tend to be lossy. The metal absorbs significant energy and an AC path to ground is unavoidable. Direct grounding of a metal enclosed display further increases losses. Some display manufacturers

have addressed this issue by relieving the metal in the lamp area with other materials.

The highest efficiency “in system” backlights have been produced by careful attention to these issues. In some cases the entire display enclosure was re-engineered for lowest losses.

Layout Considerations for Two Lamp Designs

Systems using two lamps have some unique layout problems. Almost all two lamp displays are color units. The lower light transmission characteristics of color displays necessitates more light. As such, display manufacturers use two lamps to produce more light. The wiring layout of these two lamp color displays affects efficiency and illumination balance in the lamps. Figure 17 shows an “x-ray” view of a typical display. This symmetrical arrangement presents equal parasitic losses. If C1 and C2 and the lamps are matched, the circuit’s current output splits evenly and equal illumination occurs.

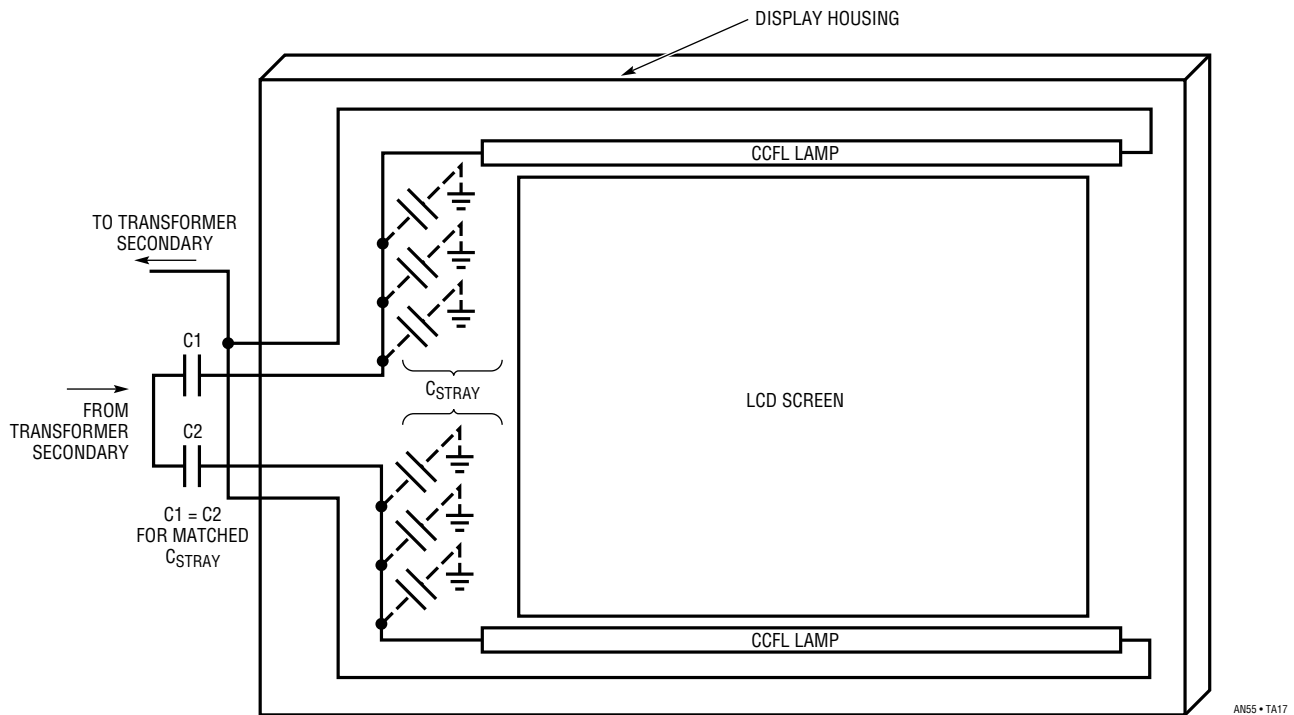


Figure 17. Loss Paths for a “Best Case” Dual Lamp Display. Symmetry Promotes Balanced Illumination

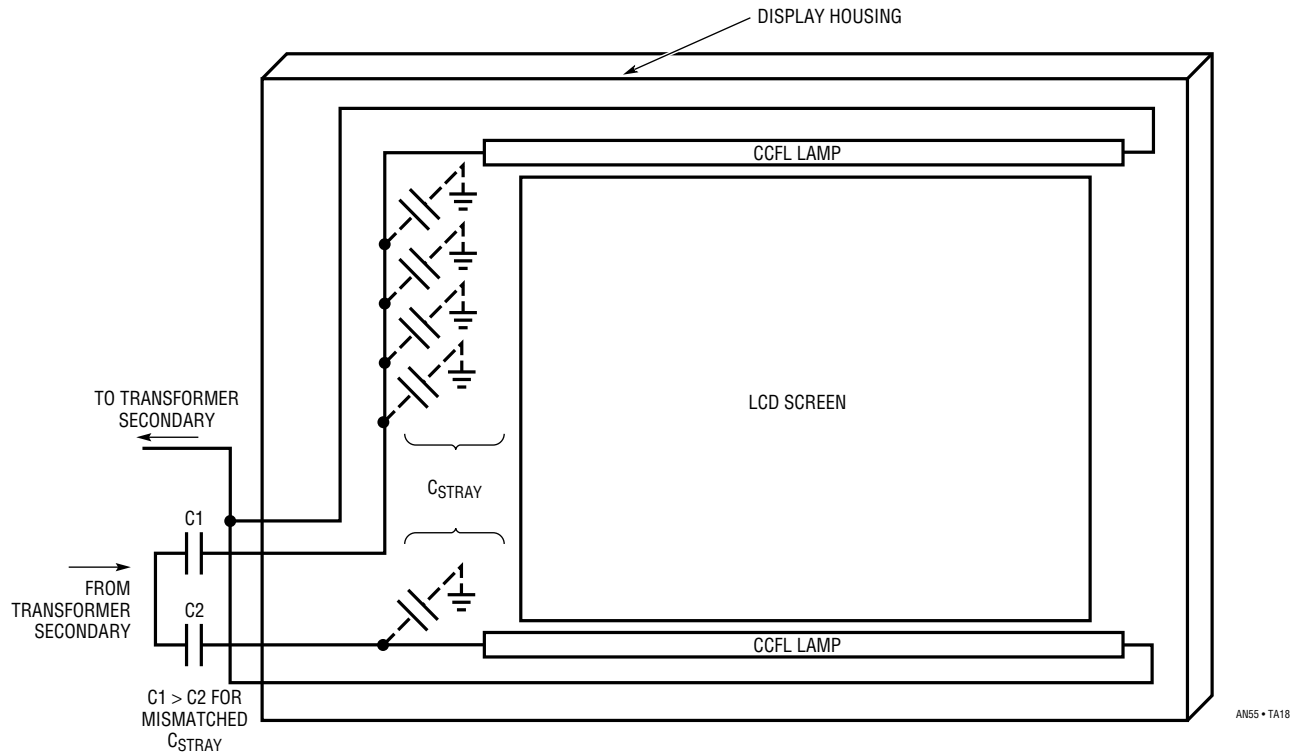


Figure 18. Asymmetric Losses in a Dual Lamp Display. Skewing C1 and C2 Values Compensates Imbalanced Loss Paths, but Not Wasted Energy

Figure 18's display arrangement is less friendly. The asymmetrical wiring forces unequal losses, and the lamps receive imbalanced current. Even with identical lamps, illumination may not be balanced. This condition is correctable by skewing C1 and C2's values. C1, because it drives greater parasitic capacitance, should be larger than C2. This tends to equalize the currents, promoting equal lamp drive. It is important to realize that this compensation does nothing to recapture the lost energy—efficiency is still compromised. There is no substitute for minimizing loss paths.

In general, imbalanced illumination causes fewer problems than might be supposed. The effect is very difficult for the eye to detect at high intensity levels. Unequal illumination is much more noticeable at lower levels. In the worst case the dimmer lamp may only partially illuminate. This phenomenon, sometimes called "Thermomentering," is discussed in detail in the text section "Extending Illumination Range."

Feedback Loop Stability Issues

The circuits shown to this point rely on closed loop feedback to maintain the operating point. All linear closed loop systems require some form of frequency compensation to achieve dynamic stability. Circuits operating with relatively low power lamps may be frequency compensated by simply overdamping the loop. Text Figures 6, 8 and 10 use this approach. The higher power operation associated with color displays requires more attention to loop response. The transformer produces much higher output voltages, particularly at start-up. Poor loop damping can allow transformer voltage ratings to be exceeded, causing arcing and failure. As such, higher power designs may require optimization of transient response characteristics.

Figure 19 shows the significant contributors to loop transmission in these circuits. The resonant Royer converter delivers information at about 50kHz to the lamp. This

Application Note 55

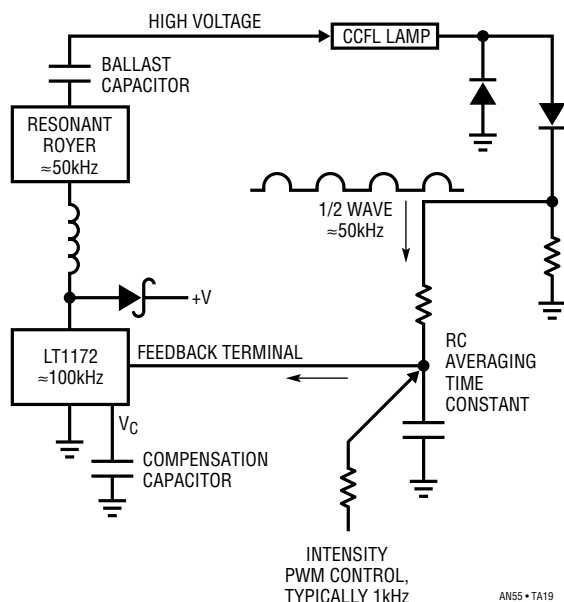


Figure 19. Delay Terms in the Feedback Path. The RC Time Constant Dominates Loop Transmission Delay and must be Compensated for Stable Operation

information is smoothed by the RC averaging time constant and delivered to the LT1172's feedback terminal as DC. The LT1172 controls the Royer converter at a 100kHz rate, closing the control loop. The capacitor at the LT1172 rolls off gain, nominally stabilizing the loop. This compensation capacitor must roll off the gain bandwidth at a low enough value to prevent the various loop delays from causing oscillation.

Which of these delays is the most significant? From a stability viewpoint the LT1172's output repetition rate and the Royer's oscillation frequency are sampled data systems. Their information delivery rate is far above the RC averaging time constants delay and is not significant. The RC time constant is the major contributor to loop delay. This time constant must be large enough to turn the half wave rectified waveform into DC. It also must be large enough to average any intensity control PWM signal to DC. Typically, these PWM intensity control signals come in at a 1kHz rate (see Appendix F, "Intensity Control and Shutdown Methods"). The RC's resultant delay dominates loop transmission. It must be compensated by the capacitor at the LT1172. A large enough value for this capacitor rolls off loop gain at low enough frequency to provide stability. The loop simply does not have enough gain to oscillate at a frequency commensurate with the RC delay.¹⁰

This form of compensation is simple and effective. It ensures stability over a wide range of operating conditions. It does, however, have poorly damped response at system turn-on. At turn-on the RC lag delays feedback, allowing output excursions well above the normal operating point. When the RC acquires the feedback value the loop stabilizes properly. This turn-on overshoot is not a concern if it is well within transformer breakdown ratings. Color displays, running at higher power, usually require large initial voltages. If loop damping is poor, the overshoot may be dangerously high. Figure 20 shows such a loop responding to turn-on. In this case the RC values are 10k and 4.7μF, with a 2μF compensation capacitor. Turn-on overshoot exceeds 3500V for over 10ms! Ring-off takes over 100ms before settling occurs. Additionally, an inadequate (too small) ballast capacitor and excessively lossy layout force a 2000V output once loop settling occurs. This photo was taken with a transformer rated well below this figure. The resultant arcing caused transformer destruction, resulting in field failures. A typical destroyed transformer appears in Figure 21.

Figure 22 shows the same circuit, with the RC values reduced to 10k and 1μF. The ballast capacitor and layout have also been optimized. Figure 22 shows peak voltage

Note 10: The high priests of feedback refer to this as "Dominant Pole Compensation." The rest of us are reduced to more pedestrian descriptives.

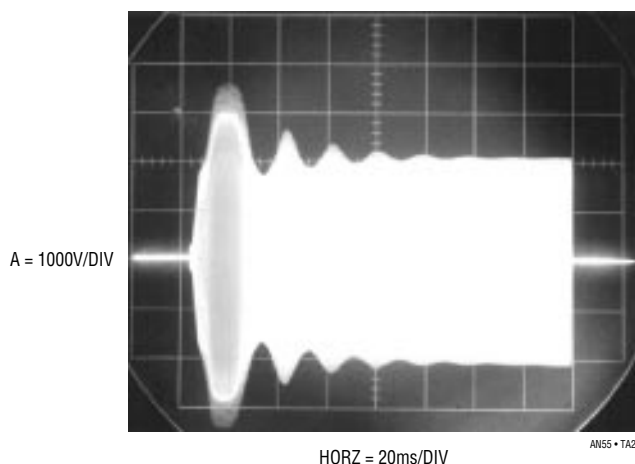
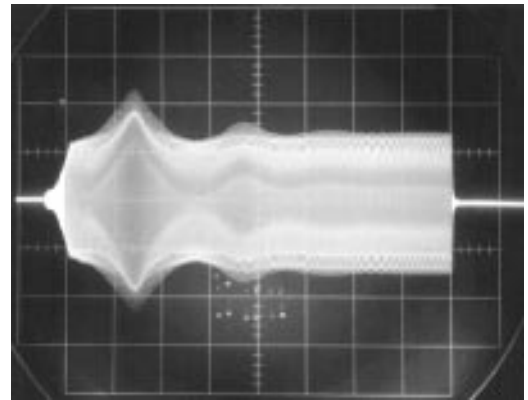


Figure 20. Destructive High Voltage Overshoot and Ring-Off Due to Poor Loop Compensation. Transformer Failure and Field Recall are Nearly Certain. Job Loss may also Occur



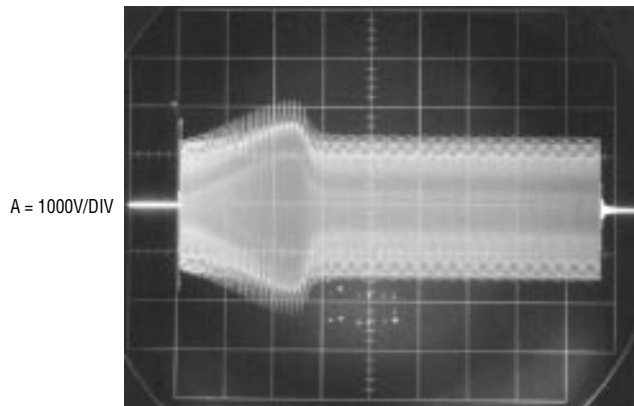
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Figure 21. Poor Loop Compensation Caused this Transformer Failure. Arc Occured in High Voltage Secondary (Lower Right). Resultant Shorted Turns Caused Overheating



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Figure 22. Reducing RC Time Constant Improves Transient Response, although Peaking, Ring-Off and Run Voltage are Still Excessive

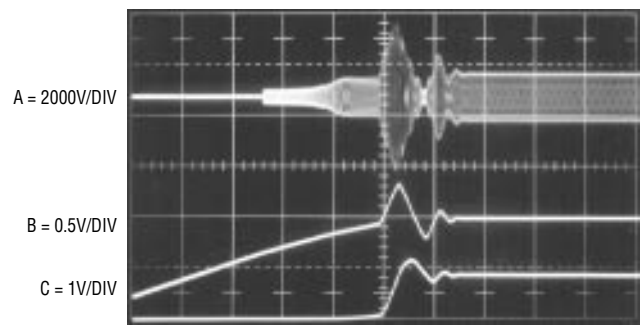


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Figure 23. Additional Optimization of RC Time Constant and Compensation Capacitor Reduces Turn-On Transient. Run Voltage is Large, Indicating Possible Lossy Layout and Display

reduced to 2.2kV with duration down to about 2ms (note horizontal scale change). Ring-off is also much quicker, with lower amplitude excursion. Increased ballast capacitor value and wiring layout optimization reduce running voltage to 1300V. Figure 23's results are even better. Changing the compensation capacitor to a 3k Ω -2 μ F network introduces a leading response into the loop, allowing faster acquisition. Now, turn-on excursion is slightly lower, but greatly reduced in duration (again, note horizontal scale change). The running voltage remains the same.

The photos show that changes in compensation, ballast value and layout result in dramatic reductions in overshoot amplitude and duration. Figure 20's performance almost



AN55 • TA24

Figure 24. Waveforms for a Lower Loss Layout and Display. High Voltage Overshoot (Trace A) is Reflected at Compensation Node (Trace B) and Feedback Pin (Trace C)

guarantees field failures, while Figures 22 and 23 do not overstress the transformer. Even with the improvements, more margin is possible if display losses can be controlled. Figures 20-23 were taken with an exceptionally lossy display. The metal enclosure was very close to the metallic foil wrapped lamps, causing large losses with subsequent high turn-on and running voltages. If the display is selected for lower losses, performance can be greatly improved.

Figure 24 shows a low loss display responding to turn-on with a 2 μ F compensation capacitor and 10k-1 μ F RC values. Trace A is the transformer's output while Traces B and C are the LT1172's $V_{Compensation}$ and feedback pins, respectively. The output overshoots and rings badly,

Application Note 55

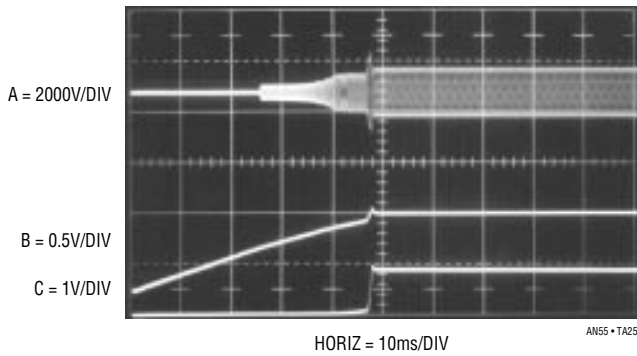


Figure 25. Reducing RC Time Constant Produces Quick, Clean Loop Behavior. Low Loss Layout and Display Result in 650V_{RMS} Running Voltage

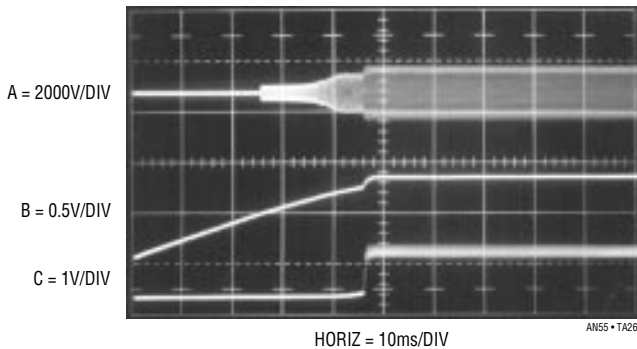


Figure 26. Very Low RC Value Provides Even Faster Response, but Ripple at Feedback Pin (Trace C) is too High. Figure 25 is the Best Compromise

peaking to about 3000V. This activity is reflected by overshoots at the $V_{\text{Compensation}}$ pin (the LT1172’s error amplifier output) and the feedback pin. In Figure 25 the RC is reduced to 10k Ω -0.1 μ F. This substantially reduces loop delay. Overshoot goes down to only 800V—a reduction of almost a factor of four. Duration is also much shorter. The $V_{\text{Compensation}}$ and feedback pins reflect this tighter control. Damping is much better, with slight overshoot induced at turn-on. Further reduction of the RC to 10k-0.01 μ F (Figure 26) results in even faster loop capture, but a new problem appears. In Trace A lamp turn on is so fast the overshoot does not register in the photo. The $V_{\text{Compensation}}$ (Trace B) and feedback nodes (Trace C) reflect this with exceptionally fast response. Unfortunately, the RC’s light filtering causes ripple to appear when the feedback node settles. As such, Figure 25’s RC values are probably more realistic for this situation.

The lesson from this exercise is clear. The higher voltages involved in color displays mandate attention to transformer outputs. Under running conditions layout and display losses can cause higher loop compliance voltages, degrading efficiency and stressing the transformer. At turn-on improper compensation causes huge overshoots, resulting in possible transformer destruction. Isn’t a day of loop and layout optimization worth a field recall?

Extending Illumination Range

Lamps operating at relatively low currents may display the “thermometer effect,” that is, light intensity may be non-uniformly distributed along lamp length. Figure 27 shows that although lamp current density is uniform, the associated field is imbalanced. The field’s low intensity, combined with its imbalance, means that there is not enough energy to maintain uniform phosphor glow beyond some point. Lamps displaying the thermometer effect emit most of their light near the positive electrode, with rapid emission fall-off as distance from the electrode increases. Placing a conductor along the lamp’s length largely alleviates “thermometering.” The trade-off is decreased efficiency due to energy leakage (see footnote 8 and associated text). It is worth noting that various lamp types have different degrees of susceptibility to the thermometer effect.

Some displays require extended illumination range. “Thermometering” usually limits the lowest practical illumination level. One acceptable way to minimize “thermometering” is to eliminate the large field imbalance. Figure 28’s circuit does this. This circuit’s most significant

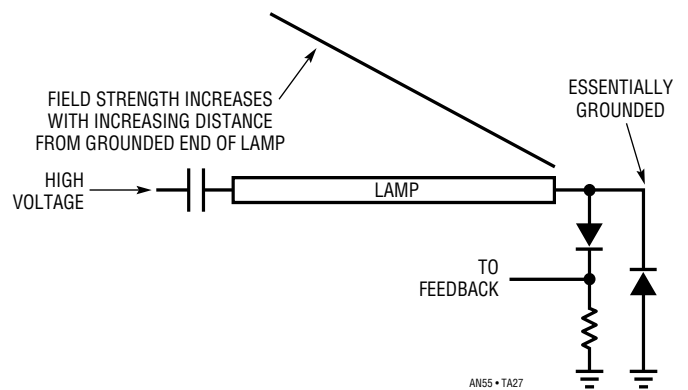


Figure 27. Field Strength vs Distance for a Ground Referred Lamp. Field Imbalance Promotes Uneven Illumination at Low Drive Levels

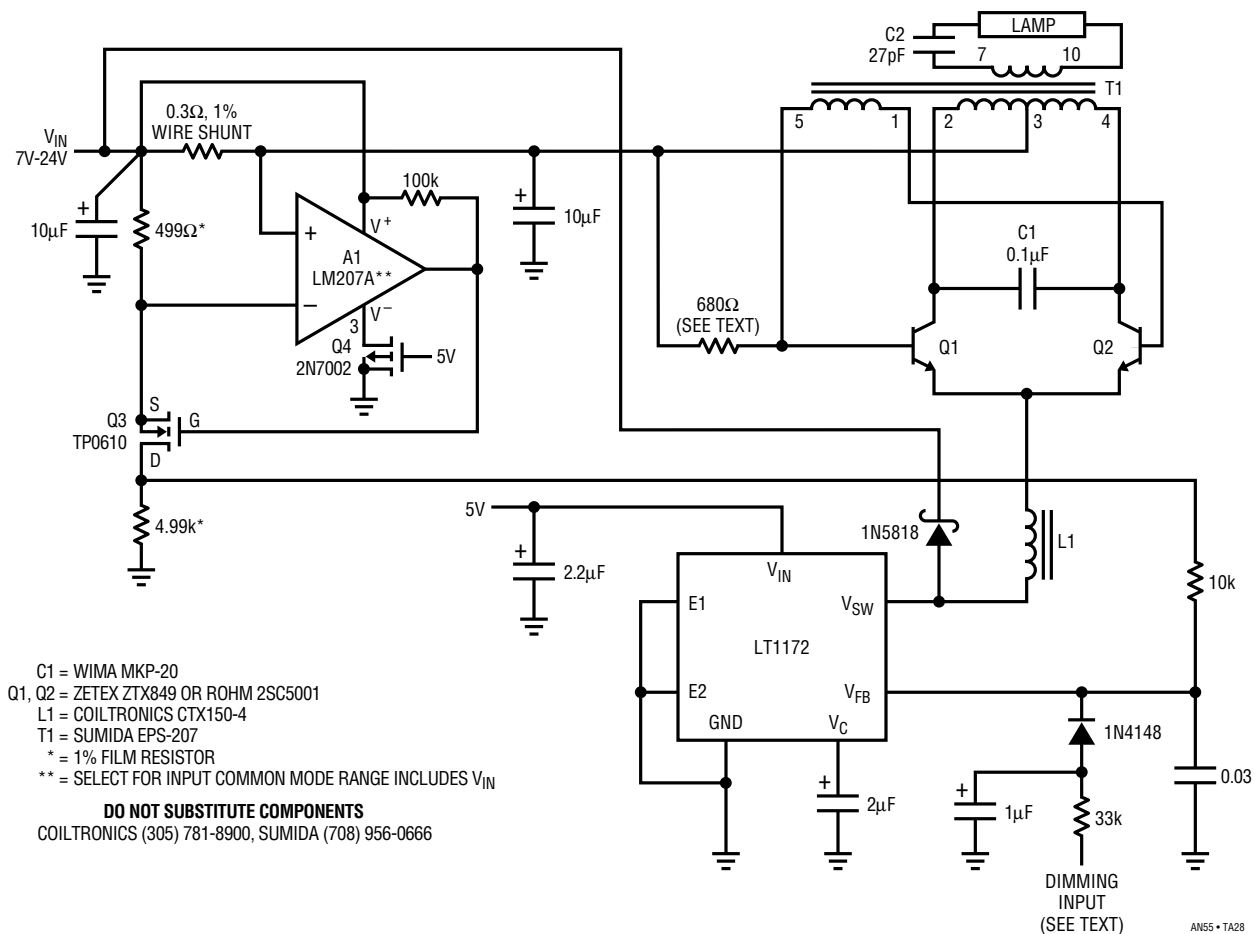


Figure 28. The “Low Thermometer” Configuration. “Topside Sensed” Primary Derived Feedback Balances Lamp Drive, Extending Dimming Range

aspect is that the lamp is fully floating—there is no galvanic connection to ground as in the previous designs. This allows T1 to deliver symmetric, differential drive to the lamp. Such balanced drive eliminates field imbalance, reducing thermomentering at low lamp currents. This approach precludes any feedback connection to the now floating output. Maintaining closed loop control necessitates deriving a feedback signal from some other point. In theory, lamp current proportions to T1’s or L1’s drive level, and some form of sensing this can be used to provide feedback. In practice, parasitics make a practical implementation difficult.¹¹

Figure 28 derives the feedback signal by measuring Royer converter current and feeding this information back to the LT1172. The Royer’s drive requirement closely proportions to lamp current under all conditions. A1 senses this current across the 0.3Ω shunt and biases Q3, closing a

local feedback loop. Q3’s drain voltage presents an amplified, single ended version of the shunt voltage to the feedback point, closing the main loop. The lamp current is not as tightly controlled as before, but 0.5% regulation over wide supply ranges is possible. The dimming in this circuit is controlled by a 1kHz PWM signal. Note the heavy filtering (33k-1μF) *outside* the feedback loop. This allows a fast time constant, minimizing turn-on overshoot.¹²

In all other respects operation is similar to the previous circuits. This circuit typically permits the lamp to operate over a 40:1 intensity range without “thermomentering.” The normal feedback connection is usually limited to a 10:1 range.

Note 11: See Appendix J, “A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas,” for details.

Note 12: See text section, “Feedback Loop Stability Issues.”

Application Note 55

The losses introduced by the current shunt and A1 degrade overall efficiency by about 2%. As such, circuit efficiency is limited to about 90%. Most of the loss can be recovered at moderate cost in complexity. Figure 29's modifications reduce shunt and A1 losses. A1, a precision micropower type, cuts power drain and permits a smaller shunt value without performance degradation. Unfortunately, A1 does not function when its inputs reside at the V^+ rail. Because the circuit's operation requires this, some accommodation must be made.¹³

At circuit start-up A1's input is pulled to its supply pin potential (actually, slightly above it). Under these conditions A1's input stage is shut off. Normally, A1's output state would be indeterminate but, for the amplifier specified, it will always be high. This turns off Q3, permitting the

Note 13: In other words, we need a hack.

LT1172 to drive the Royer stage. The Royer's operation causes Q1's collector swing to exceed the supply rail. This turns on the 1N4148, the BAT-85 goes off and A1's supply pin rises above the supply rail. This "bootstrapping" action results in A1's inputs being biased within the amplifier's common mode range and normal circuit operation commences.

The result of all this is a 1.6% efficiency gain, permitting an overall circuit efficiency of just below 92%.

Synchronizing

In some situations it is desirable to synchronize circuit operation to a system clock. In particular, pen based computers may be especially sensitive to asynchronous components. The LT1172 can be synchronized by briefly pulling its V_C pin to ground (see LT1172 data sheet).

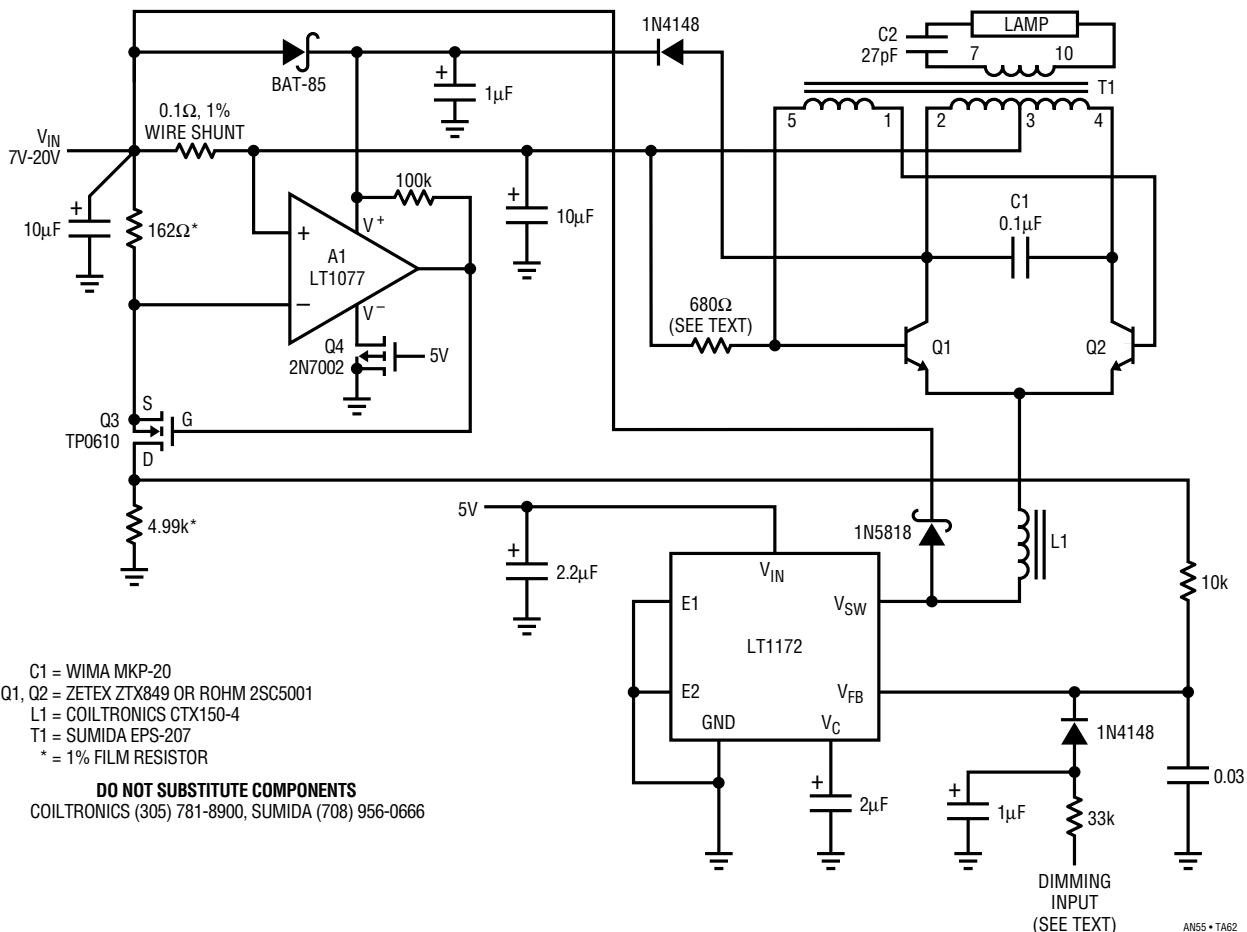


Figure 29. The “Low Thermometer” Circuit using a Micropower, Precision Topside Sensing Amplifier. Supply Bootstrapping Eliminates Input Common Mode Requirement, Permitting a 1.6% Efficiency Gain

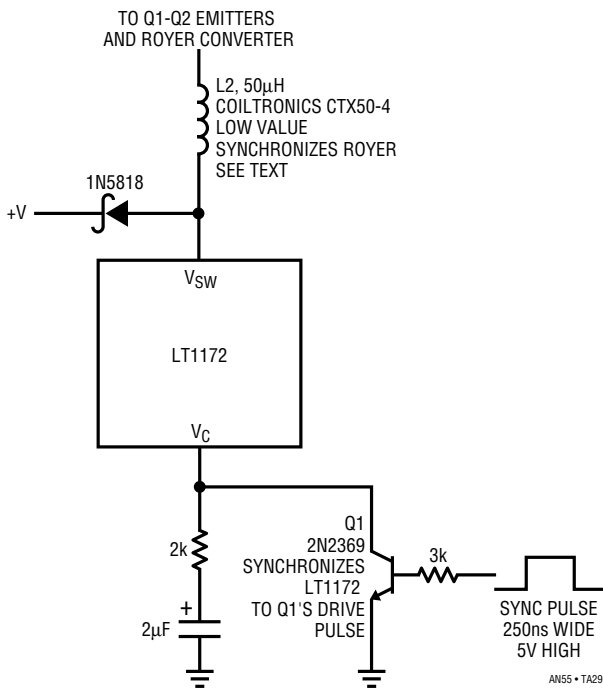


Figure 30. Synchronizing by Lowering L2's Value

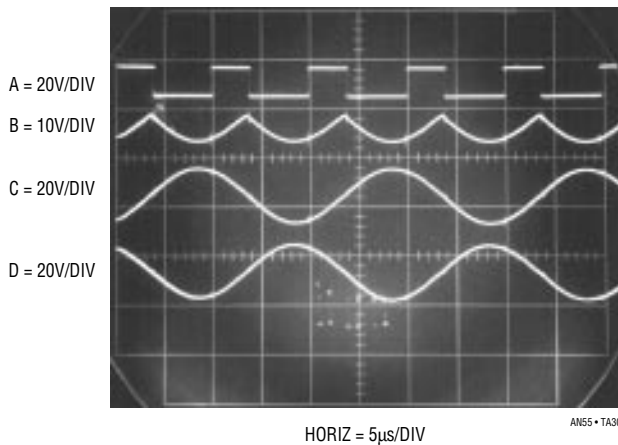


Figure 31. Waveforms for Synchronized Operation

Figure 30 shows a way to do this via Q1 and associated components. If Royer synchronization is also required, reducing L2's value can do this under some conditions. L2's low value introduces greater LT1172 harmonic, causing the Royer to lock at 1/2 the LT1172's switching frequency. This can only occur *if the free running Royer frequency is close to this value*. Pulling the Royer away from its resonant frequency causes some efficiency loss. A further limitation is that, although synchronization is never lost, phase jitter increases over extended dimming

and supply ranges. Typically, 2.5:1 ranges of supply and 10:1 dimming range are practical. Efficiency is typically degraded by about 5% at full power. This approach to full synchronization is simple, but interactions are complex and require careful evaluation for any specific application. Figure 31 shows LT1172 V_{SW} pin, Q1-Q2 emitter and Royer collector waveforms (Traces A, B, C and D respectively) for a synchronized circuit.

Figure 32 uses a different approach to achieve fully synchronized operation. Here, Q1 and Q2 are driven from L3. L3's drive, in turn, comes from a flip-flop which is clocked from the LT1172's V_{SW} pin. L3 provides a level shift, allowing drive to the floating Q1-Q2 pair. The flip-flop's differential drive prevents DC biasing of L3. D1 and D2 permit L3's output current to alternately bias Q1 and Q2 without V_{BE} reverse bias occurring. Figure 33 shows operating waveforms. Trace A is the LT1172 V_{SW} pin while traces B and C are the flip-flop outputs. Traces D and E are the Q1-Q2 bases and Traces F and G their collectors. This scheme works reasonably well, although phase jitter and

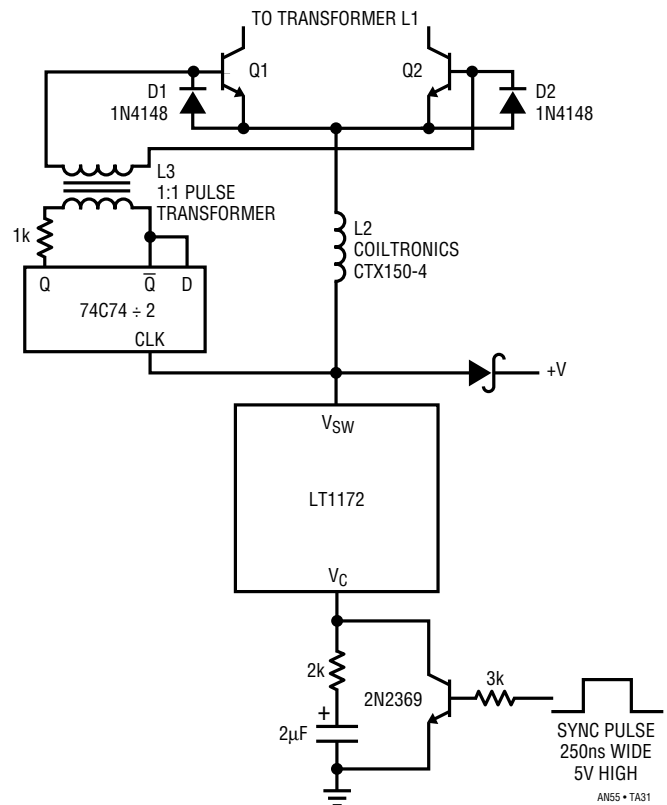


Figure 32. Synchronizing by Driving the DC to AC Converter

Application Note 55

efficiency restrictions (similar to those previously described) apply.

Figure 34's approach eliminates phase jitter. This prototype circuit replaces the Royer configuration with a flip-flop driven pair, Q1-Q2. The flip-flop is driven from an external clock. This clock also sets the frequency of the step-down regulator feeding the L1 based high voltage

converter. The step-down regulator supplies a DC potential to L2. L2's "output" end sources current to the L1 based converter. C1, C2, L1 and the lamp form a tank circuit which, nominally, resonates at the clock regulated frequency. L1's high voltage output puts current through the lamp. Feedback from the lamp, similar to the previous circuit's, closes a control loop at the step-down regulator. The 0.22 μ F capacitor stabilizes this loop.

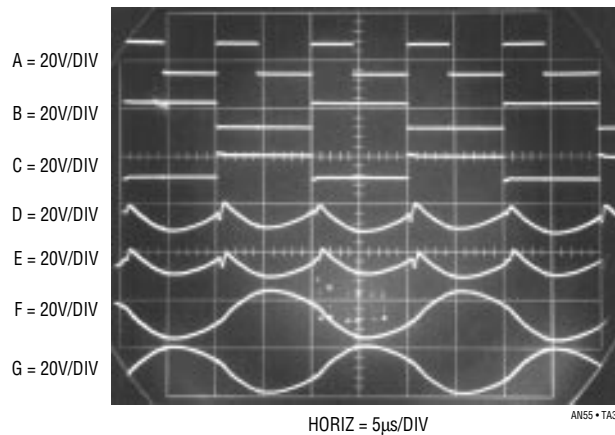


Figure 33. Waveforms for the Driven DC to AC Converter

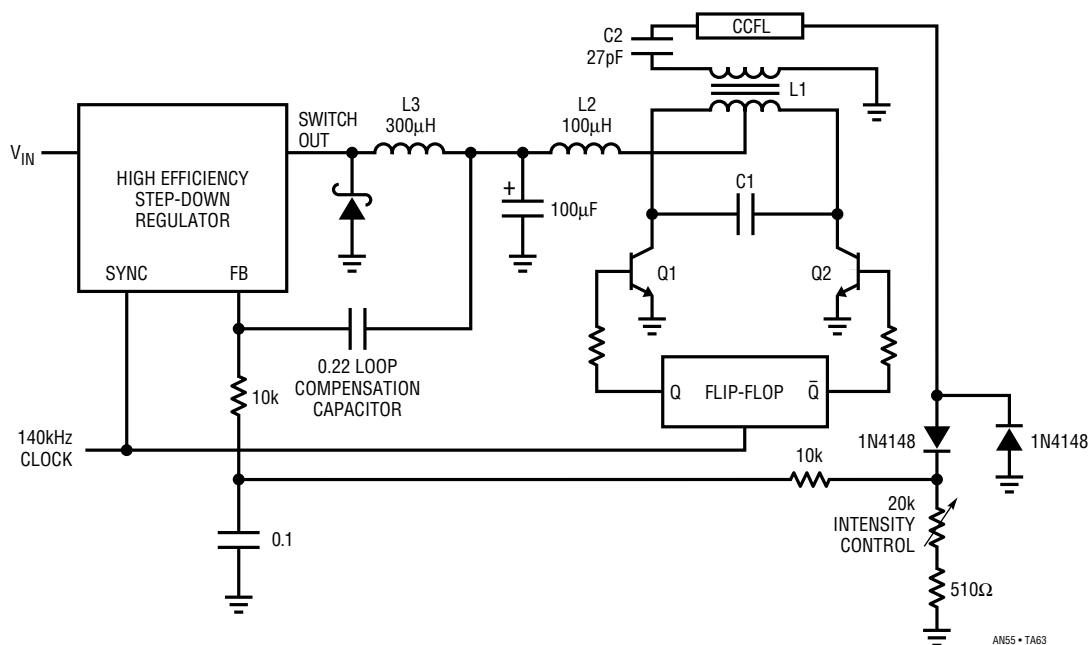


Figure 34. An Inherently Synchronous CCFL Circuit Eliminates Phase Jitter. Trade-Offs Include Increased Complexity and Lower Efficiency over Lamp Operating Range

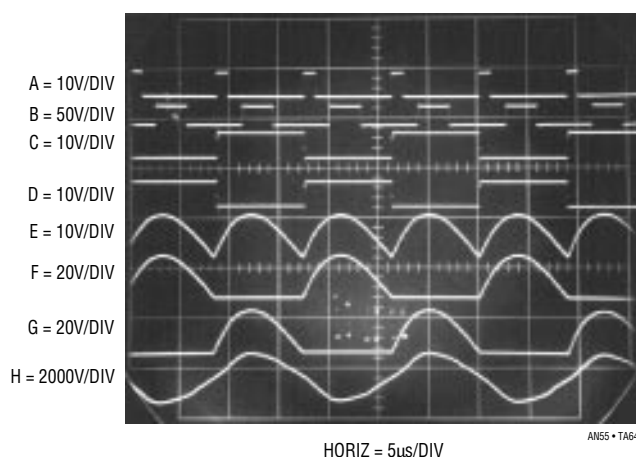


Figure 35. The Fully Synchronized CCFL Circuit's Waveforms, Taken During On-Resonance Operation

Figure 35 shows circuit waveforms. Trace A is the clock, while Trace B is the step-down regulator's switch output. Traces C and D are flip-flop Q and \bar{Q} outputs, respectively. Trace E is the L2-L1 junction and Traces F and G are the Q1 and Q2 collectors, respectively. Trace H is L1's high voltage output. The waveforms show that the synchronous drive to the resonant high voltage converter produces a clean sine wave output. The driven, fully synchronous operation eliminates phase jitter under all conditions. This circuit has the same excellent power supply rejection and regulation characteristics of the Royer based approach.

A potential drawback to this approach is that the resonant frequency of the high voltage converter changes with lamp operating current. The Royer based circuits inherently change frequency in response to this, maintaining on-resonance operation. This contributes to high efficiency operation over a broad range of lamp currents. This

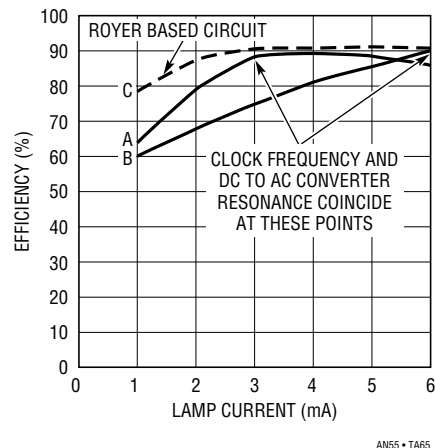


Figure 36. Efficiency vs Lamp Current for the Synchronous Circuit. Off-Resonance Operation Causes Efficiency Fall-Off away from Indicated Lamp Currents

circuit's fixed frequency drive means that on-resonance operation only occurs at one lamp current. In practice, C1 and C2 set the "true" resonant operating point at any desired current. Efficiency falls off at other currents because the high voltage converter is forced to run off-resonance.

Figure 36's plot shows the effects of this on efficiency. Curve A results with the circuit optimized at 3mA lamp current (1/2 power), while Curve B represents optimization at 6mA (full power). In both cases, efficiency suffers at currents away from these points. Curve C shows a Royer based circuit's performance for comparison.

The circuit is also sensitive to C1 and C2 tolerances. A 10% total tolerance deviation can cause 4% efficiency degradation at the nominally optimized current.

Note: This application note was derived from a manuscript originally prepared for publication in EDN Magazine.

Application Note 55

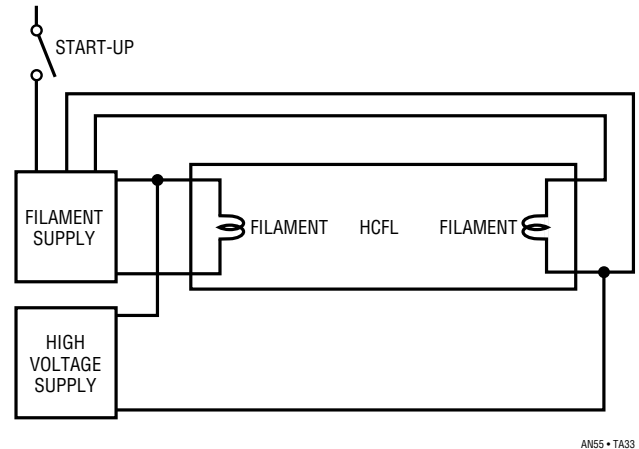
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APPENDIX A

“HOT” CATHODE FLUORESCENT LAMPS

Many CCFL characteristics are shared by so-called “Hot” Cathode Fluorescent Lamps (HCFLs). The most significant difference is that HCFLs contain filaments at each end of the lamp (see Figure A1). When the filaments are powered they emit electrons, lowering the lamp’s ionization potential. This means a significantly lower voltage will start the lamp. Typically the filaments are turned on, a relatively modest voltage impressed across the lamp, and start-up occurs. Once the lamp starts, filament power is removed. Although HCFLs reduce the high voltage requirement they require a filament supply and sequencing circuitry. The CCFL circuits shown in the text will start and run HCFLs without using the filaments. In practice this involves simply driving the filament connections at the HCFL ends as if they were CCFL electrodes.



AN55 • TA33

Figure A1. A Conceptual Hot Cathode Fluorescent Lamp Power Supply. Heated Filaments Liberate Electrons, Lowering the Lamp’s Start-Up Voltage Requirement. CCFL Supply Discussed in Text Eliminates Filament Supply

APPENDIX B

MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS

Charles L. Guthrie, Sharp Electronics Corporation

Introduction

As more companies begin the manufacturing of their next generation of computers, there is a need to reduce the overall size and weight of the units to improve their portability. This has sparked the need for more compact designs where the various components are placed in closer proximity, thus making them more susceptible to interaction from signal noise and heat dissipation. The following is a summary of guidelines for the placement of the display components and suggestions for overcoming difficult design constraints associated with component placement.

In notebook computers the thickness of the display housing is important. The design usually requires the display to be in a pivotal structure so that the display may be folded down over the keyboard for transportation. Also, the outline dimensions must be minimal so that the package will remain as compact as possible. These two constraints drive the display housing design and placement of the

display components. This discussion surveys each of the problems facing the designer in detail and offers suggestions for overcoming the difficulties to provide a reliable assembly.

The problems facing the pen based computer designer are similar to those realized in notebook designs. In addition, however, pen based designs require protection for the face of the display. In pen based applications, as the pen is moved across the surface of the display, the pen has the potential for scratching the front polarizer. For this reason the front of the display must be protected. Methods for protecting the display face while minimizing effects on the display image are given.

Additionally, the need to specify the flatness of the bezel is discussed. Suggestions for acceptable construction techniques for sound design are included. Further, display components likely to cause problems due to heat buildup are identified and methods for minimization of the heat’s effects are presented.

Application Note 55

The ideas expressed here are not the only solutions to the various problems and have not been assessed as to whether they may infringe on any patents issued or applied for.

Flatness and Rigidity of the Bezel

In the notebook computer the bezel has several distinct functions. It houses the display, the inverter for the backlight, and in some instances, the controls for contrast and brightness of the display. The bezel is usually designed to tilt to set the optimum viewing angle for the display.

It is important to understand that the bezel must provide a mechanism to keep the display flat, particularly at the mounting holds. Subtle changes in flatness place uneven stress on the glass which can cause variations in contrast across the display. Slight changes in pressure may cause significant variation in the display contrast. Also, at the extreme, significantly uneven pressures can cause the display glass to fail.

Because the bezel must be functional in maintaining the flatness of the display, consideration must be made for the strength of the bezel. Care must be taken to provide structural members, while minimizing the weight of the unit. This may be executed using a parallel grid, normal to the edges of the bezel, or angled about 45° off of the edges of the bezel. The angled structure may be more desirable in that it provides resistance to torquing the unit while lifting the cover with one hand. Again, the display is sensitive to stresses from uneven pressure on the display housing.

Another structure which will provide excellent rigidity, but adds more weight to the computer, is a “honeycomb” structure. This “honeycomb” structure resists torquing from all directions and tends to provide the best protection for the display.

With each of these structures it is easy to provide mounting assemblies for the display. “Blind nuts” can be molded into the housing. The mounting may be done to either the front or rear of the bezel. Attachment to the rear may provide better rigidity for placement of the mounting hardware.

One last caution is worth noting in the development of a bezel. The bezel should be engineered to absorb most of

the shock and vibration experienced in a portable computer. Even though the display has been carefully designed, the notebook computer presents extraordinary shock and abuse problems.

Avoiding Heat Buildup in the Display

Several of the display components are sources for heat problems. Thermal management must be taken into account in the design of the display bezel. A heated display may be adversely affected; a loss of contrast uniformity usually results. The Cold Cathode Fluorescent Tube (CCFT) itself gives off a small amount of heat relative to the amount of power dissipated in its glow discharge. Likewise, even though the inverters are designed to be extremely efficient, there is some heat generated. The buildup of heat in these components will be aggravated by the typically “tight” designs currently being introduced. There is little ventilation designed into most display bezels. To compound the problem, the plastics used are poor thermal conductors, thus causing the heat to build up which may affect the display.

Some current designs suffer from poor placement of the inverter and/or poor thermal management techniques. These designs can be improved, even where redesign of the display housing, with improved thermal management, is impractical.

One of the most common mistakes in current designs is that there has been no consideration for the buildup of heat from the CCFT. Typically, the displays for notebook applications have only one CCFT to minimize display power requirements. The lamp is usually placed along the right edge of the display. Since the lamp is placed very close to the display glass, it can cause a temperature rise in the liquid crystal. It is important to note that variations in temperature of as little as 5°C can cause an apparent non-uniformity in display contrast. Variations caused by slightly higher temperature variations will cause objectionable variations in the contrast and display appearance.

To further aggravate the situation, some designs have the inverter placed in the bottom of the bezel. This has a tendency to cause the same variations in contrast, particularly when the housing does not have any heat sinking for the inverter. This problem manifests itself as a “blooming” of the display, just above the inverter. This “blooming”

looks like a washed out area where, in the worst case, the characters on the display fade completely.

The following section discusses the recommended methods for overcoming these design problems.

Placement of the Display Components

One of the things that can be done is to design the inverter into the base of the computer with the motherboard. In some applications this is impractical because this requires the high voltage leads to be mounted within the hinges connecting the display bezel to the main body. This causes a problem with strain relief of the high voltage leads, and thus with UL certification.

One mistake, made most often, is placing the inverter at the bottom of the bezel next to the lower edge of the display. It is a fact that heat rises, yet this is one of the most overlooked problems in new notebook designs. Even though the inverters are very efficient, some energy is lost in the inverter in the form of heat. Because of the insulating properties of the plastic materials used in the bezel construction, heat builds up and affects the display contrast.

Designs with the inverter at the bottom can be improved in one of three ways. The inverter can be relocated away from the display, heat sinking materials can be placed between the display and the inverter, or ventilation can be provided to remove the heat.

In mature designs, it may be impractical to do what is obvious and move the inverter up to the side of the display towards the top of the housing. In these cases, the inverter may be insulated from the display with a "heat dam." One method of accomplishing this would be to use a piece of mica insulator die cut to fit tightly between the inverter and the display. This heat dam would divert the heat around the end of the display bezel to rise harmlessly to the top of the housing. Mica is recommended in this application because of its thermal and electrical insulation properties.

The last suggestion for removing heat is to provide some ventilation to the inverter area. This has to be done very carefully to prevent exposing the high voltage. Ventilation may not be a practical solution because resistance to liquids and dust is compromised.

The best solution for the designer of new hardware is to consider the placement of the inverter to the side of the display and at the top of the bezel. In existing designs of this type the effects of heat from the inverter, even in tight housings, has been minimal or non-existent.

One problem which is aggravated by the placement of the inverter at the bezel is heat dissipated by the CCFT. In designs where the inverter is placed up and to the side of the display, fading of the display contrast due to CCFT heat is not a problem. However, when the inverter is placed at the bezel bottom, some designs experience a loss of contrast aggravated by the heat from the CCFT and inverter.

In cases where the inverter must be left at the bottom, and the CCFT is causing a loss of contrast, the problem can be minimized by using an aluminum foil heat sink. This does not remove the heat from the display, but dissipates it over the entire display area, thus normalizing the display contrast. The aluminum foil is easy to install and in some present designs has successfully improved the display contrast.

Remember that the objection to the contrast variation stems more from non-uniformity than from a total loss of contrast.

Protecting the Face of the Display

One of the last considerations in the design of notebook and pen based computers is protection of the display face. The front polarizer is made of a mylar base and thus is susceptible to scratching. The front protection for the display, along with providing scratch protection, may also provide an anti-glare surface.

There are several ways that scratch resistance and anti-glare surfaces can be incorporated. A glass or plastic cover may be placed over the display, thus providing protection. The material should be placed as close to the display as possible to minimize possible parallax problems due to reflections off of the cover material. With anti-glare materials, the further the material is from the front of the display the greater the distortion.

In pen applications, the front anti-scratch material is best placed in contact with the front glass of the display. The cover glass material normally needs to be slightly thicker

Application Note 55

to protect the display from distortion when pressure is being exerted on the front.

There are several methods for making the pen input devices. Some use the front surface of the cover glass to provide input data and some use a field effect to a printed wiring board on the back of the display. When the pen input is on the front of the display, the input device is usually on a glass surface.

APPENDIX C

ACHIEVING MEANINGFUL EFFICIENCY MEASUREMENTS

Obtaining reliable efficiency data for the CCFL circuits presents a high order difficulty measurement problem. Establishing and maintaining accurate AC measurements is a textbook example of attention to measurement technique. The combination of high frequency, harmonic laden waveforms and high voltage makes meaningful results difficult to obtain. The choice, understanding and use of test instrumentation is crucial. Clear thinking is needed to avoid unpleasant surprises!¹

Probes

The probes employed must faithfully respond over a variety of conditions. Measuring across the resistor in series with the CCFL is the most favorable circumstance. This low voltage, low impedance measurement allows use of a standard 1X probe. The probe's relatively high input capacitance does not introduce significant error. A 10X probe may also be used, but frequency compensation issues (discussion to follow) must be attended to.

The high voltage measurement across the lamp is considerably more demanding on the probe. The waveform fundamental is at 20kHz to 100kHz, with harmonics into the MHz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects which would corrupt the measurement. The design and construction of such a probe requires significant attention. Figure C1 lists some recommended probes along with their characteristics. As stated in the text, almost all

To limit specular reflection in this application, the front cover glass should be bonded to the display. Care must be taken to insure that the coefficient of thermal expansion is matched for all of the materials used in the system. Because of the difficulties encountered with the bonding of the cover glass, and the potential to destroy the display through improper workmanship, consulting an expert is strongly recommended.

standard oscilloscope probes *will fail*² if used for this measurement. Attempting to circumvent the probe requirement by resistively dividing the lamp voltage also creates problems. Large value resistors often have significant voltage coefficients and their shunt capacitance is high and uncertain. As such, simple voltage dividing is not recommended. Similarly, common high voltage probes intended for DC measurement will have large errors because of AC effects. The P6013A and P6015 are the favored probes; their 100M Ω input and small capacitance introduces low loading error. The penalty for their 1000X attenuation is reduced output, but the recommended voltmeters (discussion to follow) can accommodate this.

All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1M Ω paralleled by (typically) 10pF-22pF. The recommended voltmeters, which will be discussed, have significantly different input characteristics. Figure C2's table shows higher input resistances and a range of capacitances. Because of this the probe must be compensated for the voltmeter's input characteristics. Normally, the optimum compensation point is easily determined and adjusted by observing probe output on an oscilloscope. A known amplitude square wave is fed in (usually from the oscilloscope calibrator) and the probe adjusted for correct response. Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct.

Note 1: It is worth considering that various constructors of text Figure 6 have reported efficiencies ranging from 8% to 115%.

Note 2: That's twice we've warned you nicely.

TEKTRONIX PROBE TYPE	ATTENUATION FACTOR	ACCURACY	INPUT RESISTANCE	INPUT CAPACITANCE	RISE TIME	BANDWIDTH	MAXIMUM VOLTAGE	DERATED ABOVE	DERATED TO AT FREQUENCY	COMPENSATION RANGE	ASSUMED TERMINATION RESISTANCE
P6007	100X	3%	10M Ω	2.2pF	14ns	25MHz	1.5kV	200kHz	700V _{RMS} at 10MHz	15-55pF	1M
P6009	100X	3%	10M Ω	2.5pF	2.9ns	120MHz	1.5kV	200kHz	450V _{RMS} at 40MHz	15-47pF	1M
P6013A	1000X	Adjustable	100M Ω	3pF	7ns	50MHz	12kV	100kHz	800V _{RMS} at 20MHz	12-60pF	1M
P6015	1000X	Adjustable	100M Ω	3pF	4.7ns	75MHz	20kV	100kHz	2000V _{RMS} at 20MHz	12-47pF	1M

Figure C1. Characteristics of some Wideband High Voltage Probes. Output Impedances are Designed for Oscilloscope Inputs

MANUFACTURER AND MODEL	FULL SCALE RANGES	ACCURACY AT 1MHz	ACCURACY AT 100kHz	INPUT RESISTANCE AND CAPACITANCE	MAXIMUM BANDWIDTH	CREST FACTOR
Hewlett-Packard 3400 Meter Display	1mV to 300V, 12 Ranges	1%	1%	0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF	10MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Hewlett-Packard 3403C Digital Display	10mV to 1000V, 6 Ranges	0.5%	0.2%	10mV and 100mV Range = 20M and 20pF \pm 10%, 1V to 1000V Range = 10M and 24pF \pm 10%	100MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Fluke 8920A Digital Display	2mV to 700V, 7 Ranges	0.7%	0.5%	10M and < 30pF	20MHz	7:1 At Full Scale, 70:1 At 0.1 Scale

Figure C2. Pertinent Characteristics of some Thermally Based RMS Voltmeters. Input Impedances Necessitate Matching Network and Compensation for High Voltage Probes

The impedance mismatch occurs at low and high frequency. The low frequency term is corrected by placing an appropriate value resistor in shunt with the probe's output. For a 10M Ω voltmeter input a 1.1M Ω resistor is suitable. This resistor should be built into the smallest possible BNC equipped enclosure to maintain a coaxial environment. No cable connections should be employed; the enclosure should be placed *directly* between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low frequency impedance mismatch. Figure C4 shows the impedance matching box attached to the high voltage probe.

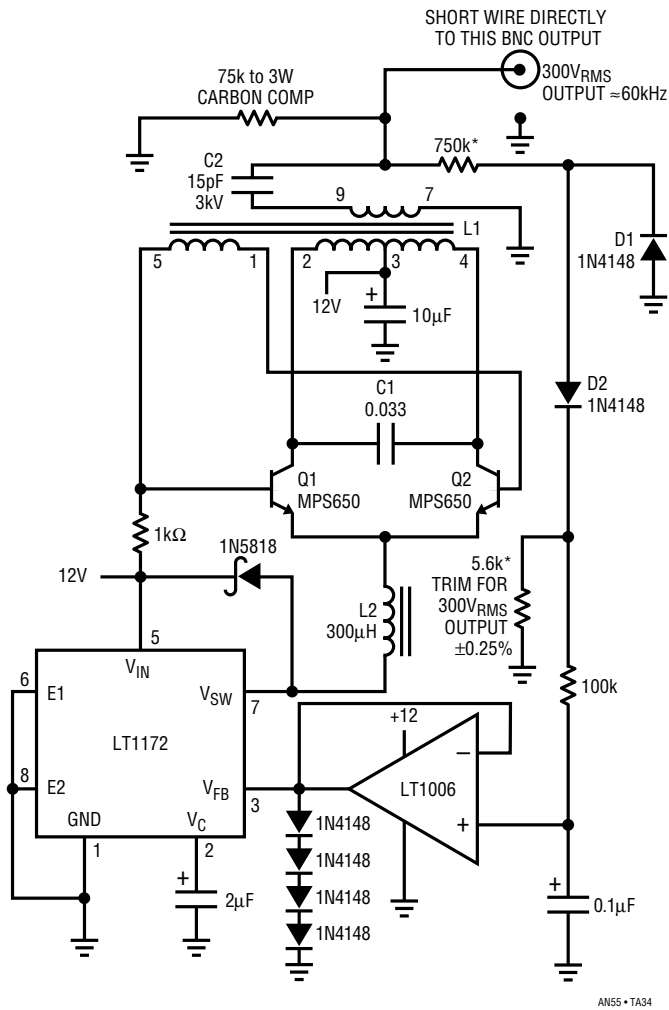
Correcting the high frequency mismatch term is more involved. The wide range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. How is the experimenter to know where to set the high frequency probe compensation adjustment? One solution is to feed a known value RMS signal to the probe-voltmeter combination and adjust compensation for a proper reading. Figure C3 shows a way to generate a known RMS voltage. This scheme is simply a standard backlight circuit reconfigured for a constant voltage output. The op amp permits low RC loading of the 5.6k feedback termination without introducing bias current

error. The 5.6k Ω value may be series or parallel trimmed for a 300V output. Stray parasitic capacitance in the feedback network affects output voltage. Because of this, all feedback associated nodes and components should be rigidly fixed and the entire circuit built into a small metal box. This prevents any significant change in the parasitic terms. The result is a known 300V_{RMS} output.

Now, the probe's compensation is adjusted for a 300V voltmeter indication using the shortest possible connection (e.g., BNC-to-probe adapter) to the calibrator box. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If the probe compensation is altered (e.g., for proper response on an oscilloscope) the voltmeter's reading will be erroneous.³ It is good practice to verify the calibrator box output before and after every set of efficiency measurements. This is done by *directly* connecting, via BNC adapters, the calibrator box to the RMS voltmeter on the 1000V range.

Note 3: The translation of this statement is to hide the probe when you are not using it. If anyone wants to borrow it, look straight at them, shrug your shoulders and say you don't know where it is. This is decidedly dishonest, but eminently practical. Those finding this morally questionable may wish to re-examine their attitude after producing a day's worth of worthless data with a probe that was unknowingly readjusted.

Application Note 55



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS CTX300-4
Q1, Q2 = AS SHOWN OR BCP 56 (PHILLIPS SO PACKAGE)
* = 1% FILM RESISTOR (TEN 75kΩ RESISTORS IN SERIES)
DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure C3. High Voltage RMS Calibrator is Voltage Output Version of CCFL Circuit

RMS Voltmeters

The efficiency measurements require an RMS responding voltmeter. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all AC voltmeters, including DVMs with AC ranges.

There are a number of ways to measure RMS AC voltage. Three of the most common include *average*, *logarithmic*,



AN55 • TA35

Figure C4. The Impedance Matching Box (Extreme Left) Mated to the High Voltage Probe. Note Direct Connection. No Cable is used

and *thermally* responding. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true RMS value. Although these instruments are "real time" analog computers their 1% error bandwidth is well below 300kHz and crest factor capability is limited. Almost all general purpose DVMs use such a logarithmically based approach and, as such, are not suitable for CCFL efficiency measurements. Thermally based RMS voltmeters are direct acting thermo-electronic analog computers. They respond to the input's RMS heating value. This technique is explicit, relying on the very definition of RMS (e.g., the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques.⁴ Additionally, they are insensitive to waveform shape and easily accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

Figure C5 shows a conceptual thermal RMS-DC converter. The input waveform warms a heater, resulting in increased output from its associated temperature sensor. A DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input-output RMS voltage relationship is linear with unity gain.

Note 4: Those finding these descriptions intolerably brief are commended to References 4, 5 and 6.

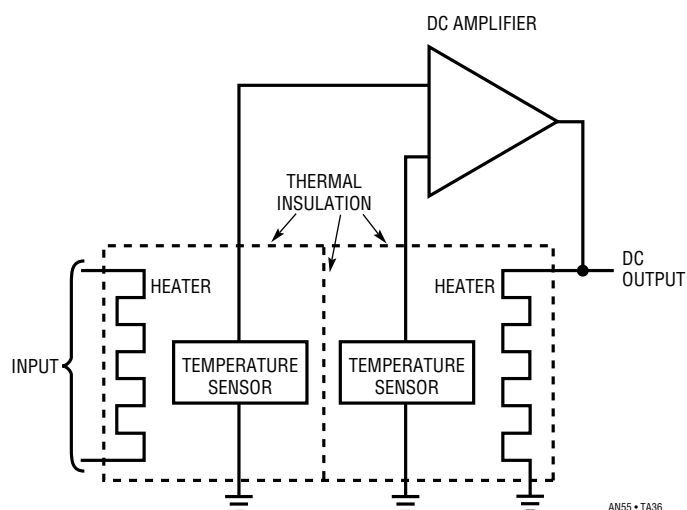


Figure C5. Conceptual Thermal RMS-DC Converter

The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier rejects this common mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure C5's output is linear because the matched thermal pair's nonlinear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS-DC measurements.

The instruments listed in Figure C2, while considerably more expensive than other options, are typical of what is required for meaningful results. The HP3400A and the Fluke 8920A are currently available from their manufacturers. The HP3403C, an exotic and highly desirable instrument, is no longer produced but readily available on the secondary market.

Figure C6 shows equipment in a typical efficiency test set-up. The RMS voltmeters (photo center and left) read output voltage and current via high voltage (left) and standard 1X probes (lower left). Input voltage is read on a DVM (upper right). A low loss clip-on ammeter (lower right) determines input current. The CCFL circuit and LCD display are in the foreground. Efficiency, the ratio of input to output power, is computed with a hand held calculator (lower right).

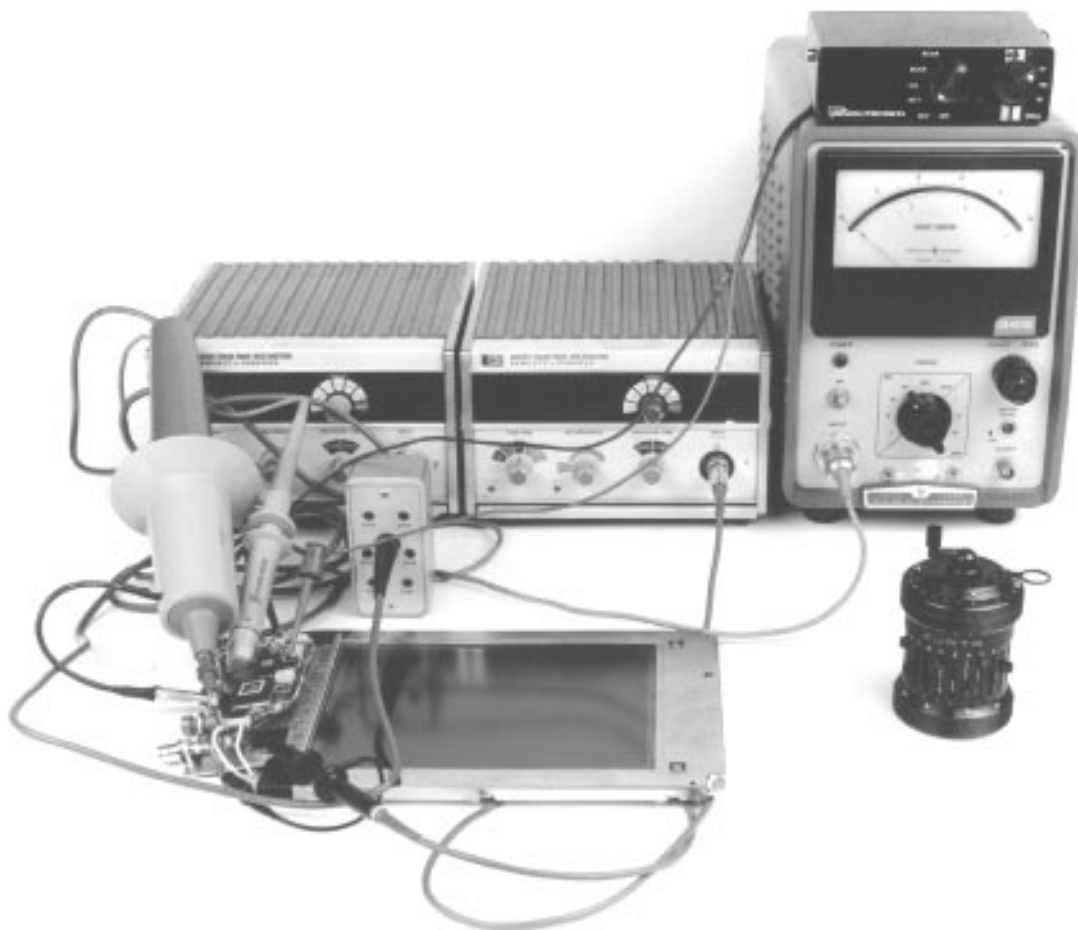
Calorimetric Correlation of Electrical Efficiency Measurements

Careful measurement technique permits a high degree of confidence in the efficiency measurement's accuracy. It is, however, a good idea to check the method's integrity by measuring in a completely different domain. Figure C7 does this by calorimetric techniques. This arrangement, identical to the thermal RMS voltmeter's operation (Figure C5), determines power delivered by the CCFL circuit by measuring its load temperature rise. As in the thermal RMS voltmeter a differential approach eliminates ambient temperature as an error term. The differential amplifier's output, assuming a high degree of matching in the two thermal enclosures, proportions to load power. The ratio of the two cell's $E \times I$ products yields efficiency information. In a 100% efficient system the amplifier's output energy would equal the power supply's output. Practically it is always less, as the CCFL circuit has losses. This term represents the desired efficiency information.

Figure C8 is similar except that the CCFL circuit board is placed within the calorimeter. This arrangement nominally yields the same information, but is a much more demanding measurement because far less heat is generated. The signal-to-noise (heat rise above ambient) ratio is unfavorable, requiring almost fanatical attention to thermal and instrumentation considerations.⁵ It is significant that the *total* uncertainty between electrical and both calorimetric efficiency determinations was 3.3%. The two thermal approaches differed by about 2%. Figure C9 shows the calorimeter and its electronic instrumentation. Descriptions of this instrumentation and thermal measurements can be found in the References section following the main text.

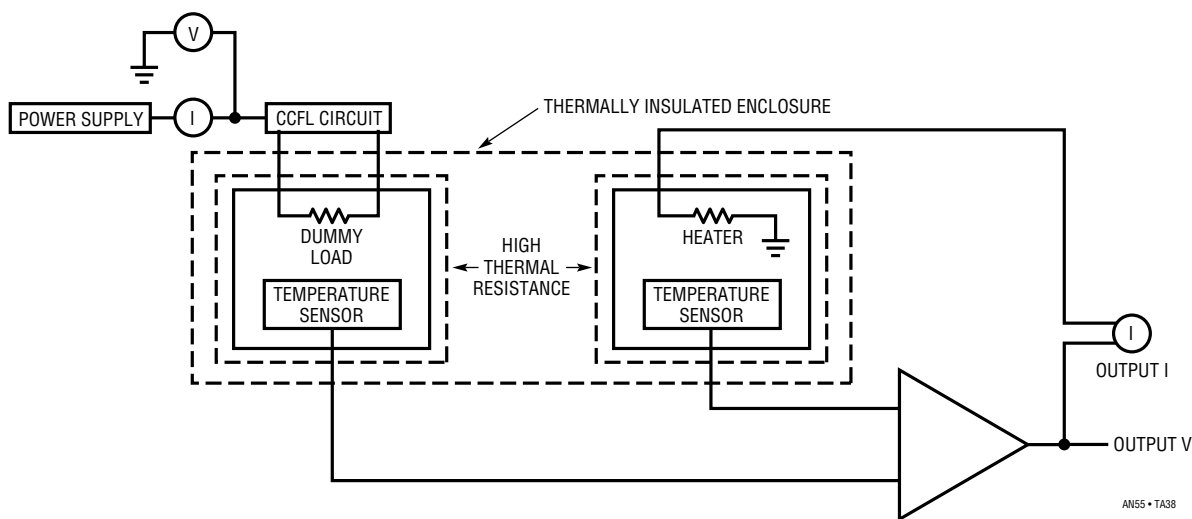
Note 5: Calorimetric measurements are not recommended for readers who are short on time or sanity.

Application Note 55



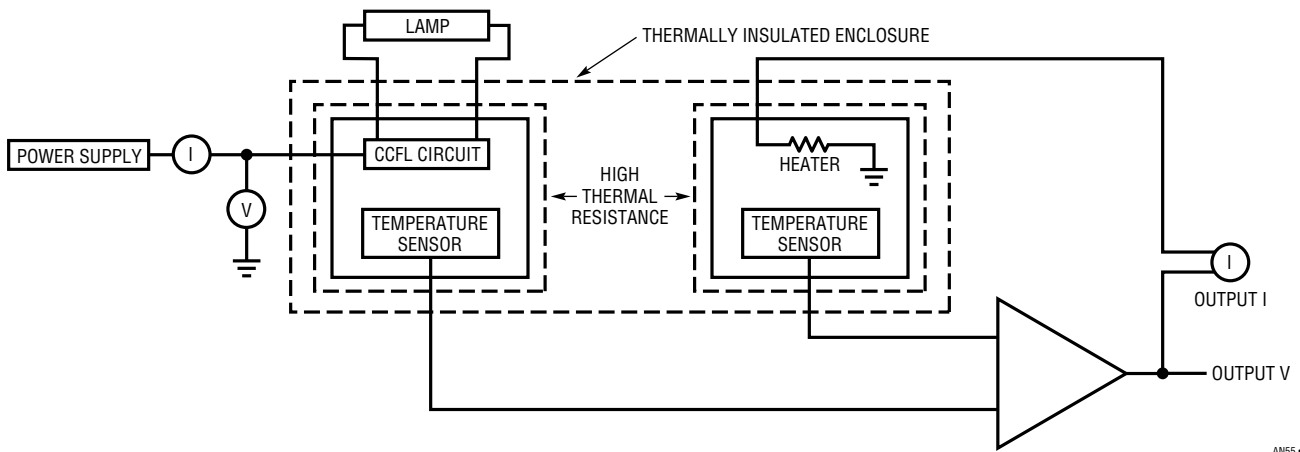
AN55 • TA37

Figure C6. Typical Efficiency Measurement Instrumentation. RMS Voltmeters (Center Left) Measure Output Voltage and Current via Appropriate Probes. Clip-On Ammeter (Right) Gives Low Loss Input Current Readings. DVM (Upper Right) Measures Input Voltage. Hand Calculator (Lower Right) is used to Compute Efficiency



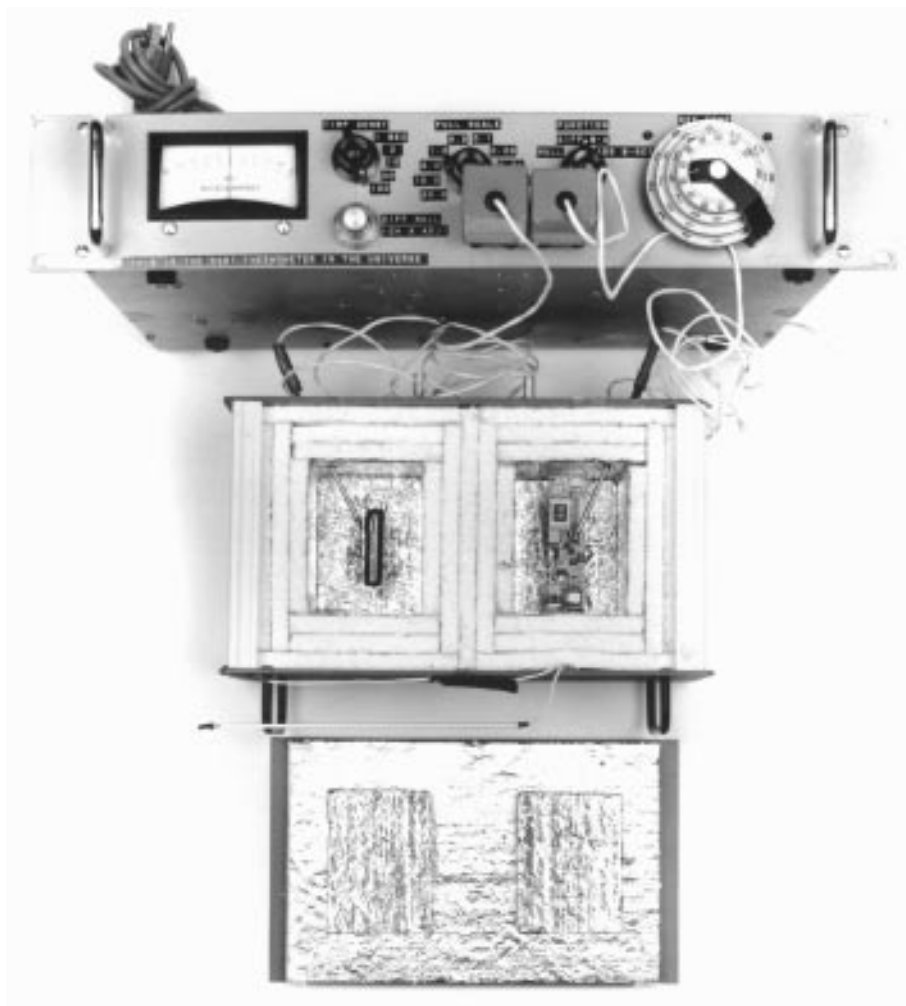
AN55 • TA38

Figure C7. Efficiency Determination via Calorimetric Measurement. Ratio of Power Supply to Output Energy Gives Efficiency Information



AN55 • TA39

Figure C8. The Calorimeter Measures Efficiency by Determining Circuit Heating Losses



AN55 • TA40

Figure C9. The Calorimeter (Center) and its Instrumentation (Top). Calorimeter's High Degree of Thermal Symmetry Combined with Sensitive Servo Instrumentation Produces Accurate Efficiency Measurements. Lower Portion of Photo is Calorimeter's Top Cover

APPENDIX D

PHOTOMETRIC MEASUREMENTS

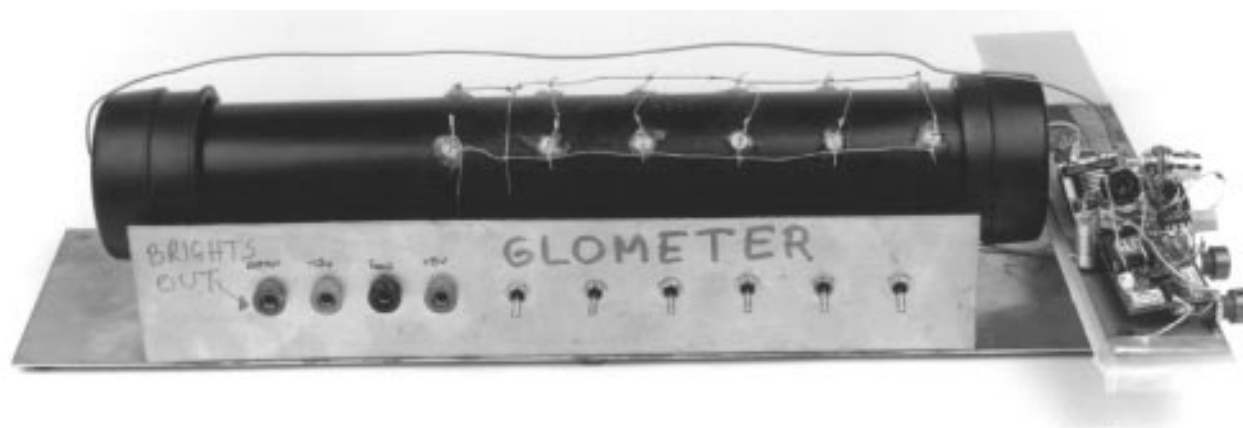
In the final analysis, the ultimate concern centers around the efficient conversion of power supply energy to light. Emitted light varies monotonically with power supply energy,¹ but certainly not linearly. In particular, lamp luminosity may be highly nonlinear, particularly at high power, vs drive power. There are complex tradeoffs involving the amount of emitted light vs power consumption and battery life. Evaluating these tradeoffs requires some form of photometer. The relative luminosity of lamps may be evaluated by placing the lamp in a light tight tube and sampling its output with photodiodes. The photodiodes are placed along the lamp's length and their outputs electrically summed. This sampling technique is an uncalibrated measurement, providing relative data only. It is, however, quite useful in determining relative lamp emittance under various drive conditions. Figure D1 shows this "glometer," with its uncalibrated output appropriately scaled in "brights." The switches allow various sampling diodes along the lamp's length to be disabled. The photodiode signal conditioning electronics are mounted behind the switch panel.

Calibrated light measurements call for a true photometer. The Tektronix J-17/J1803 photometer is such an instrument. It has been found particularly useful in evaluating display (as opposed to simply the lamp) luminosity under various drive conditions. The calibrated output permits reliable correlation with customer results.² The light tight measuring head allows evaluation of emittance evenness at various display locations. This capability is invaluable when optimizing lamp location and/or ballast capacitor values in dual lamp displays.

Figure D2 shows the photometer in use evaluating a display.

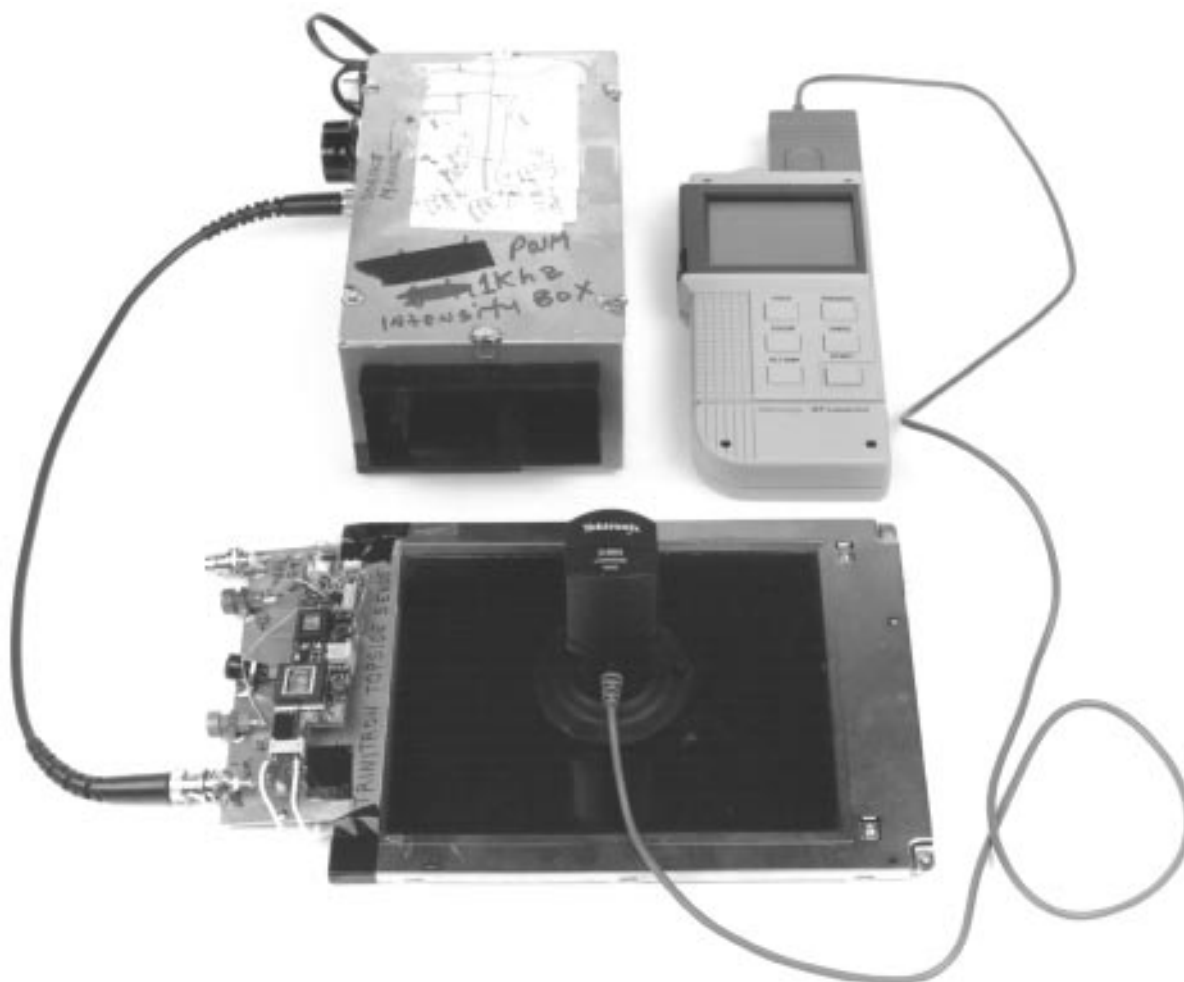
Note 1: But not always! It is possible to build highly electrically efficient circuits that emit less light than "less efficient" designs. See Appendix J, "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas."

Note 2: It is unlikely customers would be enthusiastic about correlating the "brights" units produced by the aforementioned glometer.



AN55 • TA41

Figure D1. The "Glometer" Measures Relative Lamp Emissivity. CCFL Circuit Mounts to the Right. Lamp is Inside Cylindrical Housing. Photodiodes (Center) Convert Light to Electrical Output (Lower Left) via Amplifiers (Not Visible in Photo)



AN55-TM2

Figure D2. Apparatus for Calibrated Photometric Display Evaluation. Photometer (Upper Right) Indicates Display Luminosity via Sensing Head (Center). CCFL Circuit (Left) Intensity is Controlled by a Calibrated Pulse Width Generator (Upper Left)

APPENDIX E

OPEN LAMP PROTECTION

The CCFL circuit's current source output means that "open" or broken lamps cause full output voltage to appear. If this is objectionable Figure E1's modification may be employed. Q3 and associated components form a simple voltage mode feedback loop that operates if V_Z turns on. If T1 sees no load, there is no feedback and the Q1-Q2 pair receive full drive. Collector voltage rises to abnormal levels, and V_Z biases via Q1's V_{BE} path. Q1's collector current drives the feedback node and the circuit finds a stable operating point. This action controls Royer

drive, and hence output voltage. Q3's sensing across the Royer provides power supply rejection. V_Z 's value should be somewhat above the worst case Q1-Q2 V_{CE} voltage under running conditions. It is desirable to select V_Z 's value so clamping occurs at the lowest output voltage possible while still permitting lamp start-up. This is not as tricky as it sounds because the 10k-1 μ F RC delays the effects of Q3's turn-on. Usually, selecting V_Z several volts above the worst case Q1-Q2 V_{CE} will suffice.

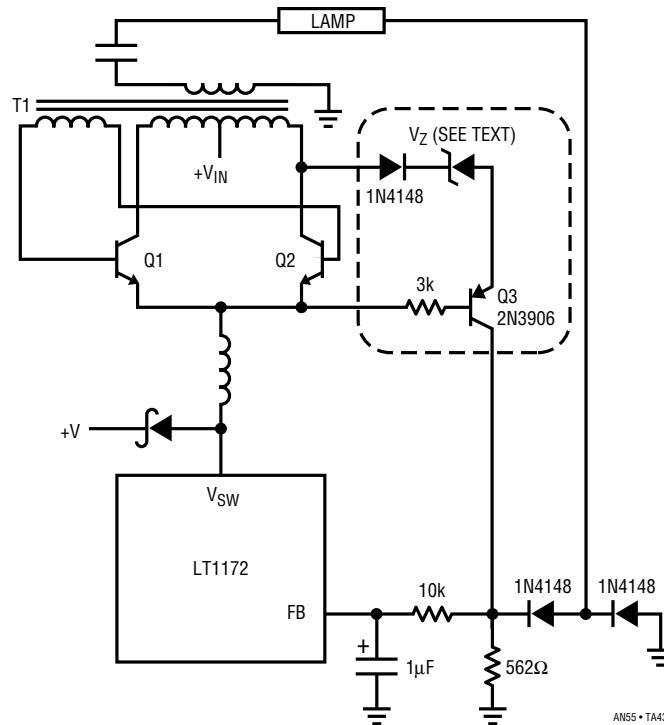


Figure E1. Q3 and Associated Components form a Local Regulating Loop to Limit Output Voltage

APPENDIX F

INTENSITY CONTROL AND SHUTDOWN METHODS

Figure F1 shows a variety of methods for shutting down and controlling intensity of the CCFL circuits. Pulling the LT1172 V_C pin to ground puts the circuit into micropower shutdown. In this mode about $50\mu\text{A}$ flows into the LT1172 V_{IN} pin with essentially no current drawn from the main (Royer center tap) supply. Turning off V_{IN} power eliminates the LT1172's $50\mu\text{A}$ drain.

Three basic ways to control intensity appear in the figure. The most common intensity control method is to add a potentiometer in series with the feedback termination. When using this method insure that the minimum value (in this case 562Ω) is a 1% unit. If a wider tolerance resistor is used the lamp current, at maximum intensity setting, will vary appropriately.

Pulse width modulation or variable DC is sometimes used for intensity control. Two interfaces work well. Directly driving the feedback pin via a diode— 22k resistor with DC or PWM produces intensity control. The other method shown is similar, but places the $1\mu\text{f}$ capacitor outside the feedback loop to get best turn-on transient response. This is the best method if output overshoot must be minimized. See the main text section, "Feedback Loop Stability Issues" for pertinent discussion.

Figure F2 shows a simple circuit which generates precision variable pulse widths. This capability is useful when testing PWM based intensity schemes. The circuit is basically a closed loop pulse width modulator. The crystal controlled 1kHz input clocks the C1-Q1 ramp generator via

the differentiator—CMOS inverter network and the LTC201 reset switch. C1's output drives a CMOS inverter to furnish the output. The output is resistively sampled, averaged and presented to A1's negative input. A1 compares this signal with a variable voltage from the potentiometer. A1's output biases the pulse width modulator, closing a loop around it. The CMOS inverter's purely ohmic output structure combines with A1's ratiometric operation (e.g., both of A1's input signals derive from the +5V supply) to hold pulse width constant. Variations in time, temperature and supply have essentially no effect. The potentiometer's setting is the sole determinant of output pulse width. The Schottky diodes protect the output from latch-up due to cable induced ESD or accidental events¹ during testing.

The output width is calibrated by monitoring it with a counter while adjusting the 2kΩ trim pot.

As mentioned, the circuit is insensitive to power supply variation. However, the CCFL circuit averages the PWM output. It cannot distinguish between a duty cycle shift and supply variation. As such, the test box's 5V supply should be trimmed $\pm 0.01V$. This simulates a "design centered" logic supply under actual operating conditions. Similarly, paralleling additional logic inverters to get lower output impedance should be avoided. In actual use, the CCFL dimming port will be driven from a single CMOS output, and its impedance characteristics must be accurately mimicked.

Note 1: "Accidental events" is a nice way of referring to the stupid things we all do at the bench. Like shorting a CMOS logic output to a -15V supply (then I installed the diodes).

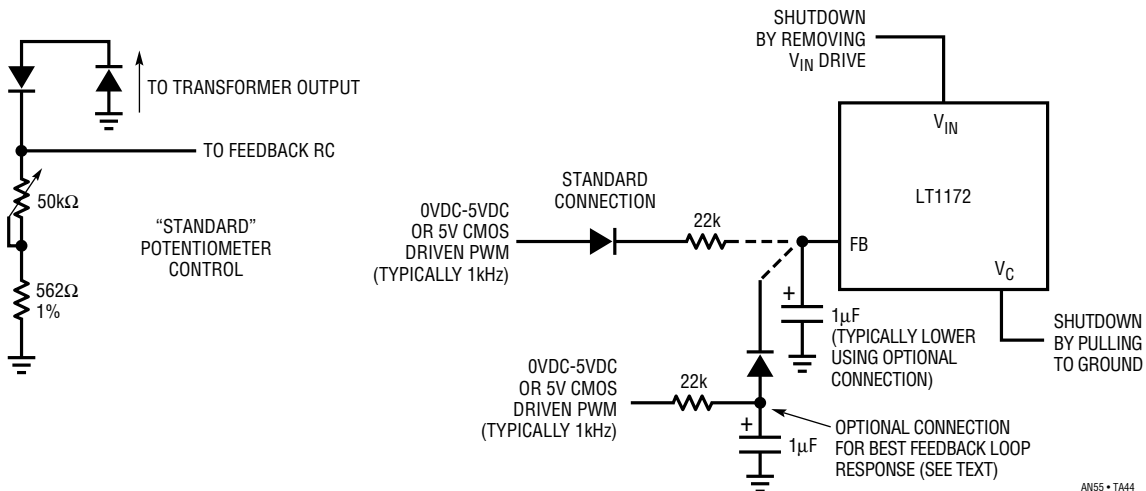


Figure F1. Various Options for Shutdown and Intensity Control

Application Note 55

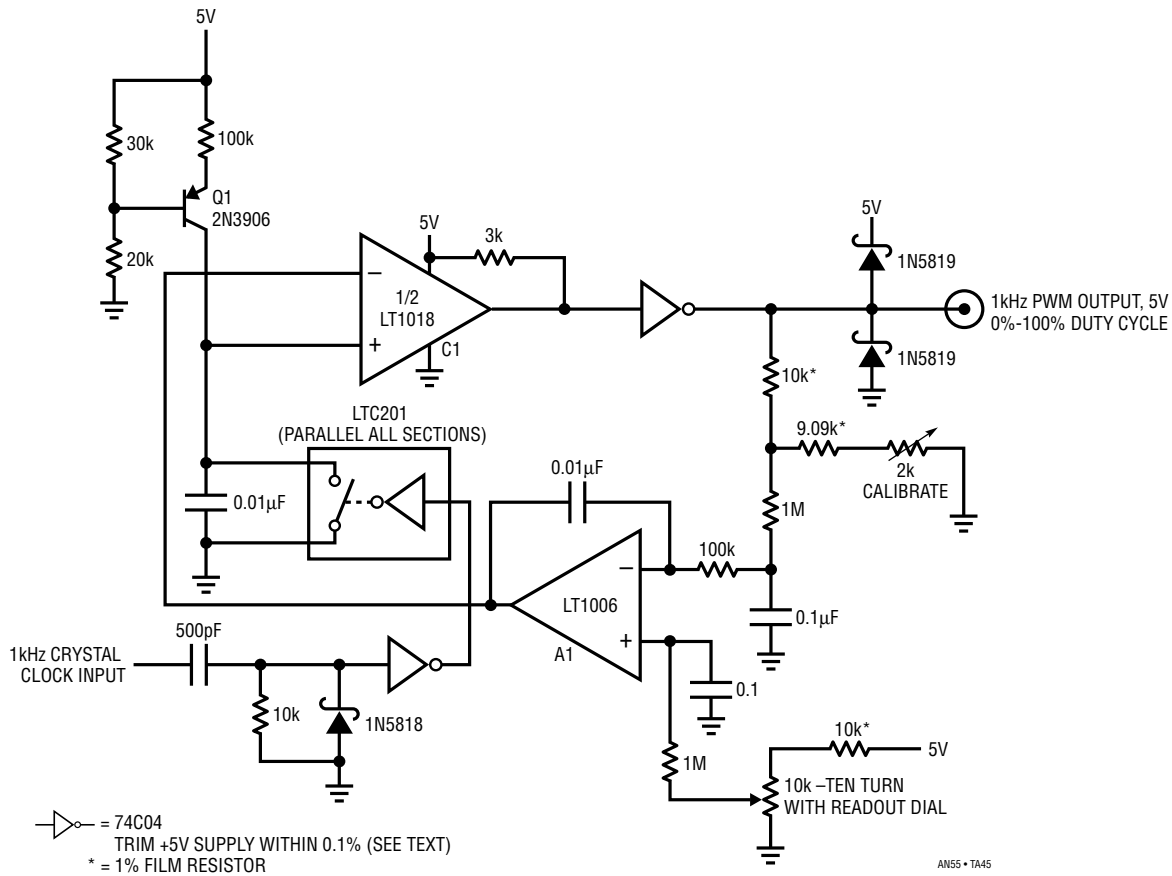


Figure F2. The Calibrated Pulse Width Test Box. A1 Controls C1 Based Pulse Width Modulator, Stabilizing its Operating Point

APPENDIX G

OPERATION FROM HIGH VOLTAGE INPUTS

Some applications require higher input voltages. The 20V maximum input specified in the figures is set by the LT1172 going into its isolated flyback mode (see LT1172 data sheet), not breakdown limits. If the LT1172 V_{IN} pin is driven from a low voltage source (e.g., 5V) the 20V limit may be extended by using Figure G1's network. If the LT1172 is driven from the same supply as L1's center tap, the network is unnecessary, although efficiency will suffer.

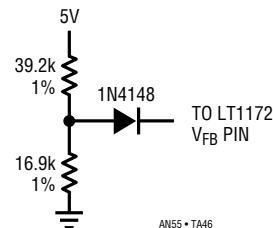


Figure G1. Network allows CCFL Operation beyond 20V Inputs

APPENDIX H

RELATED CIRCUITS

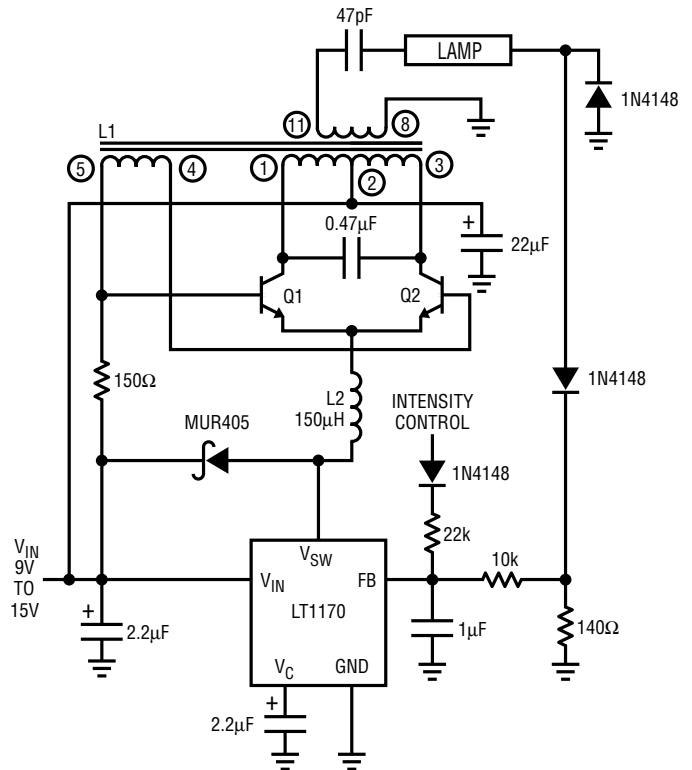
Higher Power Operation

There is no inherent limit on CCFL circuit output power. Figure H1's arrangement is a scaled up version of the text's CCFL circuits. This design, similar to ones employed for automotive use, drives a 25W CCFL. There are virtually no configuration changes, although most component power ratings have increased. The transistors can handle the higher currents, but all other power components are higher capacity. Efficiency is about 80%.

HeNe Laser Power Supply

Helium-neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10kV to start conduction, although they require only about 1500V to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure H2's circuit considerably simplifies driving the laser. The start-up and sustaining functions have been combined into a single, closed-loop current source with over 10kV of compliance. The circuit is recognizable as a reworked CCFL power supply with a voltage tripled DC output.

When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47μF capacitor resonates with L1, providing boosted sine wave drive. L1 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10kV across the laser. The laser breaks down and current begins to flow through it. The 47kΩ resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts pulse width drive to L2 to maintain the



- 0.47μF = WIMA 3X 0.15μF TYPE MKP-20
- Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
- L1 = COILTRONICS CTX02-11128
- L2 = COILTRONICS CTX150-3-52

COILTRONICS (305) 781-8900

AN55 • TA47

Figure H1. A 20W CCFL Supply

FB pin at 1.23V, regardless of changes in operating conditions. In this fashion, the laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The 10μF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9V-35V input range with an electrical efficiency of about 80%.

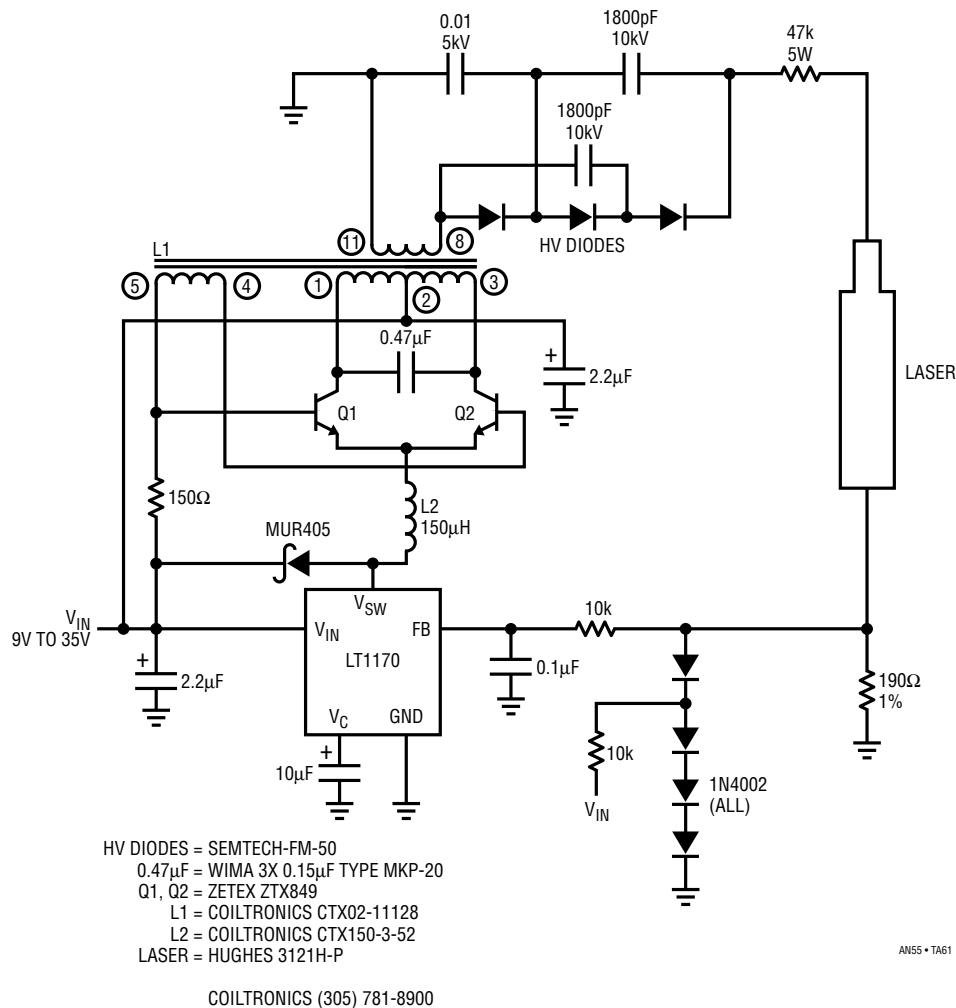


Figure H2. Laser Power Supply, Based on the CCFL Circuit, is Essentially a 10,000V Compliance Current Source

APPENDIX I

WHO WAS ROYER, AND WHAT DID HE DESIGN?

In December 1954 the paper “Transistors as On-Off Switches in Saturable-Core Circuits” appeared in *Electrical Manufacturing*. George H. Royer, one of the authors, described a “d-c to a-c converter” as part of this paper. Using Westinghouse 2N74 transistors, Royer reported 90% efficiency for his circuit. The operation of Royer’s circuit is well described in this paper. The Royer converter was widely adopted, and used in designs from watts to kilowatts. It is still the basis for a wide variety of power conversion.

Royer’s circuit is not an LC resonant type. The transformer is the sole energy storage element and the output is a square wave. Figure I1 is a conceptual schematic of a typical converter. The input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure I2, Traces A and C are Q1’s collector and base, while Traces B and D are Q2’s collector and base) each time the transformer saturates. Transformer saturation causes a quickly rising, high current to flow (Trace E).

This current spike, picked up by the base drive winding, switches the transistors. This phase opposed switching causes the transistors to exchange states. Current abruptly drops in the formerly conducting transistor and then slowly rises in the newly conducting transistor until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%.

Photograph I3 is a time and amplitude expansion of I2's Traces B and E. It clearly shows the relationship between transformer current (Trace B, Figure I3) and transistor collector voltage (Trace A, Figure I3).¹

Note 1: The bottom traces in both photographs are not germane and are not referenced in the discussion.

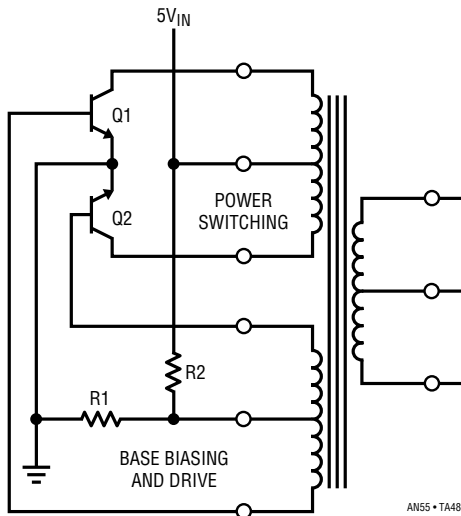


Figure I1. Conceptual Classic Royer Converter. Transformer Approaching Saturation Causes Switching

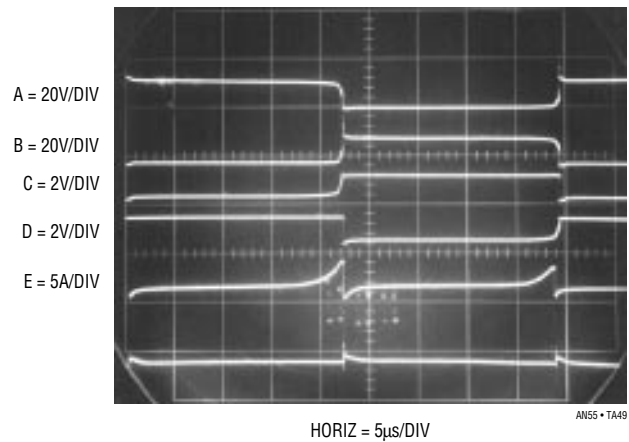


Figure I2. Waveforms for the Classic Royer Circuit

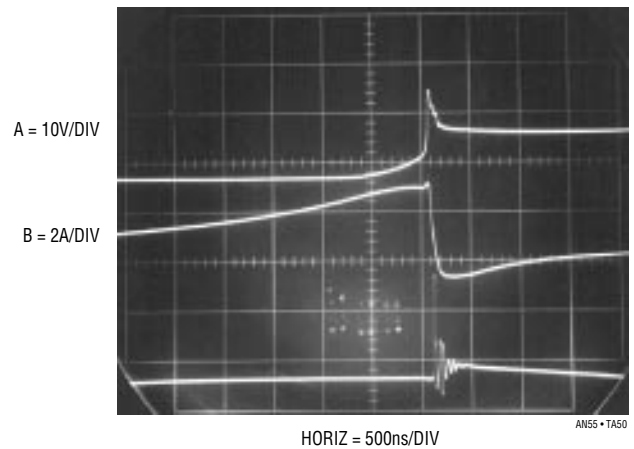


Figure I3. Detail of Transistor Switching. Turn-Off (Trace A) Occurs Just as Transformer Heads into Saturation (Trace B)

APPENDIX J

A LOT OF CUT-OFF EARS AND NO VAN GOGHS

Some Not-So-Great Ideas

The hunt for a practical CCFL power supply covered (and is still covering) a lot of territory. The wide range of conflicting requirements combined with ill-defined lamp characteristics produces plenty of unpleasant surprises. This section presents a selection of ideas that turned into disappointing breadboards. Backlight circuits are one of the deadliest places for theoretically interesting circuits the author has ever encountered.

Not-So-Great Backlight Circuits

Figure J1 seeks to boost efficiency by eliminating the LT1172's saturation loss. Comparator C1 controls a free running loop around the Royer by on-off modulation of transistor base drive. The circuit delivers bursts of high voltage sine drive to the lamp to maintain the feedback node. The scheme worked, but had poor line rejection due to the varying waveform vs supply seen by the RC averaging pair. Also, the "burst" modulation forces the loop to

Application Note 55

constantly restart the lamp at the burst rate, wasting energy. Finally, lamp power is delivered by a high crest factor waveform, causing inefficient current-to-light conversion in the lamp.

Figure J2 attempts to deal with some of these issues. It converts the previous circuit to an amplifier controlled current mode regulator. Also, the Royer base drive is controlled by a clocked, high frequency pulse width modulator. This arrangement provides a more regular waveform to the averaging RC, improving line rejection. Unfortunately, the improvement was not adequate. 1% line rejection is required to avoid annoying flicker when the line moves abruptly, such as when a charger is activated. Another difficulty is that, although reduced by the higher frequency PWM, crest factor is still non-optimal. Finally, the lamp is still forced to restart at each PWM cycle, wasting power.

Figure J3 adds a “keep alive” function to prevent the Royer from turning off. This aspect worked well. When the PWM

goes low the Royer is kept running, maintaining low level lamp conduction. This eliminates the continuous lamp restarting, saving power. The “supply correction” block feeds a portion of the supply into the RC averager, improving line rejection to acceptable levels.

This circuit, after considerable fiddling, achieved almost 94% efficiency but produced less output light than a “less efficient” version of text Figure 6! The villain is lamp waveform crest factor. The keep alive circuit helps, but the lamp still cannot handle even moderate crest factors.

Figure J4 is a very different approach. This circuit is a driven square wave converter. The resonating capacitor is eliminated. The base drive generator shapes the edges, minimizing harmonics for low noise operation. This circuit works well, but relatively low operating frequencies are required to get good efficiency. This is so because the sloped drive must be a small percentage of the fundamental to maintain low losses. This mandates relatively large magnetics—a crucial disadvantage. Also, square waves

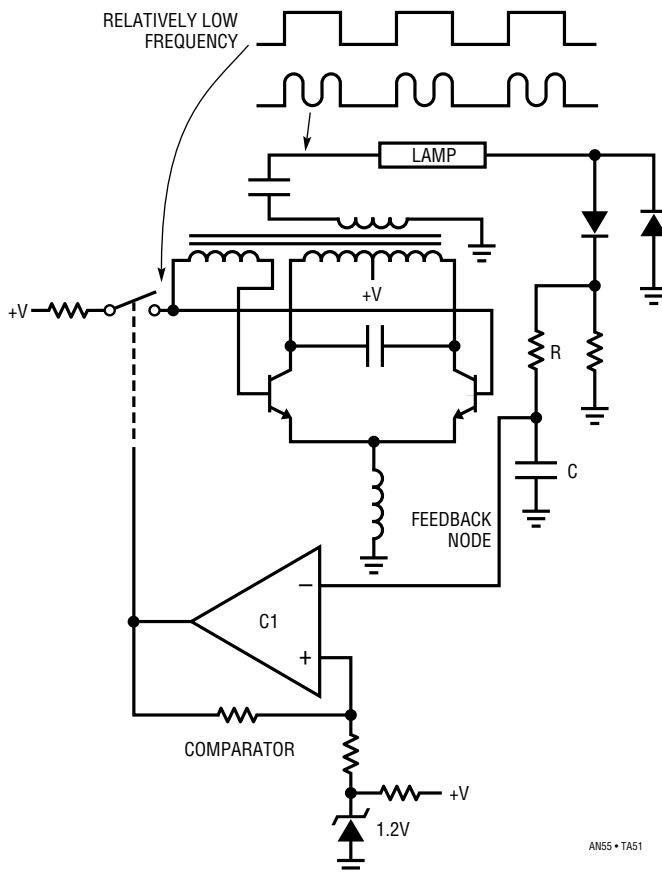


Figure J1. A First Attempt at Improving the Basic Circuit. Irregular Royer Drive Promotes Losses and Poor Regulation

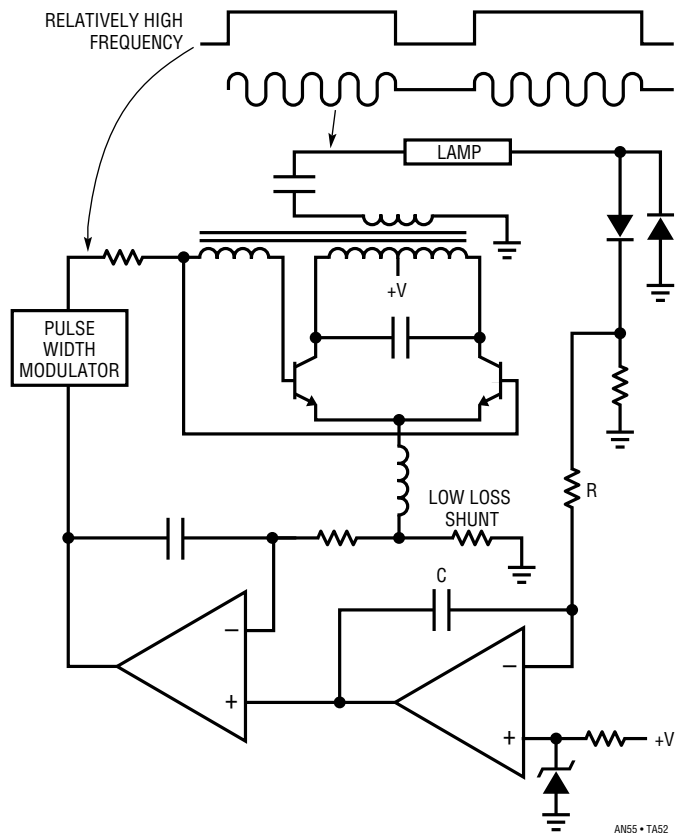


Figure J2. A more Sophisticated Failure Still has Losses and Poor Line Regulation

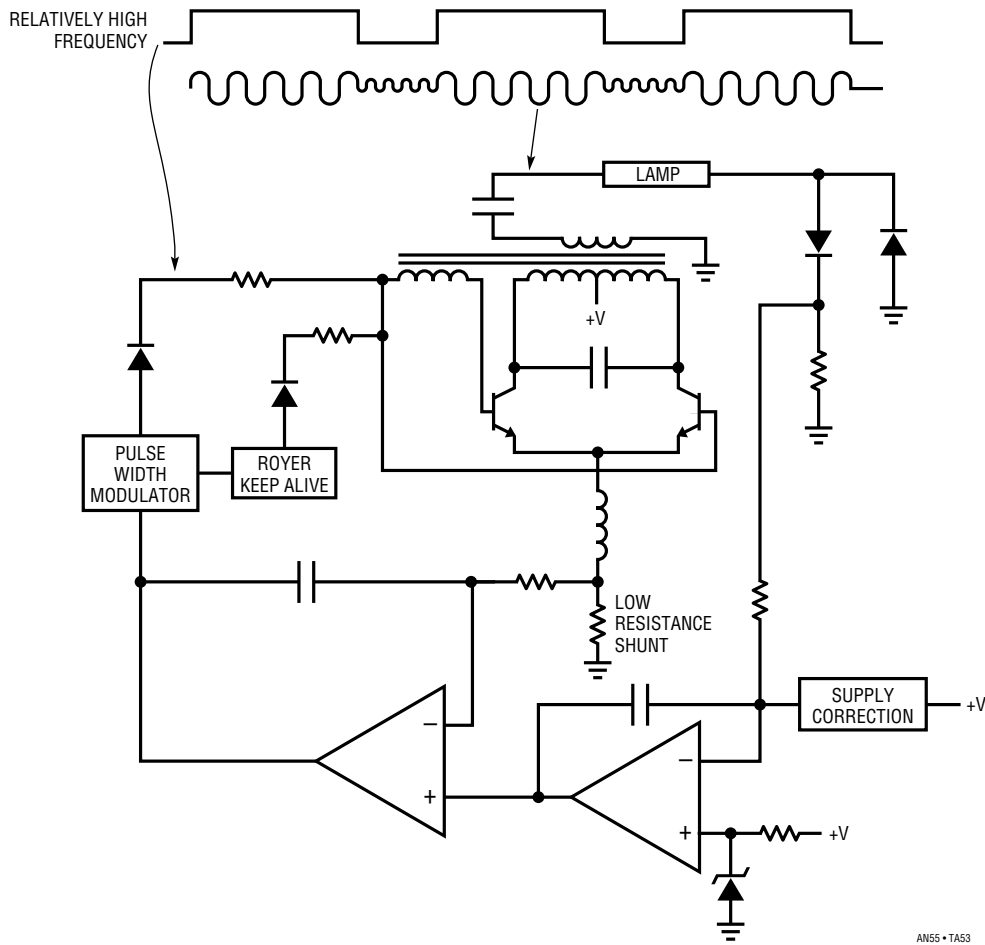


Figure J3. “Keep Alive” Circuit Eliminates Turn-On Losses and has 94% Efficiency. Light Emission is Lower than “Less Efficient” Circuits

have different crest factor and rise time than sines, forcing inefficient lamp transduction.

Not-So-Great Primary Side Sensing Ideas

Text Figures 28 and 29 use primary side current sensing to control lamp intensity. This permits the lamp to fully float, extending its dynamic operating range. A number of primary side sensing approaches were tried before the “top side sense” won the contest.

J5’s ground referred current sensing is the most obvious way to detect Royer current. It offers the advantage of simple signal conditioning—there is no common mode voltage. The assumption that essentially all Royer current derives from the LT1172 emitter pin path is true. Also true, however, is that the waveshape of this path’s current varies widely with input voltage and lamp operating current. The RMS voltage across the shunt (e.g., the Royer

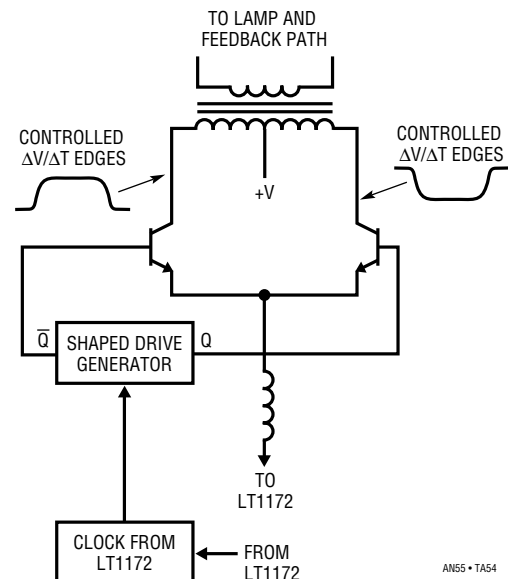


Figure J4. A Non-Resonant Approach. Slew Retarded Edges Minimize Harmonics, but Transformer Size Goes Up. Output Waveform is also Non-Optimal, Causing Lamp Losses

Application Note 55

current) is unaffected by this, but the simple RC averager produces different outputs for the various waveforms. This causes this approach to have very poor line rejection, rendering it impractical. J6 senses inductor flux, which should correlate with Royer current. This approach promises attractive simplicity. It gives better line regulation but still has some trouble giving reliable feedback as wave-shape changes. Also, in keeping with most flux sampling schemes, it regulates poorly under low current conditions.

Figure J7 senses flux in the transformer. This takes advantage of the transformer's more regular waveform. Line regulation is reasonably good because of this, but low current regulation is still poor. J8 samples Royer collector voltage capacitively, but the feedback signal does not accurately represent start-up, transient and low current conditions.

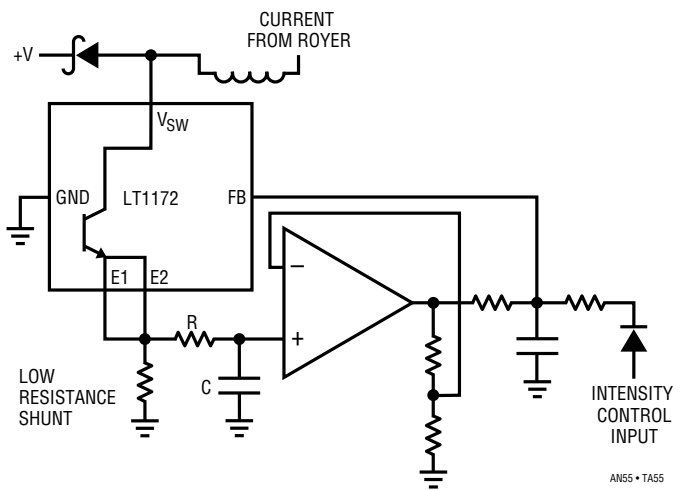


Figure J5. "Bottom Side" Current Sensing has Poor Line Regulation due to RC Averaging Characteristics

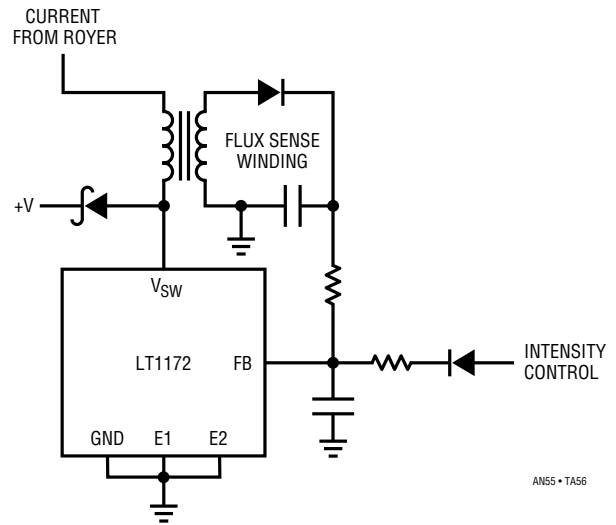


Figure J6. Flux Sensing has Irregular Outputs, Particularly at Low Currents

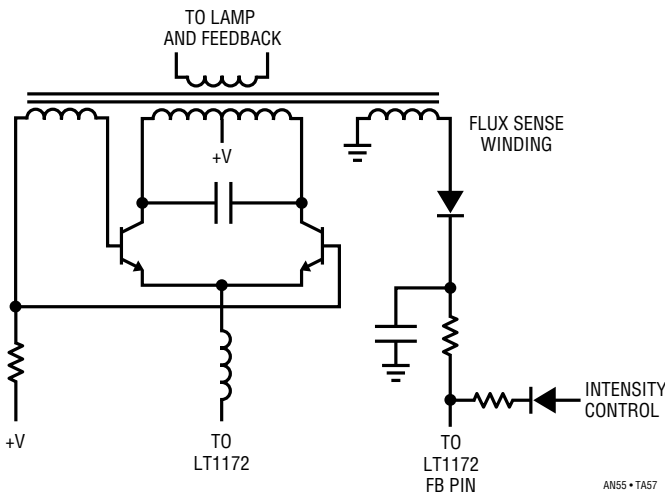


Figure J7. Transformer Flux Sensing Gives More Regular Feedback, but Not at Low Currents

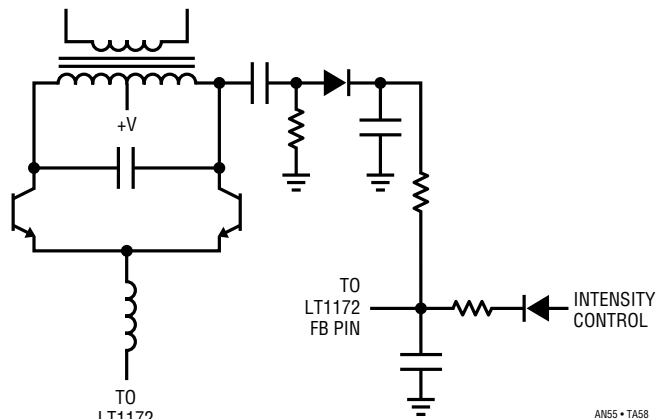


Figure J8. AC Coupled Drive Waveform Feedback is Not Reliable at Low Currents

APPENDIX K

PERSPECTIVES ON EFFICIENCY

The LCD displays currently available require two power sources, a backlight supply and a contrast supply. The display backlight is the single largest power consumer in a typical portable apparatus, accounting for almost 50% of battery drain with the display at maximum intensity. As such, every effort must be expended to maximize backlight efficiency.

The backlight presents a cascaded energy attenuator to the battery (Figure K1). Battery energy is lost in the electrical-to-electrical conversion to high voltage AC to drive the cold cathode fluorescent lamp (CCFL). This section of the energy attenuator is the most efficient; conversion efficiencies exceeding 90% are possible. The CCFL, although the most efficient electrical-to-light converter available today, has losses exceeding 80%. Additionally, the optical transmission efficiency of present displays is under 10% for monochrome, with color types

much lower. Clearly, overall backlight efficiency improvements must come from lamp and display improvements.

Higher CCFL circuit efficiency does, however, directly translate into increased operating time. For comparison purposes text Figure 8's circuit was installed in a Toshiba Model 2200 running 5mA lamp current. The result was a 19 minute increase in operating time.

Relatively small reductions in backlight intensity can greatly extend battery life. A 20% reduction in screen intensity results in nearly 30 minutes additional running time. This assumes that efficiency remains reasonably flat as power is reduced. Figure K2 shows that the circuits presented do reasonably well in this regard, as opposed to other approaches.

The contrast supply, operating at greatly reduced power, is not a major source of loss.

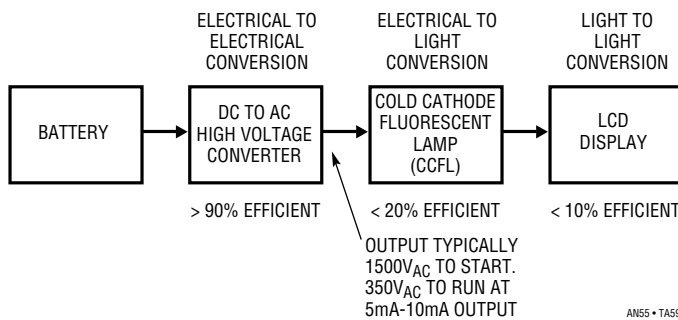


Figure K1. The Backlit LCD Display Presents a Cascaded Energy Attenuator to the Battery. DC to AC Conversion is Significantly more Efficient than Energy Conversions in Lamp and Display

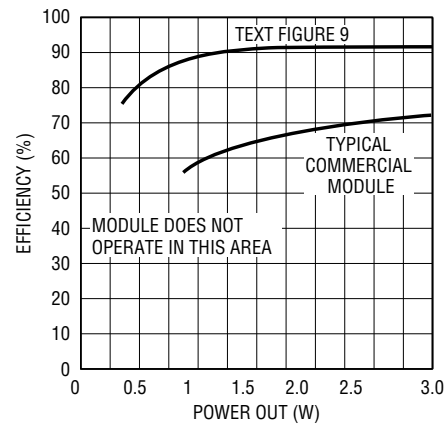


Figure K2. Efficiency Comparison Between Text Figure 9 and a Typical Modular Converter

HELP SUPPORT MY EDUCATION.
CALL MY DAD ABOUT
YOUR BACKLIGHT APPLICATION.



Wow
93

Practical Circuitry for Measurement and Control Problems

Circuits Designed for a Cruel and Unyielding World

Jim Williams

INTRODUCTION

This collection of circuits was worked out between June 1991 and July of 1994. Most were designed at customer request or are derivatives of such efforts. All represent substantial effort and, as such, are disseminated here for wider study and (hopefully) use.¹ The examples are roughly arranged in categories including power conversion, transducer signal conditioning, amplifiers and signal generators. As always, reader comment and questions concerning variants of the circuits shown may be addressed directly to the author.

Clock Synchronized Switching Regulator

Gated oscillator type switching regulators permit high efficiency over extended ranges of output current. These regulators achieve this desirable characteristic by using a gated oscillator architecture instead of a clocked pulse width modulator. This eliminates the “housekeeping” cur-

rents associated with the continuous operation of fixed frequency designs. Gated oscillator regulators simply self-clock at whatever frequency is required to maintain the output voltage. Typically, loop oscillation frequency ranges from a few hertz into the kilohertz region, depending upon the load.

In most cases this asynchronous, variable frequency operation does not create problems. Some systems, however, are sensitive to this characteristic. Figure 1 slightly modifies a gated oscillator type switching regulator by synchronizing its loop oscillation frequency to the systems clock. In this fashion the oscillation frequency and its attendant switching noise, albeit variable, become coherent with system operation.

Note 1: “Study” is certainly a noble pursuit but we never fail to emphasize use.

LT and LTC are registered trademarks and LT is a trademark of Linear Technology Corporation.

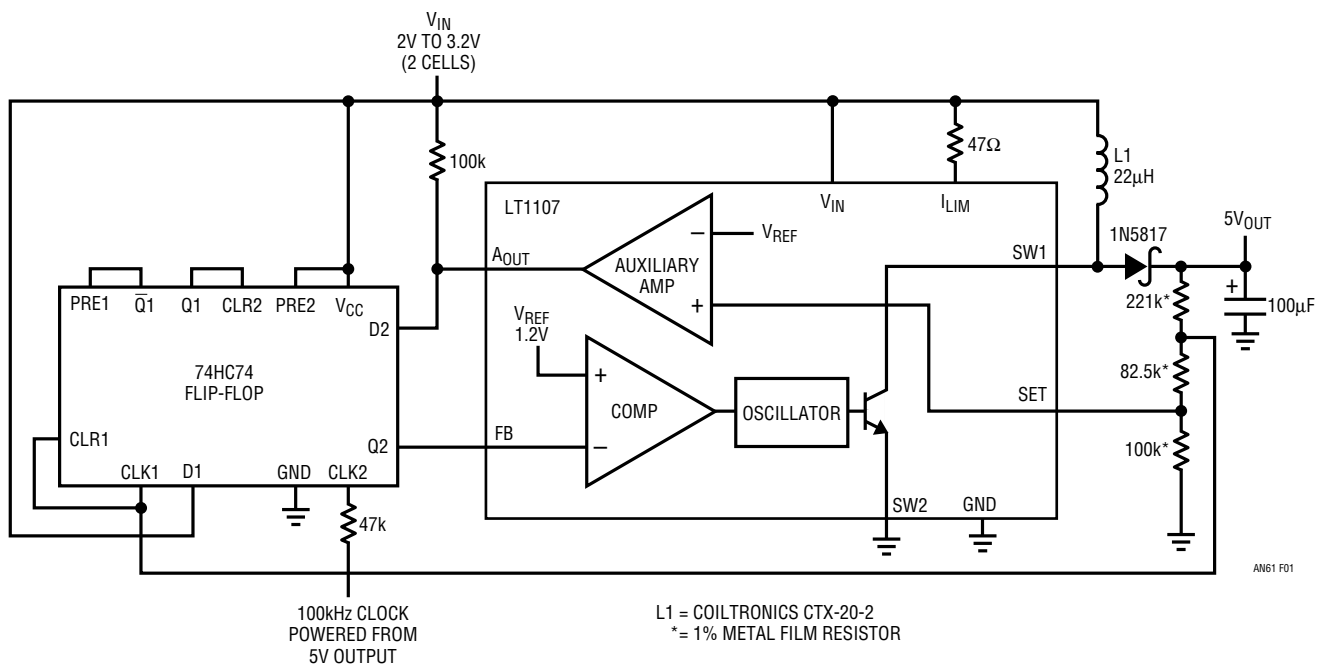


Figure 1. A Synchronizing Flip-Flop Forces Switching Regulator Noise to Be Coherent with the Clock

Application Note 61

Circuit operation is best understood by temporarily ignoring the flip-flop and assuming the LT1107 regulator's A_{OUT} and FB pins are connected. When the output voltage decays the set pin drops below V_{REF}, causing A_{OUT} to fall. This causes the internal comparator to switch high, biasing the oscillator and output transistor into conduction. L1 receives pulsed drive, and its flyback events are deposited into the 100µF capacitor via the diode, restoring output voltage. This overdrives the set pin, causing the IC to switch off until another cycle is required. The frequency of this oscillatory cycle is load dependent and variable. If, as shown, a flip-flop is interposed in the A_{OUT}-FB pin path, synchronization to a system clock results. When the output decays far enough (trace A, Figure 2) the A_{OUT} pin (trace B) goes low. At the next clock pulse (trace C) the flip-flop Q2 output (trace D) sets low, biasing the comparator-oscillator. This turns on the power switch (V_{SW} pin is trace E), which pulses L1. L1 responds in flyback fashion, depositing its energy into the output capacitor to maintain output voltage. This operation is similar to the previously described case, except that the sequence is forced to synchronize with the system clock by the flip-flops action. Although the resulting loops oscillation frequency is variable it, and all attendant switching noise, is synchronous and coherent with the system clock.

A start-up sequence is required because this circuit's clock is powered from its output. The start-up circuitry was developed by Sean Gold and Steve Pietkiewicz of LTC. The flip-flop's remaining section is connected as a buffer.

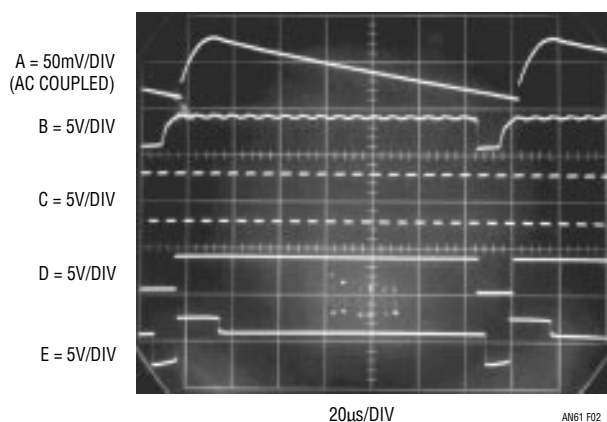


Figure 2. Waveforms for the Clock Synchronized Switching Regulator. Regulator Only Switches (Trace E) on Clock Transitions (Trace C), Resulting in Clock Coherent Output Noise (Trace A)

The CLR1-CLK1 line monitors output voltage via the resistor string. When power is applied Q1 sets CLR2 low. This permits the LT1107 to switch, raising output voltage. When the output goes high enough Q1 sets CLR2 high and normal loop operation commences.

The circuit shown is a step-up type, although any switching regulator configuration can utilize this synchronous technique.

High Power 1.5V to 5V Converter

Some 1.5V powered systems (survival 2-way radios, remote, transducer-fed data acquisition systems, etc.) require much more power than stand-alone IC regulators can provide. Figure 3's design supplies a 5V output with 200mA capacity.

The circuit is essentially a flyback regulator. The LT1170 switching regulator's low saturation losses and ease of use permit high power operation and design simplicity. Unfortunately this device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible, but requires some form of start-up

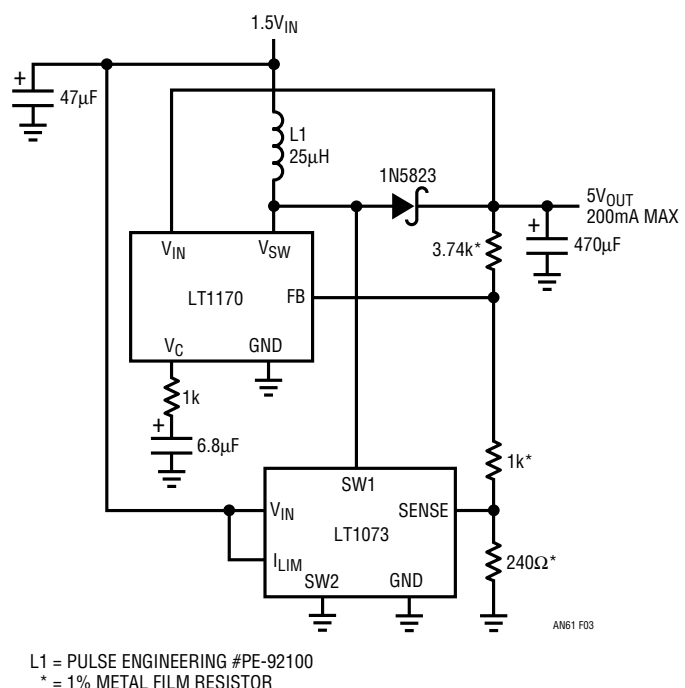


Figure 3. 200mA Output 1.5V to 5V Converter. Lower Voltage LT1073 Provides Bootstrap Start-Up for LT1170 High Power Switching Regulator

mechanism. The 1.5V powered LT1073 switching regulator forms a start-up loop. When power is applied the LT1073 runs, causing its V_{SW} pin to periodically pull current through L1. L1 responds with high voltage flyback events. These events are rectified and stored in the 470 μ F capacitor, producing the circuit's DC output. The output divider string is set up so the LT1073 turns off when circuit output crosses about 4.5V. Under these conditions the LT1073 obviously can no longer drive L1, but the LT1170 can. When the start-up circuit goes off, the LT1170 V_{IN} pin has adequate supply voltage and can operate. There is some overlap between start-up loop turn-off and LT1170 turn-on, but it has no detrimental effect.

The start-up loop must function over a wide range of loads and battery voltages. Start-up currents approach 1A, necessitating attention to the LT1073's saturation and drive characteristics. The worst case is a nearly depleted battery and heavy output loading.

Figure 4 plots input-output characteristics for the circuit. Note that the circuit will start into all loads with $V_{BAT} = 1.2V$. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive full 200mA loads down to $V_{BAT} = 1.0V$. Reduced drive is possible down to $V_{BAT} = 0.6V$ (a very dead battery)! Figure 5 graphs efficiency at two supply voltages over a range of output currents. Performance is attractive, although at lower currents circuit quiescent power degrades efficiency. Fixed junction saturation losses are responsible for lower overall efficiency at the lower supply voltage.

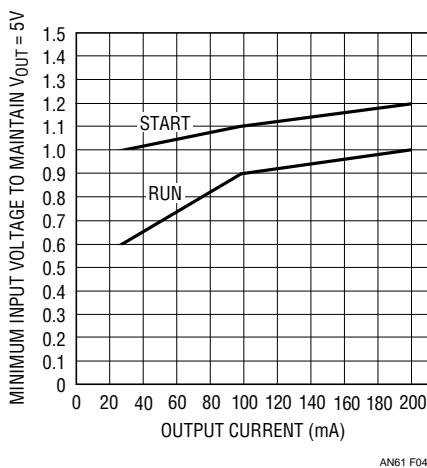


Figure 4. Input-Output Data for the 1.5V to 5V Converter Shows Extremely Wide Start-Up and Running Range into Full Load

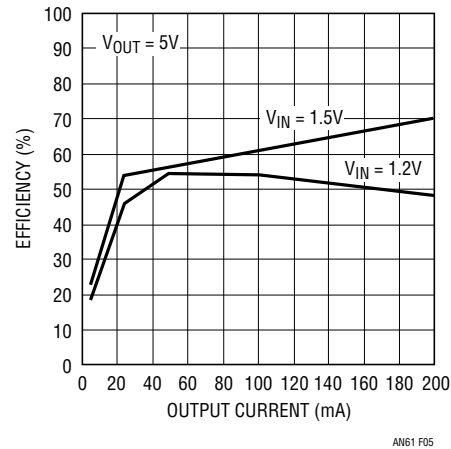


Figure 5. Efficiency vs Operating Point for the 1.5V to 5V Converter. Efficiency Suffers at Low Power Because of Relatively High Quiescent Currents

Low Power 1.5V to 5V Converter

Figure 6, essentially the same approach as the preceding circuit, was developed by Steve Pietkiewicz of LTC. It is limited to about 150mA output with commensurate restrictions on start-up current. Its advantage, good efficiency at relatively low output currents, derives from its low quiescent power consumption.

The LT1073 provides circuit start-up. When output voltage, sensed by the LT1073's "set" input via the resistor divider, rises high enough Q1 turns on, enabling the LT1302. This device sees adequate operating voltage and responds by driving the output to 5V, satisfying its feedback node. The 5V output also causes enough overdrive at the LT1073 feedback pin to shut the device down.

Figure 7 shows maximum permissible load currents for start-up and running conditions. Performance is quite good, although the circuit clearly cannot compete with the previous design. The fundamental difference between the two circuits is the LT1170's (Figure 3) much larger power switch, which is responsible for the higher available power. Figure 8, however, reveals another difference. The curves show that Figure 6 is significantly more efficient than the LT1170 based approach at output currents below 100mA. This highly desirable characteristic is due to the LT1302's much lower quiescent operating currents.

Application Note 61

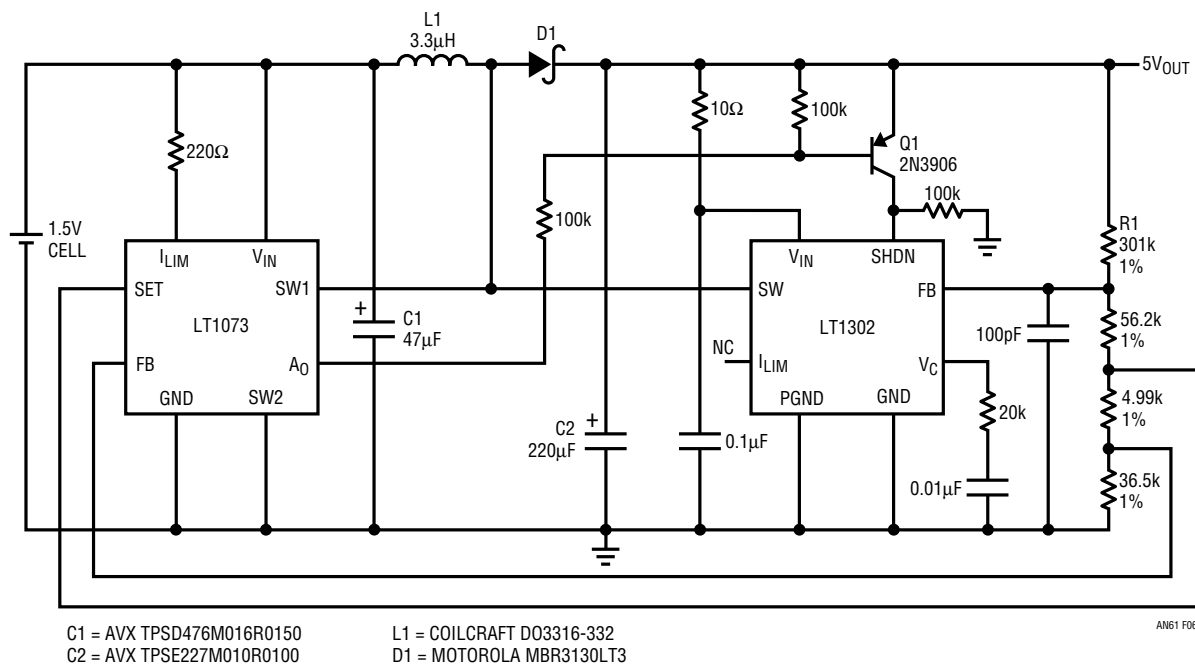


Figure 6. Single-Cell to 5V Converter Delivers 150mA with Good Efficiency at Lower Currents

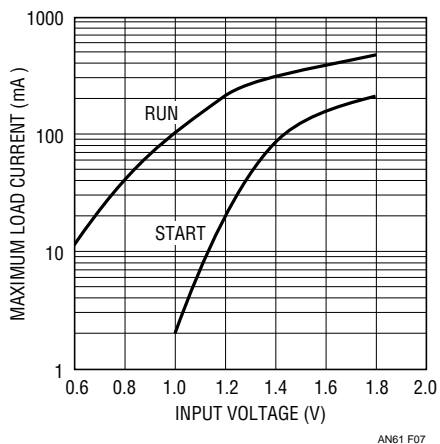


Figure 7. Maximum Permissible Loads for Start-Up and Running Conditions. Allowable Load Current During Start-Up Is Substantially Less Than Maximum Running Current.

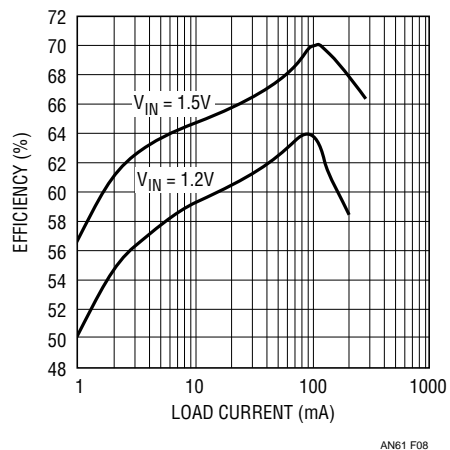


Figure 8. Efficiency Plot for Figure 6. Performance Is Better Than the Previous Circuit at Lower Currents, Although Poorer at High Power

Low Power, Low Voltage Cold Cathode Fluorescent Lamp Power Supply

Most Cold Cathode Fluorescent Lamp (CCFL) circuits require an input supply of 5V to 30V and are optimized for bulb currents of 5mA or more. This precludes lower power operation from 2- or 3-cell batteries often used in palmtop computers and portable apparatus. A CCFL power supply that operates from 2V to 6V is detailed in Figure 9. This circuit, contributed by Steve Pietkiewicz of LTC, can drive a small CCFL over a 100 μ A to 2mA range.

The circuit uses an LT1301 micropower DC/DC converter IC in conjunction with a current driven Royer class converter comprised of T1, Q1 and Q2. When power and intensity adjust voltage are applied the LT1301's I_{LIM} pin is driven slightly positive, causing maximum switching current through the IC's internal switch pin (SW). Current flows from T1's center tap, through the transistors, into L1. L1's current is deposited in switched fashion to ground by the regulator's action.

The Royer converter oscillates at a frequency primarily set by T1's characteristics (including its load) and the 0.068 μ F capacitor. LT1301 driven L1 sets the magnitude of the Q1-Q2 tail current, hence T1's drive level. The 1N5817 diode maintains L1's current flow when the LT1301's switch is off. The 0.068 μ F capacitor combines with T1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors. T1 furnishes voltage step-up and about 1400Vp-p appears at its secondary. Alternating current flows through the 22pF capacitor into the lamp. On positive half-cycles the lamp's current is steered to ground via D1. On negative half-cycles the lamp's current flows through Q3's collector and is filtered by C1. The LT1301's I_{LIM} pin acts as a 0V summing point with about 25 μ A bias current flowing out of the pin into C1. The LT1301 regulates L1's current to equalize Q3's average collector current, representing 1/2 the lamp current, and R1's current, represented by V_A/R1. C1 smooths all current flow to DC.

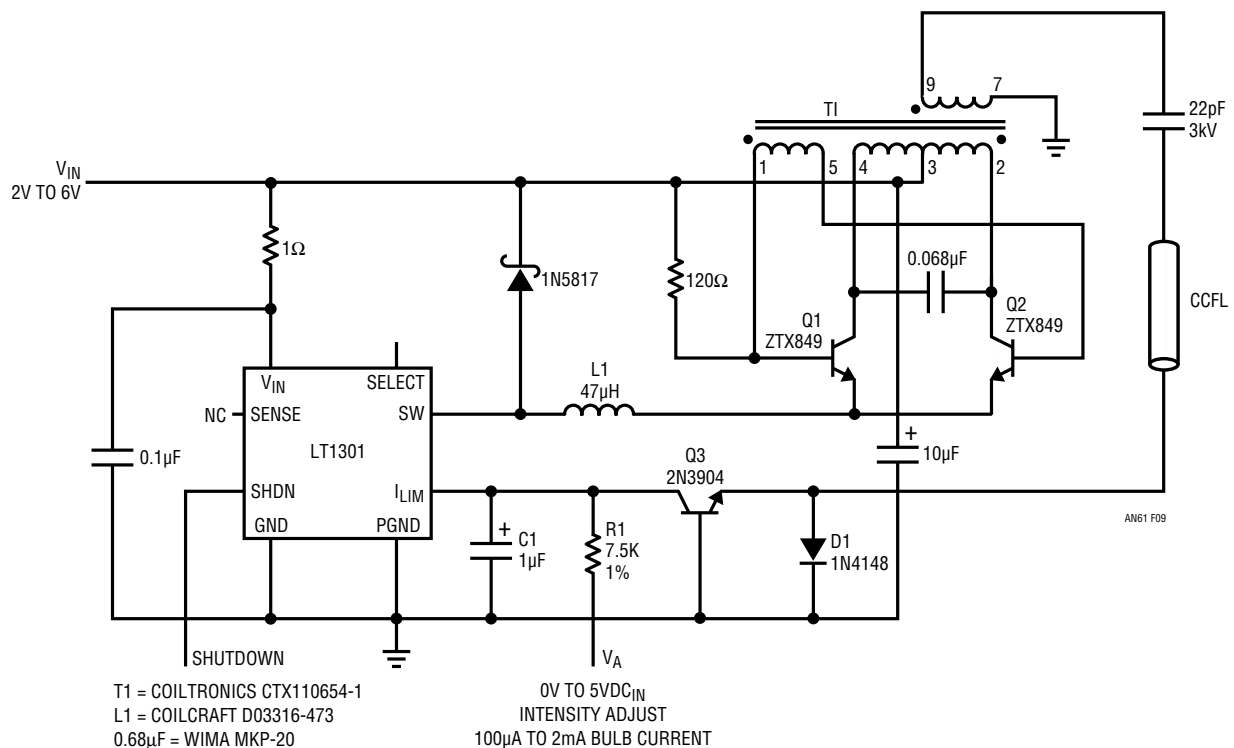


Figure 9. Low Power Cold Cathode Fluorescent Lamp Supply Is Optimized for Low Voltage Inputs and Small Lamps

Application Note 61

Circuit efficiency ranges from 80% to 88% at full load, depending on line voltage. Current mode operation combined with the Royer's consistent waveshape vs input results in excellent line rejection. The circuit has none of the line rejection problems attributable to the hysteretic voltage control loops typically found in low voltage micropower DC/DC converters. This is an especially desirable characteristic for CCFL control, where lamp intensity must remain constant with shifts in line voltage. Interaction between the Royer converter, the lamp and the regulation loop is far more complex than might be supposed, and subject to a variety of considerations. For detailed discussion see Reference 3.

Low Voltage Powered LCD Contrast Supply

Figure 10, a companion to the CCFL power supply previously described, is a contrast supply for LCD panels. It was designed by Steve Pietkiewicz of LTC. The circuit is noteworthy because it operates from a 1.8V to 6V input, significantly lower than most designs. In operation the LT1300/LT1301 switching regulator drives T1 in flyback

fashion, causing negative biased step-up at T1's secondary. D1 provides rectification, and C1 smooths the output to DC. The resistively divided output is compared to a command input, which may be DC or PWM, by the IC's "I_{LIM}" pin. The IC, forcing the loop to maintain 0V at the I_{LIM} pin, regulates circuit output in proportion to the command input.

Efficiency ranges from 77% to 83% as supply voltage varies from 1.8V to 3V. At the same supply limits, available output current increases from 12mA to 25mA.

HeNe Laser Power Supply

Helium-Neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10kV to start conduction, although they require only about 1500V to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure 11's circuit considerably simplifies driving the laser. The

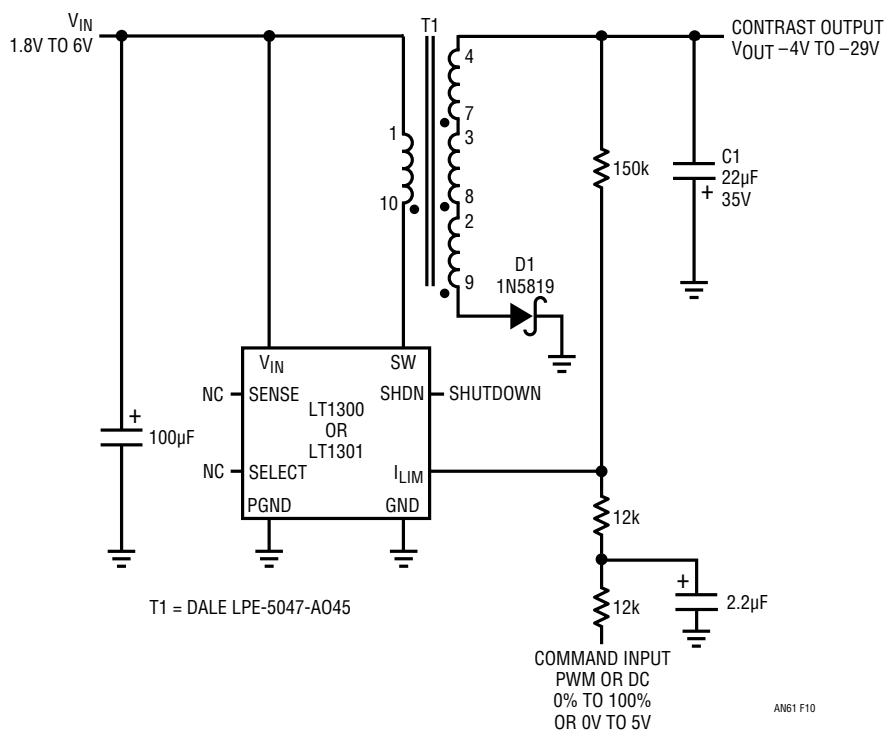


Figure 10. Liquid Crystal Display Contrast Supply Operates from 1.8V to 6V with -4V to -29V Output Range

start-up and sustaining functions have been combined into a single, closed-loop current source with over 10kV of compliance. The circuit is recognizable as a reworked CCFL power supply with a voltage tripled DC output.²

When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47μF capacitor resonates with L1, providing boosted sine wave drive. L1 provides substantial step-up, causing

about 3500V to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10kV across the laser. The laser breaks down and current begins to flow through it. The 47k resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts pulse width drive to L2 to maintain the FB pin at 1.23V, regardless of changes in operating conditions. In this fashion, the laser sees constant current drive,

Note 2: See References 2 and 3 and this text's Figure 9.

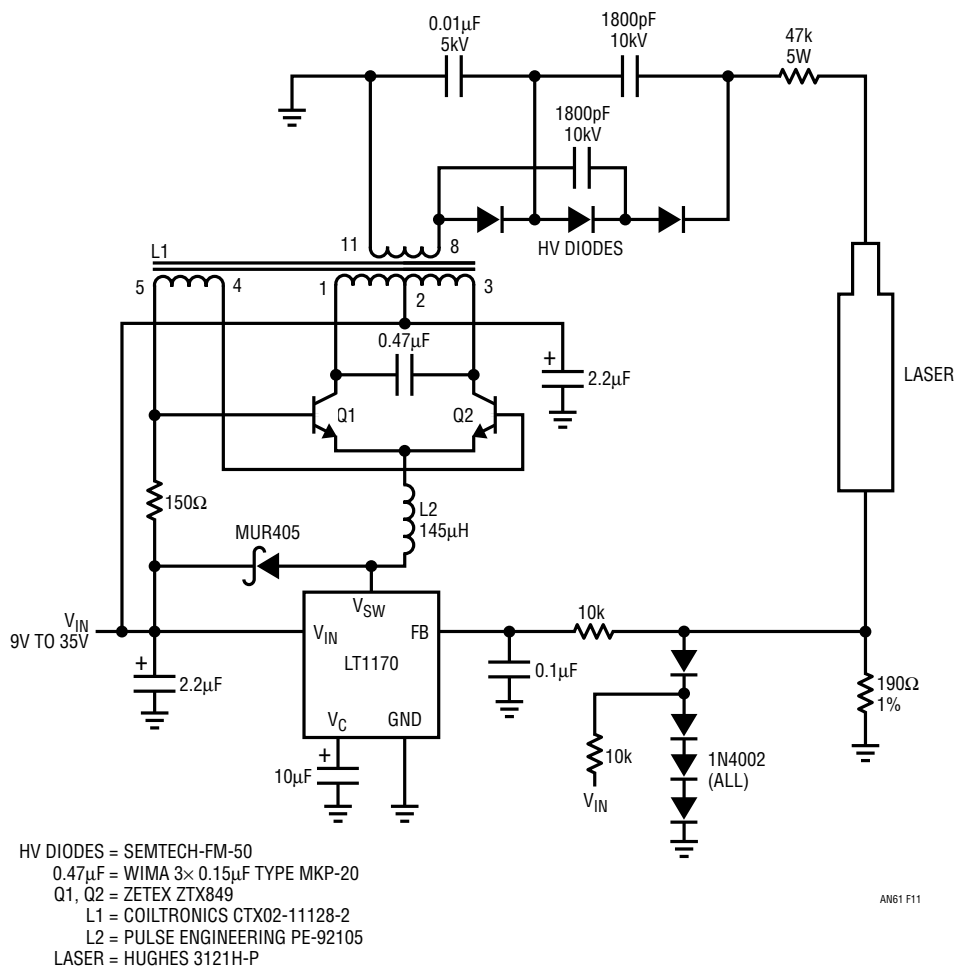


Figure 11. LASER Power Supply Is Essentially A 10,000V Compliance Current Source

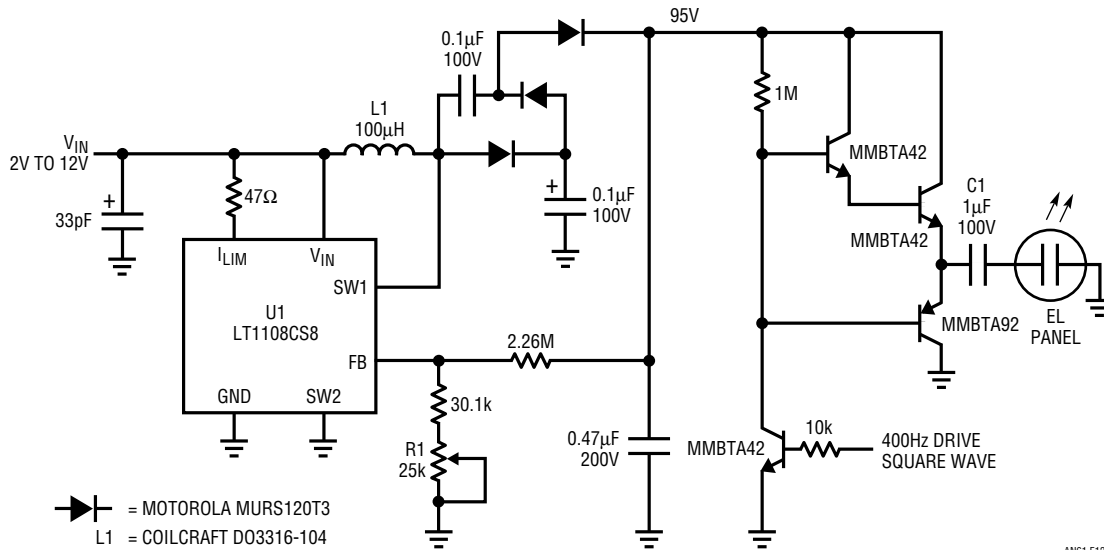
Application Note 61

in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The 10μF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9V to 35V input range with an electrical efficiency of about 80%.

Compact Electroluminescent Panel Power Supply

Electroluminescent (EL) panel LCD backlighting presents an attractive alternative to fluorescent tube (CCFL) backlighting in some portable systems. EL panels are thin, lightweight, lower power, require no diffuser and work at lower voltage than CCFLs. Unfortunately, most EL DC/AC

inverters use a large transformer to generate the 400Hz 95V square wave required to drive the panel. Figure 12's circuit, developed by Steve Pietkiewicz of LTC, eliminates the transformer by employing an LT1108 micropower DC/DC converter IC. The device generates a 95VDC potential via L1 and the diode-capacitor doubler network. The transistors switch the EL panel between 95V and ground. C1 blocks DC and R1 allows intensity adjustment. The 400Hz square wave drive signal can be supplied by the microprocessor or a simple multivibrator. When compared to conventional EL panel supplies, this circuit is noteworthy because it can be built in a square inch with a 0.5 inch height restriction. Additionally, all components are surface mount types, and the usual large and heavy 400Hz transformer is eliminated.



AN61 F12

Figure 12. Switch Mode EL Panel Driver Eliminates Large 400Hz Transformer

3.3V Powered Barometric Pressure Signal Conditioner

The move to 3.3V digital supply voltage creates problems for analog signal conditioning. In particular, transducer based circuits often require higher voltage for proper transducer excitation. DC/DC converters in standard configurations can address this issue but increase power consumption. Figure 13's circuit shows a way to provide proper transducer excitation for a barometric pressure sensor while minimizing power requirements.

The 6kΩ transducer T1 requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1 senses T1's current by monitoring the voltage drop across the resistor string in T1's return path.

A1's output biases the LT1172 switching regulator's operating point, producing a stepped up DC voltage which appears as T1's drive and A2's supply voltage. T1's return current out of pin 6 closes a loop back at A1 which is slaved to the 1.2V reference. This arrangement provides the required high voltage drive ($\approx 10V$) while minimizing power consumption. This is so because the switching regulator produces only enough voltage to satisfy T1's current requirements. Instrumentation amplifier A2 and A3 provide gain and LTC1287 A/D converter gives a 12-bit digital output. A2 is bootstrapped off the transducer supply, enabling it to accept T1's common-mode voltage. Circuit current consumption is about 14mA. If the shutdown pin is driven high the switching regulator turns off, reducing

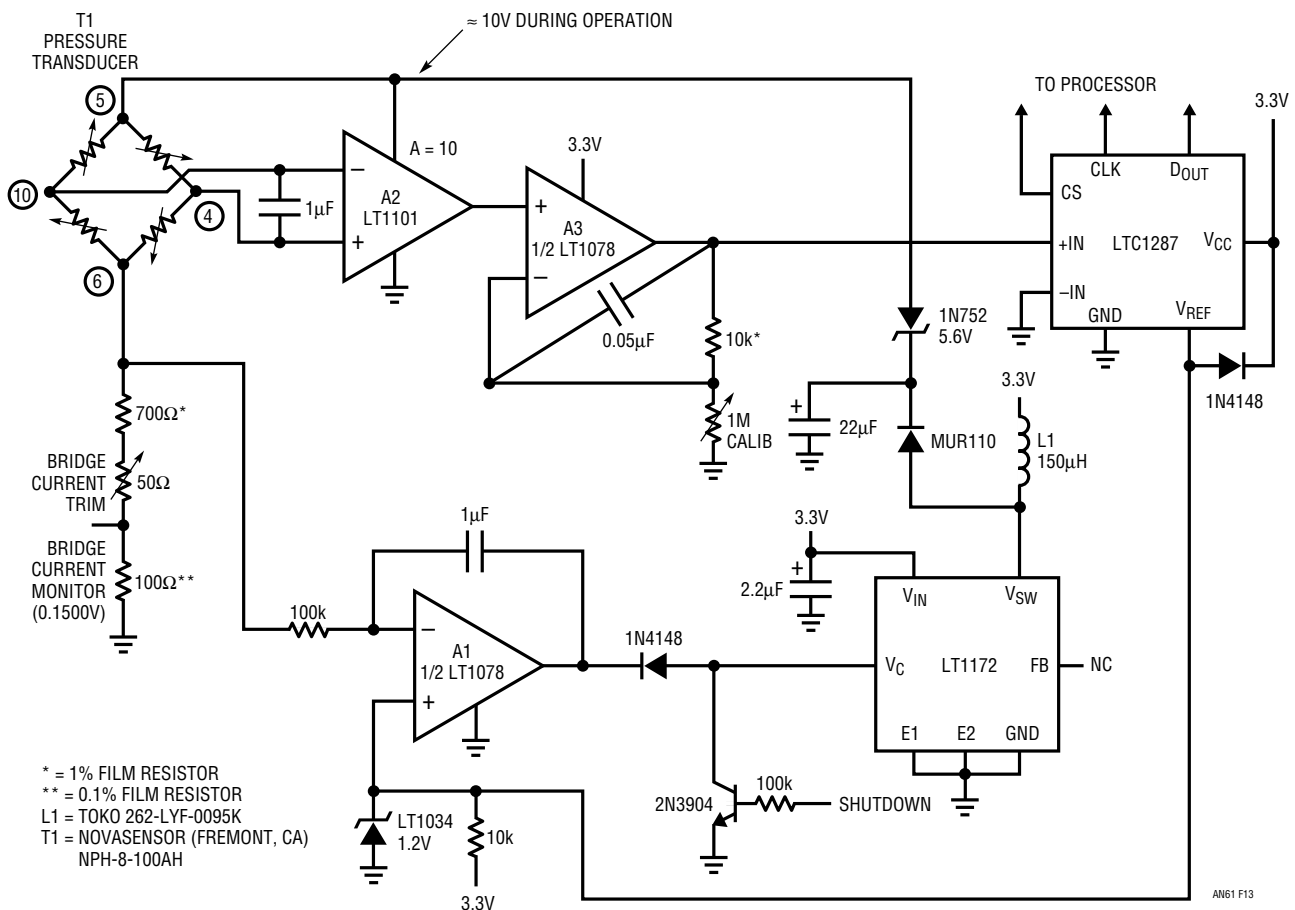


Figure 13. 3.3V Powered, Digital Output, Barometric Pressure Signal Conditioner

Application Note 61

total power consumption to about 1mA. In shutdown the 3.3V powered A/D's output data remains valid. In practice, the circuit provides a 12-bit representation of ambient barometric pressure after calibration. To calibrate, adjust the "bridge current trim" for exactly 0.1500V at the indicated point. This sets T1's current to the manufacturer's specified point. Next, adjust A3's trim so that the digital output corresponds to the known ambient barometric pressure. If a pressure standard is not available the transducer is supplied with individual calibration data, permitting circuit calibration.

Some applications may require operation over a wider supply range and/or a calibrated analog output. Figure 14's circuit is quite similar, except that the A/D converter is eliminated and a 2.7V to 7V supply is acceptable. The calibration procedure is identical, except that A3's analog output is monitored.

Single Cell Barometers

It is possible to power these circuits from a single cell without sacrificing performance. Figure 15, a direct extension of the above approaches, simply substitutes a switching regulator that will run from a single 1.5V battery. In other respects loop action is nearly identical.

Figure 16, also a 1.5V powered design, is related but eliminates the instrumentation amplifier. As before, the 6kΩ transducer T1 requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1's positive input senses T1's current by monitoring the voltage drop across the resistor string in T1's return path. A1's negative input is fixed by the 1.2V LT1034 reference. A1's output biases the 1.5V powered LT1110 switching regulator. The LT1110's switching produces two outputs from L1. Pin 4's rectified and filtered output powers A1 and T1. A1's

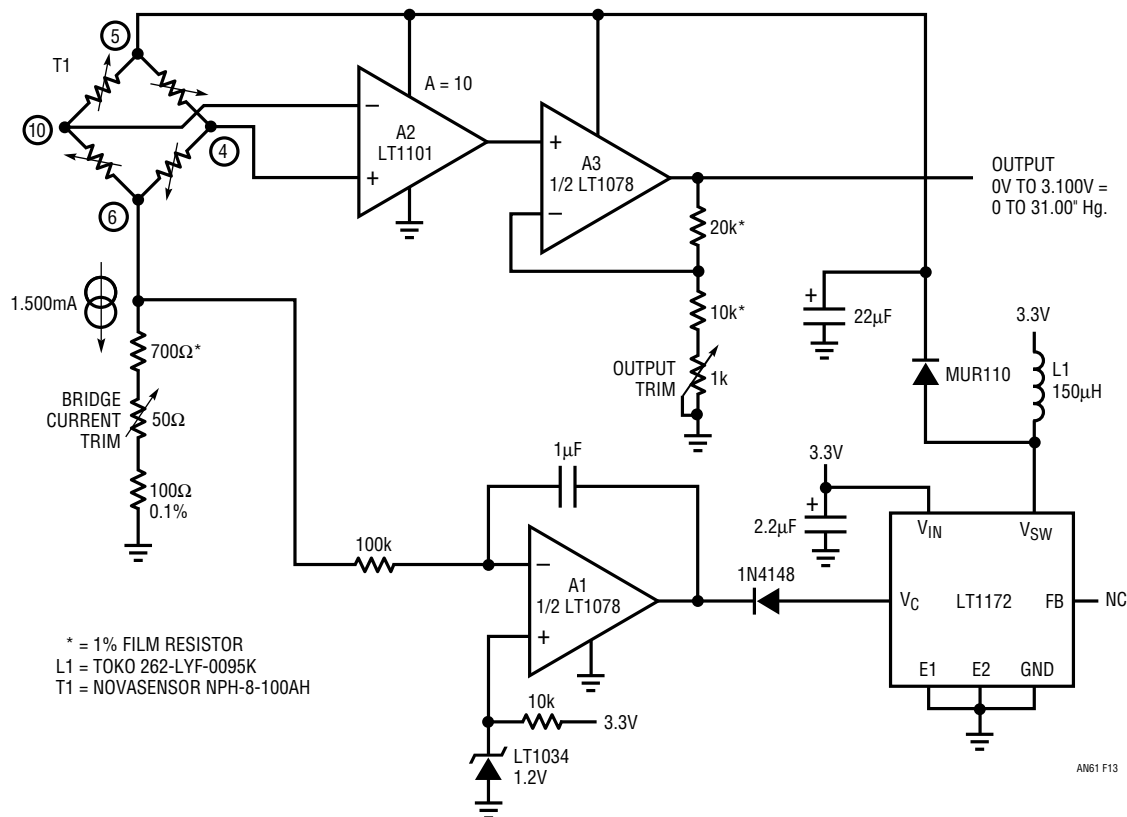


Figure 14. Single Supply Barometric Pressure Signal Conditioner Operates Over a 2.7V to 7V Range

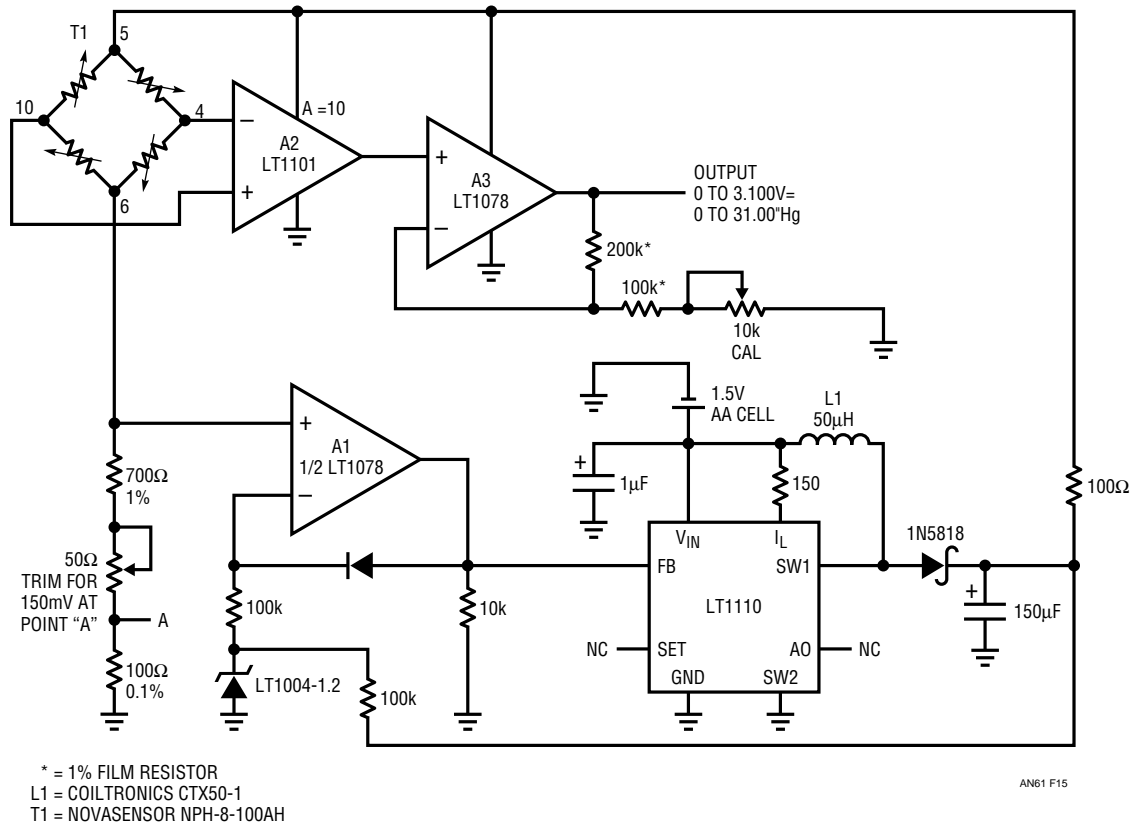


Figure 15. 1.5V Powered Barometric Pressure Signal Conditioner Uses Instrumentation Amplifier and Voltage Boosted Current Loop

output, in turn, closes a feedback loop at the regulator. This loop generates whatever voltage step-up is required to force precisely 1.5mA through T1. This arrangement provides the required high voltage drive while minimizing power consumption. This occurs because the switching regulator produces only enough voltage to satisfy T1's current requirements.

L1 pins 1 and 2 source a boosted, fully floating voltage, which is rectified and filtered. This potential powers A2. Because A2 floats with respect to T1, it can look differentially across T1's outputs, pins 10 and 4. In practice, pin 10 becomes "ground" and A2 measures pin 4's output with respect to this point. A2's gain-scaled output is the circuit's output, conveniently scaled at 3.000V = 30.00"Hg. A2's floating drive eliminates the requirement for an instrumentation amplifier, saving cost, power, space and error contribution.

To calibrate the circuit, adjust R1 for 150mV across the 100Ω resistor in T1's return path. This sets T1's current to the manufacturer's specified calibration point. Next, adjust R2 at a scale factor of 3.000V = 30.00"Hg. If R2 cannot capture the calibration, reselect the 200k resistor in series with it. If a pressure standard is not available, the transducer is supplied with individual calibration data, permitting circuit calibration.

This circuit, compared to a high-order pressure standard, maintained 0.01"Hg accuracy over months with widely varying ambient pressure shifts. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions. Additionally, because 0.01"Hg corresponds to about 10 feet of altitude at sea level, driving over hills and freeway overpasses becomes quite interesting.

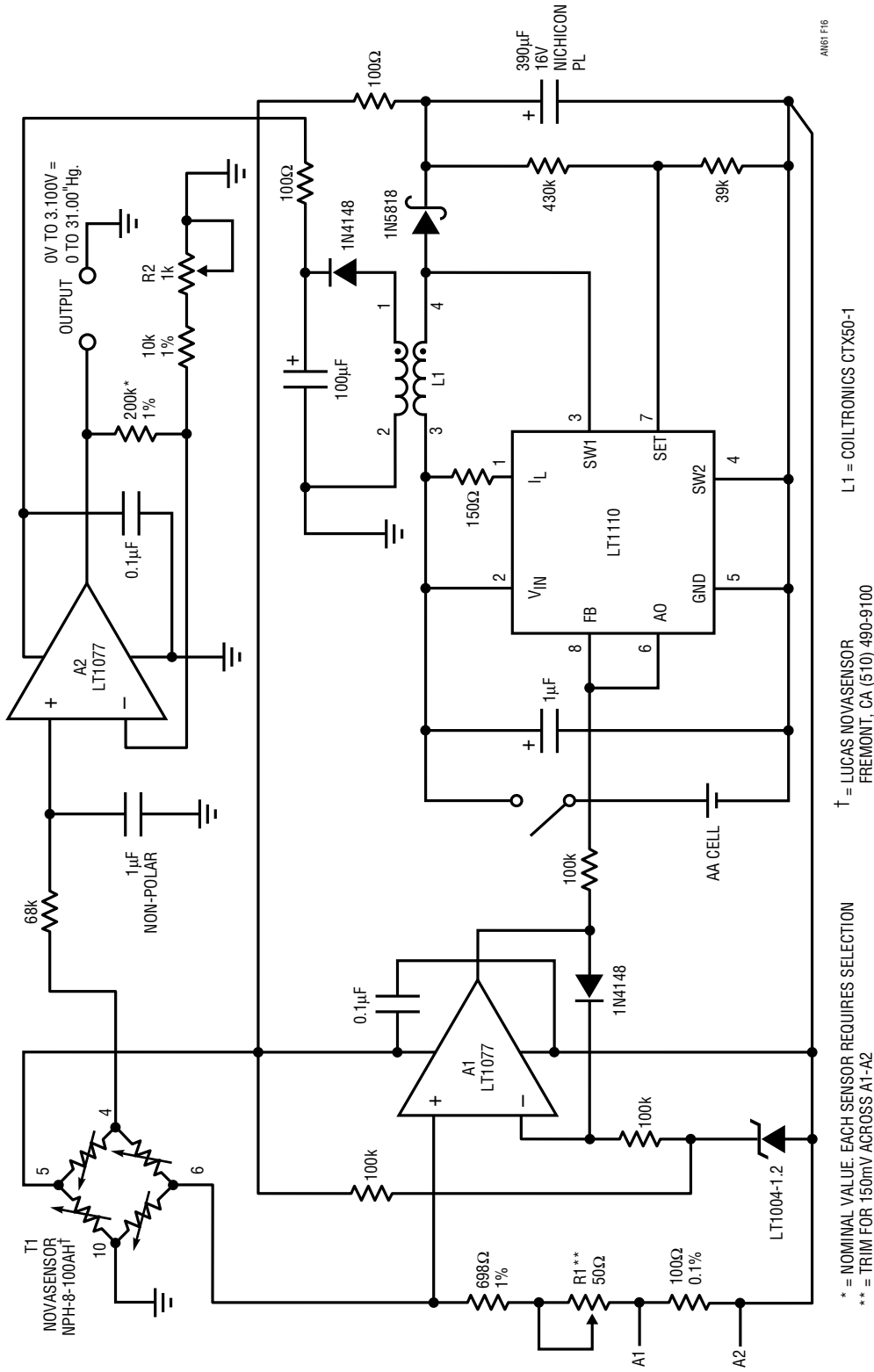


Figure 16. 1.5V Powered Barometric Pressure Signal Conditioner Floats Bridge Drive to Eliminate Instrumentation Amplifier. Voltage Boosted Current Loop Drives Transducer

Until recently, this type of accuracy and stability has only been attainable with bonded strain gauge and capacitively-based transducers, which are quite expensive. As such, semiconductor pressure transducer manufacturers whose products perform at the levels reported are to be applauded. Although high quality semiconductor transducers are still not comparable to more mature technologies, their cost is low and they are vastly improved over earlier devices.

The circuit pulls 14mA from the battery, allowing about 250 hours operation from one D cell.

Quartz Crystal-Based Thermometer

Although quartz crystals have been utilized as temperature sensors (see Reference 5), there has been almost no widespread adaptation of this technology. This is primarily due to the lack of standard product quartz-based temperature sensors. The advantages of quartz-based sensors include simple signal conditioning, good stability and a direct, noise immune digital output almost ideally suited to remote sensing.

Figure 17 utilizes an economical, commercially available (see Reference 6) quartz-based temperature sensor in a thermometer scheme suited to remote data collection.

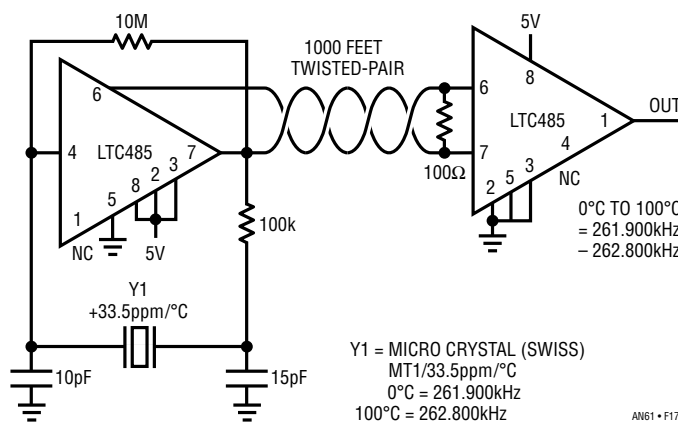


Figure 17. Quartz Crystal Based Circuit Provides Temperature-to-Frequency Conversion. RS485 Transceivers Allow Remote Sensing

The LTC485 RS485 transceiver is set up in the transmit mode. The crystal and discrete components combine with the IC's inverting gain to form a Pierce type oscillator. The LTC485's differential line driving outputs provide frequency coded temperature data to a 1000-foot cable run. A second RS485 transceiver differentially receives the data and presents a single-ended output. Accuracy depends on the grade of quartz sensor specified, with 1°C over 0°C to 100°C achievable.

Ultra-Low Noise and Low Drift Chopped-FET Amplifier

Figure 18's circuit combines the extremely low drift of a chopper-stabilized amplifier with a pair of low noise FETs. The result is an amplifier with 0.05 μ V/°C drift, offset within 5 μ V, 100pA bias current and 50nV noise in a 0.1Hz to 10Hz bandwidth. The noise performance is especially noteworthy; it is almost 35 times better than monolithic chopper-stabilized amplifiers and equals the best bipolar types.

FETs Q1 and Q2 differentially feed A2 to form a simple low noise op amp. Feedback, provided by R1 and R2, sets closed-loop gain (in this case 10,000) in the usual fashion. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1, a chopper-stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1's channel current via Q3 to minimize the difference. Q1's skewed drain values ensure that A1 will be able to capture the offset. A1 and Q3 supply whatever current is required into Q1's channel to force offset within 5 μ V. Additionally, A1's low bias current does not appreciably add to the overall 100pA amplifier bias current. As shown, the amplifier is set up for a noninverting gain of 10,000 although other gains and inverting operation are possible. Figure 19 is a plot of the measured noise performance.

The FETs' V_{GS} can vary over a 4:1 range. Because of this, they must be selected for 10% V_{GS} matching. This matching allows A1 to capture the offset without introducing any significant noise.

Application Note 61

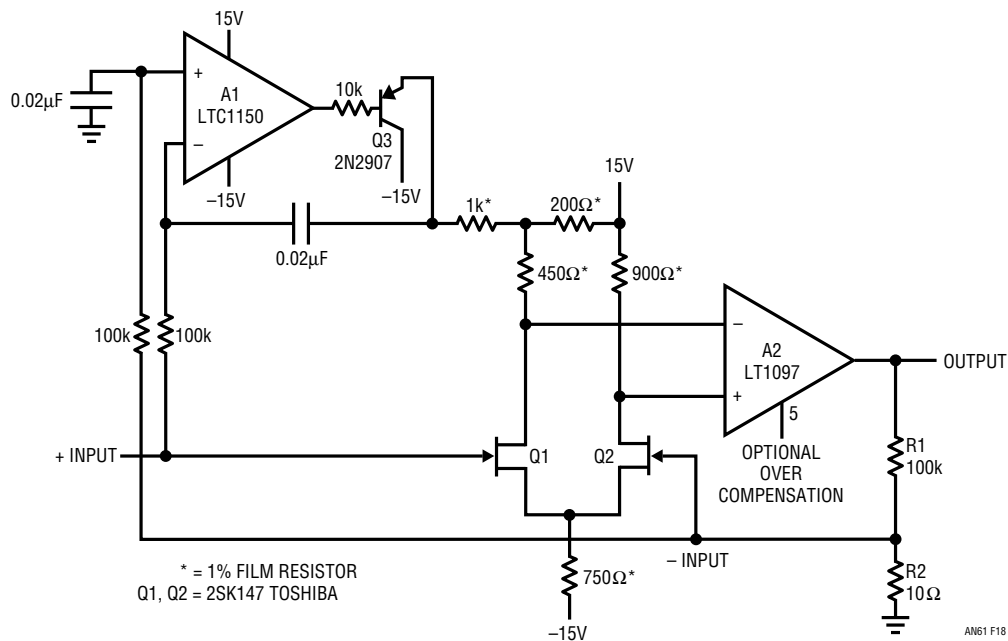


Figure 18. Chopper-Stabilized FET Pair Combines Low Bias, Offset and Drift with 45nV Noise

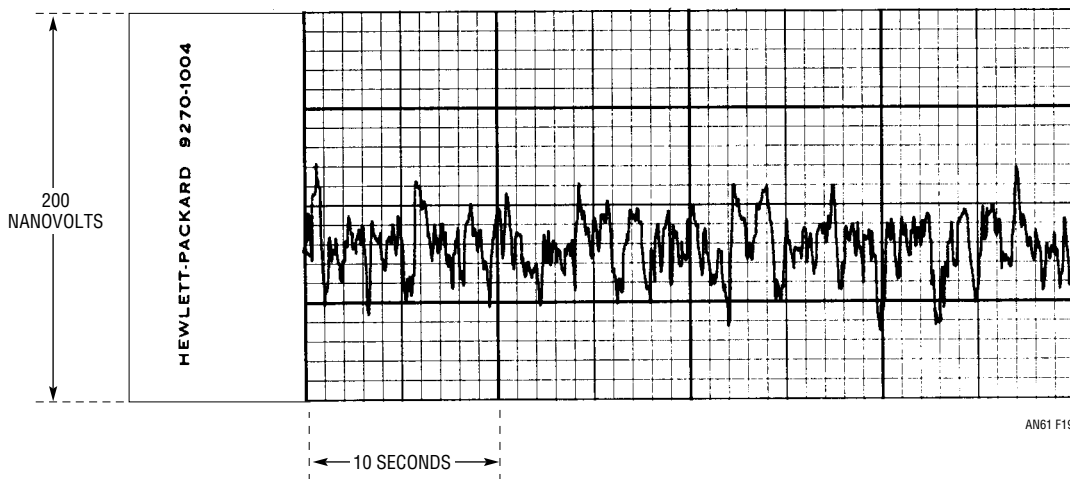


Figure 19. Figure 18's 45nV Noise Performance in a 0.1Hz to 10Hz Bandwidth. A1's Low Offset and Drift Are Retained, But Noise Is Almost 35 Times Better

Figure 20 shows the response (trace B) to a 1mV input step (trace A). The output is clean, with no overshoots or uncontrolled components. If A2 is replaced with a faster device (e.g., LT1055) speed increases by an order of magnitude with similar damping. A2's optional overcompensation can be used (capacitor to ground) to optimize response for low closed-loop gains.

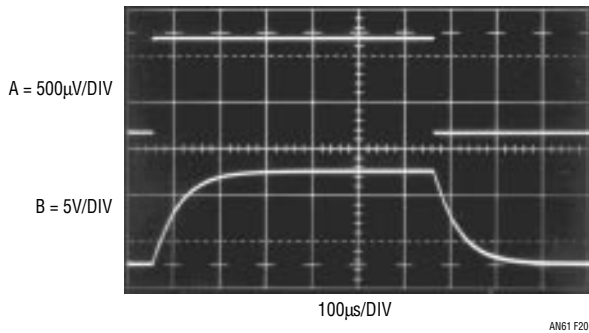


Figure 20. Step Response for the Low Noise $\times 10,000$ Amplifier. A $10\times$ Speed Increase Is Obtainable by Replacing A2 with a Faster Device

High Speed Adaptive Trigger Circuit

Line receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 21 triggers on 2mV to 100mV signals from 100Hz to 10MHz while operating from a single 5V rail. A1, operating at a gain of 20, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1-Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of A1's output signal's midpoint appears at the junction of the 500pF capacitor and the 10M Ω units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1116's positive input. The LT1116's negative input is biased directly from A1's output. The LT1116's output, the circuit's output, is unaffected by 50:1 signal amplitude variations. Bandwidth limiting in A1 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

Split supply versions of this circuit can achieve bandwidths to 50MHz with wider input operating range (See Reference 7).

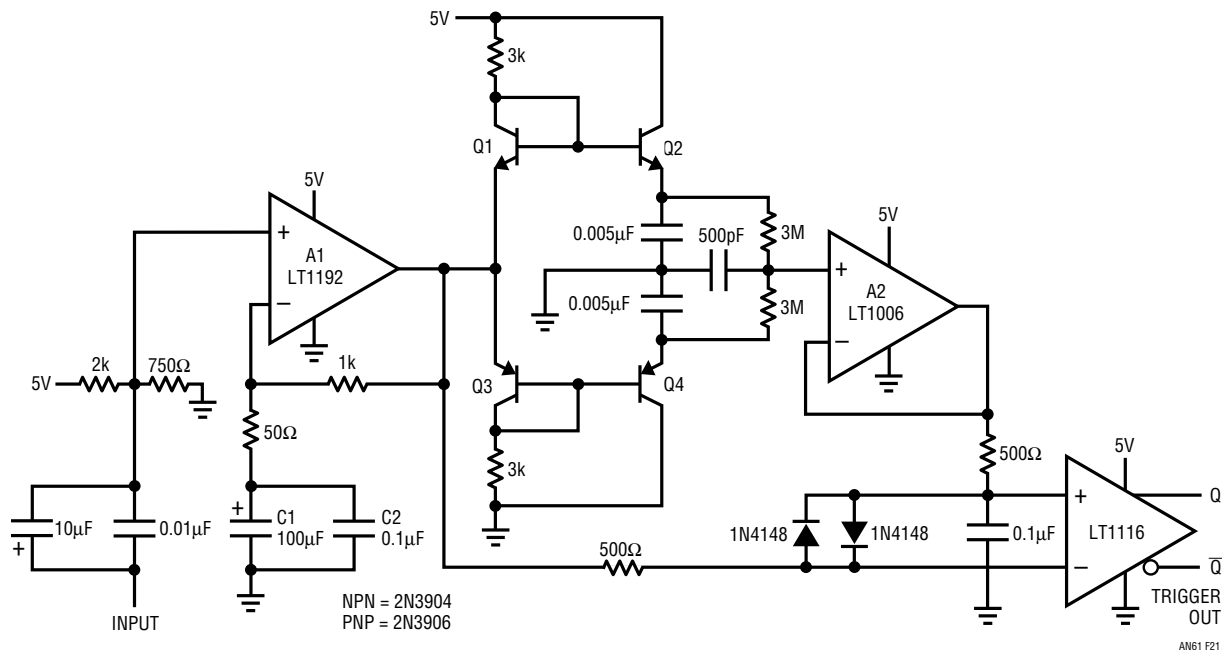


Figure 21. Fast Single Supply Adaptive Trigger. Output Comparator's Trip Level Varies Ratiometrically with Input Amplitude, Maintaining Data Integrity Over 50:1 Input Amplitude Range

Application Note 61

Wideband, Thermally-Based RMS/DC Converter

Applications such as wideband RMS voltmeters, RF leveling loops, wideband AGC, high crest factor measurements, SCR power monitoring and high frequency noise measurements require wideband, true RMS/DC conversion. The thermal conversion method achieves vastly higher bandwidth than any other approach. Thermal RMS/DC converters are direct acting, thermoelectronic analog computers. The thermal technique is explicit, relying on “first principles,” e.g., a waveforms RMS value is defined as its heating value in a load.

Figure 22 is a wideband, thermally-based RMS/DC converter.³ It provides a true RMS/DC conversion from DC to 10MHz with less than 1% error, regardless of input signal waveshape. It also features high input impedance and overload protection.

The circuit consists of three blocks; a wideband FET input amplifier, the RMS/DC converter and overload protection. The amplifier provides high input impedance, gain and drives the RMS/DC converters input heater. Input resistance is defined by the 1M resistor with input capacitance about 3pF. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1206 provides a flat 10MHz bandwidth gain of ten. Normally, this open-loop configuration would be quite drifts because there is no DC feedback. The LT1097 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The capacitor at A1 provides stable

loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. Q4, Q5 and Q6 form a low leakage clamp which precludes A1 loop latch-up during start-up or overdrive conditions. This can occur if Q1 ever forward biases. The 5K-50pF network gives A2 a slight peaking characteristic at the highest frequencies, allowing 1% flatness to 10MHz. A2's output drives the RMS/DC converter.

The LT1088 based RMS/DC converter is made up of matched pairs of heaters and diodes and a control amplifier. The LT1206 drives R1, producing heat which lowers D1's voltage. Differentially connected A3 responds by driving R2, via Q3, to heat D2, closing a loop around the amplifier. Because the diodes and heater resistors are matched, A3's DC output is related to the RMS value of the input, regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain trim, which is implemented at A4. A4's output is the circuit output. The LT1004 and associated components frequency compensate the loop and provide good settling time over wide ranges of operating conditions (see Footnote 3).

Start-up or input overdrive can cause A2 to deliver excessive current to the LT1088 with resultant damage. C1 and C2 prevent this. Overdrive forces D1's voltage to an abnormally low potential. C1 triggers low under these conditions, pulling C2's input low. This causes C2's output to go high, putting A2 into shutdown and terminating the overload. After a time determined by the RC at C2's input, A2 will be enabled. If the overload condition still exists the loop will almost immediately shut A2 down again. This oscillatory action will continue, protecting the LT1088 until the overload condition is removed.

Note 3: Thermally based RMS/DC conversion is detailed in Reference 9.

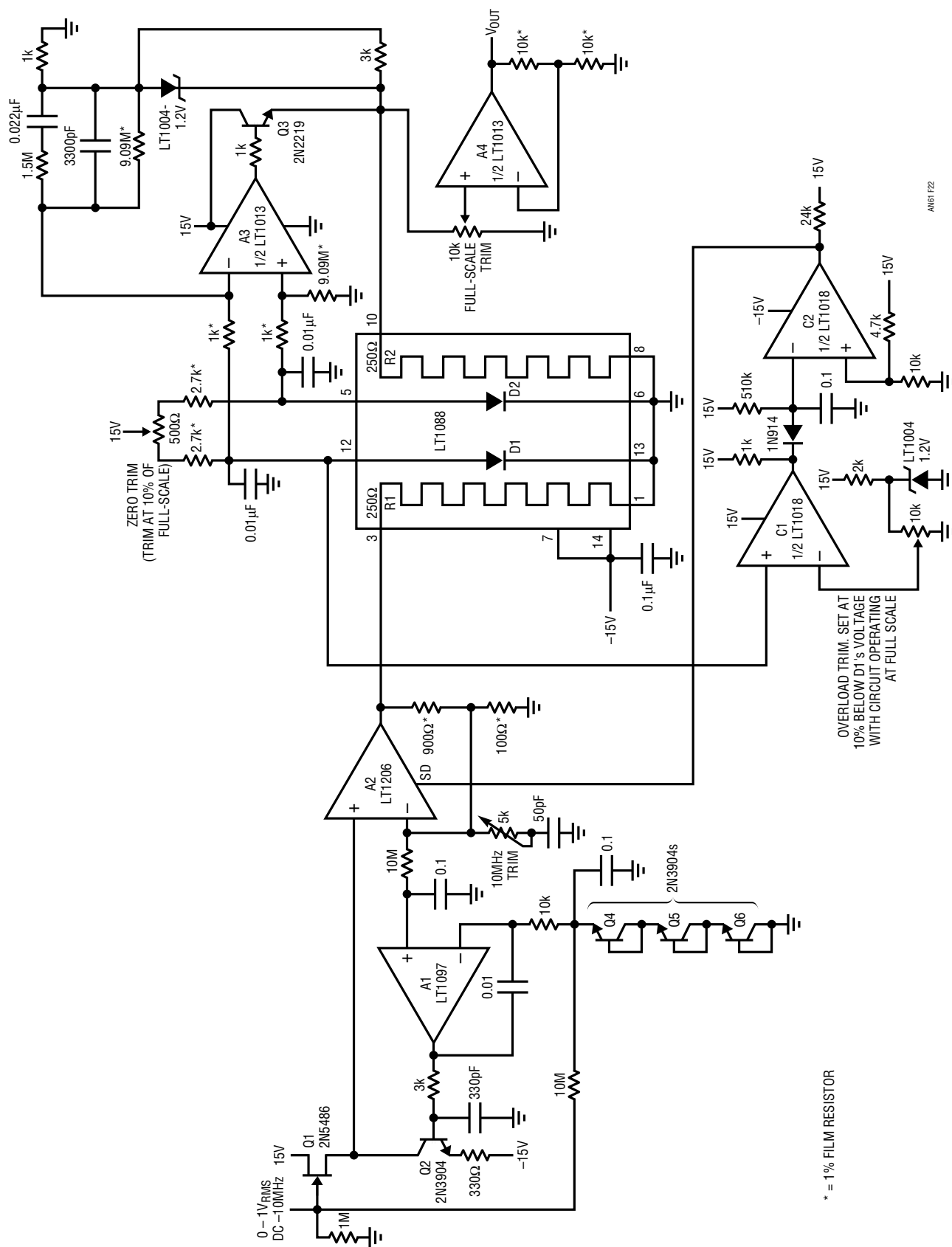


Figure 22. Complete 10MHz Thermally-Based RMS/DC Converter Has 1% Accuracy, High Input Impedance and Overload Protection

Application Note 61

Performance for the circuit is quite impressive. Figure 23 plots error from DC to 11MHz. The graph shows 1% error bandwidth of 11MHz. The slight peaking out to 5MHz is due to the gain boost network at A2's negative input. The peaking is minimal compared to the total error envelope, and a small price to pay to get the 1% accuracy to 10MHz.

To trim this circuit put the 5k Ω potentiometer at its maximum resistance position and apply a 100 mV, 5MHz signal. Trim the 500 Ω adjustment for exactly 1V_{OUT}. Next, apply a 5MHz 1V input and trim the 10k potentiometer for 10.00V_{OUT}. Finally, put in 1V at 10MHz and adjust the 5k Ω trimmer for 10.00V_{OUT}. Repeat this sequence until circuit output is within 1% accuracy for DC-10MHz inputs. Two passes should be sufficient.

It is worth considering that this circuit performs the same function as instruments costing thousands of dollars.⁴

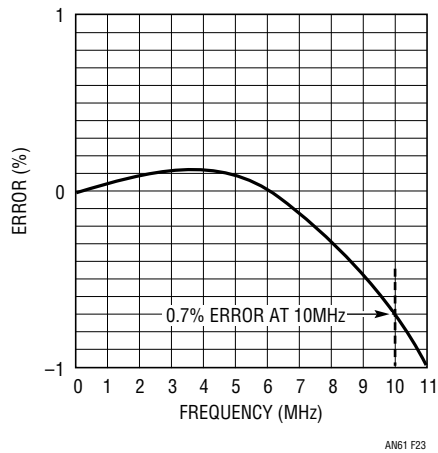


Figure 23. Error Plot for the RMS/DC Converter. Frequency Dependent Gain Boost at A2 Preserves 1% Accuracy, But Causes Slight Peaking Before Roll-Off

Hall Effect Stabilized Current Transformer

Current transformers are common and convenient. They permit wideband current measurement independent of common-mode voltage considerations. The most conve-

nient current transformers are the “clip-on” type, commercially sold as “current probes.” A problem with all simple current transformers is that they cannot sense DC and low frequency information. This problem was addressed in the mid-1960’s with the advent of the Hall effect stabilized current probe. This approach uses a Hall effect device within the transformer core to sense DC and low frequency signals. This information is combined with the current transformers output to form a composite DC-to-high frequency output. Careful roll-off and gain matching of the two channels preserves amplitude accuracy at all frequencies.⁵ Additionally, the low frequency channel is operated as a “force-balance,” meaning that the low frequency amplifier’s output is fed back to magnetically bias the transformer flux to zero. Thus, the Hall effect device does not have to respond linearly over wide ranges of current and the transformer core never sees DC bias, both advantageous conditions. The amount of DC and low frequency information is obtained at the amplifier’s output, which corresponds to the bias needed to offset the measured current.

Figure 24 shows a practical circuit. The Hall effect transducer lies within the core of the clip-on current transformer specified. A very simplistic way to model the Hall generator is as a bridge, excited by the two 619 Ω resistors. The Hall generator’s outputs (the midpoints of the “bridge”) feed differential input transconductance amplifier A1, which takes gain, with roll-off set by the 50 Ω , 0.02 μ F RC at its output. Further gain is provided by A2, in the same package as A1. A current buffer provides power gain to drive the current transformers secondary. This connection closes a flux nulling loop in the transducer core. The offset adjustments should be set for 0V output with no current flowing in the clip-on transducer. Similarly, the loop gain and bandwidth trims should be set so that the composite output (the combined high and low frequency output across the grounded 50 Ω resistor) has clean step response and correct amplitude from DC to high frequency.

Note 4: Viewed from a historical perspective it is remarkable that so much precision wideband performance is available from such a relatively simple configuration. For perspective, see Appendix A, “Precision Wideband Circuitry . . . Then and Now.”

Note 5: Details of this scheme are nicely presented in Reference 15. Additional relevant commentary on parallel path schemes appears in Reference 7.

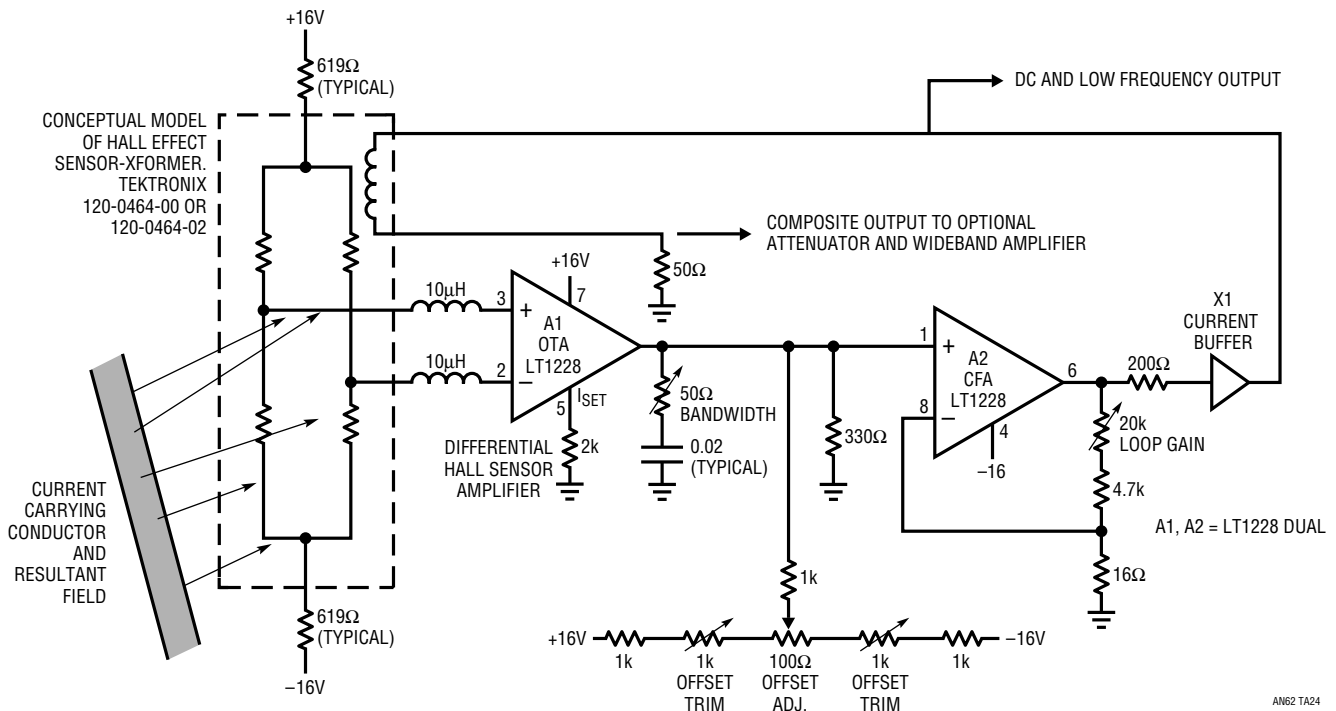


Figure 24. Hall Effect Stabilized Current Transformer (DC → High Frequency Current Probe)

Figure 25 shows a practical way to conveniently evaluate this circuit's performance. This partial schematic of the Tektronix P-6042 current probe shows a similar signal conditioning scheme for the transducer specified in Figure 24. In this case Q22, Q24 and Q29 combine with differential stage M-18 to form the Hall amplifier. To evaluate Figure 24's circuit remove M-18, Q22, Q24 and Q29. Next,

connect LT1228 pins 3 and 2 to the former M-18 pins 2 and 10 points, respectively. The $\pm 16\text{V}$ supplies are available from the P-6042's power bus. Also, connect the right end of Figure 24's 200Ω resistor to what was Q29's collector node. Finally, perform the offset, loop gain and bandwidth trims as previously described.

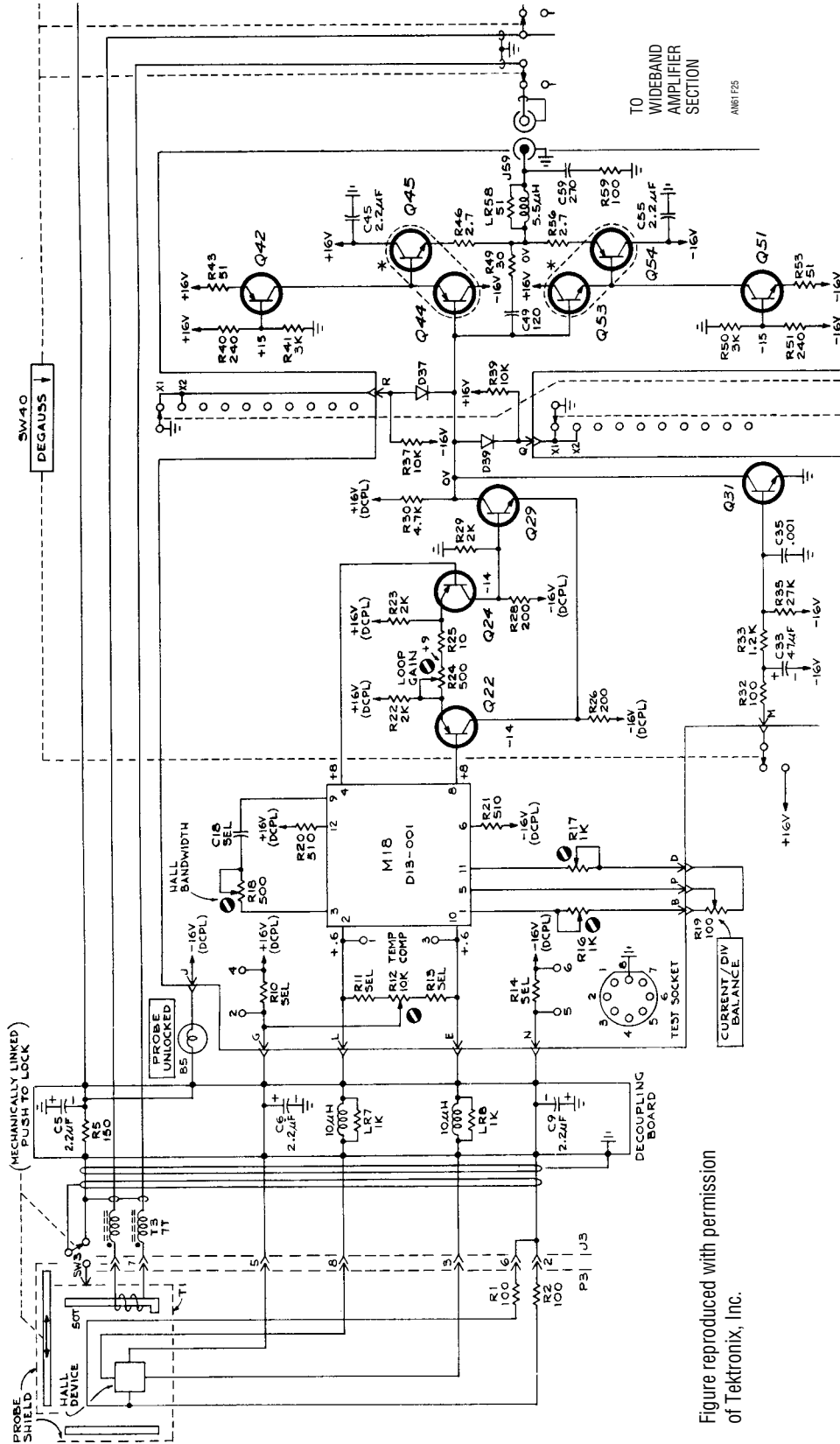


Figure reproduced with permission of Tektronix, Inc.

Figure 25. Tektronix P-6042 Hall Effect Based Current Probe Servo Loop.
Figure 24 Replaces M18 Amplifier and Q22, Q24 and Q29

Triggered 250 Picosecond Rise Time Pulse Generator

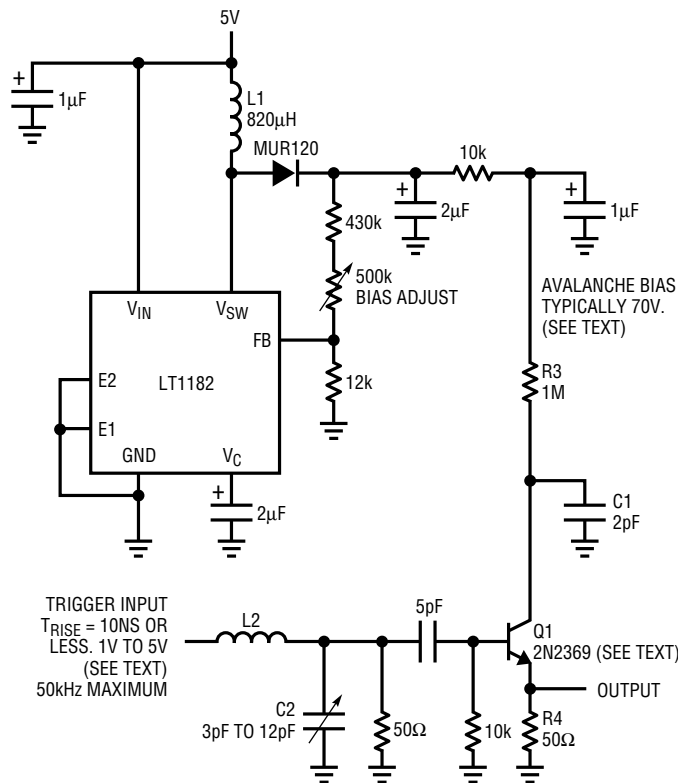
Verifying the rise time limit of wideband test equipment setups is a difficult task. In particular, the “end-to-end” rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure 26’s circuit does this, providing an 800ps pulse with rise and fall times inside 250ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit has similarities to a previously published design (see Reference 7) except that it is triggered instead of free running. This feature permits synchronization to a clock or other event. The output phase with respect to the trigger is variable from 200ps to 5ns.

The pulse generator requires high voltage bias for operation. The LT1182 switching regulator to forms a high voltage switched mode control loop. The LT1182 pulse

width modulates at its 100kHz clock rate. L1’s inductive events are rectified and stored in the 2μF output capacitor. The adjustable resistor divider provides feedback to the LT1182. The 10k-1μF RC provides noise filtering.

The high voltage is applied to Q1, a 40V breakdown device, via the R3-C1 combination. The high voltage “bias adjust” control should be set at the point where free running pulses across R4 *just* disappear. This puts Q1 slightly below its avalanche point. When an input trigger pulse is applied Q1 avalanches. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1’s collector voltage falls and breakdown ceases. C1 then recharges to just below the avalanche point. At the next trigger pulse this action repeats.⁶

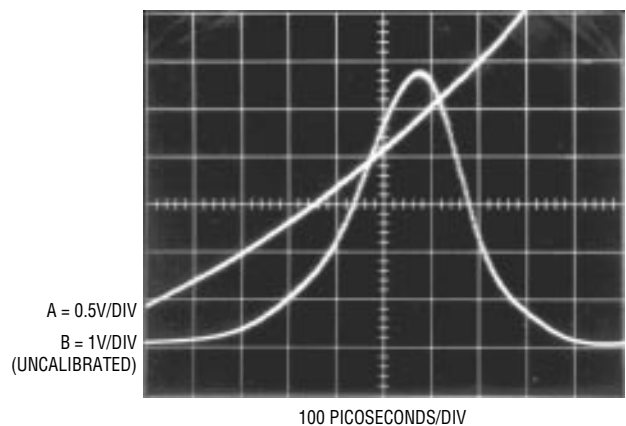
Figure 27 shows waveforms. A 3.9GHz sampling oscilloscope (Tektronix 661 with 4S2 sampling pug-in) measures the pulse (trace B) at 10V high with an 800ps base. Rise time is 250ps, with fall time indicating 200ps. The times are probably slightly faster, as the oscilloscope’s 90ps rise time influences the measurement.⁷ The input trigger pulse is trace A. Its amplitude provides a convenient way to vary the delay time between the trigger and output pulses. A 1V to 5V amplitude setting produces a continuous 5ns to 200ps delay range.



L1 = J.W. MILLER # 100267
L2 = 1 TURN # 28 WIRE, 1/4" TOTAL LENGTH

AN62 F26

Figure 26. Triggered 250ps Rise Time Pulse Generator. Trigger Pulse Amplitude Controls Output Phase



AN61 F27

Figure 27. Input Pulse Edge (Trace A) Triggers the Avalanche Pulse Output (Trace B). Display Granularity Is Characteristic of Sampling Oscilloscope Operation

Note 6: This circuit is based on the operation of the Tektronix Type 111 Pulse Generator. See Reference 16.

Note 7: I’m sorry, but 3.9GHz is the fastest ‘scope in my house (as of September, 1993).

Application Note 61

Some special considerations are required to optimize circuit performance. L2's very small inductance combines with C2 to slightly retard the trigger pulse's rise time. This prevents significant trigger pulse artifacts from appearing at the circuit's output. C2 should be adjusted for the best compromise between output pulse rise time and purity. Figure 28 shows partial pulse rise with C2 properly adjusted. There are no discernible discontinuities related to the trigger event.

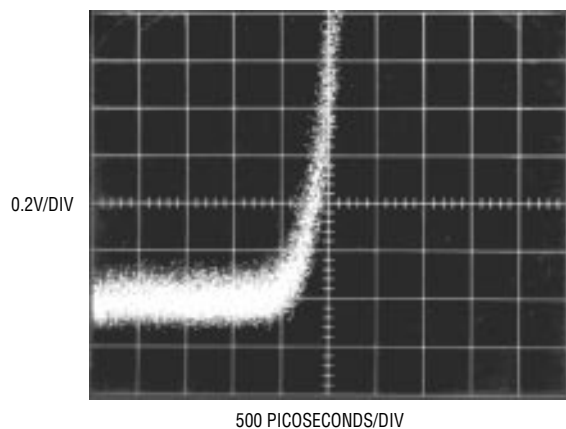


Figure 28. Expanded Scale View of Leading Edge Is Clean with No Trigger Pulse Artifacts. Display Granularity Derives from Sampling Oscilloscope Operation

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All "good" devices switched in less than 600ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout, connection and termination techniques are essential for a good results from this circuit.

Flash Memory Programmer

Although "Flash" type memory is increasingly popular, it does require some special programming features. The 5V powered memories need a carefully controlled 12V "VPP" programming pulse. The pulse's amplitude must be within 5% to assure proper operation. Additionally, the pulse must not overshoot, as memory destruction may occur for VPP outputs above 14V.⁸ These requirements usually

mandate a separate 12V supply and pulse forming circuitry. Figure 29's circuit provides the complete flash memory programming function with a single IC and some discrete components. All components are surface mount types, so little board space is required. The entire function runs off a single 5V supply.

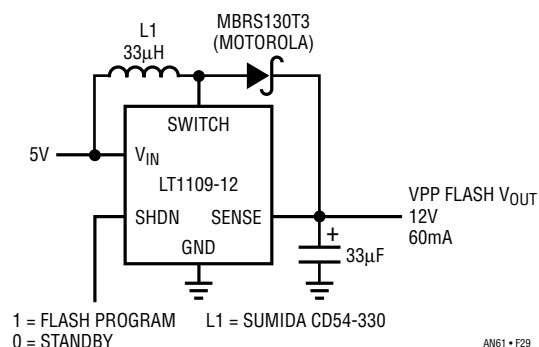


Figure 29. Switching Regulator Provides Complete Flash Memory Programmer

The LT1109-12 switching regulator functions by repetitively pulsing L1. L1 responds with high voltage flyback events, which are rectified by the diode and stored in the 10µF capacitor. The "sense" pin provides feedback, and the output voltage stabilizes at 12V within a few percent. The regulator's "shutdown" pin provides a way to control the VPP programming voltage output. With a logical zero applied to the pin the regulator shuts down, and no VPP programming voltage appears at the output. When the pin goes high (trace A, Figure 30) the regulator is activated, producing a cleanly rising, controlled pulse at the output (trace B). When the pin is returned to logical zero, the output smoothly decays off. The switched mode delivery of power combined with the output capacitor's filtering prevents overshoot while providing the required pulse amplitude accuracy. Trace C, a time and amplitude expanded version of trace B, shows this. The output steps up in amplitude each time L1 dumps energy into the output capacitor. When the regulation point is reached the amplitude cleanly flattens out, with only about 75mV of regulator ripple.

Note 8: See Reference 17 for detailed discussion.

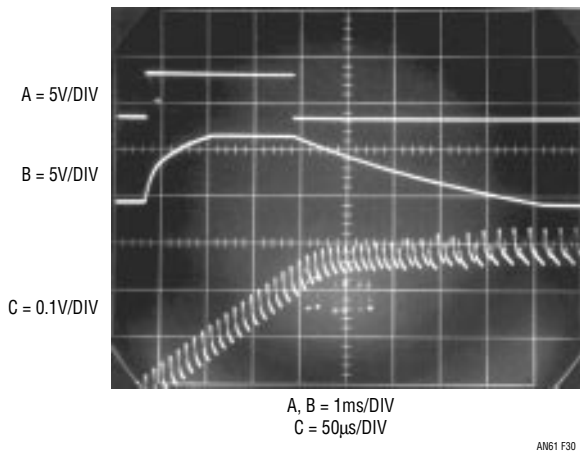


Figure 30. Flash Memory Programmer Waveforms Show Controlled Edges. Trace C Details Rise Time Settling

3.3V Powered V/F Converter

Figure 31 is a “charge pump” type V/F converter specifically designed to run from a 3.3V rail.⁹ A 0V to 2V input produces a corresponding 0kHz to 3kHz output with linearity inside 0.05%. To understand how the circuit works assume that A1’s negative input is just below 0V. The amplifier output is positive. Under these conditions, LTC1043’s pins 12 and 13 are shorted as are pins 11 and 7, allowing the 0.01µF capacitor (C1) to charge to the 1.2V LT1034 reference. When the input-voltage-derived current ramps A1’s summing point (negative input-trace A, Figure 32) positive, its output (trace B) goes low. This reverses the LTC1043’s switch states, connecting pins 12 and 14, and 11 and 8. This effectively connects C1’s positively charged end to ground on pin 8, forcing current to flow from A1’s summing junction into C1 via LTC1043 pin 14 (pin 14’s current is trace C). This action resets A1’s summing point to a small negative potential (again, trace A). The 120pF-50k-10k time constant at A1’s positive input ensures A1 remains low long enough for C1 to completely discharge (A1’s positive input is trace D). The Schottky diode prevents excessive negative excursions due to the 120pF capacitors differentiated response.

When the 120pF positive feedback path decays, A1’s output returns positive and the entire cycle repeats. The oscillation frequency of this action is directly related to the input voltage.

This is an AC coupled feedback loop. Because of this, start-up or overdrive conditions could force A1 to go low and

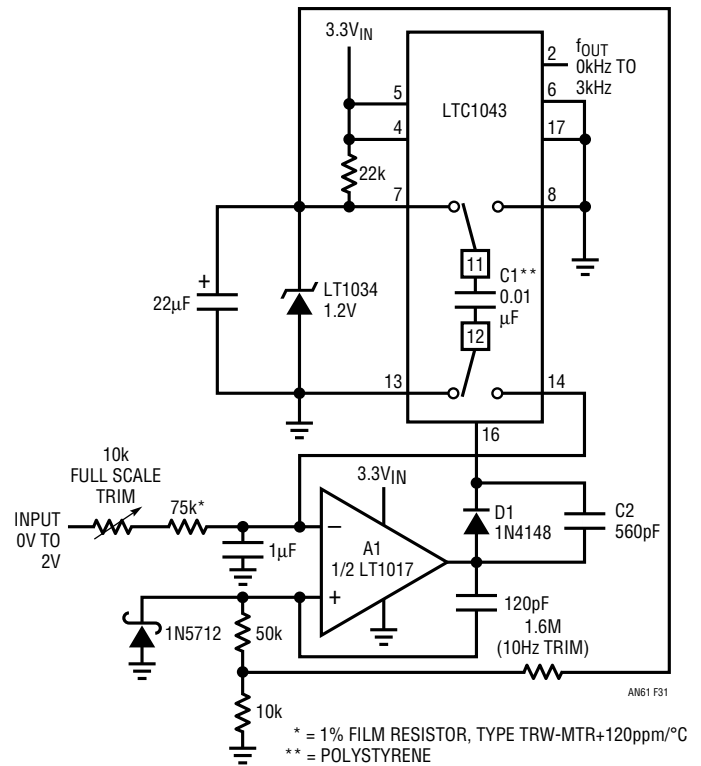


Figure 31. 3.3V Powered Voltage-to-Frequency Converter. Charge Pump Based Feedback Maintains High Linearity and Stability

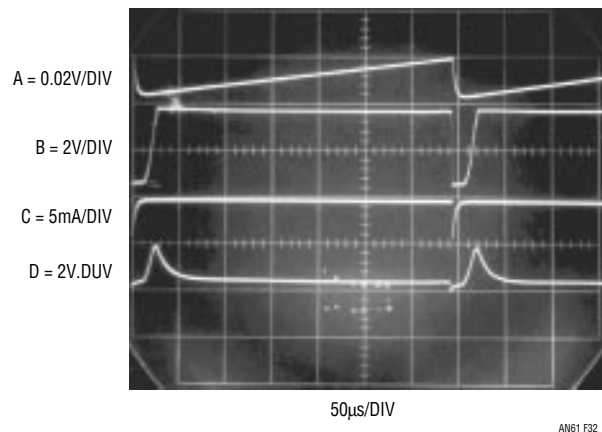


Figure 32. Waveform for the 3.3V Powered V/F. Charge Pump Action (Trace C) Maintains Summing Point (Trace A), Enforcing High Linearity and Accuracy

Note 9: See Reference 20 for a survey of V/F techniques.

Application Note 61

stay there. When A1's output is low the LTC1043's internal oscillator sees C2 and will begin oscillation if A1 remains low long enough. This oscillation causes charge pumping action via the LTC1043-C1-A1 summing junction path until normal operation commences. During normal operation A1 is never low long enough for oscillation to occur, and controls the LTC1043 switch states via D1.

To calibrate this circuit apply 7mV and select the 1.6M (nominal) value for 10Hz out. Then apply 2.000V and set the 10k trim for exactly 3kHz output. Pertinent specifications include linearity of 0.05%, power supply rejection of 0.04%/V, temperature coefficient of 75ppm/°C of scale and supply current of about 200µA. The power supply may vary from 2.6V to 4.0V with no degradation of these specifications. If degraded temperature coefficients are acceptable, the film resistor specified may be replaced by a standard 1% film resistor. The type called out has a

temperature characteristic that opposes C1's - 120ppm/°C drift, resulting in the low overall circuit drift noted.

Broadband Random Noise Generator

Filter, audio, and RF-communications testing often require a random noise source.¹⁰ Figure 33's circuit provides an RMS-amplitude regulated noise source with selectable bandwidth. RMS output is 300mV with a 1kHz to 5MHz bandwidth, selectable in decade ranges.

Noise source D1 is AC coupled to A2, which provides a broadband gain of 100. A2's output feeds a gain control stage via a simple, selectable lowpass filter. The filter's output is applied to A3, an LT1228 operational transcon-

Note 10: See Appendix B, "Symmetrical White Gaussian Noise," guest written by Ben Hessen-Schmidt of Noise Com, Inc. for tutorial on noise.

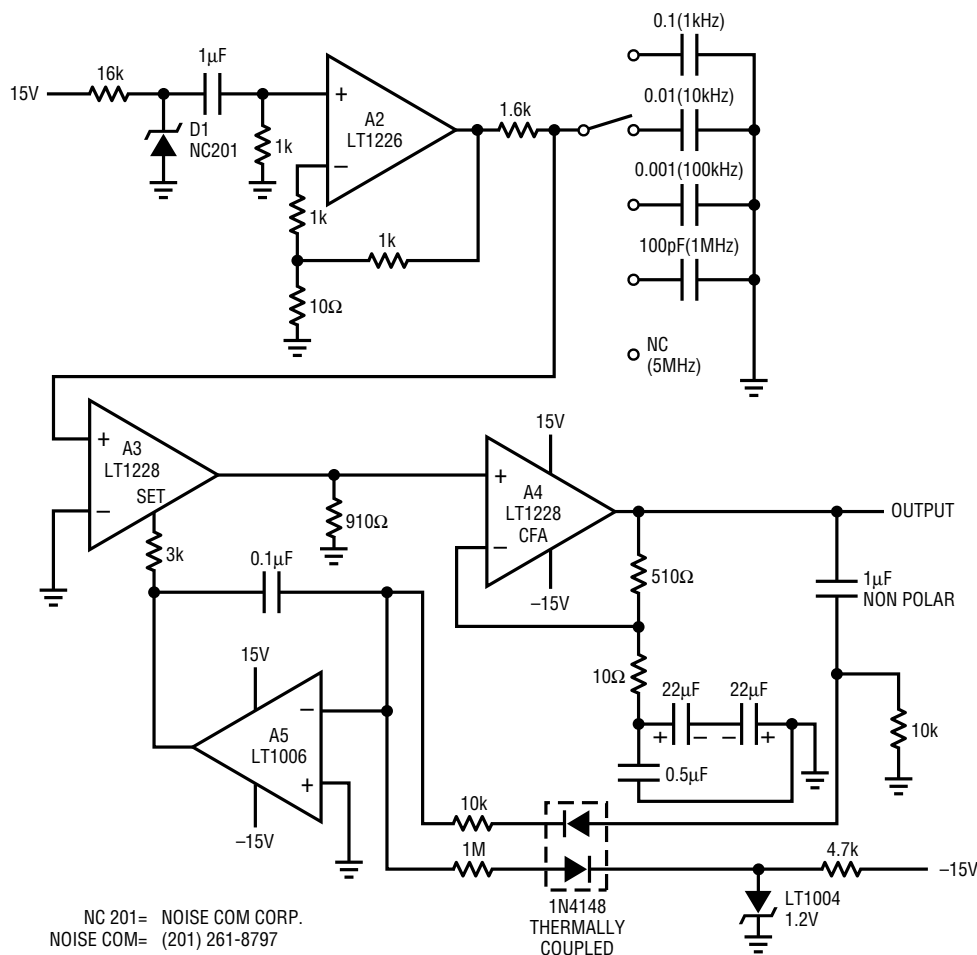


Figure 33. Broadband Random Noise Generator Uses Gain Control Loop to Enhance Noise Spectrum Amplitude Uniformity

ductance amplifier. A3's output feeds LT1228 A4, a current feedback amplifier. A4's output, also the circuit's output, is sampled by the A5-based gain control configuration. This closes a gain control loop to A3. A3's set current controls gain, allowing overall output level control.

Figure 34 shows noise at 1MHz bandpass, with Figure 35 showing RMS noise versus frequency in the same bandpass. Figure 36 plots similar information at full bandwidth (5MHz). RMS output is essentially flat to 1.5MHz with about ± 2 dB control to 5MHz before sagging badly.

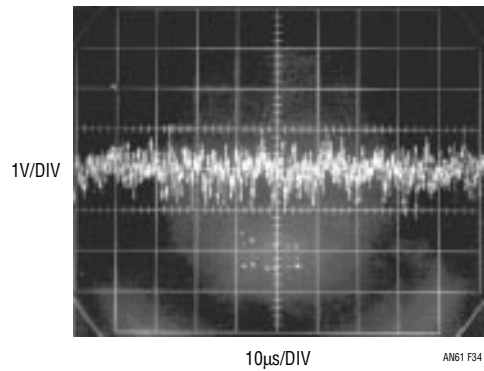


Figure 34. Figure 33's Output in the 1MHz Filter Position

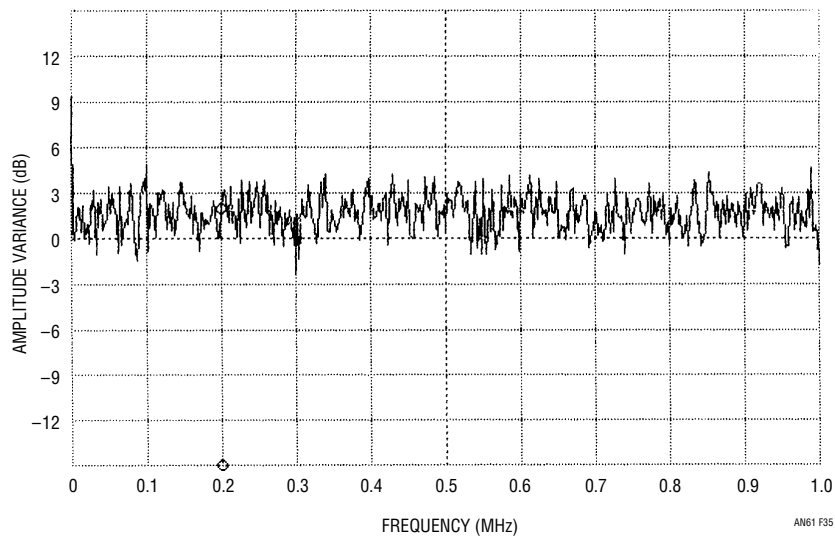


Figure 35. Amplitude vs Frequency for the Random Noise Generator Is Essentially Flat to 1MHz

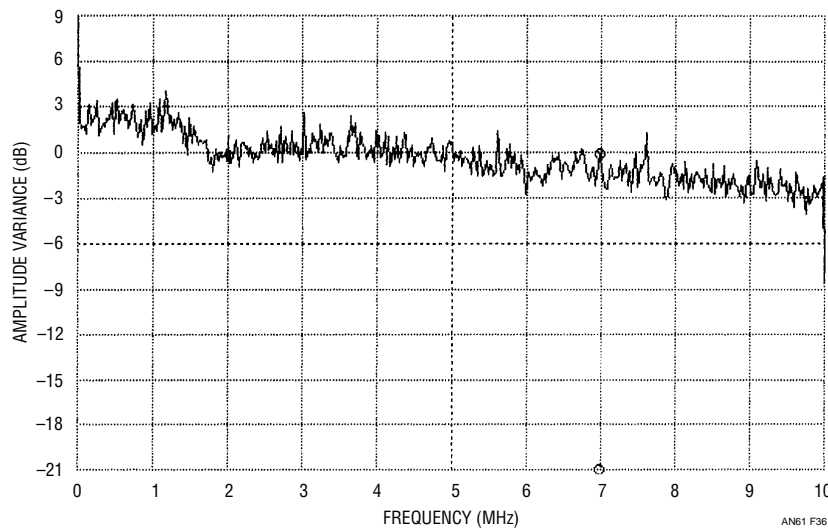


Figure 36. RMS Noise vs Frequency at 5MHz Bandpass Shows Slight Fall-Off Beyond 1MHz

Application Note 61

Figure 37's similar circuit substitutes a standard zener for the noise source but is more complex and requires a trim. A1, biased from the LT1004 reference, provides optimum drive for D1, the noise source. AC coupled A2 takes a broadband gain of 100. A2's output feeds a gain-control stage via a simple selectable lowpass filter. The filter's output is applied to LT1228 A3, an operational transconductance amplifier. A3's output feeds LT1228 A4, a current feedback amplifier. A4's output, the circuit's output,

is sampled by the A5-based gain control configuration. This closes a gain control loop back at A3. A3's set input current controls its gain, allowing overall output level control.

To adjust this circuit, place the filter in the 1kHz position and trim the 5k potentiometer for maximum negative bias at A3, pin 5.

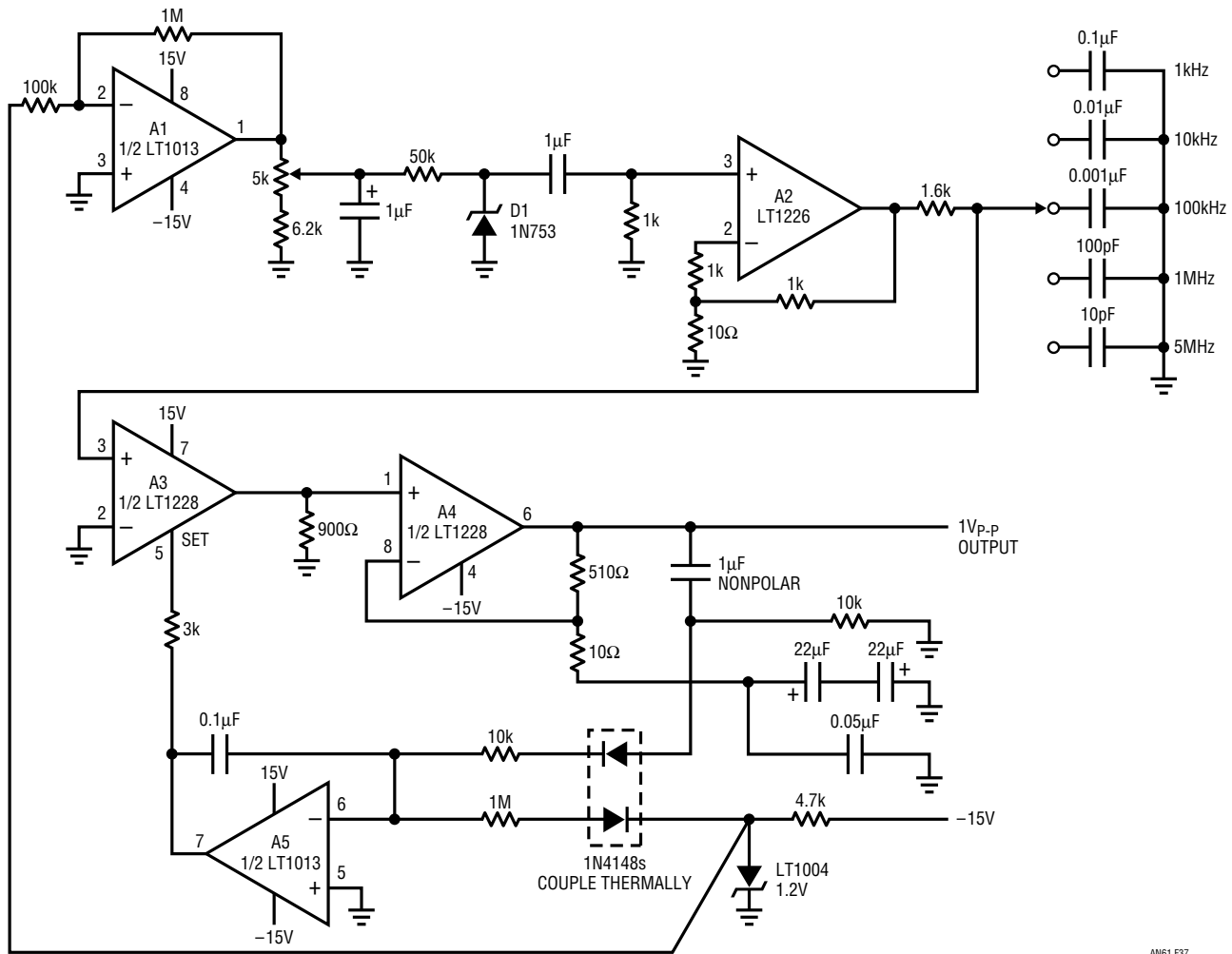


Figure 37. A Similar Circuit Uses a Standard Zener Diode, But Is More Complex and Requires Trimming

Switchable Output Crystal Oscillator

Figure 38's simple crystal oscillator circuit permits crystals to be electronically switched by logic commands. The circuit is best understood by initially ignoring all crystals. Further, assume all diodes are shorts and their associated 1k resistors open. The resistors at the LT1116's positive input set a DC bias point. The 2k-25pF path sets up phase shifted feedback and the circuit looks like a wideband unity gain follower at DC. When "Xtal A" is inserted (remember, D1 is temporarily shorted) positive feedback occurs and

oscillation commences at the crystals resonant frequency. If D1 and its associated 1k value are realized, oscillation can only continue if logic input A is biased high. Similarly, additional crystal-diode-1k branches permit logic selection of crystal frequency.

For AT cut crystals about a millisecond is required for the circuit output to stabilize due to the high Q factors involved. Crystal frequencies can be as high as 16MHz before comparator delays preclude reliable operation.

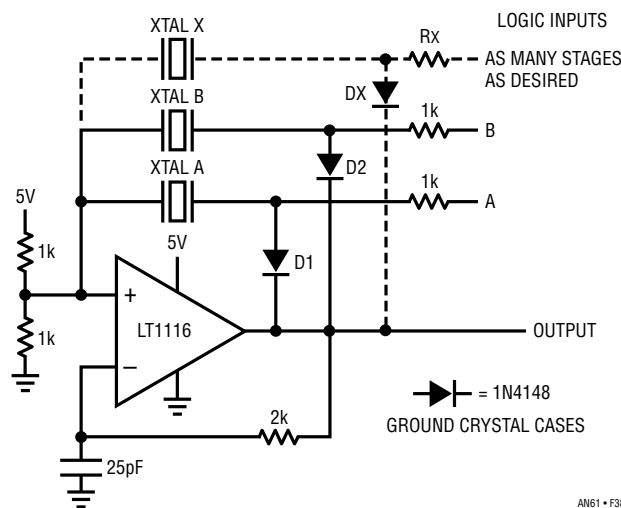


Figure 38. Switchable Output Crystal Oscillator. Biasing A or B High Places the Associated Crystal in the Feedback Path. Additional Crystal Branches Are Permissible

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APPENDIX A

Precision Wideband Circuitry . . . Then and Now

Text Figure 22's relatively straightforward design provides a sensitive, thermally-based RMS/DC conversion to 10MHz with less than 1% error. Viewed from a historical perspective it is remarkable that so much precision wideband performance is so easily achieved.

Thirty years ago these specifications presented an extremely difficult engineering challenge, requiring deep-seated knowledge of fundamentals, extraordinary levels of finesse and an interdisciplinary outlook to achieve success.

The Hewlett-Packard model HP3400A (1965 price \$525 . . . about 1/3 the yearly tuition at M.I.T.) thermally-based RMS voltmeter included all of Figure 22's elements, but considerably more effort was required in its execution.¹ Our comparative study begins by considering H-P's version of Figure 22's FET buffer and precision wideband amplifier. The text is taken directly from the *HP3400A Operating and Service Manual*.²

Note 1: We are all constantly harangued about the advances made in computers since the days of the IBM360. This section gives analog aficionados a stage for their own bragging rights. Of course, an HP3400A was much more interesting than an IBM360 in 1965. Similarly, Figure 22's

capabilities are more impressive than any contemporary computer I'm aware of.

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4-15. IMPEDANCE CONVERTER ASSEMBLY A2.

4-17. The ac signal input to the impedance converter is RC coupled to the grid of cathode follower V201³ through C201 and R203. The output signal is developed by Q201 which acts as a variable resistance in the cathode circuit of V201. The bootstrap feedback from the cathode of V201 to R203 increases the effective resistance of R203 to the input signal. This prevents R203 from loading the input signal and preserves the high input impedance of the Model 3400A. The gain compensating feedback from the plate of V201 to the base of Q201 compensates for any varying gain in V201 due to age or replacement.

4-18. Breakdown diode CR201 controls the grid bias voltage on V201 thereby establishing the operating point of this stage. CR202 and R211 across the base-emitter junction of Q201 protects Q201 in the event of a failure in the +75 volt power supply. Regulated dc is supplied to V201 filaments to avoid inducing ac hum in the signal path. This also prevents the gain of V201 changing with line voltage variations.

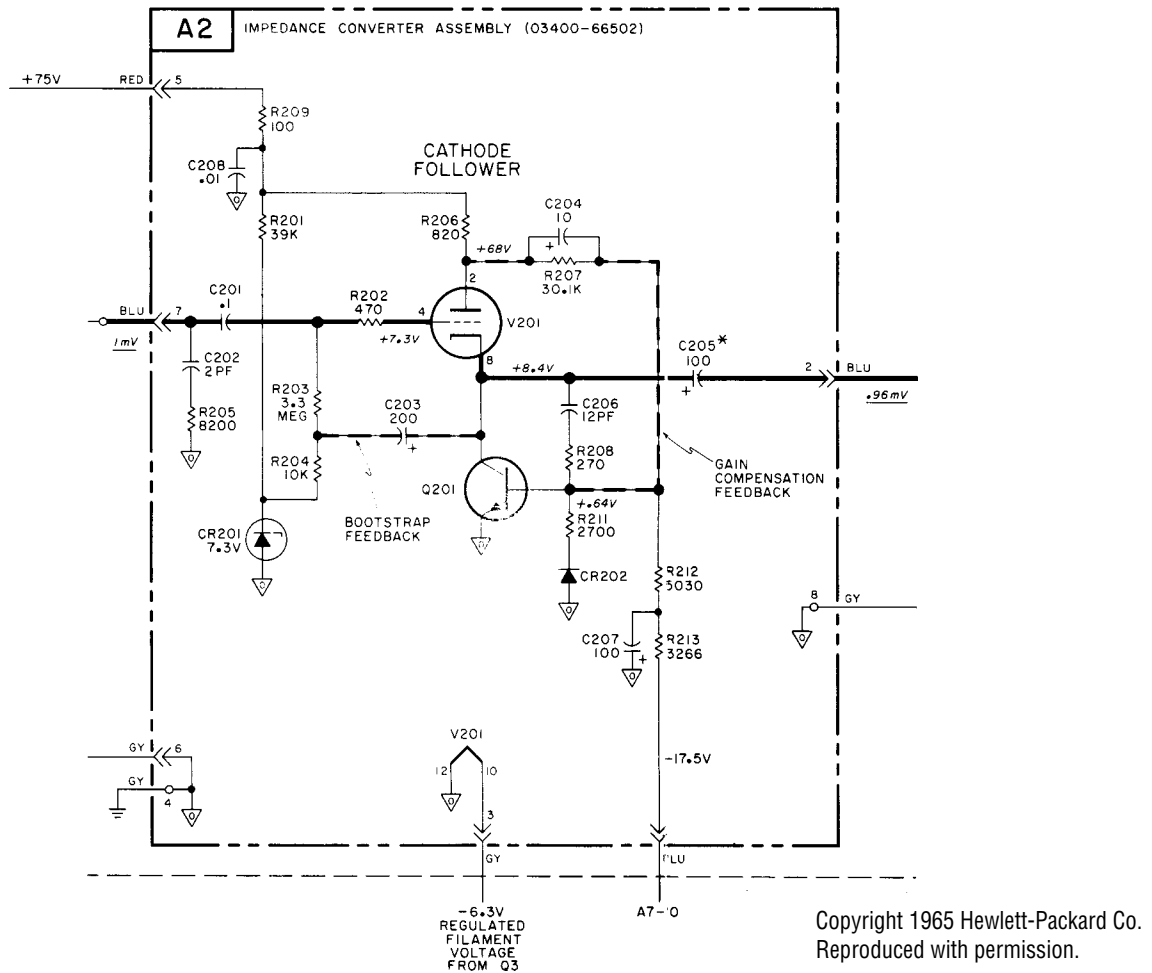


Figure A1. The "Impedance Converter Assembly," H-P's Equivalent of Figure 22's Wideband FET Buffer

Note 3: Although JFETs were available in 1965 their performance was inadequate for this design's requirements. The only available option was the Nuvistor triode described.

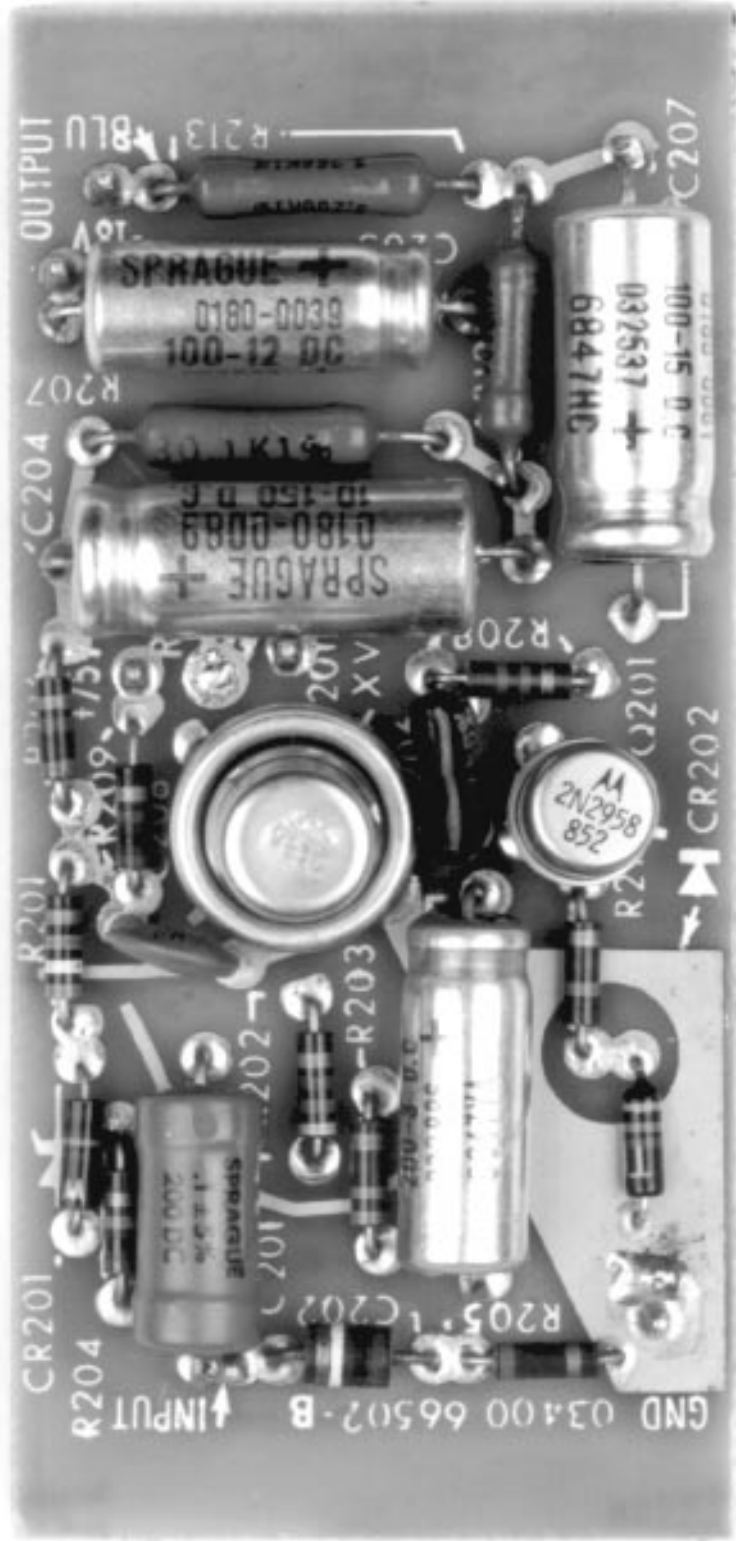


Figure A2. The Hewlett-Packard 3400A's Wideband Input Buffer. Nuvistor Triode (Upper Center) Provided Speed, Low Noise, and High Impedance. Circuit Required 75V, -17.5V and -6.3V Supplies. Regulated Filament Supply Stabilized Follower Gain While Minimizing Noise

4-22. VIDEO AMPLIFIER ASSEMBLY A4.

4-23. The video amplifier functions to provide constant gain to the ac signal being measured over the entire frequency range of Model 3400A. See video amplifier assembly schematic diagram illustrated on Figure 6-2.

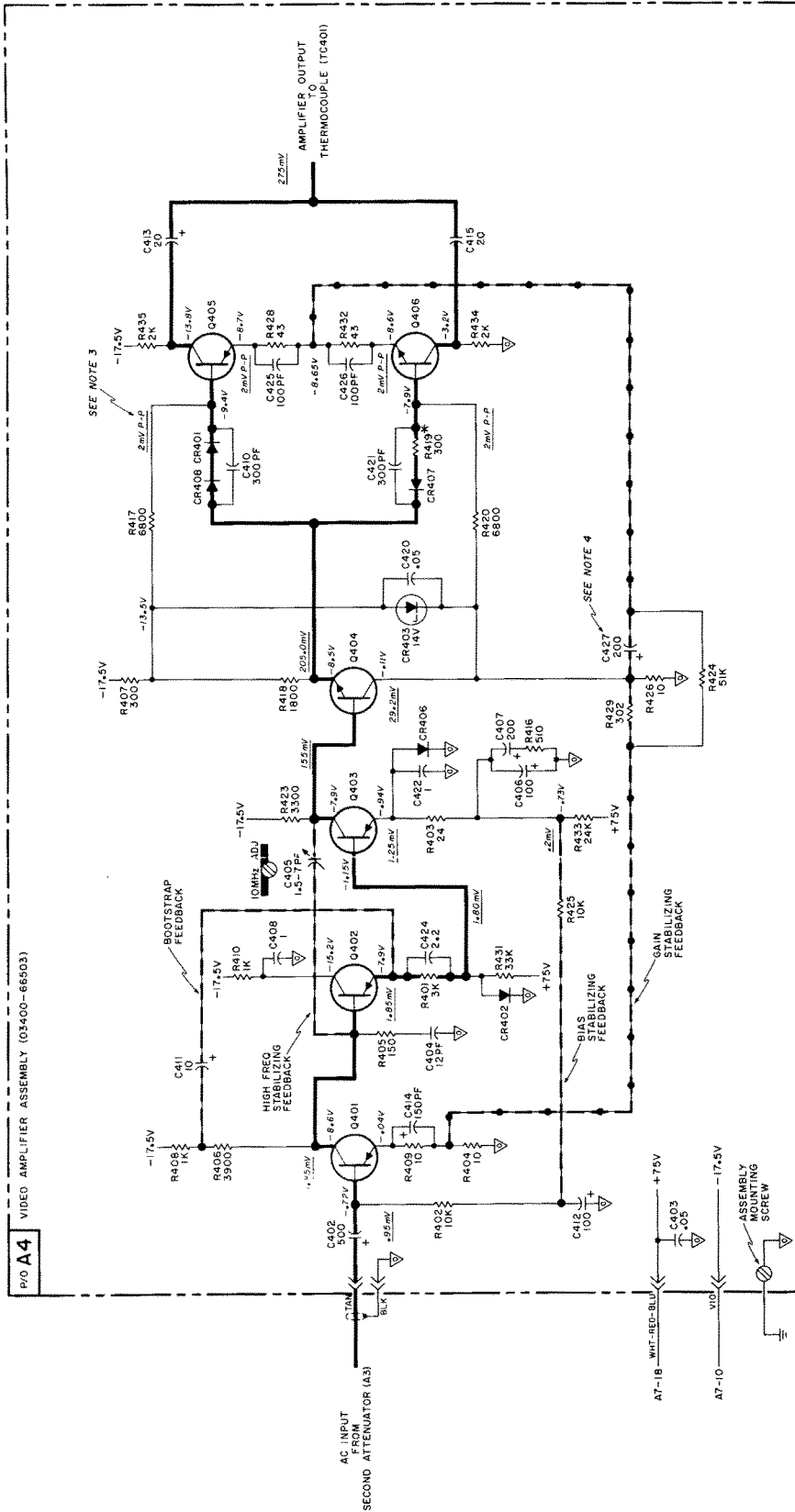
4-24. The ac input signal from the second attenuator is coupled through C402 to the base of input amplifier Q401. Q401, a class A amplifier, amplifies and inverts the signal which is then direct coupled to the base of bootstrap amplifier Q402. The output, taken from Q402 emitter is applied to the base of Q403 and fed back to the top of R406 as a bootstrap feedback. This positive ac feedback increases the effective ac resistance of R406 allowing a greater portion of the signal to be felt at the base of Q402. In this manner, the effective ac gain of Q401 is increased for the mid-band frequencies without disturbing the static operating voltages of Q401.

4-25. Driver amplifier Q403 further amplifies the ac signal and the output at Q403 collector is fed to the base circuit emitter follower Q404. The feedback path from the collector of Q403 to the base of Q402 through C405 (10 MHz ADJ) prevents spurious oscillations at high input frequencies. A dc feedback loop exists from the emitter circuit of Q403, to the base of Q401 through R425. This feedback stabilizes the Q401 bias voltage. Emitter follower Q404 acts as a driver for the output amplifier consisting of Q405 and Q406; a complimentary pair operating as a push-pull amplifier. The video amplifier output is taken from the collectors of the output amplifiers and applied to thermocouples TC401. A gain stabilizing feedback is developed in the emitter circuits of the output amplifiers. This negative feedback is applied to the emitter of input amplifier Q401 and establishes the overall gain of the video amplifier.

4-26. Trimmer capacitor C405 is adjusted at 10 MHz for frequency response of the video amplifier. Diodes CR402 and CR406 are protection diodes which prevent voltage surges from damaging transistors in the video amplifier. CR401, CR407, and CR408 are temperature compensating diodes to maintain the zero signal balance condition in the output amplifier over the operating temperature range. CR403, a breakdown diode, establishes the operating potentials for the output amplifier.

If that's not enough to make you propose marriage to modern high speed monolithic amplifiers, consider the design heroics spent on the thermal converter.

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Figure A3. H-P's Wideband Amplifier, the "Video Amplifier Assembly" Contained DC and AC Feedback Loops, Peaking Networks, Bootstrap Feedback and Other Subtleties to Equal Figure 22's Performance

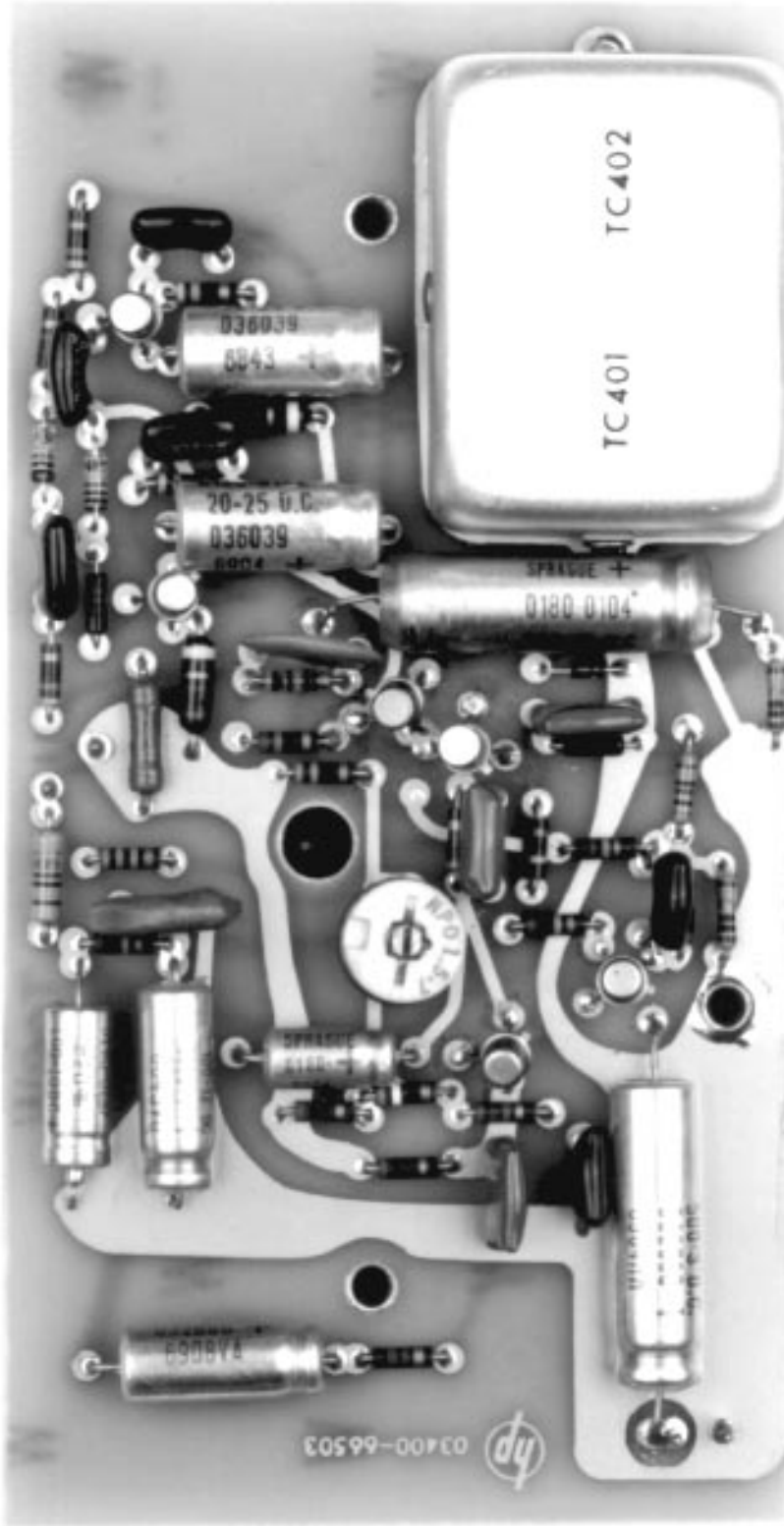


Figure A4. The Voltmeters "Video Amplifier" Received Input at Board's Left Side. Amplifier Output Drive Shrouded Thermal Converter at Lower Right. Note High Frequency Response Trimmer Capacitor at Left Center

4-27. PHOTOCHOPPER ASSEMBLY A5, CHOPPER AMPLIFIER ASSEMBLY A6, AND THERMOCOUPLE PAIR (PART OF A4).

4-28. The modulator/demodulator, chopper amplifier, and thermocouple pair form a servo loop which functions to position the direct reading meter M1 to the rms value of the ac input signal⁴. See modulator/demodulator, chopper amplifier, and thermocouple pair schematic diagram illustrated in Figure 6-3.

4-29. The video amplifier output signal is applied to the heater of thermocouple TC401. This ac voltage causes a dc voltage to be generated in the resistive portion of TC401 which is proportional to the heating effect (rms value) of the ac input. The dc voltage is applied to photocell V501.

4-30. Photocells V501 and V502 in conjunction with neon lamps DS501 and DS502 form a modulator circuit⁵. The neon lamps are lighted alternately between 90 and 100 Hz. Each lamp illuminates one of the photocells. DS501 illuminates V501; DS502 illuminates V502. When a photocell is illuminated it has a low resistance compared to its resistance when dark. Therefore, when V501 is illuminated, the output of thermocouple TC401 is applied to the input of the chopper amplifier through V501. When V502 is illuminated, a ground signal is applied to the chopper amplifier. The alternate illumination of V501 and V502 modulates the dc input at a frequency between 90 and 100 Hz. The modulator output is a square wave whose amplitude is proportional to the dc input level.

4-31. The chopper amplifier, consisting of Q601 through Q603, is a high gain amplifier which amplifies the square wave developed by the modulator. Power supply voltage variations are reduced by diodes CR601 thru CR603. The amplified output is taken from the collector of Q603 and applied to the demodulator through emitter follower Q604.

4-32. The demodulator comprises two photocells, V503 and V504, which operate in conjunction with DS501 and DS502; the same neon lamps used to illuminate the photocells in the modulator. Photocells V503 and V504 are illuminated by DS501 and DS502, respectively.

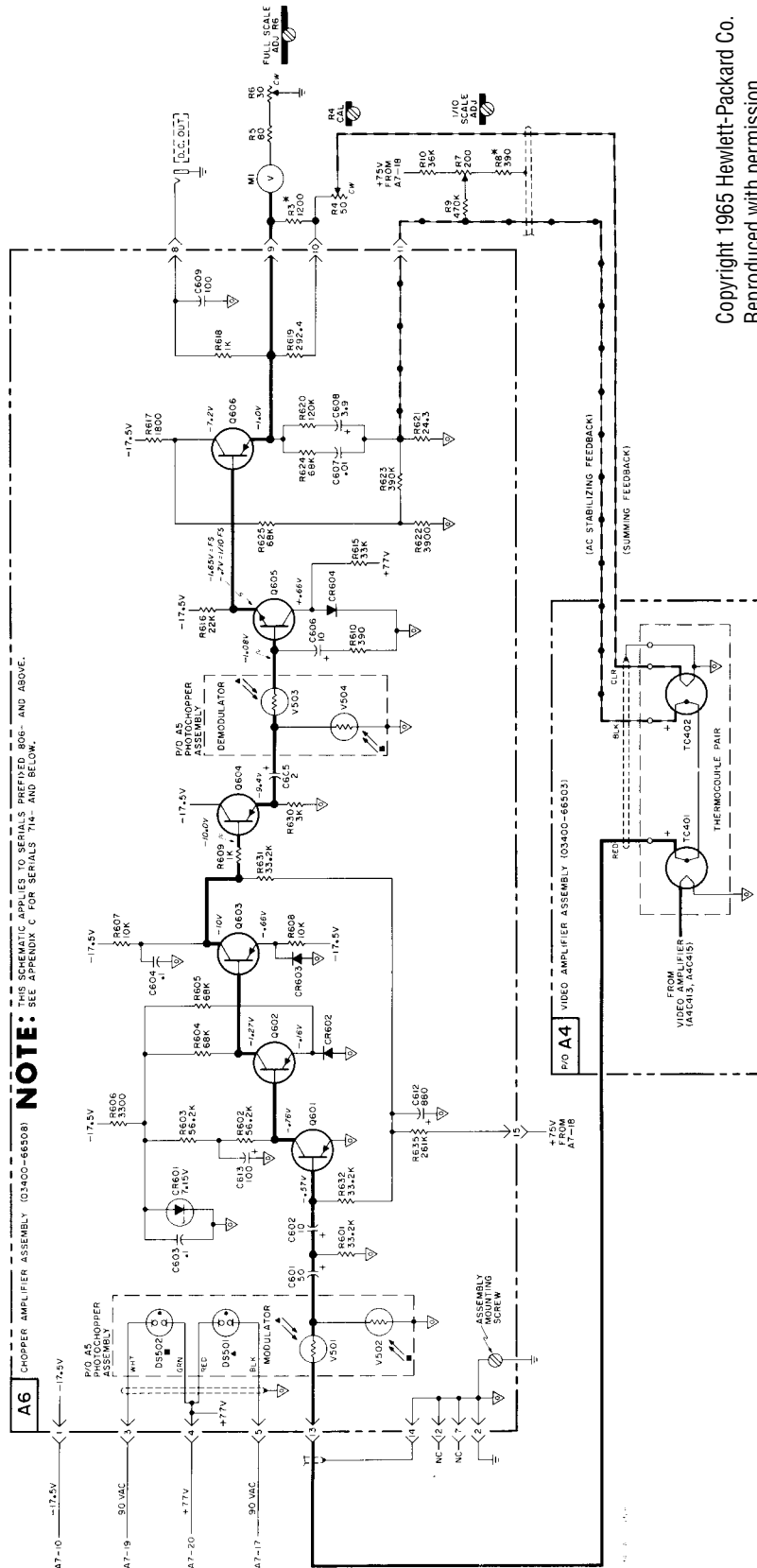
4-33. The demodulation process is the reverse of the modulation process discussed in Paragraph 4-30. The output of the demodulator is a dc level which is proportional to the demodulator input. The magnitude and phase of the input square wave determines the magnitude and polarity of the dc output level. This dc output level is applied to two emitter follower output stages.

4-34. The emitter follower is needed to match the high output impedance of the demodulator to the low input impedance of the meter and thermocouple circuits. The voltage drop across CR604 in the collector circuit of Q605 is the operating bias for Q604. This fixed bias prevents Q605 failure when the base voltage is zero with respect to ground.

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Note 4: In 1965 almost all thermal converters utilized matched pairs of discrete heater resistors and thermocouples. The thermocouples' low level output necessitated chopper amplifier signal conditioning, the only technology then available which could provide the necessary DC stability.

Note 5: The low level chopping technology of the day was mechanical choppers, a form of relay. H-P's use of neon lamps and photocells as microvolt choppers was more reliable and an innovation. Hewlett-Packard has a long and successful history of using lamps for unintended purposes.



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Figure A5. H-P's Thermal Converter ("A4") and Control Amplifier ("A6") Perform Similarly to Text Figure 22's Dual Op Amp. Circuit Realization Required Far More Attention to Details

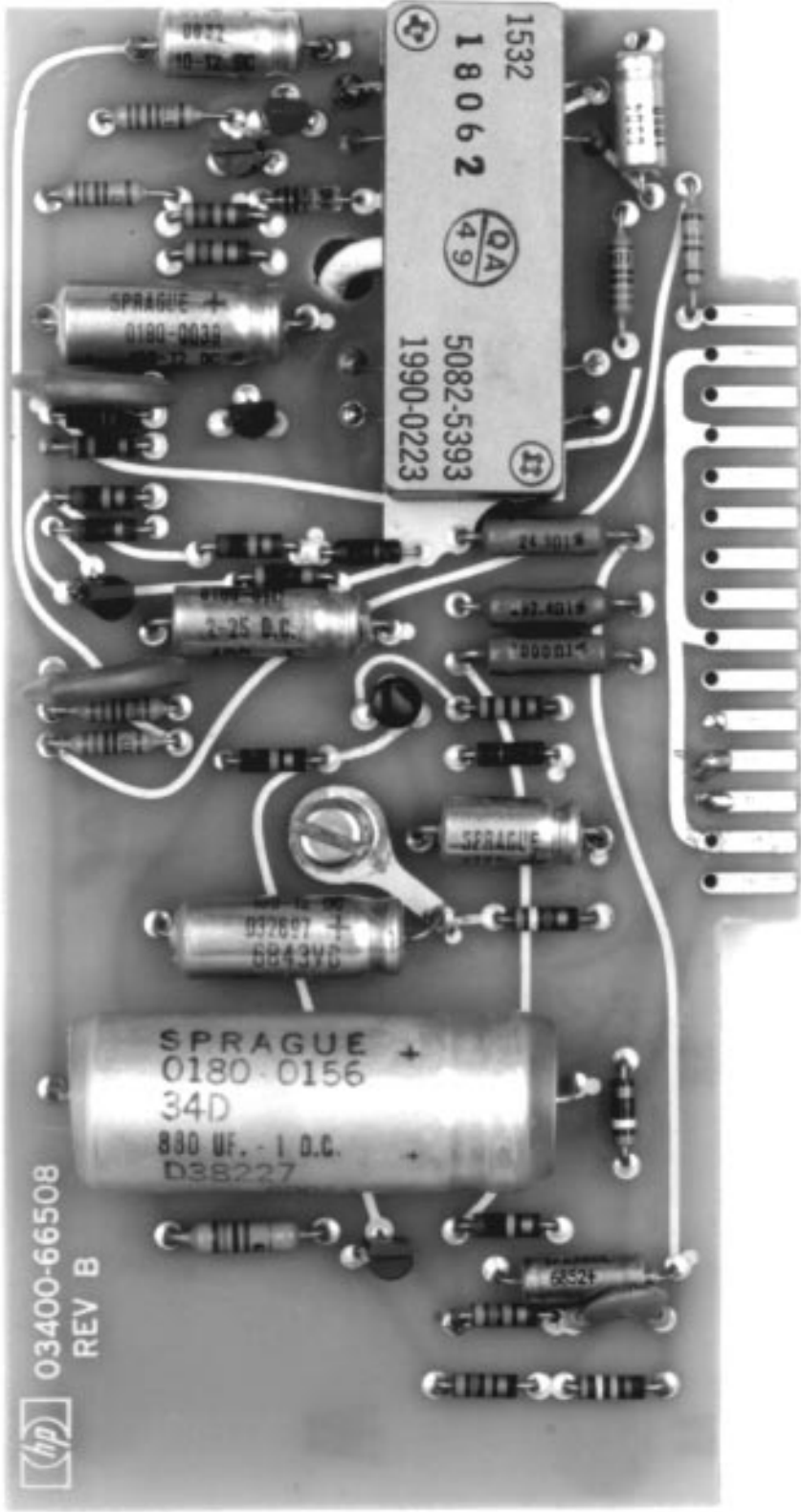


Figure A6. Chopper Amplifier Board Feedback Controlled the Thermal Converter. Over Fifty Components Were Required, Including Neon Lamps, Photocells and Six Transistors. Photo-Chopper Assembly Is at Board's Lower Right

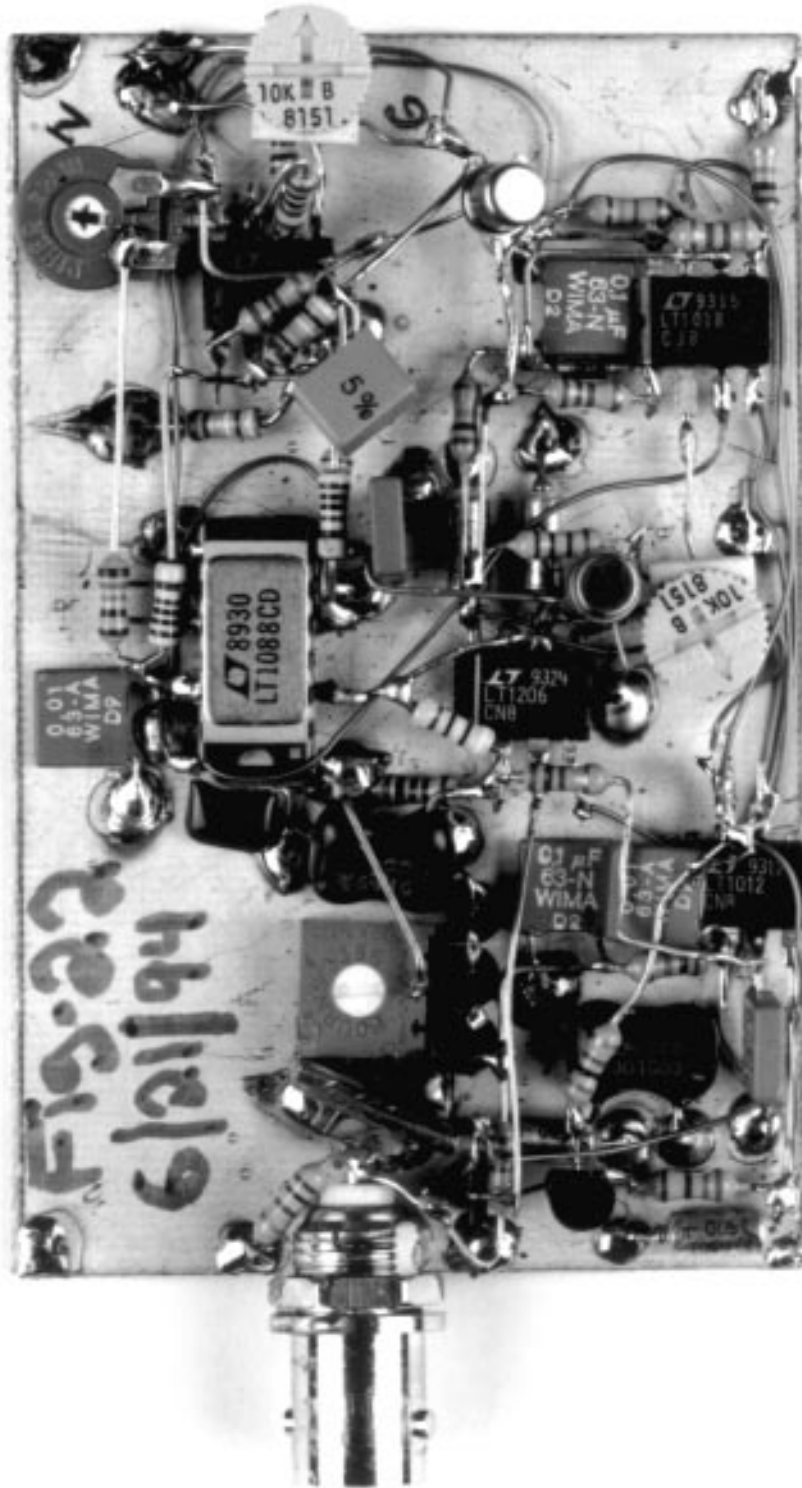


Figure A7. Figure 22's Circuit Puts Entire HP3400 Electronics on One Small Board. FET Buffer-LT1206 Amplifier Appear Left Center Behind BNC Shield. LT1088 IC (Upper Center) Replaces Thermal Converter. LT1013 (Upper Right) Based Circuitry Replaces Photo-Chopper Board. LT1018 and Components (Lower Right) Provide Overload Protection. Ain't Modern ICs Wonderful?

Application Note 61

4-35. The dc level output, taken from the emitter of Q606, is applied to meter M1 and to the heating element of thermocouple TC402. The dc voltage developed in the resistive portion of TC402 is effectively subtracted from the voltage developed by TC401. The input signal to the modulator then becomes the difference in the dc outputs of the two thermocouples. When the difference between the two thermocouples becomes zero the dc from the emitter followers (driving the meter) will be equal to the ac from the video amplifier.

4-36. Noise on the modulated square wave is suppressed by feedback from emitter of Q606 through C607 and C608 to the resistive element of TC402.

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When casually constructing a wideband amplifier with a few mini-DIPs, the reader will do well to recall the pain and skill expended by the HP3400A's designers some 30 years ago.

Incidentally, what were *you* doing in 1965?

APPENDIX B

Symmetrical White Gaussian Noise

by Ben Hessen-Schmidt,
NOISE COM, INC.

White noise provides instantaneous coverage of all frequencies within a band of interest with a very flat output spectrum. This makes it useful both as a broadband stimulus and as a power-level reference.

Symmetrical white Gaussian noise is naturally generated in resistors. The noise in resistors is due to vibrations of the conducting electrons and holes, as described by Johnson and Nyquist.¹ The distribution of the noise voltage is symmetrically Gaussian, and the average noise voltage is:

$$\bar{V}_n = 2\sqrt{kT \int R(f) p(f) df} \quad (1)$$

Where:

- k = 1.38E-23 J/K (Boltzmann's constant)
- T = temperature of the resistor in Kelvin
- f = frequency in Hz
- h = 6.62E-34 Js (Planck's constant)
- R(f) = resistance in ohms as a function of frequency

$$p(f) = \frac{hf}{kT[\exp(hf/kT) - 1]} \quad (2)$$

Note 1: See "Additional Reading" at end of this section.

$p(f)$ is close to unity for frequencies below 40GHz when T is equal to 290°K. The resistance is often assumed to be independent of frequency, and $\int df$ is equal to the noise bandwidth (B). The available noise power is obtained when the load is a conjugate match to the resistor, and it is:

$$N = \frac{\bar{V}_n^2}{4R} = kTB \quad (3)$$

where the "4" results from the fact that only half of the noise voltage and hence only 1/4 of the noise power is delivered to a matched load.

Equation 3 shows that the available noise power is proportional to the temperature of the resistor; thus it is often called thermal noise power, Equation 3 also shows that white noise power is proportional to the bandwidth.

An important source of symmetrical white Gaussian noise is the noise diode. A good noise diode generates a high level of symmetrical white Gaussian noise. The level is often specified in terms of excess noise ratio (ENR).

$$\text{ENR (in dB)} = 10\text{Log} \frac{(T_e - 290)}{290} \quad (4)$$

T_e is the physical temperature that a load (with the same impedance as the noise diode) must be at to generate the same amount of noise.

The ENR expresses how many times the effective noise power delivered to a non-emitting, nonreflecting load exceeds the noise power available from a load held at the reference temperature of 290°K (16.8°C or 62.3°F).

The importance of high ENR becomes obvious when the noise is amplified, because the noise contributions of the amplifier may be disregarded when the ENR is 17dB larger than the noise figure of the amplifier (the difference in total noise power is then less than 0.1dB). The ENR can easily be converted to noise spectral density in dBm/Hz or $\mu\text{V}/\sqrt{\text{Hz}}$ by use of the white noise conversion formulas in Table 1.

Table 1. Useful White Noise conversion

dBm	=	dBm/Hz + 10log (BW)
dBm	=	20log (\bar{V}_n) – 10log(R) + 30dB
dBm	=	20log(\bar{V}_n) + 13dB for R = 50 Ω
dBm/Hz	=	20log($\mu\bar{V}_n\sqrt{\text{Hz}}$) – 10log(R) – 90dB
dBm/Hz	=	–174dBm/Hz + ENR for ENR > 17dB

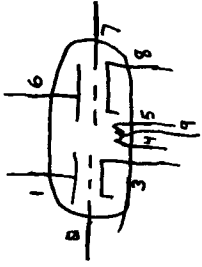
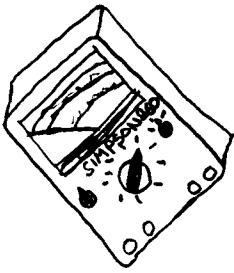
When amplifying noise it is important to remember that the noise voltage has a Gaussian distribution. The peak voltages of noise are therefore much larger than the average or RMS voltage. The ratio of peak voltage to RMS voltage is called crest factor, and a good crest factor for Gaussian noise is between 5:1 and 10:1 (14 to 20dB). An amplifier's 1dB gain-compression point should therefore be typically 20dB larger than the desired average noise-output power to avoid clipping of the noise.

For more information about noise diodes, please contact NOISE COM, INC. at (201) 261-8797.

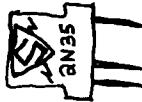
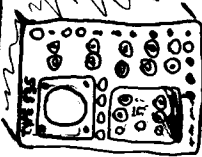
Additional Reading

1. Johnson, J.B, "Thermal Agitation of Electricity in Conductors," *Physical Review*, July 1928, pp. 97-109.
2. Nyquist, H. "Thermal Agitation of Electric Charge in Conductors," *Physical Review*, July 1928, pp. 110-113.

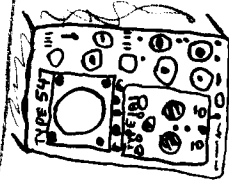
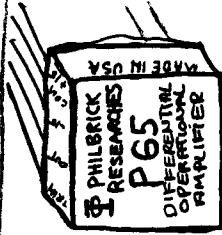
When I WAS 6 YEARS OLD
 ALL I WANTED TO DO WAS MAKE
 CIRCUITS WITH 12AX7s & 6L6s.



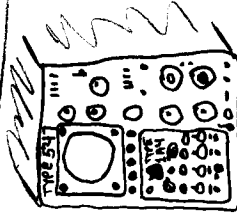
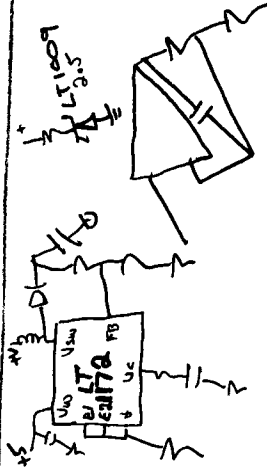
When I WAS 10 I got
 2N35s & CK-722s.
 No Filaments. wow!



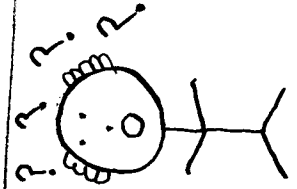
When I WAS 17 I used
 Philbrick P-65s. You
 could do anything



Now, I'm 46 & I CAN HACK
 ALL the op-amps and switching
 Regulators I WANT. EVERY DAY!



Is The Mid-Life Crisis when They
 Run out of 10K Resistors?



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A Fourth Generation of LCD Backlight Technology

Component and Measurement Improvements Refine Performance

Jim Williams

PREFACE

Current generation portable computers and instruments utilize backlit LCDs (Liquid Crystal Displays). These displays have also appeared in applications ranging from medical equipment to automobiles, gas pumps and retail terminals. Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps require high voltage AC to operate, mandating an efficient high voltage DC/AC converter. In addition to good efficiency, the converter should deliver the lamp drive in sine wave form. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency. The sine wave excitation also provides optimal current-to-light conversion in the lamp. The circuit should permit lamp control from zero to full brightness with no hysteresis or "pop-on," and must also regulate lamp intensity vs power supply variations.

The small size and battery-powered operation associated with LCD equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is usually a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including

PC board and all hardware, usually must fit within the LCD enclosure with a height restriction of 0.25 inches.

A practical, efficient LCD backlight design is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and the physical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing and other items have a major effect on electrical characteristics. The greatest care in every detail is required to achieve a practical high efficiency LCD backlight. Getting the lamp to light is just the beginning!

First generation backlights were crude, with poor performance in almost all areas. LTC (Linear Technology Corporation) has introduced feedback stabilization and optimized lamp driving configurations in three successive generations of technology. The effort has culminated in dedicated ICs for backlight driving.

This fourth publication reviews our recent work in components and measurement techniques applicable to LCD backlighting. Theoretical considerations are presented with practical suggestions, remedies and circuits. As always, we welcome reader comments, questions and requests for consultation.

TABLE OF CONTENTS

INTRODUCTION	AN65-4
PERSPECTIVES ON DISPLAY EFFICIENCY	AN65-5
Cold Cathode Fluorescent Lamps (CCFLs)	AN65-5
CCFL Load Characteristics	AN65-7
Display and Layout Losses	AN65-8
Considerations for Multilamp Designs	AN65-31
CCFL Power Supply Circuits	AN65-32
Low Power CCFL Power Supplies	AN65-37
High Power CCFL Power Supply	AN65-39
“Floating” Lamp Circuits	AN65-40
IC-Based Floating Drive Circuits	AN65-43
High Power Floating Lamp Circuit	AN65-46
Selection Criteria for CCFL Circuits	AN65-46
Summary of Circuits	AN65-49
General Optimization and Measurement Considerations	AN65-52
Electrical Efficiency Optimization and Measurement	AN65-53
Electrical Efficiency Measurement	AN65-55
Feedback Loop Stability Issues	AN65-55
REFERENCES	AN65-59
APPENDIX A	AN65-60
“HOT” CATHODE FLUORESCENT LAMPS	AN65-60
APPENDIX B	AN65-60
MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS	AN65-60
Introduction	AN65-60
Flatness and Rigidity of the Bezel	AN65-61
Avoiding Heat Buildup in the Display	AN65-61
Placement of the Display Components	AN65-62
Protecting the Face of the Display	AN65-62
APPENDIX C	AN65-63
ACHIEVING MEANINGFUL EFFICIENCY MEASUREMENTS	AN65-63
Current Probe Circuitry	AN65-64
Current Calibrator	AN65-67
Voltage Probes for Grounded Lamp Circuits	AN65-70
Voltage Probes for Floating Lamp Circuits	AN65-72
Differential Probe Calibrator	AN65-76
RMS Voltmeters	AN65-82
Calorimetric Correlation of Electrical Efficiency Measurements	AN65-84
APPENDIX D	AN65-87
PHOTOMETRIC MEASUREMENTS	AN65-87

APPENDIX E	AN65-92
OPEN LAMP/OVERLOAD PROTECTION	AN65-92
Overload Protection	AN65-93
APPENDIX F	AN65-94
INTENSITY CONTROL AND SHUTDOWN METHODS	AN65-94
About Potentiometers	AN65-96
Precision PWM Generator	AN65-98
APPENDIX G	AN65-99
LAYOUT, COMPONENT AND EMISSIONS CONSIDERATIONS	AN65-99
Circuit Segmenting	AN65-99
High Voltage Layout	AN65-99
Discrete Component Selection	AN65-106
Basic Operation of Converter	AN65-107
Requisite Transistor Characteristics	AN65-108
Additional Discrete Component Considerations	AN65-110
Emissions	AN65-110
APPENDIX H	AN65-110
LT [®] 1172 OPERATION FROM HIGH VOLTAGE INPUTS	AN65-110
APPENDIX I	AN65-111
ADDITIONAL CIRCUITS	AN65-111
Desktop Computer CCFL Power Supply	AN65-111
Dual Transformer CCFL Power Supply	AN65-112
HeNe Laser Power Supply	AM65-113
APPENDIX J	AN65-114
LCD CONTRAST CIRCUITS	AN65-114
Dual Output LCD Bias Voltage Generator	AN65-115
LT118X Series Contrast Supplies	AN65-116
APPENDIX K	AN65-119
WHO WAS ROYER, AND WHAT DID HE DESIGN?	AN65-119
APPENDIX L	AN65-120
A LOT OF CUT OFF EARS AND NO VAN GOGHS/Some Not-So-Great Ideas	AN65-120
Not-So-Great Backlight Circuits	AN65-120
Not-So-Great Primary Side Sensing Ideas	AN65-122

Application Note 65

INTRODUCTION

This scribing marks the fourth LTC publication in as many years concerning LCD illumination.¹ The extraordinary user response to previous efforts has resulted in a continuing LCD backlight development effort by our company. This level of interest, along with significant performance advances since the last publication, justifies further discussion of LCD backlighting.

Development of attractive solutions for LCD illumination has necessitated the longest sustained LTC application engineering effort to date. A single circuit in a 1991 publication (*Measurement and Control Circuit Collection*, LTC Application Note 45, June 1991) has resulted in four years of continuous investigation, summarized in three successive, dedicated publications.

The impetus for all this bustle has been an overwhelming and continuously ascending reader response. Practical, high performance LCD backlighting solutions are needed in a wide range of applications. The optical, transductive and electronic aspects combine (conspire?) to present an extraordinarily challenging problem. The LCD backlight problem's interdisciplinary nature, along with highly interactive effects, provides an exquisitely subtle engineering exercise. Backlights present the most complex set of interdependencies the author has ever encountered. Our academic interest in this challenge is, of course, well

patinaed with capitalistic intent. Substantial comfort arrives with the certainty that the audience is similarly acculturated.

This publication includes pertinent information from previous efforts in addition to updated sections and a large body of new material. The partial repetition is a small penalty compared to the benefits of text flow, completeness and time efficient communication. Older material has been altered, abridged or augmented as appropriate, while simultaneously introducing new findings. Previous work has emphasized obtaining and verifying high efficiency. This characteristic is still quite desirable, but other backlight requirements have become evident. These include low voltage operation, improved system interface, minimization of display-induced losses, circuitry compaction and better measurement/optimization techniques. These advances have been enabled by development of new ICs and instrumentation.

Finally, this preamble must appreciate the text's arrangement and review by various LTC personnel and customers. They transmuted a psychotic uproar of a manuscript into this finessed presentation. Hopefully, readers will join the author in applause.

Note 1. Previous publications are annotated in References 1, 18 and 25.

PERSPECTIVES ON DISPLAY EFFICIENCY

The LCD displays currently available require two power sources, a backlight supply and a contrast supply. The display backlight is the single largest power consumer in a typical portable apparatus, accounting for almost 50% of battery drain with the display at maximum intensity. As such, every effort must be expended to maximize backlight efficiency.

Study of LCD energy management should consider the problem from an interdisciplinary viewpoint. The backlight presents a cascaded energy attenuator to the battery (Figure 1). Battery energy is lost in the electrical-to-electrical conversion to high voltage AC to drive the CCFL. This section of the energy attenuator is the most efficient; conversion efficiencies exceeding 90% are possible. The CCFL, although the most efficient electrical-to-light converter available today, has losses exceeding 80%. Additionally, the optical transmission efficiency of present displays is under 10% for monochrome with color types much lower.

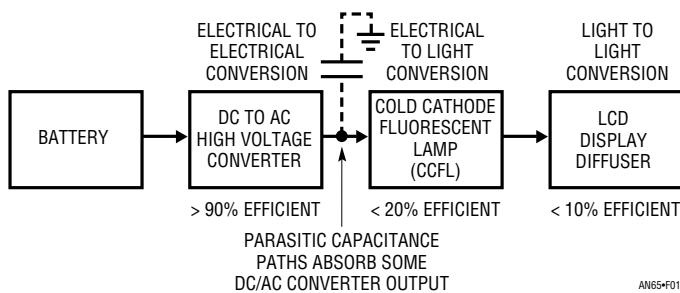


Figure 1. Backlit LCD Display Presents a Cascaded Energy Attenuator to the Battery. DC/AC Conversion is Significantly More Efficient Than Energy Conversions in Lamp and Display

The very high DC/AC conversion efficiency highlights some significant issues. Anything that improves energy transfer in the other “attenuator” areas will have greater impact than further electrical efficiency improvements. Additional improvements in electrical efficiency, while certainly desirable, are reaching the point of diminishing returns. Clearly, overall backlight efficiency gains must come from lamp and display improvements.

There is very little electrical workers can do to improve lamp and display efficiency besides call attention to the problems (see the following sections on lamps and displays).² Improvements are, however, possible in related

areas. In particular, the *form* of drive applied to the lamp is quite critical. The waveshape supplied to the lamp influences its current-to-light conversion efficiency. Thus, dissimilar waveforms containing equivalent power can produce different amounts of lamp light output. This implies that a more *electrically* efficient inverter with a nonoptimal output waveshape could produce less light than a “less efficient” inverter with a more appropriate waveform. Experiment reveals this to be true. As such, distinction between electrical and photometric efficiency is necessary and requires attention.

Another practical area where improvement is possible is transmission of inverter drive to the lamp. The high frequency AC waveform is subject to losses due to parasitic capacitances in the wiring and display. Controlling the parasitic capacitances and the manner in which lamp drive is applied can yield significant efficiency improvement.

Practical methods addressing both aforementioned areas are contained in subsequent sections of this publication.

Cold Cathode Fluorescent Lamps (CCFLs)

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are complex transducers, with many variables affecting their ability to convert electrical current to light. Factors influencing conversion efficiency include the lamp’s current, temperature, drive waveform characteristics, length, width, gas constituents and the proximity to nearby conductors.

These and other factors are interdependent, resulting in a complex overall response. Figures 2 through 8 show some typical characteristics. A review of these curves hints at the difficulty in predicting lamp behavior as operating conditions vary. The lamp’s current, temperature and warm-up time are clearly critical to emission, although electrical efficiency may not necessarily correspond to the best optical efficiency point. Because of this, both electrical and photometric evaluation of a circuit is often required. It is possible, for example, to construct a CCFL circuit with 94% electrical efficiency which produces less

Note 2. “Call attention to the problems” constitutes a pleasant euphemism for complaining. This publication’s section on displays presents such complaints in visual form along with suggested remedies.

Application Note 65

light output than an approach with 80% electrical efficiency. (See Appendix L, "A Lot of Cut Off Ears and No Van Goghs — Some Not-So-Good Ideas.") Similarly, the performance of a very well matched lamp/circuit combination can be severely degraded by a lossy display enclosure or excessive high voltage wire lengths. Display enclosures with too much conducting material near the lamp have huge losses due to capacitive coupling. A poorly designed display enclosure can easily degrade efficiency by 20%. High voltage wire runs typically cause 1% loss per inch of wire.

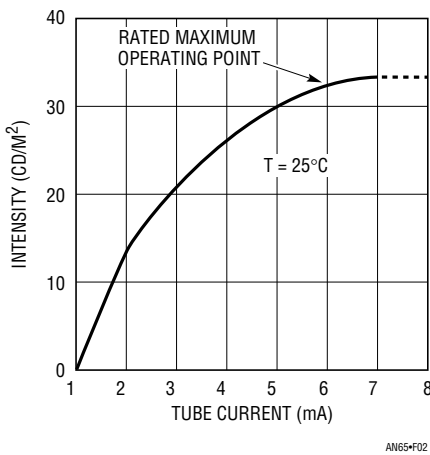


Figure 2. Emissivity for a Typical 5mA Lamp. Curve Flattens Badly Above 6mA

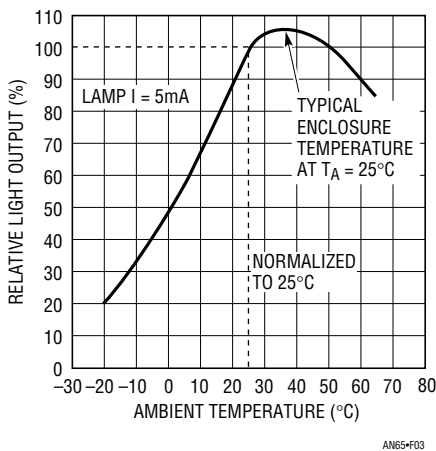


Figure 3. Ambient Temperature Effects on Emissivity of a Typical 5mA Lamp. Lamp and Enclosure Must Come to Thermal Steady State Before Measurements Are Made

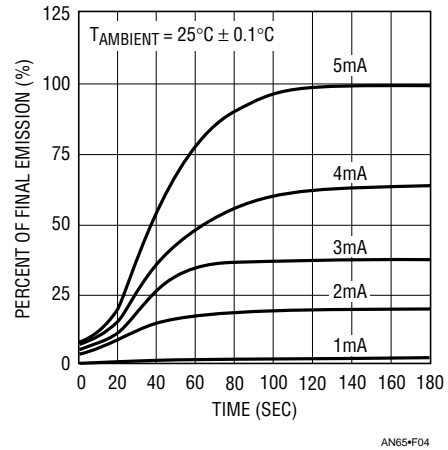


Figure 4. Emissivity vs On-Time for a Typical Lamp in Free Air. Lamp Must Arrive at Temperature Before Emission Stabilizes

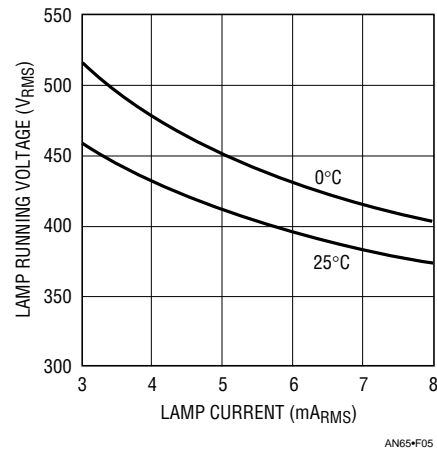


Figure 5. Lamp Current vs Voltage in the Operating Region. Note Large Temperature Coefficient

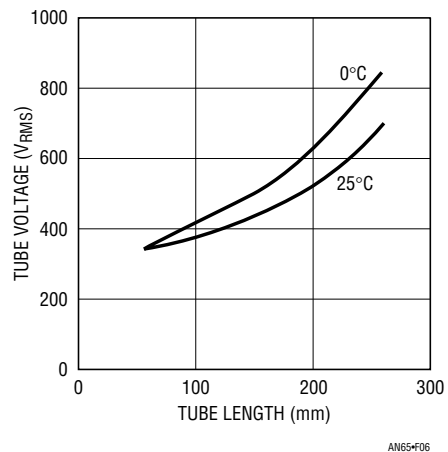


Figure 6. Running Voltage vs Lamp Length at Two Temperatures. Start-Up Voltages Are Usually 50% to 200% Higher Over Temperature

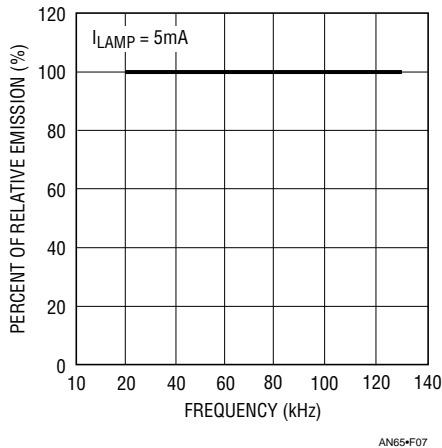


Figure 7. Lamp Emission vs Drive Frequency with Lamp in Free Space. No Change Is Measurable from 20kHz to 130kHz, Indicating Lamp Insensitivity to Frequency

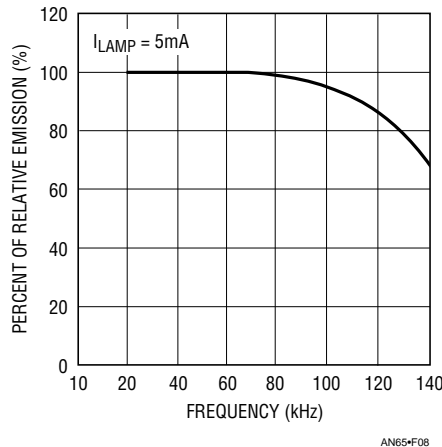


Figure 8. Figure 7's Lamp Shows Significant Emission vs Drive Frequency Degradation When Mounted in a Display. Cause Is Frequency-Dependent Loss Due to Display's Parasitic Capacitance Paths

The optimum drive frequency is determined by display and wiring losses, not lamp characteristics. Figure 7 shows lamp emissivity is essentially flat over a wide frequency range. Figure 8 shows results with the same lamp mounted in a typical display.

The apparent emissivity fall-off at high frequencies is caused by reduced lamp current due to parasitic capacitance-induced losses. As frequency increases, the display's parasitic capacitance diverts progressively more energy, lowering lamp current and emission. This effect is sometimes misinterpreted, leading to the mistaken conclusion that lamp emissivity degrades with increasing frequency.

CCFL Load Characteristics

These lamps are a difficult load to drive, particularly for a switching regulator. They have a “negative resistance” characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the start voltage is about 1000V, although higher and lower voltage lamps are common. Operating voltage is usually 300V to 500V, although other lamps may require different potentials. The lamps will operate from DC, but migration effects within the lamp will quickly damage it. As such, the waveform must be AC. No DC content should be present.

Figure 9a shows an AC driven lamp's characteristics on a curve tracer. The negative resistance-induced “snap-back” is apparent. In Figure 9b another lamp, acting against the curve tracer's drive, produces oscillation. These tenden-

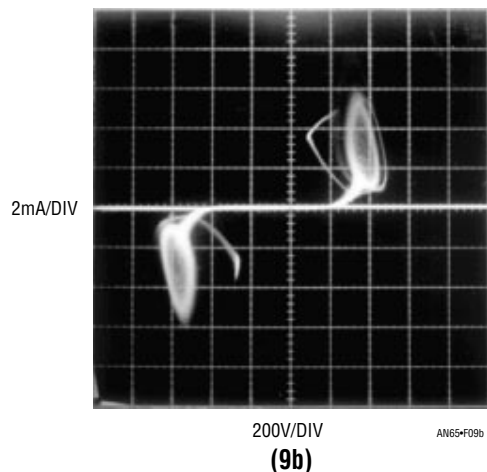
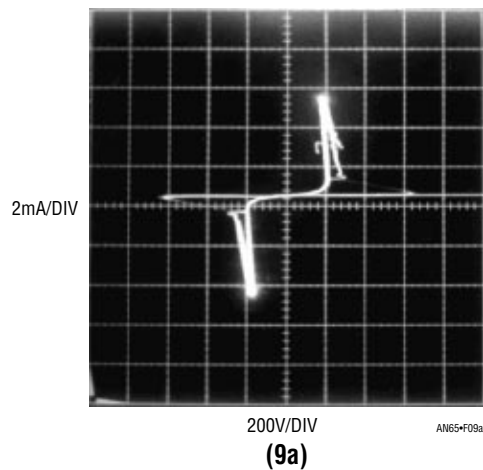


Figure 9. Negative Resistance Characteristic for Two CCFL Lamps. “Snap-Back” Is Readily Apparent, Causing Oscillation in 9b. These Characteristics Complicate Power Supply Design

Application Note 65

cies, combined with the frequency compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on start-up. Once the lamp is in its operating region it assumes a linear load characteristic, easing stability criteria. Lamp operating frequencies are typically 20kHz to 100kHz and a sine-like waveform is preferred. The sine drive's low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.³ A further benefit to the continuous sine drive is its low crest factor and controlled rise times, which are easily handled by the CCFL. CCFL's RMS current-to-light output efficiency and lifetime degrades with fast rise, high crest factor drive waveforms.⁴

Display and Layout Losses

The physical layout of the lamp, its leads, the display housing and other high voltage components are integral parts of the circuit. Placing the lamp into a display introduces pronounced electrical loading effects which must be considered. Poor layout can easily degrade efficiency by 25% and higher layout-induced losses have been observed. Producing an optimal layout requires attention to how losses occur. Figure 10 begins our study by examining potential parasitic paths between the transformer's output and the lamp. Parasitic capacitance to AC ground from any point between the power supply output and the lamp creates a path for undesired current flow. Similarly, stray coupling from any point along the lamp's length to AC ground induces parasitic current flow.

All parasitic current flow is wasted, causing the circuit to produce more energy to maintain desired current flow in the lamp. The high voltage path from the transformer to the display housing should be as short as possible to minimize losses. A good rule of thumb is to assume 1% efficiency loss per inch of high voltage lead. Any PC board traces, ground or power planes should be relieved by at least 1/4" in the high voltage area. This not only prevents losses but eliminates arcing paths.

Parasitic losses associated with lamp placement within the display housing require attention. High voltage wire length within the housing must be minimized, particularly for displays using metal construction. Ensure that the high voltage is applied to the shortest wire(s) in the display. This may require disassembling the display to verify wire length and layout. Another loss source is the reflective foil commonly used around lamps to direct light into the actual LCD. Some foil materials absorb considerably more field energy than others, creating loss. Finally, displays supplied in metal enclosures tend to be lossy. The metal absorbs significant energy and an AC path to ground is unavoidable. Direct grounding of metal enclosed displays further increases losses. Some display manufacturers have addressed this issue by relieving the metal in the lamp area with other materials. Losses introduced by the

Note 3. Many of the characteristics of CCFLs are shared by so-called "Hot" cathode fluorescent lamps. See Appendix A, "Hot" Cathode Fluorescent Lamps.

Note 4. See Appendix L, "A Lot of Cut Off Ears and No Van Goghs—Some Not-So-Great Ideas."

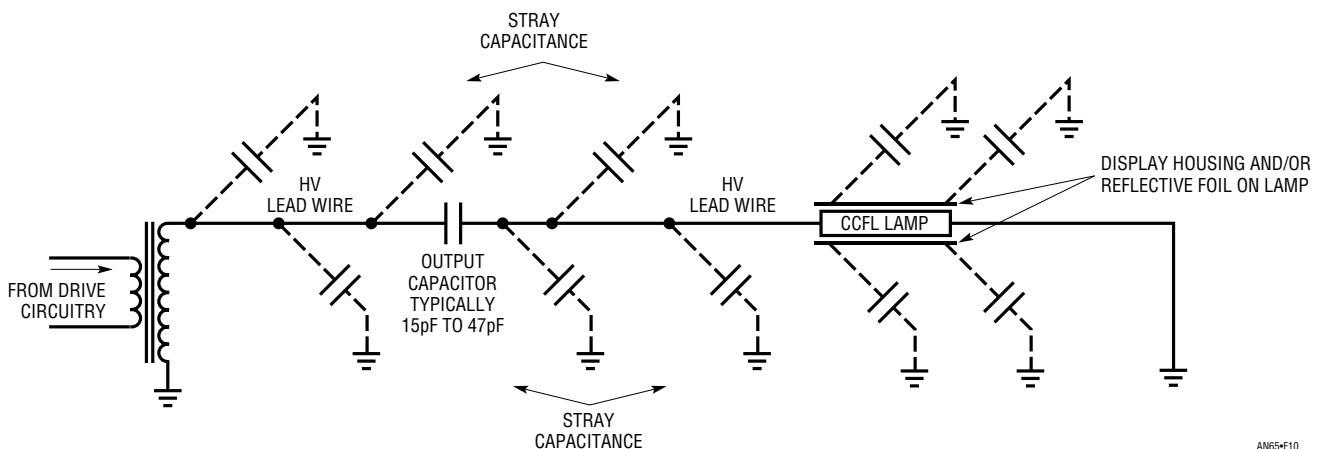


Figure 10. Loss Paths Due to Stray Capacitance in a Practical LCD Installation. Minimizing These Paths Is Essential for Good Efficiency

display are substantial and vary widely with different displays. These losses not only degrade overall efficiency, but complicate meaningful determination of the lamp current. Figure 11 shows effects of distributed parasitic capacitance loss paths on lamp current. The display housing and reflective foil-induced loss paths provide a continuous conduit for loss current flow. This results in a continuously varying value of “lamp current” along the lamp’s length. In cases where one end of the lamp is at or near ground, the current fall-off is greatest in the lamp’s high voltage regions. Although parasitic capacitance is usually uniformly distributed, its effect becomes far greater as voltage scales up.

These effects illustrate why designing around lamp specifications is such a frustrating exercise. Display vendors typically call out lamp operating parameters based on information received from the lamp manufacturer. Lamp vendors often determine operating characteristics in a completely different enclosure, or none at all. This set of uncertainties complicates design effort. The only viable solution is to determine lamp performance with the display of interest. This is the only practical way to maximize performance and ensure against overdriving the lamp, which wastes power and shortens lamp life.

In general, the display introduces parasitics which degrade performance. Latter portions of this text discuss some compensatory techniques, but the deleterious effects of display parasitics dominate practical backlight design.

There are some benefits to lossy displays. One advantage of display parasitics is that they effectively lower lamp breakdown voltage. The parasitic shunt capacitance along the tube’s length forms a distributed electrode, effectively shortening the breakdown path, lowering the lamp’s turn-on voltage. This accounts for the fact that many display mounted lamps start at lower voltages than the “naked” lamp breakdown voltage specification suggests. This effect aids low temperature start-up (see Figures 5 and 6).

A second potential advantage of distributed parasitic lamp capacitance is enhancement of low current operation. In some cases extended dimming range is possible because the parasitics provide a more evenly distributed field along the lamp’s length. This tends to maintain illumination along the lamp’s entire length at low operating currents, allowing low luminosity operation.

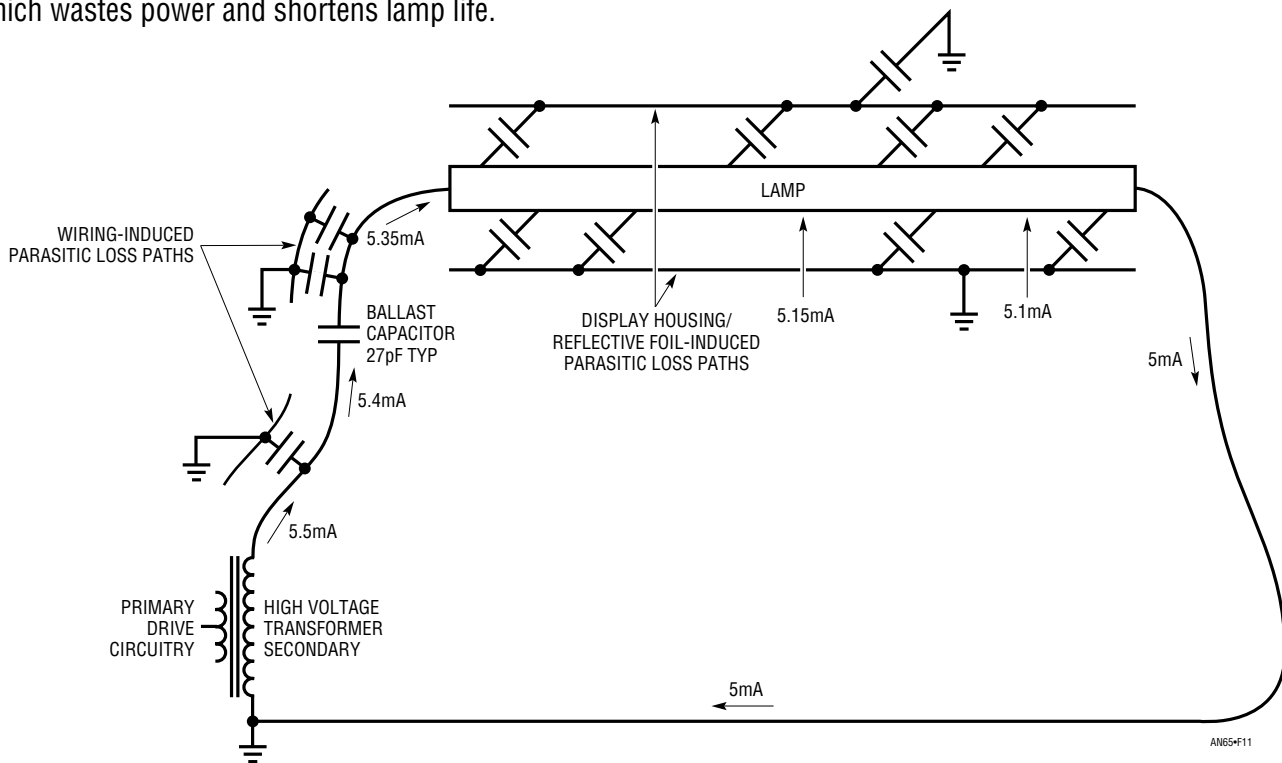
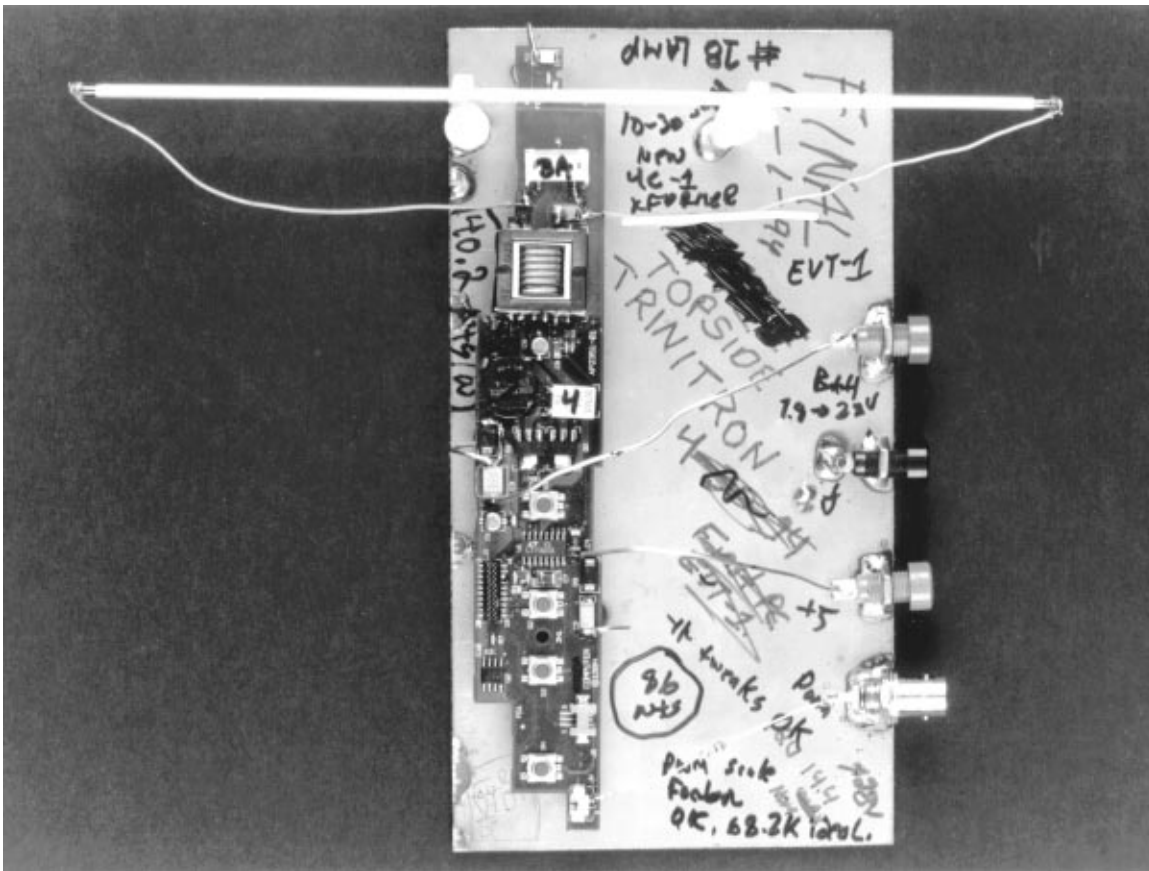


Figure 11. Distributed Parasitic Capacitances in a Practical Situation Cause Continuous Downward Shift in Measured “Lamp Current.” In This Case 0.5mA Is Lost to Parasitic Paths. Most Loss Occurs in High Voltage Regions

Application Note 65

The lessons here are clear. A thorough characterization of lamp/display losses is crucial to understanding trade-offs and obtaining the best possible performance. The highest efficiency “in system” backlights have been produced by careful attention to these issues. In some cases the entire display enclosure was re-engineered for lower losses.

The display loss issue, central to backlight design, merits detailed attention. The following briefly commented photographs (Figures 12 through 32) illustrate a variety of display situations. Hopefully, this visual tour will alert display users and manufacturers to the problems involved, promoting appropriate action by both.

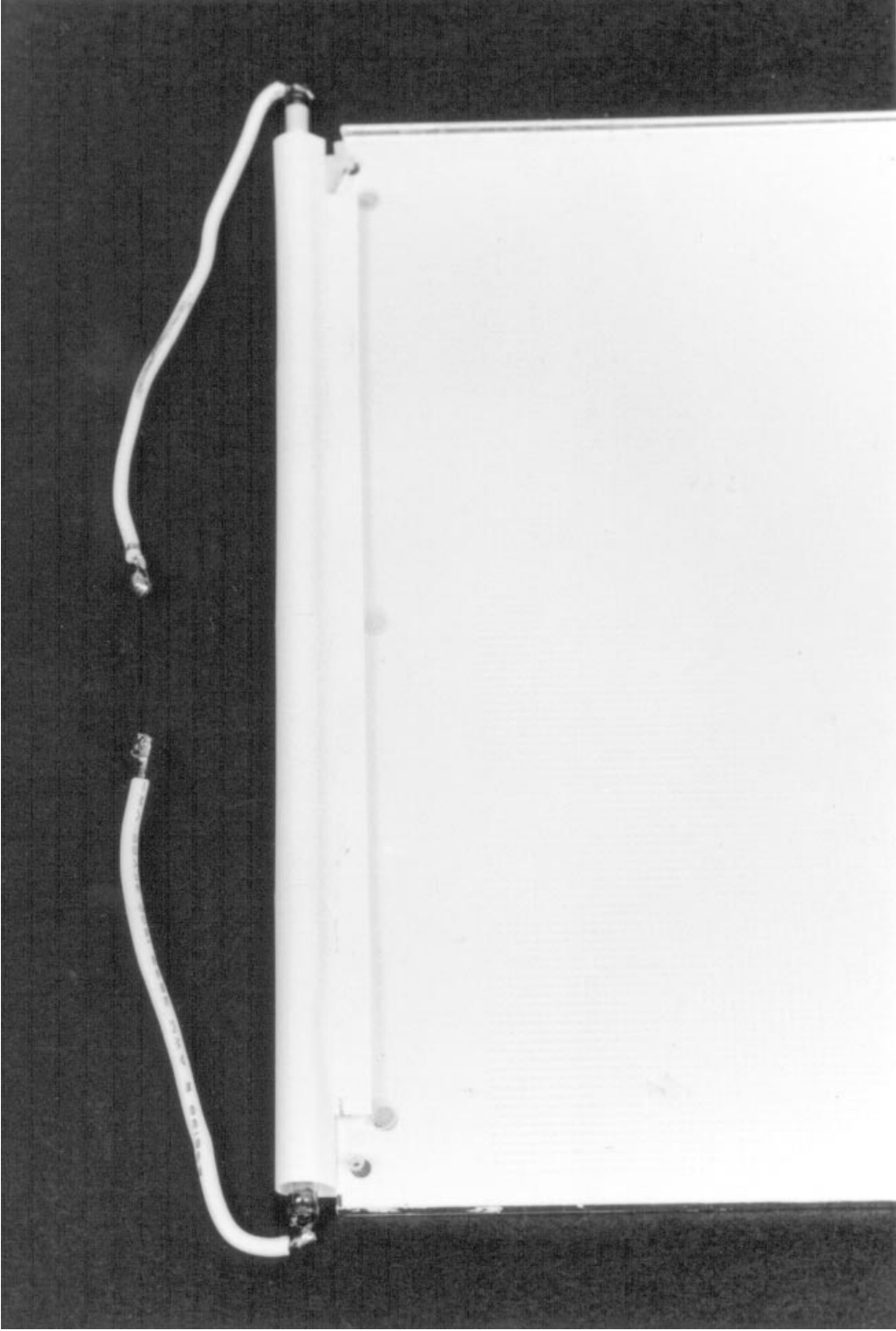


AN65-F12

Figure 12. The Ideal Display Is No Display. Drive Electronics Connected to a “Naked” Lamp Simulates a Zero Loss Display. Note Nylon Stand-Offs. Results Obtained Have No Relationship to Practical Display Driving



Figure 13. Measuring Lamp Wire to Display Frame Capacitance. Technique Gives Lead Wire-to-Frame Loss Information but Not Lamp-to-Foil-Or-Frame Loss Data. Lamp Must Be Energized Before Its Parasitics Are Measurable



AN65-F14

Figure 14. Low Loss Display Has No Metal in Lamp Region. Reflective Foil Floats from Ground and Has Low Absorption. Display Loss About 1.5%

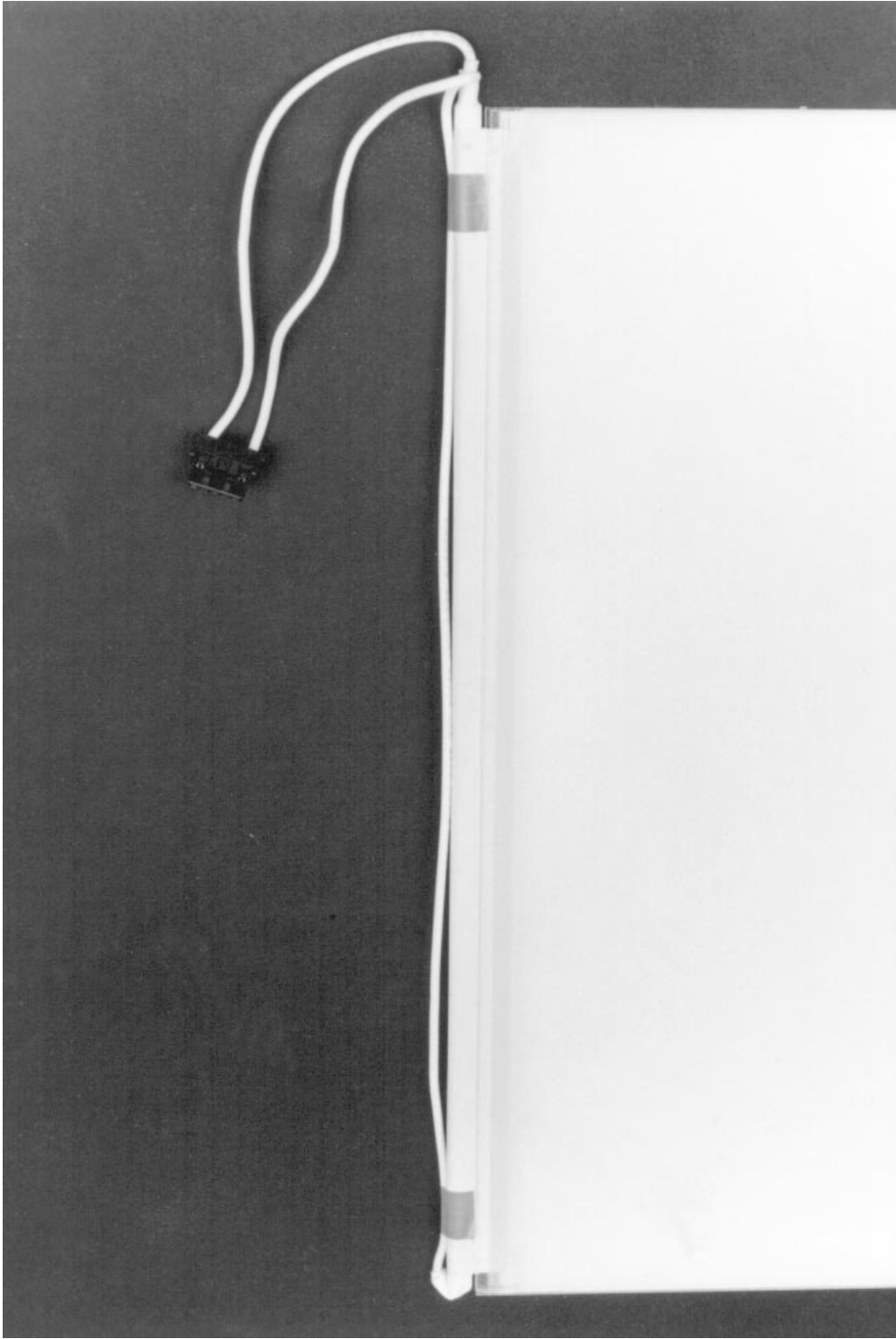
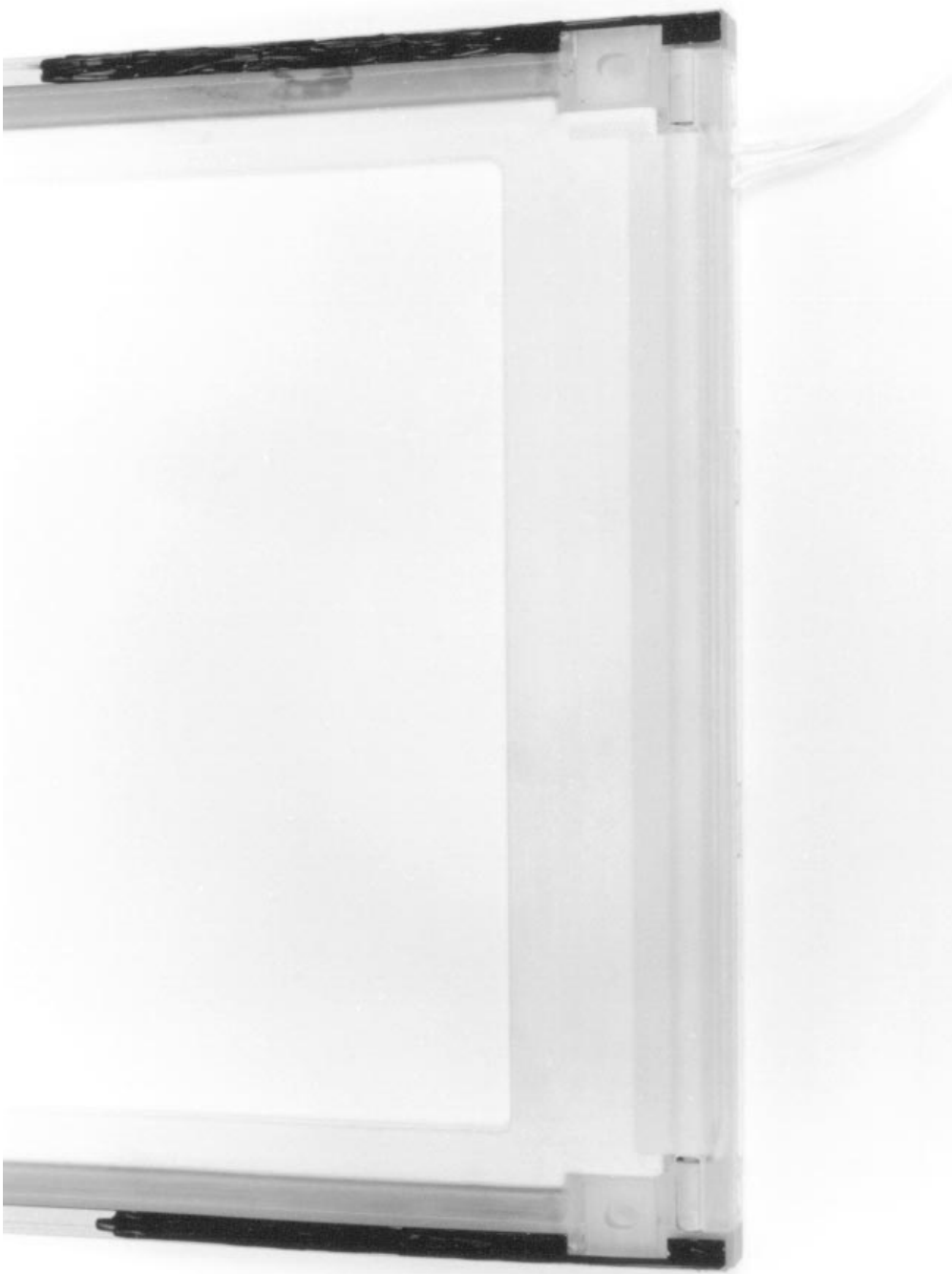
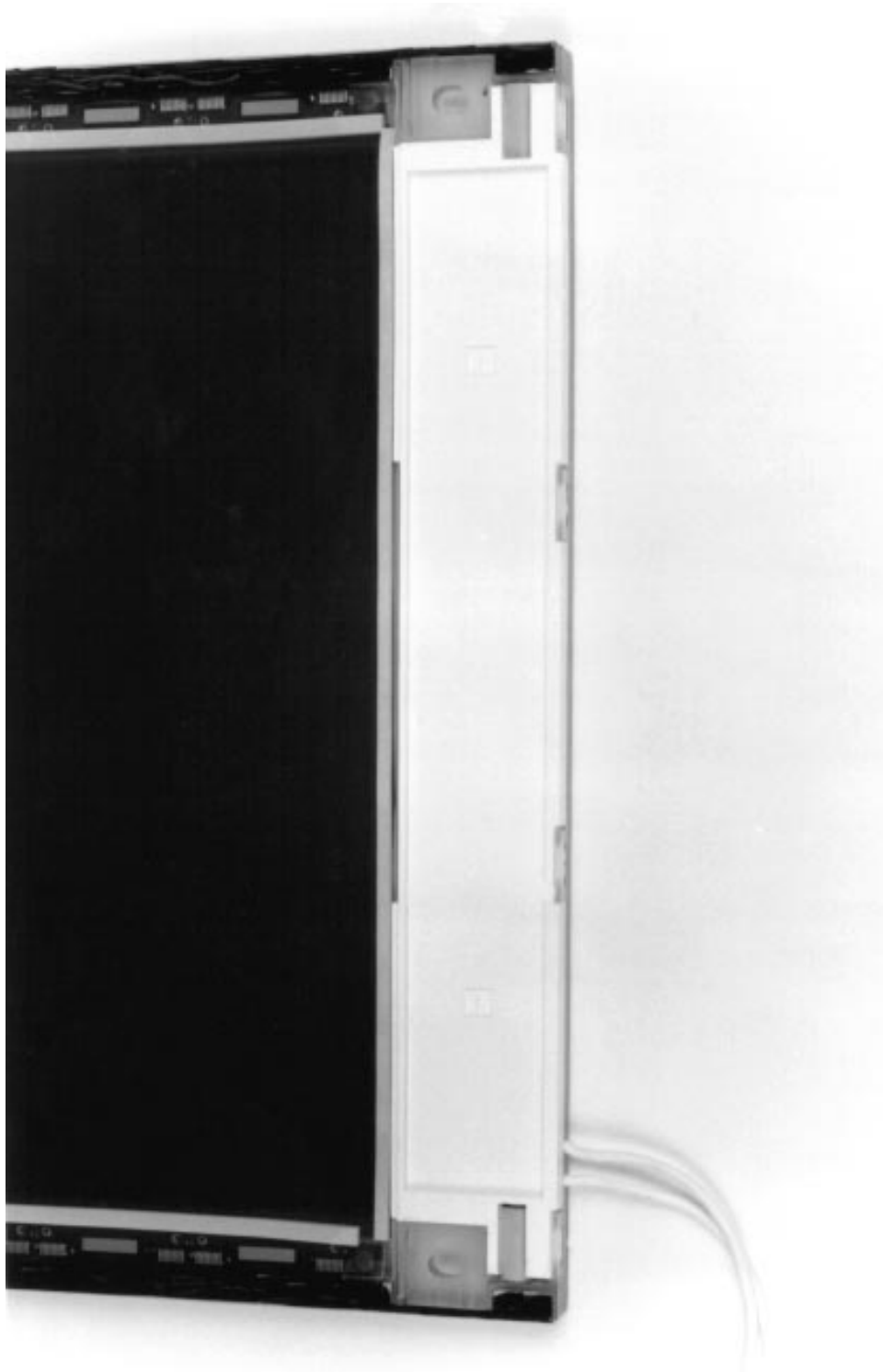


Figure 15. Another Low Loss Display Has Similar Characteristics to Figure 14. Running Long Wire Return Across Lamp Length Increases Loss to about 4%. Spacing Wire Away from Lamp Would Cut Loss by Half



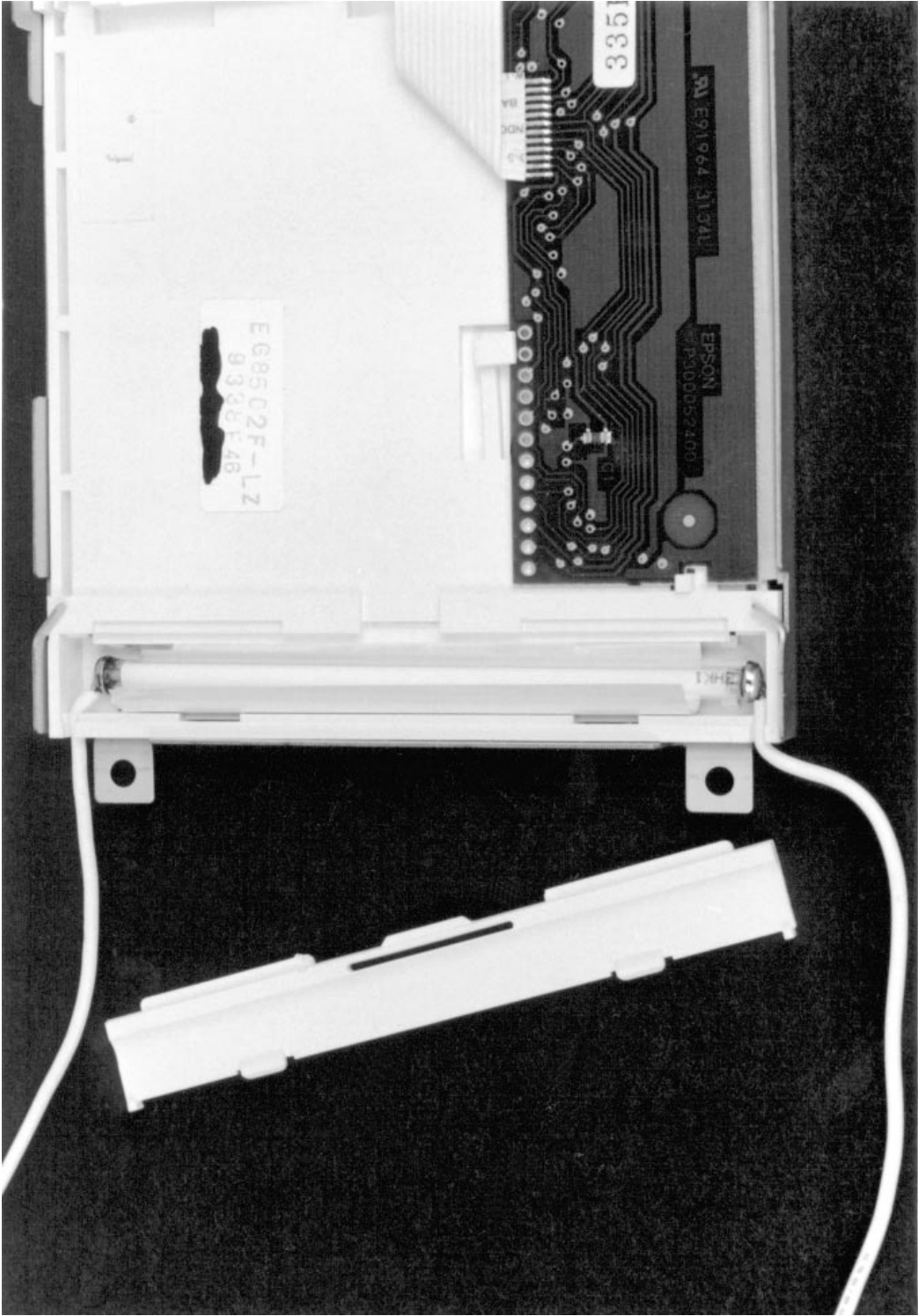
AN65-F16

Figure 16. A Custom Designed, Extremely Low Loss Display. All Metal Is Eliminated in Lamp Area (Lower Portion of Photo). A Good Compromise Between Mechanical Strength and Loss Control



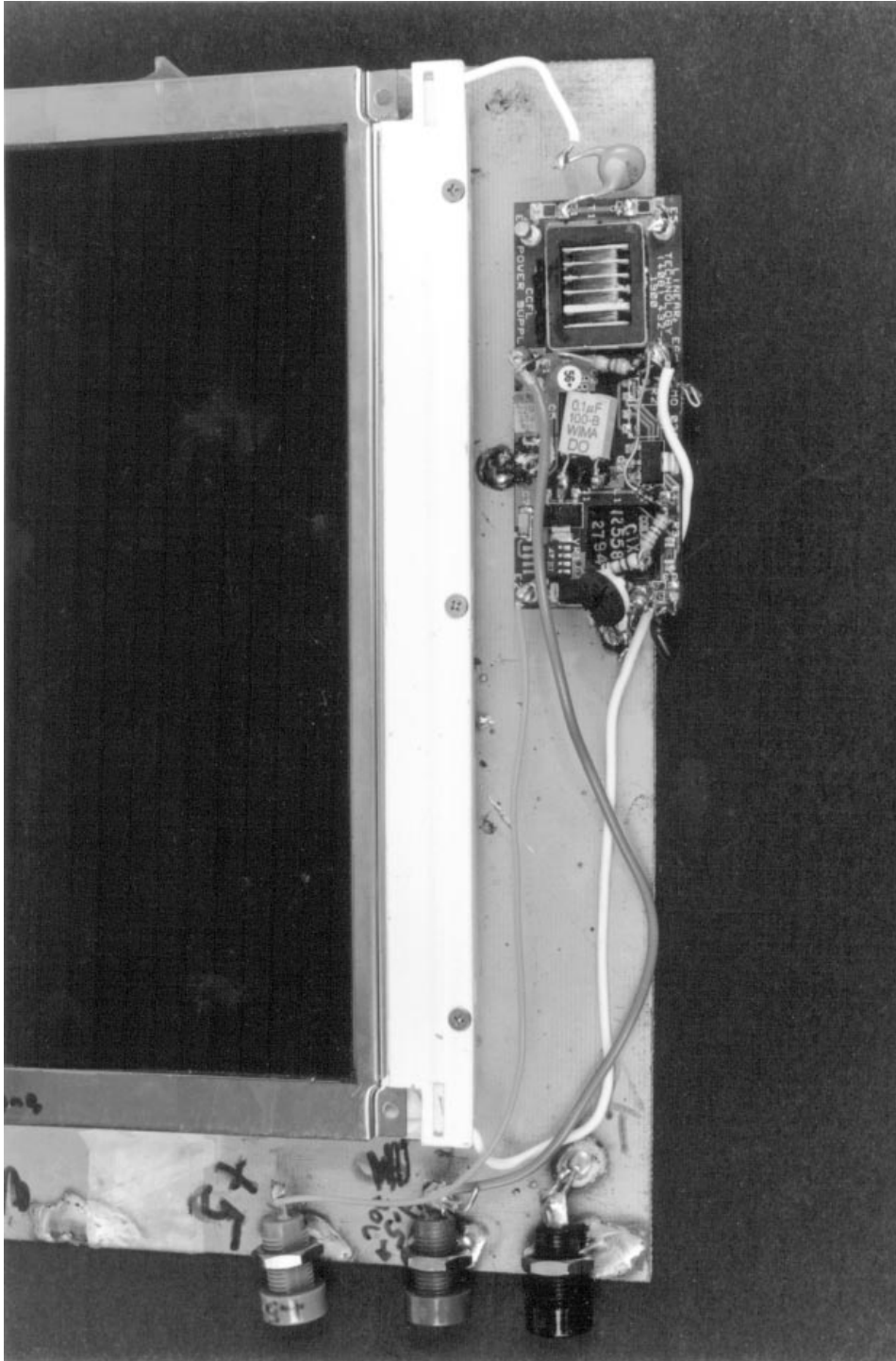
AN65FT7

Figure 17. Figure 16's Reverse Side. All Metal Is Relieved in Lamp Area, Maintaining Low Losses. An Excellent, Practical Display



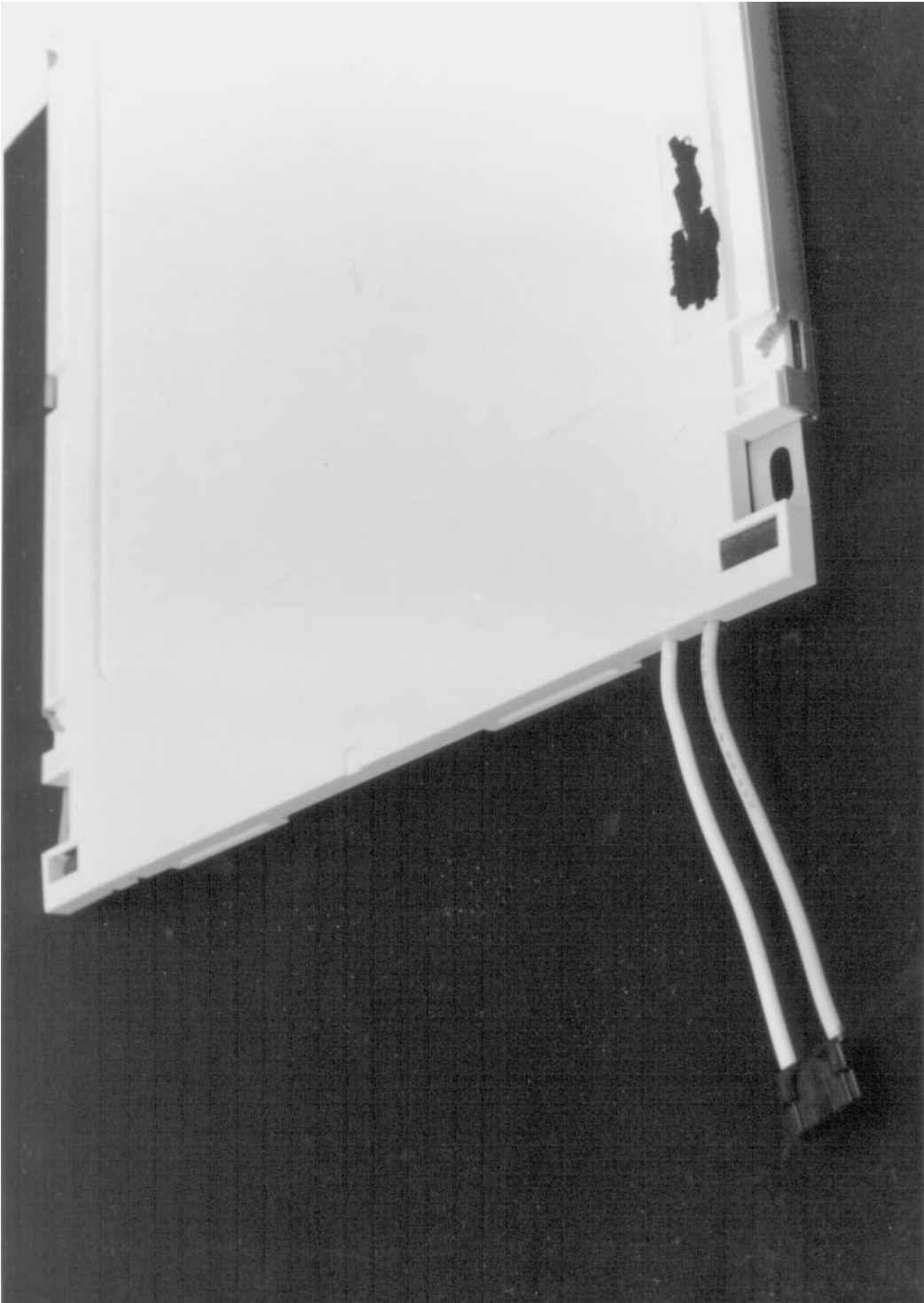
AN65-F18

Figure 18. Plastic “Cocon” Cuts Losses. Metallic Foil Is Absorptive but Floats from Grounded Display Frame. A Good Compromise with about 4% Loss



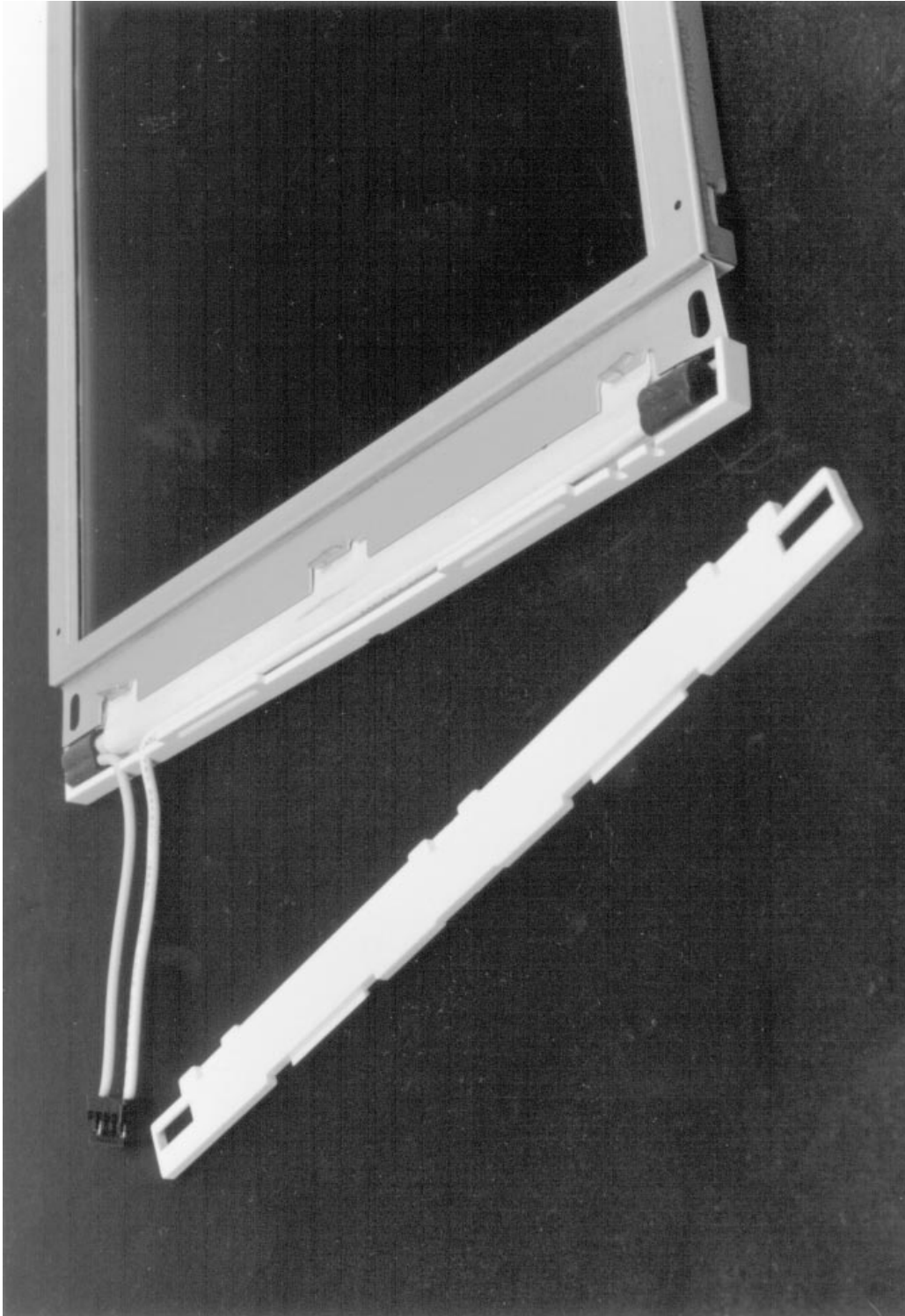
AN65-F19

Figure 19. Plastic "Outtrigger" Isolates Lamp from Metal Display Frame Loss Path



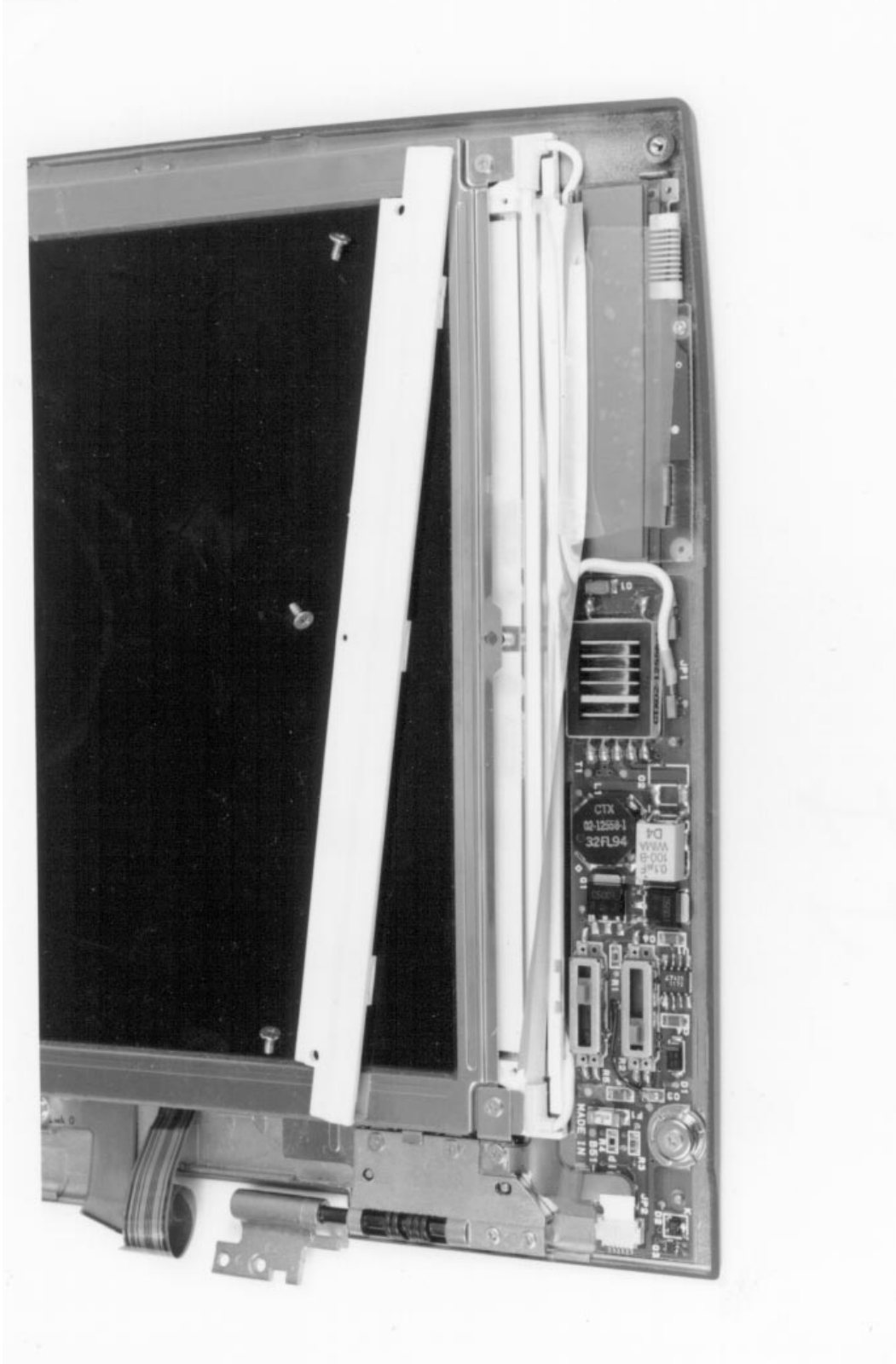
AN65F20

Figure 20. Plastic Isolates Lamp from Metal Frame in This Display's Rear View



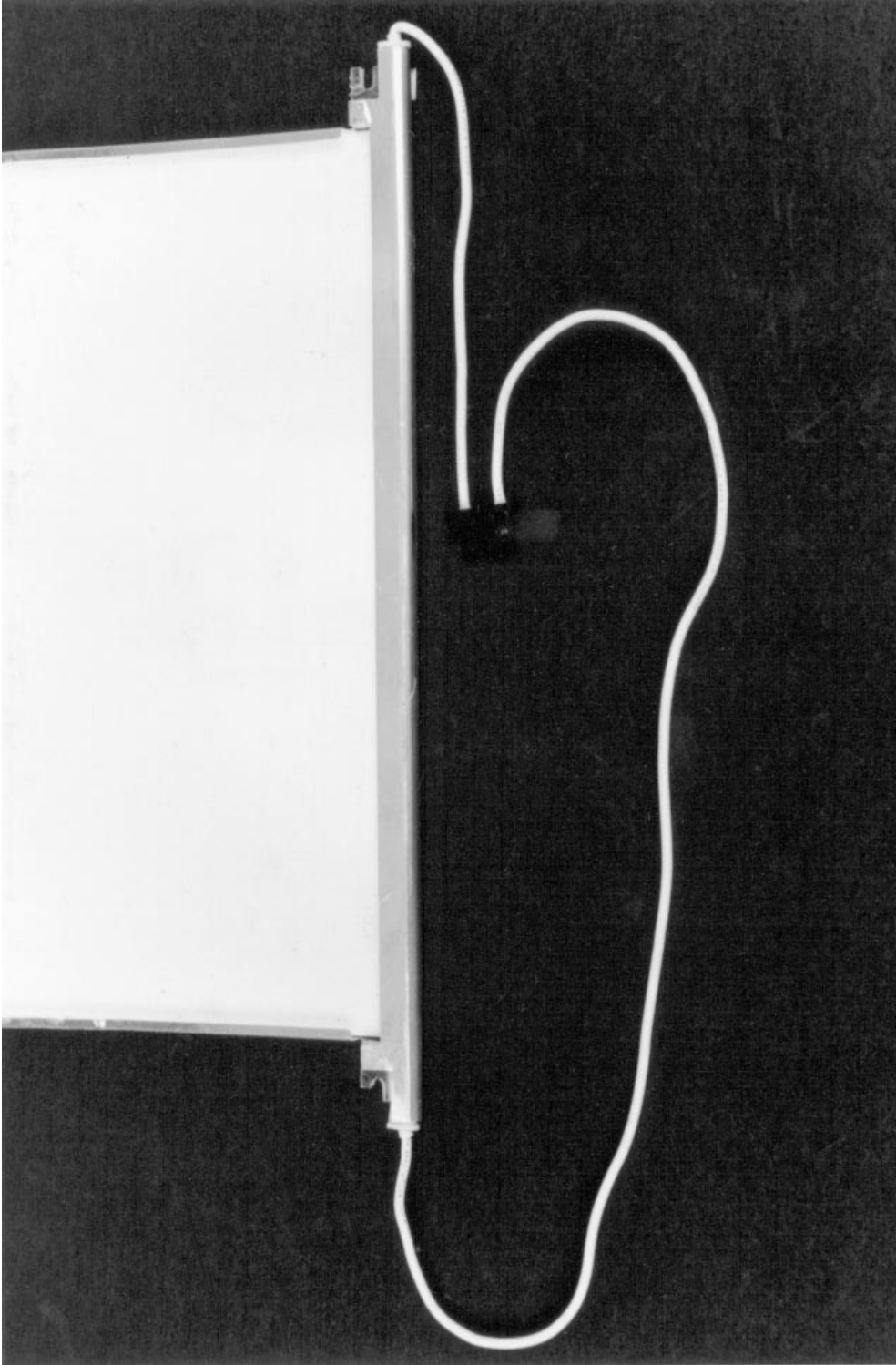
AN65-19

Figure 21. Figure 20's Display Front View Continues Plastic Isolation Treatment but Reflective Foil (over Lamp) Contacts Metal Frame. Massive Losses via This Path Cause Overall 12% Loss. Trimming Foil from Metal Cuts Loss to 4%



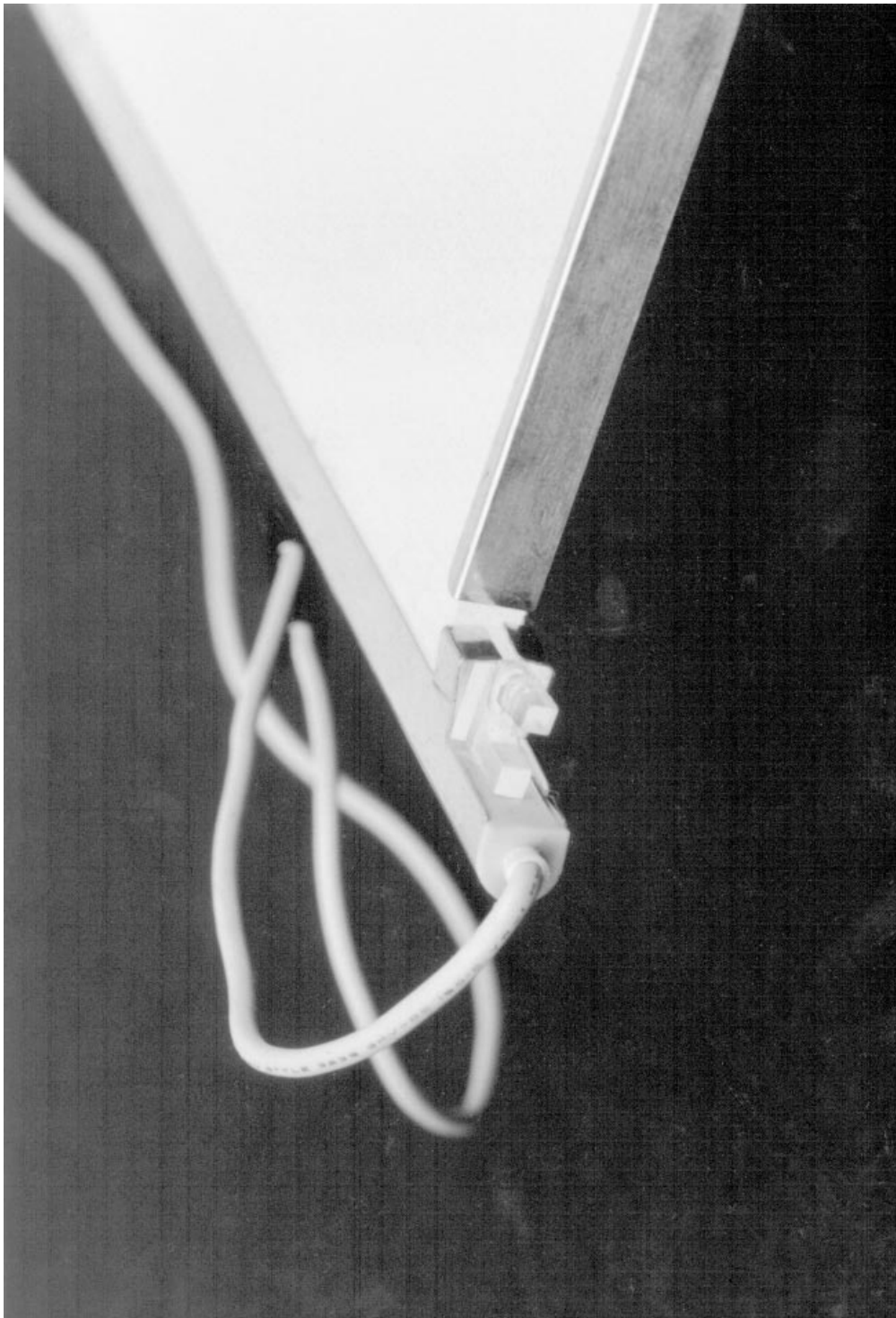
AN65#22

Figure 22. Another “Outrigged” Plastic Enclosure Suffers Foil Contacting Display’s Frame Metal. Relieving Foil from Metal Cuts Losses from 13% to 6%. Poor Wire Routing (Lower Right) Causes 3% Loss



AN65-F23

Figure 23. Isolation Slits (Center Right and Left) in Metal Reflector Prevent Losses to Grounded Metal Frame (Upper Right and Left). Overall Losses About 6%



AN65-F24

Figure 24. Close-Up of Figure 23's Isolation Slit Construction. Secondary Benefit Is Control of Reflector-to-Lamp Distance, Minimizing Capacitance

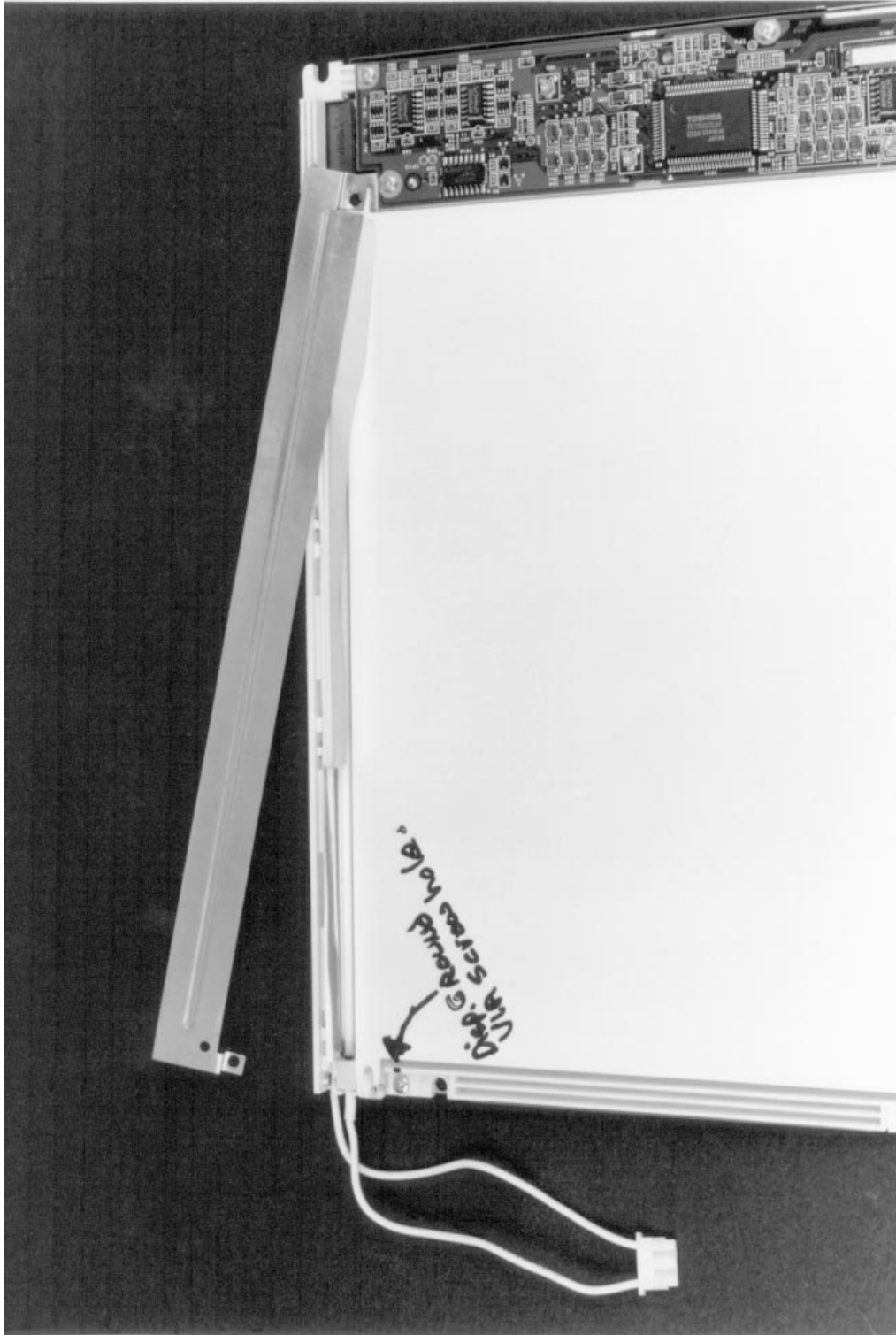
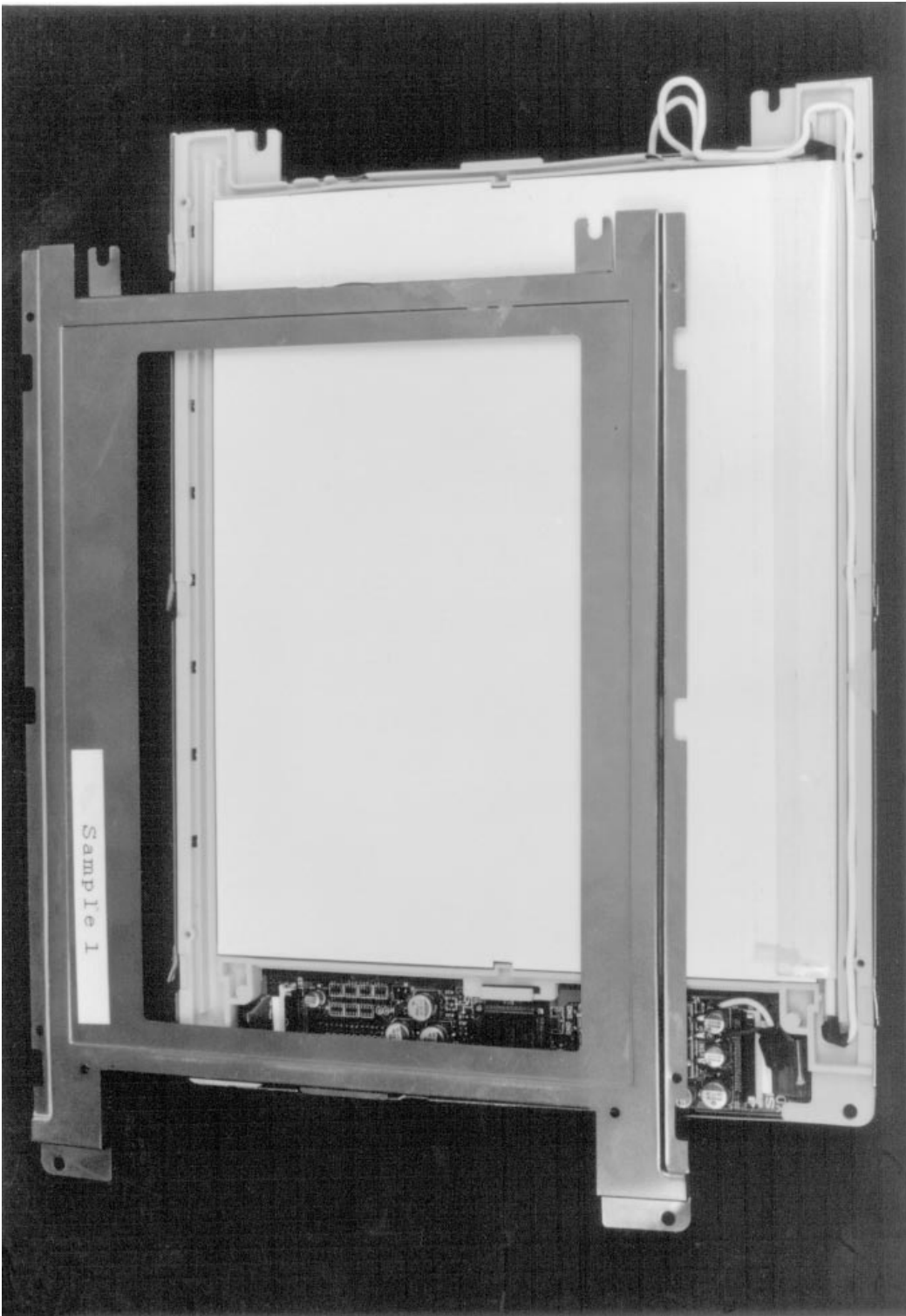
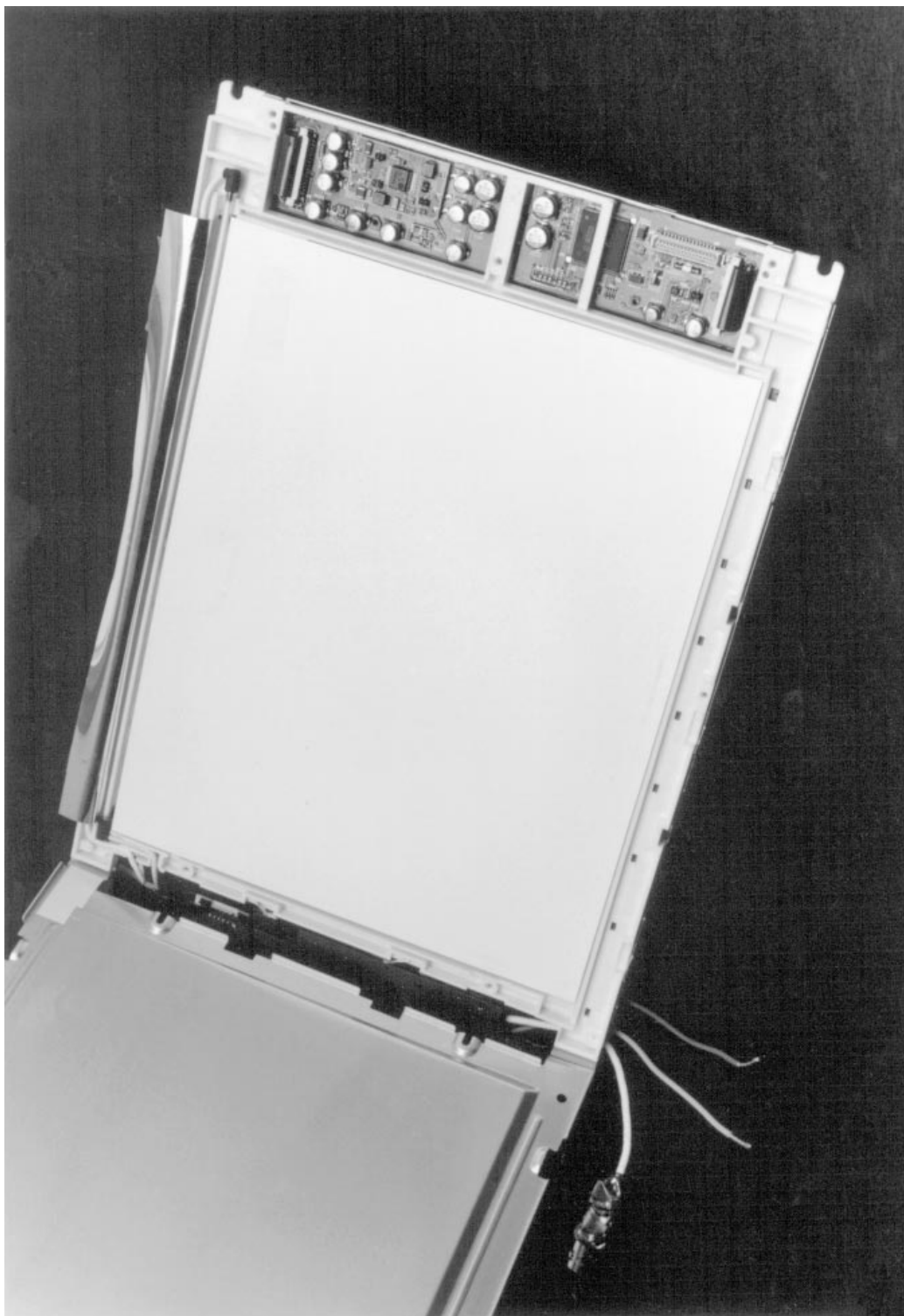


Figure 25. Metal Cover over Lamp Causes 15% Loss. Replacing Cover Securing Screws with Nylon Types Floats Cover from Ground, Dropping Loss to 8%. Replacing Cover with Plastic Improves Loss to Only 3% . . . a 5X Improvement!



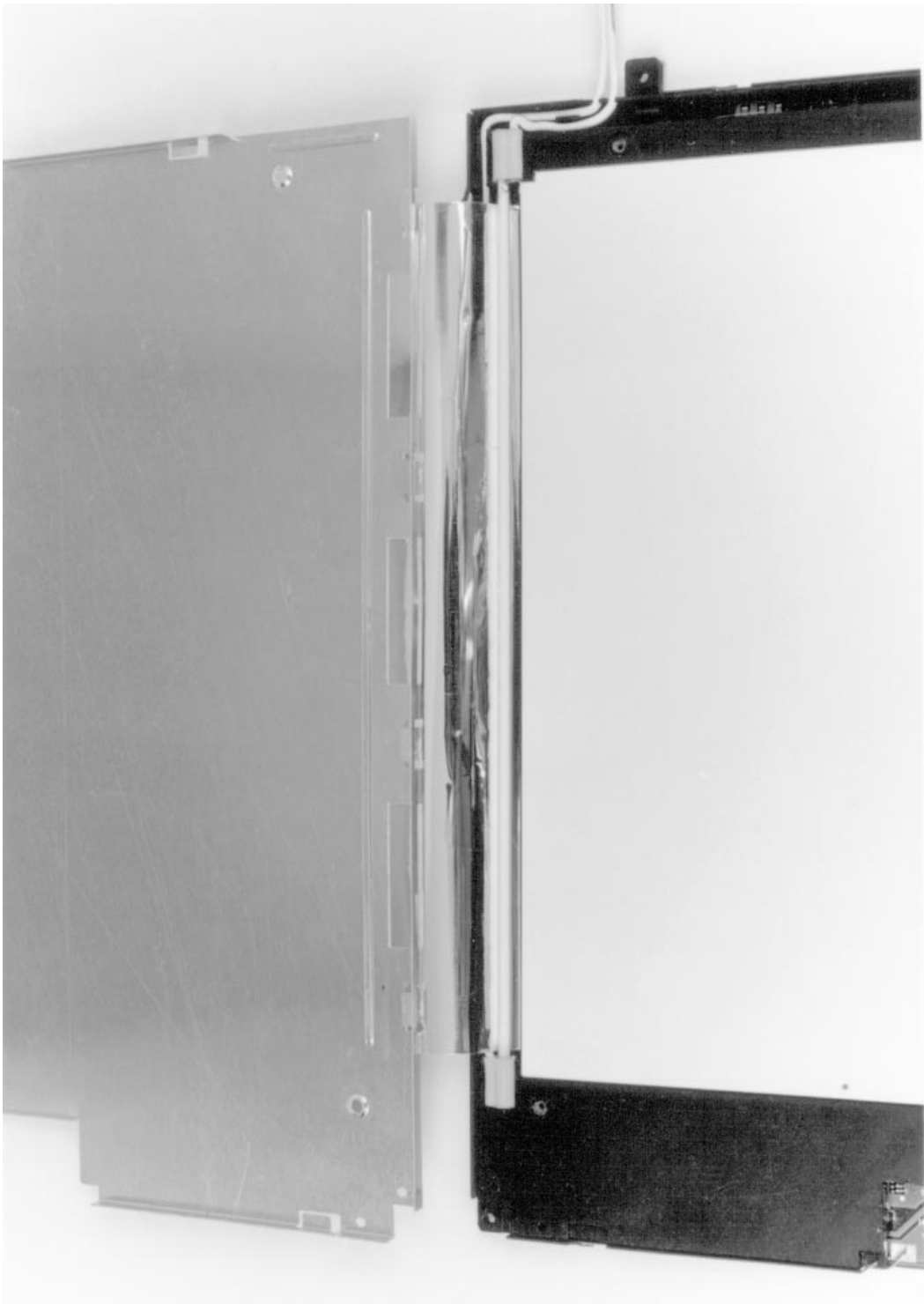
AN65F26

Figure 26. Huge Metal Area over Lamp Causes 14% Loss. Replacing Metal in Lamp Area with Plastic Cuts Loss to 6%



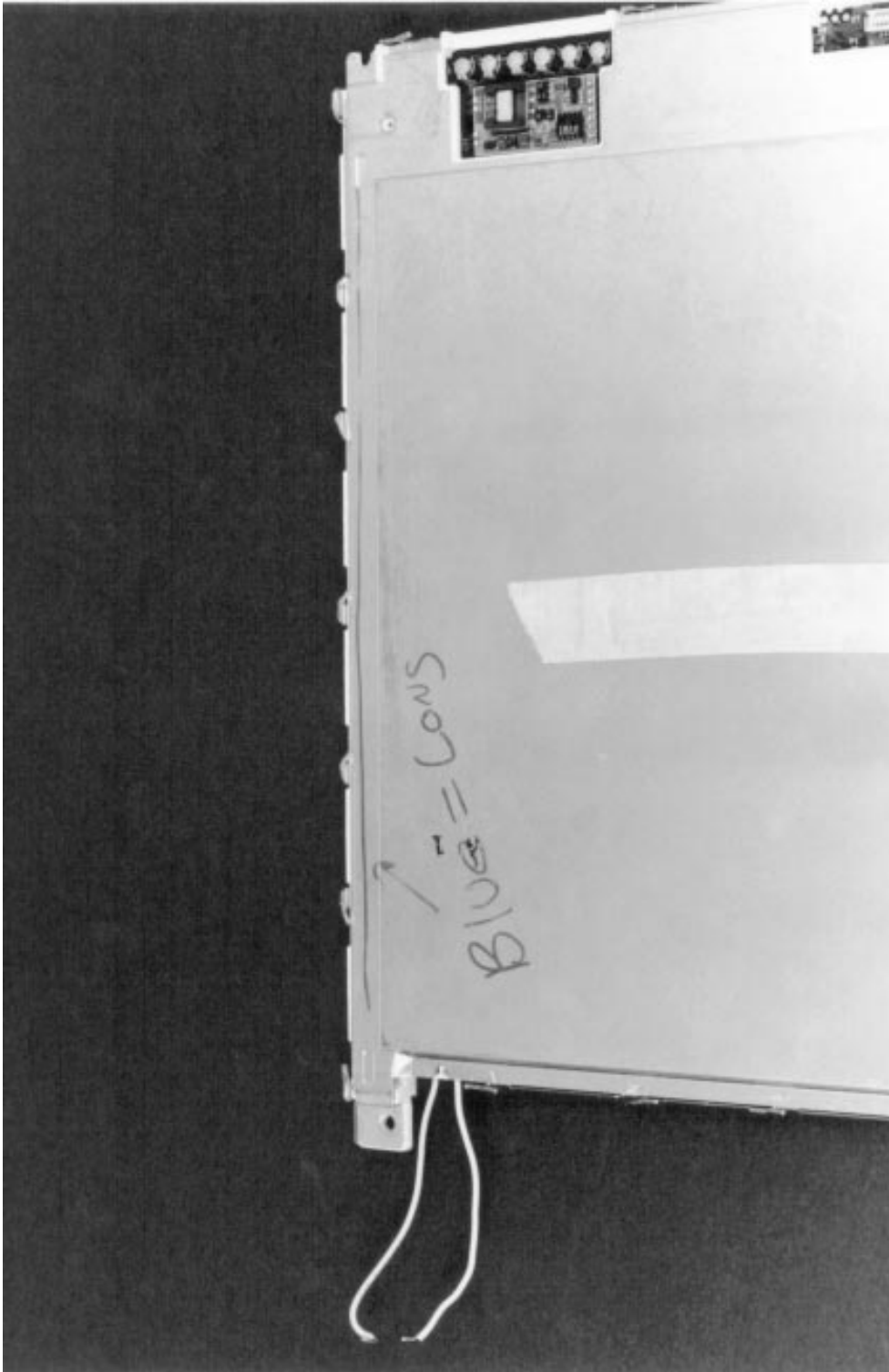
AN65-27

Figure 27. Metallic Foil over Lamp (Upper Center) Dumps Absorbed Energy to Metal Rear Cover. 16% Loss Results



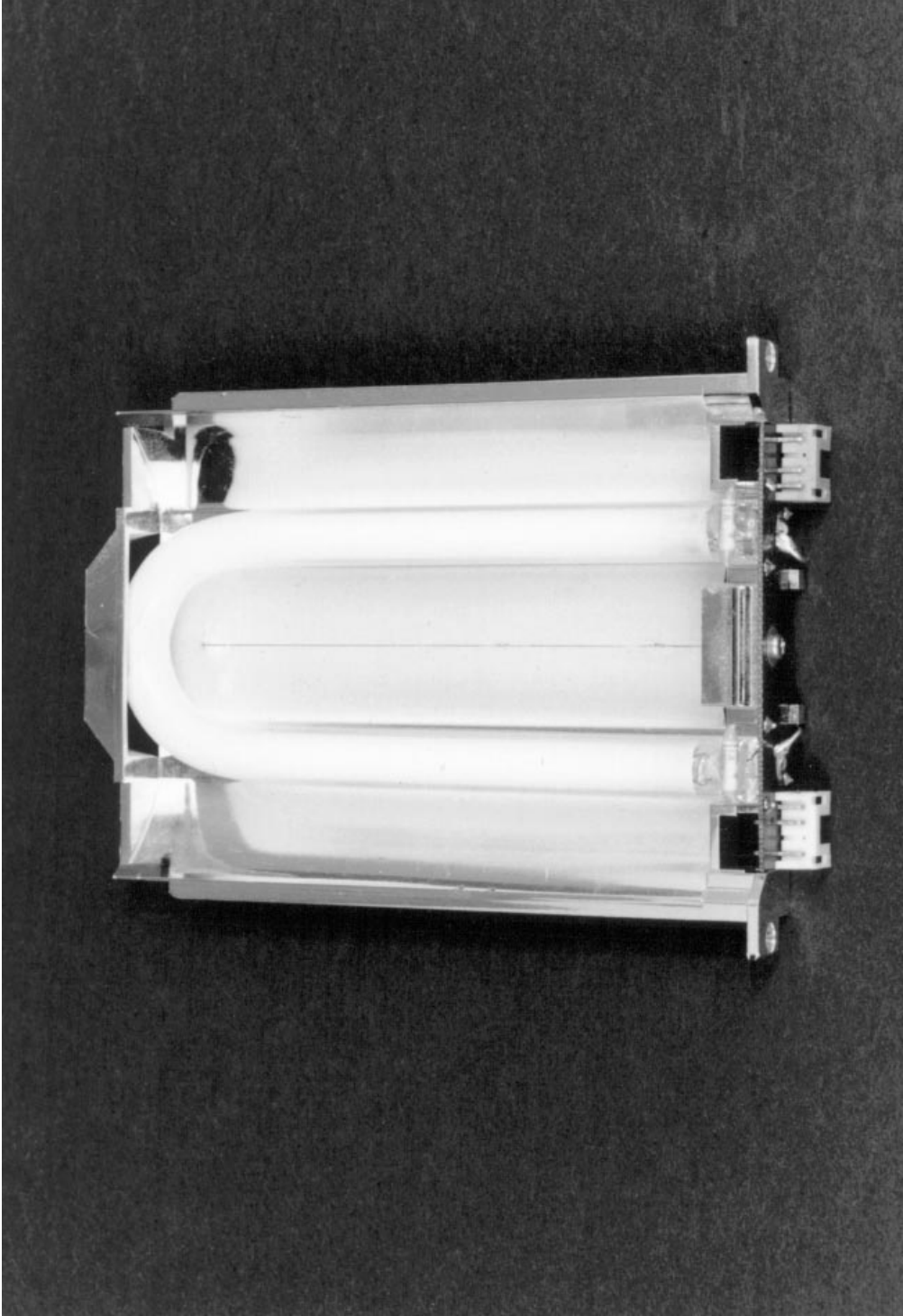
AN65-26

Figure 28. Low Losses of the Display's Nonconductive Frame (Black Plastic) Are Thrown Away by Lossy Reflective Foil Contacting Massive Metal Rear Cover. 15% Loss Results



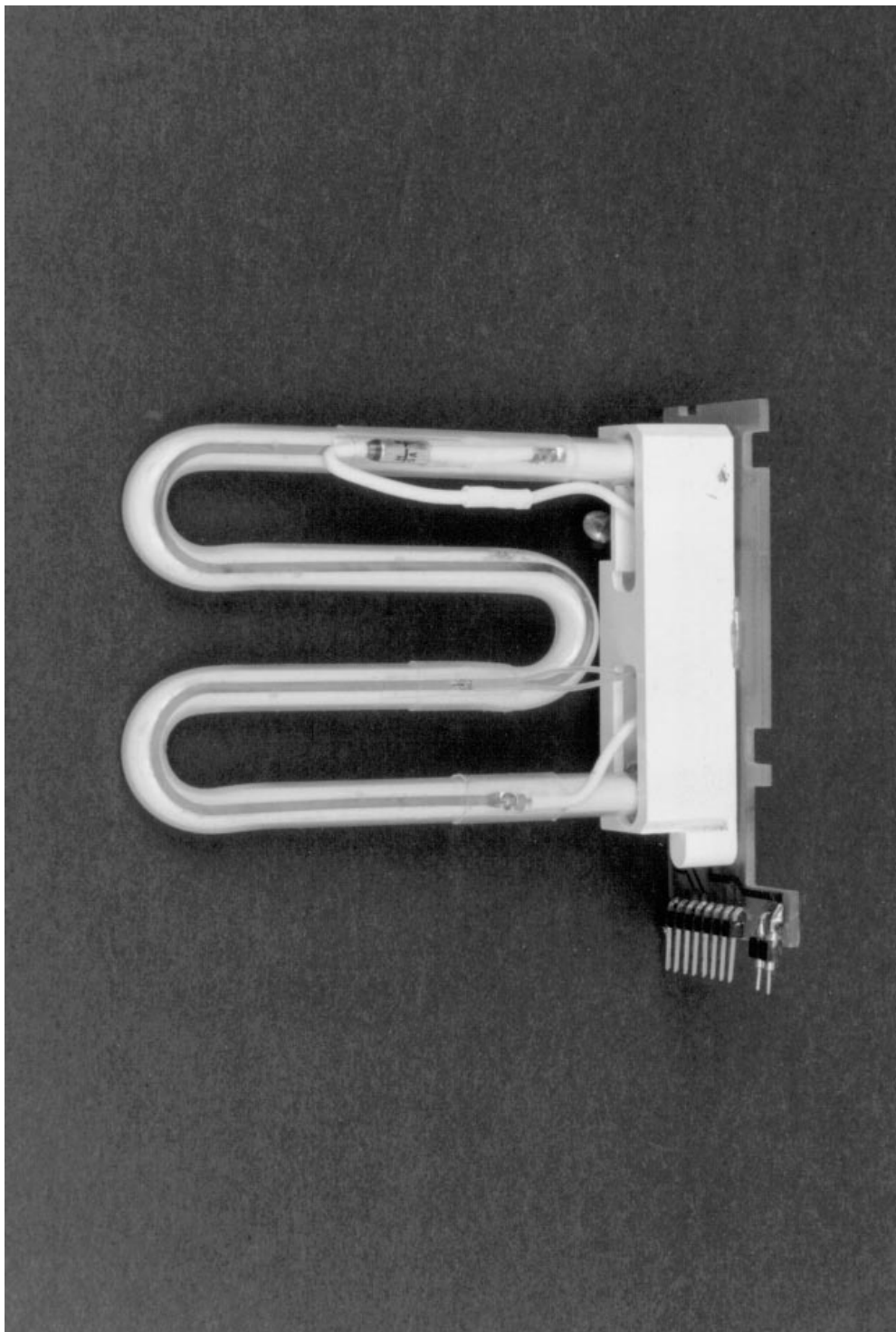
AN65-29

Figure 29. A Similar Situation to Figure 28. Large Metal Rear Cover Contacts Lossy Foil (Not Visible), Causing Huge Losses



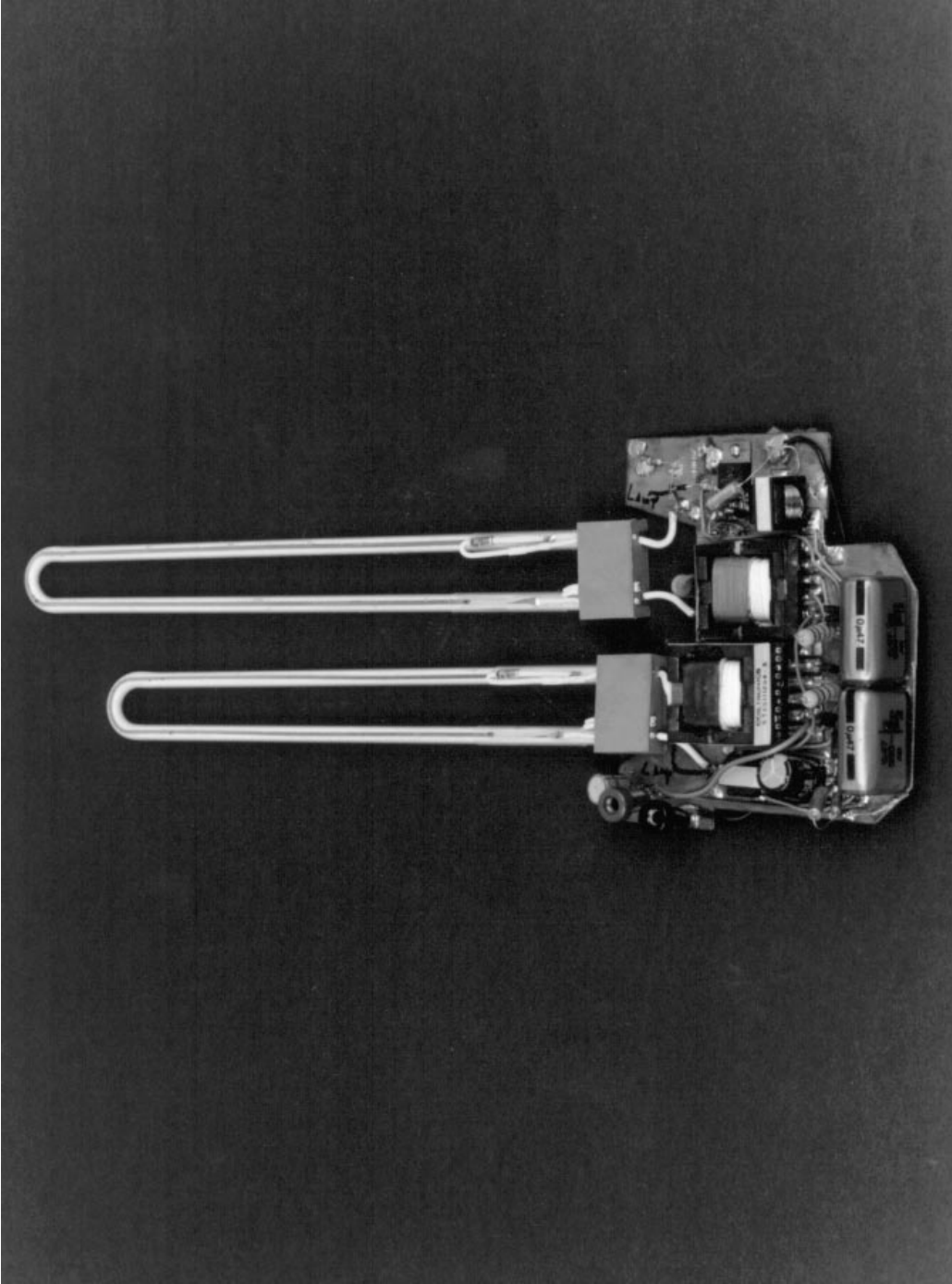
AN65-28

Figure 30. Grounded Metallic Optical Reflector in Automotive Lamp Introduces 18% Loss. Optical Gain over Nonmetallic Reflector May Justify Large Electrical Loss



AN65-31

Figure 31. Metallic Heater on Lamp in this Automotive Application Eases Low Temperature Starting but Causes 31% Loss



AN65-32

Figure 32. Similar to Figure 31. Metallic Cold Start Heaters in Automotive Application Induce 23% Loss

Considerations for Multilamp Designs

Multiple-lamp designs are not recommended if lamp intensity matching is important. Maintaining emission matching over time, temperature and production variations is quite difficult. In some restricted cases multilamp displays may be a viable option, but a single lamp with good diffuser optics is almost always the better approach. Information on dual-lamp displays is presented here for reference purposes only.⁵

Systems using two lamps have some unique layout problems. Almost all dual-lamp displays are color units. The lower light transmission characteristics of color displays necessitates more light. As such, display manufacturers sometimes use two lamps to produce more light. The wiring layout of these dual-lamp color displays affects efficiency and illumination balance in the lamps. Figure 33 shows an “x-ray” view of a typical display. This symmetrical arrangement presents equal parasitic losses. If C1 and C2 and the lamps are well-matched, the circuit’s current output splits evenly and equal illumination occurs.

Figure 34’s display arrangement is less friendly. The asymmetrical wiring forces unequal losses and the lamps receive imbalanced current. Even with identical lamps, illumination may not be balanced. This condition is partially correctable by skewing values of C1 and C2. C1, because it drives greater parasitic capacitance, should be larger than C2. This tends to equalize the currents, promoting equal lamp drive. It is important to realize that this compensation does nothing to recapture the lost energy—efficiency is still compromised. There is no substitute for minimizing loss paths. Similarly, any change in lamp characteristics (e.g., aging) can cause imbalanced illumination to recur.

In general, imbalanced illumination causes fewer problems than might be supposed at high intensity levels. Unequal illumination is much more noticeable at lower levels. In the worst case the dimmer lamp may only partially illuminate. This phenomenon, sometimes called “Thermomentering,” is discussed in detail in the text section, “Floating Drive Circuits.”

Note 5. The text’s tone is intended to convey our distaste for multilamp displays. They are the very soul of heartache.

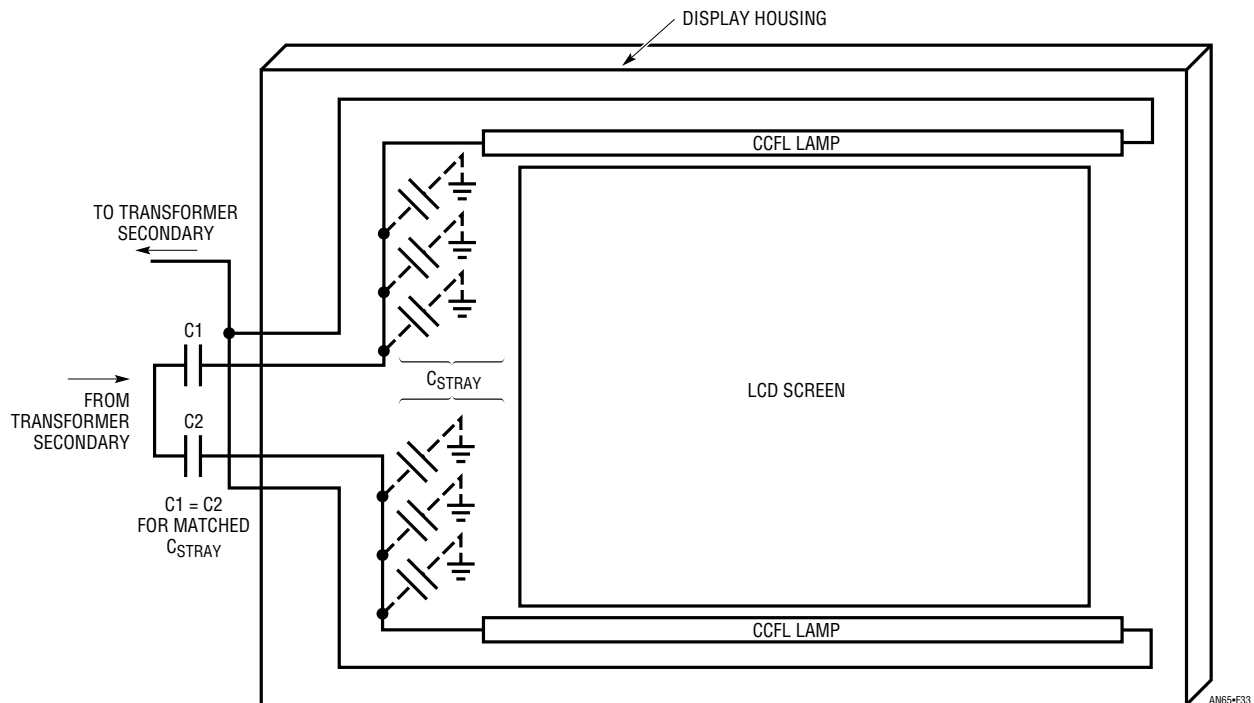


Figure 33. Loss Paths for “Best Case” Dual-Lamp Display. Symmetry Promotes Balanced Illumination, but Lamp Limitations Dominate Achievable Results

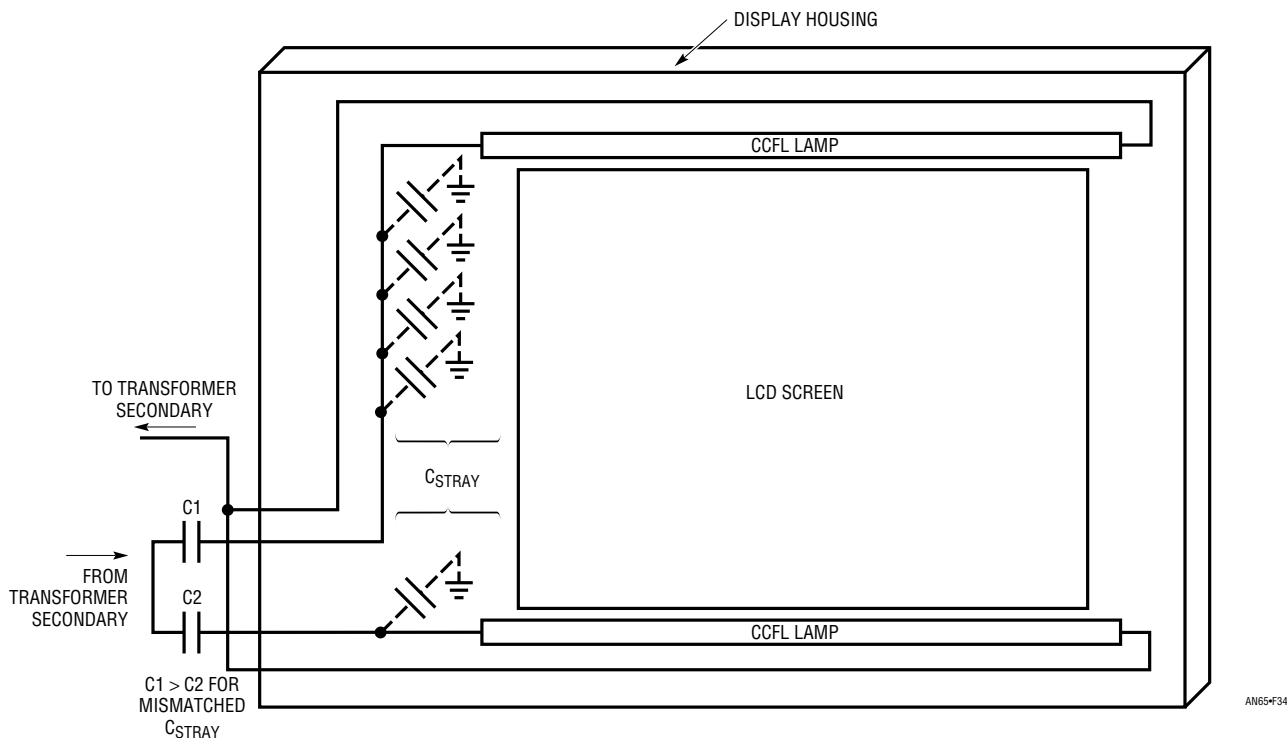


Figure 34. Asymmetric Losses in a Dual-Lamp Display. Skewing C1 and C2 Values Compensates Imbalanced Loss Paths but Not Wasted Energy

CCFL Power Supply Circuits

Choosing an approach for a general purpose CCFL power supply is difficult. A variety of disparate considerations make determining the “best” approach a thoughtful exercise. Above all, the architecture must be extraordinarily *flexible*. The sheer number and diversity of applications demands this. The considerations take many degrees of freedom. Power supply voltages range from 2V to 30V with output power from minuscule to 50W. The load is highly nonlinear and varies over operating conditions. The backlight is often located some distance from the primary power source, meaning the supply must tolerate substantial supply bus impedances. Similarly, it must not corrupt the supply bus with noise, or introduce appreciable RFI into the system or environment. Component count should be low and the supply must be physically quite small as space is usually extremely limited. Additionally, the circuit must be relatively layout-insensitive because of varying board shape requirements. Interface for shutdown and dimming control should accommodate either digital or

analog inputs, including voltage, current, resistive, PWM or serial bit-stream addressing. Finally, lamp current should be predictable and stable with changes in time, temperature and supply voltage.

A current-fed, feedback-controlled resonant Royer converter meets these requirements.⁶ This approach, because of its extreme flexibility, is a favorable compromise. It operates over wide supply ranges and scales well over a broad output power range. Current is taken from the supply bus almost continuously, making the circuit tolerate supply bus impedance. This characteristic also means that circuit operation does not corrupt power supply lines. There is no RFI problem and component count is low. It is small, relatively insensitive to layout and easy to interface to. Lastly, lamp current is stable and predictable over operating conditions.

Note 6. See Appendices K and L for detailed discussion on architecture selection and the Royer configuration.

Figure 35 is a practical CCFL power supply circuit based on the above discussion. Efficiency is 88% with an input voltage range of 6.5V to 20V. This efficiency figure can be degraded by about 3% if the LT[®]1172 V_{IN} pin is powered from the same supply as the main circuit V_{IN} terminal. Lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied the LT1172 switching regulator's Feedback pin is below the device's internal 1.2V reference, causing full duty cycle modulation at the V_{SW} pin (Trace A, Figure 36). V_{SW} conducts current (Trace B) which flows from L1's center tap,

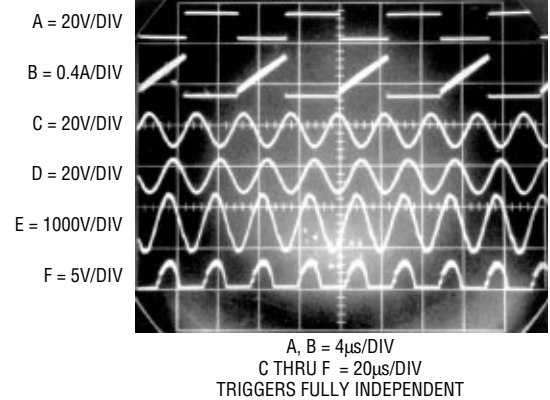
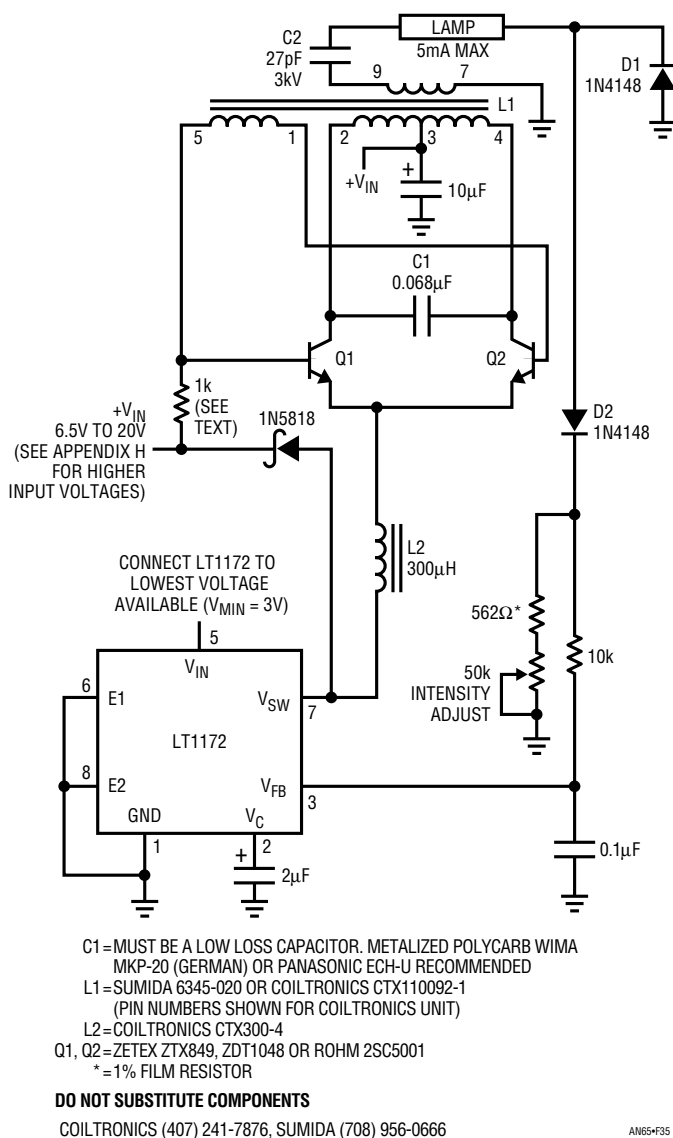


Figure 36. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B, and C through F

through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

L1 and the transistors comprise a current driven Royer class converter⁷ which oscillates at a frequency primarily set by L1's characteristics (including its load) and the 0.068µF capacitor. LT1172 driven L2 sets the magnitude of the Q1/Q2 tail current, hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1172 is off. The LT1172's 100kHz clock rate is asynchronous with respect to the push/pull converter's (60kHz) rate, accounting for Trace B's waveform thickening.

The 0.068µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (Traces C and D respectively). L1 furnishes voltage step-up and about 1400V_{P-P} appears at its secondary (Trace E). Current flows through the 27pF capacitor into the lamp. On negative waveform cycles, the lamp's current is steered to ground via D1. Positive waveform cycles are directed via D2 to the ground referred 562Ω/50k potentiometer chain. The positive half-sine appearing across the resistors (Trace F) represents 1/2 the lamp current. This signal is filtered by the 10k/0.1µF pair and presented to the LT1172's Feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1172's V_C pin provides stable loop compensation. The loop forces the LT1172 to switch

Note 7. See Appendix K, "Who Was Royer and What Did He Design?" See also Reference 2.

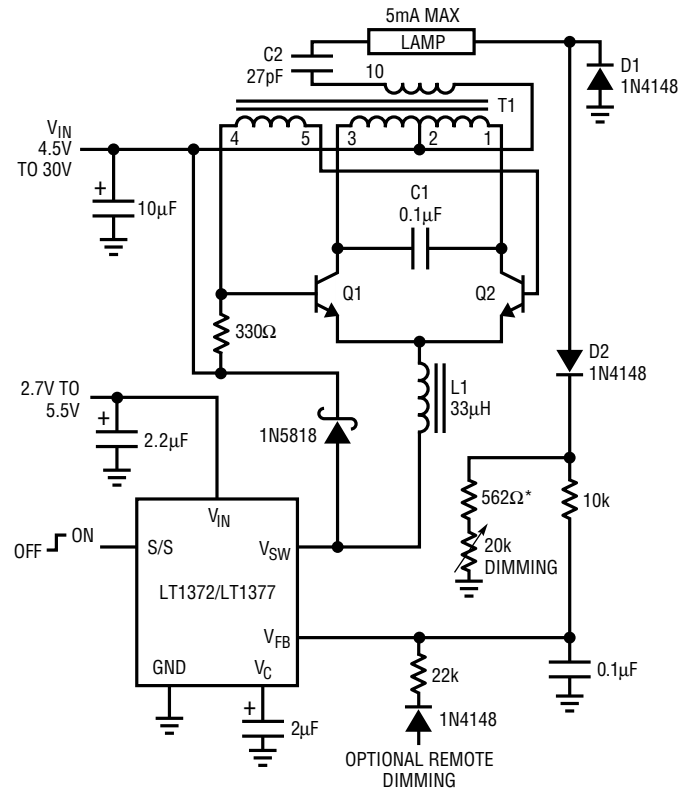
Application Note 65

mode modulate L2's average current to whatever value is required to maintain constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0% to 100% intensity control with no lamp dead zones or "pop-on" at low intensities.⁸ Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

The circuit's 0.1% line regulation is notably better than some other approaches. This tight regulation prevents lamp intensity variation when abrupt line changes occur. This typically happens when battery-powered apparatus is connected to an AC-powered charger. The circuit's excellent line regulation derives from the fact that L1's drive waveform never changes shape as input voltage varies. This characteristic permits the simple 10kΩ/0.1μF RC to produce a consistent response. The RC averaging characteristic has serious error compared to a true RMS conversion, but the error is constant and "disappears" in the 562Ω shunt's value.

This circuit is similar to one previously described⁹ but its 88% efficiency is 6% higher. The efficiency improvement is primarily due to the transistor's higher gain and lower saturation voltage. The base drive resistor's value (nominally 1k) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. A procedure for doing this is described in a following section, "General Optimization and Measurement Considerations."

Figure 37's circuit is similar, but uses a transformer with lower copper and core losses to increase efficiency to 91%. The trade-off is slightly larger transformer size. Additionally, a higher frequency switching regulator offers slightly lower V_{IN} current, aiding efficiency. L1's smaller value, a result of the higher frequency operation, permits slightly reduced copper loss. The transformer options listed allow efficiency optimization over the supply range of interest. Value shifts in C1, L2 and the base drive resistor reflect different transformer characteristics. This circuit also features shutdown and a DC or pulse width controlled dimming input. Appendix F, "Intensity Control and Shutdown Methods," details operation of these features. Figure 38, directly derived from Figure 37, produces 10mA output to drive color LCDs at 92% efficiency. The



- C1 = WIMA MKP-20, PANASONIC ECH-U
 - L1 = COILCRAFT DT3316-333
 - Q1, Q2 = ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
 - T1 = COILTRONICS CTX 02-12614-1 OR CTX110600-1 (SEE TEXT)
 - * = 1% FILM RESISTOR
- DO NOT SUBSTITUTE COMPONENTS**
 COILTRONICS (407) 241-7876
 COILCRAFT (708) 639-6400

AN65#37

Figure 37. A 91% Efficient CCFL Supply for 5mA Loads Features Shutdown and Dimming Inputs. Higher Frequency Switching Regulator Reduces L1's Size While Requiring Less V_{IN} Current

slight efficiency improvement comes from a reduction in regulator "housekeeping" current as a percentage of total current drain. Value changes in components are the result of higher power operation. The most significant change involves driving two lamps. Accommodating two lamps involves separate ballast capacitors but circuit operation is similar. Dual-lamp designs reflect slightly different loading back through the transformer's primary. C2 usu-

Note 8. Controlling a nonlinear load's current, instead of its voltage, permits applying this circuit technique to a wide variety of nominally evil loads. See Appendix I, "Additional Circuits."

Note 9. See "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, Application Note 49, August 1992 and "Techniques for 92% Efficient LCD Illumination," Linear Technology Corporation, Application Note 55, August 1993.

ally ends up in the 10pF to 47pF range. Note that C2A and B appear with their lamp loads in parallel across the transformer's secondary. As such, C2's value is often smaller than in a single-lamp circuit using the same type lamp. Ideally, the transformer's secondary current splits evenly between the C2-lamp branches, with the total load current being regulated. In practice, differences between C2A and B, and differences in lamps and lamp wiring layout preclude a perfect current split. Practically, these differences are small and the lamps appear to emit an equal amount of light at high intensity. Layout and lamp matching can influence C2's value. Some techniques for dealing with these issues appear in the text section, "Considerations for Multilamp Designs." As previously stated, dual-lamp designs are distinctly not recommended, particularly if balanced illumination over wide dimming ranges is required.

Figure 39 uses a dedicated CCFL IC, the LT1183, to enhance circuit performance. The Royer-based high voltage converter portion is recognizable from previous circuits, with the 200kHz LT1183 performing the switching regulator/feedback function. This IC also features open lamp protection circuitry, simplified frequency compensation, a separate regulator providing LCD contrast and other features.¹⁰ The contrast supply is driven by the LT1183 with L3 and associated discrete components completing the function. The CCFL and contrast outputs may be adjusted with DC, PWM or potentiometers.

Note 10. Open lamp protection is often desirable and may be added to the previous circuits at the cost of some discrete components. See Appendix E, "Open Lamp/Overload Protection." Frequency compensation issues are covered in the text section "Feedback Loop Stability Issues." See Appendix J for discussion of LCD contrast supplies.

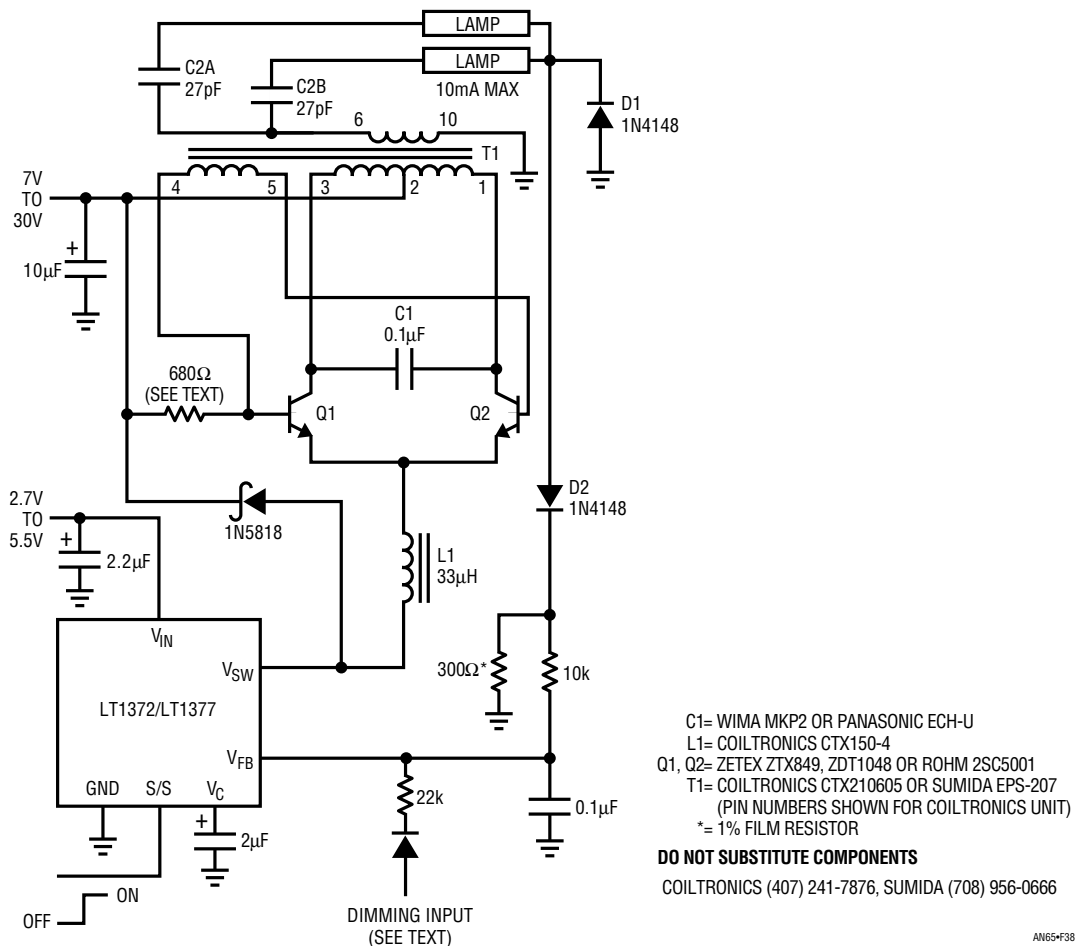


Figure 38. A 92% Efficient CCFL Supply for 10mA Loads Features Shutdown and Dimming Inputs. Dual-Lamp Designs, Typical of Early Color Displays, Are Not Recommended

Application Note 65

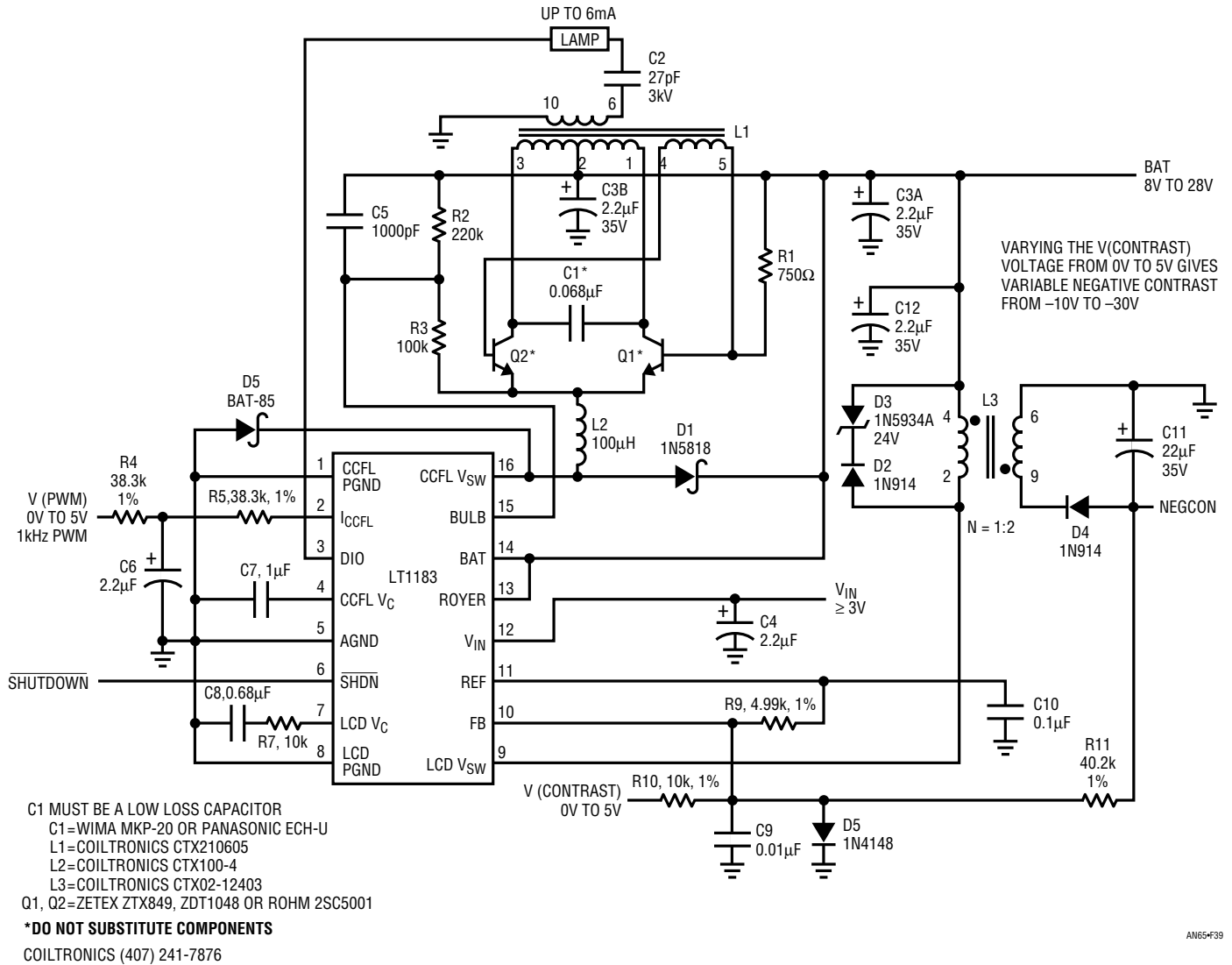


Figure 39. Dedicated Backlight IC Includes Switching Regulator, Open Lamp Protection and LCD Contrast Supply. 200kHz Operation Minimizes L2 Size. Shutdown and Control Inputs Are Simplified

Low Power CCFL Power Supplies

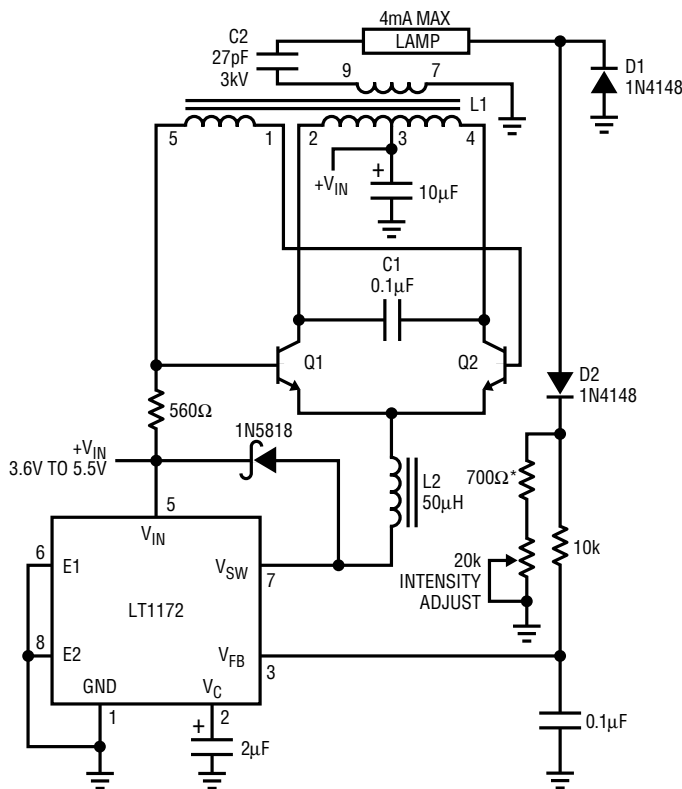
Many applications require relatively low power CCFL backlighting. Figure 40's variation, optimized for low voltage inputs, produces 4mA output. Circuit operation is similar to the previous examples. The fundamental difference is L1's higher turns ratio, which accommodates the reduced available drive voltage. The circuit values given are typical, although some variation occurs with various lamps and layouts.

Figure 41's design, the so-called "dim backlight," is optimized for very low current lamp operation. The circuit is meant for use at low input voltages, typically 2V to 6V with a 1mA maximum lamp current. This circuit maintains control down to lamp currents of 1µA, a very dim light! It is intended for applications where the longest possible

battery life is desired. Primary supply drain ranges from hundreds of microamperes to 100mA with lamp currents of microamps to 1mA. In shutdown the circuit pulls only 100µA. Maintaining high efficiency at low lamp currents requires modifying the basic design.

Achieving high efficiency at low operating current requires lowering quiescent power drain. To do this the previously employed pulse width modulator-based devices are replaced with an LT1173. The LT1173 is a Burst Mode™ operation regulator. When this device's Feedback pin is too low it delivers a burst of output current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground referred diode at the V_{SW} pin prevents substrate turn-on due to excessive L2 ring-off.

Burst Mode is a trademark of Linear Technology Corporation.

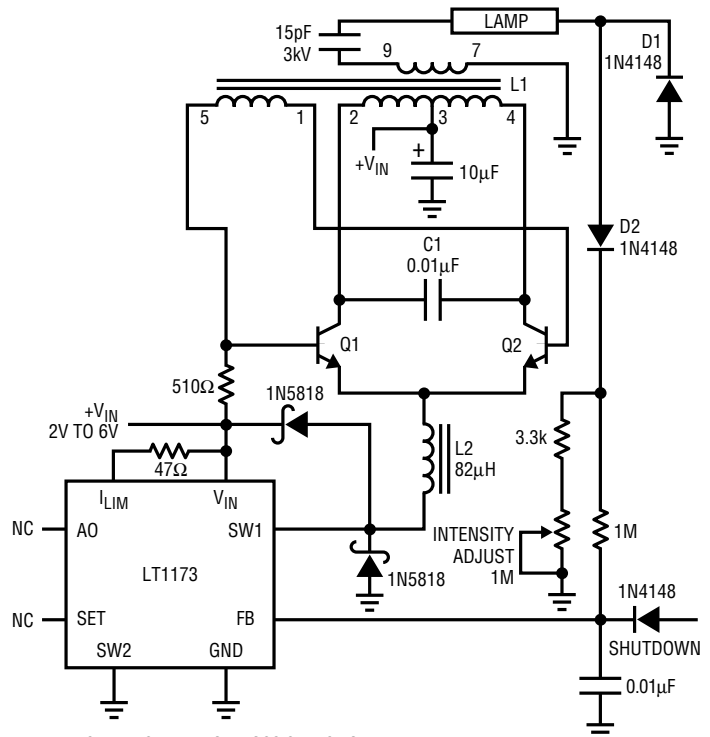


- C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA MKP-20 (GERMAN) OR PANASONIC ECH-U RECOMMENDED
- L1 = COILTRONICS CTX110654-1
- L2 = COILTRONICS CTX50-4
- Q1, Q2 = ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
- * = 1% FILM RESISTOR

DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (407) 241-7876, SUMIDA (708) 956-0666

AN65#40



- C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2, MKP-20 (GERMAN) OR PANASONIC ECH-U RECOMMENDED
- L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
- PIN NUMBERS SHOWN FOR COILTRONICS UNIT
- L2 = TOKO 262LYF-0091K (408) 432-8251
- Q1, Q2 = ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001

DO NOT SUBSTITUTE COMPONENTS

AN65#41

Figure 40. A 4mA Design Intended for Low Voltage Operation. L1's Modified Turns Ratio Allows Operation Down to 3.6V

Figure 41. Low Power CCFL Power Supply. Circuit Controls Lamp Current over a 1µA to 1mA Range

Application Note 65

During the off periods the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, the other circuit's pulse width modulator type regulators maintain "housekeeping" current between cycles. This results in more available output power but higher quiescent currents.

Figure 42 shows operating waveforms. When the regulator comes on (Trace A, Figure 42) it delivers bursts of output current to the L1/Q1/Q2 high voltage converter. The converter responds with bursts of ringing at its resonant frequency.¹¹ The circuit's loop operation is similar to the previous designs except that T1's drive waveform varies with supply. Because of this, line regulation suffers and the circuit is not recommended for wide ranging inputs.

Some lamps may display nonuniform light emission at very low excitation currents. See the text section, "Floating Lamp Circuits."

A CCFL power supply that addresses the previous circuit's line regulation problems and operates from 2V to 6V is detailed in Figure 43. This circuit, contributed by Steve Pietkiewicz of LTC, can drive a small CCFL over a 100 μ A to 2mA range.

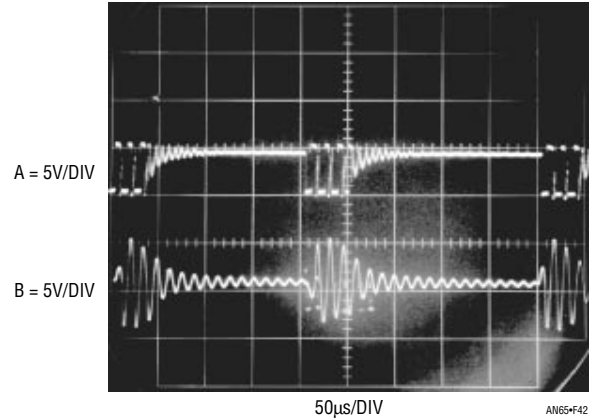


Figure 42. Waveforms for the Low Power CCFL Power Supply. LT1173 Burst Type Regulator (Trace A) Periodically Excites the Resonant High Voltage Converter (Q1 Collector Is Trace B)

Note 11. The discontinuous energy delivery to the loop causes substantial jitter in the burst repetition rate, although the high voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" mode region of most oscilloscopes, precluding a detailed display. "Alternate" mode operation causes waveform phasing errors, producing an inaccurate display. As such, waveform observation requires special techniques. Figure 42 was taken with a dual-beam instrument (Tektronix 556) with both beams slaved to one time base. Single sweep triggering eliminated jitter artifacts. Most oscilloscopes, whether analog or digital, will have trouble reproducing this display.

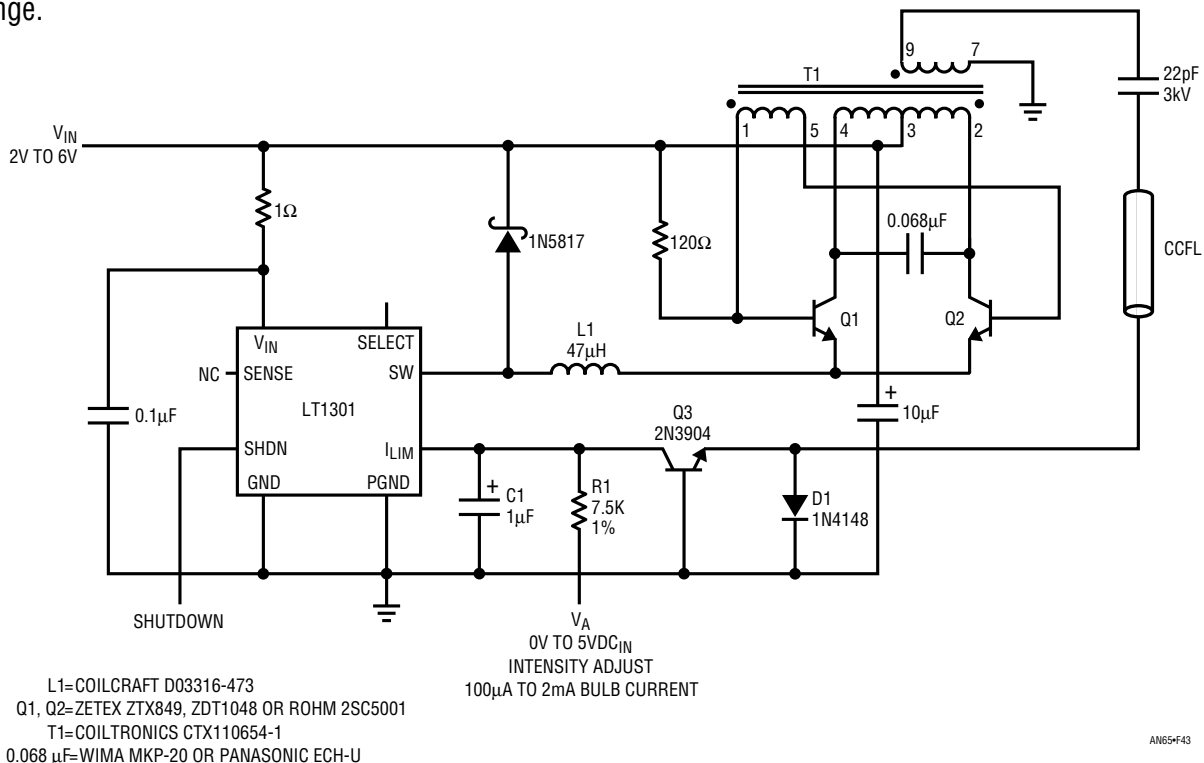


Figure 43. Low Power Cold Cathode Fluorescent Lamp Supply Is Optimized for Low Voltage Inputs and Small Lamps

The circuit uses an LT1301 micropower DC/DC converter IC in conjunction with a current driven Royer class converter comprised of T1, Q1 and Q2. When power and intensity adjust voltage are applied, the LT1301's I_{LIM} pin is driven slightly positive, causing maximum switching current through the IC's internal Switch pin (SW). Current flows from T1's center tap, through the transistors, into L1. L1's current is deposited in switched fashion to ground by the regulator's action.

Circuit efficiency ranges from 80% to 88% at full load, depending on line voltage. Current mode operation combined with the Royer's consistent waveshape vs input results in excellent line rejection. The circuit has none of the line rejection problems attributable to the hysteretic voltage control loops typically found in low voltage micropower DC/DC converters. This is an especially desirable characteristic for CCFL control, where lamp intensity must remain constant with shifts in line voltage.

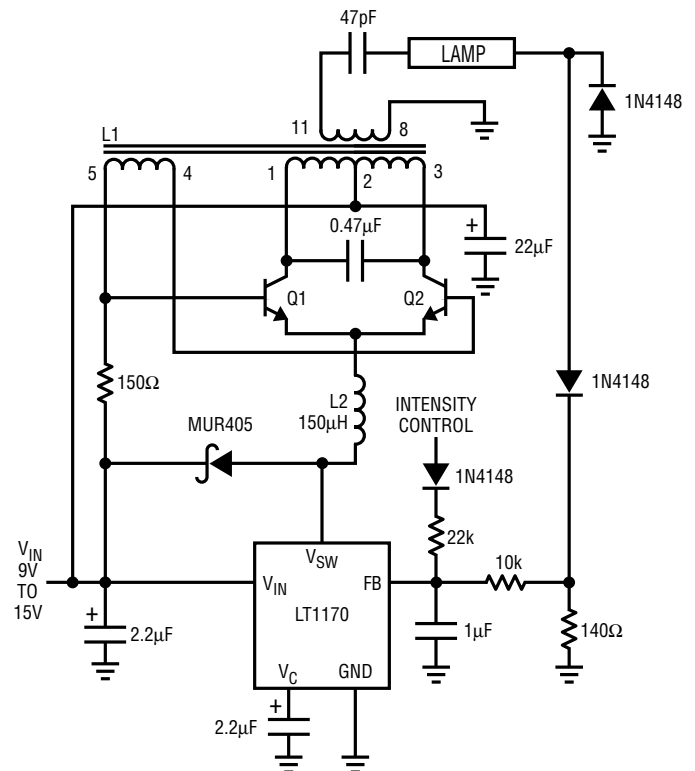
The Royer converter oscillates at a frequency primarily set by T1's characteristics (including its load) and the $0.068\mu\text{F}$ capacitor. LT1301 driven L1 sets the magnitude of the Q1/Q2 tail current, hence T1's drive level. The 1N5817 diode maintains L1's current flow when the LT1301's switch is off. The $0.068\mu\text{F}$ capacitor combines with T1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors. T1 furnishes voltage step-up and about $1400\text{V}_{\text{P-P}}$ appears at its secondary. Alternating current flows through the $22\mu\text{F}$ capacitor into the lamp. On positive half-cycles the lamp's current is steered to ground via D1. On negative half-cycles the lamp's current flows through Q3's collector and is filtered by C1. The LT1301's I_{LIM} pin acts as a 0V summing point with about $25\mu\text{A}$ bias current flowing out of the pin into C1. The LT1301 regulates L1's current to equalize Q3's average collector current, representing 1/2 the lamp current, and R1's current, represented by $V_A/R1$. C1 smooths all current flow to DC. When V_A is set to zero, the I_{LIM} pin's bias current forces about $100\mu\text{A}$ bulb current.

High Power CCFL Power Supply

As mentioned, the CCFL circuit approach presented here scales quite nicely over a wide range of output power. Most circuits are in the 0.5W to 3W region due to the application's small size and battery-driven nature. Automotive, aircraft, desktop computer and other displays often require much higher power.

Figure 44's arrangement is a scaled-up version of the text's CCFL circuits. This design, similar to ones employed for automotive use, drives a 25W CCFL. There are virtually no configuration changes, although most component power ratings have increased. The transistors can handle the higher currents, but all other power components are higher capacity. Efficiency is about 80%.

Additional high power circuits appear in Appendix I, "Additional Circuits."



L1=COILTRONICS CTX02-11128
 L2=COILTRONICS CTX150-3-52
 Q1, Q2=ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
 0.47 μF =WIMA 3X 0.15 μF TYPE MKP-20
 COILTRONICS (407) 241-7876

AN65-F44

Figure 44. A 25W CCFL Supply Is a Scaled Version of Lower Power Circuits

Application Note 65

“Floating” Lamp Circuits

All circuits presented to this point drive the lamp in single-ended fashion. Similarly, Figure 45 shows one lamp electrode receiving drive with the other terminal essentially at ground. This causes significant loss via parasitic paths associated with the lamp’s driven end. This is so because of the large voltage swing in this region. The parasitic paths near the lamp’s grounded end undergo relatively little swing, contributing small energy loss. Unfortunately, the lost energy is heavily voltage-dependent ($E = 1/2 CV^2$) and net energy loss is excessive if driven end parasitics are large. Figure 46 minimizes the losses by altering the drive scheme. In this case the lamp is driven from both ends instead of grounding one end. This “floating” lamp arrangement requires only half the voltage swing at each lamp end instead of full swing at one end. This introduces more loss in the parasitic paths previously associated with

the grounded end. In most cases these increased losses are favorably offset by the reduced swing because of the V^2 loss term associated with voltage amplitude.

The advantage gained varies considerably with display type, although a 10% to 20% reduction in lost energy is common. In some displays loss reduction is not as good, and occasionally improvement is negligible. Heavily asymmetric wiring to or within the display can sometimes make floating drive more lossy than grounded drive. In such cases testing in both modes is necessary to determine which type drive is most efficient.

A second advantage of floating operation is extended illumination range. “Grounded” lamps operating at relatively low currents may display the “thermometer effect,” that is, light intensity may be nonuniformly distributed along lamp length.

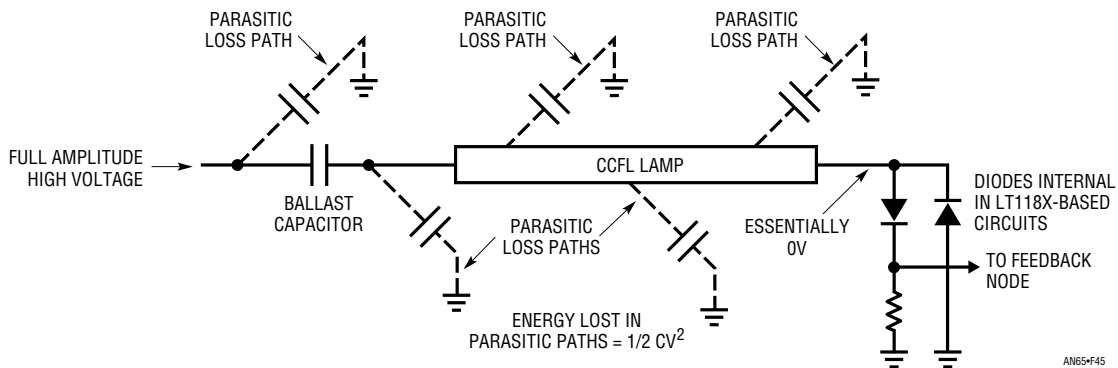


Figure 45. Ground Referred Lamp Drive Has Large Energy Loss in High Voltage Regions Due to Full Amplitude Swing

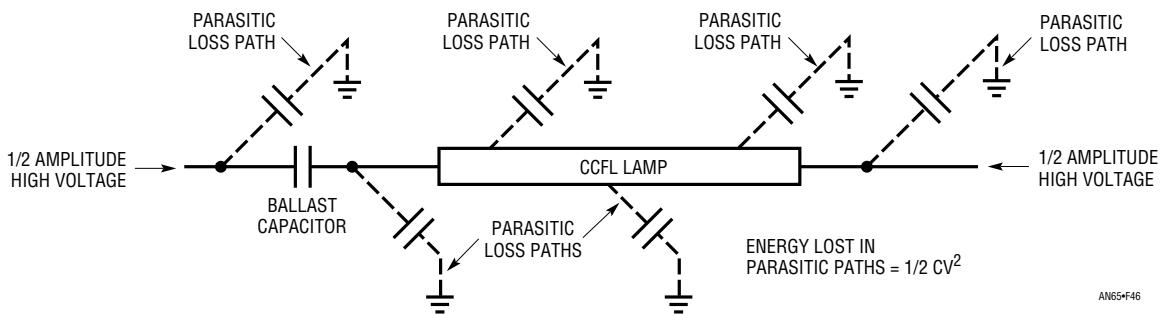


Figure 46. “Floating” Lamp Allows Reduced, Bipolar Drive, Cutting Losses Due to Parasitic Capacitance Paths. Formerly Grounded Lamp End’s Paths Absorb More Energy Than Before, but Overall Loss Is Lower Due to Equation’s V^2 Term

Figure 47 shows that although lamp current density is uniform, the associated field is imbalanced. The field's low intensity, combined with its imbalance, means that there is not enough energy to maintain uniform phosphor glow beyond some point. Lamps displaying the thermometer effect emit most of their light near the driven electrode, with rapid emission fall-off as distance from the electrode

increases. Placing a conductor along the lamp's length largely alleviates "thermometering." The trade-off is decreased efficiency due to energy leakage.¹² It is worth noting that various lamp types have different degrees of susceptibility to the thermometer effect.

Some displays require extended illumination range. "Thermometering" usually limits the lowest practical illumination level. One acceptable way to minimize "thermometering" is to eliminate the large field imbalance. The floating drive used to reduce energy loss also provides a way to minimize "thermometering." Figure 48 reviews a

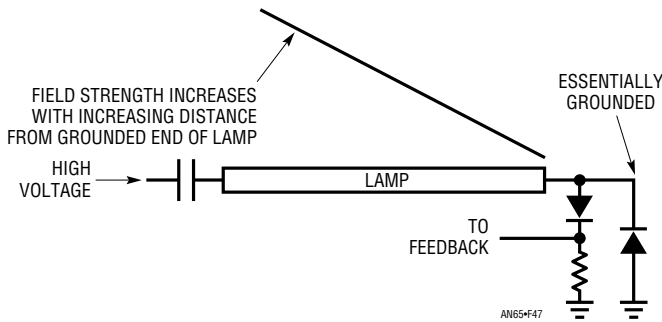


Figure 47. Field Strength vs Distance for a Ground Referred Lamp. Field Imbalance Promotes Uneven Illumination at Low Drive Levels

Note 12. A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the lamp at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb/forefinger combination towards the high voltage (higher field intensity) lamp end produces progressively greater input currents. Don't touch the high voltage lead or you may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.

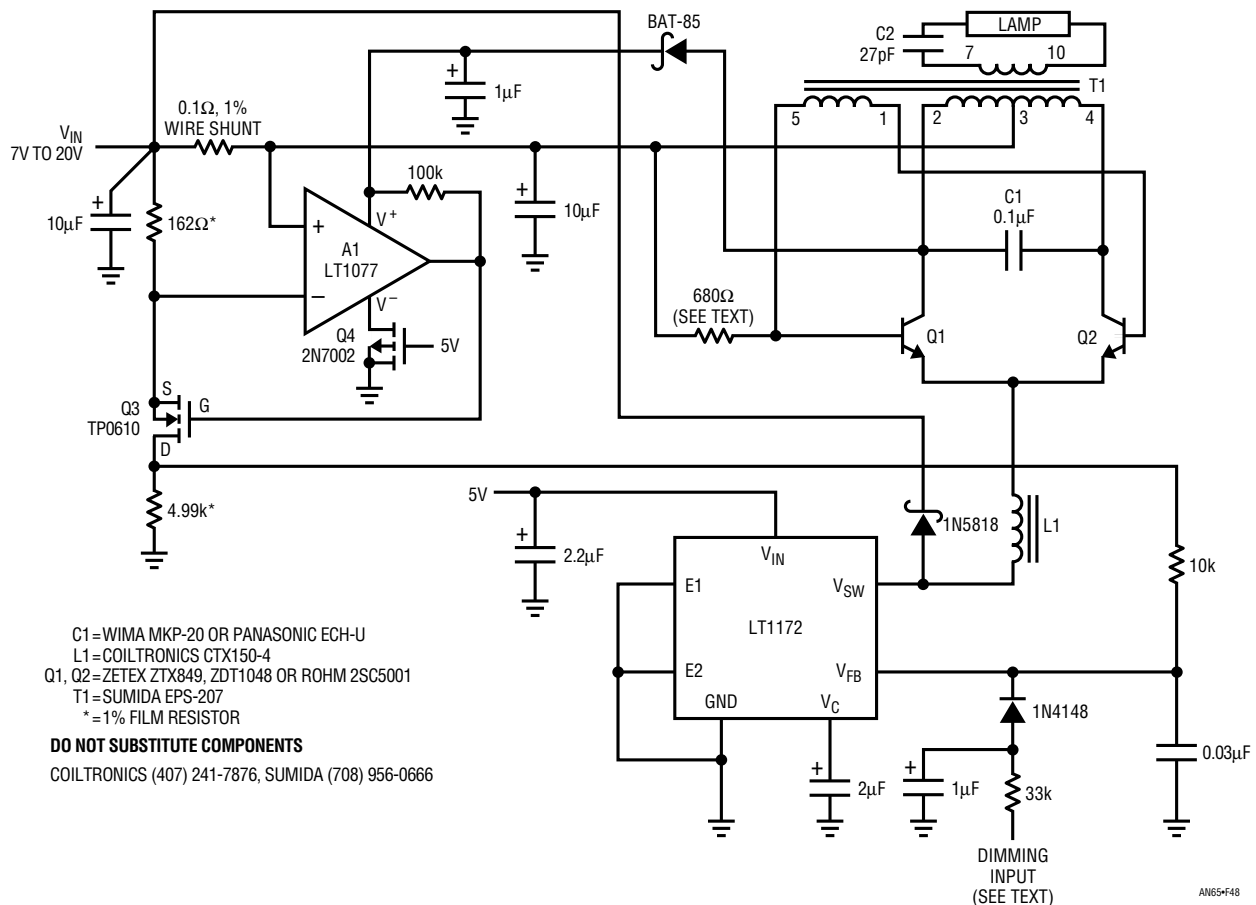


Figure 48. Practical "Floating" Lamp Drive Circuit. A1 Senses Royer Input Current with Q3 Providing Resultant Feedback Information to Switching Regulator. Circuit Reduces Lost Energy Due to Parasitics by 10% to 20%

Application Note 65

circuit originally introduced in a previous publication.¹³ The circuit's most significant aspect is that the lamp is fully floating—there is no galvanic connection to ground as in the previous designs. This allows T1 to deliver symmetric, differential drive to the lamp. Such balanced drive eliminates field imbalance, reducing thermomentering at low lamp currents. This approach precludes any feedback connection to the now floating output. Maintaining closed-loop control necessitates deriving a feedback signal from some other point. In theory, lamp current proportions to T1's or L1's drive level and some form of sensing this can be used to provide feedback. In practice, parasitics make a practical implementation difficult.¹⁴

Figure 48 derives the feedback signal by measuring Royer converter current and feeding this information back to the LT1172. The Royer's drive requirement closely proportions to lamp current under all conditions. A1 senses this current across the 0.1Ω shunt and biases Q3, closing a

local feedback loop. Q3's drain voltage presents an amplified, single-ended version of the shunt voltage to the feedback point, closing the main loop. A1's power supply pin is bootstrapped to T1's boosted swing via the BAT-85 diode, permitting it to sense across the supply-fed shunt resistor. Internal A1 characteristics ensure start-up and substitution of this device is not recommended.¹⁵

The lamp current is not as tightly controlled as before but 0.5% regulation over wide supply ranges is possible. The dimming in this circuit is controlled by a 1kHz PWM signal. Note the heavy filtering (33k/1μF) *outside* the feedback loop. This allows a fast time constant, minimizing turn-on overshoot.¹⁶

Note 13. See Reference 1.

Note 14. See Appendix L, "A Lot of Cut Off Ears and No Van Goghs—Some Not-So-Great Ideas," for details.

Note 15. See Reference 1, then don't say we didn't warn you.

Note 16. See text section, "Feedback Loop Stability Issues."

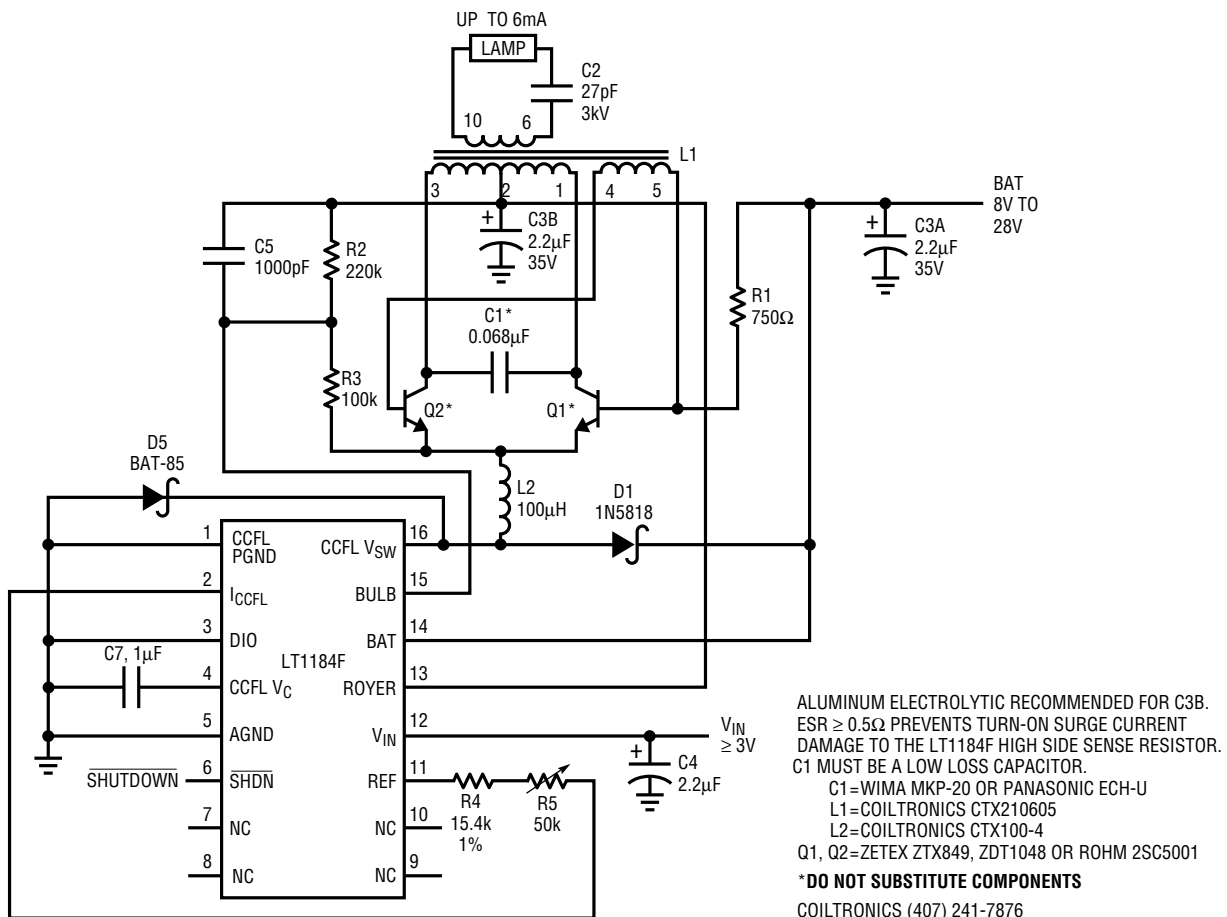


Figure 49. LT1184F IC Version of Figure 48's Floating Lamp Circuit Offers Similar Performance with Fewer Components. Open Bulb Protection and Shutdown Are Included

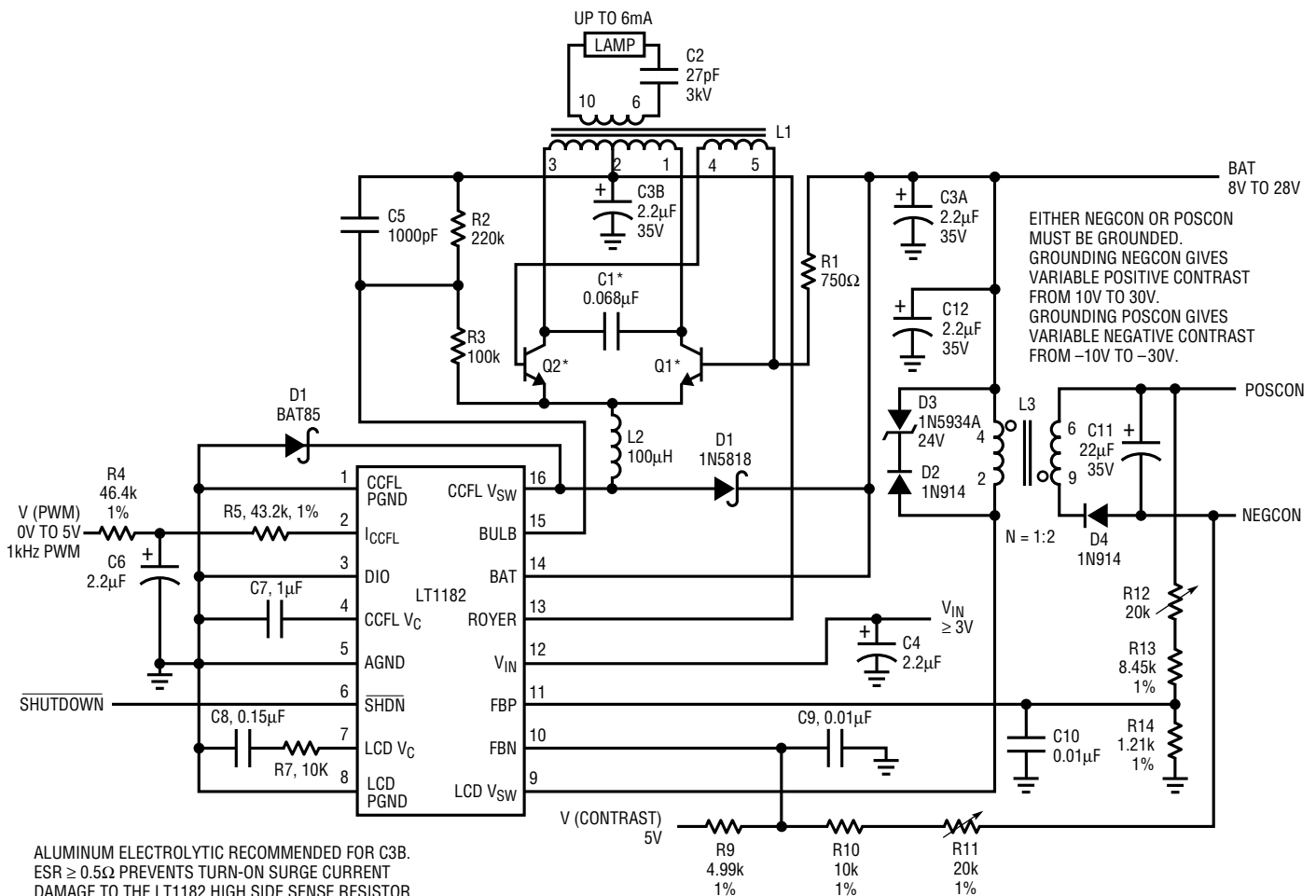
In all other respects operation is similar to the previous circuits. This circuit typically permits the lamp to operate with less energy loss and over a 40:1 intensity range without “thermometering.” The normal feedback connection is usually limited to a 10:1 range.

IC-Based Floating Drive Circuits

Figure 49 compacts Figure 48 into a low component count, floating drive circuit. The LT1184F IC contains all func-

tions except the Royer-based high voltage converter. The circuit also has “open lamp” protection and a 1.23V reference for biasing the dimming potentiometer.

Figure 50 adds a bipolar LCD contrast supply output to Figure 49. The LT1182 allows setting contrast supply polarity by simply grounding the appropriate output terminal. The CCFL portion is similar to the previous circuit, although intensity is controlled with a varying PWM or 0V to 5V input.



ALUMINUM ELECTROLYTIC RECOMMENDED FOR C3B.
 ESR $\geq 0.5\Omega$ PREVENTS TURN-ON SURGE CURRENT
 DAMAGE TO THE LT1182 HIGH SIDE SENSE RESISTOR.
 C1 MUST BE A LOW LOSS CAPACITOR.
 C1=WIMA MKP-20 OR PANASONIC ECH-U
 L1=COILTRONICS CTX210605
 L2=COILTRONICS CTX100-4
 L3=COILTRONICS CTX02-12403
 Q1, Q2=ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
***DO NOT SUBSTITUTE COMPONENTS**
 COILTRONICS (407) 241-7876

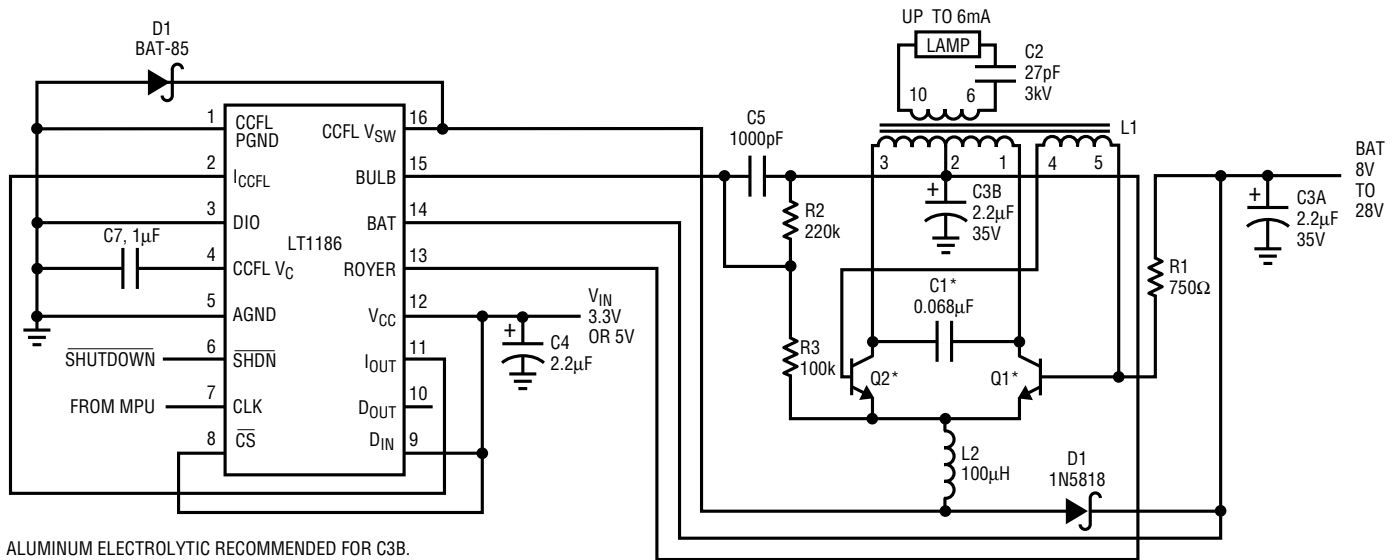
EITHER NEGCON OR POSCON
 MUST BE GROUNDING.
 GROUNDING NEGCON GIVES
 VARIABLE POSITIVE CONTRAST
 FROM 10V TO 30V.
 GROUNDING POSCON GIVES
 VARIABLE NEGATIVE CONTRAST
 FROM -10V TO -30V.

Figure 50. LT1182 Has Bipolar Output Contrast Supply in Addition to Floating Lamp Drive

Application Note 65

Figure 51's circuit is similar, although no contrast supply is included. The LT1186 implements a floating lamp drive similar to Figure 49. This IC contains an internal D/A converter which may be addressed by accumulating a bit

stream or serial protocol. Figure 52 shows a typical arrangement using an 80C31 type microcontroller. Figure 53 gives the complete software listing which was written by Tommy Wu of LTC.



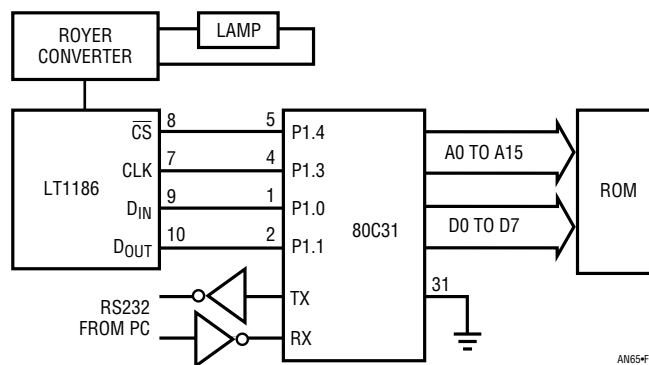
ALUMINUM ELECTROLYTIC RECOMMENDED FOR C3B.
 ESR $\geq 0.5\Omega$ PREVENTS TURN-ON SURGE CURRENT
 DAMAGE TO THE LT1186 HIGH SIDE SENSE RESISTOR.
 C1 MUST BE A LOW LOSS CAPACITOR.

C1=WIMA MKP-20 OR PANASONIC ECH-U
 L1=COILTRONICS CTX210605
 L2=COILTRONICS CTX100-4
 Q1, Q2=ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001

***DO NOT SUBSTITUTE COMPONENTS**
 COILTRONICS (407) 241-7876

AN65#F51

Figure 51. LT1186 Permits Serial or Bit Stream Data Addressing to Set Floating Lamp Current



AN65#F52

Figure 52. Typical Processor Interface for Figure 51

The LT1186 DAC algorithm is written in assembly code in a file named LT1186A.ASM as a function call from the MAIN function below.

Note: A user inputs an integer from 0 to 255 on a keyboard and the LT1186 adjusts the IOUT programming current to control the operating lamp current and the brightness of the LCD display.

```
#include <stdio.h>
#include <reg51.h>
#include <absacc.h>

extern char lt1186(char); /* external assembly function in lt1186a.asm*/
sbit Clock = 0x93;

main()
{
    int number = 0;
    int LstCode;

    Clock = 0;

    TMOD = 0x20; /* Establish serial communication 1200 baud */
    TH1 = 0xE8;
    SCON = 0x52;
    TCON = 0x69;

    while(1) /* Endless loop */
    {
        printf("\nEnter any code from 0 - 255:");
        scanf("%d",&number);
        if((0>number)|(number>255))
        {
            number = 0;
            printf("The number exceeds its range. Try again!");
        }
        else
        {
            LstCode = lt1186(number);
            printf("Previous # %u", (LstCode&0xFF)); /* AND the previous number with 0xFF to turn off sign
            extension */
        }
        number = 0;
    }
}
```

; The following assembly program named LT1186A.ASM receives the Din word from the main C program,
; lt1186 lt1186(). Assembly to C interface headers, declarations and memory allocations are listed before the
; actual assembly code.

```
;
; Port p1.4 = CS
; Port p1.3 = CLK
; Port p1.1 = Dout
; Port p1.0 = Din
;
```

Figure 53. Complete Software Listing for Figure 52's Processor Interface

Application Note 65

```
NAME LT1186_CCFL
PUBLIC It1186, ?It1186?BYTE

?PR?ADC_INTERFACE?LT1186_CCFL SEGMENT CODE
?DT?ADC_INTERFACE?LT1186_CCFL SEGMENT DATA

                RSEG ?DT?ADC_INTERFACE?LT1186_CCFL
?It1186?BYTE: DS 2

                RSEG ?PR?ADC_INTERFACE?LT1186_CCFL

CS    EQU    p1.4
CLK   EQU    p1.3
DOUT  EQU    p1.1
DIN   EQU    P1.0

lt1186: setb   CS                ;set CS high to initialize the LT1186
        mov    r7,?It1186?BYTE   ;move input number(Din) from keyboard to R7
        mov    p1, #01h          ;setup port p1.0 becomes input
        clr    CS                ;CS goes low, enable the DAC
        mov    a, r7              ;move the Din to accumulator
        mov    r4, #08h          ;load counter 8 counts
        clr    c                 ;clear carry before rotating
        rlc    a                 ;rotate left Din bit(MSB) into carry
loop:   mov    DIN, c            ;move carry bit to Din port
        setb   CLK              ;Clk goes high for LT1186 to latch Din bit
        mov    c, DOUT          ;read Dout bit into carry
        rlc    a                 ;rotate left Dout bit into accumulator
        clr    CLK              ;clear clock to shift the next Dout bit
        djnz  r4, loop          ;next data bit loop
        mov    r7, a            ;move previous code to R7 as character return
        setb   CS                ;bring CS high to disable DAC
        ret
        END
```

Note: When CS goes low, the MSB of the previous code appears at Dout.

Figure 53 (continued). Complete Software Listing for Figure 52's Processor Interface

High Power Floating Lamp Circuit

High power floating lamp circuits require more current than the LT118X series can deliver. In such cases the function can be built from discrete components and ICs. Figure 54 shows a 30W CCFL circuit used in an automotive application. This 4-lamp circuit uses an LT1269 current-fed Royer converter to provide high power. Lamp current is sensed in current transformer T2. A1 and associated components form a synchronous rectifier for T2's low level output. A2 provides gain and closes a loop back at the

LT1269's feedback terminal. T2's isolated sensing permits the advantages of floating operation with the LT1269 providing high power capability. This circuit has about 83% efficiency at 30W output, a wide dimming range and 0.1% line regulation.

Selection Criteria for CCFL Circuits

Selecting which CCFL circuit to use for a specific application involves numerous trade-offs. A variety of issues determine which circuit is the "best" approach. At a

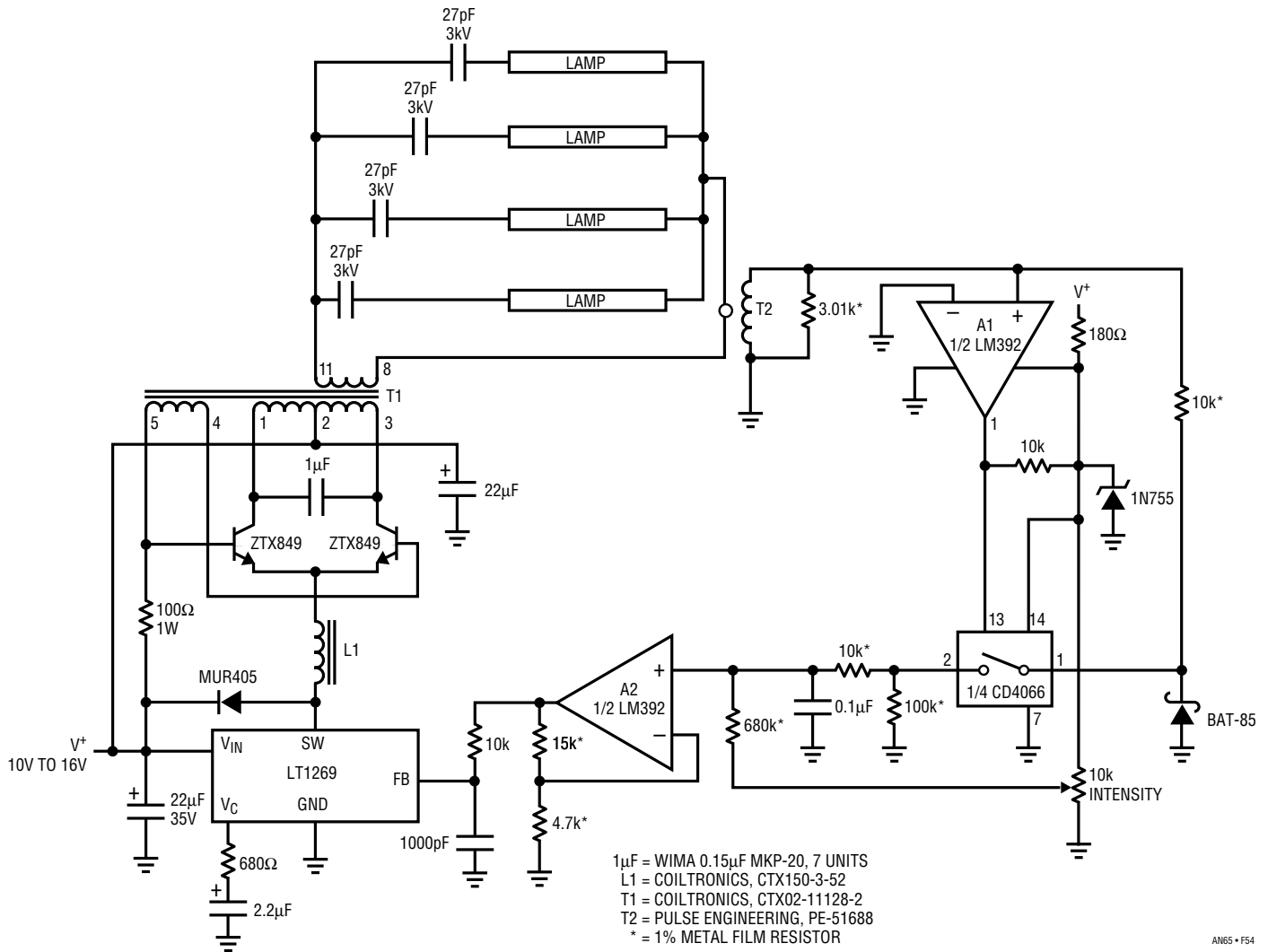


Figure 54. A High Power, Multilamp Display Using the Floating Drive Approach. Power Requirement Necessitates LT1269 Regulator and Discrete Component Approach. Floating Feedback Path Is Via Current Transformer

minimum, the user should consider the following guidelines before committing to any approach. Related discussion to all of the following topics is covered in appropriate text sections.

Display Characteristics

The display characteristics (including wiring losses) should be well-understood. Typically, display manufacturers list *lamp* requirements. These specifications are often obtained from the lamp vendor, who usually tests in free air, with no significant parasitic loss paths. This means that actual required power, start and running voltages may significantly differ from data sheet specifications. The only

way to be certain of display characteristics is to measure them. The measured display energy loss can determine if a floating or grounded circuit is applicable. Low loss displays (relatively rare) usually provide better overall efficiency with grounded drive. As losses become worse (unfortunately, relatively common) floating drive becomes a better choice. Efficiency measurements may be required in both modes to determine the best choice. (See “General Optimization and Measurement Considerations.”)

Operating Voltage Range

The operating voltage range includes the minimum to maximum voltages the circuit must operate from. In

Application Note 65

battery-driven apparatus supply range can easily be 3:1, and sometimes greater. Best backlight performance is usually obtained in the 8V to 28V range. In general, potentials below 7V require some efficiency trade-offs at moderate (1.5W to 3W) power levels. Some systems reduce backlight power when running from the battery, and this can have a pronounced effect on the design. Even seemingly small (e.g., 20%) reductions in power may make painful trade-offs unnecessary. In particular, high turns ratio transformers are required to support low voltage operation at full lamp output. They work well but somewhat less efficiently than lower ratio types due to the higher peak currents characteristic of their operation. Current trends in battery technology encourage system operation at low voltages, necessitating extreme care in transformer selection and Royer circuit design.

Auxiliary Operating Voltages

Auxiliary, logic supply voltages should be used (if available) to run CCFL “housekeeping” currents, such as IC “V_{IN}” pins. This saves power. Always run switching regulators from the lowest potential available, usually 3.3V or 5V. Many systems provide these voltages in switched form, making separate shutdown lines unnecessary. Simply turning off the switching regulator’s supply shuts the entire backlight circuit down.

Line Regulation

Grounded lamp circuits, by virtue of their true global feedback, provide the best line regulation. For abrupt changes, a user may notice anything beyond 1% regulation. A grounded circuit easily meets this requirement; a floating circuit usually will. Slowly changing line inputs causing excursions outside 1% are not normally a problem because they are not detectable. Rapid line changes, such as plugging in a systems AC line adapter, require good regulation to avoid annoying display flicker.

Power Requirements

The CCFL’s power requirement, *including display and wiring losses*, should be well-defined over all conditions, including temperature and lamp specification variations. Usually, IC versions of floating lamp circuits are restricted to 3W to 4W output power while grounded circuit power is easily scaled.

Supply Current Profile

The backlight is often physically located far “forward” in the system. Impedances in cables, switches, traces and connectors can build up to significant levels. This means that a CCFL circuit should draw operating power continuously, rather than requiring discrete, high current “chunks” from a lossy supply line. Royer-based architectures are nearly ideal in this regard, pulling current smoothly over time and requiring no special bypassing, supply impedance or layout treatment. Similarly, Royer type circuits do not cause significant disturbances to the supply line, preventing noise injection back into the supply.

Lamp Current Certainty

The ability to predict lamp current at full intensity is important to maintain lamp life. Excessive overcurrent greatly shortens lamp life, while yielding little luminosity benefit (see Figure 2). Grounded circuits are excellent in this category with 1% usually achieved. Floating circuits are typically in the 2% to 5% range. Tight current tolerances do not benefit unit/unit display luminosity because lamp emission and display attenuation variations approach $\pm 20\%$ and vary over life.

Efficiency

CCFL backlight efficiency should be considered from two perspectives. The electrical efficiency is the ability of the circuit to convert DC power to high voltage AC and deliver it to the load (lamp and parasitics) with minimum loss. The optical efficiency is perhaps more meaningful to the user. It is simply the ratio of display luminosity to DC power into the CCFL circuit. The electrical and optical losses are lumped together in this measurement to produce a luminosity vs power specification. It is quite significant that *the electrical and optical peak efficiency operating points do not necessarily coincide*. This is primarily due to the lamp’s emissivity dependence on waveshape. The optimum waveshape for emissivity may or may not coincide with the circuit’s electrical operating peak. In fact, it is quite possible for “inefficient” circuits to produce more light than “more efficient” versions. The only way to ensure peak efficiency in a given situation is to optimize the circuit to the display.

Shutdown

System shutdown almost always requires turning off the backlight. In many cases the low voltage supply is already available in switched form. If this is so, the CCFL circuits shown go off, absorbing very little power. If switched low voltage power is not available the shutdown inputs may be used, requiring an extra control line.

Transient Response

The CCFL circuit should turn on the lamp without attendant overshoot or poor control loop settling characteristics. This can cause objectionable display flicker, and in the worst case result in transformer overstress and failure. Properly prepared floating and grounded CCFL circuits have good transient response, with LT118X-based types inherently easier to optimize.

Dimming Control

The method of dimming should be considered early in the design. All of the circuits shown can be controlled by potentiometers, DC voltages and currents, pulse width modulation or serial data protocol. A dimming scheme with high accuracy at maximum current prevents excessive lamp drive and should be employed.

Open Lamp Protection

The CCFL circuits deliver a current source output. If the lamp is broken or disconnected, compliance voltage is limited by transformer turns ratio and DC input voltage. Excessive voltages can cause arcing and resultant damage. Typically, the transformers withstand this condition but open lamp protection ensures against failures. This feature is built into the LT118X series; it must be added to other circuits.

Size

Backlight circuits usually have severe size and component count limitations. The board must fit within tightly defined dimensions. LT118X series-based circuits offer lowest component count, although board space is usually dominated by the Royer transformer. In extremely tight spaces

it may be necessary to physically segment the circuit but this should be considered as a last resort.¹⁷

Contrast Supply Capability

Some LT118X parts provide contrast supply outputs. The other circuits do not. The LT118X's onboard contrast supply is usually an advantage but space is sometimes so restricted that it cannot be used. In such cases the contrast supply must be remotely located.

Emissions

Backlight circuits rarely cause emission problems and shielding is usually not required. Higher power versions (e.g., >5W) may require attention to meet emission requirements. The fast rise switching regulator output sometimes causes more RFI than the high voltage AC waveform. If shielding is used, its parasitic effects are part of the inverter load and optimization must be carried out with the shield in place.

Summary of Circuits

The interdependence of backlight parameters makes summarizing or rating various approaches a hazardous exercise. There is simply no intellectually responsible way to streamline the selection and design process if optimum results are desired. A meaningful choice *must* be the outcome of laboratory-based experimentation. There are just too many interdependent variables and surprises for a systematic, theoretically based selection. Pure analytics are pretty; working circuits come from the bench. Some generalizations having limited usefulness are, however, possible. Figures 55 and 56 attempt to summarize salient characteristics vs part type and may (however cautiously) be considered a beginning point.¹⁸

Figure 55 summarizes characteristics of all the circuits. Figure 56 focuses on the features of the LT118X series parts.

Note 17. See Appendix G, "Layout, Component and Emissions Considerations."

Note 18. Readers detecting author ambivalence about inclusion of Figures 55 and 56 are not hallucinating.

Application Note 65

ISSUES	LT118X SERIES	LT117X SERIES	LT137X SERIES
Optical Efficiency	Grounded output versions display dependent. Floating versions usually 5% to 20% better.	Display dependent	Display dependent
Electrical Efficiency	Grounded output versions—75% to 90%, depending on supply voltage and display. Floating output versions slightly lower.	75% to 90%, depending on supply voltage and display	75% to 92%, depending on supply voltage and display
Lamp Current Certainty	1% to 2% for grounded versions, 1% to 4% for floating output types	2% maximum	2% maximum
Line Regulation	0.1% to 0.3% for grounded types, 0.5% to 6% for floating versions	0.1% to 0.3%	0.1% to 3%
Operating Voltage Range	5.3V to 30V, depending on output power, temperature range, display, etc.	4.0V to 30V, depending on output power, temperature range, display etc.	4.0V to 30V, depending on output power, temperature range, display, etc.
Power Range	0.75W to 6W typical	0.75W to 20W typical	0.5W to 6W typical
Supply Current Profile	Continuous—no high current peaks	Continuous—no high current peaks	Continuous—no high current peaks
Shutdown Control	Yes—logic compatible	Requires small FET or bipolar transistor	Yes—logic compatible
Transient Response—Overshoot	Excellent—no optimization required	Excellent—requires optimization in some cases	Excellent—requires optimization in some cases
Dimming Control	Pot., PWM, variable DC voltage or current. LT1186 has serial digital input with data storage.	Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current
Emissions	Low	Low	Low, although high power versions may require attention to layout and shielding
Open Lamp Protection	Internal to IC	Requires external small-signal transistor and some discretes at high supply voltages	Requires external small-signal transistor and some discretes at high supply voltages
Size	Low component count, small overall board footprint. 200kHz magnetics.	Small—100kHz magnetics	Small—1MHz magnetics for fastest versions
Contrast Supply Capability	Various contrast supply options available, including bipolar output	No	No

AN65-F55-1

Figure 55. Design Issues vs Typical Part Choice. Chart Makes Simplistic Assumptions and Is Intended As a Guide Only

LT1269/LT1270	LT1301	LT1173
Display dependent	Display dependent	Display dependent
75% to 90%, depending on supply voltage and display	70% to 88%, depending on supply voltage and display	65% to 75%, depending on supply voltage and display
2% maximum	2% typical	5%
0.1% to 0.3%	0.1% to 0.3%	8% to 10%
4.5V to 30V, depending on output power, temperature range, display, etc.	2V to 10V practical	2V to 6V practical
5W to 35W typical	0.02W to 1W practical	Essentially 0W to about 0.6W
Continuous—no high current peaks	Continuous—no high current peaks	Irregular—relatively high current peaking requires attention to supply rail impedance
Requires small FET or bipolar transistor	Yes—logic compatible	Logic compatible shutdown practical
Excellent—requires optimization in some cases	Excellent—no optimization required	Excellent—no optimization required
Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current
High power mandates attention to layout and shielding	Real low	Itsy-bitsy
Requires external small-signal transistor and some discretes at high supply voltages	Requires external small-signal transistor and some discretes, but low supply voltages usually eliminate this consideration	None, but low supply, low power operation usually eliminates this issue
Relatively large due to high power 100kHz magnetics	Very small—low power magnetics cut size	Small—low power magnetics cut size
No	No	No

AN65-F55-2

Application Note 65

	LT1182	LT1183	LT1184	LT1184F	LT1186
Floating Lamp Operation	Yes	Yes	No	Yes	Yes
Grounded Lamp Operation	Yes	Yes	Yes	Yes	Yes
Contrast Supply	Bipolar Contrast Outputs	Unipolar Contrast Outputs	No	No	No
Voltage Reference Available	No	Yes	Yes	Yes	No
Internal Control DAC	No	No	No	No	Yes

Figure 56. Features of Various LT118X IC Backlight Controllers

General Optimization and Measurement Considerations

Once a display/lamp combination has been picked, the appropriate circuit can be selected and optimized. “Optimization” implies maximizing performance in those areas most important in a particular application. This may involve trading off characteristics in one area to gain advantage in another. The circuit types described impose mild penalty in this regard because they are quite flexible.

A desirable characteristic is something often loosely referred to as “efficiency.” There are really two types of efficiency in a backlight circuit. The *optical* efficiency measures the circuit/display combination as a transducer. It is the ratio of light output to electrical power input. This ratio lumps the converter’s electrical loss with lamp and display losses. A backlight’s *electrical* efficiency measures the converter’s electrical input vs output power without regard to optical performance. Obviously, high electrical efficiency is required and a reliable way to measure it is desirable. More subtly, the ability to measure and manipulate purely electrical terms offers a way to influence optical efficiency. This is so because the lamp is sensitive to the drive waveform’s shape. Best emissivity and lifetime are usually obtained with low crest factor, sinusoidal waveforms. The Royer circuit’s transformer and capacitors can be selected to provide this characteristic for any given display/lamp combination. Doing this optimizes lamp drive but also effects the converter’s electrical efficiency. This interaction between the optimum electrical and optical operating points must be accounted for to obtain best optical efficiency. The relationship is

quite complex with a number of variables determining just where peak optical efficiency occurs.

Typically, optical output peaking occurs with a fairly clean, low harmonic waveform at the Royer collectors (Figure 57). This is usually the result of a relatively large resonating capacitor and a small ballast capacitor. Conversely, the converter’s peak electrical efficiency point usually comes just as appreciable second harmonic appears in the Royer collector waveform (Figure 58). The peak electrical and optical efficiency points almost never coincide and optical efficiency often occurs 5% or more off the electrical efficiency peak. Happily, this very messy situation can be resolved by a relatively simple functional trim. The trimming procedure assumes transformer turns ratio and ballast capacitor values commensurate with the lowest

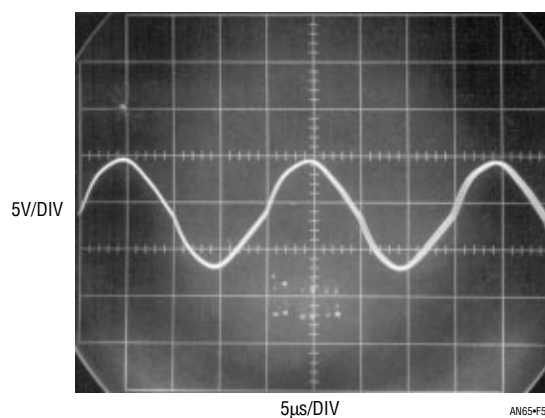


Figure 57. Typical Royer Collector Waveform at the Peak Optical Output Point. Relatively Large Resonating Capacitor May Degrade Electrical Efficiency

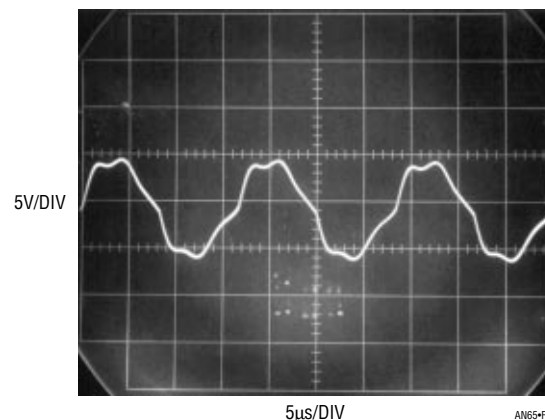


Figure 58. Typical Royer Collector Waveform at the Peak Electrical Efficiency Point. Relatively High Harmonic Content May Degrade Optical Efficiency

required circuit operating voltage have been chosen. If this factor is not considered, the optical efficiency peak will be realized but the design may not regulate at low supply voltages. Low supply voltage operation mandates high turns ratio and larger ballast capacitor values for a given display loss. If display loss is high, ballast capacitor value generally must rise to offset voltage dividing effects between it and the display's parasitic loss paths. Establish the lowest values of turns ratio and ballast capacitor that maintain regulation at minimum supply voltage before performing the trim.

Achieving peak optical efficiency involves comparing display luminosity to input power for different resonating capacitor values. For a given lamp/transformer/ ballast capacitor combination different resonating capacitors produce varying amounts of light. Large values tend to smooth harmonics, peaking optical output but increasing converter circulating losses. Smaller values promote lower circulating currents but less light output. Figure 59 shows typical results for five capacitor values at a forced 10V main supply and 5mA lamp current. Large values produce more light but require more supply current. The raw data is expressed as the ratio of light output-per-watt of input power in the right-most column. This Nits-per-Watt ratio peaks at 0.1 μ F, indicating the best optical efficiency.¹⁹

This test must be performed in a stable thermal environment because of the lamp's emission sensitivity to temperature (see Figure 3). Additionally, some arrangement for rapidly switching the capacitor values is desirable. This avoids power interruptions and the resultant long display warm-up times.

CAPACITOR (μ F)	10V MAIN SUPPLY CURRENT	5V SUPPLY CURRENT	TOTAL SUPPLY WATTS	INTENSITY (NITS)	NITS/WATT
0.15	0.304	0.014	3.11	118	37.9
0.1	0.269	0.013	2.75	112	40.7
0.068	0.259	0.013	2.65	101	38.1
0.047	0.251	0.013	2.57	95	37.3
0.033	0.240	0.013	2.46	88	35.7

Note: Maintain I_{MAIN} Supply = 10.0V and I_{LAMP} = 5mA_{RMS} under all conditions.

Figure 59. Typical Data Taken for Optical Efficiency Optimization. Note Emissivity Peak (Nits/Watt) for 0.1 μ F Resonating Value, Indicating Best Trade-Off Point for Electrical vs Optical Efficiency. Data Should Be Retaken for Several Ballast Capacitor Values to Ensure Maximum Optical Efficiency

Electrical Efficiency Optimization and Measurement

Several points should be kept in mind when observing operation of these circuits. The high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*²⁰ Tektronix probe types P-6007 and P-6009 (acceptable in some cases) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The switching regulator frequency is completely asynchronous from the Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 36 was obtained using a dual beam oscilloscope (Tektronix 556). Traces A and B are triggered on one beam while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used but are less versatile and restricted to four traces.

Obtaining and verifying high electrical efficiency²¹ requires some amount of diligence. The optimum efficiency values given for C1 and C2 (C1 is the resonating capacitor and C2 is the ballast capacitor) are typical and will vary for specific types of lamps. An important realization is that the term "lamp" includes the *total* load seen by the transformer's secondary. This load, reflected back to the primary, sets transformer input impedance. The transformer's input impedance forms an integral part of the LC tank that produces the high voltage drive. Because of this, circuit efficiency must be optimized with the

Note 19. Optical measurement units are beyond arcane; a monument to obscurity. Candela/Meter² is a basic unit, and 1 Nit = 1 Candela/Meter². "Nit" is a contracted form of the Latin word "Nitere," meaning "to emit light . . . to sparkle."

Note 20. Don't say we didn't warn you!

Note 21. The term "efficiency" as used here applies to electrical efficiency. In fact, the ultimate concern centers around the efficient conversion of power supply energy into light. Unfortunately, lamp types show considerable deviation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life and history of any particular lamp. As such, this text portion treats "efficiency" on an electrical basis; the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp/display combination has been selected, the ratio of primary supply power to lamp emitted light energy may be measured with the aid of a photometer. This is covered in the immediately preceding text and Appendix D.

Application Note 65

wiring, display housing and physical layout arranged *exactly* the same way they will be built in production. Deviations from this procedure will result in lower efficiency than might otherwise be possible. In practice, a “first cut” efficiency optimization with “best guess” lead lengths and the intended lamp in its display housing usually produces results within 5% of the achievable figure. Final values for C1 and C2 may be established when the physical layout to be used in production has been decided on. C1 sets the circuit’s resonance point, which varies to some extent with the lamp’s characteristic. C2 ballasts the lamp, effectively buffering its negative resistance characteristic. Small C2 values provide the most load isolation but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage but degrade load buffering. C2 values also affect waveform distortion, influencing lamp emissivity and optical efficiency (see previous text discussion). Also, C1’s “best” value is somewhat dependent on the lamp type used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but generalized guidelines are possible. Typical values for C1 are 0.01 μ F to 0.15 μ F. C2 usually ends up in the 10pF to 47pF range. C1 *must* be a low loss capacitor and substitution of the recommended devices is not recommended. A poor quality dielectric for C1 can easily degrade efficiency by 10%. Before capacitor selection the Q1/Q2 base drive resistor should be set to a value which ensures saturation, e.g., 470 Ω . Next, C1 and C2 are selected by trying different values for each and iterating towards best efficiency. During this procedure ensure that loop closure is maintained. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q1, Q2 and output. Finally, the base drive resistor’s value should be optimized.

The base drive resistor’s value (nominally 1k) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. This point may be established for any lamp type by determining the peak collector current at full lamp power.

The base resistor should be set at the largest value that ensures saturation for worst-case transistor beta. This condition may be verified by varying the base drive resis-

tor about the ideal value and noting small variations in input supply current. The minimum obtainable current corresponds to the best beta vs saturation trade-off. In practice, supply current rises slightly on either side of this point. This “double value” behavior is due to efficiency degradation caused by either excessive base drive or saturation losses.

Other issues influencing efficiency include lamp wire length and energy leakage from the lamp. The high voltage side(s) of the lamp should have the smallest practical lead length. Excessive length results in radiative losses which can easily reach 3% for a 3-inch wire. Similarly, no metal should contact or be in close proximity to the lamp. This prevents energy leakage which can exceed 10%.²²

It is worth noting that a custom designed lamp affords the best possible results. A jointly tailored lamp/circuit combination permits precise optimization of circuit operation, yielding highest efficiency.

These considerations should be made with knowledge of other LCD issues. See Appendix B, “Mechanical Design Considerations for Liquid Crystal Displays.” This section was guest-written by Charles L. Guthrie of Sharp Electronics Corporation.

Special attention should be given to the circuit board layout since high voltage is generated at the output. The output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination buildup can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. It is good practice for minimization of leakage to break the silk screen line which outlines the transformer. This prevents leakage from the

Note 22. This footnote annotates similar issues raised in Footnote 12 and associated text. The repetition is based on the necessity for emphasis. A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the lamp at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb/forefinger combination towards the high voltage (higher field intensity) lamp end produces progressively greater input currents. Don’t touch the high voltage lead or you may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.

high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk screen ink for its ability to withstand high voltages. Appendix G, “Layout, Component and Emissions Considerations,” details high voltage layout practice.

Electrical Efficiency Measurement

Once these procedures have been followed efficiency can be measured. Efficiency may be measured by determining lamp current and voltage. Measuring current involves utilization of a wideband, high accuracy clip-on current probe having a true (thermally based) RMS readout. No commercially manufactured current probe will meet the accuracy and bandwidth requirements and the probe must be constructed.²³

Lamp RMS voltage is measured at the lamp with a wideband, properly compensated high voltage probe.²⁴ Multiplying these two results gives power in watts, which may be compared to the DC input supply (E)(I) product. In practice, the lamp’s current and voltage contain small out-of-phase components but their error contribution is negligible.

Both the current and voltage measurements require a wideband true RMS voltmeter. The meter must employ a thermal type RMS converter—the more common logarithmic computing type-based instruments are inappropriate because their bandwidth is too low.

The previously recommended high voltage probes are designed to see a 1M Ω /10pF-22pF oscilloscope input. The RMS voltmeters have a 10M Ω input. This difference necessitates an impedance matching network between the probe and the voltmeter. Floating lamp circuits require this matching and differential measurement, severely complicating instrumentation design. See Footnote 24.

Feedback Loop Stability Issues

The circuits shown to this point rely on closed-loop feedback to maintain the operating point. All linear closed-loop systems require some form of frequency compensation to achieve dynamic stability. Circuits operating with relatively low power lamps may be frequency compensated by simply overdamping the loop. Text Figures 35, 37 and 38 use this approach. The higher power operation

associated with color displays requires more attention to loop response. The transformer produces much higher output voltages, particularly at start-up. Poor loop damping can allow transformer voltage ratings to be exceeded, causing arcing and failure. As such, higher power designs may require optimization of transient response characteristics. LT118X series parts almost never require optimization because their error amplifier’s gain/phase characteristics are specially tailored to CCFL load characteristics. The LT1172, LT1372 and other general purpose switching regulators require more attention to ensure proper behavior. The following discussion, applicable to general purpose LTC switching regulators in CCFL applications, uses the LT1172 as an example.

Figure 60 shows the significant contributors to loop transmission in these circuits. The resonant Royer converter delivers information at about 50kHz to the lamp. This information is smoothed by the RC averaging time constant and delivered to the LT1172’s feedback terminal as

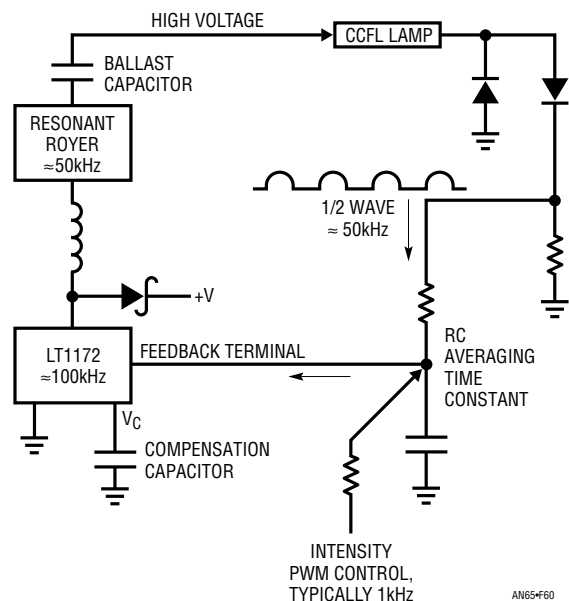


Figure 60. Delay Terms in the Feedback Path. The RC Time Constant Dominates Loop Transmission Delay and Must Be Compensated for Stable Operation

Note 23. Justification for this requirement and construction details appear in Appendix C, “Achieving Meaningful Electrical Measurements.”

Note 24. Measuring floating lamp circuit voltages is a particularly demanding exercise requiring a wideband differential high voltage probe. Probe construction details appear in Appendix C.

Application Note 65

DC. The LT1172 controls the Royer converter at a 100kHz rate, closing the control loop. The capacitor at the LT1172 rolls off gain, nominally stabilizing the loop. This compensation capacitor must roll off the gain-bandwidth at a low enough value to prevent the various loop delays from causing oscillation.

Which of these delays is the most significant? From a stability viewpoint the LT1172's output repetition rate and the Royer's oscillation frequency are sampled data systems. Their information delivery rate is far above the RC averaging time constants delay and is not significant. The RC time constant is the major contributor to loop delay. This time constant must be large enough to turn the half wave rectified waveform into DC. It also must be large enough to average any intensity control PWM signal to DC. Typically, these PWM intensity control signals come in at a 1kHz rate (see Appendix F, "Intensity Control and Shutdown Methods"). The RC's resultant delay dominates loop transmission. It must be compensated by the capacitor at the LT1172. A large enough value for this capacitor rolls off loop gain at low enough frequency to provide stability. The loop simply does not have enough gain to oscillate at a frequency commensurate with the RC delay.²⁵

This form of compensation is simple and effective. It ensures stability over a wide range of operating conditions. It does, however, have poorly damped response at system turn-on. At turn-on the RC lag delays feedback, allowing output excursions well above the normal operating point. When the RC acquires the feedback value the loop stabilizes properly. This turn-on overshoot is not a concern if it is well within transformer breakdown ratings. Color displays, running at higher power, usually require large initial voltages. If loop damping is poor, the overshoot may be dangerously high. Figure 61 shows such a loop responding to turn-on. In this case the RC values are 10k and 4.7 μ F, with a 2 μ F compensation capacitor. Turn-on overshoot exceeds 3500V for over 10ms! Ring-off takes over 100ms before settling occurs. Additionally, an inadequate (too small) ballast capacitor and excessively lossy layout force a 2000V output once loop settling occurs. This photo was taken with a transformer rated well below this figure. The resultant arcing caused transformer destruction, resulting in field failures. A typical destroyed transformer appears in Figure 62.

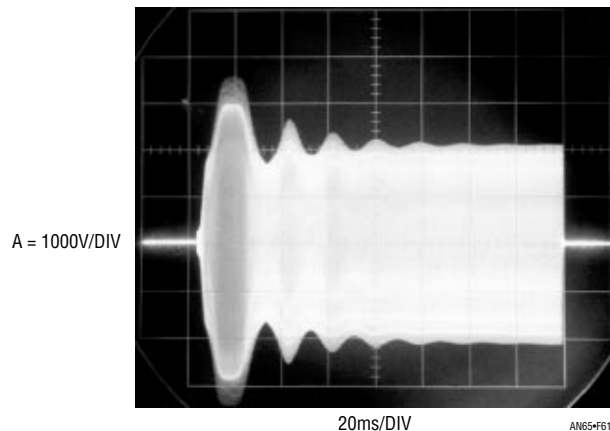


Figure 61. Destructive High Voltage Overshoot and Ring-Off Due to Poor Loop Compensation. Transformer Failure and Field Recall Are Nearly Certain. Job Loss May also Occur

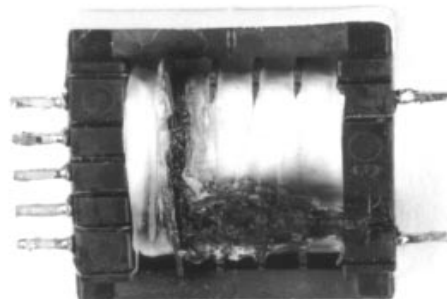


Figure 62. Poor Loop Compensation Caused This Transformer Failure. Arc Occurred in High Voltage Secondary (Lower Right). Resultant Shorted Turns Caused Overheating

Figure 63 shows the same circuit with the RC values reduced to 10k and 1 μ F. The ballast capacitor and layout have also been optimized. Figure 63 shows peak voltage reduced to 2.2kV with duration down to about 2ms (note horizontal scale change). Ring-off is also much quicker with lower amplitude excursion. Increased ballast capacitor value and wiring layout optimization reduce running voltage to 1300V. Figure 64's results are even better. Changing the compensation capacitor to a 3k Ω /2 μ F network introduces a leading response into the loop, allowing faster acquisition. Now, turn-on excursion is slightly lower, but greatly reduced in duration (again, note horizontal scale change). The running voltage remains the same.

Note 25. The high priests of feedback refer to this as "Dominant Pole Compensation." The rest of us are reduced to more pedestrian descriptives.

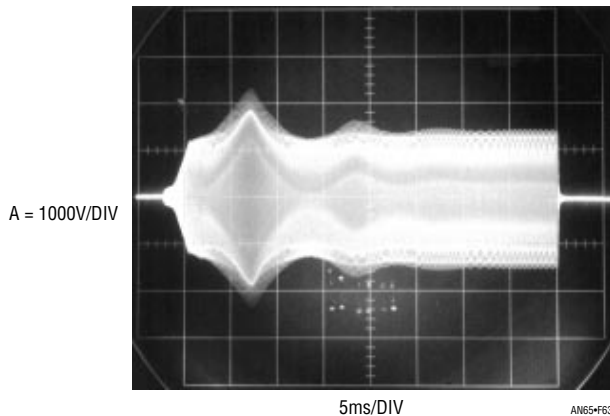


Figure 63. Reducing RC Time Constant Improves Transient Response, Although Peaking, Ring-Off and Run Voltage Are Still Excessive

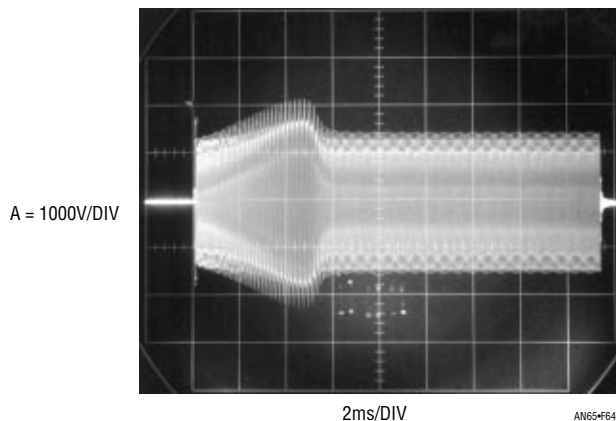


Figure 64. Additional Optimization of RC Time Constant and Compensation Capacitor Reduces Turn-On Transient. Run Voltage Is Large, Indicating Possible Lossy Layout and Display

The photos show that changes in compensation, ballast value and layout result in dramatic reductions in overshoot amplitude and duration. Figure 62's performance almost guarantees field failures while Figures 63 and 64 do not overstress the transformer. Even with the improvements, more margin is possible if display losses can be controlled. Figures 62, 63 and 64 were taken with an exceptionally lossy display. The metal enclosure was very close to the metallic foil wrapped lamp, causing large losses with subsequent high turn-on and running voltages. If the display is selected for lower losses, performance can be greatly improved.

Figure 65 shows a low loss display responding to turn-on with a $2\mu\text{F}$ compensation capacitor and $10\text{k}/1\mu\text{F}$ RC values. Trace A is the transformer's output while Traces B and C are the LT1172's $V_{\text{COMPENSATION}}$ and Feedback pins, respectively. The output overshoots and rings badly, peaking to about 3000V. This activity is reflected by overshoots at the $V_{\text{COMPENSATION}}$ pin (the LT1172's error amplifier output) and the Feedback pin. In Figure 66 the RC is reduced to $10\text{k}\Omega/0.1\mu\text{F}$. This substantially reduces loop delay. Overshoot goes down to only 800V—a reduction of almost a factor of four. Duration is also much shorter.

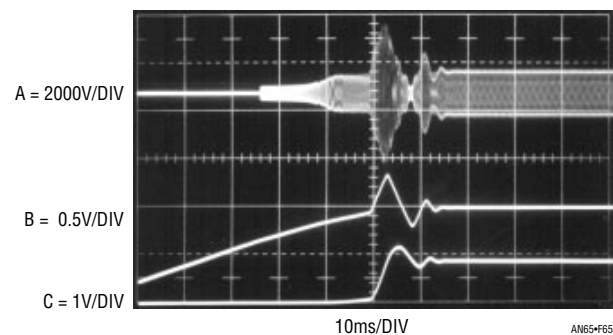


Figure 65. Waveform for a Lower Loss Layout and Display. High Voltage Overshoot (Trace A) Is Reflected at Compensation Node (Trace B) and Feedback Pin (Trace C)

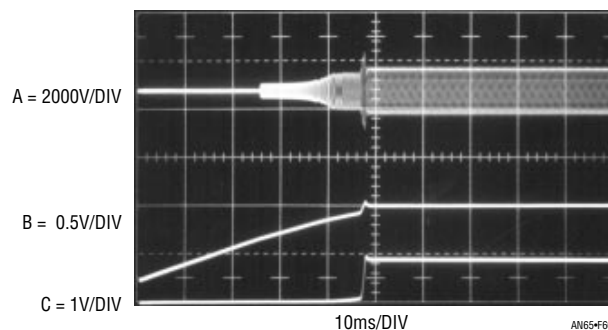


Figure 66. Reducing RC Time Constant Produces Quick, Clean Loop Behavior. Low Loss Layout and Display Result in 650V_{RMS} Running Voltage

Application Note 65

The $V_{\text{COMPENSATION}}$ and Feedback pins reflect this tighter control. Damping is much better, with slight overshoot induced at turn-on. Further reduction of the RC to $10\text{k}\Omega/0.01\mu\text{F}$ (Figure 67) results in even faster loop capture but a new problem appears. In Trace A lamp turn-on is so fast the overshoot does not register in the photo. The $V_{\text{COMPENSATION}}$ (Trace B) and feedback nodes (Trace C) reflect this with exceptionally fast response. Unfortunately, the RC's light filtering causes ripple to appear when the feedback node settles. As such, Figure 66's RC values are probably more realistic for this situation.

The lesson from this exercise is clear. The higher voltages involved in color displays mandate attention to transformer outputs. Under running conditions layout and display losses can cause higher loop compliance voltages, degrading efficiency and stressing the transformer. At turn-on improper compensation causes huge overshoots, resulting in possible transformer destruction. Isn't a day of loop and layout optimization worth a field recall?

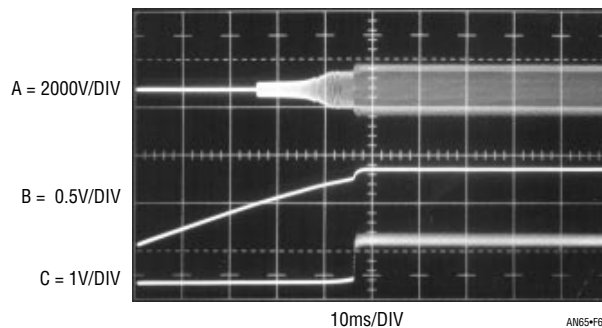


Figure 67. Very Low RC Value Provides Even Faster Response, but Ripple at Feedback Pin (Trace C) Is Too High. Figure 66 Is the Best Compromise

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Application Note 65

APPENDIX A

“HOT” CATHODE FLUORESCENT LAMPS

Many CCFL characteristics are shared by so-called “Hot” Cathode Fluorescent Lamps (HCFLs). The most significant difference is that HCFLs contain filaments at each end of the lamp (see Figure A1). When the filaments are powered they emit electrons, lowering the lamp’s ionization potential. This means a significantly lower voltage will start the lamp. Typically, the filaments are turned on, a relatively modest voltage impressed across the lamp and start-up occurs. Once the lamp starts, filament power is removed. Although HCFLs reduce the high voltage requirement they require a filament supply and sequencing circuitry. The CCFL circuits shown in the text will start and run HCFLs without using the filaments. In practice, this involves simply driving the filament connections at the HCFL ends as if they were CCFL electrodes.

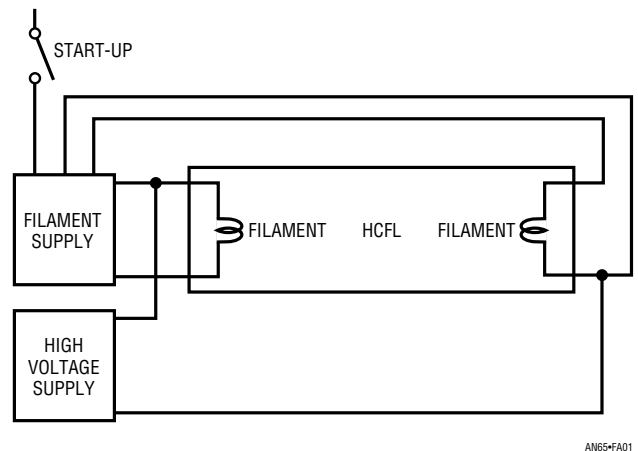


Figure A1. A Conceptual Hot Cathode Fluorescent Lamp Power Supply. Heated Filaments Liberate Electrons, Lowering the Lamp’s Start-Up Voltage Requirement. CCFL Supply Discussed in Text Eliminates Filament Supply

APPENDIX B

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MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS

Charles L. Guthrie, Sharp Electronics Corporation

Introduction

As more companies begin the manufacturing of their next generation of computers, there is a need to reduce the overall size and weight of the units to improve their portability. This has sparked the need for more compact designs where the various components are placed in closer proximity, thus making them more susceptible to interaction from signal noise and heat dissipation. The following is a summary of guidelines for the placement of the display components and suggestions for overcoming difficult design constraints associated with component placement.

In notebook computers the thickness of the display housing is important. The design usually requires the display to be in a pivotal structure so that the display may be folded down over the keyboard for transportation. Also, the outline dimensions must be minimal so that the package will remain as compact as possible. These two constraints drive the display housing design and placement of the

display components. This discussion surveys each of the problems facing the designer in detail and offers suggestions for overcoming the difficulties to provide a reliable assembly.

The problems facing the pen-based computer designer are similar to those realized in notebook designs. In addition, however, pen-based designs require protection for the face of the display. In pen-based applications, as the pen is moved across the surface of the display, the pen has the potential for scratching the front polarizer. For this reason the front of the display must be protected. Methods for protecting the display face while minimizing effects on the display image are given.

Additionally, the need to specify the flatness of the bezel is discussed. Suggestions for acceptable construction techniques for sound design are included. Further, display components likely to cause problems due to heat buildup are identified and methods for minimization of the heat’s effects are presented.

The ideas expressed here are not the only solutions to the various problems and have not been assessed as to whether they may infringe on any patents issued or applied for.

Flatness and Rigidity of the Bezel

In the notebook computer the bezel has several distinct functions. It houses the display, the inverter for the backlight, and in some instances, the controls for contrast and brightness of the display. The bezel is usually designed to tilt to set the optimum viewing angle for the display.

It is important to understand that the bezel must provide a mechanism to keep the display flat, particularly at the mounting holds. Subtle changes in flatness place uneven stress on the glass which can cause variations in contrast across the display. Slight changes in pressure may cause significant variation in the display contrast. Also, at the extreme, significantly uneven pressures can cause the display glass to fail.

Because the bezel must be functional in maintaining the flatness of the display, consideration must be made for the strength of the bezel. Care must be taken to provide structural members while minimizing the weight of the unit. This may be executed using a parallel grid, normal to the edges of the bezel, or angled about 45° off of the edges of the bezel. The angled structure may be more desirable in that it provides resistance to torquing the unit while lifting the cover with one hand. Again, the display is sensitive to stresses from uneven pressure on the display housing.

Another structure which will provide excellent rigidity, but adds more weight to the computer, is a "honeycomb" structure. This "honeycomb" structure resists torquing from all directions and tends to provide the best protection for the display.

With each of these structures it is easy to provide mounting assemblies for the display. "Blind nuts" can be molded into the housing. The mounting may be done to either the front or rear of the bezel. Attachment to the rear may provide better rigidity for placement of the mounting hardware.

One last caution is worth noting in the development of a bezel. The bezel should be engineered to absorb most of

the shock and vibration experienced in a portable computer. Even though the display has been carefully designed, the notebook computer presents extraordinary shock and abuse problems.

Avoiding Heat Buildup in the Display

Several of the display components are sources for heat problems. Thermal management must be taken into account in the design of the display bezel. A heated display may be adversely affected; a loss of contrast uniformity usually results. The Cold Cathode Fluorescent Tube (CCFT) itself gives off a small amount of heat relative to the amount of power dissipated in its glow discharge. Likewise, even though the inverters are designed to be extremely efficient, there is some heat generated. The buildup of heat in these components will be aggravated by the typically "tight" designs currently being introduced. There is little ventilation designed into most display bezels. To compound the problem, the plastics used are poor thermal conductors, thus causing the heat to build up which may affect the display.

Some current designs suffer from poor placement of the inverter and/or poor thermal management techniques. These designs can be improved even where redesign of the display housing with improved thermal management is impractical.

One of the most common mistakes in current designs is that there has been no consideration for the buildup of heat from the CCFT. Typically, the displays for notebook applications have only one CCFT to minimize display power requirements. The lamp is usually placed along the right edge of the display. Since the lamp is placed very close to the display glass, it can cause a temperature rise in the liquid crystal. It is important to note that variations in temperature of as little as 5°C can cause an apparent non-uniformity in display contrast. Variations caused by slightly higher temperature variations will cause objectionable variations in the contrast and display appearance.

To further aggravate the situation, some designs have the inverter placed in the bottom of the bezel. This has a tendency to cause the same variations in contrast, particularly when the housing does not have any heat sinking for the inverter. This problem manifests itself as a "blooming" of the display, just above the inverter. This "blooming"

Application Note 65

looks like a washed out area where, in the worst case, the characters on the display fade completely.

The following section discusses the recommended methods for overcoming these design problems.

Placement of the Display Components

One of the things that can be done is to design the inverter into the base of the computer with the motherboard. In some applications this is impractical because this requires the high voltage leads to be mounted within the hinges connecting the display bezel to the main body. This causes a problem with strain relief of the high voltage leads and thus with UL certification.

One mistake made most often is placing the inverter at the bottom of the bezel next to the lower edge of the display. It is a fact that heat rises, yet this is one of the most overlooked problems in new notebook designs. Even though the inverters are very efficient, some energy is lost in the inverter in the form of heat. Because of the insulating properties of the plastic materials used in the bezel construction, heat builds up and affects the display contrast.

Designs with the inverter at the bottom can be improved in one of three ways. The inverter can be relocated away from the display, heat sinking materials can be placed between the display and the inverter, or ventilation can be provided to remove the heat.

In mature designs it may be impractical to do what is obvious and move the inverter up to the side of the display towards the top of the housing. In these cases the inverter may be insulated from the display with a "heat dam." One method of accomplishing this would be to use a piece of mica insulator die cut to fit tightly between the inverter and the display. This heat dam would divert the heat around the end of the display bezel to rise harmlessly to the top of the housing. Mica is recommended in this application because of its thermal and electrical insulation properties.

The last suggestion for removing heat is to provide some ventilation to the inverter area. This has to be done very carefully to prevent exposing the high voltage. Ventilation may not be a practical solution because resistance to liquids and dust is compromised.

The best solution for the designer of new hardware is to consider the placement of the inverter to the side of the display and at the top of the bezel. In existing designs of this type the effects of heat from the inverter, even in tight housings, has been minimal or nonexistent.

One problem which is aggravated by the placement of the inverter at the bezel is heat dissipated by the CCFT. In designs where the inverter is placed up and to the side of the display, fading of the display contrast due to CCFT heat is not a problem. However, when the inverter is placed at the bezel bottom, some designs experience a loss of contrast aggravated by the heat from the CCFT and inverter.

In cases where the inverter must be left at the bottom, and the CCFT is causing a loss of contrast, the problem can be minimized by using an aluminum foil heat sink. This does not remove the heat from the display but dissipates it over the entire display area, thus normalizing the display contrast. The aluminum foil is easy to install and in some present designs has successfully improved the display contrast.

Remember that the objection to the contrast variation stems more from nonuniformity than from a total loss of contrast.

Protecting the Face of the Display

One of the last considerations in the design of notebook and pen-based computers is protection of the display face. The front polarizer is made of a mylar base and thus is susceptible to scratching. The front protection for the display, along with providing scratch protection, may also provide an antiglare surface.

There are several ways that scratch resistance and antiglare surfaces can be incorporated. A glass or plastic cover may be placed over the display, thus providing protection. The material should be placed as close to the display as possible to minimize possible parallax problems due to reflections off of the cover material. With antiglare materials the further the material is from the front of the display the greater the distortion.

In pen applications, the front antiscratch material is best placed in contact with the front glass of the display. The cover glass material normally needs to be slightly thicker

to protect the display from distortion when pressure is being exerted on the front.

There are several methods for making the pen input devices. Some use the front surface of the cover glass to provide input data and some use a field effect to a printed wiring board on the back of the display. When the pen input is on the front of the display, the input device is usually on a glass surface.

To limit specular reflection in this application, the front cover glass should be bonded to the display. Care must be taken to ensure that the coefficient of thermal expansion is matched for all of the materials used in the system. Because of the difficulties encountered with the bonding of the cover glass, and the potential to destroy the display through improper workmanship, consulting an expert is strongly recommended.

APPENDIX C

ACHIEVING MEANINGFUL ELECTRICAL MEASUREMENTS

Obtaining reliable efficiency data for the CCFL circuits presents a high order difficulty measurement problem. The accuracy required in the high frequency AC measurements is uncomfortably close to the state-of-the-art. Establishing and maintaining accurate wideband AC measurements is a textbook example of attention to measurement technique. The combination of high frequency, harmonic laden waveforms and high voltage makes meaningful results difficult to obtain. The choice, understanding and use of test instrumentation is crucial. Clear thinking is needed to avoid unpleasant surprises!¹

The lamp's current and voltage waveforms contain energy content over a wide frequency range. Most of this energy is concentrated at the inverter's fundamental frequency and immediate harmonics. However, if 1% measurement uncertainty is desirable, then energy content out to 10MHz must be accurately captured. Figure C1, a spectrum analysis of lamp current, shows significant energy out to 500kHz. Diminished, but still significant, content shows

Note 1: It is worth considering that various constructors of text Figure 35 have reported efficiencies ranging from 8% to 115%.

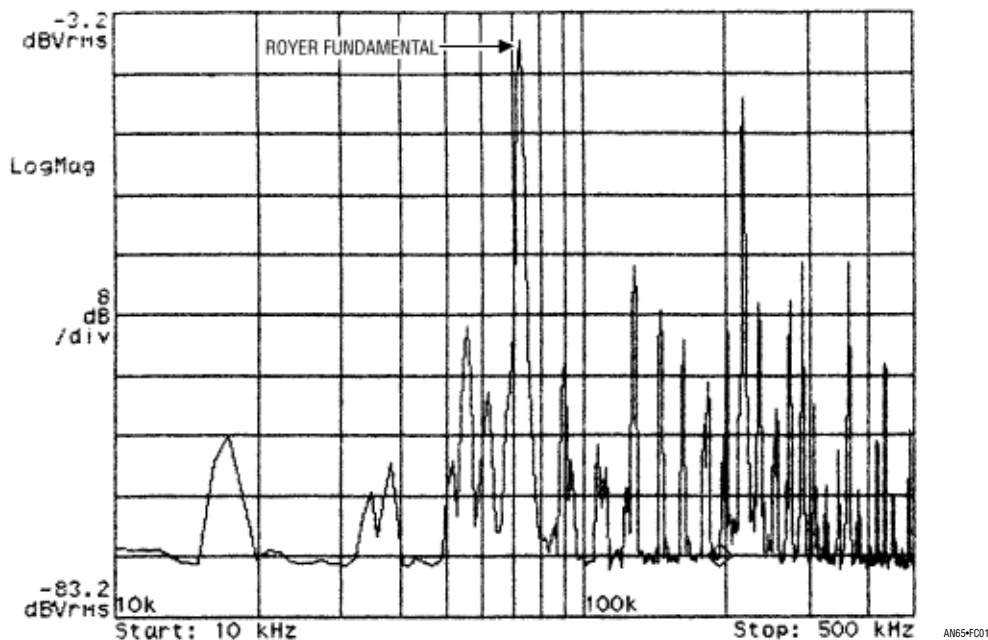


Figure C1. Hewlett-Packard HP89410A Spectral Plot of Lamp Current Shows Significant Energy Out to 500kHz

Application Note 65

up in Figure C2's 6MHz wide plot. This data suggests that monitoring instrumentation must maintain high accuracy over wide bandwidth.

Accurate determination of RMS operating current is important for electrical and emissivity efficiency computations and to ensure long lamp life. Additionally, it is desirable to be able to perform current measurements in the presence of high common mode voltage ($> 1000V_{RMS}$). This capability allows investigation and quantification of display and wiring-induced losses, regardless of their origins in the lamp drive circuitry.

Current Probe Circuitry

Figure C3's circuitry meets the discussed requirements. It signal-conditions a commercially available "clip-on" current probe with a precision amplifier to provide 1% measurement accuracy to 10MHz. The "clip-on" probe provides convenience, even in the presence of the high common voltages noted. The current probe biases A1, operating at a gain of about 3.75. No impedance matching is required due to the probe's low output impedance termination. Additional amplifiers provide distributed gain, maintaining wide bandwidth with an overall gain of about

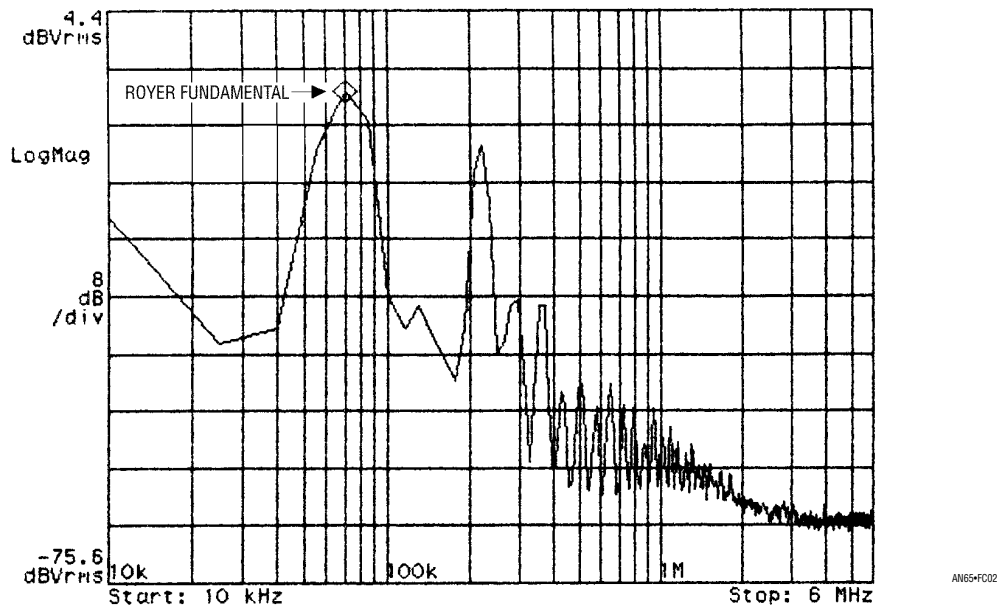


Figure C2. Extended HP89410A Spectral Plot Shows Lamp Current Has Measurable Energy Well into MHz Range. Data Indicates that Lamp Voltage and Current Instrumentation Must Have Precision, Wideband Response

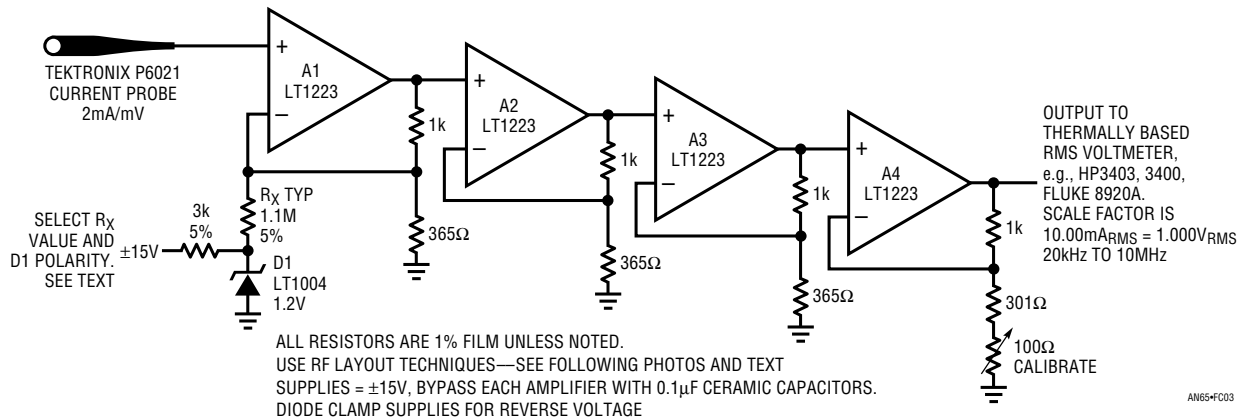


Figure C3. Precision "Clip-On" Current Probe for CCFL Measurements Maintains 1% Accuracy over 20kHz to 10MHz Bandwidth

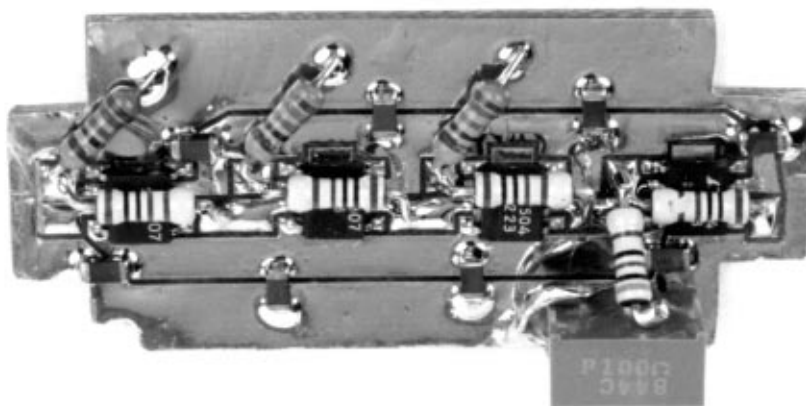
200. The individual amplifiers avoid any possible crosstalk-based error that could be introduced by a monolithic quad amplifier. D1 and R_x are selected for polarity and value to trim overall amplifier offset. The 100Ω trimmer sets gain, fixing the scale factor. The output drives a thermally

based, wideband RMS voltmeter. In practice, the circuit is built into a $2.25" \times 1" \times 1"$ enclosure which is *directly* connected via BNC hardware to the voltmeter. No cable is used. Figure C4 shows the probe/amplifier combination. Figure C5 details RF layout techniques used in the amplifier's



AN65-FC04

Figure C4. Current Probe Amplifier Mated to the Current Probe Termination Box



AN65-FC05

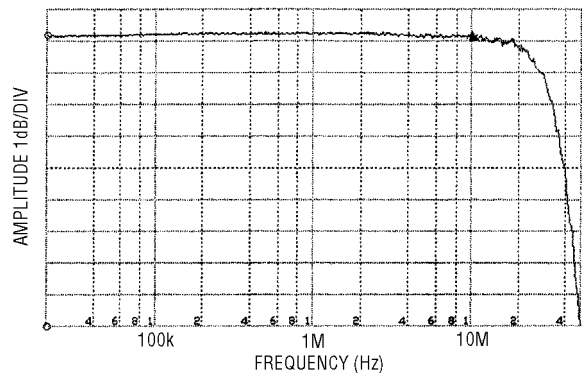
Figure C5. RF Layout Technique for the Current Probe Amplifier Is Required for Performance Levels Quoted in Text



AN65-FC06

Figure C6. A Version of the Current Probe Amplifier in Its Housing. Current Probe Terminator Is at Left

construction. Figure C6 shows a version of the amplifier, detailing enclosure layout and construction. The result is a “clip-on” current probe with 1% accuracy over a 20kHz to 10MHz bandwidth. This tool has proven to be indispensable to any rigorously conducted backlight work. Figure C7 shows response for the probe/amplifier as measured on a Hewlett-Packard HP4195A network analyzer.



AN65-FC07

Figure C7. Amplitude vs Frequency Output of HP4195A Network Analyzer. Current Probe/Amplifier Maintains 1% (0.1dB) Error Bandwidth from 20kHz to 10MHz. Small Aberrations Between 10MHz and 20MHz Are Test Fixture Related

Current Calibrator

Figure C8's circuit, a current calibrator, permits calibration of the probe/amplifier and can be used to periodically check probe accuracy. A1 and A2 form a Wein bridge oscillator. Oscillator output is rectified by A4 and A5 and compared to a DC reference at A3. A3's output controls Q1, closing an amplitude stabilization loop. The stabilized amplitude is terminated into a 100Ω, 0.1% resistor to provide a precise 10.00mA, 60kHz current through the series current loop. Trimming is performed by altering the nominal 15k resistor for exactly 1.000V_{RMS} across the 100Ω unit.

In use, this current probe has shown 0.2% baseline stability with 1% absolute accuracy over one year's time. The sole maintenance requirement for preserving accuracy is to keep the current probe jaws clean and avoid rough or abrupt handling of the probe.² Figure C9a shows the probe/calibrator used with an RMS voltmeter. Figure C9b shows the current probe in use, in this case determining display frame parasitic loss.

Note 2: Private communication, Tektronix, Inc.

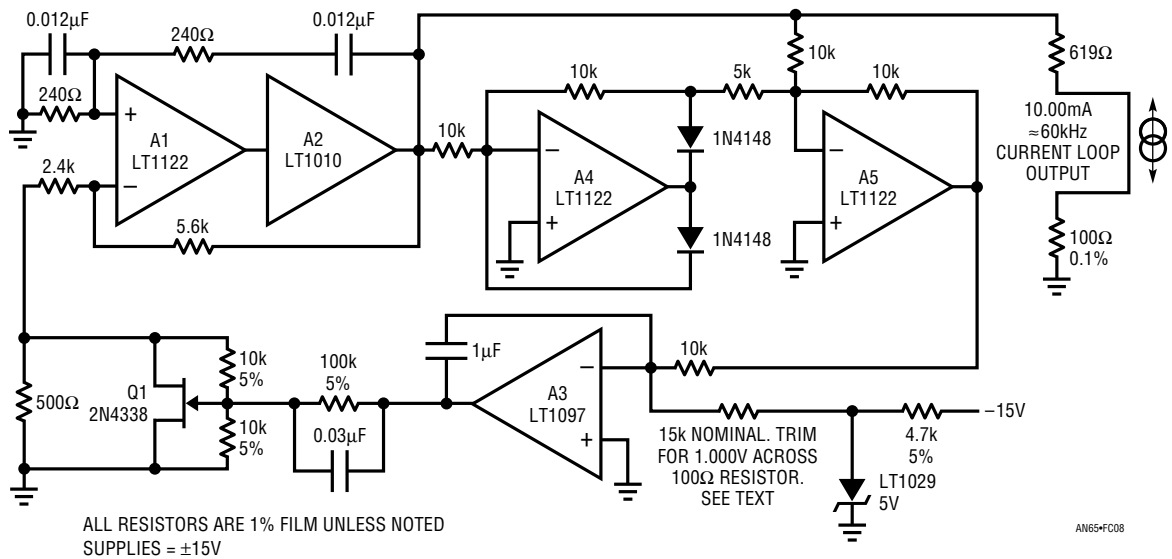


Figure C8. Current Calibrator for Probe Trimming and Accuracy Checks. Stabilized Oscillator Forces 10.00mA Through Output Current Loop at 60kHz



ANSI-C028A

Figure C9a. Complete Current Probe Test Set Includes Probe, Amplifier, Calibrator and Thermally Based RMS Voltmeter. Accuracy Is 1% to 10MHz



AN65-FC09b

Figure C9b. Current Probe Measuring Display Frame Parasitic Current. "Clip-On" Capability Allows Measurement at Any Point in Lamp Circuit

Application Note 65

Voltage Probes for Grounded Lamp Circuits

The high voltage measurement across the lamp is quite demanding on the probe. The simplest case is measuring grounded lamp circuits. The waveform fundamental is at 20kHz to 100kHz, with harmonics into the MHz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects which would corrupt the measurement. The design and construction of such a probe requires significant attention. Figure C10 lists some recommended probes along with their characteristics. As stated in the text, almost all standard oscilloscope probes *will fail*³ if used for this measurement. Attempting to circumvent the probe requirement by resistively dividing the lamp voltage also creates problems. Large value resistors often have significant voltage coefficients and their shunt capacitance is high and uncertain. As such, simple voltage dividing is not recommended. Similarly, common high voltage probes intended for DC measurement will have large errors because of AC effects. The P6013A and P6015 are the favored probes; their 100MΩ input and small capacitance introduces low loading error.

The penalty for their 1000X attenuation is reduced output, but the recommended voltmeters (discussion to follow) can accommodate this.

All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1MΩ paralleled by (typically) 10pF to 22pF. The recommended voltmeters, which will be discussed, have significantly different input characteristics. Figure C11's table shows higher input resistances and a range of capacitances. Because of this the probe must be compensated for the voltmeter's input characteristics. Normally, the optimum compensation point is easily determined and adjusted by observing probe output on an oscilloscope. A known amplitude square wave is fed in (usually from the oscilloscope calibrator) and the probe adjusted for correct response. Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct.

The impedance mismatch occurs at low and high frequency. The low frequency term is corrected by placing an appropriate value resistor in shunt with the probe's output.

Note 3: That's twice we've warned you nicely.

TEKTRONIX PROBE TYPE	ATTENUATION FACTOR	ACCURACY	INPUT RESISTANCE	INPUT CAPACITANCE	RISE TIME	BANDWIDTH	MAXIMUM VOLTAGE	DERATED ABOVE	DERATED TO AT FREQUENCY	COMPENSATION RANGE	ASSUMED TERMINATION RESISTANCE
P6007	100X	3%	10M	2.2pF	14ns	25MHz	1.5kV	200kHz	700V _{RMS} at 10MHz	15pF to 55pF	1M
P6009	100X	3%	10M	2.5pF	2.9ns	120MHz	1.5kV	200kHz	450V _{RMS} at 40MHz	15pF to 47pF	1M
P6013A	1000X	Adjustable	100M	3pF	7ns	50MHz	12kV	100kHz	800V _{RMS} at 20MHz	12pF to 60pF	1M
P6015	1000X	Adjustable	100M	3pF	4.7ns	75MHz	20kV	100kHz	2000V _{RMS} at 20MHz	12pF to 47pF	1M

Figure C10. Characteristics of Some Wideband High Voltage Probes. Output Impedances Are Designed for Oscilloscope Inputs

MANUFACTURER AND MODEL	FULL SCALE RANGES	ACCURACY AT 1MHz	ACCURACY AT 100kHz	INPUT RESISTANCE AND CAPACITANCE	MAXIMUM BANDWIDTH	CREST FACTOR
Hewlett-Packard 3400 Meter Display	1mV to 300V, 12 Ranges	1%	1%	0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF	10MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Hewlett-Packard 3403C Digital Display	10mV to 1000V, 6 Ranges	0.5%	0.2%	10mV and 100mV Range = 20M and 20pF ±10%, 1V to 1000V Range = 10M and 24pF ±10%	100MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Fluke 8920A Digital Display	2mV to 700V, 7 Ranges	0.7%	0.5%	10M and < 30pF	20MHz	7:1 At Full Scale, 70:1 At 0.1 Scale

Figure C11. Pertinent Characteristics of Some Thermally Based RMS Voltmeters. Input Impedances Necessitate Matching Network and Compensation for High Voltage Probes

For a $10\text{M}\Omega$ voltmeter input a 1.1M resistor is suitable. This resistor should be built into the smallest possible BNC equipped enclosure to maintain a coaxial environment. No cable connections should be employed; the enclosure should be placed *directly* between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low frequency impedance mismatch. Figure C12 shows the impedance matching box attached to the high voltage probe.

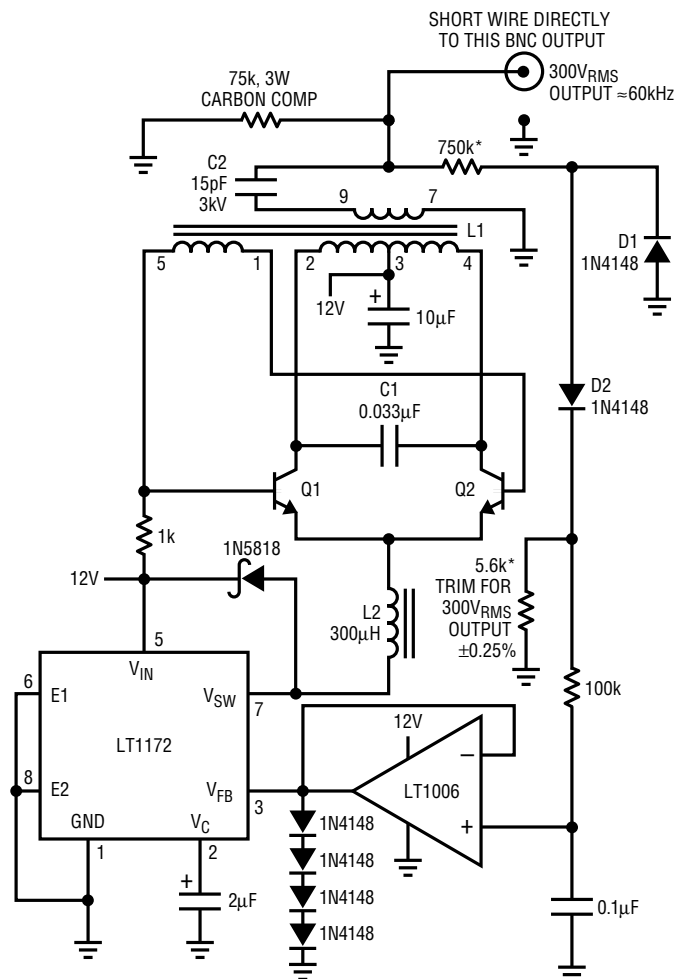
Correcting the high frequency mismatch term is more involved. The wide range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. How is the experimenter to know where to set the high frequency probe compensation adjustment? One solution is to feed a known value RMS signal to the probe/voltmeter combination and adjust compensation for a proper reading. Figure C13 shows a way to generate a known RMS voltage. This scheme is simply a standard backlight circuit reconfigured for a constant voltage output. The op amp permits low RC loading of the $5.6\text{k}\Omega$ feedback termination without introducing bias current error. The $5.6\text{k}\Omega$ value may be series or parallel trimmed for a 300V_{RMS} output. Stray parasitic capacitance in the feedback network affects output voltage. Because of this, all feedback associated nodes and components should be rigidly fixed and the entire circuit built into a small metal box. This prevents any significant change in the parasitic terms. The result is a known 300V_{RMS} output.

Now, the probe's compensation is adjusted for a 300V voltmeter indication using the shortest possible connection (e.g., BNC-to-probe adapter) to the calibrator box. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If the probe compensation is altered (e.g., for proper response on an oscilloscope) the voltmeter's reading will be erroneous.⁴ It is good practice to verify the calibrator box output before and after every set of efficiency measurements. This is done by *directly* connecting, via BNC adapters, the calibrator box to the RMS voltmeter on the 1000V range.

Note 4: The translation of this statement is to hide the probe when you are not using it. If anyone wants to borrow it, look straight at them, shrug your shoulders and say you don't know where it is. This is decidedly dishonest, but eminently practical. Those finding this morally questionable may wish to re-examine their attitude after producing a day's worth of worthless data with a probe that was unknowingly readjusted.



Figure C12. The Impedance Matching Box (Extreme Left) Mated to the High Voltage Probe. Note Direct Connection. No Cable Is Used



- C1 = MUST BE A LOW LOSS CAPACITOR. METALIZED POLYCARB WIMA FKP2, MKP-20 (GERMAN) OR PANASONIC ECH-U RECOMMENDED
- L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1 PIN NUMBERS SHOWN FOR COILTRONICS UNIT
- L2 = COILTRONICS CTX300-4
- Q1, Q2 = ZETEX ZTX849 OR ZDT1048
- * = 1% FILM RESISTOR (TEN 75k RESISTORS IN SERIES)

DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (407) 241-7876, SUMIDA (708) 956-0666

AN65-FC13

Figure C13. High Voltage RMS Calibrator Is Voltage Output Version of CCFL Circuit

Application Note 65

Voltage Probes for Floating Lamp Circuits

Measuring voltage of floating lamp circuits requires a nearly heroic effort. Floating lamp measurement involves all the difficulties of the grounded case but also needs a fully differential input. This is so because the lamp is freely floating from ground. The two probes must not only be properly compensated but matched and calibrated within 1%. Additionally, a fully floating source is required to check calibration instead of Figure C13's simple single-ended approach.

Figure C14's differential amplifier converts the differential output of the high voltage probes to a single-ended signal for driving an RMS voltmeter. It introduces less than 1% error in 10MHz bandwidth if probe compensation and calibration are correct (discussion to follow). Both probe inputs feed source followers (Q1-Q4) via RC networks that provide proper probe termination. Q2 and Q4 bias differential amplifier A2, running at a gain of ≈ 2 . FET DC and low frequency differential drift is controlled by A1. A1 measures a band limited version of A2's inputs and biases Q4's gate termination resistor. This forces Q4 and Q2 to equal source voltages. This control loop eliminates DC and low

frequency error due to FET mismatches.⁵ Q1 and Q3 also follow the probe output and feed a small, frequency-dependent, summed signal to A2's auxiliary input. This term is used to correct high frequency common mode rejection limitations of A2's main inputs. A2's output drives the RMS voltmeter via a 20:1 divider. The divider combines with A2's gain-bandwidth characteristics to give 1% accuracy out to 10MHz at the voltmeter input.

To calibrate the amplifier, tie both inputs together and select R_X (shown at Q4) so A1's output is near 0V. It may be necessary to place R_X at Q2 to make this trim. Next, drive the shorted inputs with a 1V, 10MHz sine wave. Adjust the "10MHz CMRR trim" for a minimum RMS voltmeter reading, which should be below 1mV. Finally, lift the "+" input from ground, apply 1V_{RMS} at 60kHz and set A2's gain trim for a 100mV voltmeter reading. As a check, grounding the "+" input and driving the "-" input with the 60kHz signal should produce an identical meter reading.

Note 5: A more obvious and less complex way to control FET mismatch-induced offset would utilize a matched dual monolithic FET. Readers are invited to speculate on why this approach has unacceptable high frequency error.

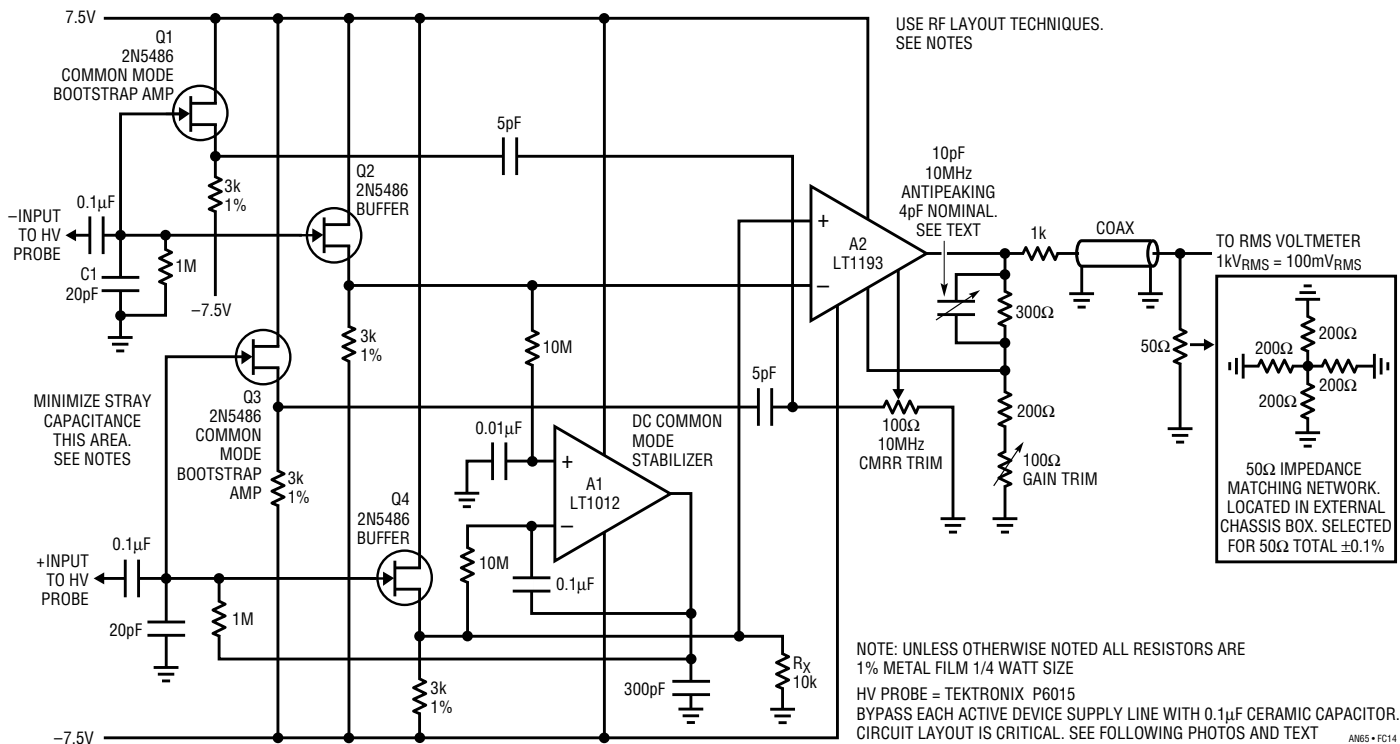


Figure C14. Precision Wideband Differential Probe Amplifier Permits Floating Lamp Voltage Measurement. Source Followers Combine with Impedance Matching Networks to Unload Probes. A2 Provides Differential-to-Single-Ended Transition

Further, known differential inputs at any frequency from 10kHz to 10MHz should produce corresponding calibrated and stable RMS voltmeter readings within 1%. Errors outside this figure at the highest frequencies are correctable by adjusting the “10MHz antipeaking” trim. This completes amplifier calibration.

The high voltage probes must be properly frequency-compensated to give calibrated results with the amplifier. The RC values at the amplifier inputs approximate the termination impedance the probe is designed for. Individual probes must, however, be precisely frequency-compensated to achieve required accuracy. This is quite a demanding exercise because of probe characteristics.

Figure C15 is an approximate schematic of the Tektronix P6015 high voltage probe. A physically large, 100M resistor occupies the probe head. Although the resistor has repeatable wideband characteristics, it suffers distributed parasitic capacitances. These distributed capacitances combine with similar cable losses, presenting a distorted version of the probed waveform to the terminator box. The terminator box impedance-frequency characteristic, when properly adjusted, corrects the distorted information, presenting the proper waveform at the output. The probe’s 1000X attenuation factor, combined with its high impedance, provides a safe, minimally invasive measure of the input waveform.

The large number of parasitic terms associated with the probe head and cable result in a complex, multitime-constant response characteristic. Faithful wideband response requires the terminator box components to separately compensate each of these time constants. As such, no less than seven user adjustments are required to compensate the probe to any individual instrument input. These trims are interactive, requiring a repetitive sequence before the probe is fully compensated. The probe manual describes the trimming sequence, using the intended oscilloscope display as the output. In the present case the ultimate output is an RMS voltmeter via the differential amplifier just described. This complicates determining the probe’s proper compensation point but can be accommodated.

To compensate the probes, connect them *directly* to the calibrated differential amplifier (see Figures C16, C17, C18) and ground the probe associated with the “-” input. Drive the “+” input probe with a 100V, 100kHz square wave that has a clean 10ns edge with minimal aberrations following the transition.⁶ The absolute amplitude of the waveform is unimportant. Monitor this waveform⁷ on an oscilloscope. Additionally, monitor A2’s output in the

Note 6: Suitable instruments include the Hewlett-Packard 214A and the Tektronix type 106 pulse generators.

Note 7: Use a properly compensated probe, please!

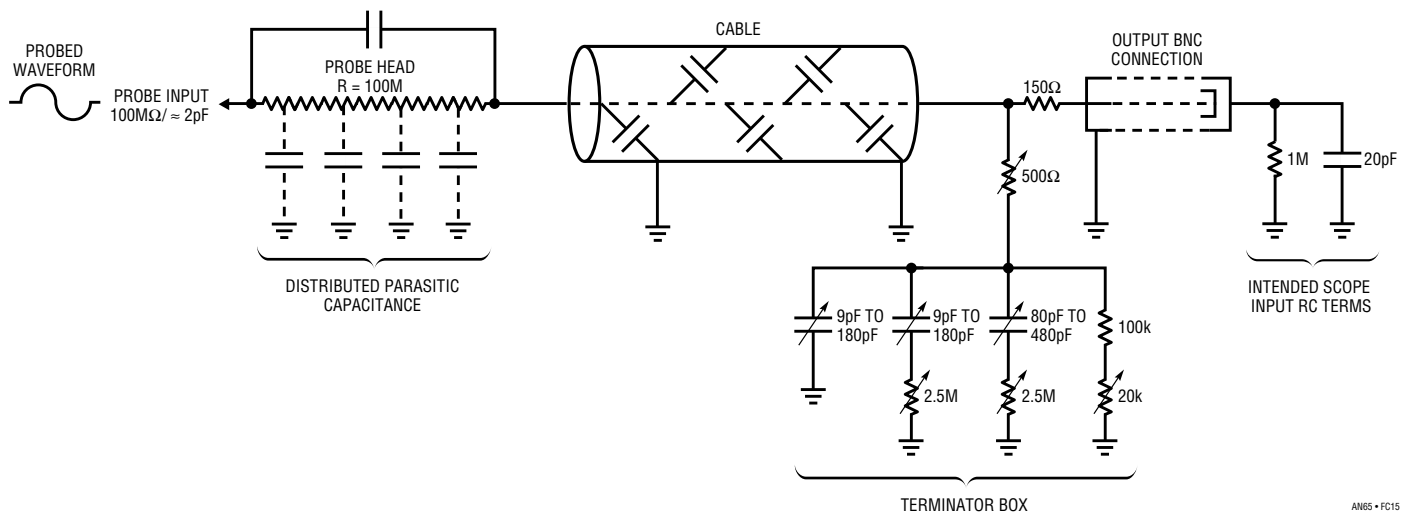


Figure C15. Approximate Schematic of Tektronix P6015 High Voltage Probe. Distributed Parasitic Capacitances Necessitate Numerous Interactive Trims, Complicating Probe Matching to Voltmeter



AN65-FC16

Figure C16. Complete Differential Probe and Calibrator. BNC Outputs Provide Precision, Floating 500V_{RMS} Calibration Source to Check Probe/Amplifier Section

differential amplifier (see Figure C14) with the oscilloscope.⁸ Perform the compensation procedure described in the Tektronix P6015 manual until both waveforms displayed on the oscilloscope have identical shapes. When this state is reached, repeat this procedure with the “-” input probe driven and the “+” input probe grounded. This sequence brings the probe’s interactive adjustments reasonably close to the optimum points.

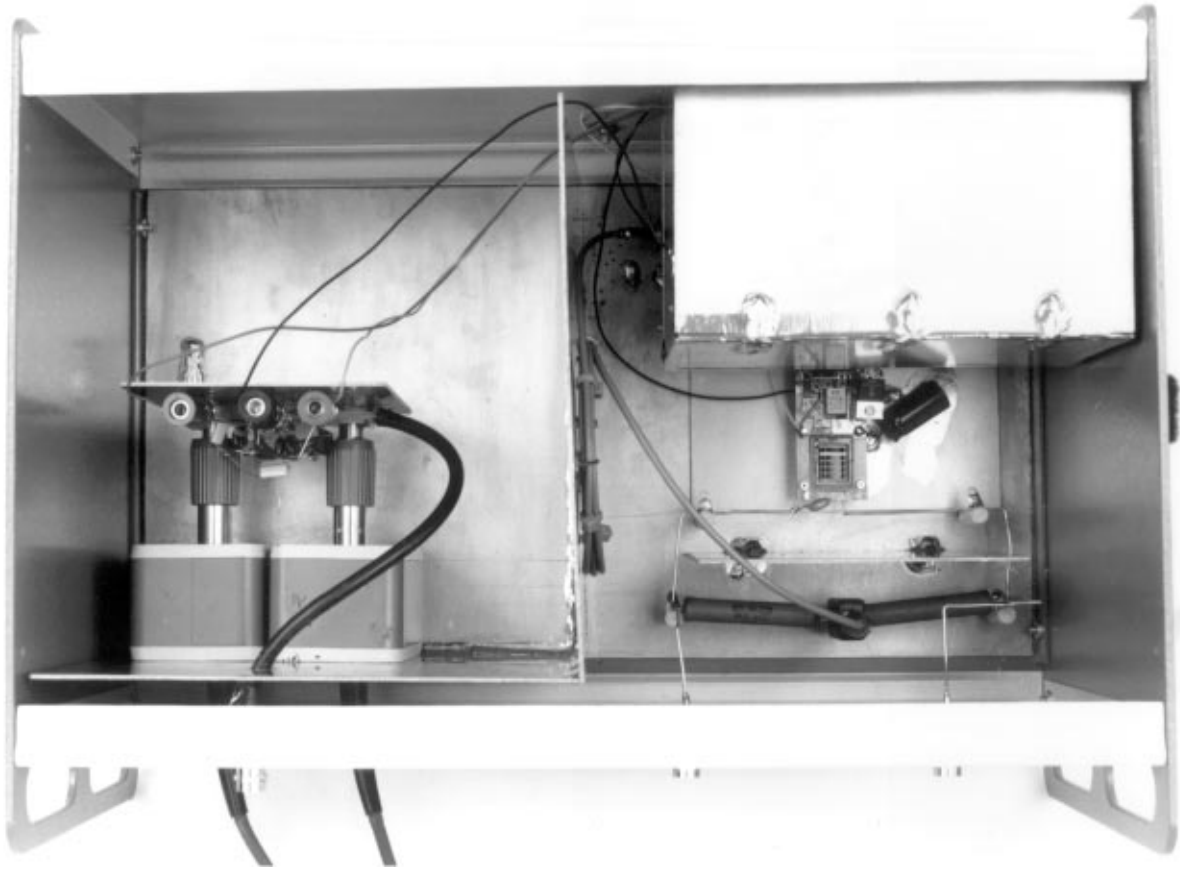
To complete the calibration, connect the 50Ω precision termination (see Figures C14 and C16) and the RMS voltmeter to the differential amplifier’s output (see Figure C16). Ground the “-” input probe and drive the “+” probe with a known amplitude high voltage waveform of about 60kHz.⁹

Perform *very slight* readjustments of this probe’s compensation trims to get the voltmeter’s reading to agree with the calibrated input (account for scaling differences—e.g., ignore the voltmeter’s range and decimal point indications). The trim(s) having the greatest influence should be utilized for this adjustment—only a slight adjustment should be required. Upon completing this step repeat the procedure using the 100V, 100kHz square wave, verifying input/output waveform edge fidelity. If waveform fidelity has been lost retrim and try again. Several iterations may be necessary until both conditions are met.

Repeat the above procedure for the “-” probe adjustment with the “+” probe grounded.

Note 8: See Footnote 7.

Note 9: Figure C13’s calibrator is appropriate.



AN65-FC17

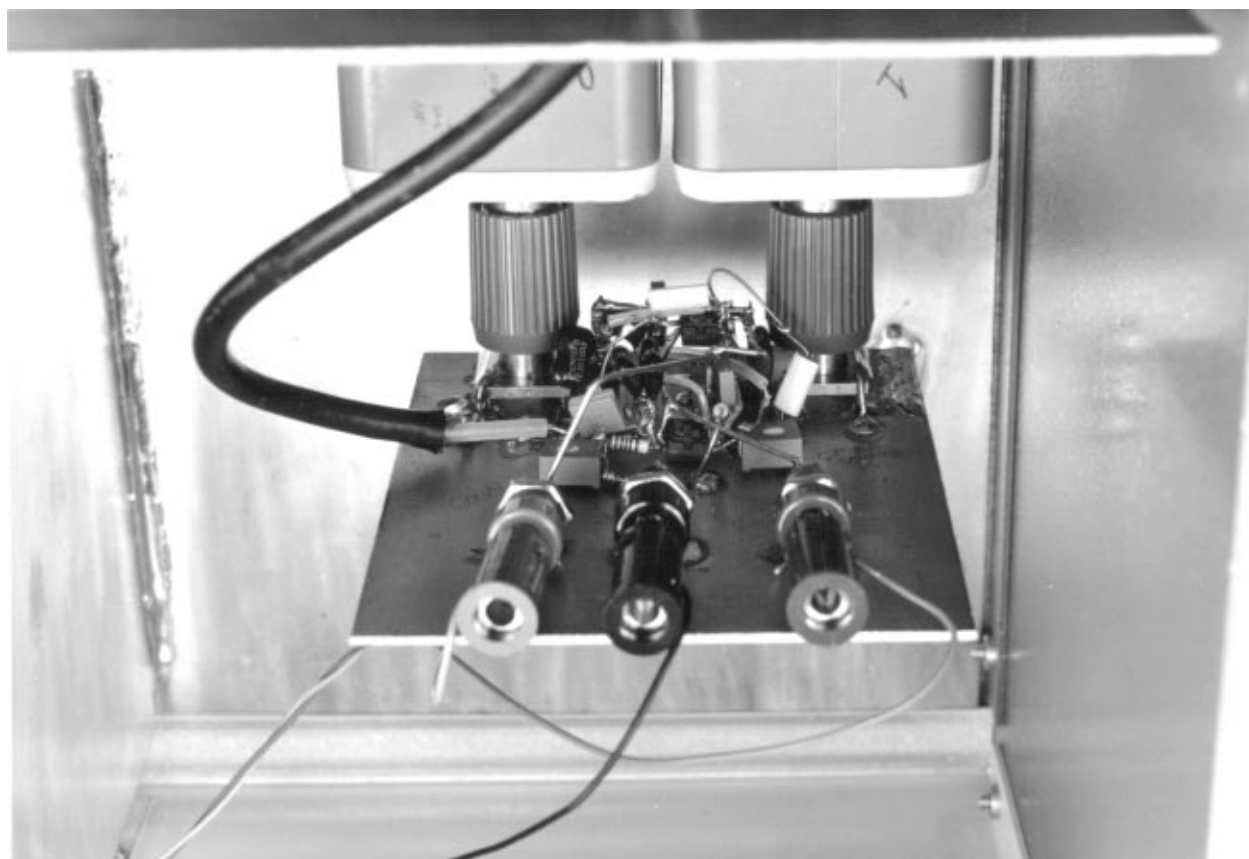
Figure C17. Top View of Differential Probe/Calibrator. Probes Are Directly Mated to Differential Amplifier (Left). Calibrator Is to Right. Current Transformer Is Located Between Load Resistors

Short both probes together and drive them with the 100V, 100kHz square wave. The RMS voltmeter should read (ideally) zero. Typically, it should indicate well below 1% of input. The differential amplifier's "10MHz CMRR trim" (Figure C14) can be adjusted to minimize the voltmeter reading.

Next, with the probes still shorted, apply a swept 20kHz to 10MHz sine wave with the highest amplitude available. Monitor A2's output with an RMS voltmeter, ensuring that it never rises above 1% of input amplitude. Finally,¹⁰ apply the highest available known amplitude, swept 20kHz

to 10MHz signal to each probe with the other probe grounded. Verify that the RMS voltmeter indicates correct and flat gain over the entire swept frequency range for each case. If any condition described in this paragraph is not met, the entire calibration sequence must be repeated. This completes the calibration.

Note 10: "Finally" is more than an appropriate descriptive. Achieving a wideband, matched probe response involving 14 interactive adjustments takes time, patience and utter determination. Allow at least six hours for the entire session. You'll need it.



AN65#C18

Figure C18. Detail of Probe/Amplifier Connection Shows Direct, Low Loss BNC Coupling

Differential Probe Calibrator

A calibrator with a fully floating, differential output allows periodic operational checking of the differential probe's accuracy. This calibrator is built into the same enclosure as the differential probe (Figure C16). Figure C19 is a schematic of the calibrator.

The circuit is a highly modified form of the basic backlight power supply. Here, T1's output drives two precision resistors which are well-specified for high frequency, high voltage operation. The resistor's current is monitored by L2, a wideband current transformer. L2's placement between the resistors combines with T1's floating drive to minimize the effects of L2's parasitic capacitance. Although L2 has parasitic capacitance, it is bootstrapped to essentially 0V, negating its effect.

L2's secondary output is amplified by A1 and A2, with A3 and A4 serving as a precision rectifier. A4's output is smoothed by the $10\text{k}\Omega/0.1\mu\text{F}$ filter, closing a loop at the LT1172's Feedback pin. Similar to previously described CCFL circuits, the LT1172 controls Royer drive, setting T1's output.

To calibrate this circuit, ground the LT1172's V_C pin, open T1's secondary and select the LT1004's polarity and associated resistor value for 0V at A4's output. Next, put a 5.00mA, 60kHz current through L2.¹¹ Measure A4's smoothed output (the LT1172's Feedback pin) and adjust the "output trim" for 1.23V. Next, reconnect T2's secondary, remove the current calibrator connection and unground

Note 11: Figure C8's output, rescaled for 5.00mA, is a source of calibrated current.

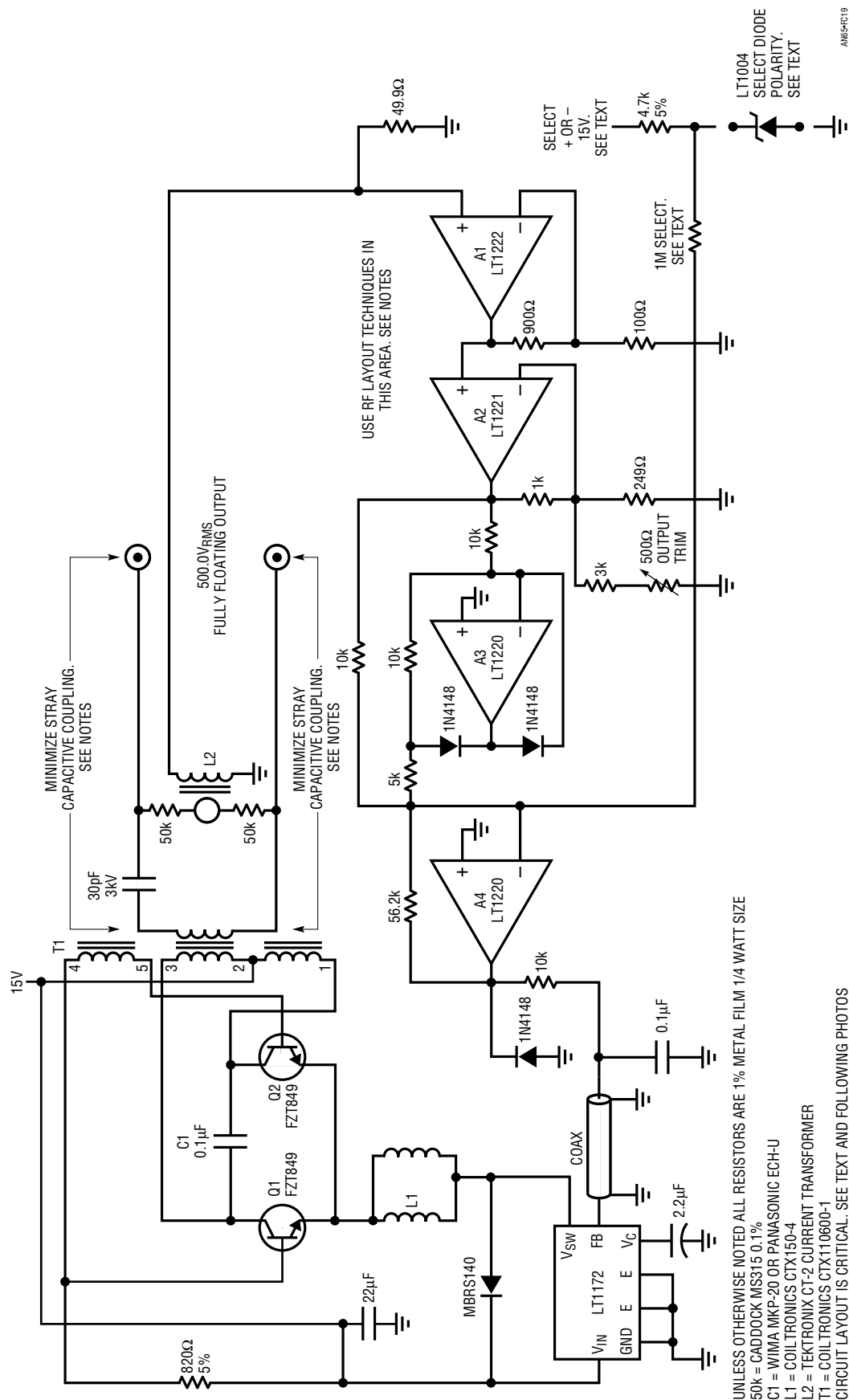


Figure C19. The Floating Output Calibrator. Current Transformer Permits Floating Output while Maintaining Tight Loop Control. Amplifiers Provide Gain to Inverter Circuit's Feedback Node

Application Note 65

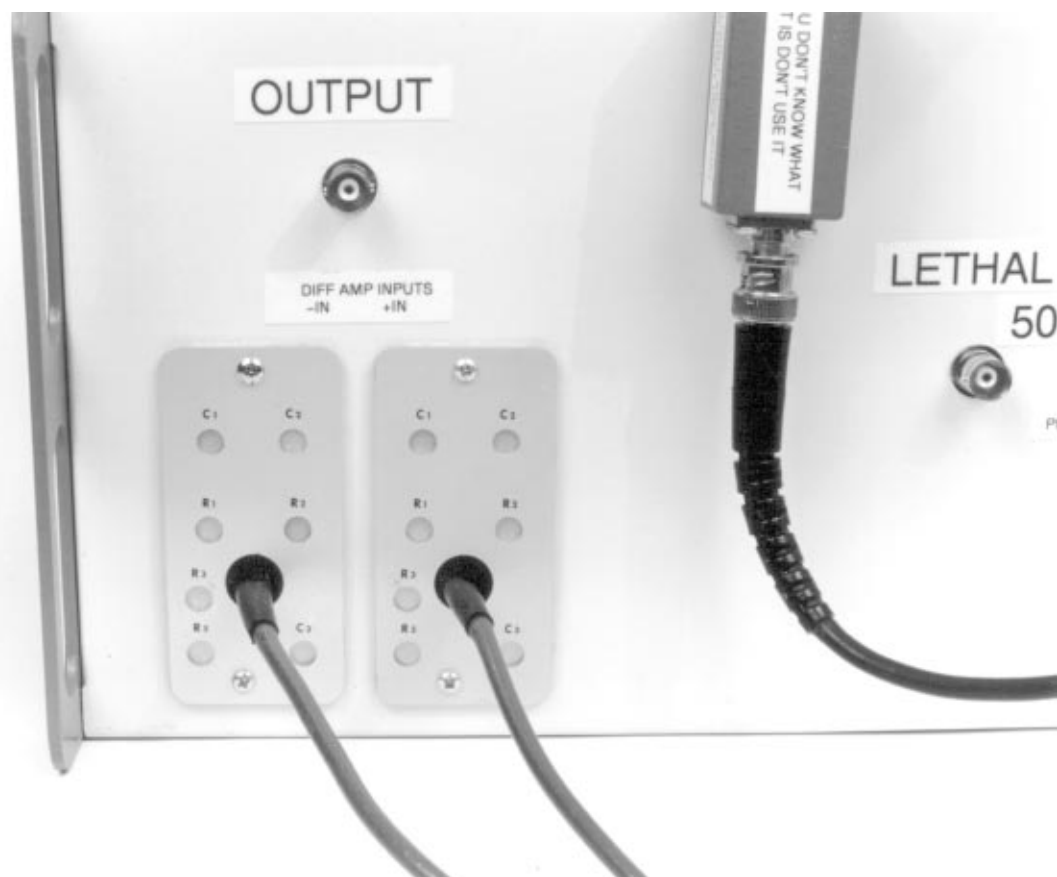
the LT1172 V_C pin. The result is $500V_{RMS}$ at the calibrator's differential output. This may be checked with the differential probe. Reversing the probe connections should have no effect, with readings well within 1%.¹²

The differential probe and floating output calibrator require almost fanatical attention to layout to achieve the performance levels noted. The wideband amplifier sections utilize RF layout techniques which are reasonably

well-documented.¹³ Practical construction considerations for parasitic capacitance related issues are photographically detailed in Figures C17 through C23.

Note 12: Those who construct and trim the differential probe and calibrator will experience the unmitigated joy that breaks loose when they agree within 1%.

Note 13: See Reference 26.



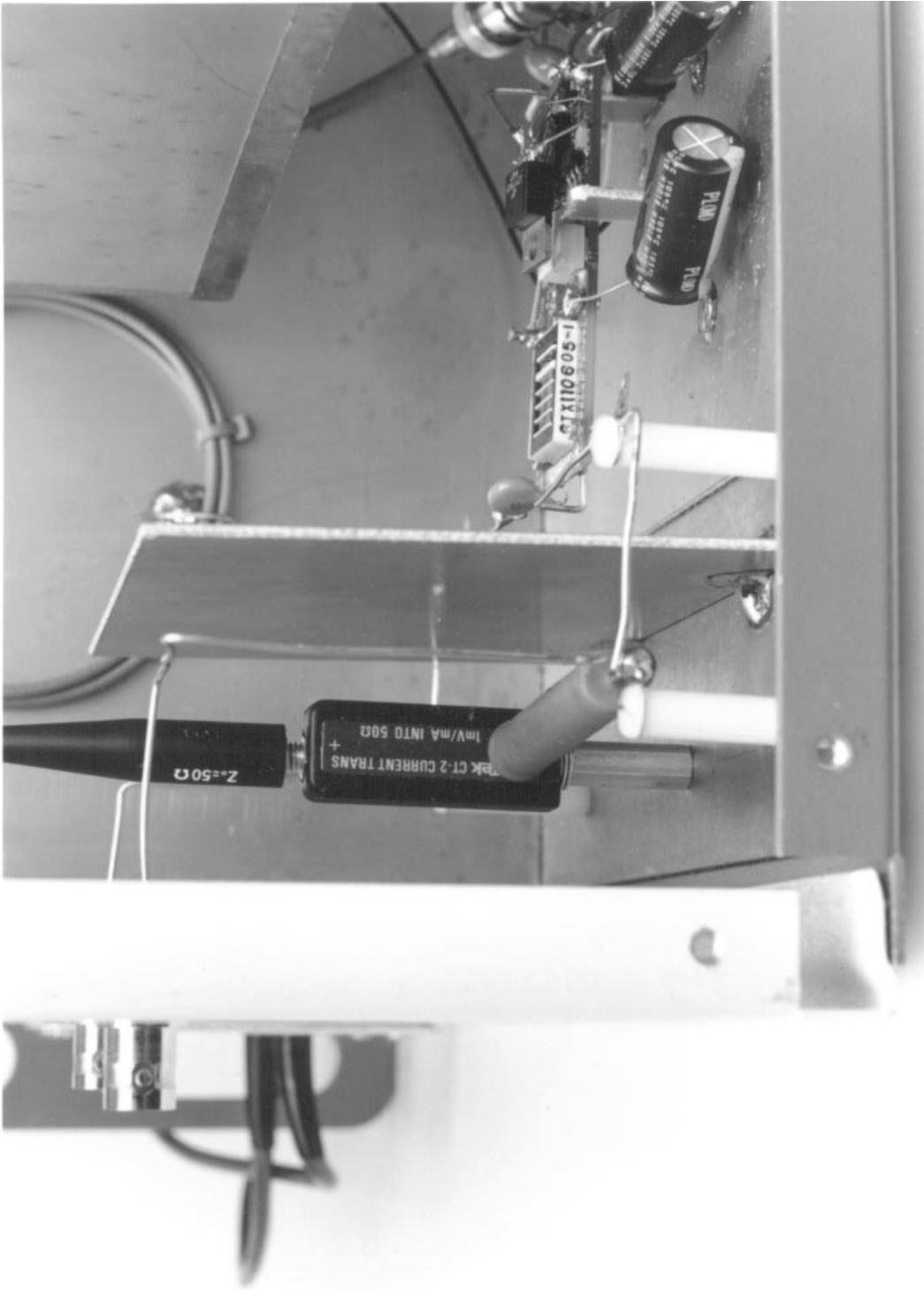
AN65-FC20

Figure C20. Differential Probes Are Mechanically Secured to Chassis, Discouraging Unauthorized Removal. All Compensation Access Holes Are Sealed, Preventing Unwanted Adjustment



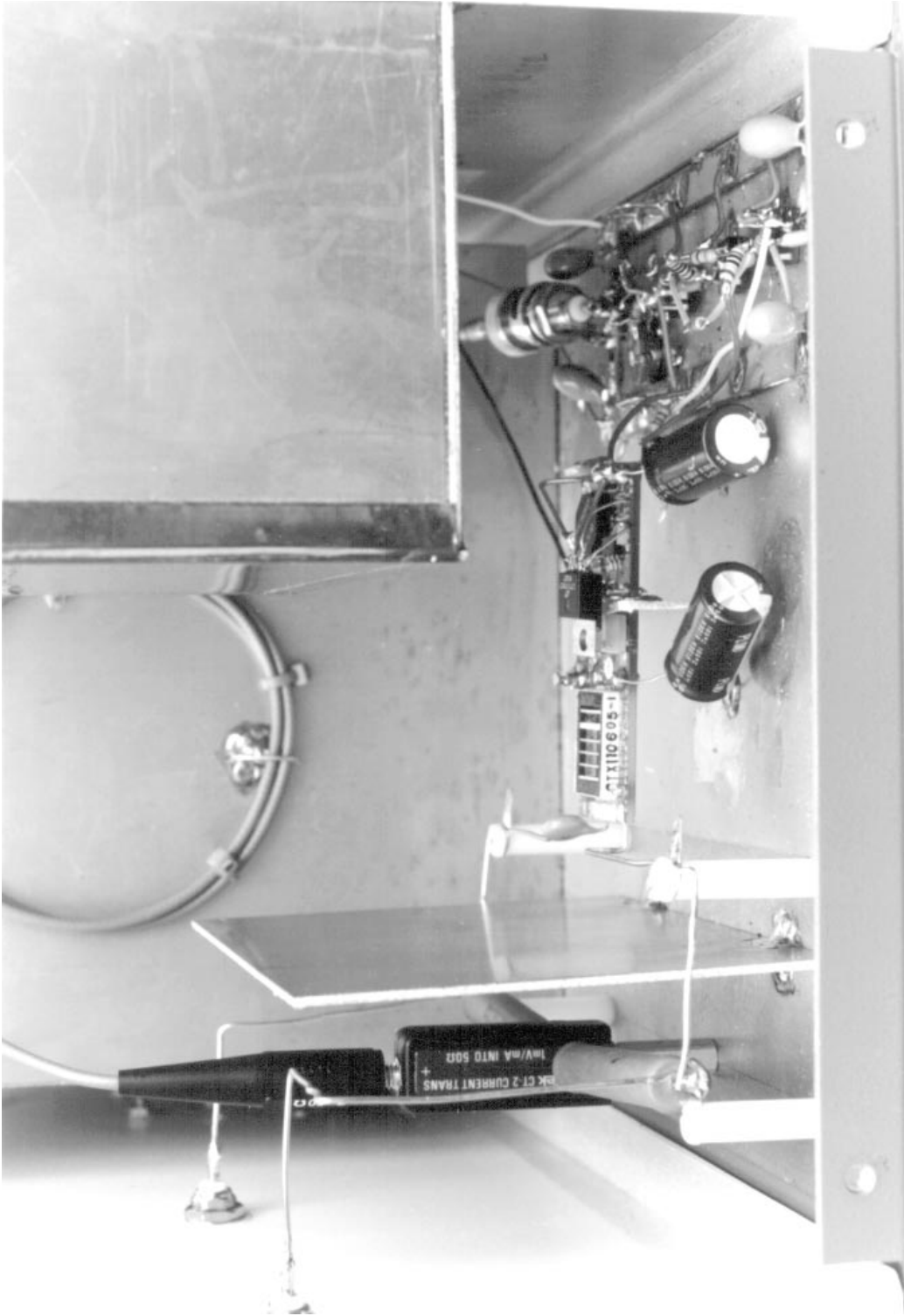
AN65-C21

Figure C21 . Calibrator Section Detail. Inverter in Center with Load Resistors and Current Transformer in Foreground. Note Shield Between Inverter and Load Resistors, and Low Capacitance Layout



AN65-C22

Figure C22. Calibrator Output Detail. Current Transformer Is Bootstrapped to Load Resistor's 0V Midpoint. Shield (Center) Prevents Interaction Between Transformer Field and Load Resistors or Current Transformer. Bus Wire and Nylon Stand-Offs Minimize Stray Capacitance



AN65FC23

Figure C23. Calibrator Section Showing Bus Wire/Nylon Post Construction Used to Minimize Stray Capacitance (Left). Inverter in Center; Control Electronics Located at Lower Right. Power Supply Is Enclosed in Shielded Box at Upper Right

Application Note 65

RMS Voltmeters

The efficiency measurements require an RMS responding voltmeter. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all AC voltmeters, including DVMs with AC ranges.

There are a number of ways to measure RMS AC voltage. Three of the most common include *average*, *logarithmic* and *thermally* responding. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true RMS value. Although these instruments are "real time" analog computers, their 1% error bandwidth is well below 300kHz and crest factor capability is limited. Almost all general purpose DVMs use such a logarithmically based approach and, as such, are not suitable for CCFL efficiency measurements. Thermally based RMS voltmeters are direct acting thermoelectronic analog computers. They respond to the input's RMS heating value. This technique is explicit, relying on the very definition of RMS (e.g., the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques.¹⁴ Additionally, they are insensitive to waveform shape and easily accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

Figure C24 shows a conceptual thermal RMS/DC converter. The input waveform warms a heater, resulting in increased output from its associated temperature sensor. A DC amplifier forces a second, identical, heater/sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input/output RMS voltage relationship is linear with unity gain.

The ability of this arrangement to reject ambient temperature shifts depends on the heater/sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater/sensor pairs are

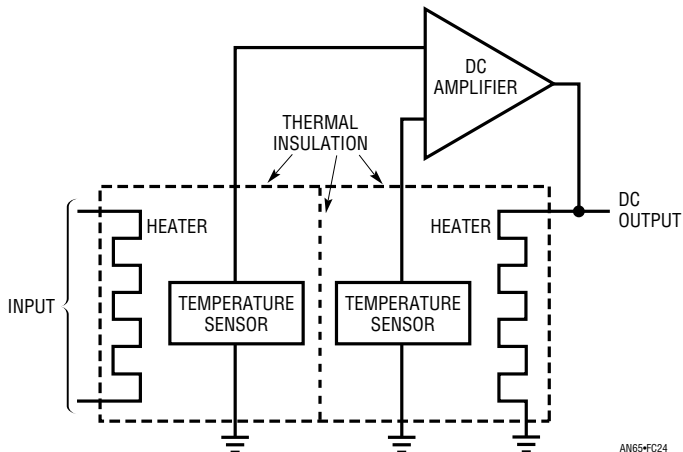


Figure C24. Conceptual Thermal RMS/DC Converter

matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier rejects this common mode term. Note that although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure C24's output is linear because the matched thermal pair's nonlinear voltage/temperature relationships cancel each other.

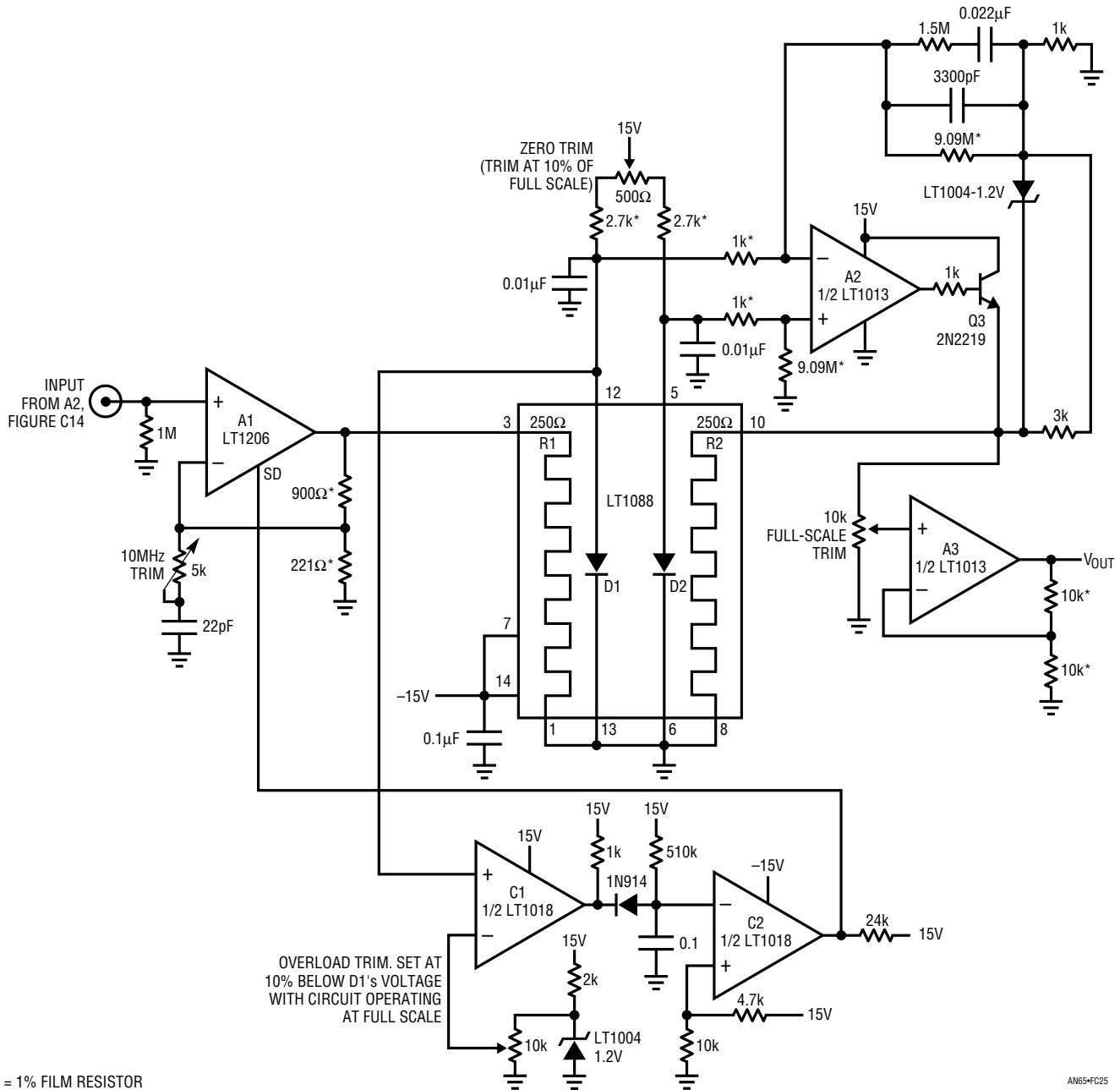
The advantages of this approach have made its use popular in thermally based RMS/DC measurements.

The instruments listed in Figure C11, while considerably more expensive than other options, are typical of what is required for meaningful results. The HP3400A and the Fluke 8920A are currently available from their manufacturers. The HP3403C, an exotic and highly desirable instrument, is no longer produced but readily available on the secondary market.

Figure C25 shows an RMS voltmeter which can be constructed instead of purchased.¹⁵ Its small size permits it to be built into bench and production test equipment. As shown, it is designed to be used with Figure C14's differential probe, although the configuration is adaptable to any CCFL-related measurement. It provides a true

Note 14: Those finding these descriptions intolerably brief are commended to References 4, 5, 6, 9, 10, 11 and 12.

Note 15: This circuit derives from Reference 27.



* = 1% FILM RESISTOR

AN65*FC25

Figure C25. Wideband RMS/DC Converter for Use with Differential Probe/Amplifier. Circuit Is also Usable with Current Probe/Amplifier with Appropriate Gain Adjustments

RMS/DC conversion from DC to 10MHz with less than 1% error, regardless of input signal waveshape. It also features high input impedance and overload protection.

The circuit consists of three blocks; a wideband amplifier, the RMS/DC converter and overload protection. The amplifier provides high input impedance and gain, and drives the RMS/DC converter's input heater. Input resistance is defined by the 1M resistor with input capacitance about

10pF. The LT1206 provides a flat 10MHz bandwidth gain of 5. The 5kΩ/22pF network gives A1 a slight peaking characteristic at the highest frequencies, allowing 1% flatness to 10MHz. A1's output drives the RMS/DC converter.

The LT1088-based RMS/DC converter is made up of matched pairs of heaters and diodes and a control amplifier. The LT1206 drives R1, producing heat which lowers

Application Note 65

D1's voltage. Differentially connected A2 responds by driving R2 via Q3 to heat D2, closing a loop around the amplifier. Because the diodes and heater resistors are matched, A2's DC output is related to the RMS value of the input, regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain trim, which is implemented at A3. A3's output is the circuit output. The LT1004 and associated components provide loop compensation and good settling time over wide ranges of operating conditions (see Footnote 14).

Start-up or input overdrive can cause A1 to deliver excessive current to the LT1088 with resultant damage. C1 and C2 prevent this. Overdrive forces D1's voltage to an abnormally low potential. C1 triggers low under these conditions, pulling C2's input low. This causes C2's output to go high, putting A1 into shutdown and terminating the overload. After a time determined by the RC at C2's input, A1 will be enabled. If the overload condition still exists the loop will almost immediately shut A1 down again. This oscillatory action will continue, protecting the LT1088 until the overload condition is removed.

Performance for the circuit is quite impressive. Figure C26 plots error from DC to 11MHz. The graph shows 1% error bandwidth of 11MHz. The slight peaking out to 5MHz is due to the gain boost network at A1's negative input. The peaking is minimal compared to the total error envelope, and a small price to pay to get the 1% accuracy to 10MHz.

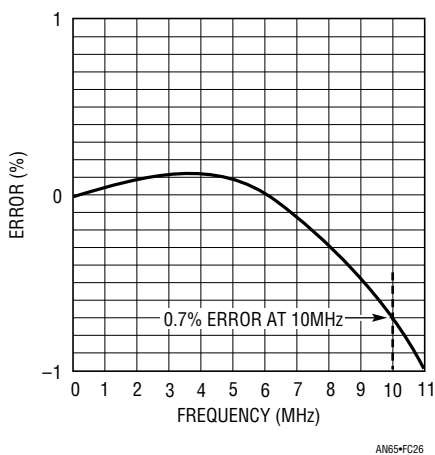


Figure C26. Error Plot for the RMS/DC Converter. Frequency-Dependent Gain Boost at A1 Preserves 1% Accuracy but Causes Slight Peaking Before Rolloff

To trim this circuit put the 5k Ω potentiometer at its maximum resistance position and apply a 100mV, 5MHz signal. Trim the 500 Ω adjustment for exactly 1V_{OUT}. Next, apply a 5MHz, 1V input and trim the 10k Ω potentiometer for 10.00V_{OUT}. Finally, put in 1V at 10MHz and adjust the 5k Ω trimmer for 10.00V_{OUT}. Repeat this sequence until circuit output is within 1% accuracy for DC-10MHz inputs. Two passes should be sufficient.

Calorimetric Correlation of Electrical Efficiency Measurements

Careful measurement technique permits a high degree of confidence in the efficiency measurement's accuracy. It is, however, a good idea to check the method's integrity by measuring in a completely different domain. Figure C27 does this by calorimetric techniques. This arrangement, identical to the thermal RMS voltmeter's operation (Figure C24), determines power delivered by the CCFL circuit by measuring its load temperature rise. As in the thermal RMS voltmeter, a differential approach eliminates ambient temperature as an error term. The differential amplifier's output, assuming a high degree of matching in the two thermal enclosures, proportions to load power. The ratio of the enclosure's E • I products yields efficiency information. In a 100% efficient system the amplifier's output energy would equal the power supply's output. Practically it is always less as the CCFL circuit has losses. This term represents the desired efficiency information.

Figure C28 is similar except that the CCFL circuit board is placed within the calorimeter. This arrangement nominally yields the same information, but is a much more demanding measurement because far less heat is generated. The signal-to-noise (heat rise above ambient) ratio is unfavorable, requiring almost fanatical attention to thermal and instrumentation considerations.¹⁶ It is significant that the *total* uncertainty between electrical and both calorimetric efficiency determinations was 3.3%. The two thermal approaches differed by about 2%. Figure C29 shows the calorimeter and its electronic instrumentation. Descriptions of this instrumentation and thermal measurements can be found in the References section following the main text.

Note 16: Calorimetric measurements are not recommended for readers who are short on time or sanity.

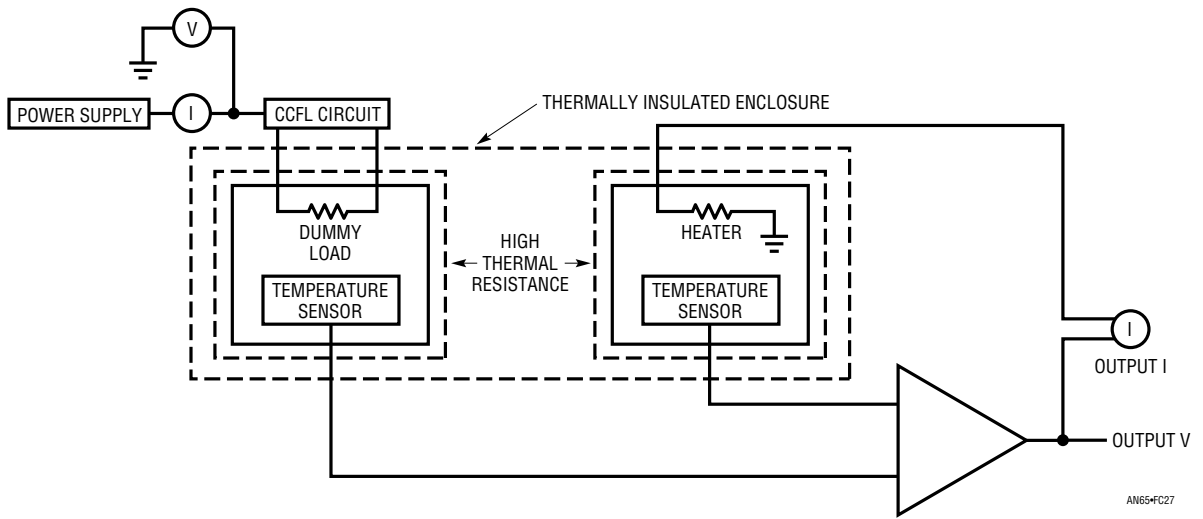


Figure C27. Efficiency Determination via Calorimetric Measurement. Ratio of Power Supply to Output Energy Gives Efficiency Information

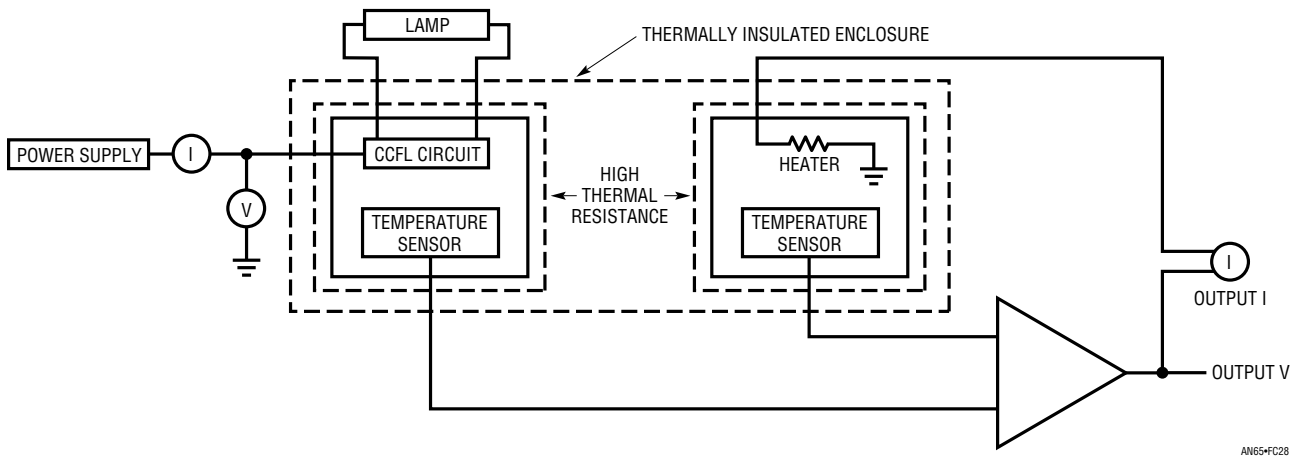
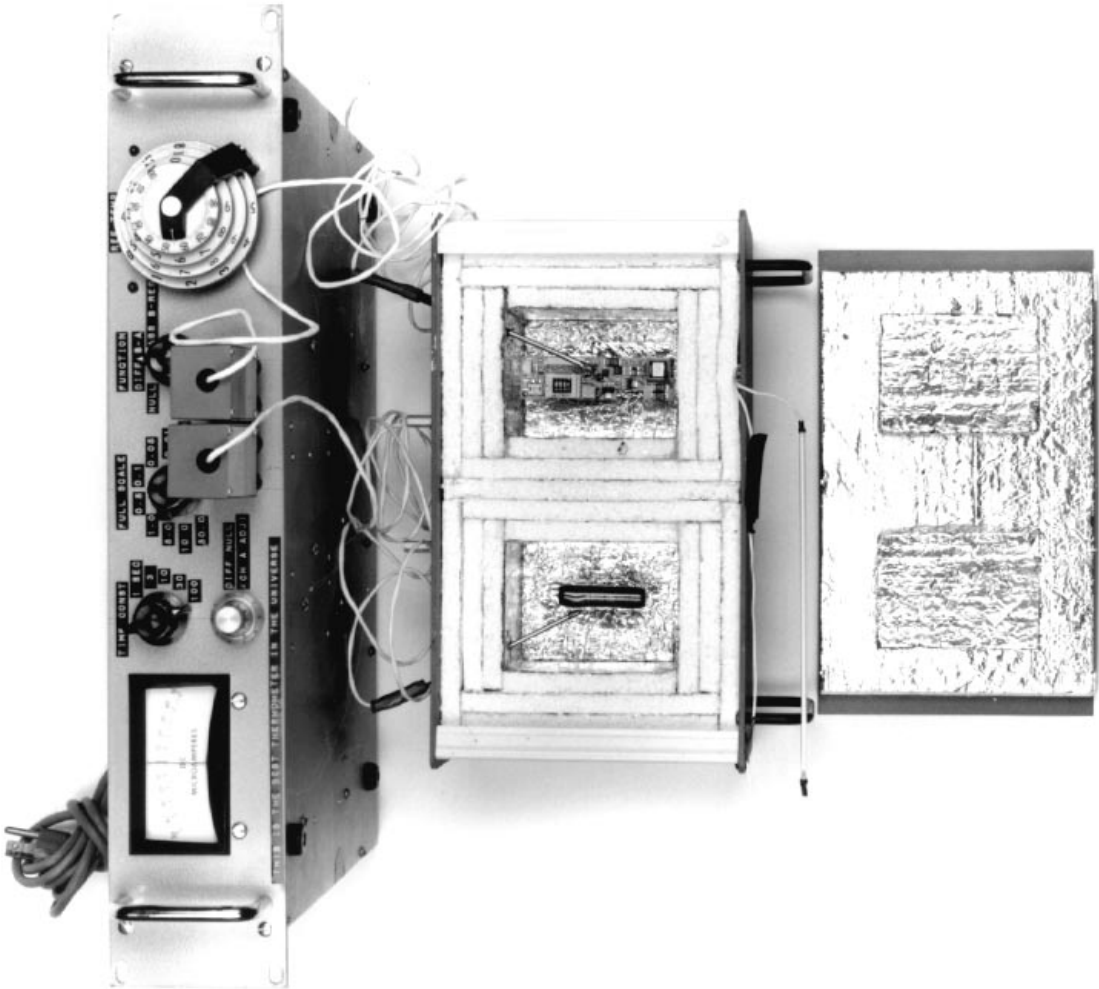


Figure C28. The Calorimeter Measures Efficiency by Determining Circuit Heating Losses



ASIN65-FC29

Figure C29. The Calorimeter (Center) and Its Instrumentation (Top). Calorimeter's High Degree of Thermal Symmetry Combined with Sensitive Servo Instrumentation Produces Accurate Efficiency Measurements. Lower Portion of Photo Is Calorimeter's Top Cover

APPENDIX D

PHOTOMETRIC MEASUREMENTS

In the final analysis, the ultimate concern centers around the efficient conversion of power supply energy to light. Emitted light varies monotonically with power supply energy,¹ but certainly not linearly. In particular, lamp luminosity may be highly nonlinear, particularly at high power vs drive power. There are complex trade-offs involving the amount of emitted light vs power consumption, drive waveform shape and battery life. Evaluating these trade-offs requires some form of photometer. The relative luminosity of lamps may be evaluated by placing the lamp in a light tight tube and sampling its output with photodiodes. The photodiodes are placed along the lamp's length and their outputs electrically summed. This sampling technique is an uncalibrated measurement, providing relative data only. It is, however, quite useful in determining relative lamp emittance under various drive conditions. Additionally, because the enclosure has essentially no parasitic capacitance, lamp performance may be evaluated under "zero loss" conditions. Figure D1 shows this "glometer," with its uncalibrated output appropriately scaled in "brights." The switches allow various sampling diodes along the lamp's length to be disabled. The photodiode signal-conditioning electronics are mounted behind the switch panel with the drive electronics located to the left.

Figure D2 details the drive electronics. A1 and A2 form a stabilized output Wein bridge sine wave oscillator. A1 is the oscillator and A2 provides gain stabilization in concert with Q1. The stabilizing loop's operating point is derived from the LT1021 voltage reference. A3 and A4 constitute a voltage-controlled amplifier which feeds power stage A5. A5 drives T1, a high ratio step-up transformer. T1's output sources current to the lamp. Lamp current is rectified and its positive portion terminated into the 1k resistor. The voltage appearing across this resistor, indicative of lamp current, biases A6. Band-limited A6 compares the lamp current-derived signal against the LT1021 reference and closes a loop back to A3. This loop's operating point, and hence lamp current, is set by the "current amplitude" adjustment over a 0mA to 6mA range. A1's "Frequency Adjust" control permits a 20kHz to 130kHz frequency operating range. The switch located at A1's output permits external sources of various waveforms and frequencies to drive the amplifier.

Note 1: But not always! It is possible to build highly electrically efficient circuits that emit less light than "less efficient" designs. See previous text and Appendix L, "A Lot of Cut Off Ears and No Van Goghs—Some Not-So-Great Ideas."

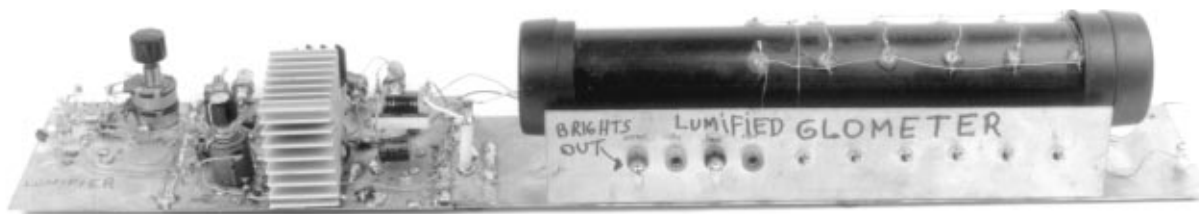


Figure D1. "Glometer" Measures Relative Lamp Emissivity under Various Drive Conditions. Test Lamp Is Inside Cylindrical Housing. Photodiodes on Housing Convert Light to Electrical Output (Center) Via Amplifiers (Not Visible in Photo). Electronics (Left) Permit Varying Drive Waveforms and Frequency

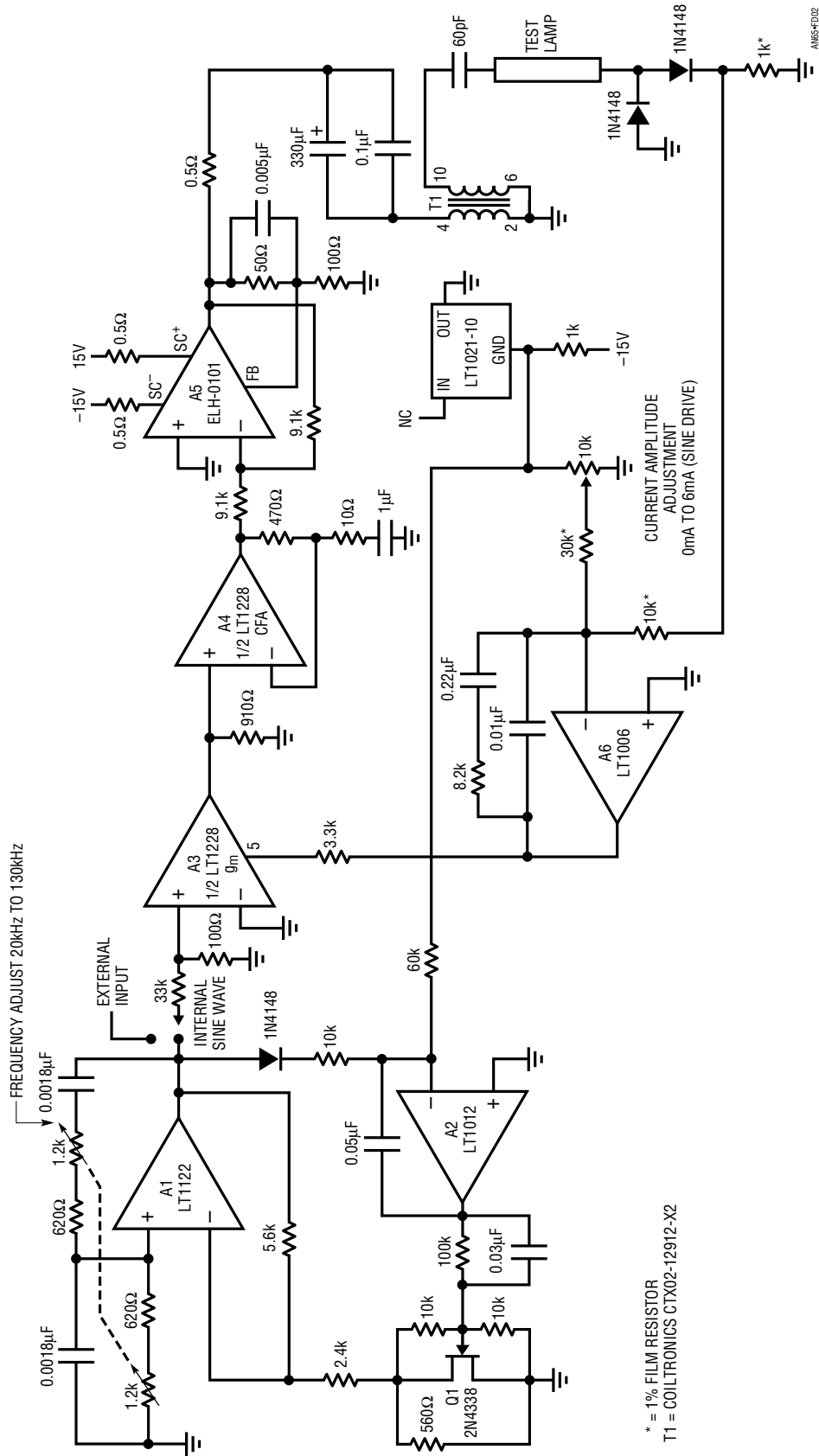


Figure D2. Glometer Drive Electronics Permits Varying Frequency and Waveshape Applied to Test Lamp. Resultant Data Shows Lamp Sensitivity to These Parameters

The drive scheme and wideband transformer provide extremely faithful response. Figure D3 shows waveform fidelity at 100kHz with a 5mA lamp load. Trace A is T1's primary drive and Trace B is the high voltage output. Figure D4, a horizontal and vertical expansion of D3, indicates well-controlled phase shift. Residual effects cause slight primary impedance variations (note primary drive nonlinearity at the sixth vertical division), although the output remains singularly clean.

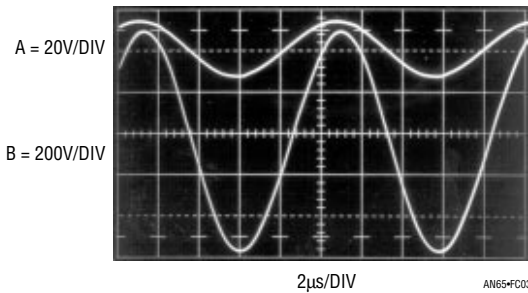


Figure D3. Wideband Transformers Input (Trace A) and Output (Trace B) Waveforms Indicate Clean Response at 100kHz

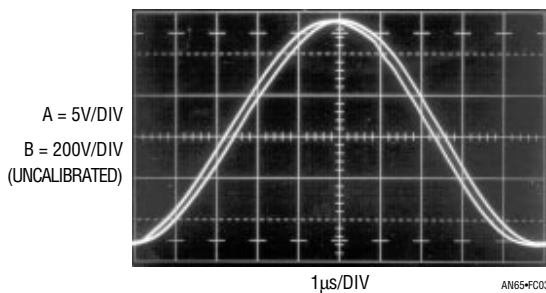


Figure D4. Magnified Versions of Figure D3's waveforms. Output (Trace B) Is Undistorted Despite Slight Drive (Trace A) Deformity at Sixth Vertical Division. Transformer Rolloff Dictates This Desirable Behavior

Figure D5 shows the photodiode signal conditioning. Groups of various photodiodes bias amplifiers A1 through A6. Each amplifier's output is fed via a switch to summing amplifier A7. The switches permit establishment of "dead zones" along the test lamp's length, enhancing ability to study emissivity vs location. A7's output represents the summation of all sensed lamp emission.

The glometer's ability to measure relative lamp emission under controlled settings of frequency, waveshape and drive current in a "lossless" environment is invaluable for evaluating lamp performance. Evaluating display performance and correlating results with customers requires absolute light intensity measurements.

Calibrated light measurements call for a true photometer. The Tektronix J-17/J1803 photometer is such an instrument. It has been found particularly useful in evaluating display (as opposed to simply the lamp) luminosity under various drive conditions. The calibrated output permits reliable correlation with customer results.² The light tight measuring head allows evaluation of emittance evenness at various display locations.

Figure D6 shows the photometer in use evaluating a display. Figure D7 is a complete display evaluation setup. It includes lamp and DC input voltage and current instrumentation, the photometer described and a computer (lower right) for calculating optical and electrical efficiency.

Note 2: It is unlikely customers would be enthusiastic about correlating the "brights" units produced by the aforementioned glometer.

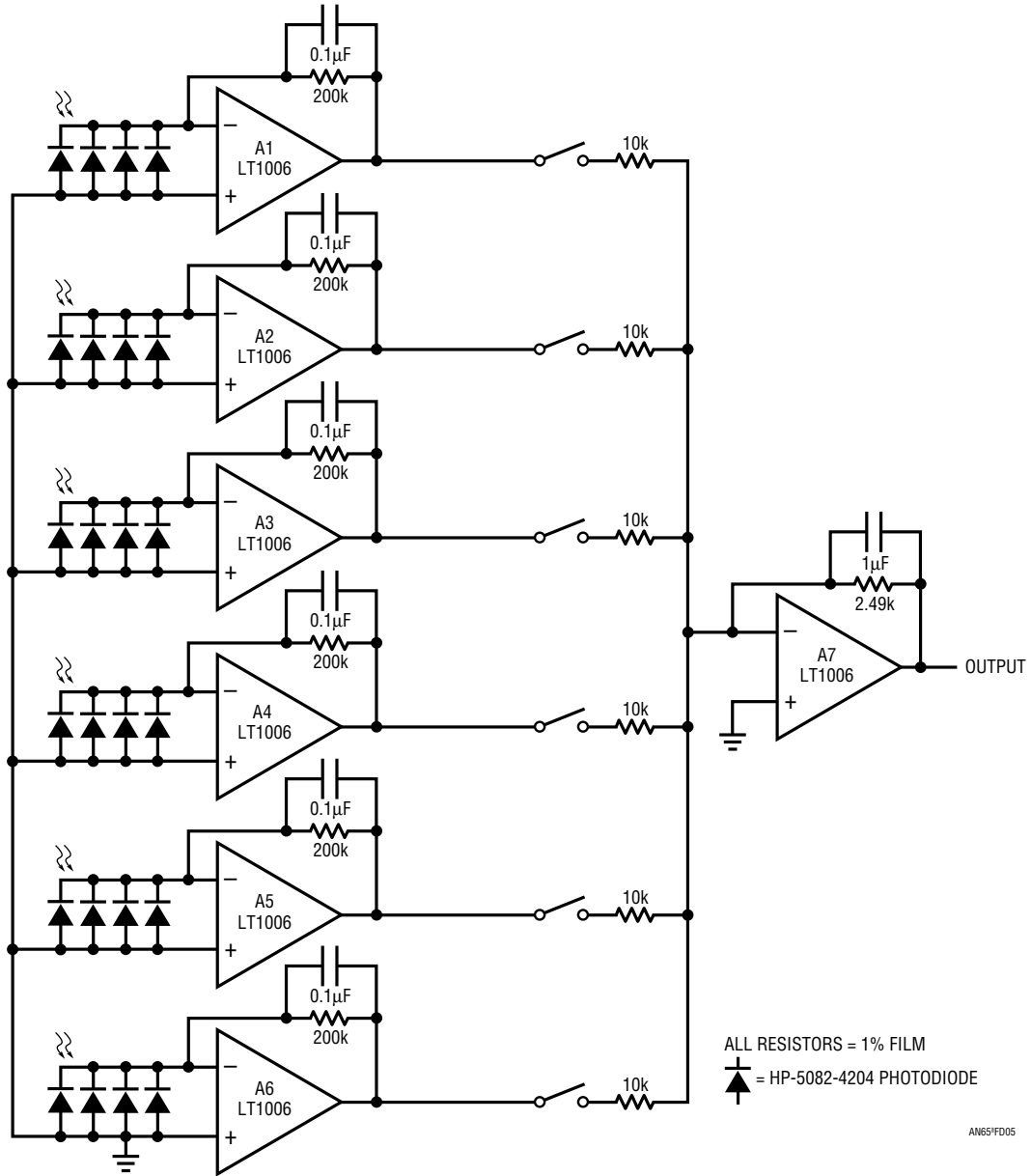
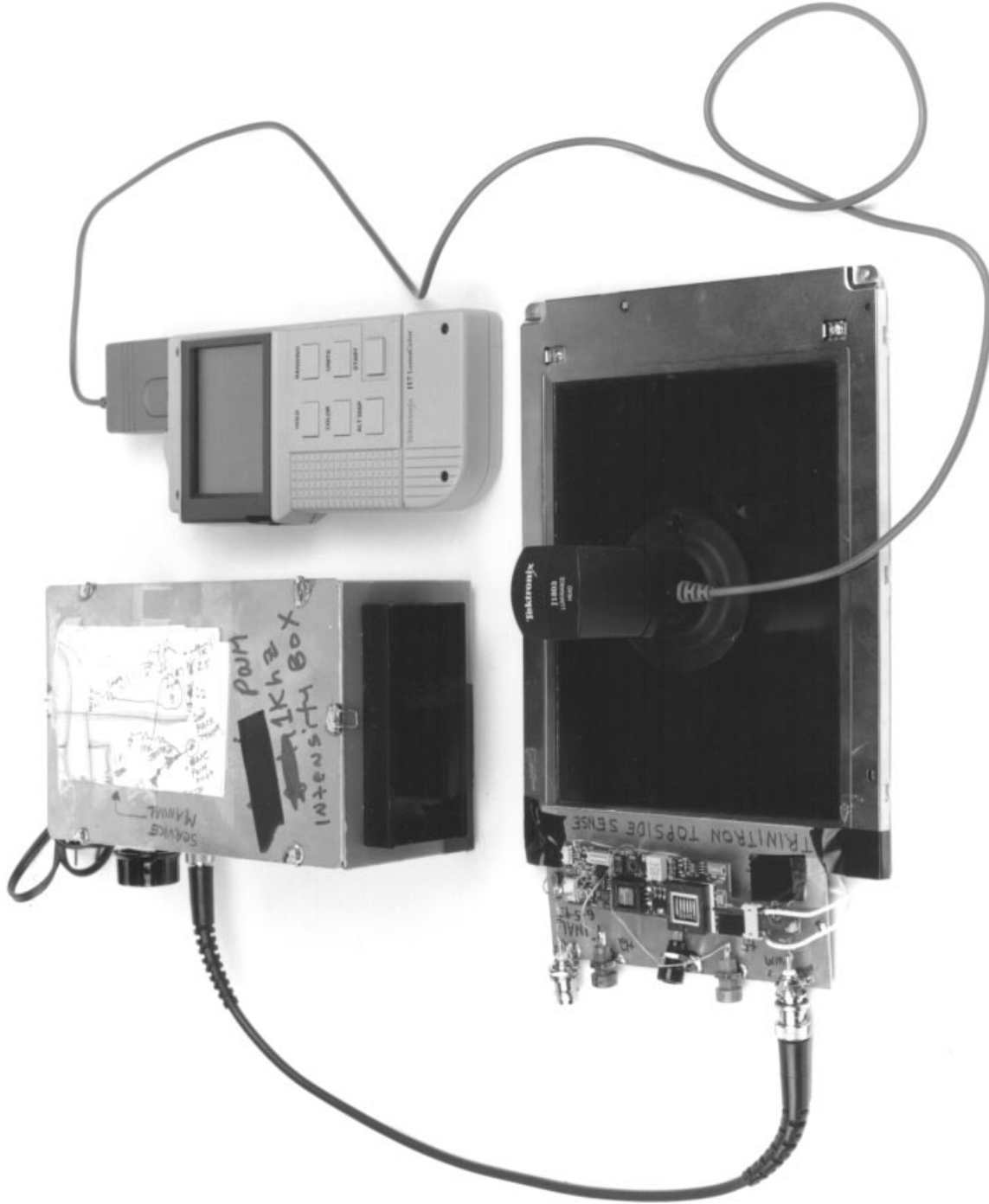


Figure D5. Glometer Photodiode/Amplifier Converts Lamp Light to Relative, Uncalibrated Electrical Output. Switches Permit Investigation of Individual Portions of Lamp Output



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Figure D6. Apparatus for Calibrated Photometric Display Evaluation. Photometer (Upper Right) Indicates Display Luminosity Via Sensing Head (Center). CCFL Circuit (Left) Intensity Is Controlled by Figure F6's Calibrated Pulse Width Generator (Upper Left)



Figure D7. Complete CCFL Test Set Includes Photometer (Left and Center), Differential Voltage Probe/Amplifier (Upper and Lower Center), Current Probe Electronics (Right) and Input V and I DC Instrumentation (Upper Left). Computer (Lower Right) Permits Calculation of Electrical and Optical Efficiency

APPENDIX E

OPEN LAMP/OVERLOAD PROTECTION

The CCFL circuit's current source output means that "open" or broken lamps cause full voltage to appear at the transformer output. Safety or reliability considerations sometimes make protecting against this condition desirable. This protection is built into the LT118X series parts. Figure E1 shows a typical circuit. C5, R2 and R3 sense differentially across the Royer converter. Normally, the voltage across the Royer is controlled to relatively small values. An open lamp will cause full duty cycle modulation at the V_{SW} pin, resulting in large current drive through L2. This forces excessive Royer voltage at the C5/R2/R3

network, causing LT1184 shutdown via the "bulb" pin. C5 sets a delay, allowing Royer operation at high drive levels during lamp start-up. This prevents unwarranted shut-down during the lamp's transient high impedance start-up state.

The LT1172 and similar switching regulator parts need additional circuitry for open lamp protection. Figure E2 details the modifications. Q3 and associated components form a simple voltage mode feedback loop that operates if V_Z turns on. If T1 sees no load, there is no feedback and the Q1/Q2 pair receives full drive. Collector voltage rises to

abnormal levels, and V_Z biases via Q1's V_{BE} path. Q1's collector current drives the feedback node and the circuit finds a stable operating point. This action controls Royer drive and hence output voltage. Q3's sensing across the Royer provides power supply rejection. V_Z 's value should be somewhat above the worst-case Q1/Q2 V_{CE} voltage under running conditions. It is desirable to select V_Z 's value so clamping occurs at the lowest output voltage possible while still permitting lamp start-up. This is not as tricky as it sounds because the $10k/1\mu F$ RC delays the effects of Q3's turn-on. Usually, selecting V_Z several volts above the worst-case Q1/Q2 V_{CE} will suffice.

Additional protection for all CCFL circuits is possible by fusing the main supply line, typically at a value twice the largest expected DC current. Also, a thermally activated fuse is sometimes mated to Q1 and Q2. Excessive Royer current causes heating in the transistors, activating the fuse.

Overload Protection

In certain cases it is desirable to limit output current if either lamp wire shorts to ground. Figure E3 modifies a switching regulator-based circuit to do this. The current sensing network, normally series connected with the lamp, is moved to the transformer. Any overload current must originate from the transformer. Feedback sensing in this path provides the desired protection. This connection measures *total* delivered current, including parasitic terms, instead of lamp return current. Slight line regulation and current accuracy degradation occurs, but not to an objectionable extent.

Floating lamp circuits, because of their isolation, are inherently immune to ground referred shorts. Shorted lamp wires are also tolerated because of the primary side current sensing.

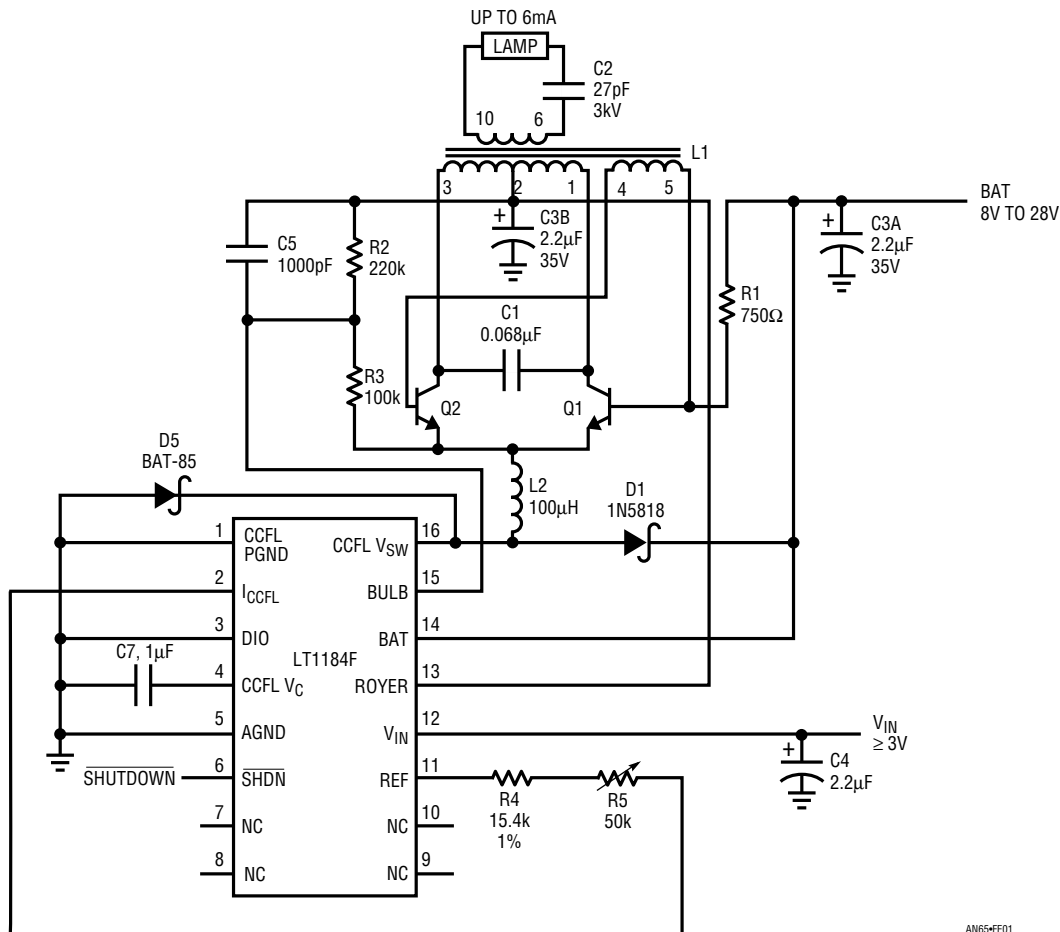


Figure E1. C5, R2 and R3 Provide Delayed Sensing Across Royer Converter, Protecting Against Open Lamp Conditions in LT118X Series ICs

Application Note 65

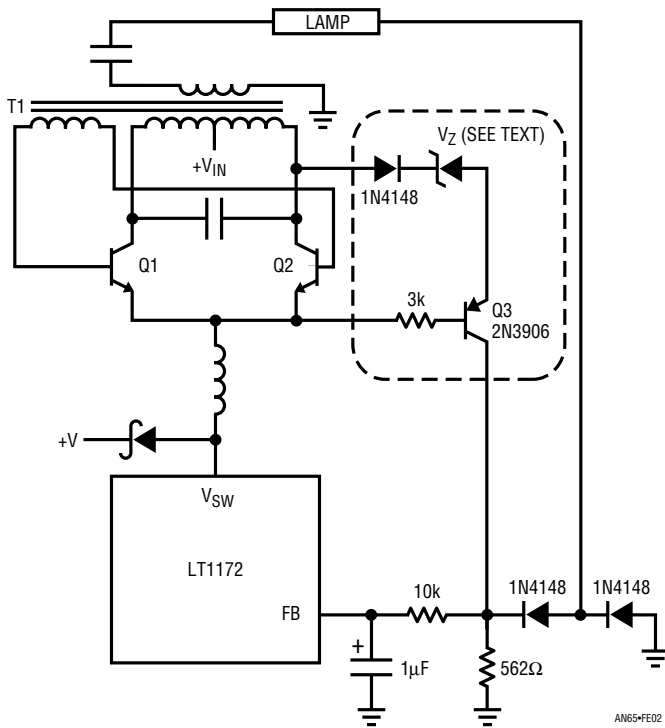


Figure E2. Q3 and Associated Components Form a Local Regulating Loop to Limit Output Voltage

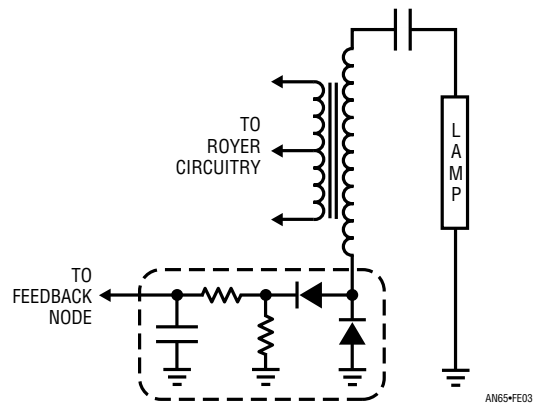


Figure E3. Relocating Feedback Network (Circled Components) to Transformer Secondary Maintains Current Control When Output Is Shorted. Trade-Off Is Slight Degradation in Line Regulation and Current Accuracy

APPENDIX F

INTENSITY CONTROL AND SHUTDOWN METHODS

The CCFL circuits usually require shutdown capability and some form of intensity (dimming) control. Figure F1 lists various options for the LT118X parts. Control sources include pulse width modulation (PWM), potentiometers and DACs or other voltage sources. The LT1186 (not shown) uses a digital serial-bit stream data input and is discussed in text associated with Figure 51.

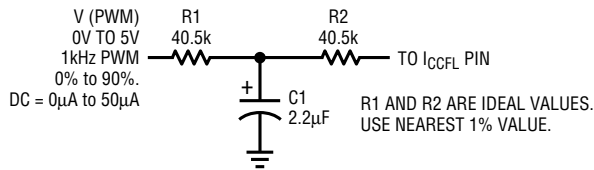
In all cases shown the average current into the I_{CCFL} pin sets lamp current. As such, the amplitude and duty cycle must be controlled in cases A and B. The remaining examples use the LT118X's reference to eliminate amplitude uncertainty-induced errors.

Figure F2 shows shutdown options for LT118X parts. The parts have a high impedance Shutdown pin, or power may simply be removed from V_{IN} . Switching V_{IN} power requires a higher current control source but shutdown current is somewhat lower.

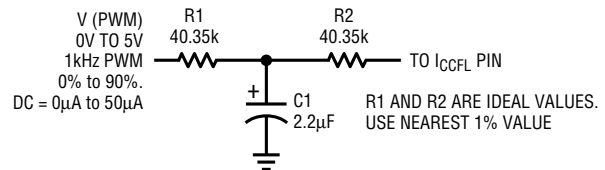
Figure F3 shows options for dimming control in LT1172 and similar regulator-based CCFL circuits. Three basic ways to control intensity appear in the figure. The most common intensity control method is to add a potentiometer in series with the feedback termination. When using this method ensure that the minimum value (in this case 562Ω) is a 1% unit. If a wide tolerance resistor is used the lamp current, at maximum intensity setting, will vary appropriately.

Pulse width modulation or variable DC is sometimes used for intensity control. Two interfaces work well. Directly driving the Feedback pin via a diode— $22k$ resistor with DC or PWM produces intensity control. The other method shown is similar, but places the $1\mu F$ capacitor outside the feedback loop to get best turn-on transient response. This is the best method if output overshoot must be minimized. Note that in all cases the PWM source amplitude at 0%

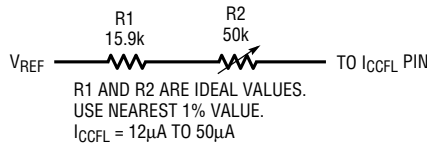
(F1a) LT1182/LT1183 I_{CCFL} PWM Programming



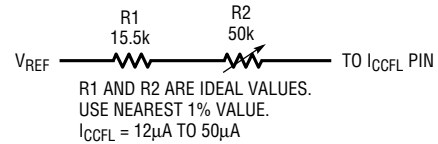
(F1b) LT1184/LT1184F I_{CCFL} PWM Programming



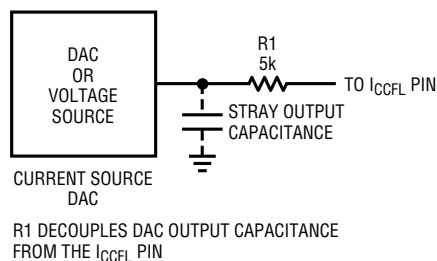
(F1c) LT1183 I_{CCFL} Programming with Potentiometer Control



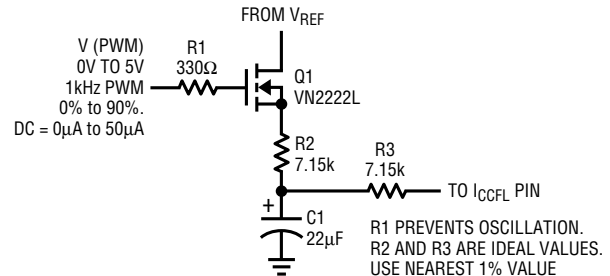
(F1d) LT1184/LT1184F I_{CCFL} Programming with Potentiometer Control



(F1e) LT1182/LT1183/LT1184/LT1184F I_{CCFL} Programming with DAC or Voltage Source Control

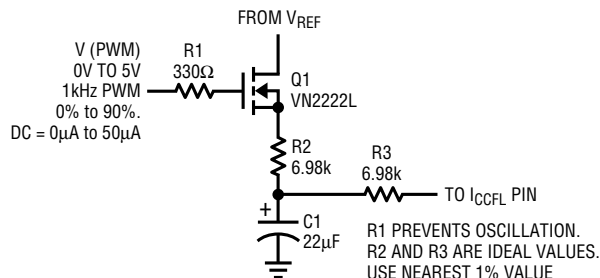


(F1f) LT1183 I_{CCFL} PWM Programming with V_{REF}

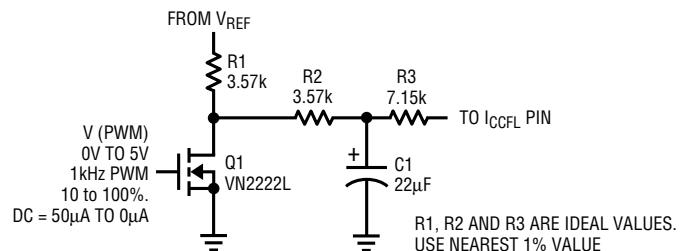


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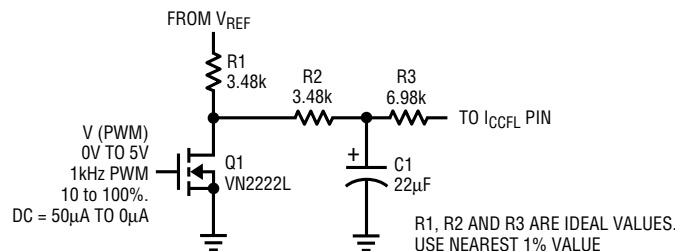
(F1g) LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}



(F1h) LT1183 I_{CCFL} PWM Programming with V_{REF}



(F1i) LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}



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Figure F1. Various Dimming Options for LT118X Series Parts. LT1186 (Not Shown) Has Serial-Bit Stream Digital Dimming Input

Application Note 65

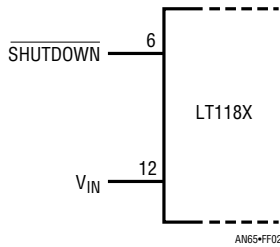


Figure F2. Shutdown Options for LT118X Series Parts Include Shutdown Pin or Simply Removing V_{IN}

duty cycle does not, by definition, effect full-scale lamp current certainty. See the main text section, “Feedback Loop Stability Issues” for pertinent discussion.

Figure F4 shows methods for shutting down switching regulator-based CCFL circuits. In LT1172 circuits pulling the V_C pin to ground puts the circuit into micropower shutdown. In this mode about $50\mu A$ flows into the LT1172 V_{IN} pin with essentially no current drawn from the main (Royer center tap) supply. Turning off V_{IN} power eliminates the LT1172’s $50\mu A$ drain. Other regulators, such as the LT1372, have a separate Shutdown pin.

About Potentiometers

Potentiometers, frequently used in CCFL dimming, require thought to avoid problems. In particular, resistance, ratio tolerances and other issues can upset an ill-prepared design. Keep in mind that ratio tolerances (see Figure F5)

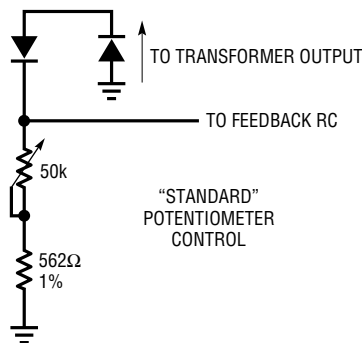


Figure F3. Various Options for Intensity Control in LT1172 and Similar Switching Regulator-Based CCFL Circuits

are usually better than absolute resistance specifications. Because of this, it is sometimes advantageous to use the device as a voltage divider instead of a rheostat. The key issue in potentiometer-based dimming is usually ensuring that lamp overdrive cannot occur. This is why arranging dimming schemes for maximum intensity at “shorted” potentiometer positions is preferable. The “end resistance” tolerance, which should be checked, is often less significant and more repeatable than that for maximum resistance or even ratio setting. Other issues include wiper current capability, taper characteristic and circuit sensitivity to “opens.” Always review circuit behavior for maximum wiper current demands. CCFL dimming schemes almost never require significant wiper current, but ensure that the particular scheme used doesn’t have this problem.

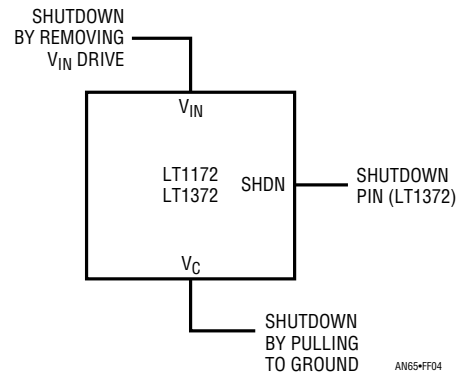
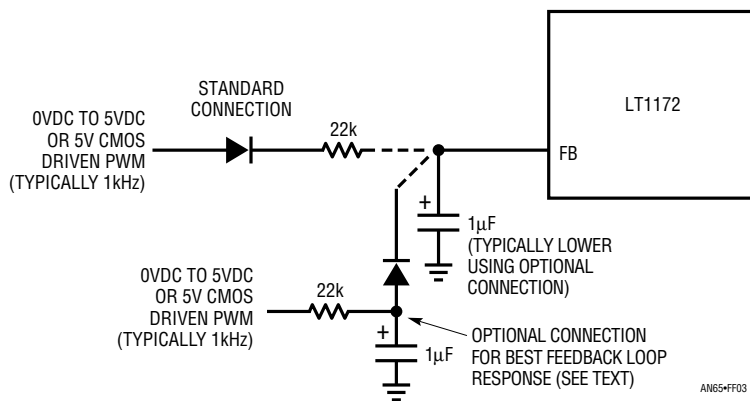


Figure F4. Various Shutdown Options in LT1172/ LT1372 Type CCFL Circuits



The potentiometers taper, which may be linear or logarithmic, should be matched to the lamp's current-vs-light output characteristic to provide easy user settability. A poorly chosen unit can cause most of the useful dimming range to occur in a small section of potentiometer travel. Finally, always evaluate how the circuit will react if any terminal develops an open condition, which sometimes happens. It is imperative that the circuit have some relatively benign failure mode instead of forcing excessive lamp current or some other regrettable behavior.

Electronic equivalents of potentiometers are monolithic resistor chains tapped by MOS switches. Some devices

feature nonvolatile onboard memory. These units have voltage rating restrictions which must be adhered to as with any integrated circuit. Additionally, they have all the limitations discussed in the section on mechanical potentiometers. Their most serious potential difficulty in backlight dimming applications is extremely high end resistance. In the "shorted" position the FET switch's on-resistance is typically 200Ω —much higher than a mechanical unit. Because of this, electronic potentiometers must almost always be set up as 3-terminal voltage dividers. This can usually be accommodated but may eliminate these devices in some applications.

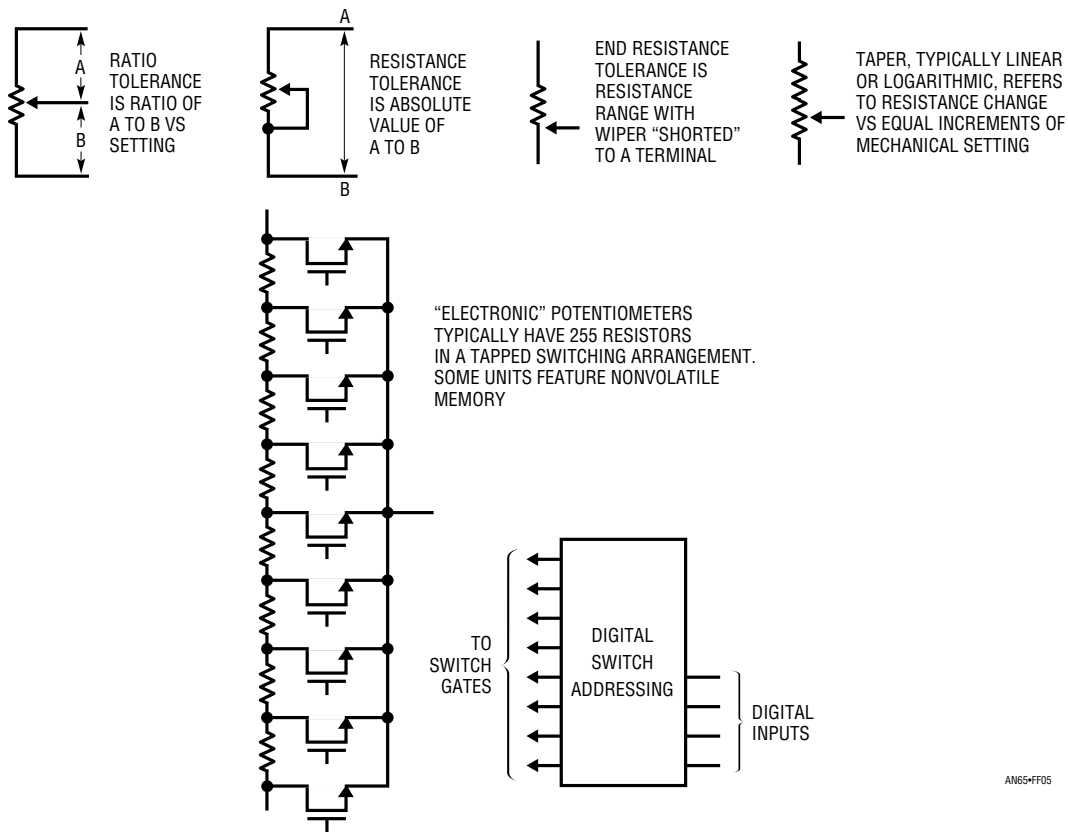


Figure F5. Relevant Characteristics of Mechanical and Electronic Potentiometers in CCFL Dimming Applications

Application Note 65

Precision PWM Generator

Figure F6 shows a simple circuit which generates precision variable pulse widths. This capability is useful when testing PWM-based intensity schemes. The circuit is basically a closed-loop pulse width modulator. The crystal controlled 1kHz input clocks the C1/Q1 ramp generator via the differentiator/CMOS inverter network and the LTC201 reset switch. C1's output drives a CMOS inverter, the output of which is resistively sampled, averaged and presented to A1's negative input. A1 compares this signal with a variable voltage from the potentiometer. A1's output biases the pulse width modulator, closing a loop around it. The CMOS inverter's purely ohmic output structure combines with A1's ratiometric operation (e.g., both of A1's input signals derive from the 5V supply) to hold pulse width constant. Variations in time, temperature and supply have essentially no effect. The potentiometer's setting is the sole determinant of output pulse width. Additional inverters provide buffering and furnish the

output. The Schottky diodes protect the output from latchup due to cable-induced ESD or accidental events¹ during testing.

The output width is calibrated by monitoring it with a counter while adjusting the 2kΩ trim pot.

As mentioned, the circuit is insensitive to power supply variation. However, the CCFL circuit averages the PWM output. It cannot distinguish between a duty cycle shift and supply variation. As such, the test box's 5V supply should be trimmed $\pm 0.01V$. This simulates a "design centered" logic supply under actual operating conditions. Similarly, paralleling additional logic inverters to get lower output impedance should be avoided. In actual use, the CCFL dimming port will be driven from a single CMOS output, and its impedance characteristics must be accurately mimicked.

Note 1: "Accidental events" is a nice way of referring to the stupid things we all do at the bench. Like shorting a CMOS logic output to a -15V supply (then I installed the diodes).

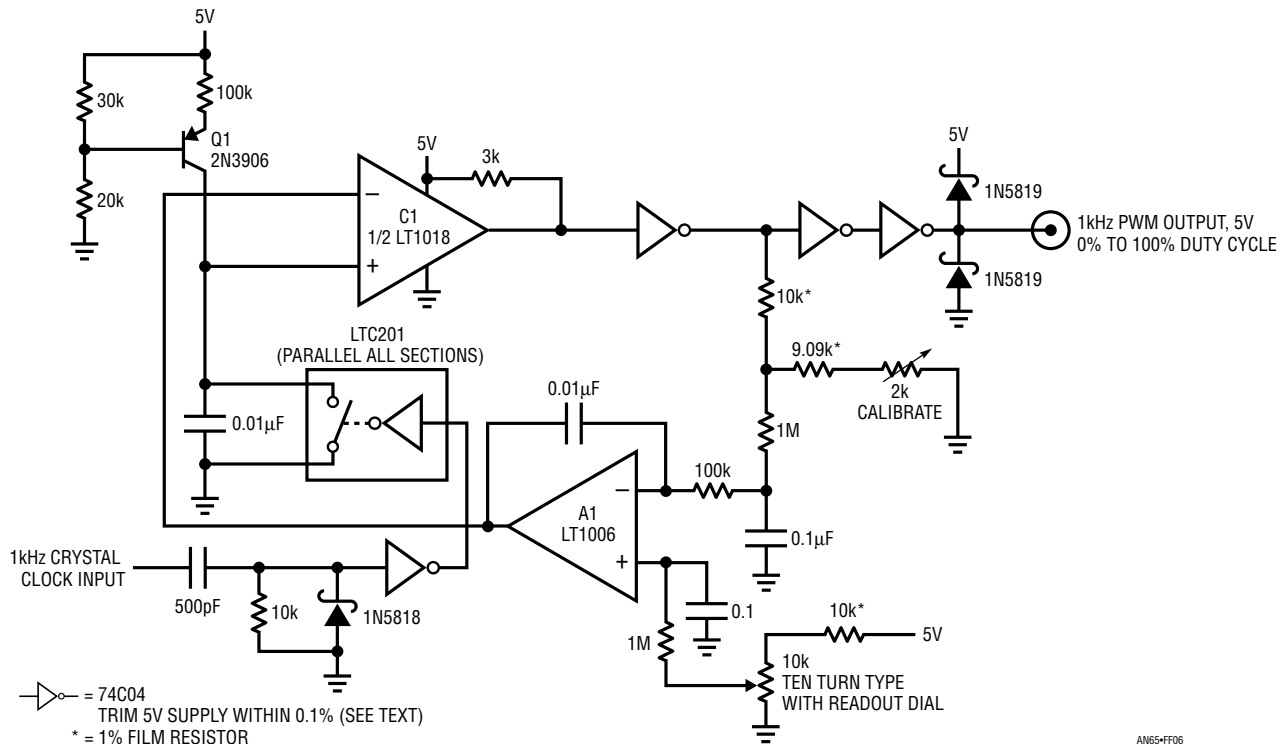


Figure F6. The Calibrated Pulse Width Test Box. A1 Controls C1-Based Pulse Width Modulator, Stabilizing Its Operating Point

APPENDIX G

LAYOUT, COMPONENT AND EMISSIONS CONSIDERATIONS

The CCFL circuits described in the text are remarkably tolerant of layout and impedance in supply lines. This is due to the Royer's relatively continuous current drain over time. Some review of current flow is, however, worthwhile. Figure G1 shows the more critical paths in thick lines for switching regulator-based CCFL circuits. In actual layout, these traces should be reasonably short and thick. The most critical consideration is that C1, T1's center tap and the diode should be connected *directly* together with minimum trace area between them. Similarly, C2 should be near the V_{IN} pin, although this placement is not nearly as critical as C1's.

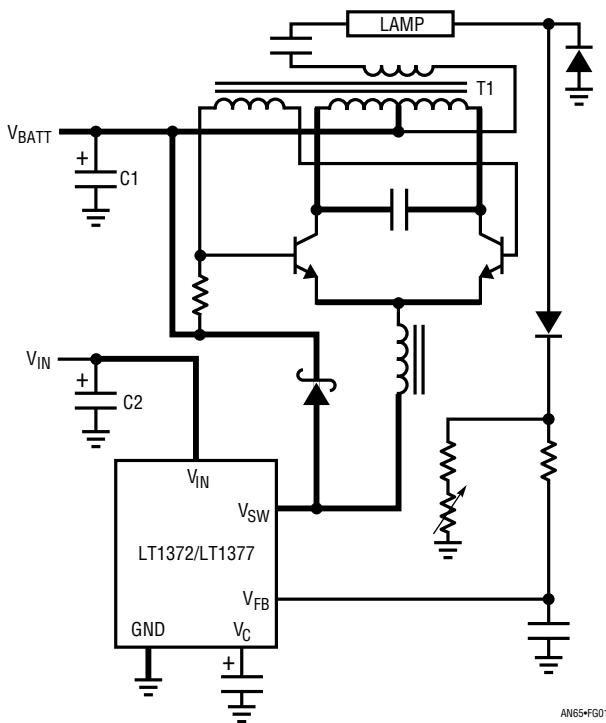


Figure G1. Thick Lines Denote PC Traces Requiring Low Impedance Layout in LT1172/LT1372 Type CCFL Circuits. Bypass Capacitors Associated with These Paths Should Be Mounted Near Load Point

Figure G2 indicates similar layout treatment for LT118X-based circuits. As before, the Royer and V_{IN} bypass capacitors should be near their respective load points, with the diode in close proximity to the Royer center tap.

Circuit Segmenting

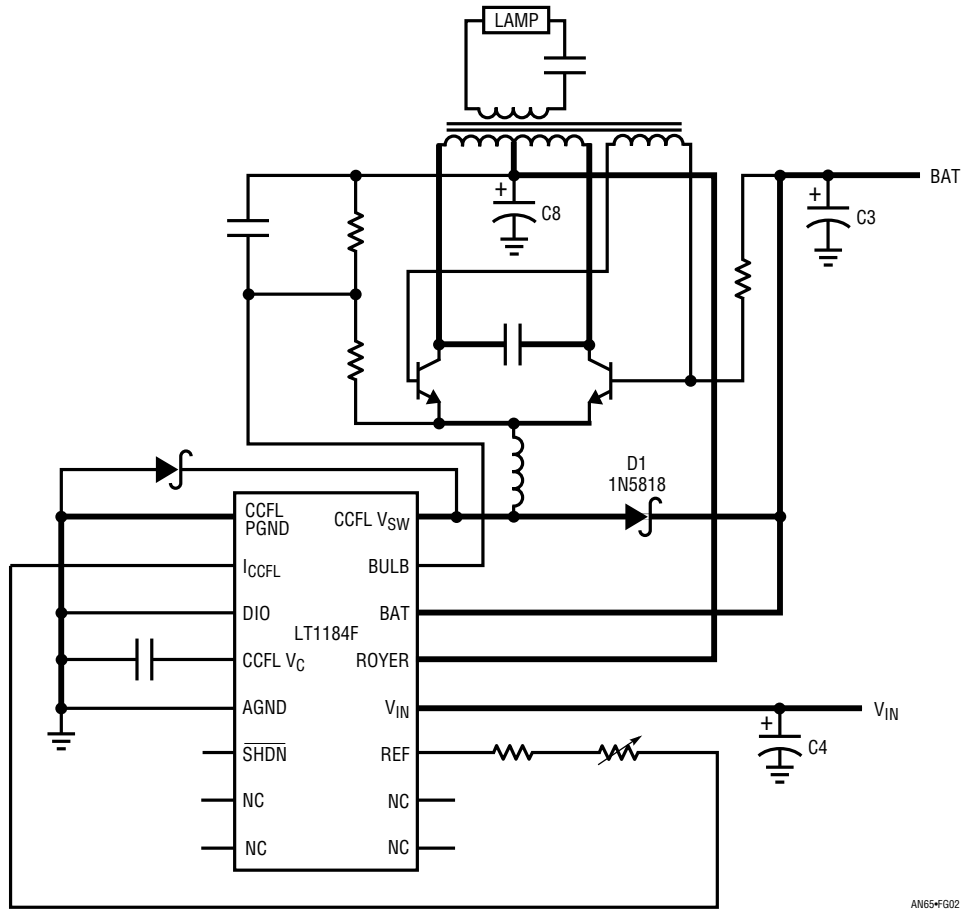
In cases where space is extremely limited it may be desirable to physically segment the circuit. Some designs have placed a section of the circuit near the display with another portion remotely located. The best place for segmenting is the junction of the Royer transistor emitters and the inductor (Figure G3). Introducing a long, relatively lossy connection at this point imposes no penalty because signal flow into the inductor closely resembles a constant current source.

There are no wideband components due to the inductor's filtering effect. Figure G4 shows emitter voltage (Trace A) and current (Trace B) waveforms. There is no wideband component or other significant high speed energy movement. The inductor current waveform trace thickening due to Royer and switching regulator frequency mixing is not deleterious.

A very special case of segmentation involves replacing the transformer with two smaller units. Aside from space (particularly height) savings, electrical advantages are also realized. See Appendix I for details.

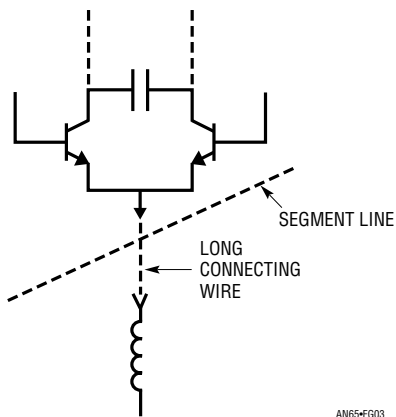
High Voltage Layout

Special attention is required for the board's high voltage sections. Board leakage, which can increase dramatically over life due to condensation cycling and particulate matter trapping, must be minimized. If precautions are not taken leakage will cause degraded operation, failures or destructive arcing. The only sure way to eliminate these possibilities is to *completely isolate the high voltage points from the circuit*. Ideally, no high voltage point should be within 0.25" of any conductor. Additionally, moisture trapping due to condensation cycling or improper board washing can be eliminated by routing the



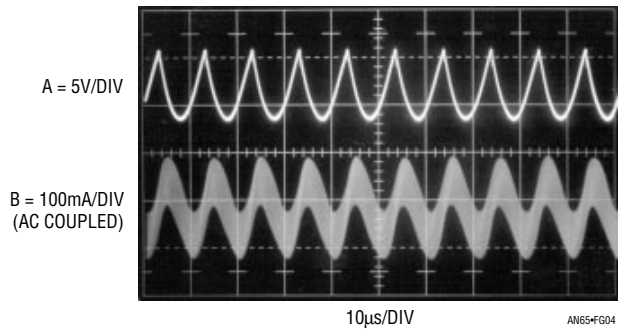
AN65-FG02

Figure G2. Critical Current Paths for LT118X Type Circuits. Thick Lines Denote PC Traces Requiring Low Impedance. Bypass Capacitors Associated with These Paths Should Be Near Load Points



AN65-FG03

Figure G3. CCFL Circuit May Be Segmented in Limited Space Applications. Breaking at Emitter/Inductor Junction Imposes No Penalty



AN65-FG04

Figure G4. Royer Emitter/Inductor Junction Is Ideal Point for Segmenting CCFL Circuit. Voltage (Trace A) and Current (Trace B) Waveforms Contain Little High Frequency Content. Trace Thickening of Current Waveform Is Due to Frequency Mixing in Inductor

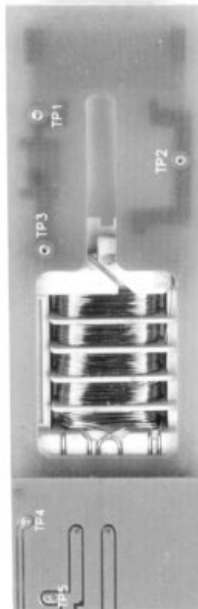
area under the transformer. This treatment, standard technique in high voltage layout, is strongly recommended. In general, carefully evaluate all high voltage areas for possible leakage or arcing problems due to layout, board

manufacturing or environmental factors. Clear thinking is needed to avoid unpleasant surprises. The following commented photographs, visually summarizing the above discussion, are examples of high voltage layout.



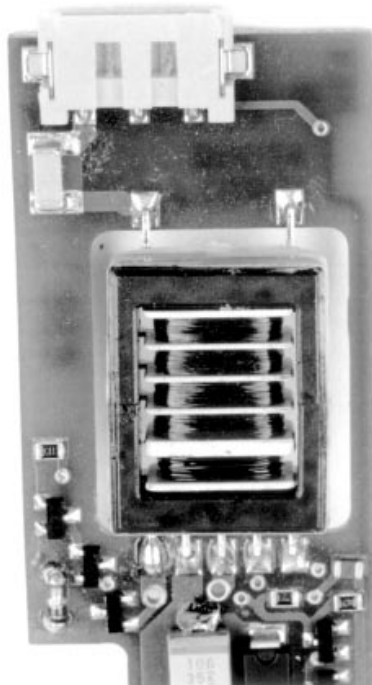
AN65-FG05

Figure G5. Transformer Output Terminals, Ballast Capacitor and Connector Are Isolated at End of Board. Slit Prevents Leakage



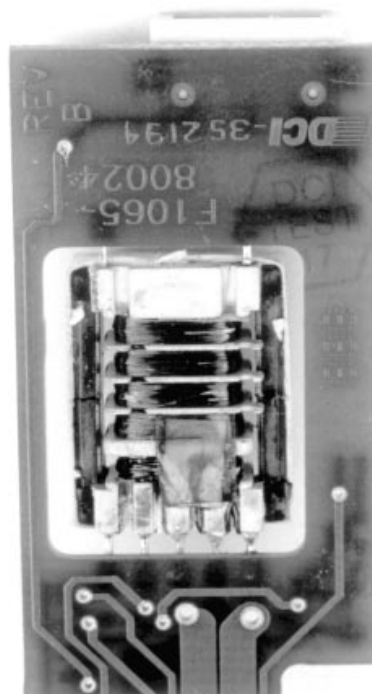
AN65-FG06

Figure G6. Reverse Side of G5. Note Routed Area under Transformer, Eliminating Possibility of Moisture or Contaminant Trappings



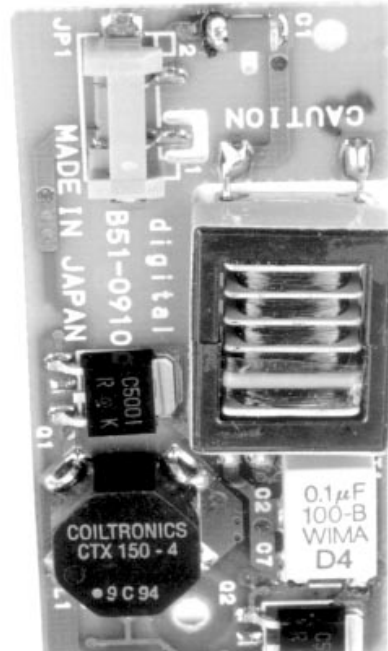
AN65-FG07

Figure G7. A Fully Routed Transformer, with High Voltage Capacitor Mounted Well Away from Transformer Ground Terminal (Right). Note Connector “Low Side” Trace Running Directly Away from High Voltage Points



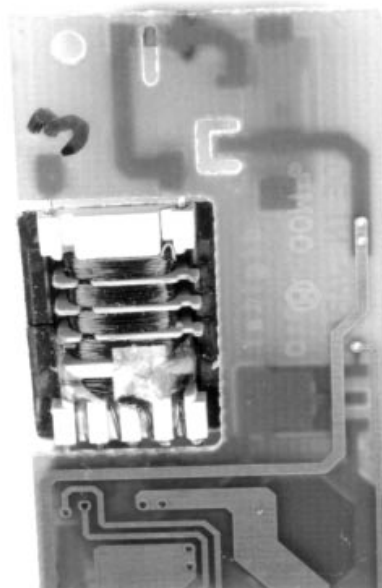
AN65-FG08

Figure G8. Routing Detail of Figure G7’s Reverse Side. Transformer Header Sits Inside Routed Area, Saving Height Space. Board Markings Are Allowable Because HV Contacts Do Not Plate Through and Board Dielectric Strength Is Known



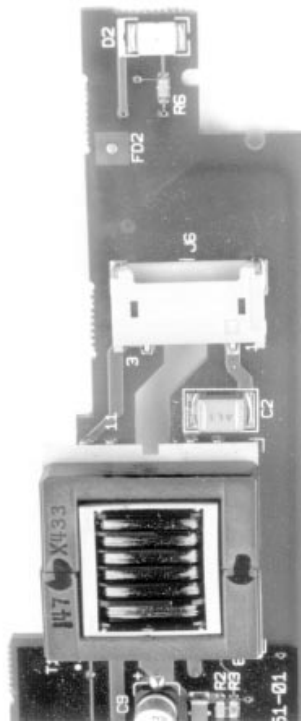
AN65-FG09

Figure G9. Very Thorough Routing Treatment Breaks Up Leakage. Routing Under Ballast Capacitor and Around Connector “Low Side” Pin Allows Tight Layout



AN65-FG10

Figure G10. Reverse Side of G9 Shows Offset Transformer Placement Necessitated by Packaging Restrictions. Transformer Header Sits in Routed Area, Minimizing Overall Board Height



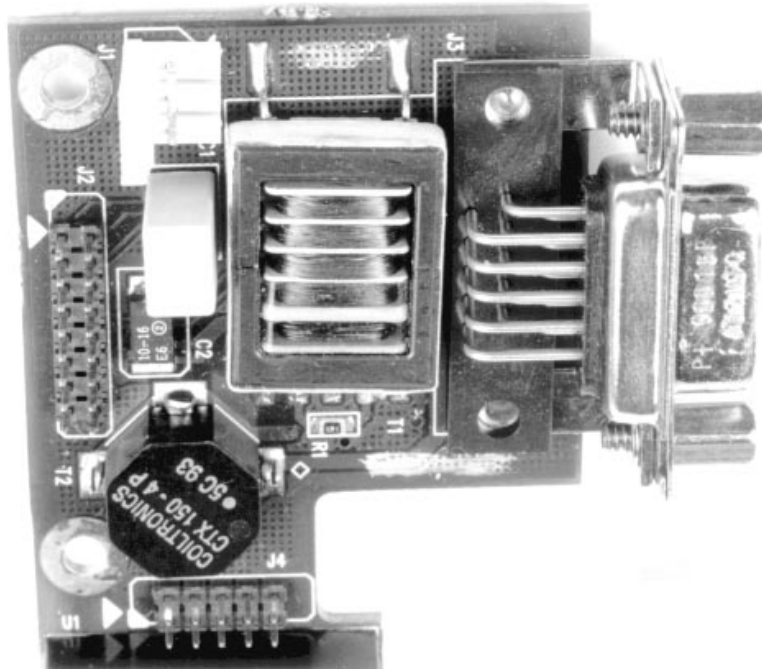
AN65FG11

Figure G11. Topside of Board Shows Isolation Slit Running to the HV Connector



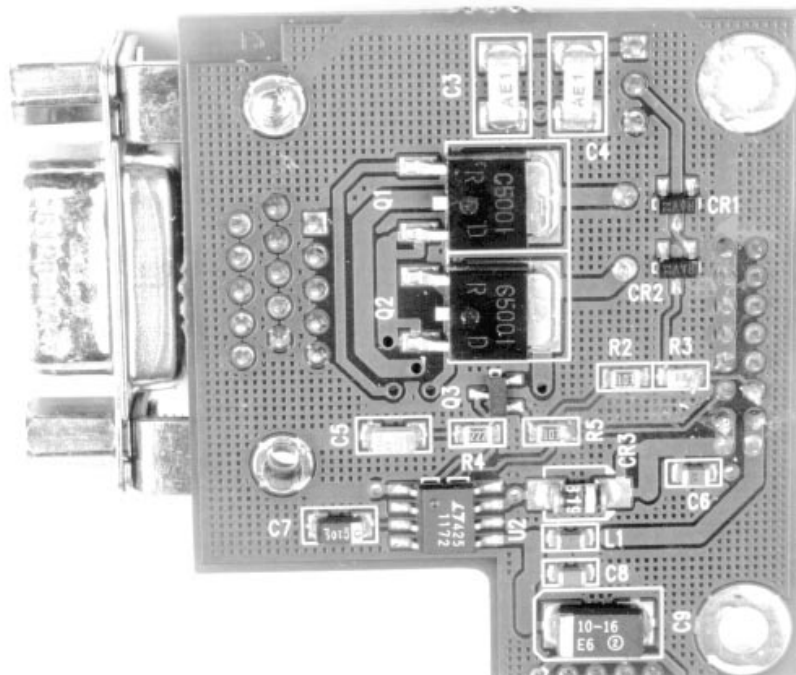
AN65FG12

Figure G12. Bottom of G11 Shows Routed Area. Traces at Board Extreme Left Are Undesirable but Acceptable. Isolation Slit Between Traces and HV Points Would Be Preferable



AN65-FG13

Figure G13. A Disaster. Cross-Hatched Ground Plane Surrounds Output Connector and High Voltage Transformer Pins (Upper Center) in This Computer “Aided” Layout. Board Failed Spectacularly at Turn-On



AN65-FG14

Figure G14. Bottom Side of G13. Ground Plane in Region of Paralleled Ballast Capacitors (Upper Center) Caused Massive Arcing at Turn-On. Board Needs Complete Re-Layout. Computer Layout Software Package Needs E and M Course

Application Note 65

Discrete Component Selection

Discrete component selection is quite critical to CCFL circuit performance. A poorly chosen dielectric for the collector resonating capacitor can easily degrade efficiency by 5% to 8%. The WIMA and Panasonic types specified are quite good and very few other capacitors perform as well. The Panasonic unit is the only surface mounting type recommended although about 1% more lossy than the “through-hole” WIMA.

The transistors specified are quite special. They feature extraordinary current gain and V_{CE} saturation specifications. The ZDT1048, a dual unit designed specifically for backlight service, saves space and is the preferred device. Figure G15 summarizes relevant characteristics. Substitution of standard devices can degrade efficiency by 10% to 20% and in some cases cause catastrophic failures.¹

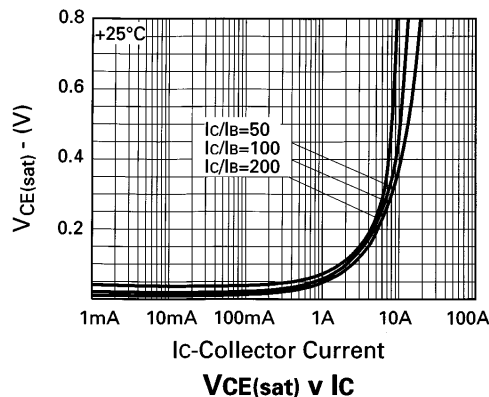
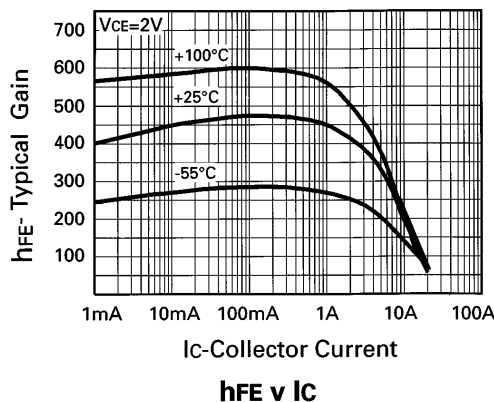
Note 1: Don't say we didn't warn you.

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
Collector-Emitter Breakdown Voltage	V_{CES}	50	85		V	$I_C=100\mu A$
Collector-Emitter Breakdown Voltage	V_{CEV}	50	85		V	$I_C=100\mu A, V_{EB}=1V$
Collector Cut-Off Current	I_{CBO}		0.3	10	nA	$V_{CB}=35V$
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$		27 55 120 200 250	45 75 160 240 350	mV	$I_C=0.5A, I_B=10mA^*$ $I_C=1A, I_B=10mA^*$ $I_C=2A, I_B=10mA^*$ $I_C=5A, I_B=100mA^*$ $I_C=5A, I_B=20mA^*$
Static Forward Current Transfer Ratio	h_{FE}	280 300 300 250 50	440 450 450 300 80	1200		$I_C=10mA, V_{CE}=2V^*$ $I_C=0.5A, V_{CE}=2V^*$ $I_C=1A, V_{CE}=2V^*$ $I_C=5A, V_{CE}=2V^*$ $I_C=20A, V_{CE}=2V^*$
Transition Frequency	f_T		150		MHz	$I_C=50mA, V_{CE}=10V$ $f=50MHz$

ZETEX
U.K. FAX: 0161627-5467
U.S. FAX: 5168647630
HONG KONG FAX: 987 9595

*Measured under pulsed conditions. Pulse width=300 μs . Duty cycle \leq 2%



Figures reproduced with permission of Zetex.

Figure G15. Short Form Specifications for Zetex ZDT1048 Dual Transistor. Extraordinary Beta and Saturation Characteristics Are Ideal for Royer Converter Section of Backlight Circuits

The following section, excerpted with permission from Zetex Application Note 14 (see Reference 28), reviews

Royer circuit operation with emphasis on transistor operating conditions and requirements.

Excerpted from "Transistor Considerations for LCD Backlighting," Neil Chadderton, Zetex plc.

Basic Operation Of Converter

The drive requirements dictated by the CCFL tube's behaviour and preferred operating conditions can be achieved by the resonant push-pull converter shown in Figure G16. This is also referred to as the Royer Converter, after G.H. Royer who proposed the topology in 1954 as a power converter. (Note: Strictly speaking the backlighting converter uses a modified version of the Royer converter – the original used a saturating transformer to fix the operating frequency, and therefore produced a squarewave drive waveform). The circuit looks simple but this is very deceptive: many components interact, and while the circuit is capable of operation with widely varying component values, (useful during development) optimisation is required for each design to achieve the highest possible efficiencies.

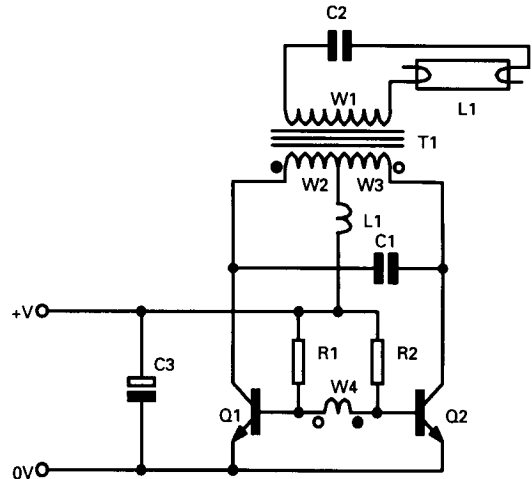


Figure G16. Generalised Royer Converter.

Transistors Q1 and Q2 are alternatively saturated by the base drive provided by the feedback winding W4. The base current is defined by resistors R1 and R2. Supply inductor L1 and primary capacitance C1 force the circuit to run sinusoidally thereby minimising harmonic generation and RFI, and providing the preferred drive waveform to the load. Voltage step-up is achieved by the $W1:(W2+W3)$ turns ratio. C2 is the secondary winding ballast capacitor, and effectively sets the tube current.

Prior to the tube striking, or when no tube is connected, the operating frequency is set by the resonant parallel circuit comprising the primary capacitance C1, and the transformer's primary winding $W2+W3$. Once the tube has struck, the ballast capacitor C2 plus distributed tube and parasitic capacitances are reflected back through the transformer, and the operating frequency is lowered.

The secondary load can become dominant in circuits with a high transformer turns ratio, Eg. those designed to operate from very low DC input voltages.

Each transistor's collector is subject to a voltage = $2 \times \pi/2 \times V_s$, (or just $\pi \times V_s$) where V_s is the DC input voltage to the converter. (The $\pi/2$ factor being due to the relationship between average and peak values for a sinewave, and the x2 multiplier being due to the 2:1 autotransformer action of the transformer's centre-tapped primary). This primary voltage is stepped up by the transformer turns ratio $N_s:N_p$, to a high enough level to reliably strike the tube under all conditions:- starting voltage is dependent on display housing, location of ground planes, tube age, and ambient temperature.

Application Note 65

The basic converter shown in Figure G16 is a valid and useful circuit that has been utilised for many systems and indeed offered as a sub-system by several manufacturers.

Requisite Transistor Characteristics

The relatively low operating frequency as required by the backlighting Royer Converter (to minimise HV parasitic capacitance losses), and the ease of transformer drive, makes this circuit particularly suitable for bipolar transistor implementation. This isn't to exclude MOSFET based designs (some IC vendors have specified MOS as this suits their technology) but in terms of equivalent on-resistance and silicon efficiency, the low voltage bipolar device has no equal. For example, the ZETEX ZTX849 E-LINE (TO-92 compatible) transistor exhibits a $R_{CE(sat)}$ of $36m\Omega$. This can only be matched by a much larger (and expensive) MOSFET die, only available in TO-220, D-PAK, and similar larger packages.

The most important transistor characteristics are voltage rating, $V_{CE(sat)}$, and h_{FE} , and are considered in some detail below.

The voltage rating required deserves some thought with respect to the standard transistor breakdown parameters, as it is possible to over-specify a device on grounds of voltage rating, and thereby incur a reduction in efficiency due to unnecessary on-resistance losses. The primary breakdown voltage BV_{CBO} , of a planar bipolar transistor depends on the epitaxial layer - specifically it's thickness and resistivity. The breakdown voltage of most interest to the designer is usually that attained across the Collector-Emitter (C-E) terminals. This value can vary between the primary breakdown BV_{CBO} and a much lower voltage dependent on the state of the base terminal bias.

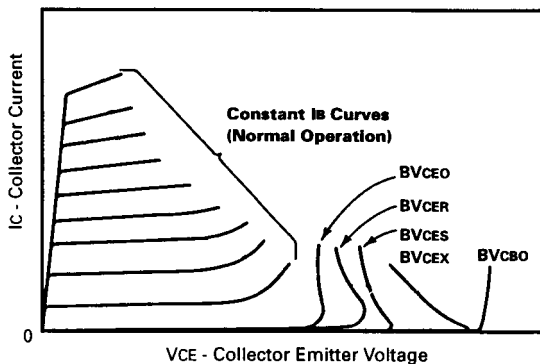


Figure G17. Voltage Breakdown Modes of Bipolar

[The breakdown mechanism is caused by the avalanche multiplication effect, whereby free electrons can be imparted with sufficient energy by the reverse bias electric field such that any collisions can lead to ionisation of the lattice atoms. The free electrons thus generated are then accelerated by the field and produce further ionisation. This multiplication of free carriers increases the reverse current dramatically, and so the junction effectively clamps the applied voltage. The base terminal can obviously influence the junction current – thereby modulating the voltage required for a breakdown condition.]

Figure G17 shows how the breakdown characteristic is seen to vary for different circuit conditions. The BV_{CEO} rating (or when the base is open circuit) allows the Collector-Base (C-B) leakage current I_{CBO} to be effectively amplified by the transistor's β thus significantly increasing the leakage component to I_{CEO} . Shorting the base to the Emitter (BV_{CES}) provides a parallel path for the C-B leakage, and so the voltage required for breakdown is higher than the open base condition. BV_{CER} denotes the case between the open and shorted base options:- R indicating an external base-emitter resistance, the value of which is typically 100 to 10k Ω . BV_{CEV} or BV_{CEX} is a special case where the base-emitter is reverse biased; this can provide a better path for the C-B leakage, and so this rating yields a voltage close to, or coincident with the BV_{CBO} value. Figure G18 shows a curve tracer view of the relevant breakdown modes of the ZTX849 transistor, including a curve showing the device in the "on" state. Curves 1 and 2 are virtually coincident and show BV_{CBO} and BV_{CES} respectively. Curve 3 shows the BV_{CEV} case with an applied base bias (V_{EB}) of -1V. Curve 4 shows BV_{CEO} at approximately 36V. Curve 5 is a BV_{CE} curve, showing how the breakdown condition is affected by a positive base bias of 0.5V.

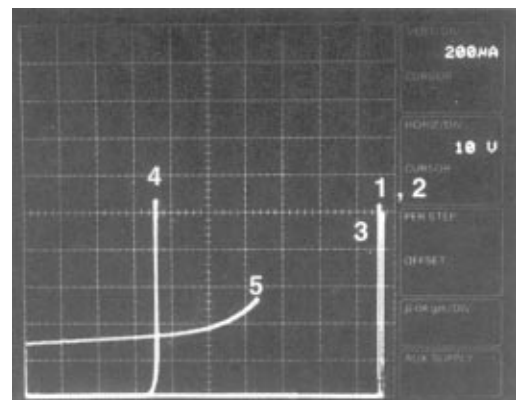


Figure G18. Breakdown Modes of ZTX849.

The BV_{CEV} rating has particular relevance to the Royer Converter, as can be surmised from Figure 19. Examination of this will show that the transistor only experiences the high C-E voltage when the base voltage has been taken negative by the feedback winding, these events of course being in perfect synchronism. An expanded view of the C-E and B-E waveforms is shown in Figure G20.

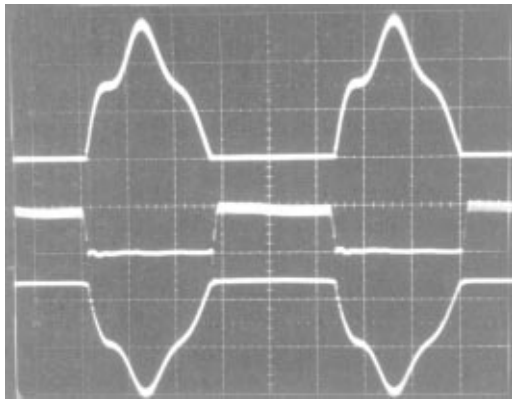


Figure G19. Royer Converter Operating Waveforms:
 V_{CE} 10V/div; I_E 0.5A/div; V_{BE} 2V/div respectively,
 2 μ s/div horizontal

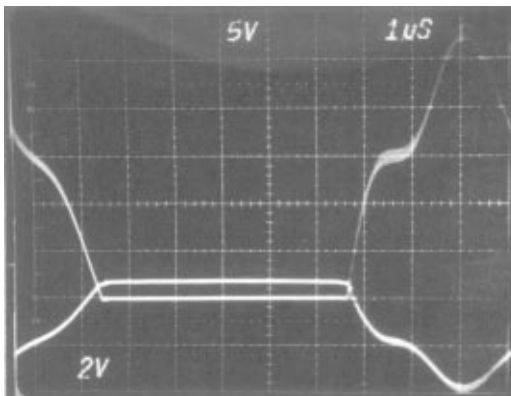


Figure G20. Royer Converter: V_{CE} and V_{BE}
 Waveforms; 5V/div and 2V/div respectively.

[Note: The voltage applied by the feedback winding must not exceed the BV_{EBO} of the transistor. This is specified at 5V usually, against an actual of 7.5 to 8.5V].

The $V_{CE(sat)}$ and h_{FE} parameters have a direct bearing on the circuit's electrical conversion efficiency. This is especially true of low voltage battery powered systems, due to the high current levels involved. Selection of standard LF amplifier transistors provides far from ideal results; these parts are for general

purpose linear and non-critical switching use only. The high $V_{CE(sat)}$ inherent to these parts, and low current gain could reduce circuit efficiency to less than 50%. For example, the stated $V_{CE(sat)}$ maximum measured at 500mA, for the FZT849 SOT223 transistor, and a LF device sometimes quoted as a suitable Royer Converter transistor are 50mV and 0.5V respectively. Eg.

	$V_{CE(sat)}$	@ I_C	I_b
FZT849	50mV	0.5A	20mA
BCP56	0.5V	0.5A	50mA

To address the $V_{CE(sat)}$ issue, large power transistors are occasionally specified. Unfortunately their capacitance, and characteristic low base transport factor (a feature of Epitaxial Base devices) can lead to problems with cross-conduction losses due to long storage and switching times. The current gain is also important, as the losses in the base bias can be significant to the overall figure; judicious selection of the bias resistor to ensure a minimum $V_{CE(sat)}$ while preventing base overdrive needs to consider supply variation, maximum lamp current, and transistor h_{FE} minimum value and range.

For the above reasons, transistors designed and optimised for high current switching applications offer the most cost-effective and efficient solutions. Figure G21 shows the $V_{CE(sat)}$ exhibited by the ZTX1048A for a range of forced gain values. This device is one of the ZTX1050 series of transistors that employ a scaled up variant of the highly efficient Matrix geometry, developed for the ZETEX "Super-SOT" series. This enables a $V_{CE(sat)}$ performance similar to the ZTX850 series at the low to moderate currents relevant to this application, though utilising a smaller die, and therefore providing a cost and possibly a space saving advantage.

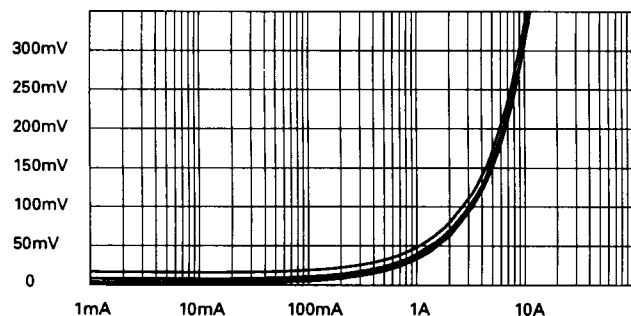


Figure G21. $V_{CE(sat)}$ v I_C for the ZTX1048A
 Forced gains of 10,20,50,100.

Application Note 65

Additional Discrete Component Considerations

The magnetics specified have also been carefully selected and substitution can lead to problems ranging from poor efficiency to bad line regulation.

Bypass capacitors can be any type specified for switching regulator service, although tantalum types should be avoided for Royer bypassing if the supply is capable of delivering high current. As of this writing no tantalum supplier can guarantee reliability in the face of high current turn-on. If tantalums must be used, an X2 voltage derating factor *must* be enforced.²

The 2.2 μ F Royer bypass value used in LT118X-based circuits has been selected to ensure against any possible long-term damage to the IC's internal current shunt. Turn-on current surges can be large and this value limits them to safe excursions.

The high speed catch diode associated with the V_{SW} pin should be capable of handling the fast current spikes

encountered. Schottky types offer lower loss than regular high speed units.³

Emissions

There are rarely emission problems with the CCFL circuits. The Royer circuit's resonant operation minimizes radiated energy at frequencies of interest. There is often more RF energy associated with the switching regulators V_{SW} node and minimizing exposed trace area eliminates problems. Incidental radiation from magnetics is reasonably low. Some (relatively rare) cases require consideration of magnetics placement to prevent interaction with other circuitry. If shielding is required its effects should be evaluated early in the design. Shielding in the vicinity of the Royer transformer can cause effects ranging from changing the inverter resonance to secondary arcing.

Note 2: See Footnote 1. Read it twice.

Note 3: Discussing utilization of 60Hz rectifier diodes (e.g., 1N4002) in this application qualifies as obscene literature. See also Footnote 1.

APPENDIX H

LT1172 OPERATION FROM HIGH VOLTAGE INPUTS

Some applications require higher input voltages. The 20V maximum input specified in the figures is set by the LT1172 going into its isolated flyback mode (see LT1172 data sheet), not breakdown limits. If the LT1172 V_{IN} pin is driven from a low voltage source (e.g., 5V) the 20V limit may be extended by using Figure H1's network. If the LT1172 is driven from the same supply as L1's center tap, the network is unnecessary, although efficiency will suffer. No other switching regulator discussed in the text is subject to this issue. Their operating voltage is set solely by voltage breakdown limits.

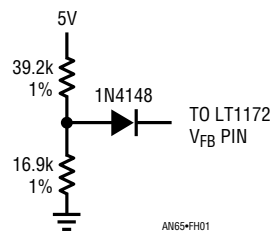


Figure H1. Network Allows LT1172 Operation Beyond 20V Inputs

APPENDIX I

ADDITIONAL CIRCUITS

Desktop Computer CCFL Power Supply

Desktop computers, being line operated, can support higher power displays. High power operation permits high luminosity, enlarged display area or both. Typically, desktop displays absorb 4W to 6W and run from a relatively high voltage, regulated supply. Figure I1 shows such a

display. This “grounded lamp” LT1184-based configuration, similar to previously described versions, requires little comment. The transformer is a high power type, and scaling of the “ I_{CCFL} ” current programming resistors allows 9mA lamp current. In this case programming is via clamped PWM (see Appendix F), although all other methods described are feasible.

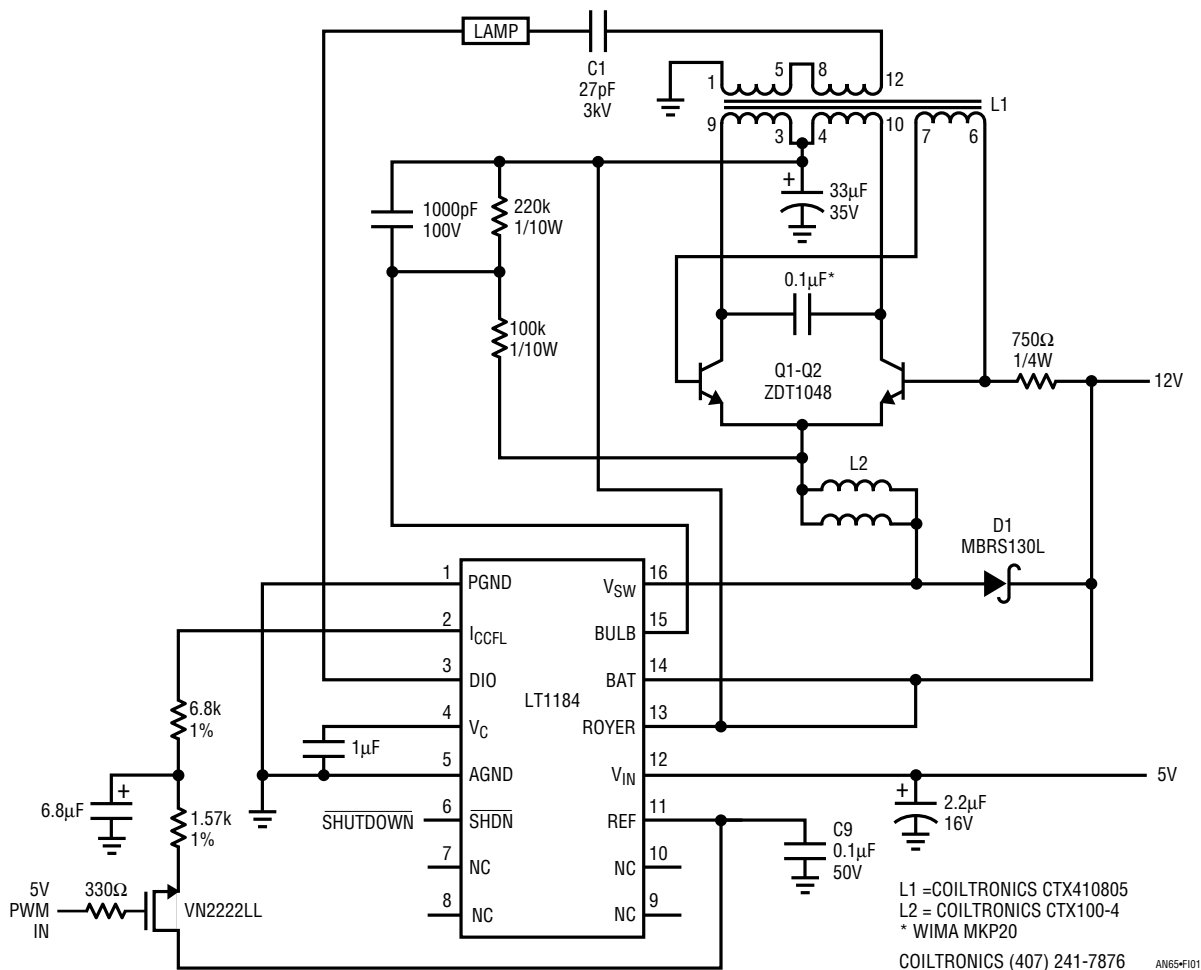


Figure I1. High Power Transformer and Scaled I_{CCFL} Values Permit Desktop Computer LCD Operation

Application Note 65

Dual Transformer CCFL Power Supply

Space constraints may dictate utilization of two small transformers instead of a single, larger unit. Although this approach is somewhat more expensive, it can solve space problems and offers other attractive advantages. Figure 12's approach is essentially a "grounded lamp" LT1184-based circuit. The transistors drive two transformer primaries in parallel. The transformer secondaries, stacked in series, provide the output. The relatively small transformers, each supplying half the load power, may be located directly at the lamp terminals. Aside from the obvious space advantage (particularly height), this arrangement minimizes parasitic wiring losses by eliminating high

voltage lead length. Additionally, although the lamp receives differential drive, with its attendant low parasitic losses, the feedback signal is ground referred. Thus, the stacked secondaries afford floating lamp operation efficiency with grounded mode current certainty and line regulation.

L1 is directly driven, with winding 4-5 furnishing feedback in the normal fashion. L3, "slaved" to L1, produces phase-opposed output at its secondary. L1's and L3's interconnects must be laid out for low inductance to maintain waveform purity. The traces should be as wide as possible (e.g., 1/8") and overlaid to cancel inductive effects.

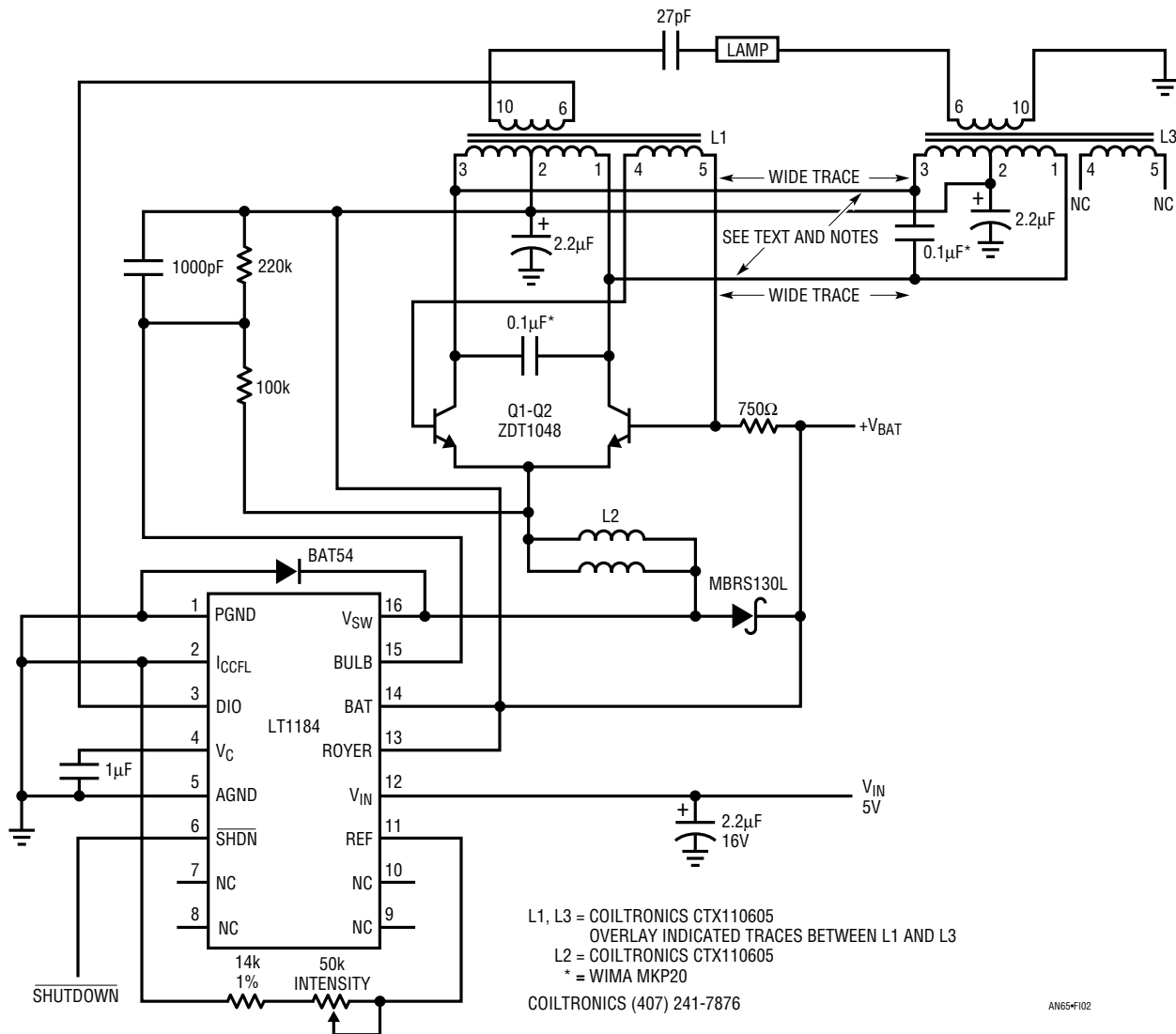


Figure 12. Dual Transformers Save Space and Minimize Parasitic Losses While Maintaining Current Accuracy and Line Regulation. Trade-Off Is Increased Cost

HeNe Laser Power Supply

Helium-neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10kV to start conduction, although they require only about 1500V to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure 13's circuit considerably simplifies driving the laser. The start-up and sustaining functions have been combined into a single closed-loop current source with over 10kV of compliance. The circuit is recognizable as a reworked CCFL power supply with a voltage tripled DC output.

When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its Switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47μF capacitor resonates with L1, providing boosted sine wave drive. L1 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10kV across the laser. The laser breaks down and current begins to flow through it. The 47k

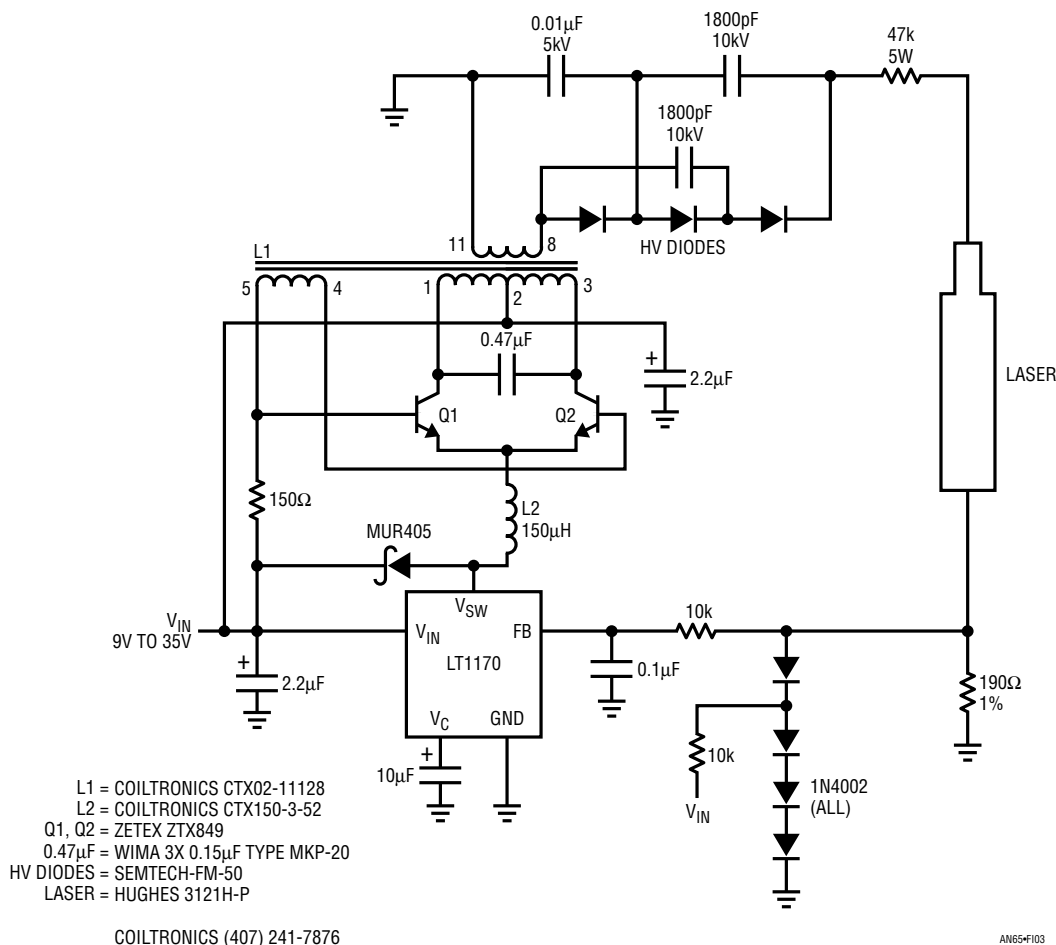


Figure 13. Laser Power Supply, Based on the CCFL Circuit, Is Essentially a 10,000V Compliance Current Source

Application Note 65

resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts pulse width drive to L2 to maintain the FB pin at 1.23V, regardless of changes in operating conditions. In this fashion, the laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by

varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The $10\mu\text{F}$ capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9V to 35V input range with an electrical efficiency of about 80%.

APPENDIX J

LCD CONTRAST CIRCUITS

LCD panels require variable output contrast control circuits. Contrast power supplies of various capabilities are presented here.

Figure J1 is a contrast supply for LCD panels. It was designed by Steve Pietkiewicz of LTC. The circuit is noteworthy because it operates from a 1.8V to 6V input, significantly lower than most designs. In operation the LT1300/LT1301 switching regulator drives T1 in flyback fashion, causing negative biased step-up at T1's second-

ary. D1 provides rectification, and C1 smooths the output to DC. The resistively divided output is compared to a command input, which may be DC or PWM, by the IC's I_{LIM} pin. The IC, forcing the loop to maintain 0V at the I_{LIM} pin, regulates circuit output in proportion to the command input.

Efficiency ranges from 77% to 83% as supply voltage varies from 1.8V to 3V. At the same supply limits, available output current increases from 12mA to 25mA.

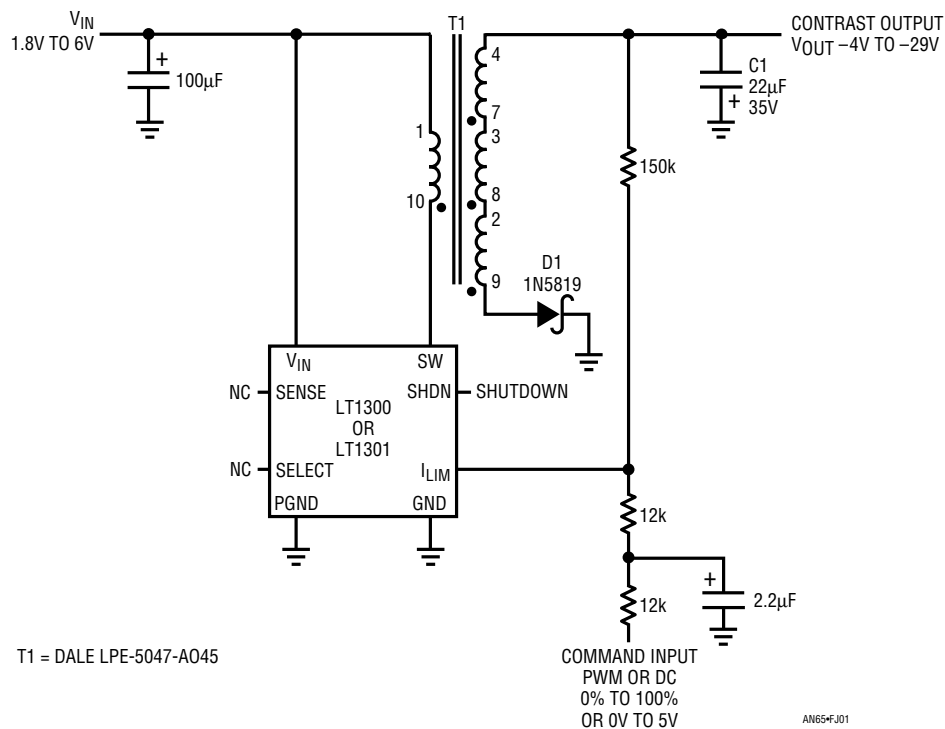


Figure J1. Liquid Crystal Display Contrast Supply Operates from 1.8V to 6V with -4V to -29V Output Range

Another LCD bias generator, also developed by Steve Pietkiewicz of LTC, is shown in Figure J2. In this circuit U1 is an LT1173 micropower DC/DC converter. The 3V input is converted to 24V by U1's switch, L2, D1 and C1. The Switch pin SW1 also drives a charge pump composed of C2, C3, D2 and D3 to generate -24V. Line regulation is less than 0.2% from 3.3V to 2V inputs. Load regulation, although suffering somewhat since the -24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2V input at 75% efficiency.

If greater output power is required, Figure J2's circuit can be driven from a 5V source. R1 should be changed to 47Ω and C3 to 47μF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing D4's anode to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage. Shutdown current is 110μA from the input source and 36μA from the shutdown signal.

Dual Output LCD Bias Voltage Generator

The many different kinds of LCDs available make programming LCD bias voltage at the time of manufacture attrac-

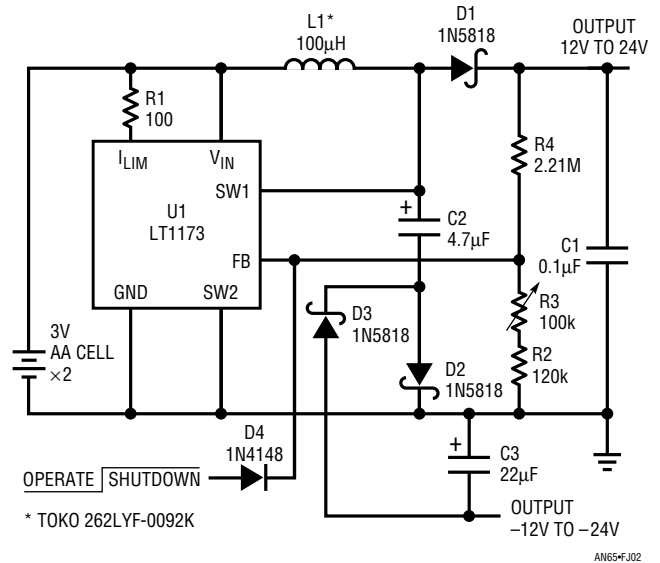


Figure J2. DC/DC Converter Generates LCD Bias from 3V Supply

tive. Figure J3's circuit, developed by Jon Dutra of LTC, is an AC-coupled boost topology. The feedback signal is derived separately from the outputs, so loading does not affect loop compensation, although load regulation is somewhat compromised. With 28V out, from 10% to 100% load (4mA to 40mA), the output voltage sags about

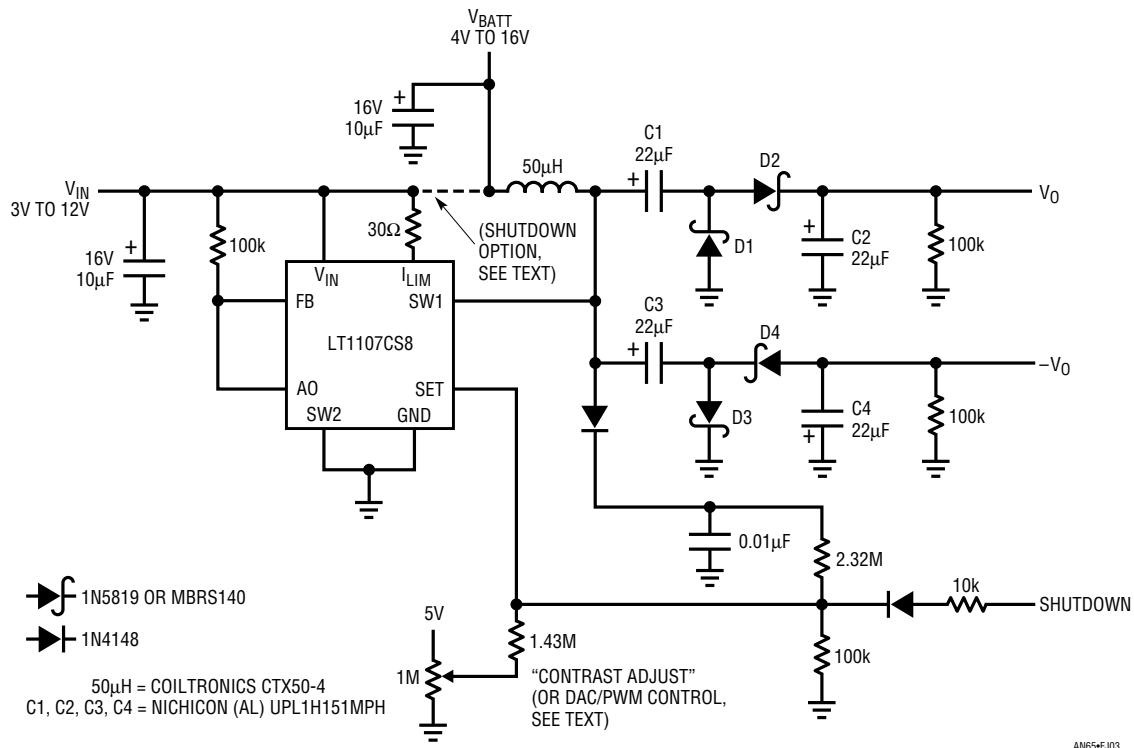


Figure J3. Dual Output LCD Bias Voltage Generator

Application Note 65

0.65V. From 1mA to 40mA load the output voltage drops about 1.4V. This is acceptable for most displays.

Output noise is reduced by using the auxiliary gain block within the LT1107 (see LT1107 data sheet) in the feedback path. This added gain effectively reduces comparator hysteresis and tends to randomize output noise. Output noise is below 30mV over the output load range. Output power increases with V_{BATT} , from about 1.4W with $5V_{IN}$ to about 2W with 8V or more. Efficiency is 80% over a broad output power range. If only a positive or negative output voltage is required, the diodes and capacitors associated with the unused output can be eliminated. The 100k resistor is required on each output to load a parasitic voltage doubler created by D2/D4 shunt capacitance. Without this minimum load, the output voltage can rise to unacceptable levels.

The voltage at the Switch pin SW1 swings from 0V to V_{OUT} plus 2 diode drops. This voltage is AC-coupled to the positive output through C1 and D1, and to the negative output through C3 and D3. C1 and C3 have the full RMS output current flowing through them. Most tantalum capacitors are not rated for current flow. Use of a rated tantalum or electrolytic is recommended for reliability. At lower output currents monolithic ceramics are also an option.

The circuit may be shut down in several ways. The easiest is to pull the Set pin above 1.25V. This approach consumes 200 μ A in shutdown. A lower power method is to turn off V_{IN} to the LT1107 by a high side switch or simply disable the input supply (see option in schematic). This

drops quiescent current from the V_{BATT} input below 10 μ A. In both cases V_{OUT} drops to 0V. In the event $+V_{OUT}$ does not need to drop to zero, C1 and D1 can be eliminated. The output voltage can be adjusted from any voltage above V_{BATT} to 46V. Output voltage can be controlled by the user with DAC, PWM or potentiometer control. Summing currents into the feedback node allows downward adjustment of output voltage.

LT118X Series Contrast Supplies

Some LT118X series parts include a contrast supply based on a boost regulator. Figure J4 shows a basic positive output circuit. The V_{SW} -driven inductor provides voltage step-up with D5 and C11 rectifying and filtering the output to DC. The R12/R14 divider chain sets feedback ratio and hence output voltage. The connection to the LT1182 Feedback pin closes a control loop with R7 and C8 providing frequency compensation.

Figure J5 is similar, except that it uses charge pump techniques to reduce shutdown current. D4 and C12 are placed in L3's discharge path, AC coupling it to the output. In shutdown, no DC current can flow through L3, reducing battery drain over J4's DC-coupled approach.

Figure J6's transformer-fed output provides negative output voltages with the LT1183's "FBN" pin directly accepting the resultant negatively biased feedback signal. No level shift is required. In this case output voltage is set by a voltage control input, although potentiometer or PWM inputs could be accommodated (see Appendix F). D3 and D2 damp L3 flyback amplitude to safe levels and the

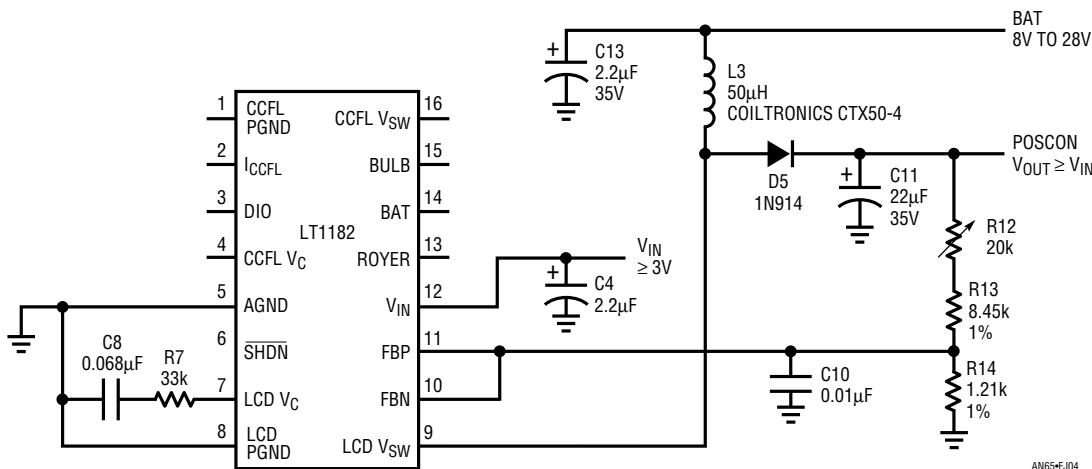
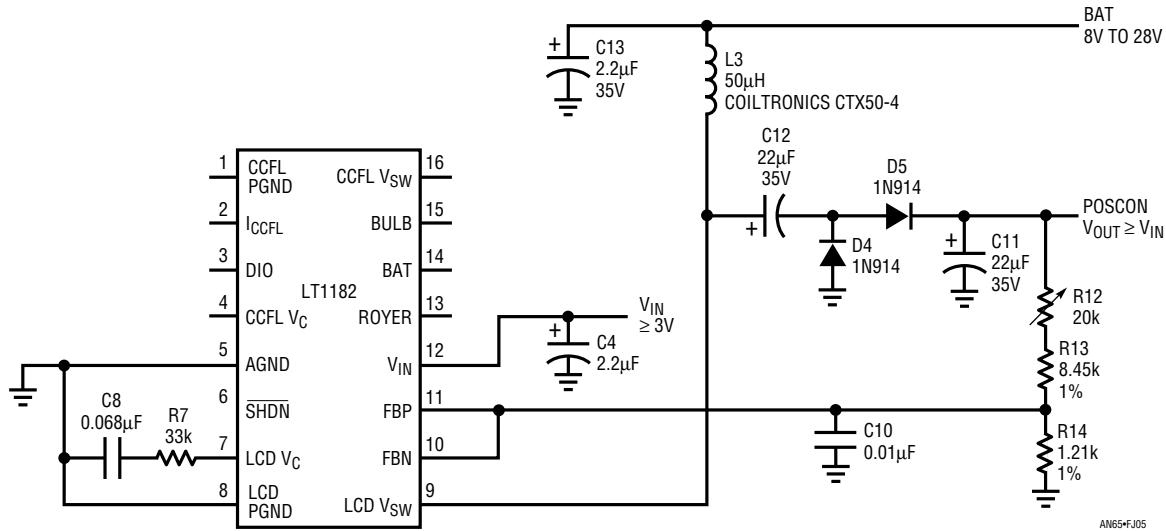
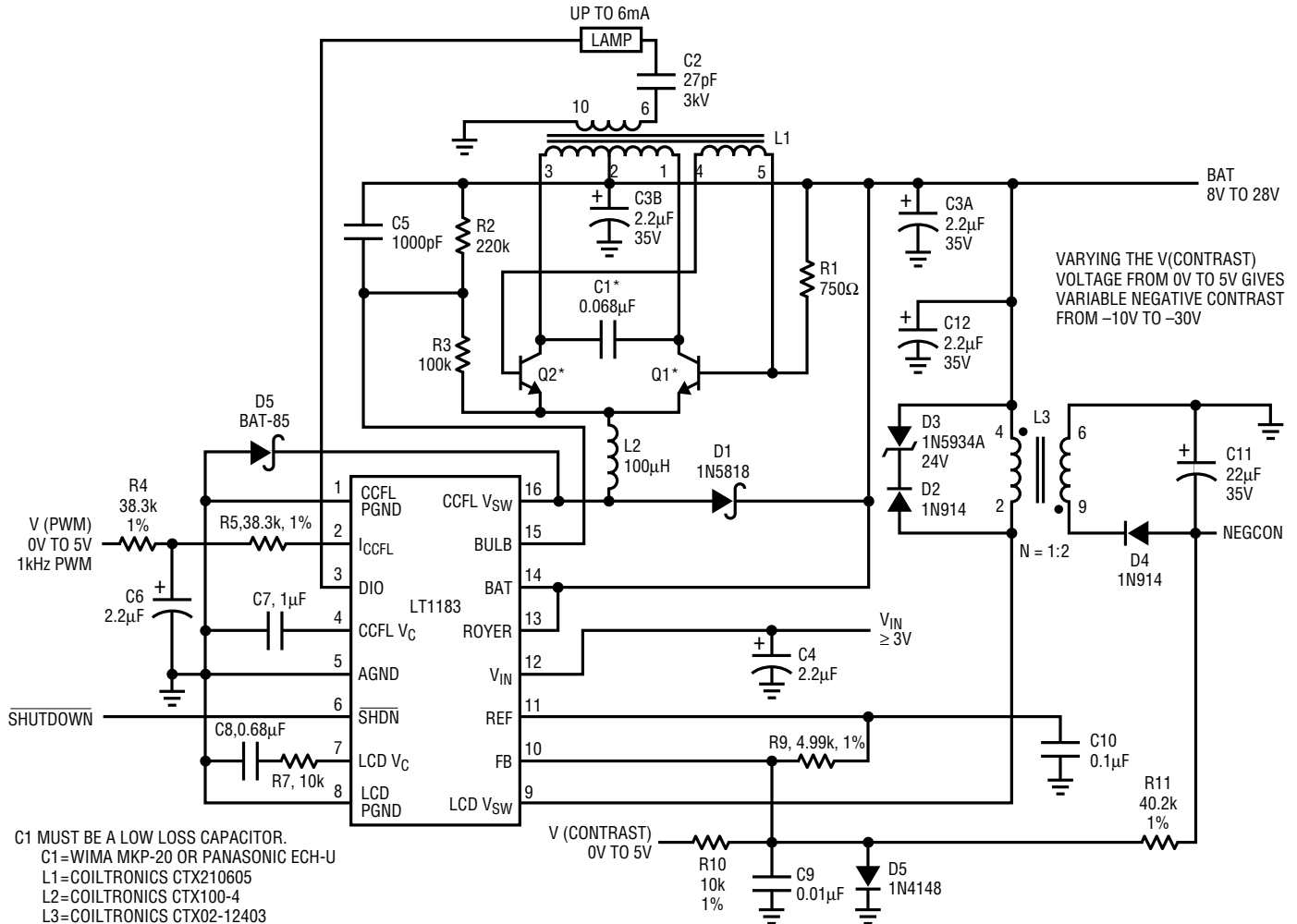


Figure J4. LT1182 LCD Contrast Positive Boost Converter. CCFL Circuitry Is Omitted for Clarity



AN65-FJ05

Figure J5. LT1182 LCD Contrast Positive Boost/Charge Pump Converter Reduces Battery Current in Shutdown



C1 MUST BE A LOW LOSS CAPACITOR.

C1=WIMA MKP-20 OR PANASONIC ECH-U

L1=COILTRONICS CTX210605

L2=COILTRONICS CTX100-4

L3=COILTRONICS CTX02-12403

Q1, Q2=ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001

***DO NOT SUBSTITUTE COMPONENTS**

COILTRONICS (407) 241-7876

AN65-FJ06

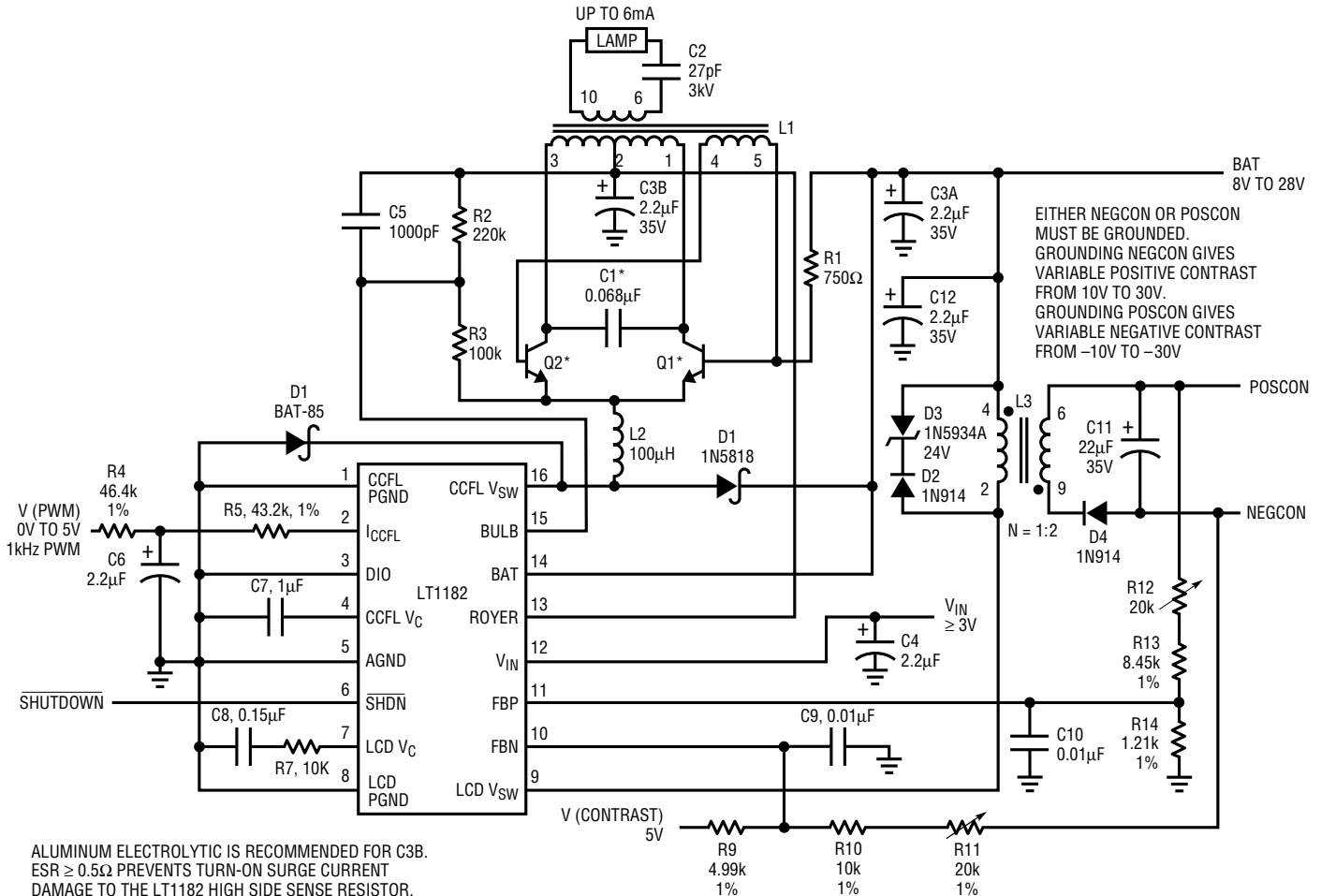
Figure J6. LT1183 Grounded Lamp CCFL Circuit with Negative Output LCD Contrast Supply

Application Note 65

isolated secondary permits low shutdown current compared to a simple inductor-based circuit.

Figure J7 takes advantage of the LT1182's bipolar feedback inputs to provide selectable output polarity. This scheme permits the same circuit to be used with LCD's requiring either positive or negative bias. This can be a

significant advantage in volume production involving different LCD panels. In operation the circuit is similar to Figure J6, except that L3's secondary winding feeds two separate feedback paths. Output polarity is selected by simply grounding the appropriate L3 secondary terminal.



ALUMINUM ELECTROLYTIC IS RECOMMENDED FOR C3B.
ESR ≥ 0.5Ω PREVENTS TURN-ON SURGE CURRENT DAMAGE TO THE LT1182 HIGH SIDE SENSE RESISTOR.
C1 MUST BE A LOW LOSS CAPACITOR.
C1 = WIMA MKP-20, PANASONIC ECH-U
L1 = COILTRONICS CTX210605
L2 = COILTRONICS CTX100-4
L3 = COILTRONICS CTX02-12403
Q1, Q2 = ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
***DO NOT SUBSTITUTE COMPONENTS**
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AN65-FJ07

Figure J7. LT1182 Floating Lamp CCFL Circuit with Positive or Negative LCD Contrast Supply

APPENDIX K

WHO WAS ROYER AND WHAT DID HE DESIGN?

In December 1954 the paper “Transistors as On-Off Switches in Saturable-Core Circuits” appeared in *Electrical Manufacturing*. George H. Royer, one of the authors, described a “d-c to a-c converter” as part of this paper. Using Westinghouse 2N74 transistors, Royer reported 90% efficiency for his circuit. The operation of Royer’s circuit is well-described in this paper. The Royer converter was widely adopted and used in designs from watts to kilowatts. It is still the basis for a wide variety of power conversion.

Royer’s circuit is not an LC resonant type. The transformer is the sole energy storage element and the output is a square wave. Figure K1 is a conceptual schematic of a typical converter. The input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure K2, Traces A and C are Q1’s collector and base, while Traces B and D are Q2’s collector and base) each time the transformer saturates. Transformer saturation causes a quickly rising, high current to flow (Trace E).

This current spike, picked up by the base drive winding, switches the transistors. This phase opposed switching causes the transistors to exchange states. Current abruptly drops in the formerly conducting transistor and then slowly rises in the newly conducting transistor until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%.

Figure K3 is a time and amplitude expansion of K2’s Traces B and E. It clearly shows the relationship between transformer current (Trace B, Figure K3) and transistor collector voltage (Trace A, Figure K3).¹

Note 1: The bottom traces in both photographs are not germane and are not referenced in the discussion.

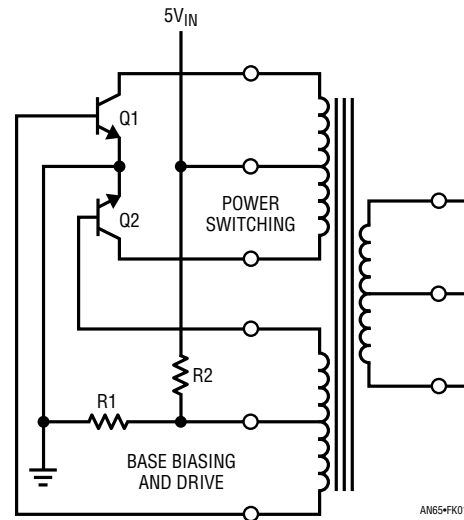


Figure K1. Conceptual Classic Royer Converter. Transformer Approaching Saturation Causes Switching

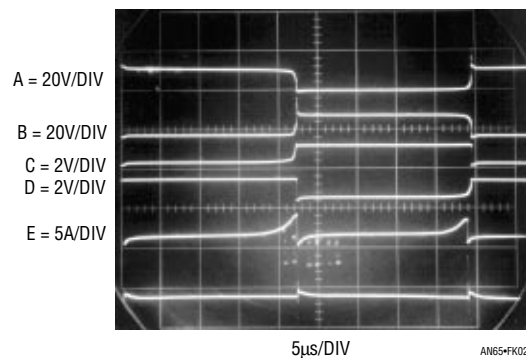


Figure K2. Waveforms for the Classic Royer Circuit

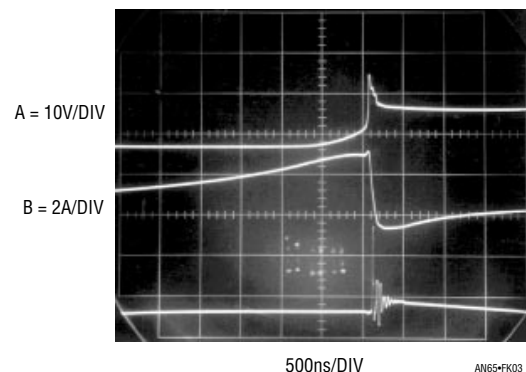


Figure K3. Detail of Transistor Switching. Turn-Off (Trace A) Occurs Just as Transformer Heads into Saturation (Trace B)

Application Note 65

APPENDIX L

A LOT OF CUT OFF EARS AND NO VAN GOGHS

Some Not-So-Great Ideas

The hunt for a practical, broadly applicable and easily utilized CCFL power supply covered (and is still covering) a lot of territory. The wide range of conflicting requirements combined with ill-defined lamp characteristics produces plenty of unpleasant surprises. This section presents a selection of ideas that turned into disappointing breadboards. Backlight circuits are one of the deadliest places the author has ever encountered for theoretically interesting circuits.

Not-So-Great Backlight Circuits

Figure L1 seeks to boost efficiency by eliminating the LT1172's saturation loss. Comparator C1 controls a free running loop around the Royer by on-off modulation of transistor base drive. The circuit delivers bursts of high

voltage sine drive to the lamp to maintain the feedback node. The scheme worked, but had poor line rejection due to the varying waveform vs supply seen by the RC averaging pair. Also, the "burst" modulation forces the loop to constantly restart the lamp at the burst rate, wasting energy. Finally, lamp power is delivered by a high crest factor waveform, causing inefficient current-to-light conversion in the lamp and shortening its life.

Figure L2 attempts to deal with some of these issues. It converts the previous circuit to an amplifier-controlled current mode regulator. Also, the Royer base drive is controlled by a clocked, high frequency pulse width modulator. This arrangement provides a more regular waveform to the averaging RC, improving line rejection. Unfortunately, the improvement was not adequate. To

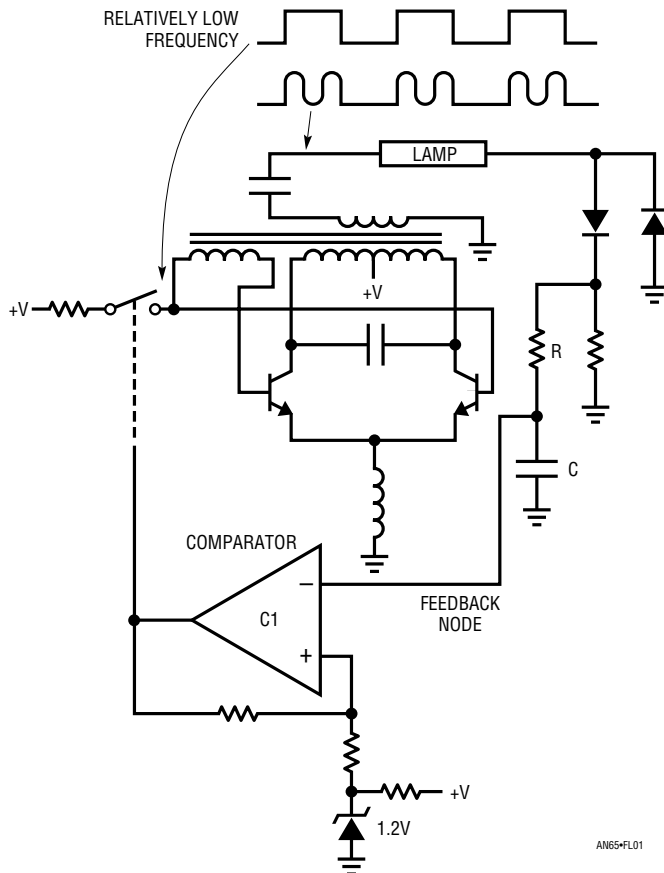


Figure L1. A First Attempt at Improving the Basic Circuit. Irregular Royer Drive Promotes Losses and Poor Regulation

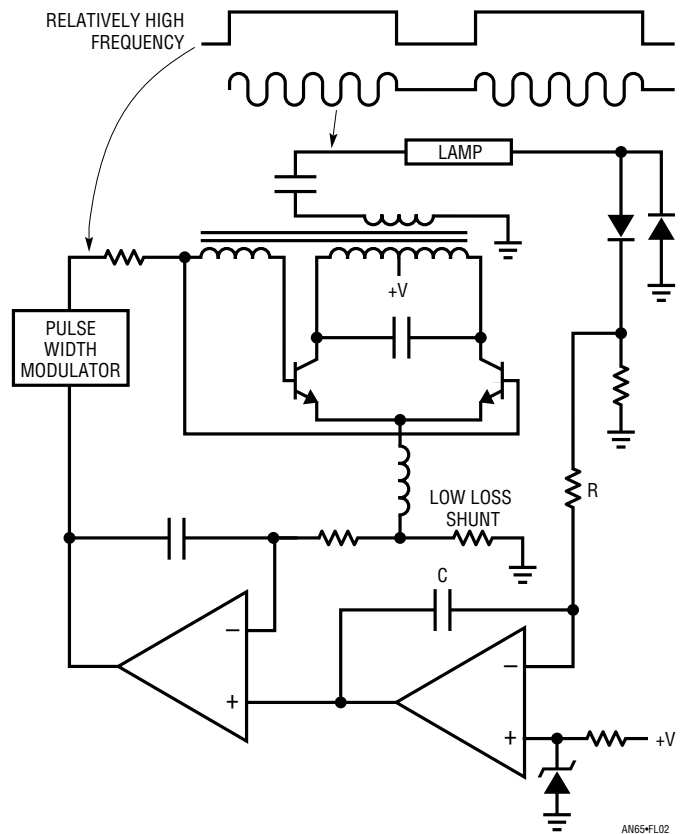


Figure L2. A More Sophisticated Failure Still Has Losses and Poor Line Regulation

avoid annoying flicker, 1% line rejection is required when the line moves abruptly, such as when a charger is activated. Another difficulty is that, although reduced by the higher frequency PWM, crest factor is still nonoptimal with respect to lamp emissivity and life. Finally, the lamp is still forced to restart at each PWM cycle, wasting power.

Figure L3 adds a “keep alive” function to prevent the Royer from turning off. This aspect worked well. When the PWM goes low the Royer is kept running, maintaining low level lamp conduction. This eliminates the continuous lamp

restarting, saving power. The “supply correction” block feeds a portion of the supply into the RC averager, improving line rejection to acceptable levels.

This circuit, after considerable fiddling, achieved almost 94% efficiency but produced less output light than a “less efficient” version of text Figure 35! The villain is lamp waveform crest factor. The keep alive circuit helps, but the lamp still cannot handle even moderate crest factors and lamp lifetime is still questionable.

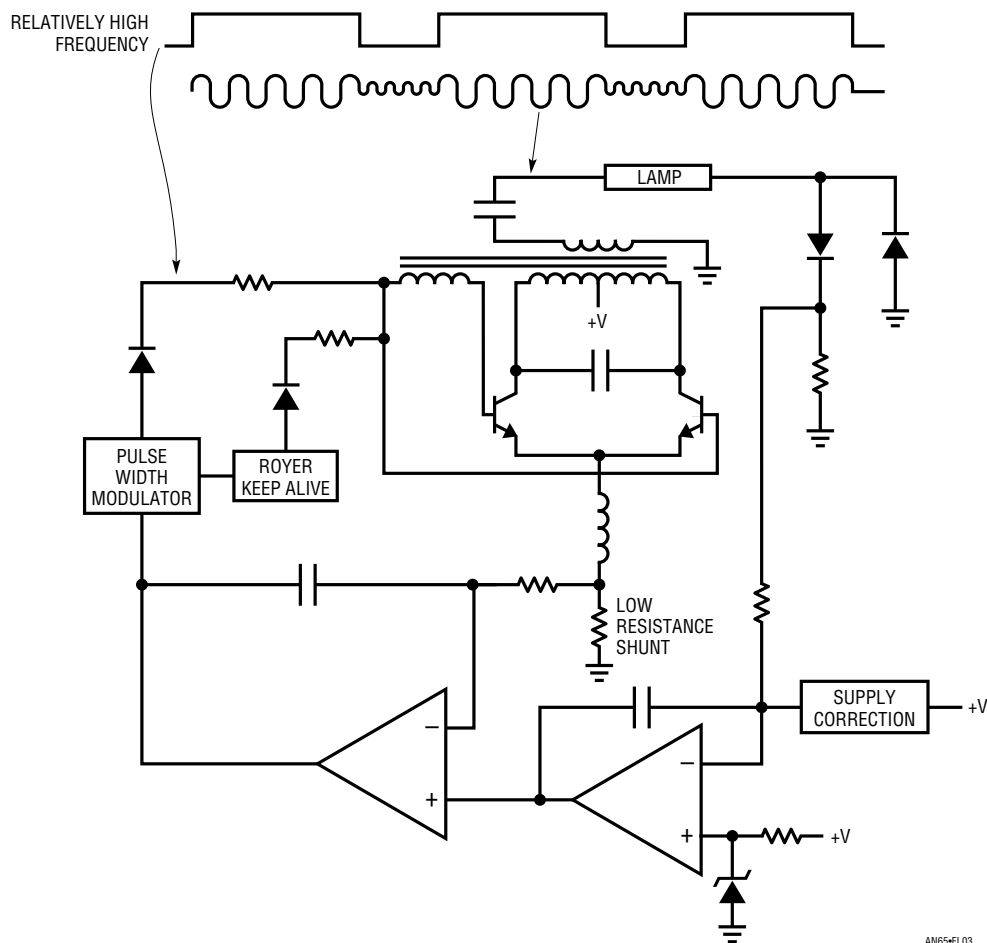


Figure L3. “Keep Alive” Circuit Eliminates Turn-On Losses and Has 94% Efficiency. Light Emission Is Lower Than “Less Efficient” Circuits

Application Note 65

Figure L4 is a very different approach. This circuit is a driven square wave converter. The resonating capacitor is eliminated. The base drive generator shapes the edges, minimizing harmonics for low noise operation. This circuit works well, but relatively low operating frequencies are required to get good efficiency. This is so because the sloped drive must be a small percentage of the fundamental to maintain low losses. This mandates relatively large magnetics—a crucial disadvantage. Also, square waves have a different crest factor and rise time than sines, forcing inefficient lamp transduction.

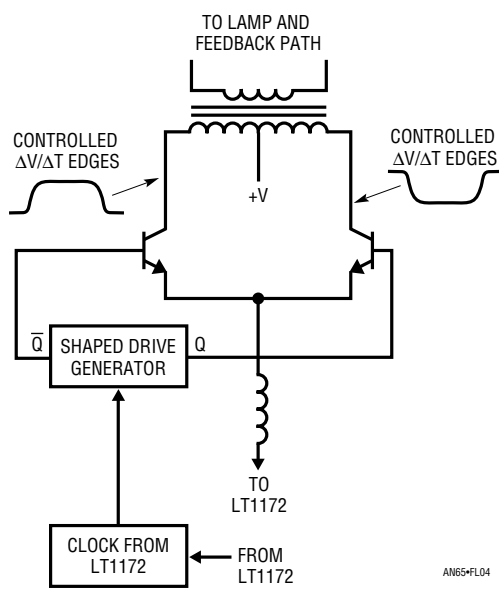


Figure L4. A Nonresonant Approach. Slew Retarded Edges Minimize Harmonics, but Transformer Size Goes Up. Output Waveform Is also Nonoptimal, Causing Lamp Losses

Not-So-Great Primary Side Sensing Ideas

Various text figures use primary side current sensing to control lamp intensity. This permits the lamp to fully float, extending its dynamic operating range. A number of primary side sensing approaches were tried before the “top side sense” won the contest.

L5’s ground-referred current sensing is the most obvious way to detect Royer current. It offers the advantage of simple signal conditioning—there is no common mode voltage. The assumption that essentially all Royer current derives from the LT1172 emitter pin path is true. Also true, however, is that the waveshape of this path’s current varies widely with input voltage and lamp operating cur-

rent. The RMS voltage across the shunt (e.g., the Royer current) is unaffected by this, but the simple RC averager produces different outputs for the various waveforms. This causes this approach to have very poor line rejection, rendering it impractical. L6 senses inductor flux, which should correlate with Royer current. This approach promises attractive simplicity. It gives better line regulation but still has some trouble giving reliable feedback as wave-shape changes. Also, in keeping with most flux sampling schemes, it regulates poorly under low current conditions.

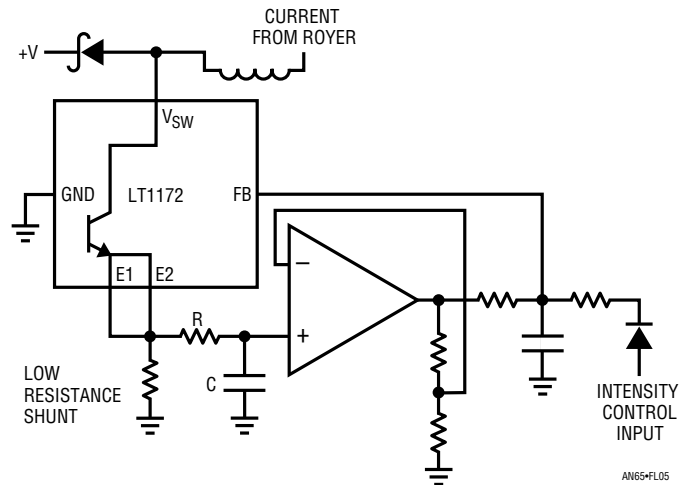


Figure L5. “Bottom Side” Current Sensing Has Poor Line Regulation Due to RC Averaging Characteristics

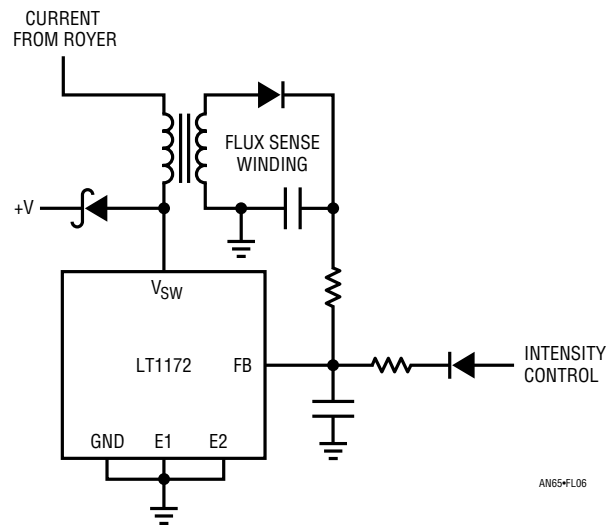


Figure L6. Inductor Flux Sensing Has Irregular Outputs, Particularly at Low Currents

Figure L7 senses flux in the transformer. This takes advantage of the transformer's more regular waveform. Line regulation is reasonably good because of this, but low current regulation is still poor. Figure L8 samples Royer collector voltage capacitively, but the feedback signal does not accurately represent start-up, transient and low current conditions.

Figure L9 is a true, photometrically sensed feedback loop. In theory, it gets around all of the above difficulties by

directly sensing lamp emission and feeding back a representative electrical signal. In practice, it introduces severe drawbacks.

The loop servo controls current to whatever value is required to force lamp emission to the photodiode determined point. This eliminates the gradually increasing lamp output (see text Figure 4) at turn-on. Unfortunately, it also forces huge turn-on currents through the lamp for 10 to 20 seconds, greatly shortening lamp life. Typically, the display immediately settles to the final emission point, but turn-on current peaks at four to six times lamp rating. It is possible to clamp or limit this behavior, but a more insidious problem remains.

As the lamp ages its emissivity drops. Typically, a properly driven lamp will drop to 70% of its original emission level after 10,000 hours. In a photometrically sensed loop, the inverter will continually raise lamp current to counteract decreasing emissivity. Although lamp emission remains constant, life is greatly shortened by the continually increasing overdrive required to maintain output. This positive feedback enforced degenerative spiral assures rapid, systematic lamp destruction. A five to eight times lamp lifetime reduction in this type of loop has been observed. As before, some form of limiting or 2-loop control scheme can mitigate the undesired characteristics, but advantages would be obviated. Finally, an economical photosensor with well-specified response is elusive.

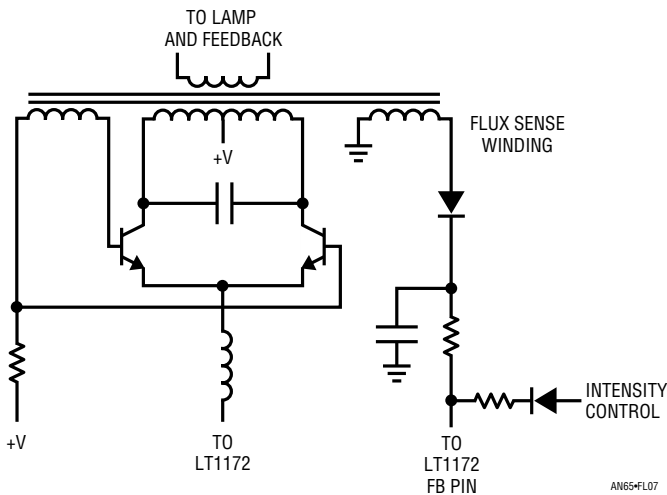


Figure L7. Transformer Flux Sensing Gives More Regular Feedback, but Not at Low Currents

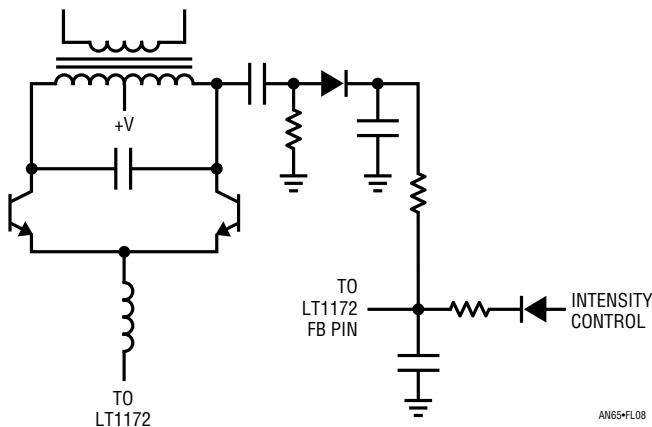


Figure L8. AC-Coupled Drive Waveform Feedback Is Not Reliable at Low Currents

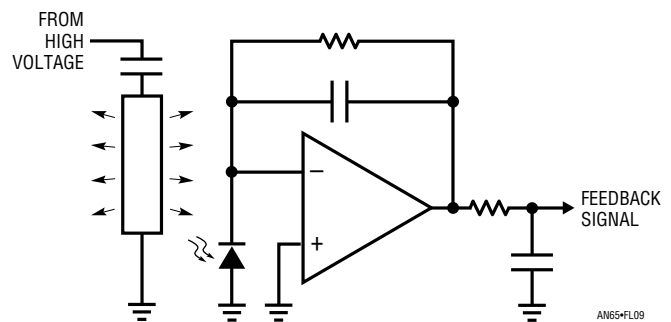
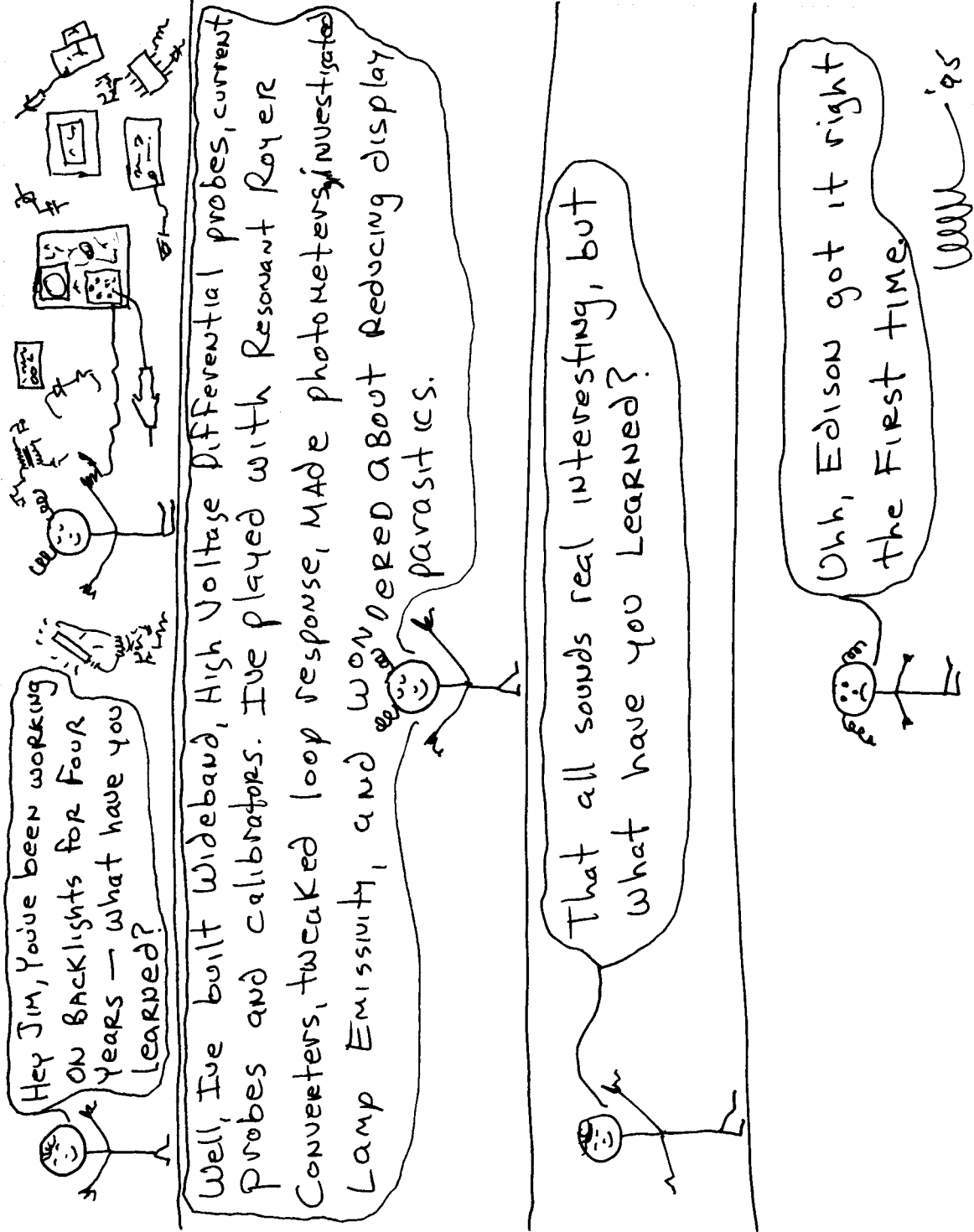


Figure L9. True Optical Sensing Eliminates Feedback Irregularities, but Introduces Systematic Lamp Degradation



A Monolithic Switching Regulator with 100 μ V Output Noise

“Silence is the perfectest herald of joy ...”

Jim Williams

INTRODUCTION

Size, output flexibility and efficiency advantages have made switching regulators common in electronic apparatus. The continued emphasis on these attributes has resulted in circuitry with 95% efficiency that requires minimal board area. Although these advantages are welcome, they necessitate compromising other parameters.

Switching Regulator “Noise”

Something commonly referred to as “noise” is a primary concern. The switched mode power delivery that permits the aforementioned advantages also creates wideband harmonic energy. This undesirable energy appears as radiated and conducted components commonly labeled as “noise.” Actually, switching regulator output “noise” is not really noise at all, but coherent, high frequency residue directly related to the regulator’s switching.¹ Figure 1 shows typical switching regulator output noise. Two distinct characteristics are present. The slow, ramping output ripple is caused by finite storage capacity of the regulator’s output filter components. The quickly rising spikes are associated with the switching transitions. Figure 2 shows another switching regulator output. In this case the ripple has been eliminated by adequate filtering and linear postregulation, but the wideband spikes remain. It is these fast spikes that cause so much difficulty in systems. Their high frequency content often corrupts associated circuitry, degrading performance or even disabling operation. Noise gets into adjacent circuitry via three paths. It is conducted out of the regulator output lead, it is conducted

back to the driving source (“reflected” noise) and it is radiated. The multiple transmission paths combine with the high frequency content to make noise suppression difficult. Unconscionable amounts of bypass capacitors, ferrite beads, shields, Mu-metal and aspirin have been expended in attempts to ameliorate noise-induced effects.

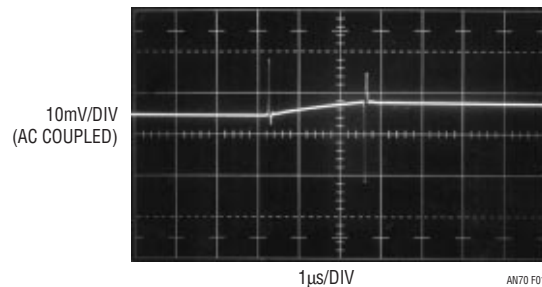


Figure 1. Typical Switching Regulator Output “Noise.” Wideband Spikes Are Difficult to Suppress, Causing System Interference Problems. Ripple Component Has Low Harmonic Content, Is Relatively Easily Filtered

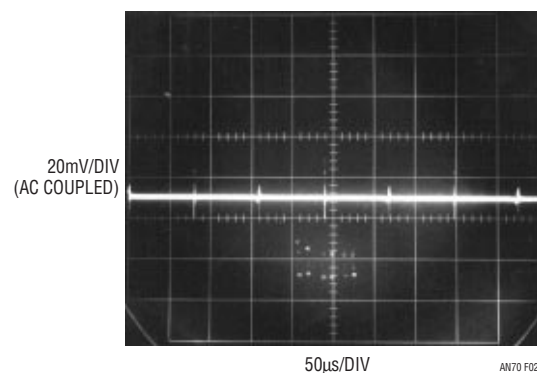


Figure 2. Linear Regulator Eliminates Ripple, but Wideband Spikes Remain. Peak-to-Peak Amplitude Exceeds 30mV (Just Visible Near 2nd, 5th and 8th Vertical Graticule Divisions)

Note 1. Noise contains no regularly occurring or coherent components. As such, switching regulator output “noise” is a misnomer. Unfortunately, undesired switching related components in the regulated output are almost always referred to as “noise.” As such, although technically incorrect, this publication treats all undesired output signals as “noise.” See Appendix B, “Specifying and Measuring Something Called Noise.”

Application Note 70

Alternate approaches involve synchronizing switching regulator operation to the host system or turning off switching during critical system operation (an “interrupt driven” power supply). Another approach places critical system operations between switch cycles, literally running between electronic rain drops.²

The difficulty of debugging a noise-laden system and the compromises involved in synchronized approaches could be eliminated with a low noise switching regulator. An inherently low noise switching regulator is the most attractive approach because it eliminates noise concerns while maintaining system flexibility.

A Noiseless Switching Regulator Approach

The key to an inherently low noise regulator is to minimize harmonic content in the switching transitions. Slowing down the switching interval does this, although power dissipated during the transition causes some efficiency loss. Reducing switch repetition rate can largely offset the

losses, resulting in a reasonably efficient design with small magnetics and the desired low noise. Noise reduction by restricting harmonic generation has been employed before, although the implementations were complex and narrowly applicable.³ A monolithic approach, broadly usable over a range of magnetics and applications, is described here.

A Practical, Low Noise Monolithic Regulator

Figure 3 describes the LT[®]1533, a monolithic regulator designed for low noise switching supplies. Figure 4 details the pin functions. Figure 3’s functional blocks show a fairly conventional push-pull architecture with a major exception. The push-pull approach has good magnetics utilization (power transfer is always occurring in the transformer; the core does not store energy) and pulls current

Note 2: See References 2 and 3 for details and practical examples of these techniques.

Note 3: See Appendix A, “A History of Low Noise DC/DC Conversion.” See also References 4 through 10.

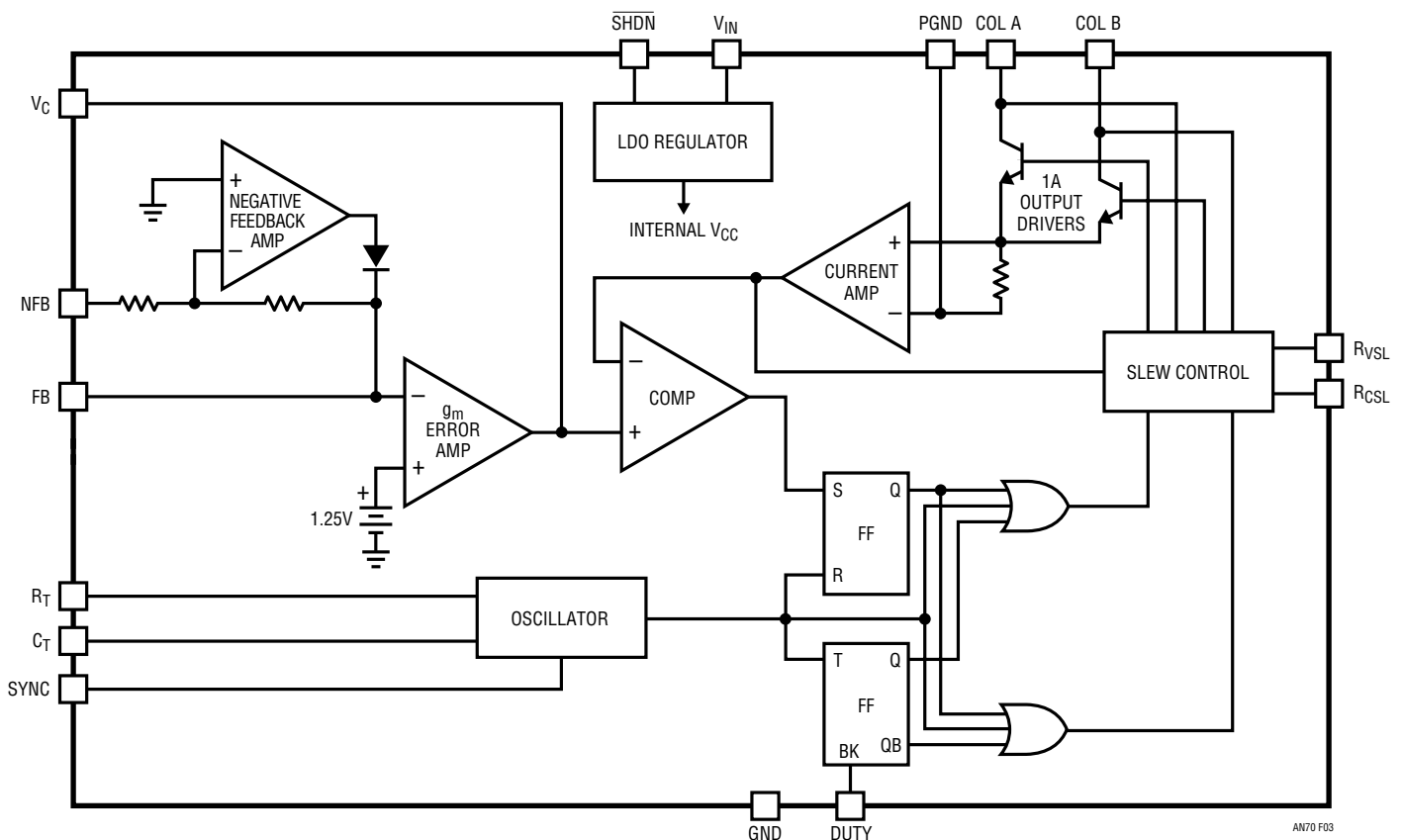


Figure 3. LT1533 Simplified Block Diagram. 1A Slew-Controlled Output Stages Provide Low Noise Switching

COL A, COL B: Output transistor collectors which switch out-of-phase.
 DUTY: Grounding this pin forces the outputs to switch at a 50% duty cycle. This pin must float if not used.
 SYNC: Used to synchronize to an external clock. Float or tie to ground if unused.
 C_T : Oscillator timing capacitor.
 R_T : Oscillator timing resistor.
 FB: Used for positive output voltage sensing.
 NFB: Used for negative output voltage sensing.
 GND: Analog ground pin.
 PGND: High current ground return. Should be returned to ground via $\approx 50\text{nH}$ ($\approx 1''$ of PC trace or wire, or a small ferrite bead). See Appendix F or schematic (Figures 5 and 26) notes for details. In some package options, this pin may be internally connected to "GND" pin.
 V_C : Frequency compensation node.
 SHDN: Normally high. Grounding this pin shuts the part down. $I_{\text{SHDN}} = 20\mu\text{A}$.
 R_{CSL} : Current slew control resistor.
 R_{VSL} : Voltage slew control resistor.
 V_{IN} : Input supply pin. 2.7V to 30V range. Undervoltage lockout at 2.55V.

Figure 4. LT1533 Short Form Pin Function Descriptions

continuously from the source. The even, continuous current drain from the source eliminates the fast, high peak currents required by flyback and other approaches. The source sees a benign load and is not corrupted. The switches also receive nonoverlapping drive, ensuring they do not conduct simultaneously. Simultaneous conduction

would cause excessive, quickly rising currents, degrading efficiency and generating noise.

The design's most significant aspect is the output stage. Each 1A power transistor operates inside a broadband control loop. The voltage across each transistor and the current through it are sensed and the loop controls slew rate of each parameter. The voltage and current slew rates are independently settable by external programming resistors. This ability to control the switching's rate-of-change makes low noise switching regulation practical. Operating the switching transistors in a local loop permits predictable, wide range control over a variety of situations.⁴ Figure 5 is a 40kHz, 5V to 12V converter using the LT1533 in a push-pull, "forward" configuration. The feedback resistor's ratio produces a 12V output. A two-section LC filter provides high ripple attenuation, although a single section will give good performance. It is particularly noteworthy that high frequency noise content (as opposed to the 40kHz fundamental related ripple) is unaffected by output filter characteristics. This is so simply because there is so little high frequency energy developed in this circuit. If there's nothing there, it doesn't need to be filtered!

L2 provides compensation for the output current control loop. In practice, L2 may be a length of PC trace, a small inductor, a coiled section of wire or a ferrite bead. See Appendix F, "Magnetics Considerations" for complete discussion.

Note 4: Patent pending.

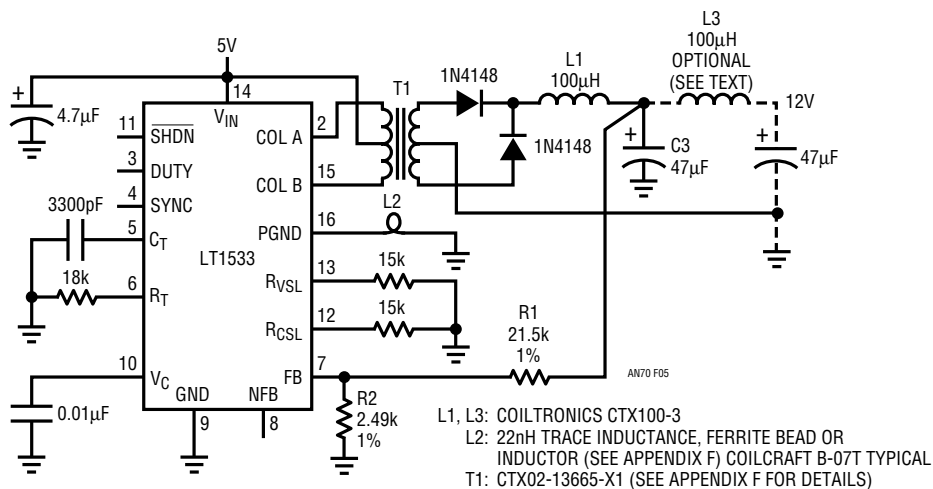


Figure 5. 100µV Noise 5V-to-12V Converter. Output LC Section May Be Deleted If Low Frequency Ripple Is Acceptable

Application Note 70

Measuring Output Noise

Measuring the LT1533's unprecedented low noise levels requires care.⁵ Figure 6 shows a test setup for taking the measurement. Good connection and signal handling technique combined with judicious instrumentation choice should yield a $100\mu\text{V}$ noise floor in a 100MHz bandwidth. This corresponds to the noise of a 50Ω resistor in a 100MHz bandwidth.

Before measuring regulator output noise, it is good practice to verify test setup performance. This is done by running the test setup with no input. Figure 7 shows a noise base line of $100\mu\text{V}$ in a 100MHz bandwidth, indicating the instrumentation is operating properly. Measuring Figure 5's noise involves AC coupling the circuit's output into the test setup's input. Figure 8 shows this. Coaxial connections must be maintained to preserve measurement integrity.⁶ Figure 9's waveforms detail circuit operation. Traces A and C are switching transistor collector voltages, B and D are the respective transistor currents. The test setup's output, representing circuit output noise, is Trace E. Wideband spiking and ripple, just visible in the noise floor, is inside $100\mu\text{V}$, even in a 100MHz bandpass.⁷

This is spectacularly good performance and is, in fact, actually better than the photo shows. Removing all probes from the breadboard leaves only Trace E's coaxial connection. This eliminates any possible ground loop-induced error.⁸ Figure 10's trace shows 40kHz ripple with about the same amplitude as in Figure 9. Switching related spikes, just faintly outline in the noise, are reduced.

Measurement bandwidth is reduced to 10MHz in Figure 11, attenuating test fixture amplifier noise. Switching and ripple residue amplitude and shape do not change, indicating no signal activity beyond this frequency. Figure 12's

Note 5: Equipment selection and measurement techniques are detailed in Appendix B, "Specifying and Measuring Something Called Noise." See also Appendix C, "Probing and Connection Techniques for Low Level, Wideband Signal Integrity."

Note 6: Again, see Appendices B and C for extended treatment of these and related issues.

Note 7: It is common industry practice to specify switching regulator noise in a 20MHz bandpass. There can be only one reason for this, and it is a disservice to users. See Appendix B for tutorial on observed noise versus measurement bandwidth.

Note 8: See Appendix C for related discussion and techniques for triggering oscilloscopes without invasively probing the circuit.

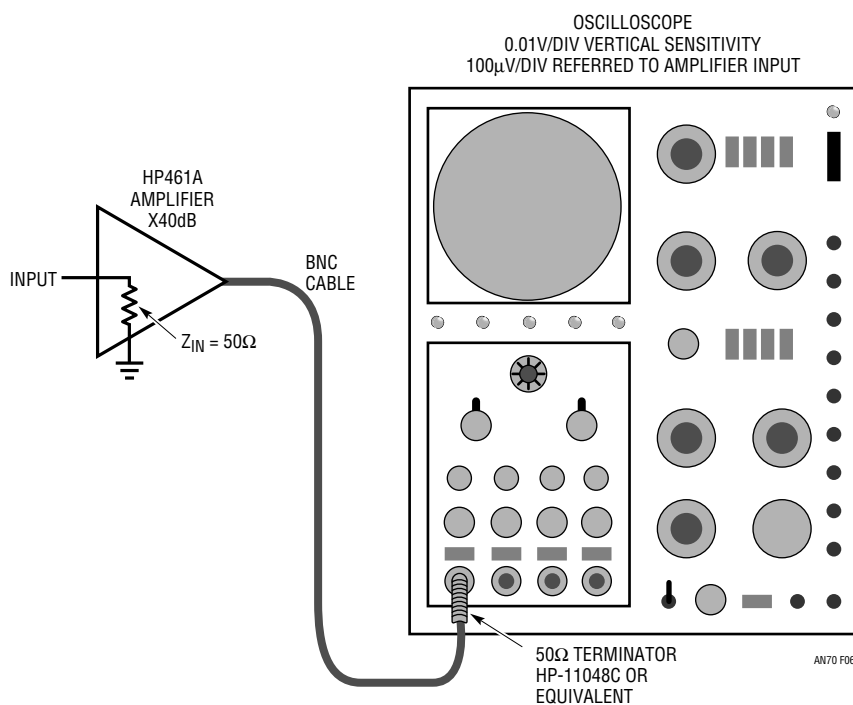


Figure 6. Test Setup Noise Baseline Is $100\mu\text{V}_{\text{p-p}}$ in 100MHz Bandwidth. Performance Is 50Ω Resistor Noise Limited. BNC Cable Connections and Terminations Provide Coaxial Environment, Ensuring Wideband, Low Noise Characteristics

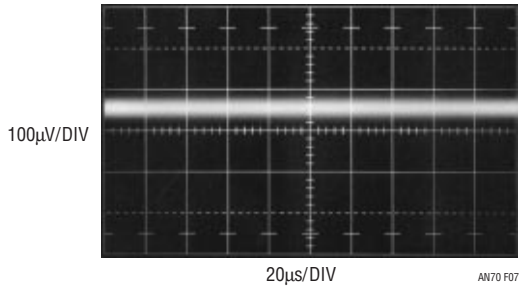


Figure 7. Oscilloscope Verifies Test Setup 100µV Noise Floor in 100MHz Bandwidth. Indicated Noise Is That of a 50Ω Resistor

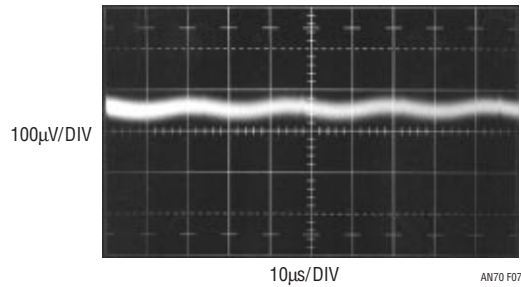


Figure 10. Removing Probes from Figure 9's Test Eliminates Ground Loops, Slightly Reducing Observed Noise. Switching Artifacts Are Just Discernible Above Noise Floor

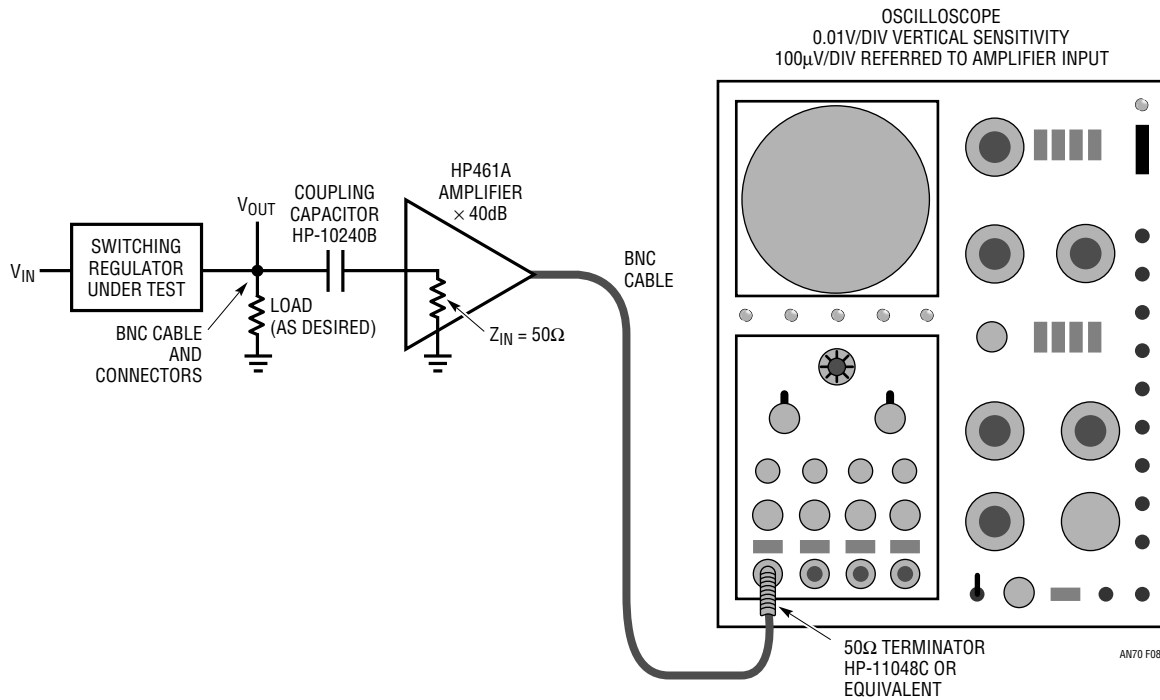


Figure 8. Connecting Figure 5's Circuit to the Test Setup. Coaxial Connections Must Be Maintained to Preserve Measurement Integrity

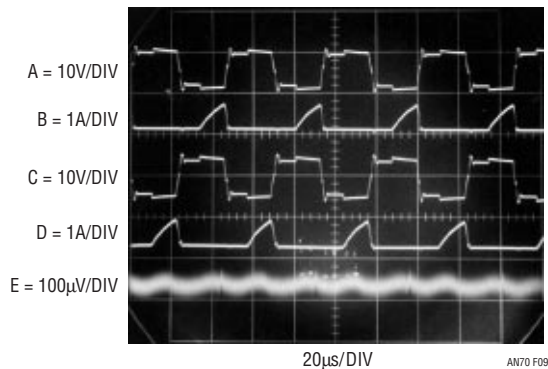


Figure 9. Waveforms for Figure 5 at 100mA Loading. Traces A and C Are Voltage; B and D are Current, Respectively. Switching Transition's Noise Signature Appears in Trace E, the Circuit's Output Noise

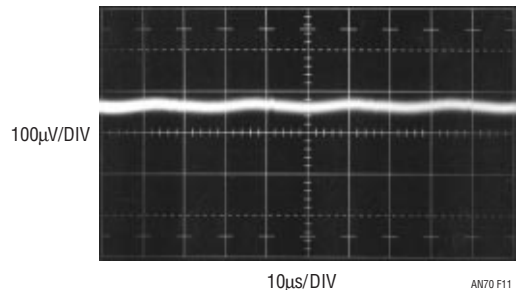


Figure 11. Reducing Measurement Bandwidth to 10MHz Attenuates Amplifier Noise. Switching Residue Characteristics Remain Unchanged, Indicating No Signal Activity Beyond This Frequency

Application Note 70

horizontal expansion of Figure 10 returns to 100MHz bandpass. The switching spike appears in the center screen region. At 2 μ s/division sweep, there is no wide-band activity observable. Figure 13, a 10MHz bandpass version of Figure 12, retains all signal information, further suggesting no signal power beyond 10MHz.

Figure 14 is the noise floor of an HP4195A spectrum analyzer in a 500MHz sweep. When Figure 5's circuit is AC coupled into the analyzer, the output (Figure 15a) is essentially identical. The analyzer is unable to detect switching-induced noise in a 500MHz bandpass. Some 40kHz fundamental-related components are detectable in Figure 15b's 1MHz wide plot, although the rest of the sweep is analyzer noise limited. Additional filtering or a linear postregulator could eliminate the 40kHz ripple-related residue if desired.

The preamplified oscilloscope is a more sensitive tool for these measurements because its triggered operation has the advantage of synchronous detection. This is demonstrable by free running the preamplified oscilloscope sweep; the switching-related components are indistinguishable in the noise background.

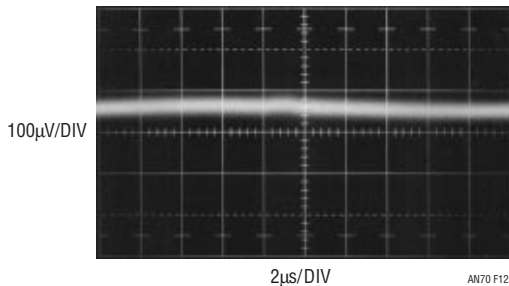


Figure 12. Horizontal Expansion of Figure 10 Shows No Wideband Components. Switching Originated Noise Appears in Center Screen Region

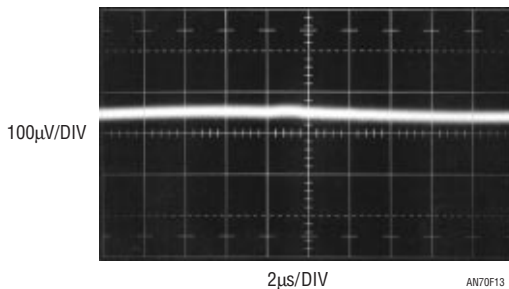


Figure 13. A 10MHz Band Limited Version of Figure 12. As Before, Signal Information Is Retained, Although Amplifier Noise Is Reduced. Results Indicate No Signal Power Beyond 10MHz

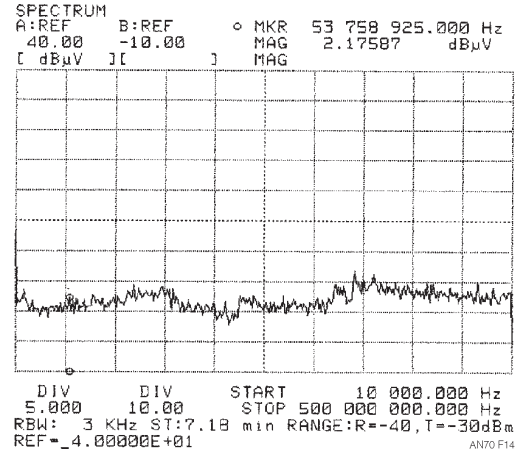


Figure 14. Noise Floor of Test Fixture and HP-4195A Spectrum Analyzer in a 500MHz Sweep

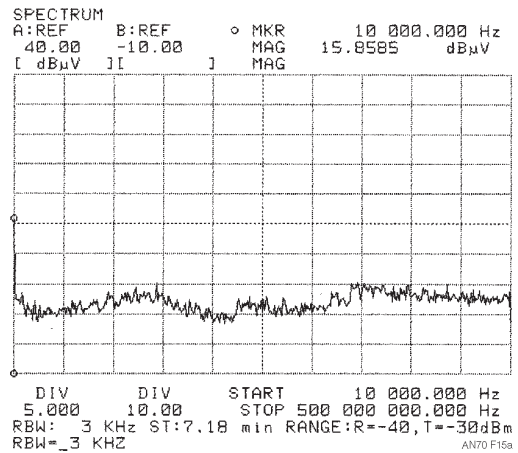


Figure 15a. Figure 5's Circuit Connected to the Spectrum Analyzer Produces Essentially Identical Results to Figure 14. Circuit's Noise Is Undetectable

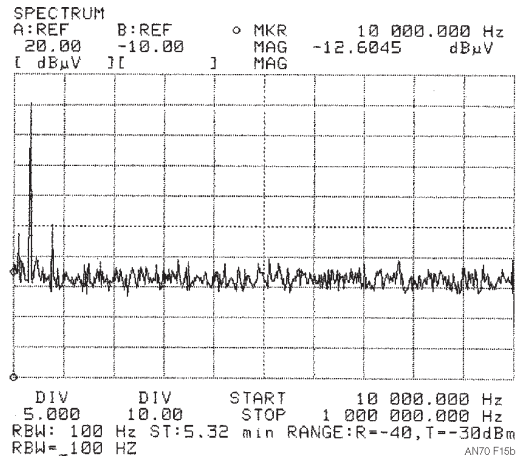


Figure 15b. Reducing Analyzer Sweep to 1MHz Width Reveals 40kHz Related Components. Remainder of Plot Is Analyzer Noise Floor Limited, Even in Sensitive 455kHz Band

Figure 16 studies ripple at the first LC filter section output. The ripple's 40kHz fundamental is clearly seen, although no wideband spikes are visible. Figure 17 horizontally expands Figure 14's time scale, but high frequency harmonics and spikes are not observable.

Low frequency noise is rarely a concern, although Figure 18 shows it is inside 50 μ V in a 10Hz to 10kHz bandpass. Input current noise is usually of more interest. Excessive "reflected" noise can corrupt the regulator's driving source, causing system level interference. Figure 19 shows Figure 5's input current as DC with a small, 40kHz fundamental-related sinusoidal component. There is no high frequency content, and the sinusoidal variations are easily handled by the driving source.

System-Based Noise "Measurement"

In the final analysis, the effect of switching regulator output noise on the system it is powering is the ultimate test. Appendix K, "System-Based Noise "Measurement," presents results when the LT1533 is used to power a 16-bit A/D converter.

Transition Rate Effects on Noise and Efficiency

In theory, simply setting transition rate to low values will achieve low noise. Practically, such an approach, while workable, wastes power during transitions, lowering efficiency. A good compromise sets transition time at the fastest rate permitting desired noise performance. The LT1533's slew adjustments allow easy determination of this point. Figure 20's photographs dramatically demonstrate the relationship between transition time and output noise for Figure 5's circuit. The sequence shows >5:1 noise reduction as switch transition time slows from 100ns (20a) to 1 μ s (20d). Figure 20d's displayed noise is actually lower, as the probing-induced error caused by monitoring the switch corrupts the measurement.⁹

Figure 21 graphically summarizes Figure 20's information. Significant noise reduction coincides with descending transition slew time until about 1.3 μ s. Little additional noise benefit occurs beyond this point. Figure 22 shows efficiency fall-off with slew time. There is a 6% penalty between 100ns and 1.3 μ s, the same region where noise performance improves by a factor of 5 (per previous

Note 9: See Appendix C, "Probing and Connection Techniques for Low Level, Wideband Signal Integrity" for guidance.

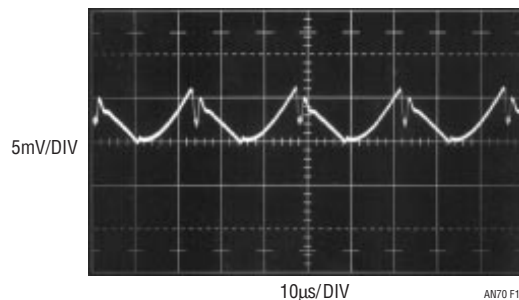


Figure 16. Ripple at Figure 5's First LC Output Has No Wideband Spikes

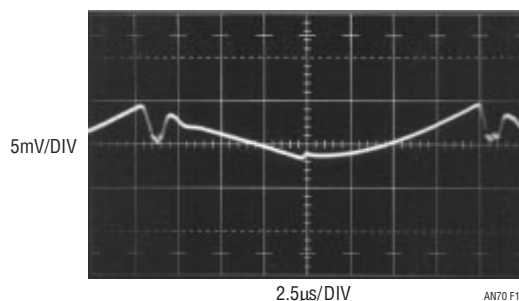


Figure 17. Time Expansion of Previous Figure. No High Frequency Content Is Visible

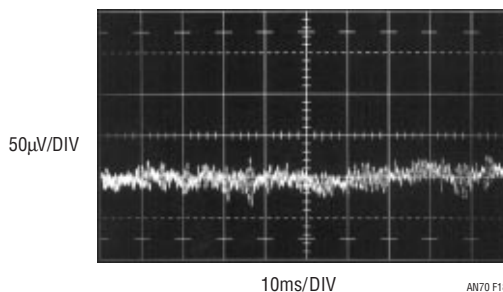


Figure 18. Low Frequency Noise in a 10Hz to 10kHz Bandpass

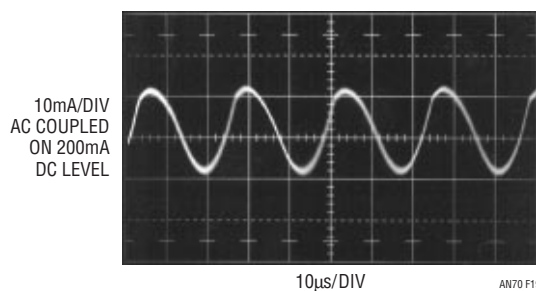


Figure 19. Figure 5's Small Sinusoidal Input Current Variations Contain No High Frequency Content and Are Easily Absorbed by Input Supply

Application Note 70

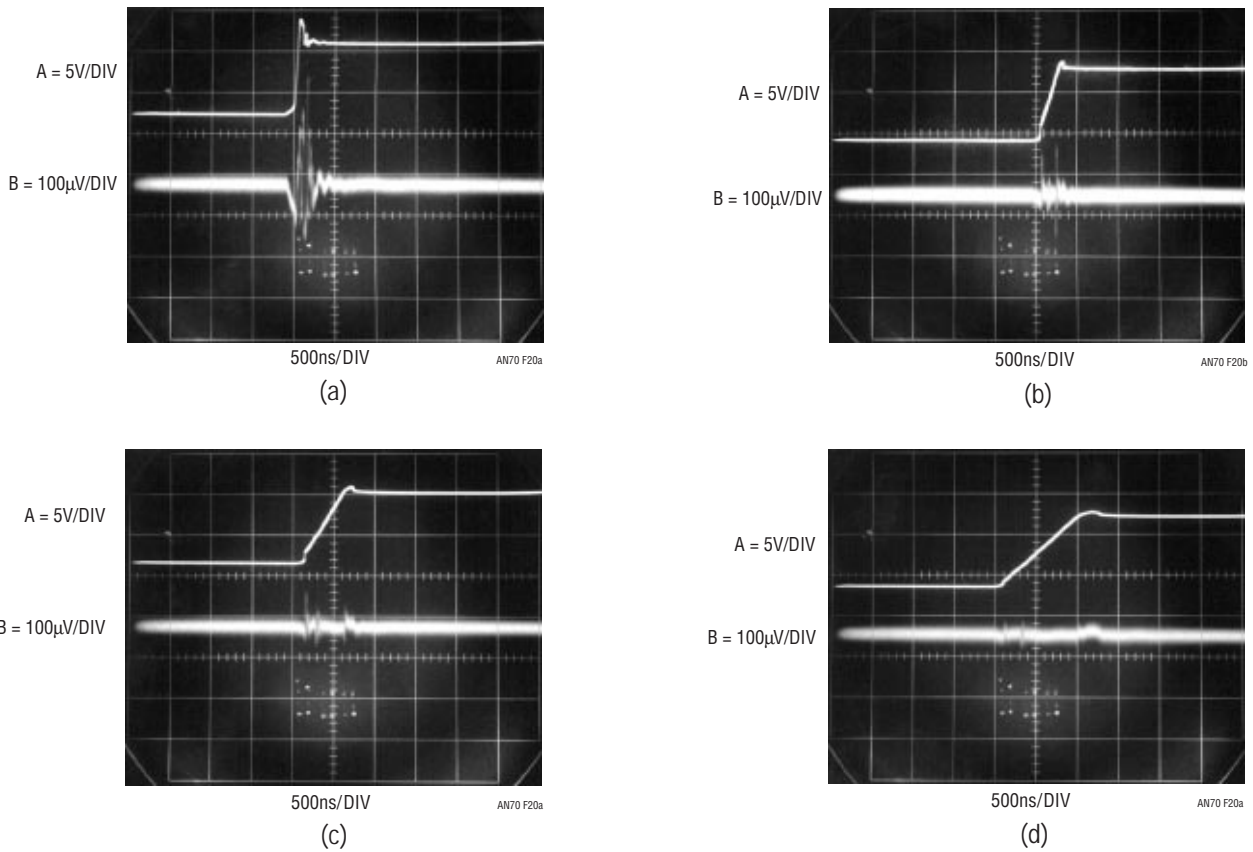


Figure 20. Output Noise (Trace B) vs Different Switch Slew Rates (Trace A). Highest Slew Rate (Figure a) Causes Largest Noise. Retarding Slew Rate (Figures b and c) Decreases Noise Until Lowest Noise Performance Is Achieved (Figure d)

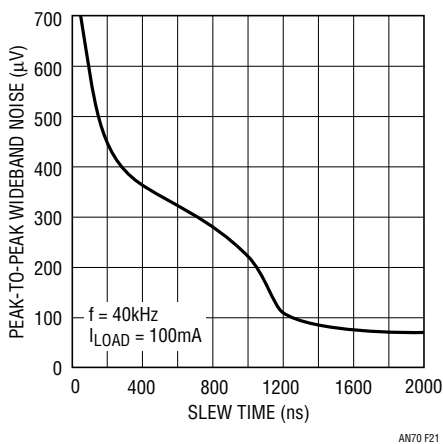


Figure 21. Figure 5's Noise vs Slew Time at 40kHz Switching Frequency. Noise Reduction Beyond 1.3µs Is Minimal

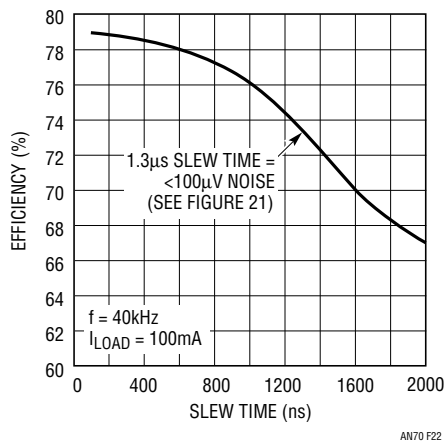


Figure 22. Figure 5's Efficiency Drops 6% as Slew Time Extends to 1.3µs. Operation Beyond This Point Gains Little Noise Performance (See Previous Curve) with 6% Efficiency Penalty

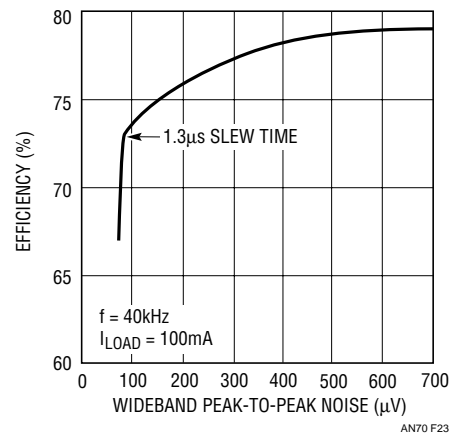


Figure 23. Efficiency vs Noise for Figure 5. Data Shows Significant Efficiency Fall-Off for Noise Below 80µV

figure). There is an additional 6% penalty beyond 1.3 μ s, although no significant noise reduction occurs (again, per Figure 21). As such, operation in this region is undesirable. Figure 23 clearly shows the inflection point in the efficiency versus noise trade-off.¹⁰

Negative Output Regulator

The LT1533 has a separate feedback input that directly accepts negative inputs.¹¹ This permits negative outputs without the usual discrete level shifting stage. Figure 24's 5V to -12V converter is similar to Figure 5's circuit, except that the negative output is fed back to the negative feedback input. The feedback scale factor change is necessitated by the higher effective reference voltage. In all other respects, the circuit (and its performance) is similar to Figure 5.

Floating Output Regulator

Figure 25's isolation stage permits a fully floating, regulated output. The LT1431 shunt regulator compares a portion of the output to its internal reference and drives the optoisolator with the error signal. The optoisolator's collector output biases the LT1431's V_C pin, closing a feedback loop to regulate circuit output. The 0.22 μ F capacitor stabilizes the loop and the 240k Ω resistor biases the optoisolator into a favorable operating region. This circuit's operation and characteristics are similar to Figure 5 with the added benefit of the isolated output.

Floating Bipolar Output Converter

Grounding the LT1533's "DUTY" pin and biasing FB forces the device into its 50% duty cycle mode. Figure 26's output is full wave rectified with respect to T1's secondary center tap, producing bipolar outputs. The forced 50% duty cycle combined with no feedback means the outputs are unregulated, proportioning to T1's drive voltage. An output inductor is usually not required, as in Figure 5's "forward" converter. At the very highest output currents, some inductance may be necessary to limit inrush current. If this is not done, the circuit may not start. Typically, linear regulators provide regulation.¹²

Figure 26's waveforms appear in Figure 27. Collector voltage (Traces A and C) and current (Traces B and D) are shown, along with the indicated output noise (Trace E). In this case linear regulators and an output filter are in use. In Figure 28 all probes except the coaxial output connection are removed. This eliminates probing induced parasitics,¹³ allowing a higher fidelity signal presentation. Here, the switching residuals are barely detectable in the noise floor. Removing the optional output filter (Figure 29) allows linear regulator contributed noise and switching spikes to rise, but noise is still below 300 μ V_{P-P}.

Note 10: The noise and efficiency characteristics appearing in Figures 20 to 23 were generated at the bench in about ten minutes. All you CAD modeling types out there might want to think about that.

Note 11: See Figure 3's Block Diagram.

Note 12: See Appendix E, "Selection Criteria for Linear Regulators."

Note 13: See Appendix C, "Probing and Connection Techniques for Low Level, Wideband Signal Integrity," for relevant discussion.

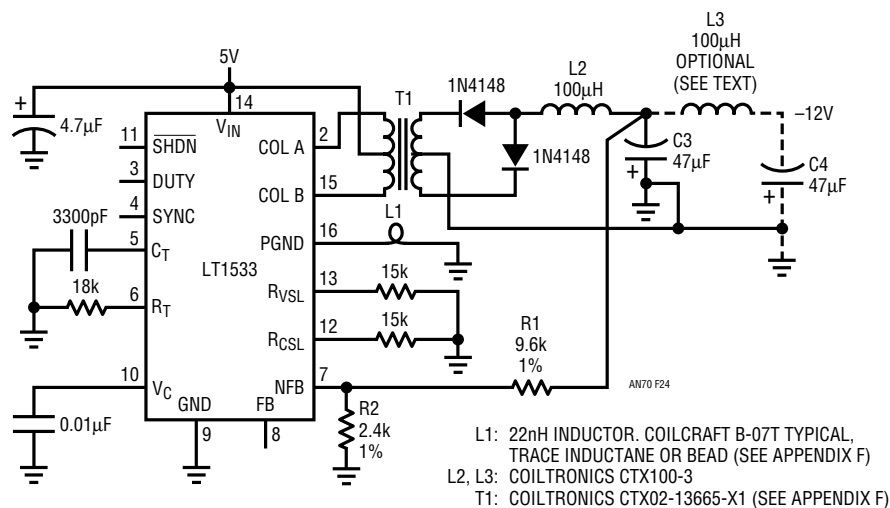


Figure 24. A Negative Output Version of Figure 5. LT1533's Negative Feedback Input Requires Minimal Configuration Changes. Noise Performance Is Identical to Positive Output Version

Application Note 70

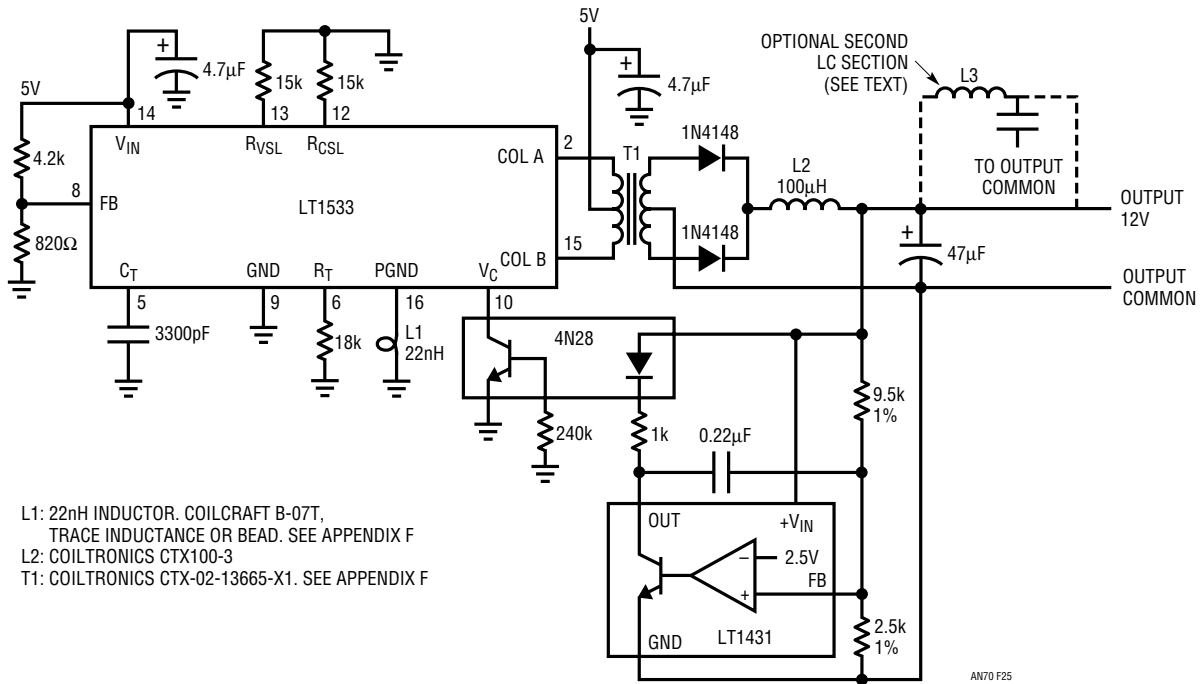


Figure 25. An Optoisolated Output Variant of Figure 5. Loop Closure to V_C Pin Bypasses LT1533 Error Amplifier, Enhancing Loop Stability. Noise Performance is Maintained.

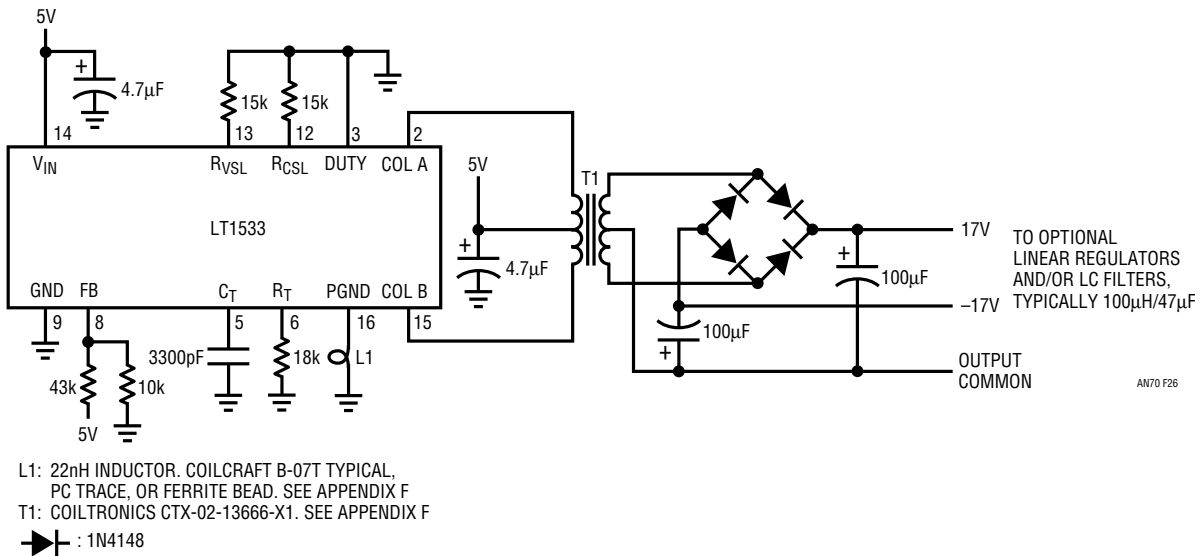


Figure 26. A Bipolar, Floating Output Converter. Grounding "DUTY" Pin and Biasing FB Puts Regulator into 50% Duty Cycle Mode. Floating, Unregulated Outputs Proportion to T1's Center Tap Voltage. Linear Regulators Are Optional

As in Figure 5's case, spectrum analyzer measurements are instrument limited. Figure 30 shows the analyzer's noise floor in a 500MHz sweep when monitoring the unpowered Figure 26's breadboard. In Figure 31, the breadboard is powered, but analyzer output is noise limited and essentially indistinguishable from the unpowered case. Similarly, Figure 32's 1MHz wide "power-on" plot is identical to Figure 33's noise floor limited "power-off" sweep. Note that linear postregulation is in use and the 40kHz fundamental components are not detectable. Figure 5's circuit did not have linear postregulation and 40kHz fundamental residue appeared in Figure 15b.

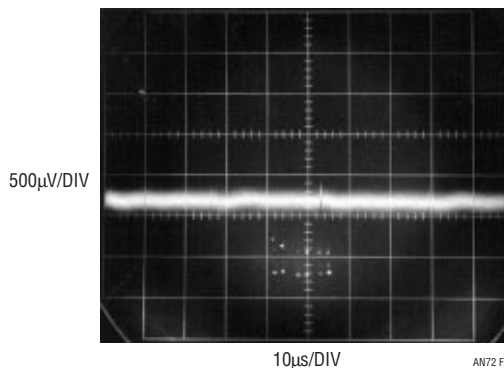


Figure 29. Removing Optional LC Filter Causes Linear Regulator-Contributed Noise and Switching Spikes to Rise. Peak-to-Peak Noise Is Still <math>< 300\mu\text{V}</math>

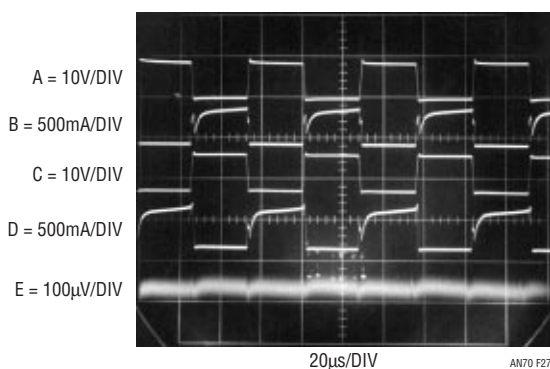


Figure 27. Waveforms for the Floating Output Converter at 100mA Loading. Linear Postregulator and Optional LC Filter Are Employed. Slew-Controlled Collector Voltage (Traces A and C) and Current (Traces B and D) Produce Output (Trace E) with Under $100\mu\text{V}$ Noise

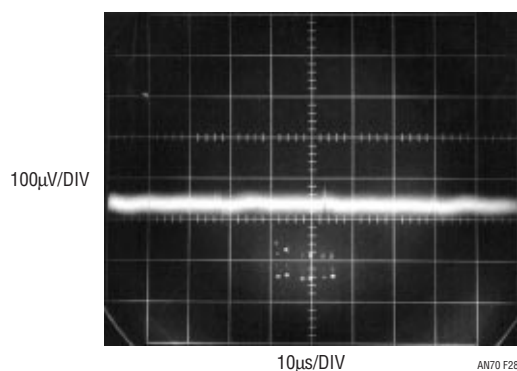


Figure 28. Removing All Probes Except Coaxial Output Connection Reveals Figure 27's True Noise Figure. Switching Residue Is Just Detectable in Amplifier Noise

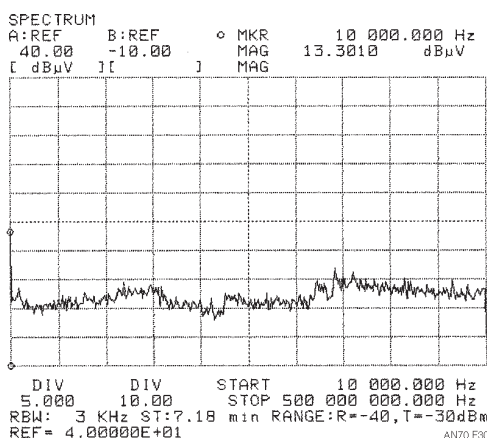


Figure 30. HP4195A Analyzer's Noise Floor in a 500MHz Sweep When Connected to Unpowered Figure 26

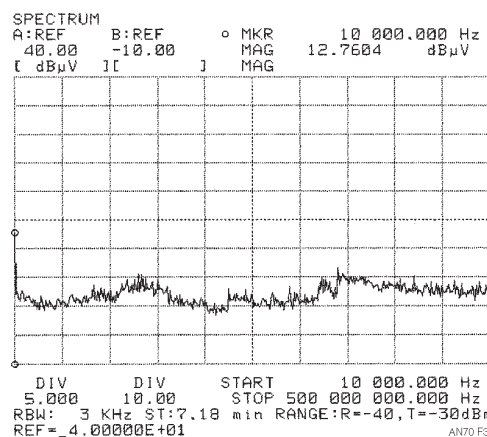


Figure 31. Figure 26's "Power-On" Output Noise Is Undetectable in Analyzer's Noise Floor Limited 500MHz Sweep

Application Note 70

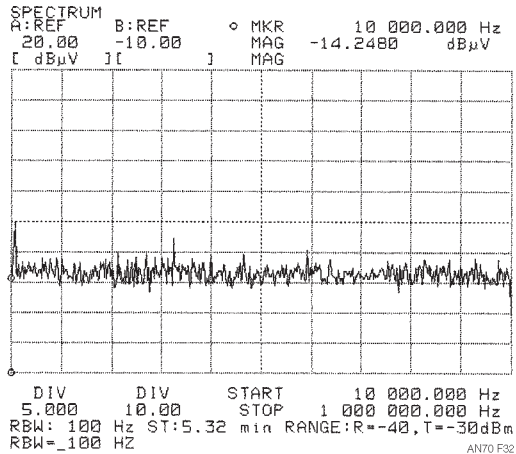


Figure 32. Linear Postregulation Eliminates 40kHz Fundamental-Related Components in 1MHz Sweep

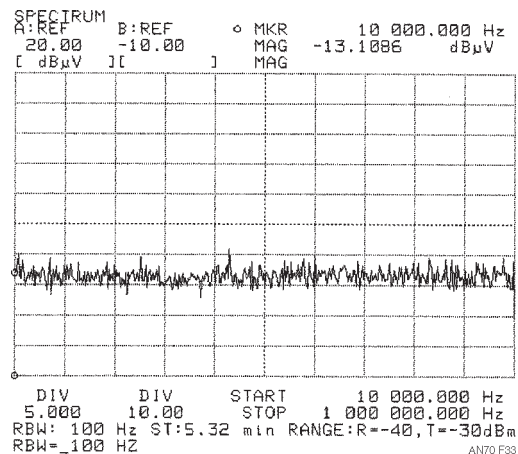


Figure 33. Turning Circuit Power Off Verifies Figure 32's Plot Is Analyzer Noise Floor Limited. Sweep Results Are Identical to Figure 32's "Power-On" Data

Battery-Powered Circuits

The basic configurations may be battery-powered for use in portable apparatus. Figure 34, similar to Figure 5, runs from 2.7V_{MIN} (e.g., three NiCd batteries), producing 12V output. This design induces no noise-based error when powering a fast 16-bit A/D converter, something almost no DC/DC converter can do. Appendix K contributes compelling testimony to this somewhat boastful claim.

Figure 35 also operates from three NiCd cells, producing a 9V output. This design achieves 100μV output noise, qualifying it as the electronic equivalent of a 9V battery.

Performance Augmentation

In some cases it may be desirable to augment LT1533 performance characteristics. Usually, this involves additional circuitry, and may necessitate trading off performance in one area to gain the desired benefit.

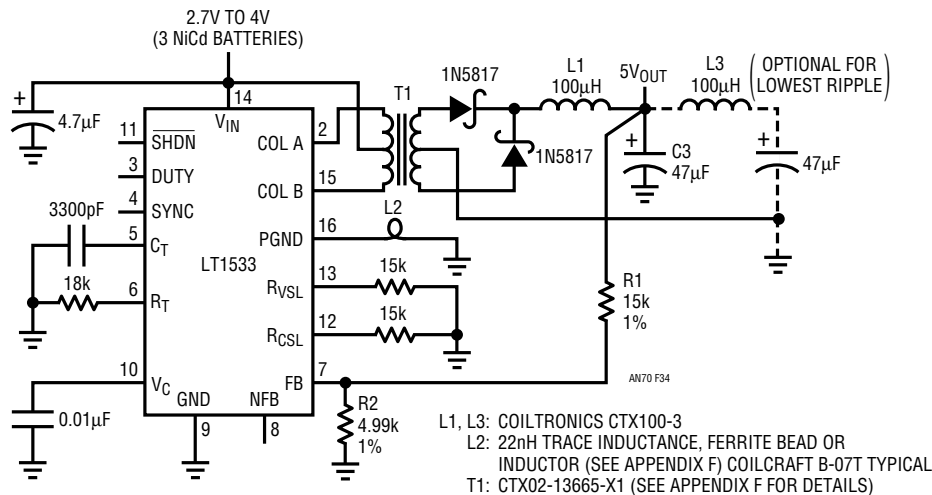


Figure 34. Circuit Delivers 5V from Three NiCd Batteries, Has 100μV Wideband Output Noise. This Design Contributes No Noise-Based Error When Powering a 16-Bit A/D Converter (See Appendix K)

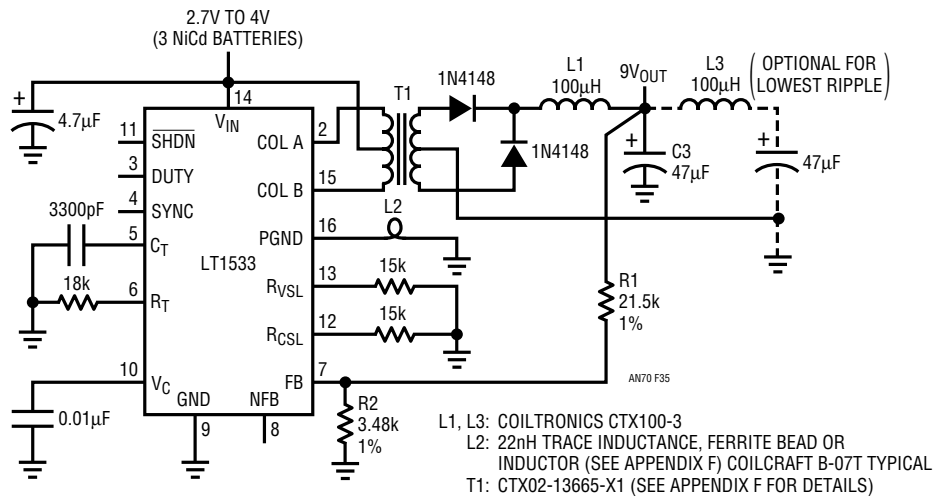


Figure 35. Electronic Equivalent of 9V Battery Operates from Three NiCd Cells. Output Noise Is Below 100µV

Low Quiescent Current Regulator

The LT1533 has a quiescent current of about 6mA. Figure 36's circuit reduces this figure to 100µA by running an on-off control loop around the device. The control loop replaces the normal error amplifier, achieving regulation by switching the IC in and out of shutdown in accordance with loop demands.

Comparator C1 compares a scaled version of the output with its internal reference and biases the regulators shutdown pin. Loop hysteresis is obtained by utilizing the phase shift (e.g., time delay) of the output LC components. In a normal continuously closed loop this phase shift must be minimized and compensated. In this case it promotes the desired hysteretic control characteristic. Local AC positive feedback at C1 ensures clean transitions. Figure 37 shows the loop at work. When circuit output drops below the regulation point, C1's output (Trace A) goes high. This enables the regulator and it responds with a burst of drive (Trace B) to the transformer. The output is restored and C1 goes low until the next cycle. During C1's low time the regulator is shut down, resulting in the extremely low quiescent current noted. The loop's on-off control characteristic causes low frequency output noise related to LC tank ring. Trace C shows 600µV peaks, although no wideband components are observable.

High Voltage Input Regulator

The LT1533's IC process limits collector breakdown to 30V. A complicating factor is that the transformer swings to 2× supply. Thus, 15V represents the maximum allowable input supply. Many applications require higher voltage inputs and Figure 38 uses a cascoded¹⁴ output stage to achieve such high voltage capability. This 24V-to-50V converter is reminiscent of previous circuits, except that Q1 and Q2 appear. These devices, interposed between the IC and the transformer, constitute a cascoded high voltage stage. They provide voltage gain while isolating the IC from their large collector voltage savings.

Normally, high voltage cascodes are designed to simply supply voltage isolation. Cascoding the LT1533 presents special considerations because the transformers instantaneous voltage and current information must be accurately transmitted, albeit at lower amplitude, to the LT1533. If this is not done, the regulator's slew control loops will

Note 14: The term "cascoding," derived from "cascade to cathode," is applied to a configuration that places active devices in series. The benefit may be higher breakdown voltage, decreased input capacitance, bandwidth improvement, etc. Cascoding has been employed in op amps, power supplies, oscilloscopes and other areas to obtain performance enhancement. The origin of the term is clouded and the author will mail a magnum of champagne to the first reader correctly identifying the original author and publication.

Application Note 70

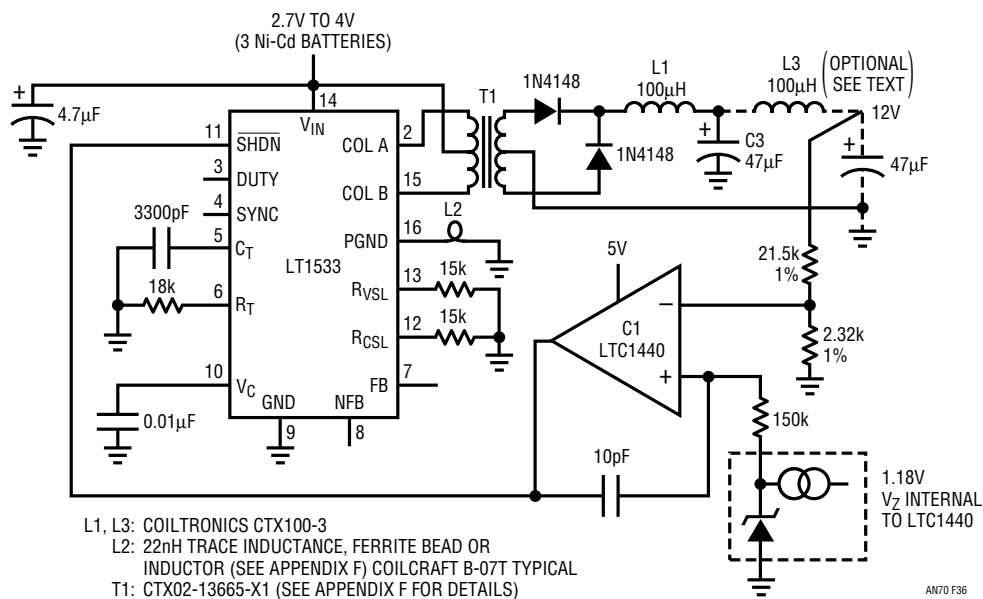


Figure 36. Hysteretic "Burst Mode™" Loop Lowers Quiescent Current to 100µA While Maintaining Low Output Noise

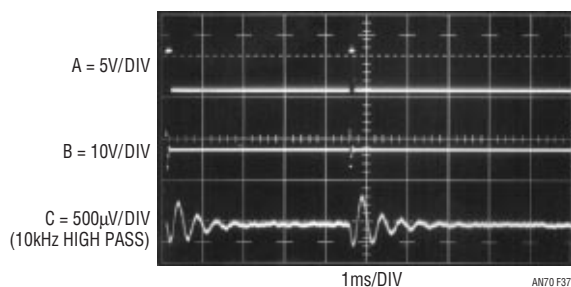


Figure 37. Operating Waveforms for the Low Quiescent Current Converter. Comparator Output (Trace A) Restores Output Voltage by Turning LT1533 On (Trace B). Output Noise Shows LC Ringing (Trace C), Although High Frequency Content Is Negligible

Burst Mode is a trademark of Linear Technology Corporation.

not function, causing a dramatic output noise increase. The AC compensated resistor dividers associated with the Q1-Q2 base collector biasing serve this purpose. Q3 and associated components provide a stable DC termination for the dividers. Figure 39 shows waveforms for Q1's operation (Q2 is identical, although of opposing phase). Trace A is Q1's emitter, Trace B its base and Trace C the collector. T1's ring-off obscures the fact that waveform fidelity is maintained through the cascode, although inspection reveals this to be the case. Additional testimony is given by circuit output noise (Trace D), which measures about 100 μ V peak.

24V-to-5V Low Noise Regulator

Figure 40 extends Figure 38's cascoding technique in a step-down design.¹⁵ Inputs from 20V to 50V are converted to a 5V/2A capacity output. Q3 and Q4 protect the regulators V_{IN} pin from the high input voltages. The cascode must accommodate 100V transformer swings. In this instance MOSFETs (Q1-Q2) are utilized, although the divider technique is necessarily retained. RC gate damper networks prevent transformer swings coupled via gate-channel capacitance from corrupting the cascode's waveform transfer fidelity. Figure 41 shows that resultant cascode response is faithful, even with 100V swings. Trace A is Q1's source, with Traces B and C its gate and drain, respectively. Under these conditions, at 2A output, noise is inside 400 μ V peak. Note that Q3 and Q4 protect the regulator from excessive input voltages.

10W, 5V to 12V Low Noise Regulator

Figure 42 boosts the regulator's 1A output capability to over 5A. It does this with simple emitter followers (Q1-Q2). Theoretically, the followers preserve T1's voltage and current waveform information, permitting the LT1533's slew control circuitry to function. In practice, the transistors must be relatively low beta types. At 3A collector current their beta of 20 sources \approx 150mA via the Q1-Q2 base paths, adequate for proper slew loop operation.¹⁶ The follower loss limits efficiency to about 68%. Higher input voltages minimize follower-induced loss, permitting efficiencies in the low 70% range.

Figure 43 shows noise performance. Ripple measures 4mV (Trace A) using a single LC section, with high frequency content just discernible. Adding the optional second LC section drops ripple below 100 μ V (Trace B), and high frequency content is seen (note \times 50 vertical scale factor change) to be inside 180 μ V.

7500V Isolated Low Noise Supply

A final form of performance augmentation is extremely high voltage isolation. This is often required in situations where circuitry must withstand high common mode voltage effects. Figure 44 is similar to Figure 25's isolated supply, except that it has 7500V (peak) breakdown capability. Transformer and optoisolator changes permit this. The remaining operating and performance characteristics are identical to Figure 25.

Note 15: This circuit was developed from a design by Jeff Witt of Linear Technology Corporation.

Note 16: Operating the slew loops from follower base current was suggested by Bob Dobkin of Linear Technology Corporation.

Application Note 70

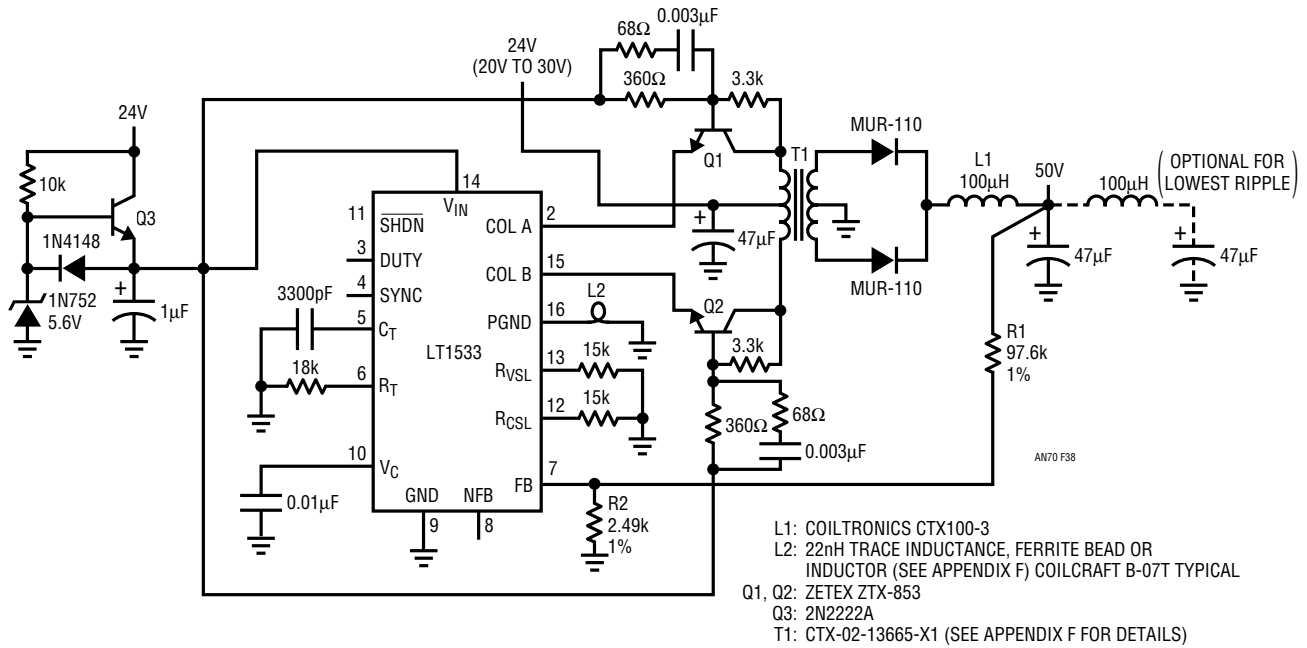


Figure 38. A 50V Output Low Noise Regulator. Cascode Bipolar Transistors Accommodate 60V Transformer Swings, Permitting 24V (20V_{IN} to 30V_{IN}) Powered Operation

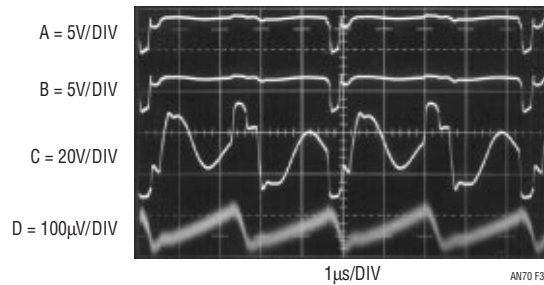


Figure 39. Cascode Transmits Instantaneous Voltage and Slew Information, Permitting LT1533 to Maintain Low Noise Output. Trace A is Q1 Emitter, Trace B Is Its Base and Trace C the Collector. Transformer Ring-Off Obscures Cascode Action, but Study Reveals Faithful Transmission. Output (Trace D) Has 100μV Noise

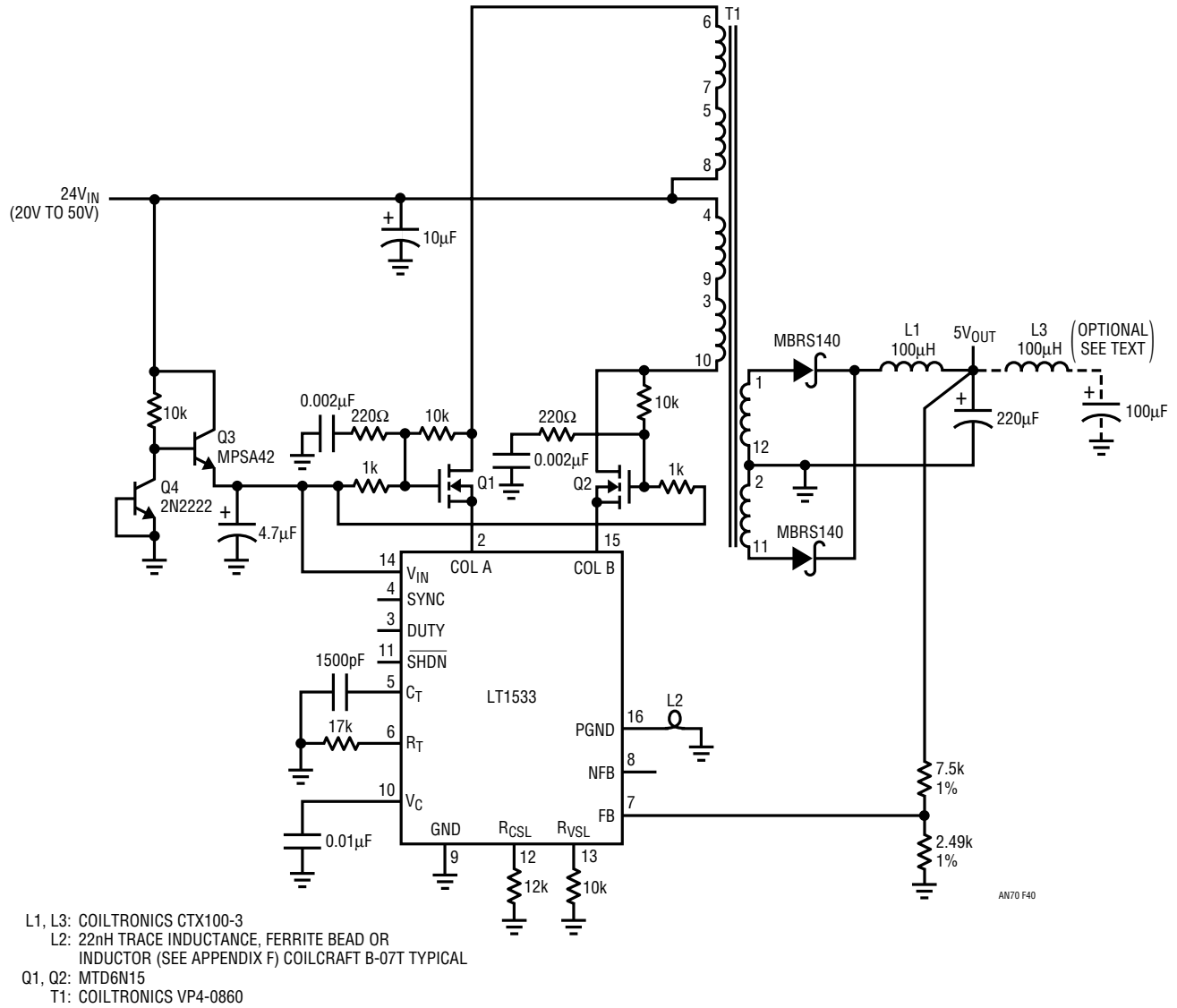


Figure 40. A Low Noise 24V-(20V_{IN} to 50V_{IN})-to-5V Converter. Cascoded MOSFETs Withstand 100V Transformer Swings, Permitting LT1533 to Control 5V/2A Output

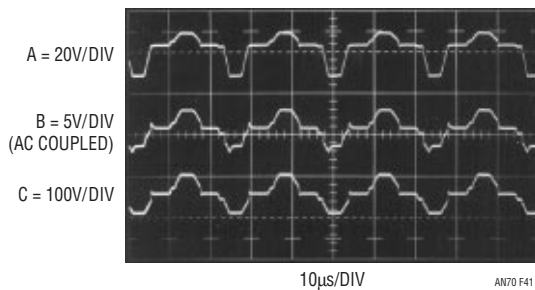


Figure 41. MOSFET-Based Cascode Permits Regulator to Control 100V Transformer Swings While Maintaining Low Noise 5V Output. Trace A Is Q1's Source, Trace B Q1's Gate and Trace C the Drain. Waveform Fidelity Through Cascode Permits Proper Slew Control Operation

Application Note 70

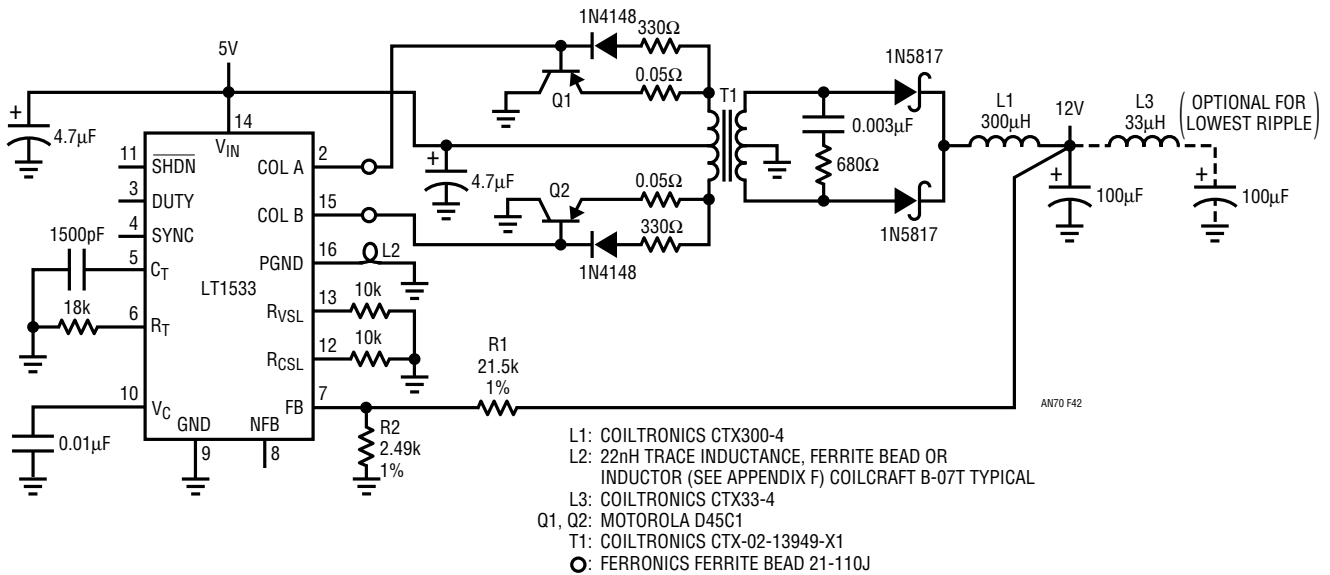


Figure 42. A 10W Low Noise 5V-to-12V Converter. Q1-Q2 Provide 5A Output Capacity While Preserving LT1533's Voltage/Current Slew Control. Efficiency Is 68%. Higher Input Voltages Minimize Follower Loss, Boosting Efficiency Above 71%

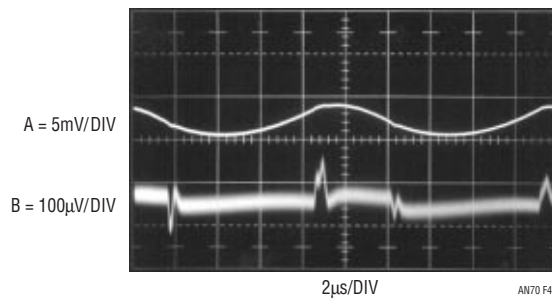


Figure 43. Waveforms for Figure 42 at 10W Output. Trace A Shows Fundamental Ripple with Higher Frequency Residue Just Discernible. Optional LC Section Produces Trace B's 180µV_{p,p} Wideband Noise Performance

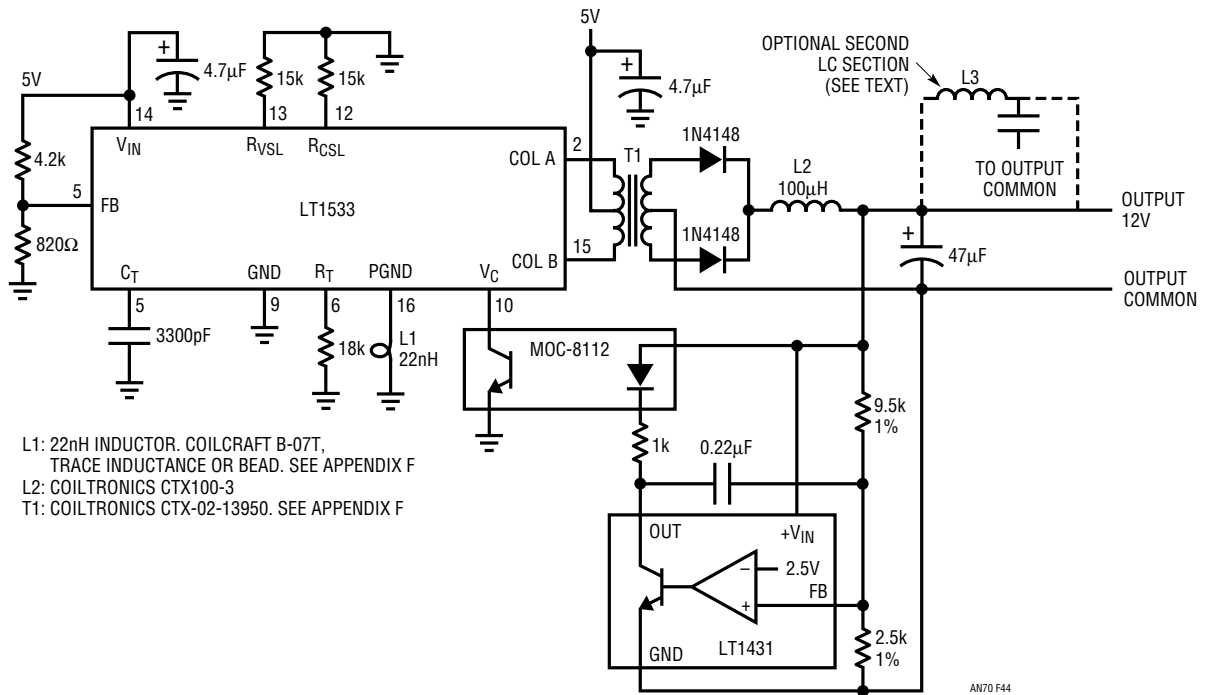


Figure 44. A 7500V Isolation Version of Figure 25. Transformer and Optoisolator Are Changed to Achieve Isolation and Noise Immunity. Circuit Operation Is as Before

Note: This Application Note was derived from a manuscript originally prepared for publication in EDN magazine.

Application Note 70

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APPENDIX A

A HISTORY OF LOW NOISE DC/DC CONVERSION

Why are batteries low noise power sources? Why do 60Hz AC power line derived linear regulators have low output noise? As with most innocent questions, thoughtful answers provide surprising insights. These sources have low output noise because they have low harmonic energy content. A 60Hz fundamental driven supply produces some harmonic activity, but power becomes very small well inside 1kHz. A battery is even better.

These conclusions set a direction towards designing low noise DC/DC converters. If the goal is low noise, the key is reduction of harmonic energy, in particular, wideband harmonics. This simple guideline is central to LT1533 operation, although refinements are necessary for a generally applicable IC.

History

The notion of minimizing harmonics in DC/DC conversion to get low output noise is not new. Oscilloscopes have used this technique to generate high voltage CRT accelerating potentials without degrading instrument operation.¹ Designing a 10,000V output DC/DC converter that does not disrupt a 500MHz, high sensitivity vertical amplifier is challenging.

Figure A1 shows the CRT DC/DC converter from a Tektronix 454 oscilloscope. Q1430, configured as a modified Hartley power oscillator, drives T1430. T1430's output is multiplied by the diode-capacitor tripler, producing 12,000V. Feedback to Q1414 is summed against a 75V derived reference, closing a regulation loop around the power oscillator.

The sine wave transformer drive (see waveforms in the figure) has low harmonic content, resulting in the desired low conducted and radiated noise. This approach is not very efficient—Q1430 operates in its linear region—but the power loss is acceptable in a 125W instrument.

Tektronix 7000 series oscilloscopes used a resonant, off-line converter to power the entire instrument. As before, CRT high voltage was generated separately (see Footnote

1). Figure A2, a partial schematic of a Tektronix 7904 power converter, shows a series resonant network, L1237-C1237 in the Q1234-Q1241 drive path. This results in sine wave drive to output transformer T1310, despite Q1234-Q1241's rectangular waveshape. Feedback (not shown) closes a loop around this stage, stabilizing its operating point. The resonant, sine wave transformer drive provides the desired low noise characteristics with good efficiency.

A less specific example appears in LTC Application Note 29. Figure A3, a partial schematic of Application Note 29's Figure 4, shows a sine wave oscillator (A1 based) driving a power amplifier (A3 and Q2 to Q6). L3, the output transformer, provides voltage boosted secondary drive to linear regulators (not shown). This brute force approach provides a converter with extraordinarily low noise, but is complex and inefficient. Q4 and Q5, operating in their linear regions, dissipate considerable power, and efficiency is 30%.

Figure A4's approach, also from AN29's Figure 1, achieves better efficiency. The partial schematic shows source followers driven from 100Ω-0.003μF edge slow-down networks. This slows down the transistor's transitions, resulting in harmonic reduction and low noise. Unfortunately, the drive scheme is complex and somewhat inflexible, requiring bootstrapped voltages to fully switch the transistors on and off. Additionally, a transformer change would require drive rework to maintain efficiency and low noise characteristics. Finally, the dynamic voltage and current control in the transistors is passively determined and not very well controlled.

The LT1533 uses closed-loop control² around its output stages to tightly control voltage and current slewing. This allows a variety of circuits and magnetics to be easily accommodated, resulting in a true general purpose solution. Text Figure 3 and the associated discussion provide more LT1533 operating details.

Note 1: Ancillary benefits include eliminating a complex and expensive high voltage winding in the main power transformer, avoidance of long, high voltage wire runs and space and weight savings.

Note 2: Patent pending.

Application Note 70

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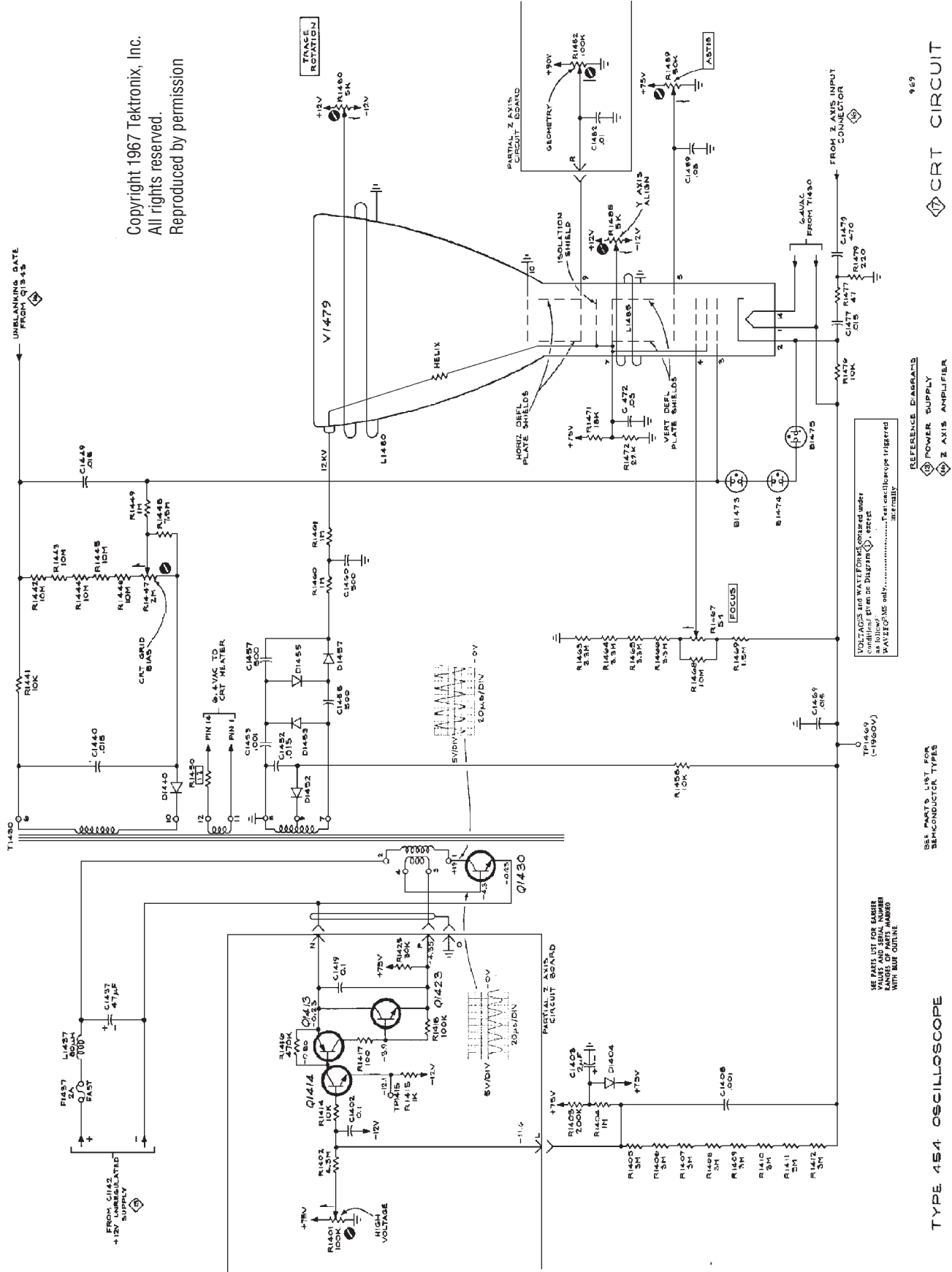
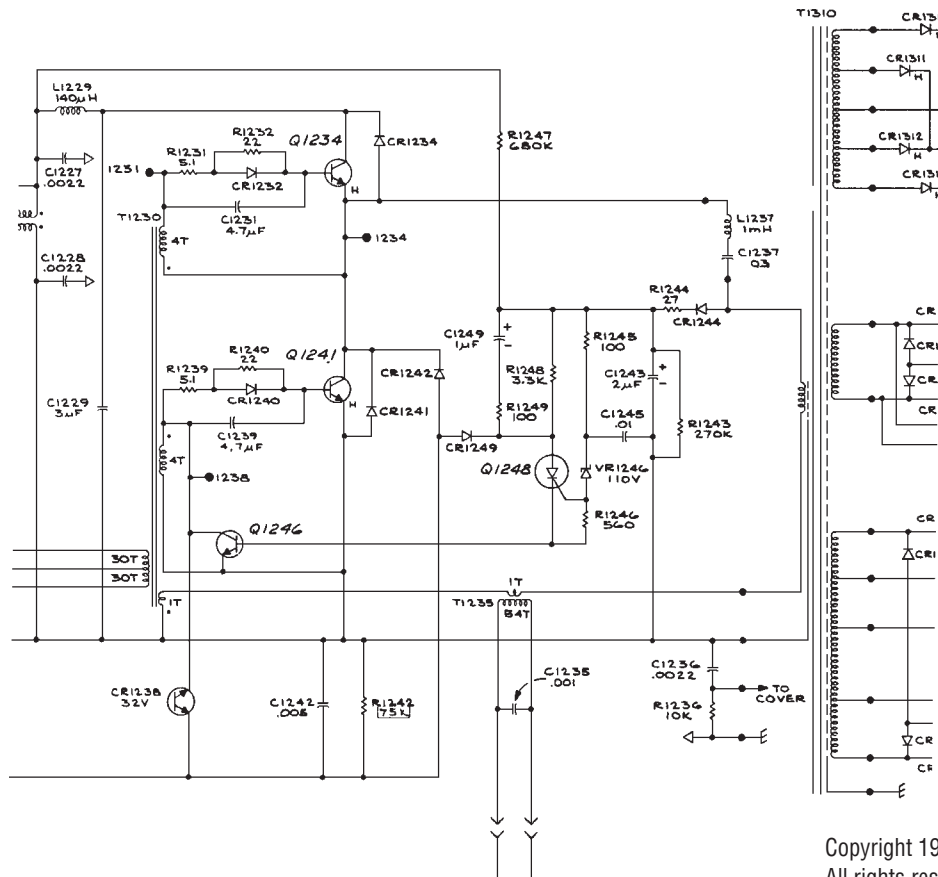


Figure A1. Tektronix 454 CRT Circuit Uses Sine Wave Drive for Low Noise DC/DC Conversion. Efficiency Is Poor, Because Q1430 Remains in Linear Region



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Figure A2. Tektronix 7904 Main Inverter Obtains Low Noise by Converting Q1234-Q1241 Rectangular Drive to Sine Wave via L1237-C1237 Resonating Network. Output Transformer Produces Low Noise Power with Good Efficiency. Approach Is Application Specific and Inflexible

Application Note 70

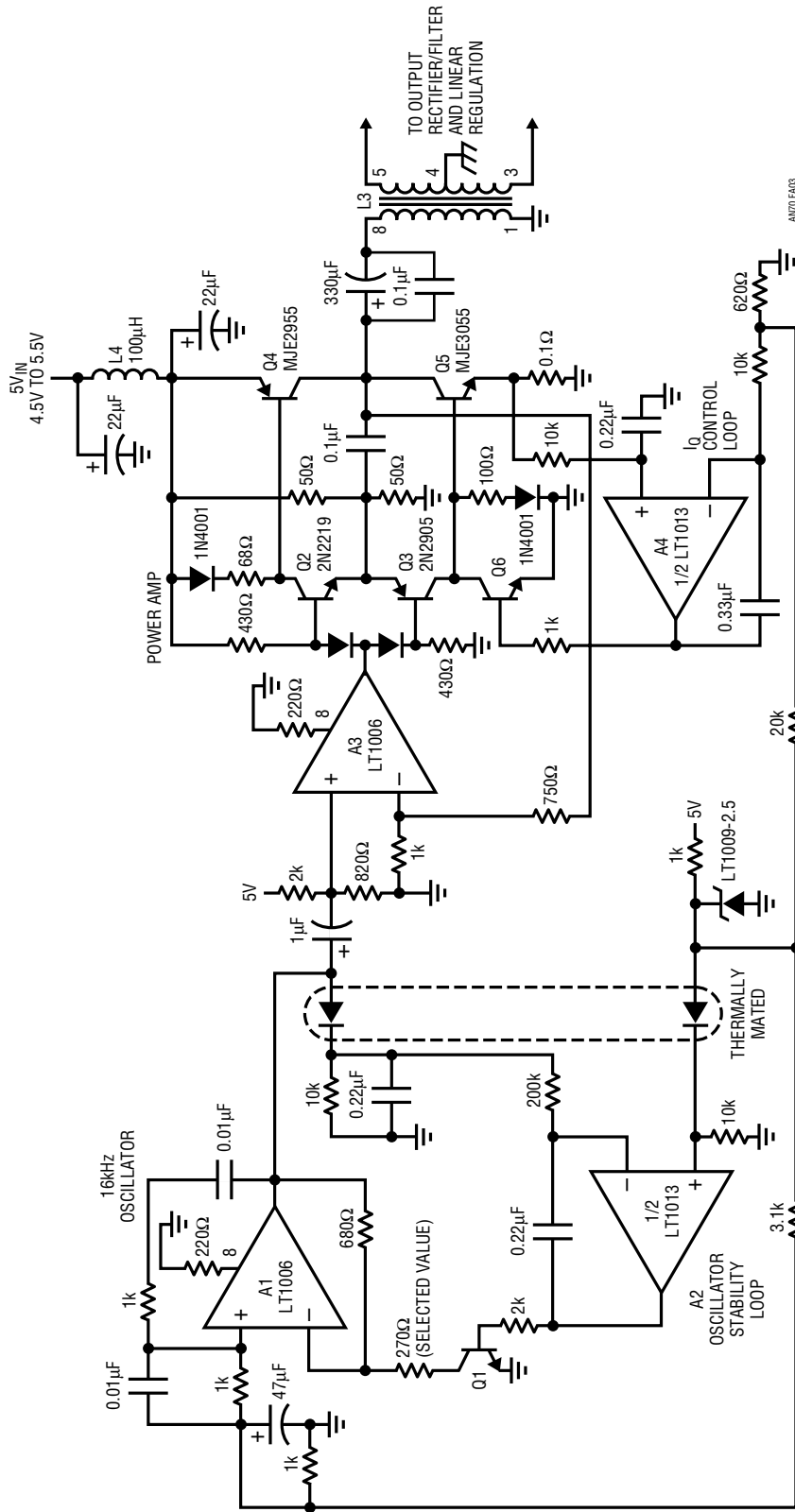


Figure A3. Sine Wave-Based DC/DC Converter Appeared in LC Application Note 29. Output Noise Is Low, but Circuit Is Complex and Inefficient

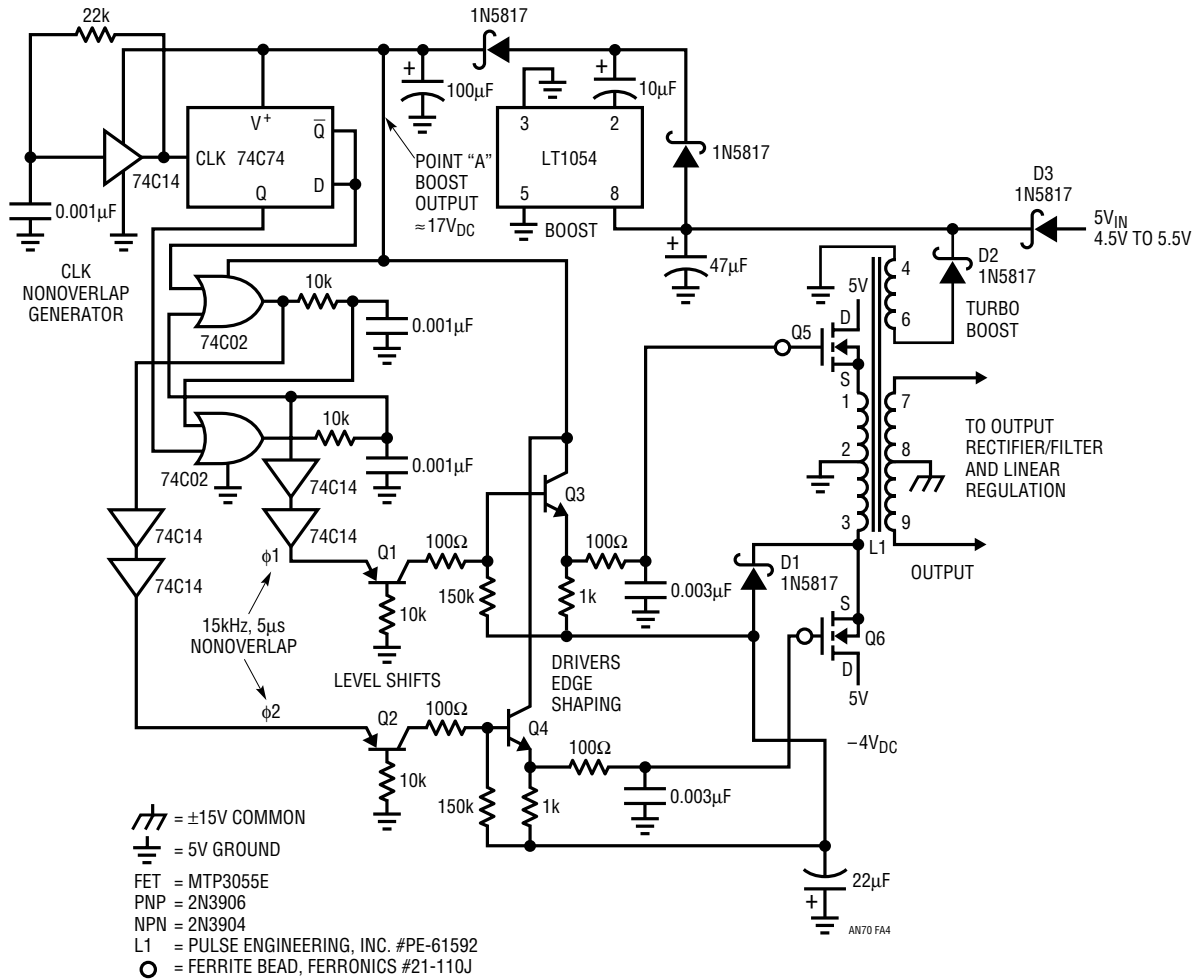


Figure A4. LTC Application Note 29 Circuit Slopes Edge Drive for Low Noise and Better Efficiency. Gate Drive Circuitry is Complex and Poorly Controlled, Making Circuit Inflexible

Application Note 70

APPENDIX B

SPECIFYING AND MEASURING SOMETHING CALLED NOISE

Undesired output components in switching regulators are commonly referred to as “noise.” The rapid, switched mode power delivery that permits high efficiency conversion also creates wideband harmonic energy. This undesirable energy appears as radiated and conducted components, or “noise.” Actually switching regulator output “noise” isn’t really noise at all, but coherent, high frequency residue directly related to the regulator’s switching. Unfortunately, it is almost universal practice to refer to these parasitics as “noise,” and this publication maintains this common, albeit inaccurate, terminology.¹

Measuring Noise

There are an almost uncountable number of ways to specify noise in a switching regulator’s output. It is common industrial practice to specify peak-to-peak noise in a 20MHz bandpass.² Realistically, electronic systems are readily upset by spectral energy beyond 20MHz, and this specification restriction benefits no one.³ Considering all this, it seems appropriate to specify peak-to-peak noise in a verified 100MHz bandwidth. Reliable low level measurements in this bandpass require careful instrumentation choice and connection practices.

Our study begins by selecting test instrumentation and verifying its bandwidth and noise. This necessitates the arrangement shown in Figure B1. Figure B2 diagrams signal flow. The pulse generator supplies a subnanosecond rise time step to the attenuator, which produces a <1mV version of the step. The amplifier takes 40dB of gain ($A = 100$) and the oscilloscope displays the result. The “front-to-back” cascaded bandwidth of this system should be about 100MHz ($t_{rise} = 3.5ns$) and Figure B3 reveals this to be so. Figure B3’s trace shows 3.5ns rise time and about

100 μ V of noise. The noise is limited by the amplifier’s 50 Ω noise floor.⁴

Figure B4’s presentation of text Figure 5’s output noise shows barely visible switching artifacts (at vertical graticule lines 4, 6 and 8) in the 100MHz bandpass. Fundamental ripple is seen more clearly, although similarly noise floor dominated. Restricting measurement bandwidth to 10MHz (Figure B5) reduces noise floor amplitude, although switching noise and ripple amplitudes are preserved. This indicates that there is no signal power beyond 10MHz. Further measurements as bandwidth is successively reduced can determine the highest frequency content present.

The importance of measurement bandwidth is further illustrated by Figures B6 to B8. Figure B6 measures a commercially available DC/DC converter in a 1MHz bandpass. The unit appears to meet its claimed 5mV_{P-P} noise specification. In Figure B7, bandwidth is increased to 10MHz. Spike amplitude enlarges to 6mV_{P-P}, about 1mV outside the specification limit. Figure B8’s 50MHz viewpoint brings an unpleasant surprise. Spikes measure 30mV_{P-P}—six times the specified limit!⁵

Note 1: Less genteelly, “If you can’t beat ‘em, join ‘em.”

Note 2: One DC/DC converter manufacturer specifies *RMS* noise in a 20MHz bandwidth. This is beyond deviousness and unworthy of comment.

Note 3: Except, of course, eager purveyors of power sources who specify them in this manner.

Note 4: Observed peak-to-peak noise is somewhat affected by the oscilloscope’s “intensity” setting. Reference 11 describes a method for normalizing the measurement.

Note 5: Caveat Emptor.



Figure B1. 100MHz Bandwidth Verification Test Setup.
Note Coaxial Connections for Wideband Signal Integrity

Application Note 70

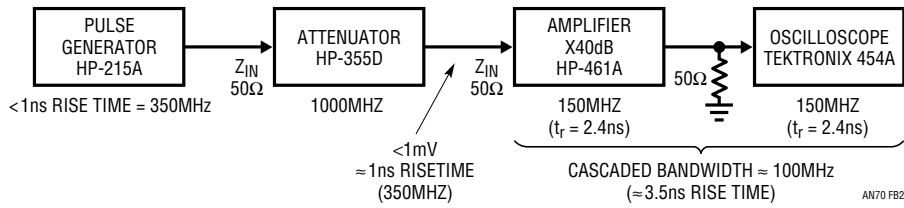


Figure B2. Subnanosecond Pulse Generator and Wideband Attenuator Provide Fast Step to Verify Test Setup Bandwidth

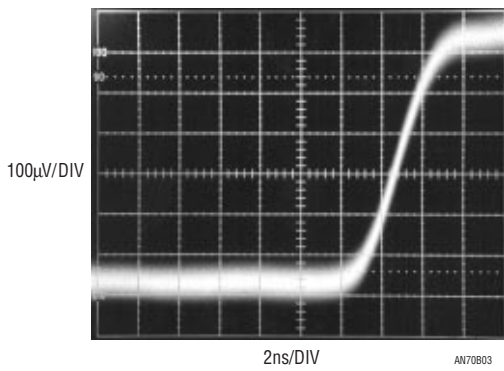


Figure B3. Oscilloscope Display Verifies Test Setup's 100MHz (3.5ns Rise Time) Bandwidth. Baseline Noise Derives from Amplifier's 50Ω Input Noise Floor

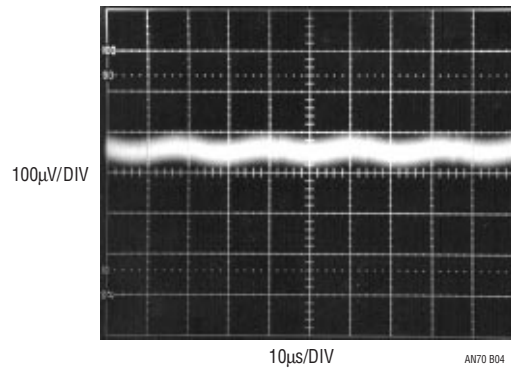


Figure B4. Text Figure 5's Output Switching Noise Is Just Discernible in A 100MHz Bandpass

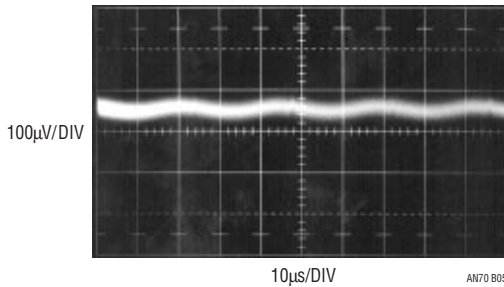


Figure B5. 10MHz Band Limited Version of Preceding Photo. All Switching Noise Information Is Preserved, Indicating Adequate Bandwidth

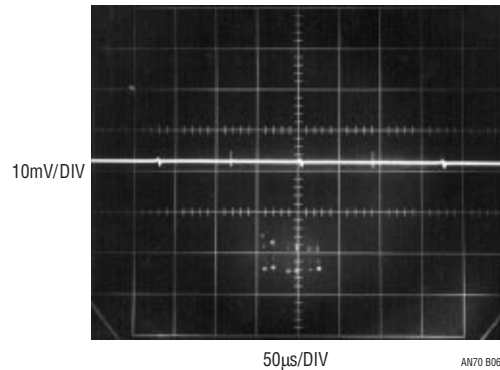


Figure B6. Commercially Available Switching Regulator's Output Noise in a 1MHz Bandpass. Unit Appears to Meet Its 5mV_{p,p} Noise Specification

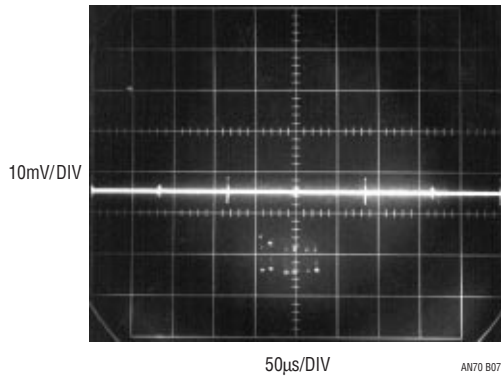


Figure B7. Figure A6's Regulator Noise in a 10MHz Bandpass. 6mV_{P-P} Noise Exceeds Regulator's Claimed 5mV Specification

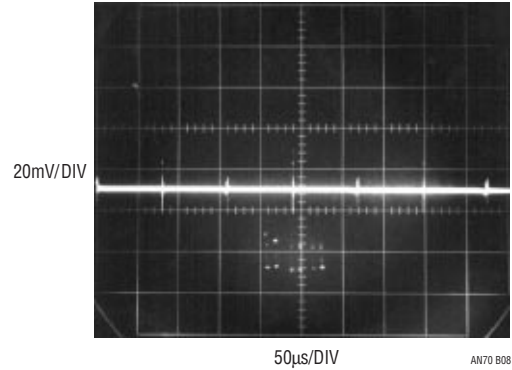


Figure B8. Wideband Observation of Figure A7 Shows 30mV_{P-P} Noise—Six Times the Regulator's Specification!

Low Frequency Noise

Low frequency noise is rarely a concern, because it almost never affects system operation. Text Figure 5's low frequency noise is shown in Figure B9. It is possible to reduce low frequency noise by rolling off control loop bandwidth (e.g., via a 0.68µF feedback capacitor across R1 and V_C value of 2000pF in text Figure 5). Figure B10 shows about a five times improvement when this is done, even with greater measurement bandwidth. A possible disadvantage is loss of loop bandwidth and slower transient response.

Preamplifier and Oscilloscope Selection

The low level measurements described require some form of preamplification for the oscilloscope. Current generation oscilloscopes rarely have greater than 2mV/DIV sensitivity, although older instruments offer more capability. Figure B11 lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These

units feature wideband, low noise performance. It is particularly significant that the majority of these instruments are no longer produced. This is in keeping with current instrumentation trends, which emphasize digital signal acquisition as opposed to analog measurement capability.

The monitoring oscilloscope should have adequate bandwidth and exceptional trace clarity. In the latter regard high quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments is well-suited to low level noise measurement.⁶ The digitizing uncertainties and raster scan limitations of DSOs impose display resolution penalties. Many DSO displays will not even register the small levels of switching-based noise.

Note 6: In our work we have found Tektronix types 454, 454A, 547 and 556 excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise floor limited background.

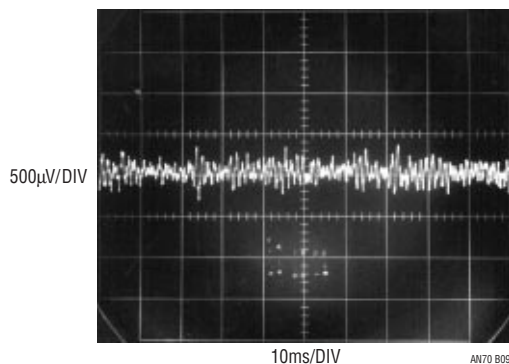


Figure B9. 1Hz to 3kHz Noise Using Standard Frequency Compensation. Almost All Noise Power Is Below 1kHz

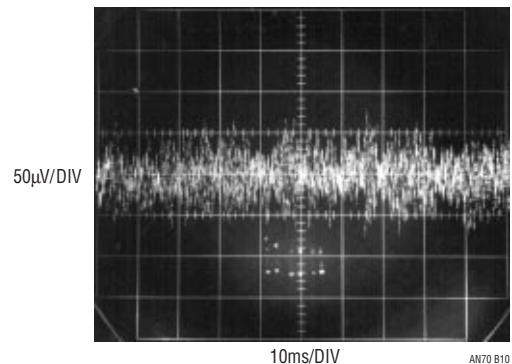


Figure B10. Feedback Lead Network Decreases Low Frequency Noise, Even as Measurement Bandwidth Expands to 100kHz

Application Note 70

INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	BANDWIDTH	MAXIMUM SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Amplifier	Hewlett-Packard	461A	150MHz	Gain = 100	Secondary Market	50Ω Input, Stand-Alone
Differential Amplifier	Tektronix	1A5	50MHz	1mV/DIV	Secondary Market	Requires 500 Series Mainframe
Differential Amplifier	Tektronix	7A13	100MHz	1mV/DIV	Secondary Market	Requires 7000 Series Mainframe
Differential Amplifier	Tektronix	11A33	150MHz	1mV/DIV	Secondary Market	Requires 11000 Series Mainframe
Differential Amplifier	Tektronix	P6046	100MHz	1mV/DIV	Secondary Market	Stand-Alone
Differential Amplifier	Preamble	1855	100MHz	Gain = 10	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Tektronix	1A7/1A7A	1MHz	10μV/DIV	Secondary Market	Requires 500 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	7A22	1MHz	10μV/DIV	Secondary Market	Requires 7000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	5A22	1MHz	10μV/DIV	Secondary Market	Requires 5000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	ADA-400A	1MHz	10μV/DIV	Current Production	Stand-Alone with Optional Power Supply, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 1000	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Stanford Research Systems	SR-560	1MHz	Gain = 50000	Current Production	Stand-Alone, Settable Bandstops, Battery or Line Operation

Figure B11. Some Applicable High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Bandwidth, Sensitivity and Availability

APPENDIX C

PROBING AND CONNECTION TECHNIQUES FOR LOW LEVEL, WIDEBAND SIGNAL INTEGRITY

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. The low level, wideband measurements demand care in routing signals to test instrumentation.

This problem can be avoided by grounding all line powered test equipment at the same outlet strip or otherwise ensuring that all chassis are at the same ground potential. Similarly, any test arrangement that permits circuit current flow in chassis interconnects must be avoided.

Ground Loops

Figure C1 shows the effects of a ground loop between pieces of line-powered test equipment. Small current flow between test equipment's nominally grounded chassis creates 60Hz modulation in the measured circuit output.

Pickup

Figure C2 also shows 60Hz modulation of the noise measurement. In this case, a 4-inch voltmeter probe at the feedback input is the culprit. *Minimize the number of test connections to the circuit and keep leads short.*

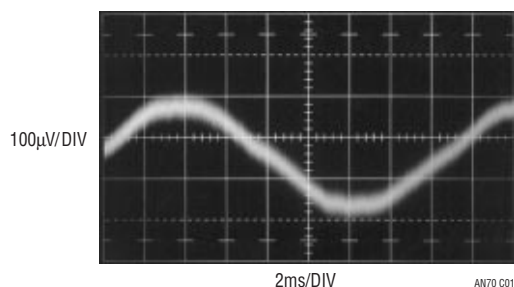


Figure C1. Ground Loop Between Pieces of Test Equipment Induces 60Hz Display Modulation

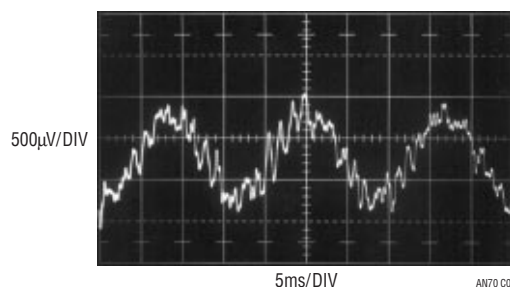


Figure C2. 60Hz Pickup Due to Excessive Probe Length at Feedback Node

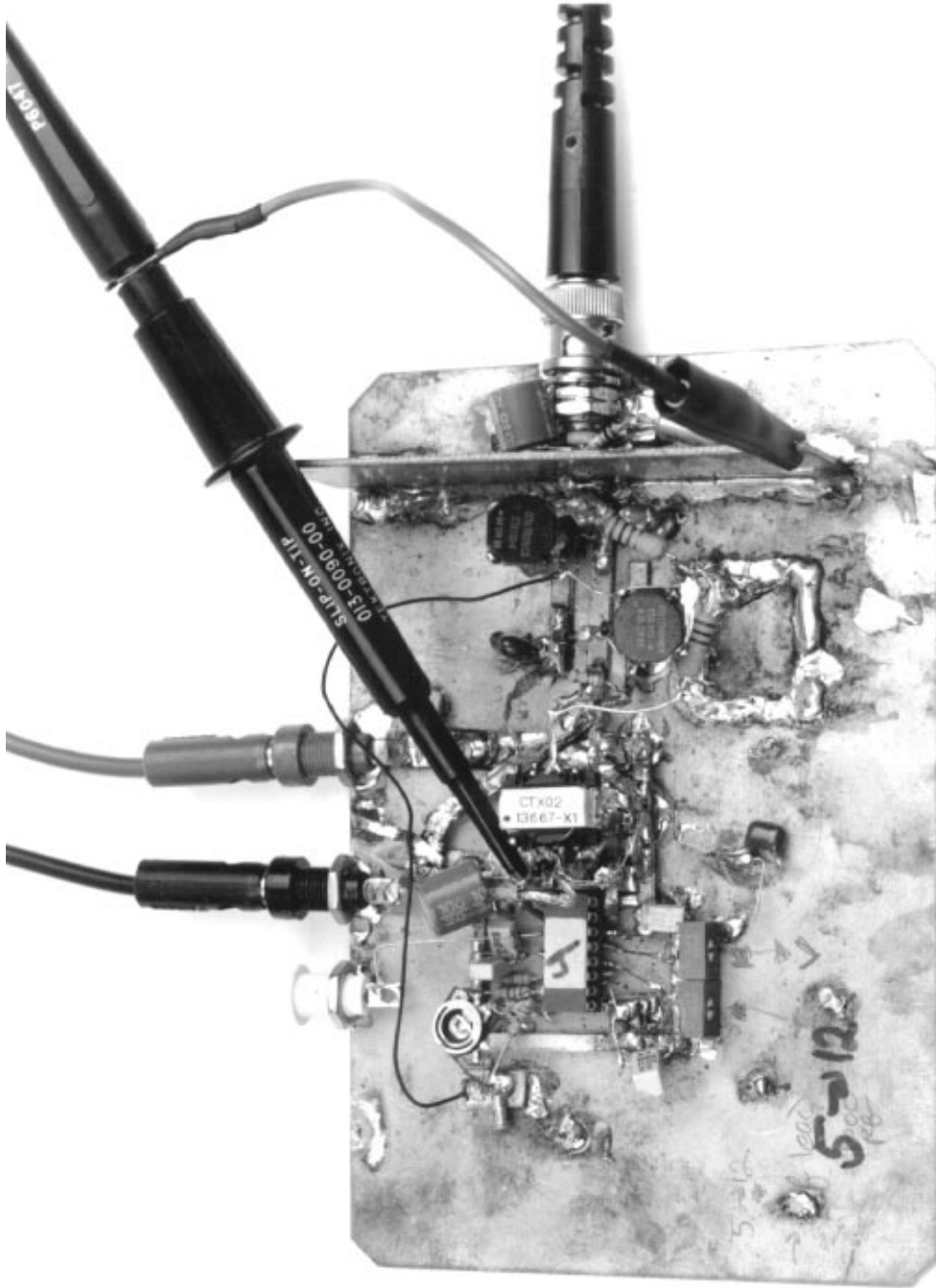


Figure C3. Poor Probing Technique. Trigger Probe Ground Lead Can Cause Ground Loop-Induced Artifacts to Appear in Display

Application Note 70

Poor Probing Technique

Figure C3's photograph shows a short ground strap affixed to a scope probe. The probe connects to a point which provides a trigger signal for the oscilloscope. Circuit output noise is monitored on the oscilloscope via the coaxial cable shown in the photo.

Figure C4 shows results. A ground loop on the board between the probe ground strap and the ground referred cable shield causes apparent excessive ripple in the display. *Minimize the number of test connections to the circuit and avoid ground loops.*

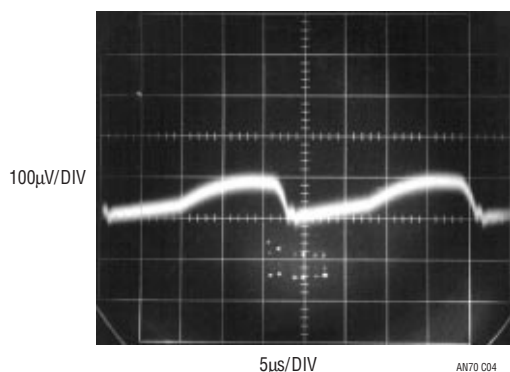


Figure C4. Apparent Excessive Ripple Results from Figure C3's Probe Misuse. Ground Loop on Board Introduces Serious Measurement Error

Violating Coaxial Signal Transmission—Felony Case

In Figure C5, the coaxial cable used to transmit the circuit output noise to the amplifier-oscilloscope has been replaced with a probe. A short ground strap is employed as the probe's return. The error inducing trigger channel probe in the previous case has been eliminated; the 'scope is triggered by a noninvasive, isolated probe.¹ Figure C6 shows excessive display noise due to breakup of the coaxial signal environment. The probe's ground strap violates coaxial transmission and the signal is corrupted by RF. *Maintain coaxial connections in the noise signal monitoring path.*

Violating Coaxial Signal Transmission—Misdemeanor Case

Figure C7's probe connection also violates coaxial signal flow, but to a less offensive extent. The probe's ground

strap is eliminated, replaced by a tip grounding attachment. Figure C8 shows better results over the preceding case, although signal corruption is still evident. *Maintain coaxial connections in the noise signal monitoring path.*

Proper Coaxial Connection Path

In Figure C9, a coaxial cable transmits the noise signal to the amplifier-oscilloscope combination. In theory, this affords the highest integrity cable signal transmission. Figure C10's trace shows this to be true. The former examples aberrations and excessive noise have disappeared. The switching residuals are now faintly outlined in the amplifier noise floor. *Maintain coaxial connections in the noise signal monitoring path.*

Direct Connection Path

A good way to verify there are no cable-based errors is to eliminate the cable. Figure C11's approach eliminates all cable between breadboard, amplifier and oscilloscope. Figure C12's presentation is indistinguishable from Figure C10, indicating no cable-introduced infidelity. *When results seem optimal, design an experiment to test them. When results seem poor, design an experiment to test them. When results are as expected, design an experiment to test them. When results are unexpected, design an experiment to test them.*

Test Lead Connections

In theory, attaching a voltmeter lead to the regulator's output should not introduce noise. Figure C13's increased noise reading contradicts the theory. The regulator's output impedance, albeit low, is not zero, especially as frequency scales up. The RF noise injected by the test lead works against the finite output impedance, producing the 200µV of noise indicated in the figure. If a voltmeter lead must be connected to the output during testing, it should be done through a 10kΩ-10µF filter. Such a network eliminates Figure C13's problem while introducing minimal error in the monitoring DVM. *Minimize the number of test lead connections to the circuit while checking noise. Prevent test leads from injecting RF into the test circuit.*

Note 1: To be discussed. Read on.

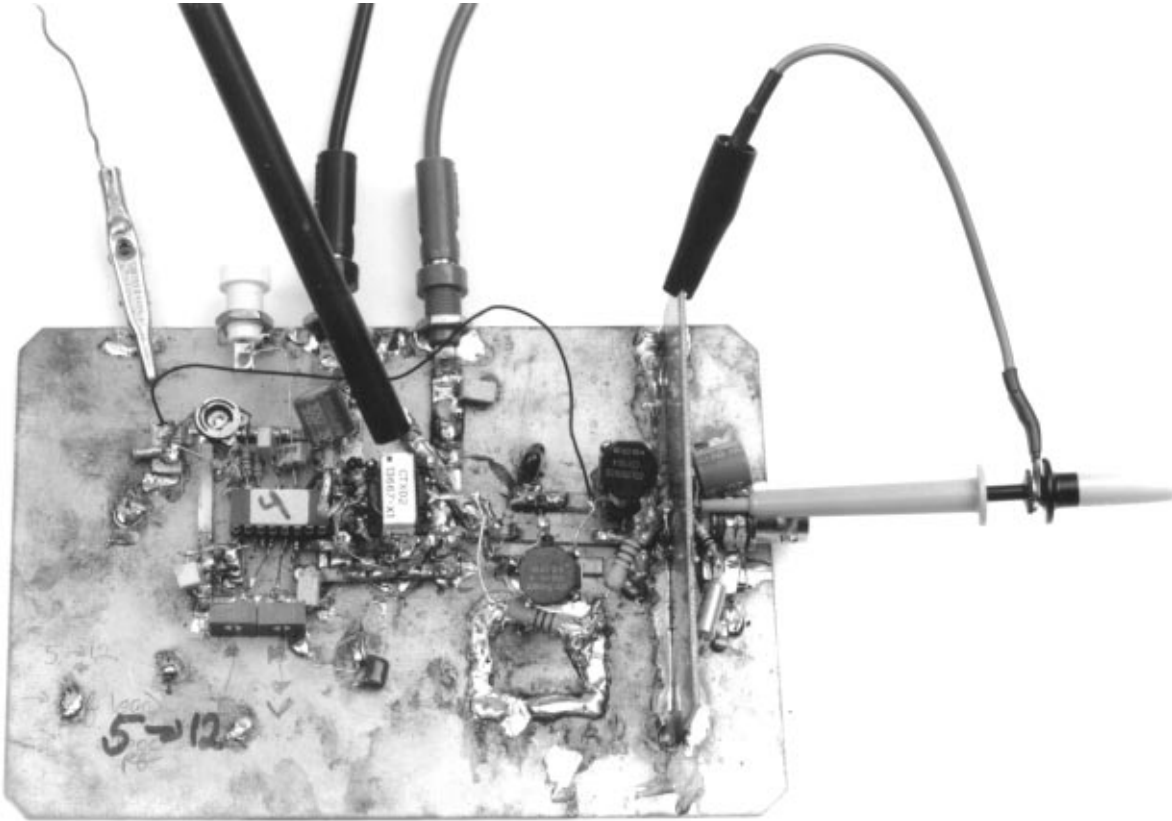


Figure C5. Floating Trigger Probe Eliminates Ground Loop, but Output Probe Ground Lead (Photo Upper Right) Violates Coaxial Signal Transmission

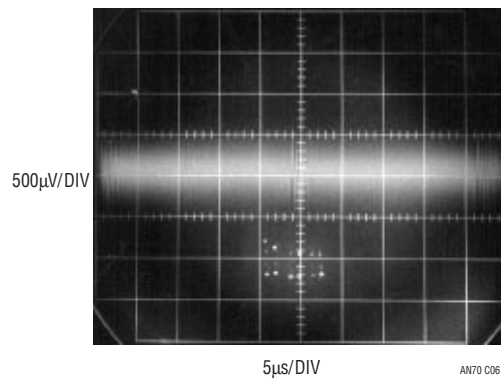


Figure C6. Signal Corruption Due to Figure C5's Noncoaxial Probe Connection

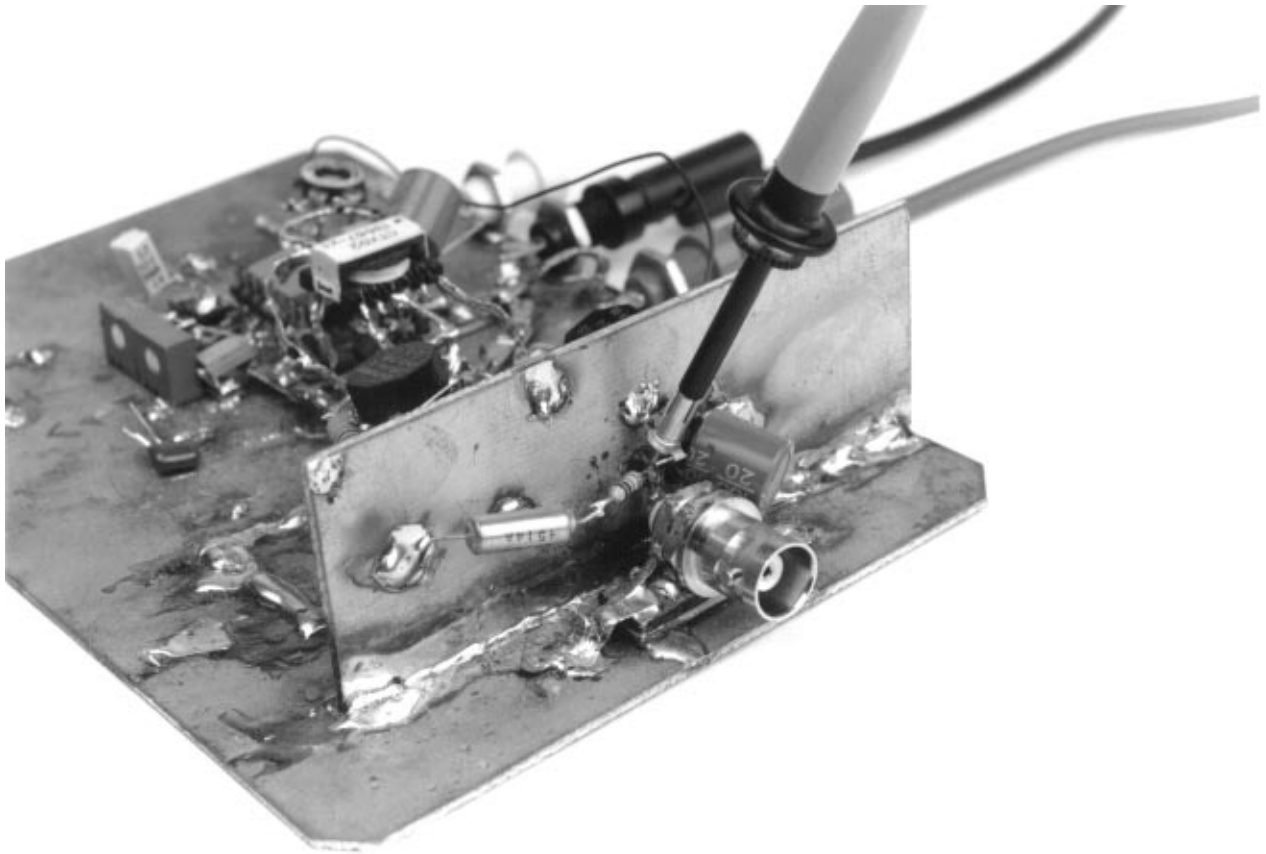


Figure C7. Probe with Tip Grounding Attachment Approximates Coaxial Connection

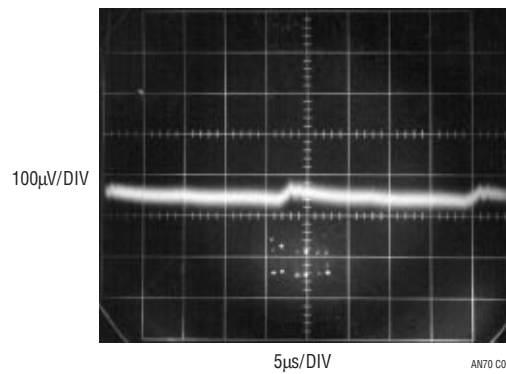


Figure C8. Probe with Tip Grounding Attachment Improves Results. Some Corruption Is Still Evident

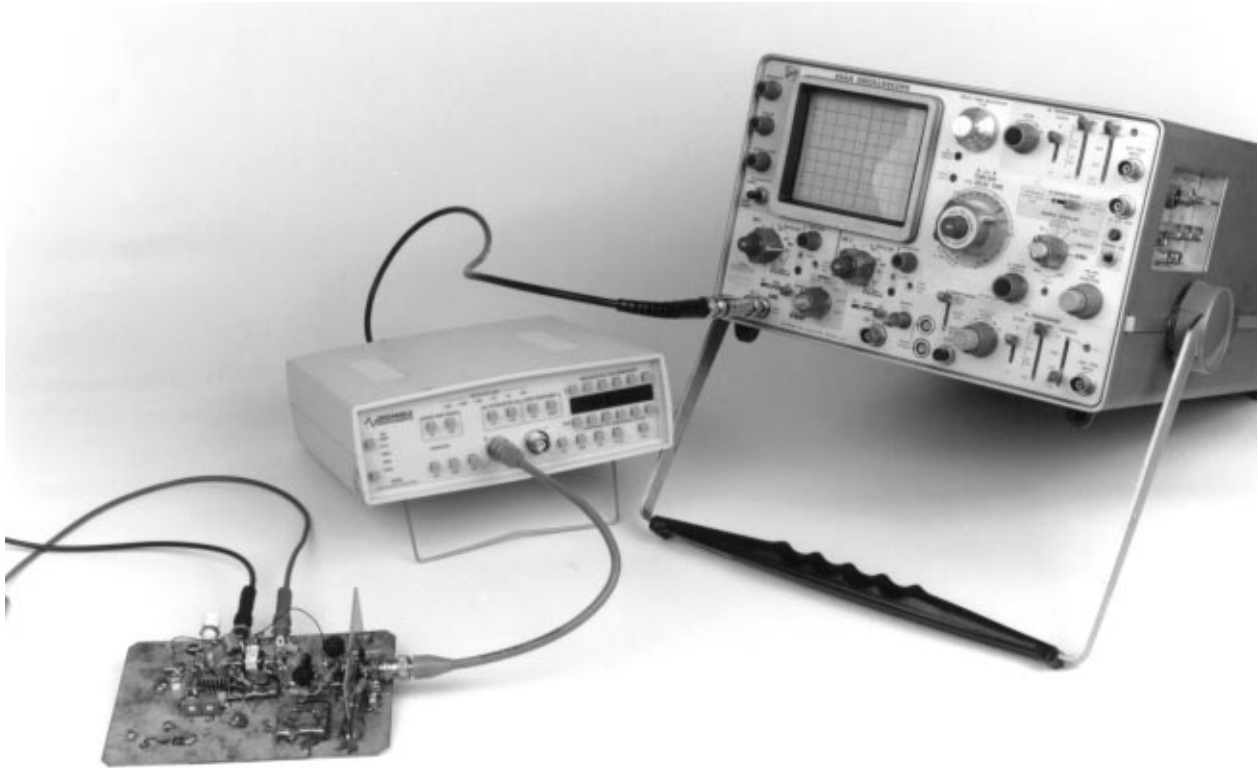


Figure C9. Coaxial Connection Theoretically Affords Highest Fidelity Signal Transmission

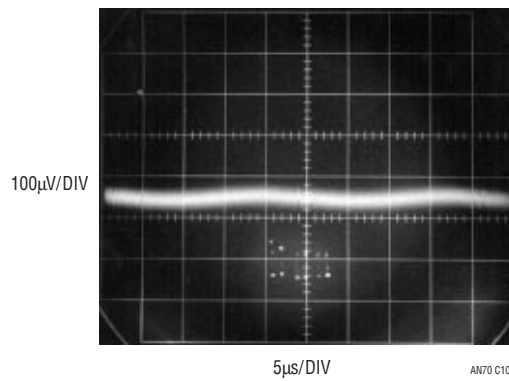


Figure C10. Life Agrees with Theory. Coaxial Signal Transmission Maintains Signal Integrity. Switching Residuals Are Faintly Outlined in Amplifier Noise

Application Note 70

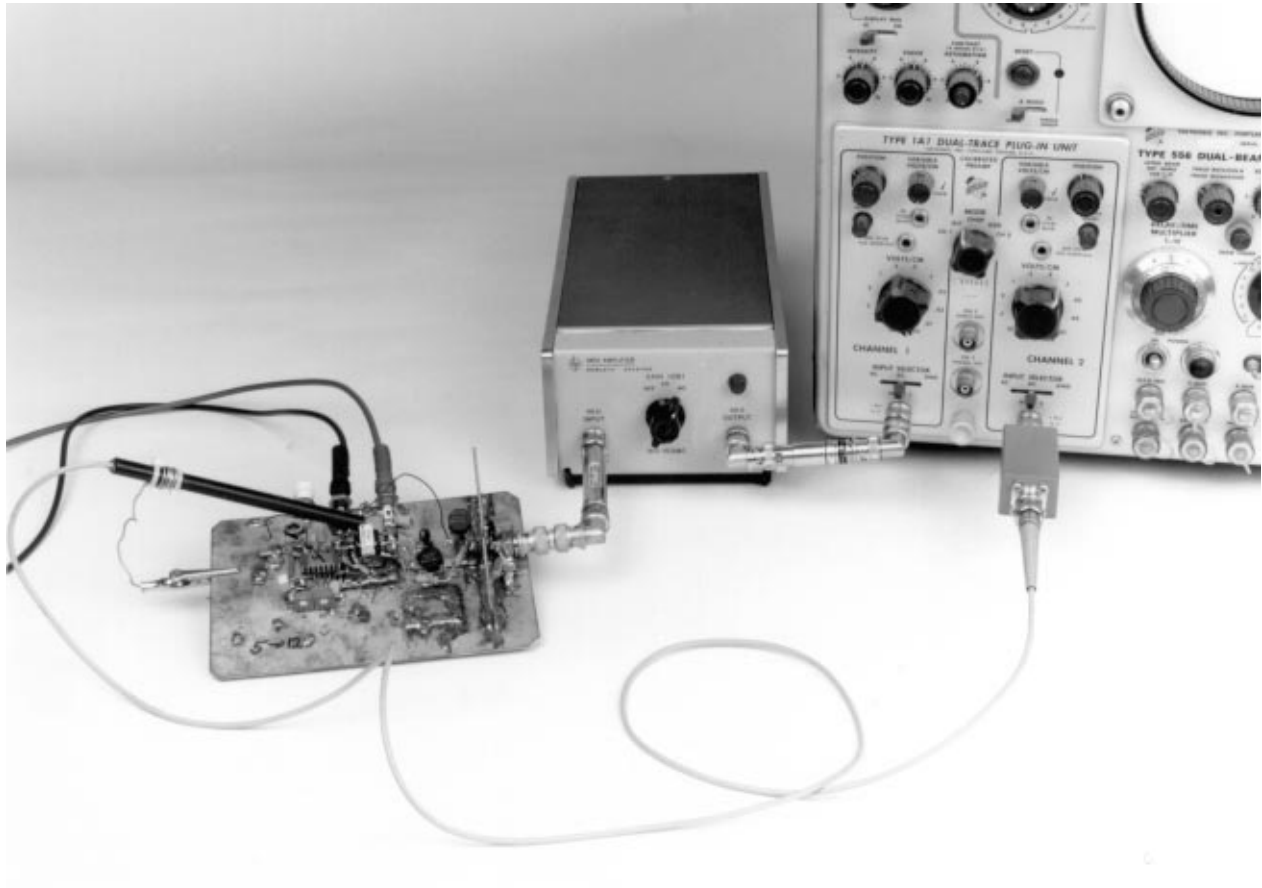


Figure C11. Direct Connection to Equipment Eliminates Possible Cable-Termination Parasitics, Providing Best Possible Signal Transmission

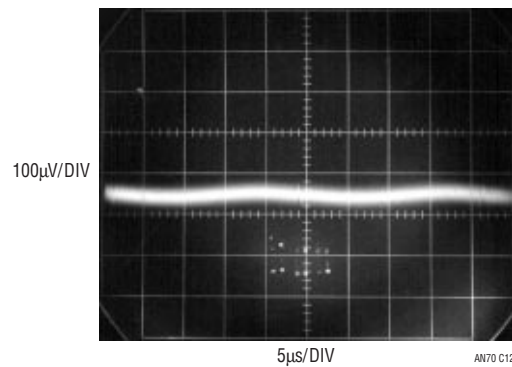


Figure C12. Direct Connection to Equipment Provides Identical Results to Cable-Termination Approach. Cable and Termination Are Therefore Acceptable

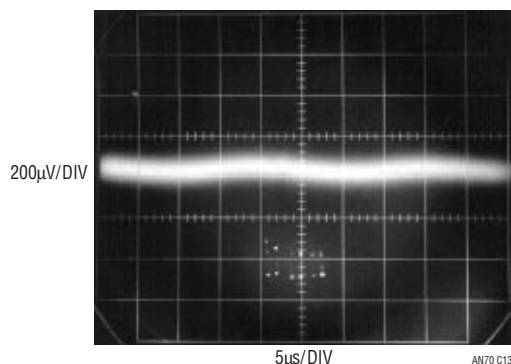


Figure C13. Voltmeter Lead Attached to Regulator Output Introduces RF Pickup, Multiplying Apparent Noise Floor

Isolated Trigger Probe

The text associated with Figure C5 somewhat cryptically alluded to an “isolated trigger probe.” Figure C14 reveals this to be simply an RF choke terminated against ringing. The choke picks up residual radiated field, generating an isolated trigger signal. This arrangement furnishes a 'scope trigger signal with essentially no measurement corruption. The probe's physical form appears in Figure C15. For good results the termination should be adjusted for minimum ringing while preserving the highest possible amplitude output. Light compensatory damping produces Figure C16's output, which will cause poor 'scope triggering. Proper adjustment results in a more favorable output (Figure C17), characterized by minimal ringing and well-defined edges.

Trigger Probe Amplifier

The field around the switching magnetics is small and may not be adequate to reliably trigger some oscilloscopes. In such cases, Figure C18's trigger probe amplifier is useful. It uses an adaptive triggering scheme to compensate for variations in probe output amplitude. A stable 5V trigger output is maintained over a 50:1 probe output range. A1, operating at a gain of 100, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's

output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1116's positive input. The LT1116's negative input is biased directly from A1's output. The LT1116's output, the circuit's trigger output, is unaffected by >50:1 signal amplitude variations. An X100 analog output is available at A1.

Figure C19 shows the circuit's digital output (Trace B) responding to the amplified probe signal at A1 (Trace A).

Figure C20 is a typical noise testing setup. It includes the breadboard, trigger probe, amplifier, oscilloscope and coaxial components.

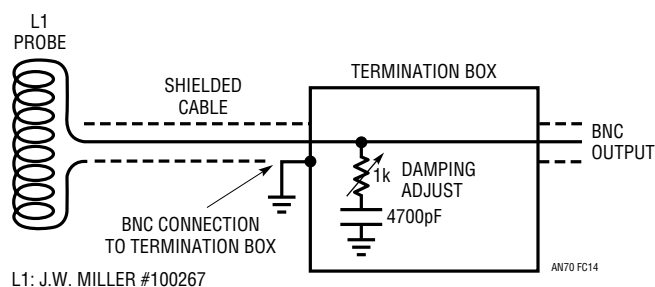


Figure C14. Simple Trigger Probe Eliminates Board Level Ground Loops. Termination Box Components Damp L1's Ringing Response

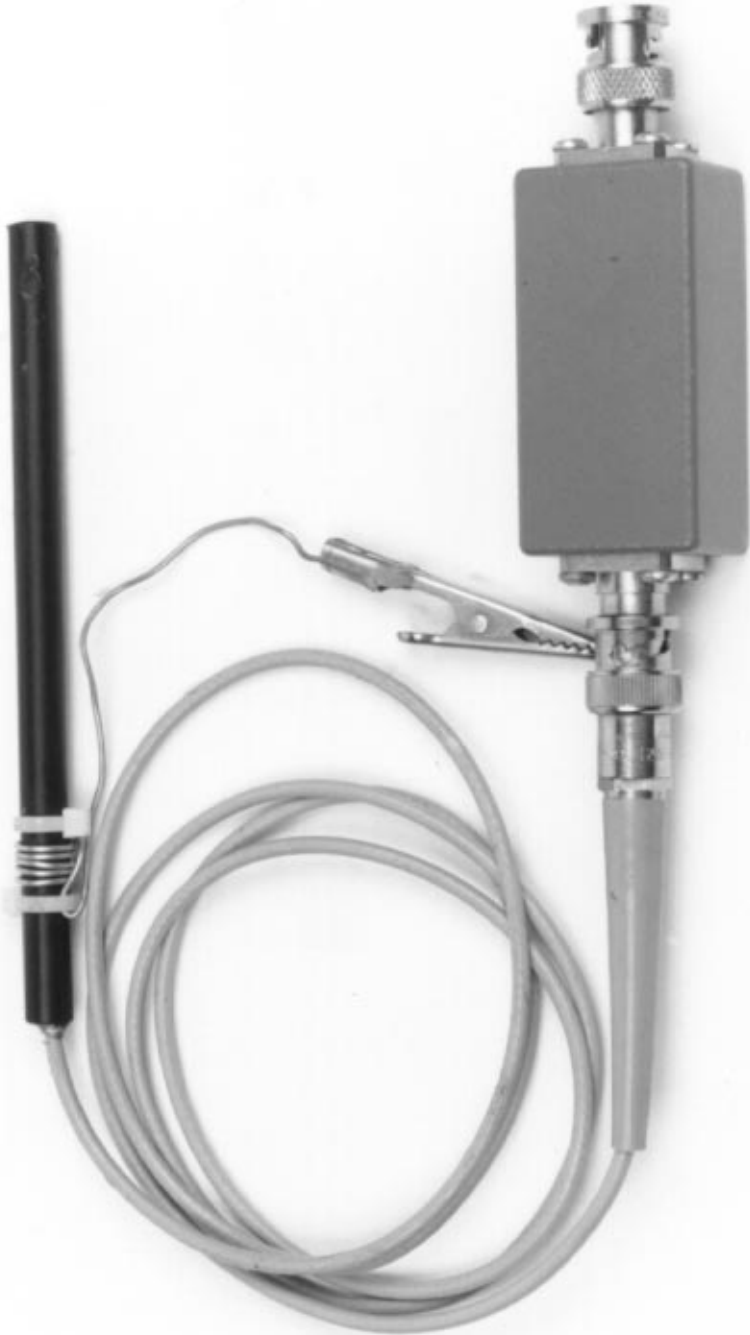


Figure C15. The Trigger Probe and Termination Box. Clip Lead Facilitates Mounting Probe, Is Electrically Neutral

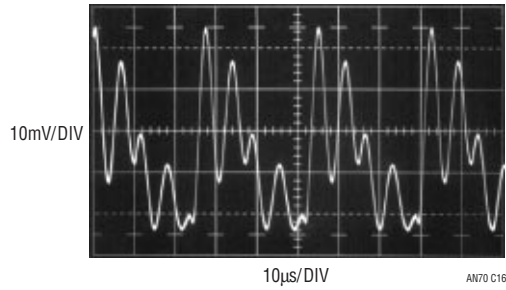


Figure C16. Misadjusted Termination Causes Inadequate Damping. Unstable Oscilloscope Triggering May Result

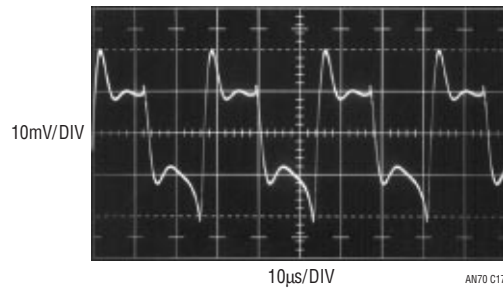


Figure C17. Properly Adjusted Termination Minimizes Ringing with Small Amplitude Penalty

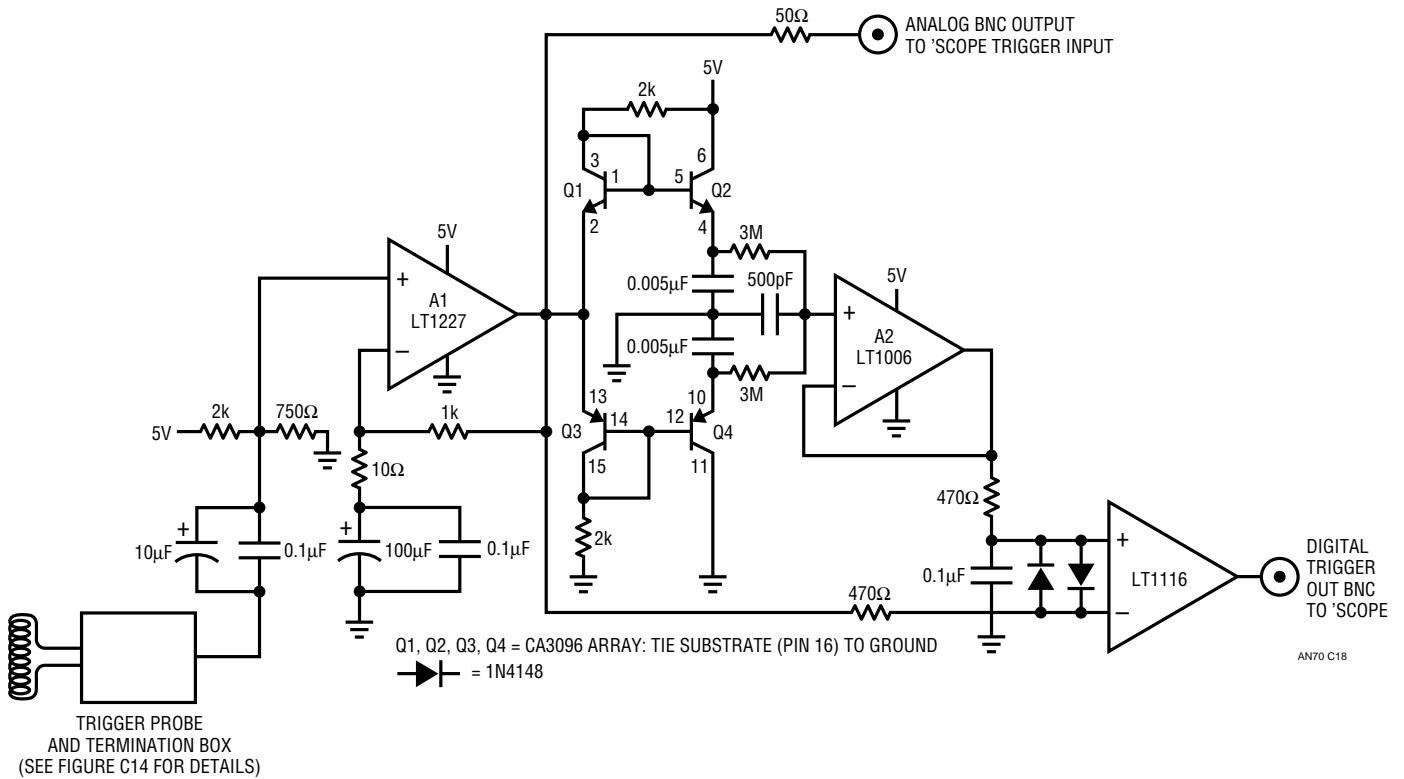


Figure C18. Trigger Probe Amplifier Has Analog and Digital Outputs. Adaptive Threshold Maintains Digital Output over 50:1 Probe Signal Variations

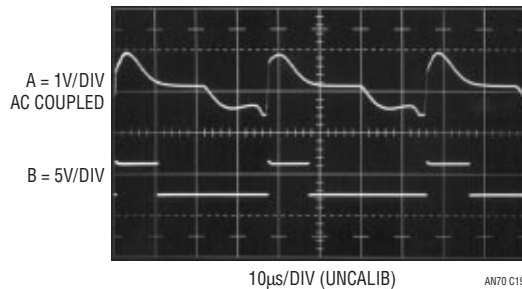


Figure C19. Trigger Probe Amplifier Analog (Trace A) and Digital (Trace B) Outputs

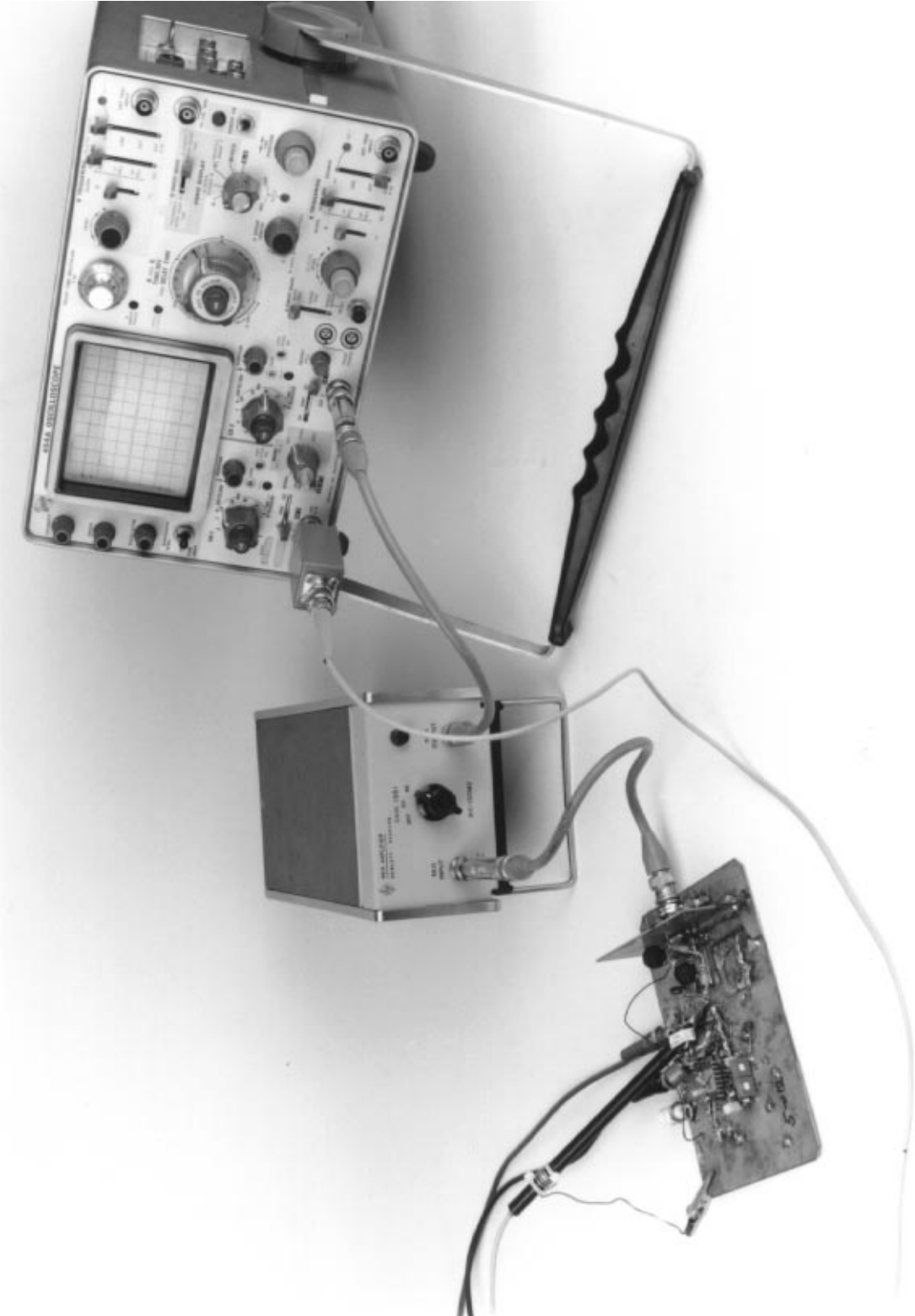


Figure C20. Typical Noise Test Setup Includes Trigger Probe, Amplifier, Oscilloscope and Coaxial Components

APPENDIX D

BREADBOARDING AND LAYOUT CONSIDERATIONS

LT1533-based circuit's low harmonic content allows their noise performance to be less layout sensitive than other switching regulators. However, some degree of prudence is in order. As in all things, cavaliness is a direct route to disappointment. Obtaining the absolute lowest noise figure requires care, but performance below 500 μ V is readily achieved. In general, lowest noise is obtained by preventing mixing of ground currents in the return path. Indiscriminate disposition of ground currents into a bus or ground plane will cause such mixing, raising observed output noise. The LT1533's restricted edge rates mitigate against corrupted ground path-induced problems, but best noise performance occurs in a "single-point" ground scheme. Single-point return schemes may be impractical in production PC boards. In such cases, provide the lowest possible impedance path to the power entry point from the inductor associated with the LT1533's power ground pin. (Pin 16). Locate the output component ground returns as close to the circuit load point as possible. Minimize return current mixing between input and output sections by restricting such mixing to the smallest possible common conductive area.

5V to 12V Breadboard

Figure D1 shows text Figure 5's breadboard. In keeping with a breadboard's purpose, it is constructed to be fast and easy to modify. Single-point returns arrive separately

from the output area (right side of photo) and Pin 16 of the LT1533 (center left photo). The ground plane carries no current. The dummy load resistors are *not* terminated to the plane, but returned to the transformer's center tap. The center tap and plane are separately tied into the ground system at the power input common jack.

5V to \pm 15V Breadboard

Text Figure 24's breadboard appears in Figure D2. Layout considerations are similar to Figure D1, although the design's floating output mandates changes. The output load (photo's right, above BNC connector) returns directly to the transformer secondary, which floats from input (and plane) ground potential. The main ground plane is tied to input common at the power entry port (left banana jack). The floating output potentials are referred to a separate, smaller planed area (photo lower right) which is tied to the transformer secondary center tap.

Demonstration Board

Figure D3 enticingly portrays an LT1533 demonstration board. The board's practical layout is readily adaptable to production versions. This board is useful for observing LT1533 performance and as an example of a practical layout. Noise performance is similar to the text's breadboards.

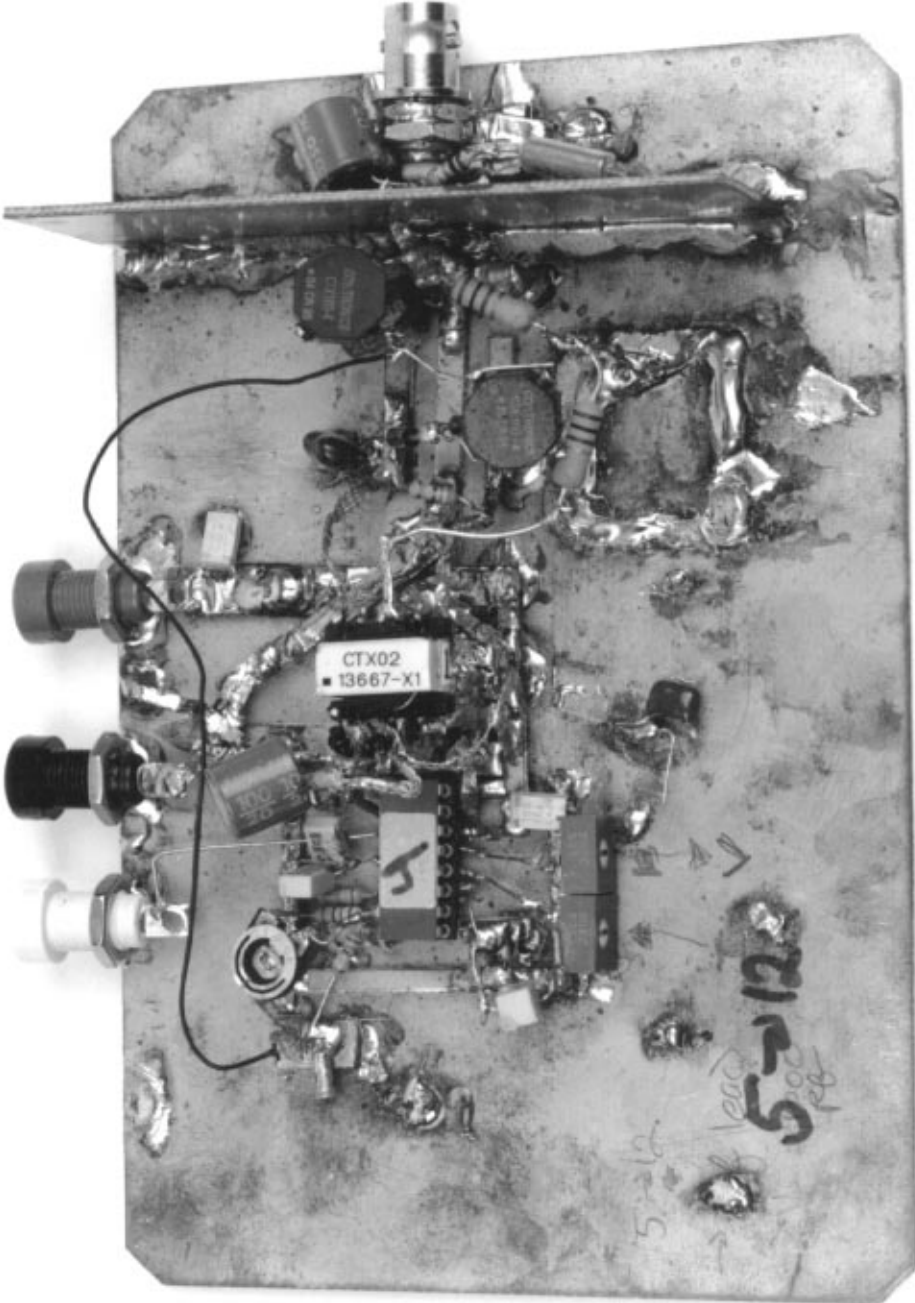


Figure D1. Text Figure 5's 5V-to-12V Converter Breadboard. Construction Is Easy to Change, Facilitating Experiments. Note Single-Point Ground Returns. Ground Plane Carries No Current, Is Tied to Input Common at Board Entry Point (Middle Banana Jack)

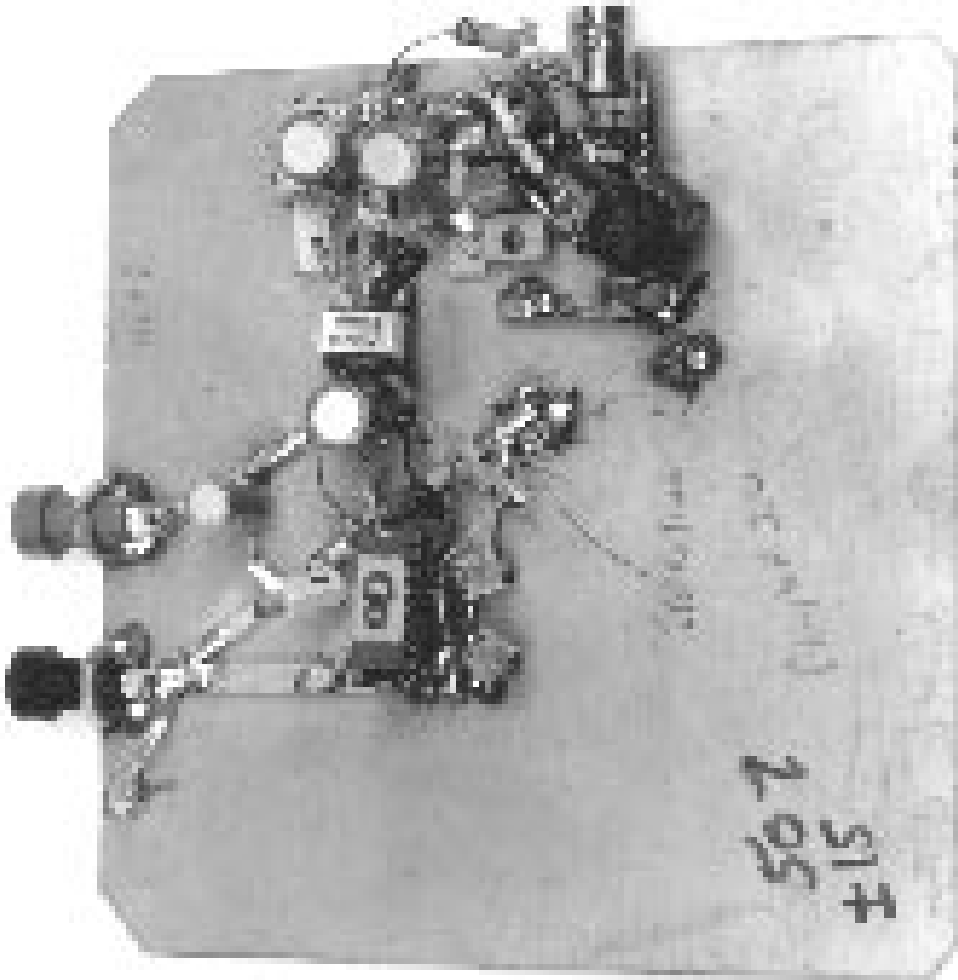


Figure D2. Text Figure 26's Breadboard with Linear Output Regulators. Construction Encourages Changes and Measurement. Layout Is Similar to Figure D1, Although Floating Output Necessitates Changes. Separate Planed Area (Photo Center Right) Maintains Low Impedance Between Output-Related Returns

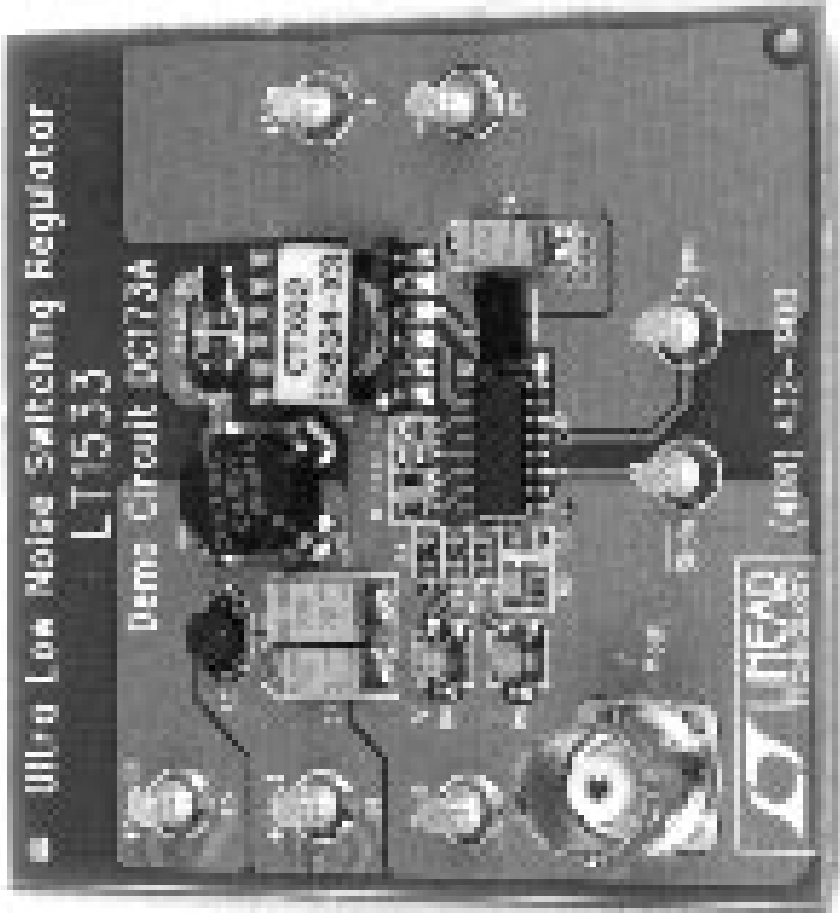


Figure D3. The Very Civilized LT1533 Demonstration Board in All Its Comely Splendor

APPENDIX E

SELECTION CRITERIA FOR LINEAR REGULATORS

Some applications, particularly floating output circuits, may require linear postregulators. Selection criteria include regulator output accuracy, dropout, ripple rejection and line regulation. Often, short-circuit protection is not needed because drive circuit output impedance and current limiting prevent destructive overload. In such cases, if relatively poor output load regulation and accuracy are acceptable, simple Zener diode-emitter follower-based regulation may suffice. LM78L/79L type devices offer 5% output accuracy and improved line regulation, although dropout is about 2V—significantly higher than a simple Zener-emitter follower regulator. Ripple rejection in LM78L/79L types degrades as they approach dropout, which is the desirable operating region for best efficiency. High performance regulators such as the LT1575 (negative) and LT1521 (positive) offer dropout voltages below 0.5V, tight line regulation, 1% accuracy and fully specified ripple rejection close to dropout.

It is usually desirable to operate close to dropout to maintain good overall efficiency. Because of this, regulator ripple rejection should be tested in this intended operating region. Additionally, cost, size and performance trade-offs of various filter components and regulators should be evaluated to determine the best solution for a particular application.

Testing Ripple Rejection

Ripple rejection may be tested with Figure E1's arrangement. The generator should operate over the frequency range of interest and be capable of supplying the required output drive. In practice, the generator is set to supply the regulator input operating voltage at the expected LT1533 switching frequency. Comparison of different regulators and filter components under varying operating conditions is easily carried out.

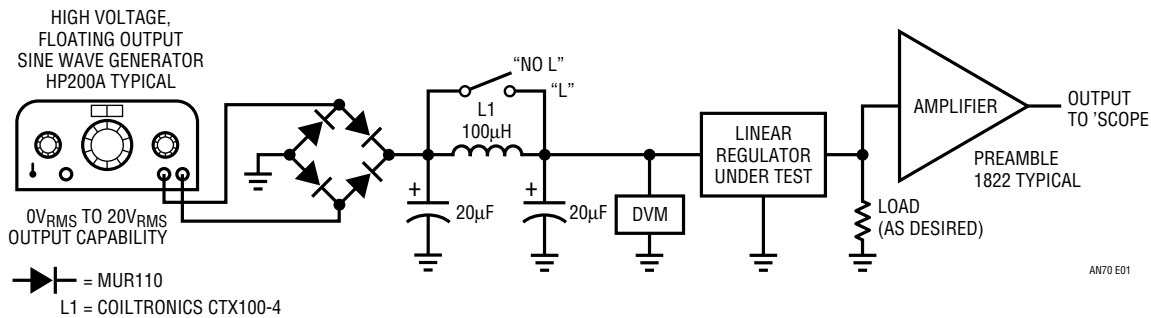


Figure E1. Ripple Rejection Test Setup for Linear Regulators. LC Combinations and Regulators May Be Evaluated



Figure E2. Ripple Rejection Test Setup Includes Sine Wave Generator, Breadboard, Amplifier and Oscilloscope

APPENDIX F

MAGNETICS CONSIDERATIONS

Transformers

The LT1533's symmetrical "push-pull" drive makes transformer behavior quite predictable. As such, transformers may usually be specified by indicating the operating frequency, power and desired input/output voltages. Figure F1 lists the transformers used in the text circuits along with some of their characteristics. These components, and variations on them, are available from Coiltronics, telephone #561-241-7876.

Inductors

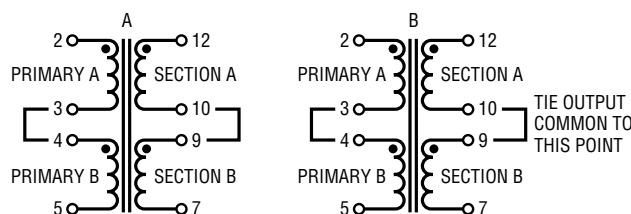
Inductors in LT1533 circuits do not have special characteristics. Text Figure 5's circuit, a "forward" type converter,¹ requires an inductor ahead of its filter capacitor, although additional LC filtering is optional. Figure 26's "50%" mode circuit has no output inductor requirement

unless heavily loaded (see text), although LC sections may be used for best possible ripple attenuation. In either case, inductor characteristics are not particularly critical. All circuits shown in the text use Coiltronics "Octa-Pak" type toroidal core-based inductors.

The 22nH inductor used in the LT1533's power ground return (Pin 16) is mandatory. It may take several forms, including trace inductance, a small coil of wire, a ferrite bead or the packaged inductor specified in the schematics. If coiled wire is employed, five turns of #28 is sufficient. An equivalent length of PC trace gives similar results. A ferrite bead (e.g., Ferronics #21-110J or equivalent) with one or two turns of wire also works well. An example of a packaged 22nH inductor is the Coilcraft B-07T which is specified in the test circuits.

Note 1: See References 16 and 17 for basic forward converter theory.

NOMINAL INPUT VOLTAGE	NOMINAL OUTPUT VOLTAGE AFTER LINEAR REGULATOR	OUTPUT POWER	COILTRONICS PART NUMBER	CONNECTION DIAGRAM
5V	12V	1.5W	CTX-02-13716-X1	A
5V	12V	3.0W	CTX-02-13665-X1	A
5V	±15V	1.5W	CTX-02-13713-X1	B
5V	±15V	3.0W	CTX-02-13664-X1	B
5V	12V	1.5W	CTX-02-13834-X3*	A
5V	12V	10W	CTX-02-13949-X1	A



☐ = TIED TOGETHER

* = HIGH TURNS RATIO VERSION OF CTX-02-13716-X1. ACCOMMODATES LOW SUPPLY VOLTAGES OR HIGH DROPOUT REGULATORS

AN70 FF01

Figure F1. Transformer Types Used in Text Circuits. Variations for Specific Requirements Are Available from Coiltronics, 561-241-7876

Application Note 70

APPENDIX G

WHY VOLTAGE AND CURRENT SLEW CONTROL?

Carl T. Nelson

The LT1533 gives dramatic reduction of high frequency noise by controlling both voltage and current slew rates in the switch. This technique also has the advantage of controlling noise in the other switching regulator components, namely, the catch diode and input and output capacitors.

Figure G1's block diagram shows the basic concepts for slew control. The switch Q1 is driven on and off with currents I_1 and I_2 switched via S1. These currents are large enough to drive the switch at very high slew rates. Actual slew rates are set by I_3 for voltage slew and I_4 for current slew.

During switch turn-on, the collector of Q1 is initially high and current is zero. Inductor current holds the switch high until switch current equals inductor current. The first limiting action occurs as current builds in Q1. Current is sensed by a fixed gain amplifier A3. The increasing current generates a current through C2 proportional to switch current slew rate. This current is compared to I_4 , and the

difference is amplified by A2, which shunts away all excess I_1 current to control switch current slew rate.

When switch current exceeds inductor current, Q1's collector would normally fall low at a speed limited only by diode and switch parasitic capacitance. To control voltage slew, the current through C1 is compared to I_3 , and the difference is amplified by A1 to clamp the base current of Q1. This stops any further rise in switch current and forces switch voltage to fall at a controlled rate.

At switch turn-off, current and voltage must be controlled in the reverse order. Switch S1 is flipped to provide reverse base drive, and the polarity of I_3 and I_4 is reversed. Almost immediately, switch current falls slightly below inductor current. This would normally cause the switch voltage to slew up, limited only by diode and switch capacitance. Here, C1 senses voltage slew and A1 controls switch base drive to limit switch rise time. Switch current remains essentially constant during voltage slew.

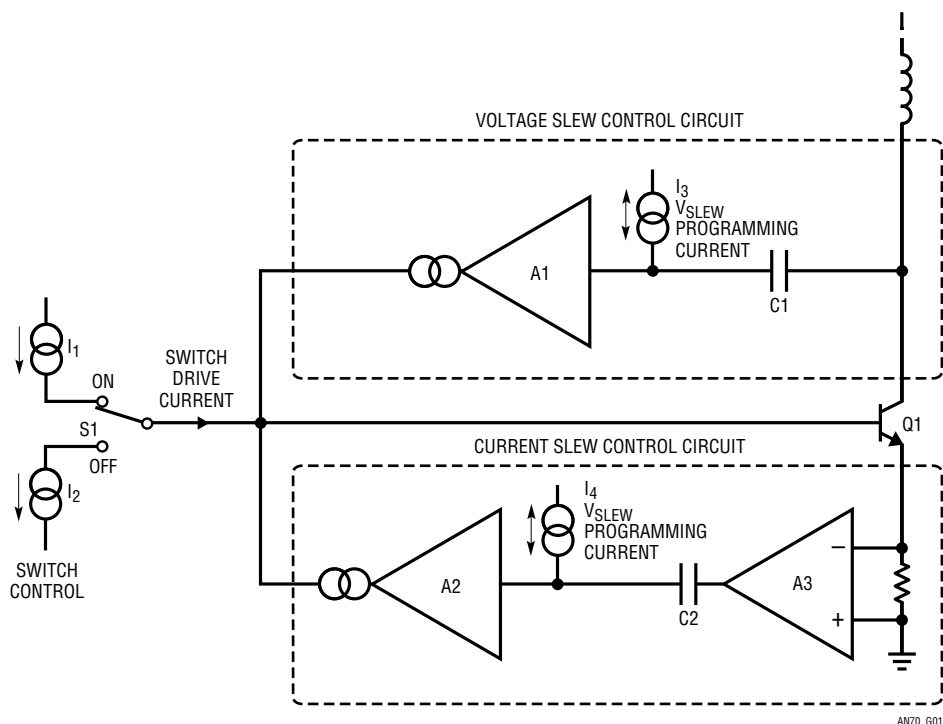


Figure G1. Slew Control Conceptual Block Diagram

When switch voltage reaches the level where the catch diode turns on, switch current would normally drop rapidly, creating fast B field transients around the switch, diode and output capacitor lines. A3 and C2 come into play here, sensing the decreasing switch current and controlling the base drive via A2 to force a controlled decrease in switch, diode and capacitor current.

Figure G2 shows switch, diode and output capacitor waveforms with controlled switch drive in operation. Note that current and voltage slew limiting do not occur simultaneously. One must take over when the first is complete. This requires very fast control circuitry to avoid crossover glitches that would create noise spikes.

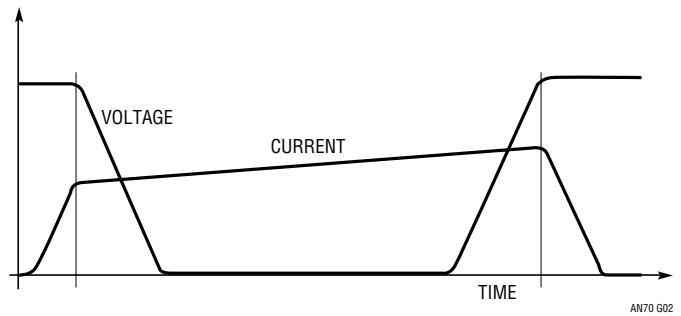


Figure G2. Switch Voltage and Current During Turn-On and Turn-Off

APPENDIX H

HINTS FOR LOWEST NOISE PERFORMANCE

The LT1533's controlled switching times allow extraordinarily low noise DC/DC conversion with surprisingly little design effort. Wideband output noise well below 500 μ V is easily achieved. In most situations this level of performance is entirely adequate. Applications requiring the lowest possible output noise will benefit from special attention to several areas.

Noise Tweaking

The slew time versus efficiency trace-off discussed in the text should be weighted towards lowest noise to the extent tolerable. Typically, slew times beyond 1.3 μ s result in "expensive" noise reduction in terms of lost efficiency, but the benefit is available. The issue is how much power is expendable to obtain incremental decreases in output noise. Similarly, the layout techniques discussed in Appendix D should be reviewed. Rigid adherence to these guidelines will result in correspondingly lower noise performance. The text's breadboards were originally constructed to provide the lowest possible noise levels, and then systematically degraded to test layout sensitivity. This approach allows experimentation to determine the best layout without expending fanatical attention to details that provide essentially no benefit.

The slow edge times greatly minimize radiated EMI, but experimentation with the component's physical orienta-

tion can sometimes improve things. Look at the components (yes, literally!) and try and imagine just what their residual radiated field impinges on. In particular, the optional output inductor may pick up field radiated by other magnetics, resulting in increased output noise. Appropriate physical layout will eliminate this effect, and experimentation is useful. The EMI probe described in Appendix J is a useful tool in this pursuit and highly recommended. Appendix I contributes hints on magnetics-based noise and is similarly recommended.

Capacitors

The filter capacitors used should have low parasitic impedance. Sanyo OS-CON types are excellent in this regard and contributed to the performance levels quoted in the text. Tantalum types are nearly as good. The input supply bypass capacitor, which should be located directly at the transformer center tap, needs similarly good characteristics. Aluminum electrolytics are not suitable for any service in LT1533 circuits.

Damper Network

Some circuits may benefit from a small (e.g., 330 Ω -1000pF) damper network across the transformer secondary if the absolutely lowest noise is needed. Extremely small (20 μ V to 30 μ V) excursions can briefly appear during

Application Note 70

the switching interval when no energy is coming through the transformer. These events are so minuscule that they are barely measurable in the noise floor, but the damper will eliminate them.

Measurement Technique

Strictly speaking, measurement technique is not a way to obtain lowest noise performance. Realistically, it is essen-

tial that measurement technique be trustworthy. Uncountable hours have been lost chasing “circuit problems” that in reality are manifestations of poor measurement technique. Please read Appendices B and C before pursuing solutions to circuit noise that isn’t really there.¹

Note 1: I do not wax pedantic here. My guilt in this offense runs deep.

APPENDIX I

PROTECTION AGAINST MAGNETICS NOISE IS KNOWLEDGE AND GOOD COMMON SENSE

Jon Roman—Coiltronics, Inc.

Noise Test Data

For this test I chose four of the most common magnetics geometries that are currently in production use today. They are as follows: Pot Core, ER Core, E Core and the Toroid. The following test data was taken using the methods as described in the following paragraphs. The test circuit used to determine the amount of noise radiation is as shown in Figure I1 . The push-pull configuration, power ratings and turns ratios were chosen to align with the Jim Williams’ low noise designs presently under study. The distance chosen for the Sniffer Noise Probe¹ was set at 0.250 inches from the surface of the core structure. This distance was chosen as a result of preliminary testing to allow for a measurable reading on the smallest amount of flux lines coming from the quietest core structure. The measured worst-case full load noise is shown in Figure I2, for each of the four geometries chosen for this test. Note

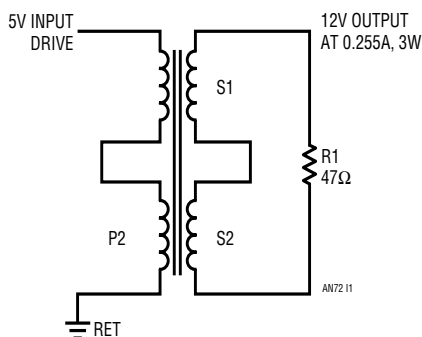


Figure I1. Test Circuit

that the noise is shown in millivolts rather than gauss, the conversion for gauss is:

$$V_{\text{PROBE}}(\text{mV}_{\text{P-P}}) = 2.88\text{mGauss}/\mu\text{s}^2$$

After taking the noise reading for each of the UUT’s under their full load conditions, the load resistor was removed to allow for observation of magnetizing flux noise. Then, using the same measurement techniques, the noise was measured a second time to determine the difference between the load noise and the magnetizing noise. The measured worst-case magnetizing noise is shown in Figure I3.

Note 1: See Appendix J.

Note 2: See Appendix J.

GEOMETRY	FULL LOAD MAGNETIZING
Pot Core	20mV
ER Core	63mV
E Core	488mV
Toroid	860mV

Figure I2. Worst-Case Full Load Noise

GEOMETRY	FULL LOAD MAGNETIZING
Pot Core	16mV
ER Core	49mV
E Core	95mV
Toroid	91mV

Figure I3. Worst-Case Magnetizing Load Noise

Pot Core

The Pot core tested was as predicted the quietest geometry of the ones tested. Just as expected the “Hot Spot” for noise was located at the window of the gap where the leads exit the core. Reference the waveform shown in Figure I4. Note the top waveform shows the voltage input, the middle waveform shows the noise as recorded using an amplifier and the bottom waveform is the current through the UUT.

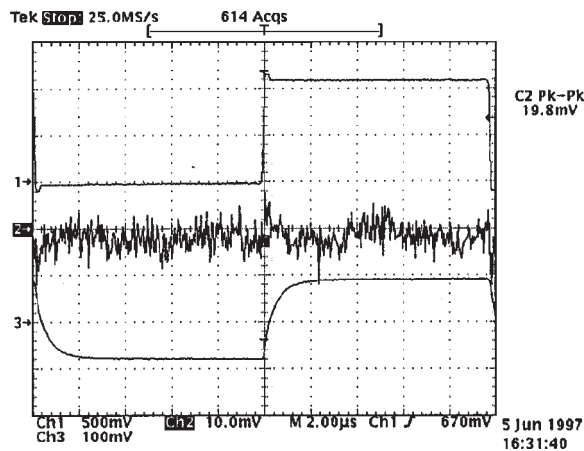
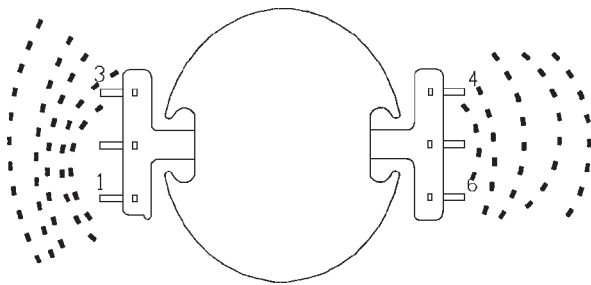


Figure I4

ER Core

The ER core tested was the surprise of the group with a much lower noise reading than one would have originally thought possible. Reference the waveform shown in Figure I5. Note the top waveform shows the voltage input, the middle waveform shows the noise as recorded using an amplifier and the bottom waveform is the current through the UUT.

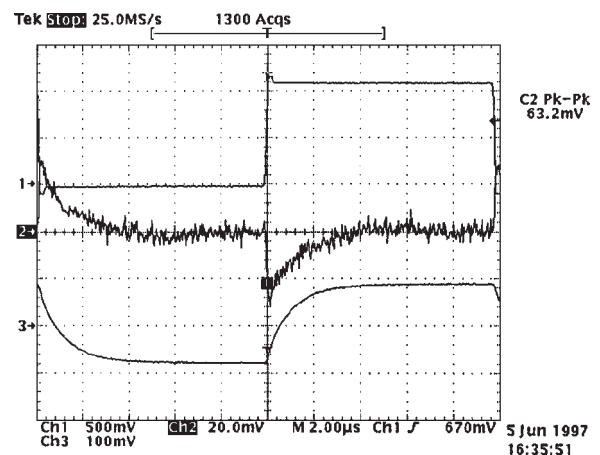
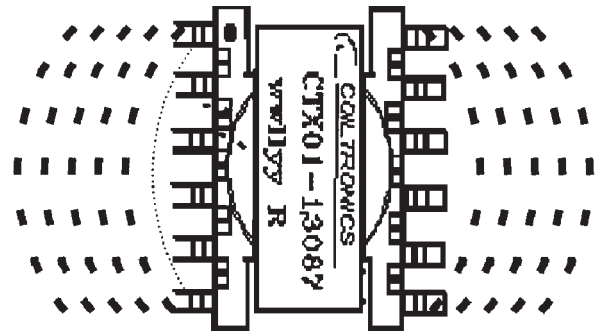


Figure I5

Application Note 70

Toroid

The Toroid core (Figure I6) tested showed a much higher electronic noise than was originally expected from a closed-path geometry. The worst-case noise came from the top of the core, with the winding placed as evenly on the core as possible. Note the top waveform shows the voltage input, the middle waveform shows the noise as recorded using an amplifier and the bottom waveform is the current through the UUT.

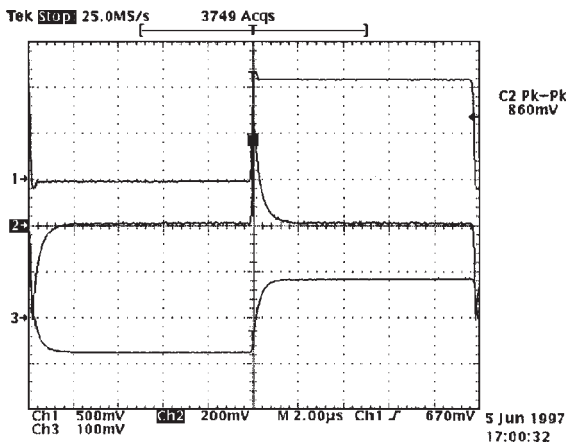
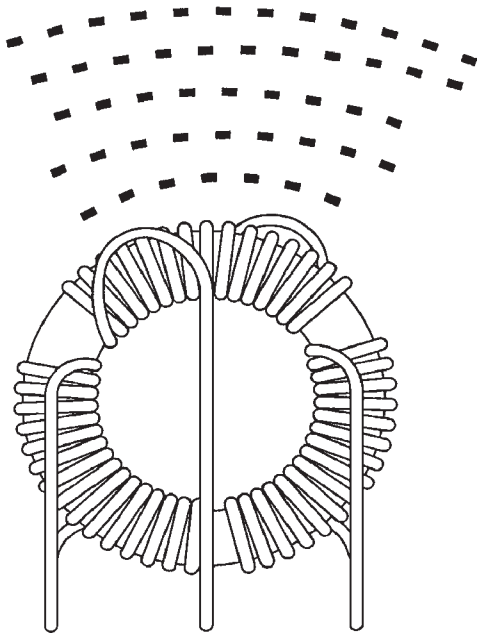


Figure I6

E Core

The E-core (Figure I7) showed the highest concentration of noise just above the winding on the top center of the device. The noise on the surrounding sides was measurable but far below the field that was found directly above and below the part. Note the top waveform shows the voltage input, middle waveform shows the noise as recorded using an amplifier and the bottom waveform is the current through the UUT.

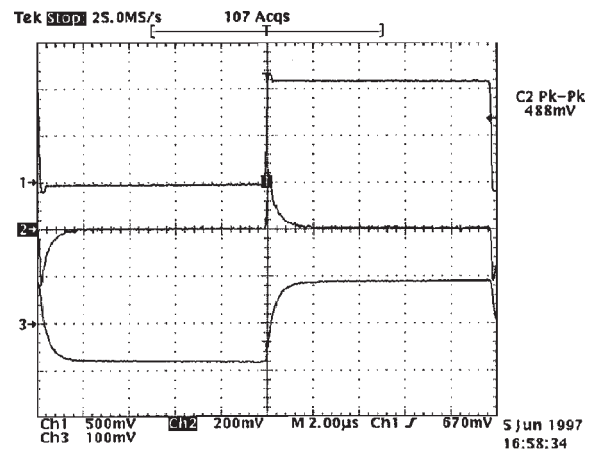
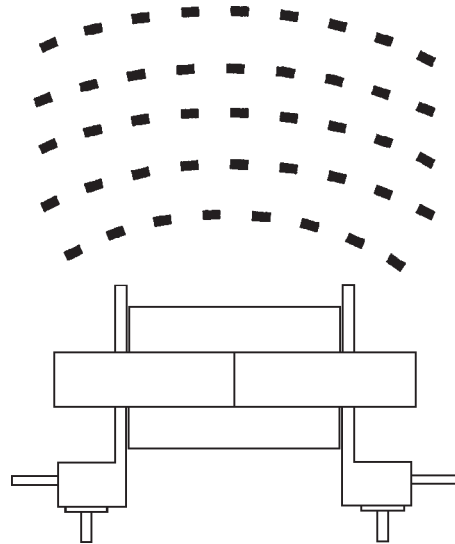


Figure I7

Summary

Figure 18 is a graph showing the relative difference comparing the full load noise against the magnetizing load noise. It is recognized that closed core structures such as toroids in inductors produce less stray (leakage) flux than open structures like rod cores or bobbin cores. Some recent products offer “magnetic shields” or tubes of magnetic material around a bobbin-type core in an attempt to provide a “magnetic shunt” for the flux to follow. These structures offer very little reduction in noise because of the high reluctance in the air gap between the “shield” and the inner bobbin core. The reluctance in this gap is much higher than that of the magnetic material. The resultant leakage flux from the gap can defeat the purpose of the shield almost entirely! The best approach for reducing noise in inductors is to use true closed-field geometries, such as the toroid.

When designing for the lowest possible noise in transformer applications, it is important to observe the effects

of the load current, as opposed to the magnetizing current. The preceding test demonstrates that the traditional low noise structures (toroid) can radiate relatively high amounts of leakage flux due to the coupling characteristics between windings. The reflected load currents in both the primary and the secondary do not affect the magnetizing flux, but create a magnetic leakage field around the wire, if the coupling is less than perfect. This is, by definition, leakage flux. The size and shape of the window area can have an effect on coupling between windings, as well as the shape of the flux field emanating from the transformer.

Winding technique also has an effect on coupling and noise. Multifilar winding, as opposed to layer winding, can offer better coupling characteristics, which in turn, lowers noise by lessening leakage flux.

Conclusion

Every *millivolt* counts.

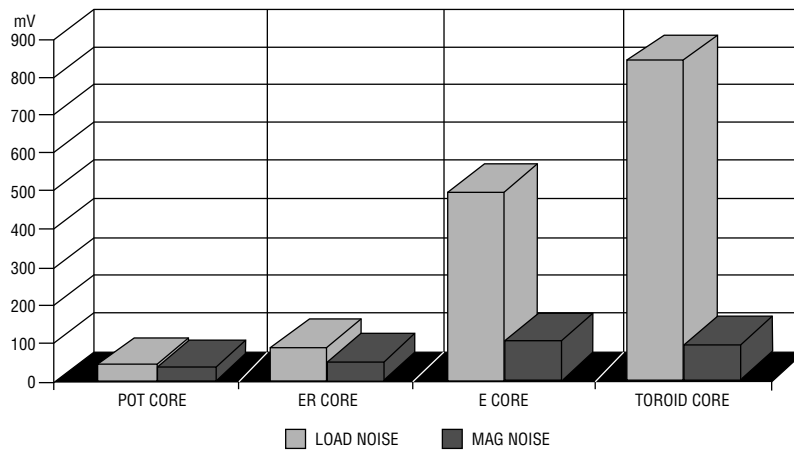


Figure 18

APPENDIX J

MEASURING EMI RADIATION

EMI (Electromagnetic Interference) is a form of switching regulator noise. It is a radiated, as opposed to conducted, phenomenon. LT1533-based circuits produce low amounts of EMI for the same reason they minimize conducted noise—controlled switching times. This appendix, guest written by Bruce Carsten, describes an excellent tool for

relative EMI measurement and how to use it.¹ Carsten’s methods not only show how to measure relative EMI, but how to identify and silence its source.

Note 1: Calibrated measurements are discussed in References 14 and 15.

Application Note 70

APPLICATION NOTE E101: EMI "SNIFFER" PROBE
Bruce Carsten Associates, Inc.
6410 NW Sisters Place, Corvallis, Oregon 97330
541-745-3935

The EMI Sniffer Probe² is used with an oscilloscope to locate and identify magnetic field sources of electromagnetic interference (EMI) in electronic equipment. The probe consists of a miniature 10 turn pickup coil located in the end of a small shielded tube, with a BNC connector provided for connection to a coaxial cable (Figure J1). The Sniffer Probe output voltage is essentially proportional to the rate of change of the ambient magnetic field, and thus to the rate of change of nearby currents.

The principal advantages of the Sniffer Probe over simple pickup loops are:

1. Spatial resolution of about a millimeter.
2. Relatively high sensitivity for a small coil.
3. A 50Ω source termination to minimize cable reflections with unterminated scope inputs.
4. Faraday shielding to minimize sensitivity to electric fields.

The EMI Sniffer Probe was developed to diagnose sources of EMI in switch mode power converters, but it can also be used in high speed logic systems and other electronic equipment.

SOURCES OF EMI

Rapidly changing voltages and currents in electrical and electronic equipment can easily result in radiated and conducted noise. Most EMI in switch mode power converters is thus generated during switching transients when power transistors are turned on or off.

Conventional scope probes can readily be used to see dynamic voltages, which are the principal sources of common mode conducted EMI. (High dV/dt can also feed through poorly designed filters as normal mode voltage spikes and may radiate fields from a circuit without a conductive enclosure.)

Dynamic currents produce rapidly changing magnetic fields which radiate far more easily than electric fields as

they are more difficult to shield. These changing magnetic fields can also induce low impedance voltage transients in other circuits, resulting in unexpected normal and common mode conducted EMI.

These high dI/dt currents and resultant fields can not be directly sensed by voltage probes, but are readily detected and located with the Sniffer Probe. While current probes can sense currents in discrete conductors and wires, they are of little use with printed circuit traces or in detecting dynamic magnetic fields.

PROBE RESPONSE CHARACTERISTICS

The Sniffer Probe is sensitive to magnetic fields only along the probe axis. This directionality is useful in locating the paths and sources of high dI/dt currents. The resolution is usually sufficient to locate which trace on a printed circuit board, or which lead on a component package, is conducting the EMI generating current.

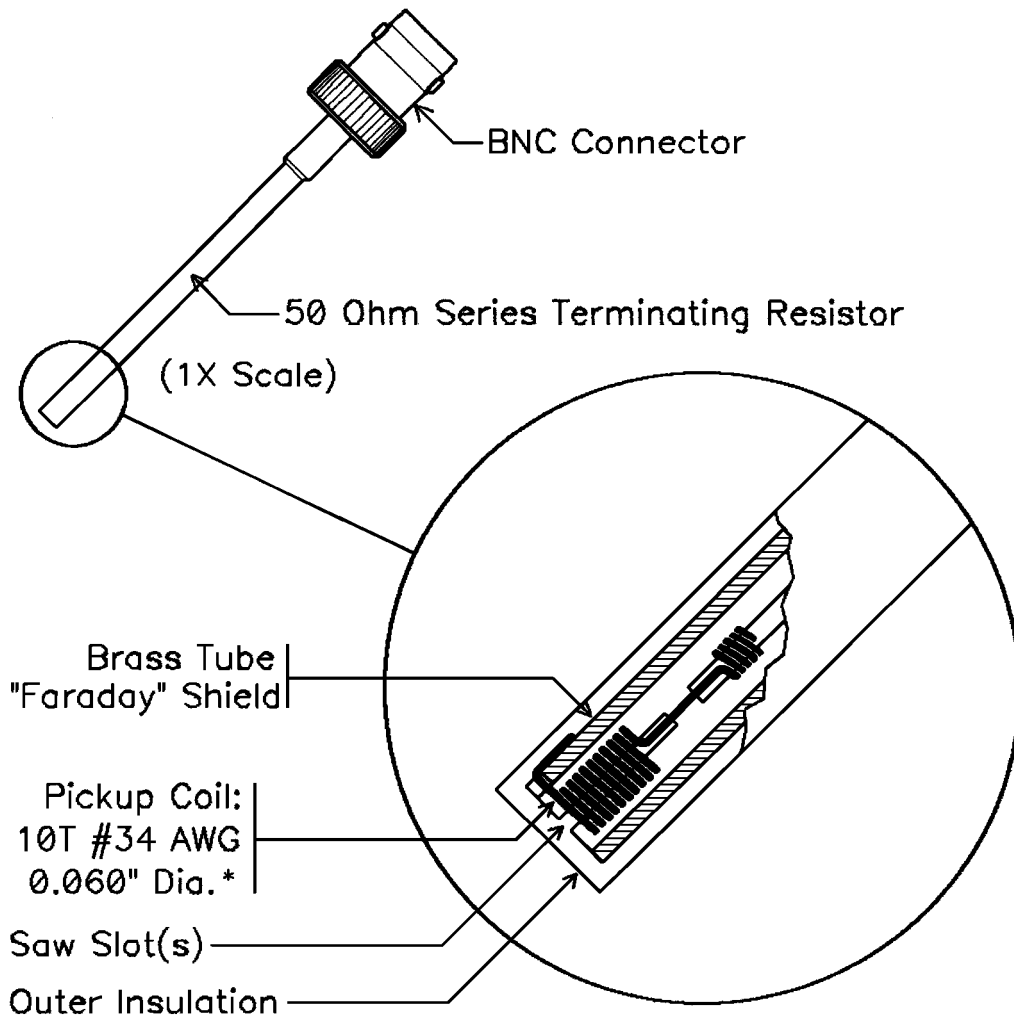
For "isolated" single conductors or PC traces, the Probe response is greatest just to either side of the conductor where the magnetic flux is along with probe axis. (Probe response may be a little greater with the axis tilted towards the center of the conductor.) As shown in Figure J2, there is a sharp response null in the middle of the conductor, with a 180° phase shift to either side and a decreasing response with distance. The response will increase on the inside of a bend where the flux lines are crowded together, and is reduced on the outside of a bend where the flux lines spread apart.

When the return current is in an adjacent parallel conductor, the Probe response is greatest between the two conductors as shown in Figure J3. There will be a sharp null and phase shift over each conductor, with a lower peak response outside the conductor pair, again decreasing with distance.

Note 2: The EMI Sniffer Probe is available from Bruce Carsten Associates at the address noted in the title of this appendix.

The response to a trace with a return current on the opposite side of the board is similar to that of a single isolated trace, except that the probe response may be greater with the Probe axis tilted away from the trace. A

“ground plane” below a trace will have a similar effect, as there will be a counter-flowing “image” current in the ground plane.



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* Approx. 160 μ Wire, 1.5mm Coil Dia.

Figure J1. Construction of the EMI "Sniffer Probe" for Locating and Identifying Magnetic Field Sources of EMI

Application Note 70

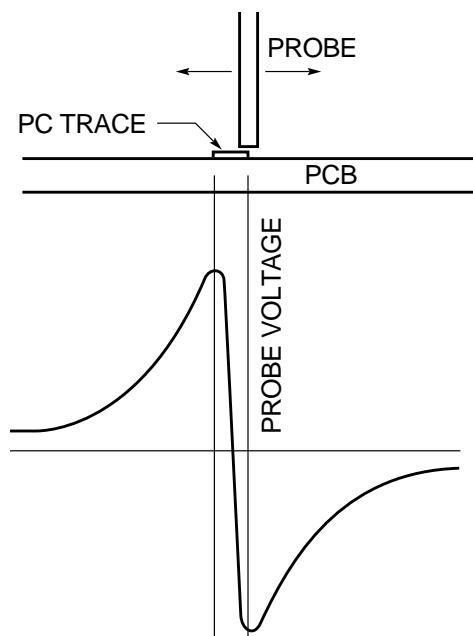


Figure J2. Sniffer Probe Response to Current in a Physically "Isolated" Conductor

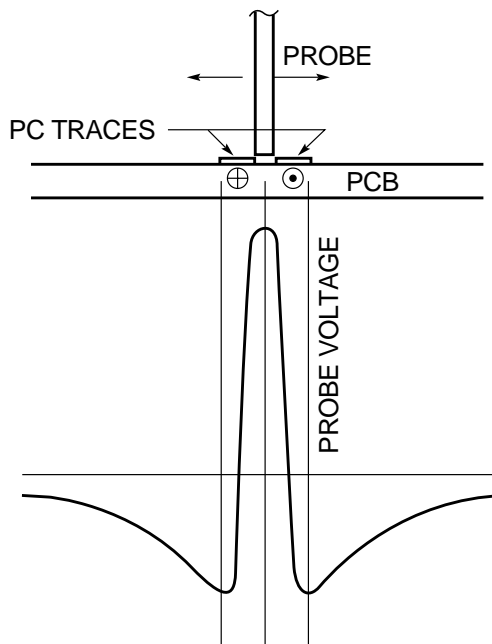


Figure J3. Sniffer Probe Response with Return Current in a Parallel Conductor

The Probe frequency response to a uniform magnetic field is shown in Figure J4. Due to large variations in field strength around a conductor, the Probe should be considered as a qualitative indicator only, with no attempt made to "calibrate" it. The response fall-off near 300MHz is due to the pickup coil inductance driving the coax cable impedance, and the mild resonant peaks (with a 1M Ω scope termination) at multiples of 80MHz are due to transmission line reflections.

PRINCIPLES OF PROBE USE

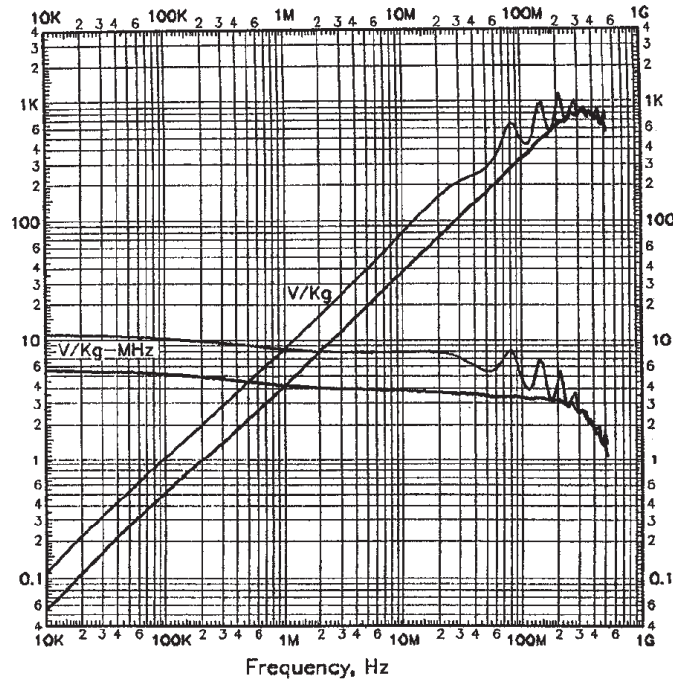
The Sniffer Probe is used with at least a 2-channel scope. One channel is used to view the noise whose source is to be located (which may also provide the scope trigger) and the other channel is used for the Sniffer Probe. The probe response nulls make it inadvisable to use this scope channel for triggering.

A third scope trigger channel can be very useful, particularly if it is difficult to trigger on the noise. Transistor drive waveforms (or their predecessors in the upstream logic) are ideal for triggering; they are usually stable, and allow immediate precursors of the noise to be viewed.

Start with the Probe at some distance from the circuit with the Probe channel at maximum sensitivity. Move the probe around the circuit, looking for "something happening" in the circuit's magnetic fields at the same time as the noise problem. A precise "time domain" correlation between EMI noise transients and internal circuit fields is fundamental to the diagnostic approach.

As a candidate noise source is located, the Probe is moved closer while the scope sensitivity is decreased to keep the probe waveform on-screen. It should be possible to quickly bring the probe down to the PC board trace (or wiring) where the probe signal seems to be a maximum. This may not be near the point of EMI generation, but it should be near a PC trace or other conductor carrying the current from the EMI source. This can be verified by moving the probe back and forth in several directions; when the appropriate PC trace is crossed at roughly right angles, the probe output will go through a sharp null over the trace, with an evident phase reversal in probe voltage on each side of the trace (as noted above).

This EMI "hot" trace can be followed (like a bloodhound on the scent trail) to find all or much of the EMI generating current loop. If the trace is hidden on the back side (or



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Figure J4. Typical EMI "Sniffer" Probe Frequency Response Measured with 1.3m (51") of 50Ω Coax to Scope
 Upper Traces: 1Meg Scope Input Impedance
 Lower Traces: 50Ω Scope Input Impedance

inside) of the board, mark its path with a felt pen and locate the trace on disassembly, on another board or on the artwork. From the current path and the timing of the noise transient, the source of the problem usually becomes almost self-evident.

Several not-uncommon problems (all of which have been diagnosed with various versions of the Sniffer Probe) are discussed here with suggested solutions or fixes.

TYPICAL DI/DT EMI PROBLEMS

Rectifier Reverse Recovery

Reverse recovery of rectifiers is the most common source of di/dt-related EMI in power converters; the charge stored in P-N junction diodes during conduction causes a momentary reverse current flow when the voltage reverses. This reverse current may stop very quickly (<1ns) in diodes with a "snap" recovery (more likely in devices with a PIV rating of less than 200V), or the reverse current may

decay more gradually with a "soft" recovery. Typical Sniffer Probe waveforms for each type of recovery are shown in Figure J5.

The sudden change in current creates a rapidly changing magnetic field, which will both radiate external fields and induce low impedance voltage spikes in other circuits. This reverse recovery may "shock" parasitic L-C circuits into ringing, which will result in oscillatory waveforms with varying degrees of damping when the diode recovers. A series R-C damper circuit in parallel with the diode is the usual solution.

Output rectifiers generally carry the highest currents and are thus the most prone to this problem, but this is often recognized and they may be well-snubbed. It is not uncommon for unsnubbed catch or clamp diodes to be *more* of an EMI problem. (The fact that a diode in an R-C-D snubber may need its *own* R-C snubber is not always self-evident, for example).

Application Note 70

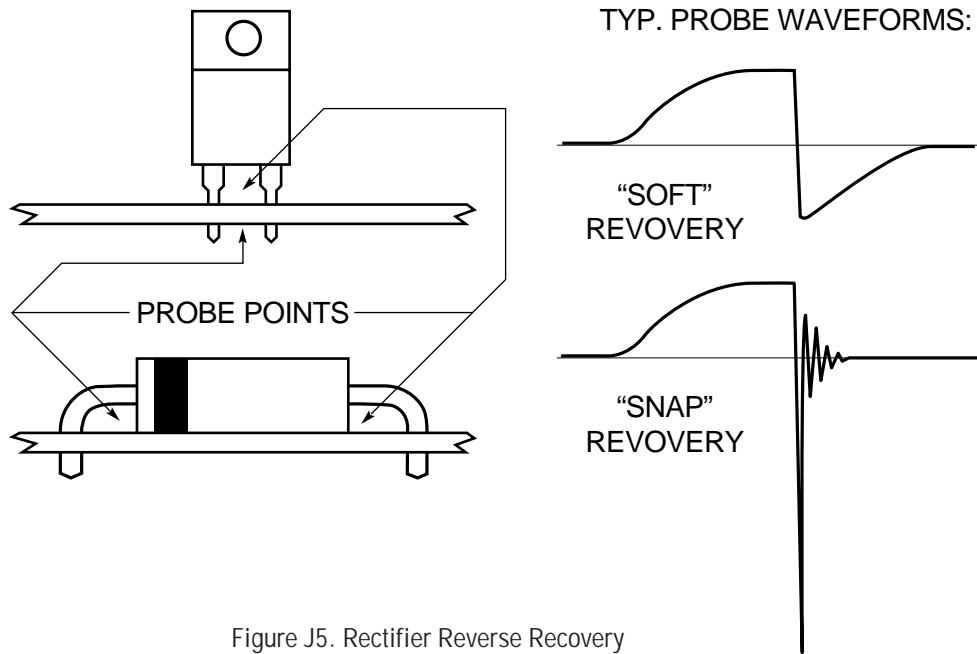


Figure J5. Rectifier Reverse Recovery
Typical Fix: Tightly Coupled R-C Snubber

The problem can usually be identified by placing the Sniffer Probe near a rectifier lead. The signal will be strongest on the inside of a lead bend in an axial package, or between the anode and cathode leads in a TO-220, TO-247 or similar type of package, as shown in Figure J5.

Using “softer” recovery diodes is a possible solution and Schottky diodes are ideal in low voltage applications. However, it must be recognized that a P-N diode with soft recovery is also inherently lossy (while a “snap” recovery is not), as the diode simultaneously develops a reverse voltage while still conducting current: The fastest possible diode (lowest recovered charge) with a moderately soft recovery is usually the best choice. Sometimes a faster, slightly “snappy” diode with a tightly coupled R-C snubber works as well or better than a soft but excessively slow recovery diode.

If significant ringing occurs, a “quick-and-dirty” R-C snubber design approach works fairly well: increasingly large damper capacitors are placed across the diode until the ringing frequency is halved. We know that the total ringing capacity is now quadrupled or that the original ringing capacity is 1/3 of the added capacity. The damper resistance required is about equal to the capacitive reactance of

the original ringing capacity at the original ringing frequency. The “frequency halving” capacity is then connected in series with the damping resistance and placed across the diode, as tightly coupled as possible.

Snubber capacitors must have a high pulse current capability and low dielectric loss. Temperature stable (disc or multilayer) ceramic, silvered mica and some plastic film-foil capacitors are suitable. Snubber resistors should be noninductive; metal film, carbon film and carbon composition resistors are good, but wirewound resistors must be avoided. The maximum snubber resistor dissipation can be estimated from the product of the damper capacity, switching frequency and the square of the peak snubber capacitor voltage.

Snubbers on passive switches (diodes) or active switches (transistors) should always be coupled as closely as physically possible, with minimal loop inductance. This minimizes the radiated field from the change in current path from the switch to the snubber. It also minimizes the turn-off voltage overshoot “required” to force the current to change path through the switch-snubber loop inductance.

Ringing in Clamp Zeners

A capacitor-to-capacitor ringing problem can occur when a voltage clamping Zener or TransZorb[®] is placed across the output of a converter for overvoltage protection (OVP). Power Zeners have a large junction capacity, and this can ring in series with the lead ESL and the output capacitors, with some of the ringing voltage showing up on the output. This ringing current can be most easily detected near the Zener leads, particularly on the inside of a bend as shown in Figure J6.

R-C snubbers have not been found to work well in this case as the ringing loop inductance is often as low or lower than the obtainable parasitic inductance in the snubber. Increasing the external loop inductance to allow damping is not advisable as this would limit dynamic clamping capability. In this case, it was found that a small ferrite bead on one or both of the Zener leads dampened the HF oscillations with minimal adverse side effects (a high permeability ferrite bead quickly saturates as soon as the Zener begins to conduct significant current).

TransZorb is a registered trademark of General Instruments, GSI.

Paralleled Rectifiers

A less evident problem can occur when dual rectifier diodes in a package are paralleled for increased current capability, even with a tightly coupled R-C snubber. The two diodes seldom recover at exactly the same time, which can cause a very high frequency oscillation (hundreds of MHz) to occur between the capacities of the two diodes in series with the anode lead inductances, as shown in Figure J7. This effect can really only be observed by placing the probe between the two anode leads, as the ringing current exists almost nowhere else (the ringing is nearly “invisible” to a conventional voltage probe, like many other EMI effects that can be easily found with a magnetic field Sniffer Probe).

This “teeter-totter” oscillation has a voltage “null” about where the R-C snubber is connected, so it provides little or no damping (see Figure J7a). It is actually very difficult to insert a suitable damping resistance into this circuit.

The easiest way to dampen the oscillation is to “slit” the anode PC trace for an inch or so and place a damping resistor at the anode leads as shown in Figure J7b. This

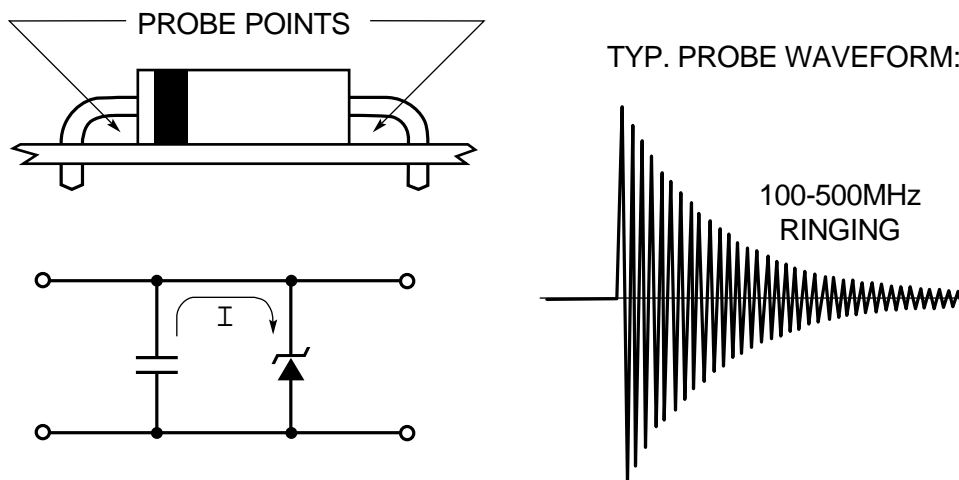


Figure J6. Ringing Between Clamp Zener and Capacitor
Typical Fix: Small Ferrite Bead on Zener Lead(s)

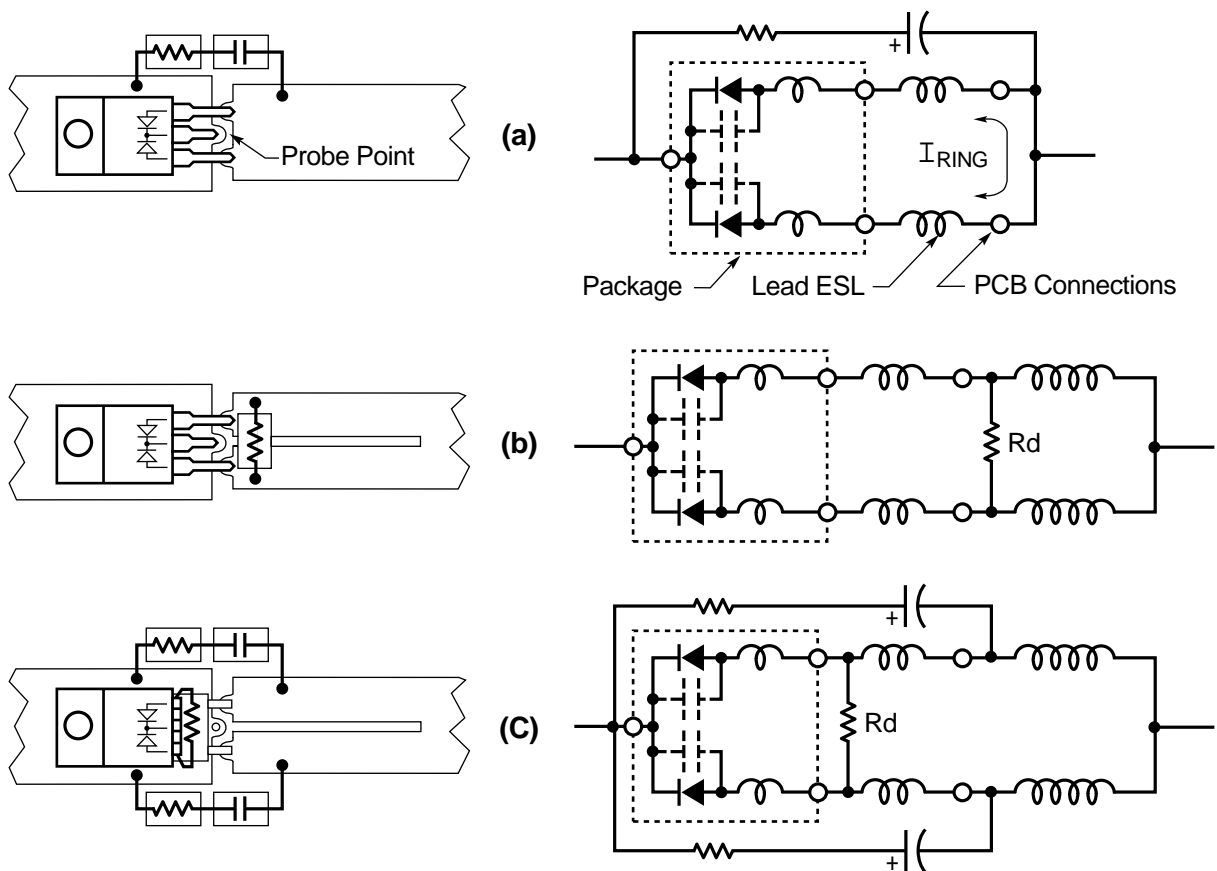


Figure J7. Ringing in Paralleled Dual Rectifiers

increases the inductance in series with the diode-diode loop external to the package and leads, while having minimal effect on the effective series inductance. Even better damping is obtained by placing the resistor across the anode leads at the entry point to the case, as shown in Figure J7c, but this violates the mindset of many production engineers.

It is also preferable to split the original R-C damper into two $(2R) - (C/2)$ dampers, one on each side of the dual rectifier (also shown in Figure 7c). In practice, it is always preferable to use dual R-C dampers, one each side of the diode; loop inductance is cut about in half, and the external di/dt field is reduced even further due to the oppositely “handed” currents in the two snubber networks.

Paralleled Snubber or Damper Caps

A problem similar to that with the paralleled diodes occurs when two or more low loss capacitors are paralleled and driven with a sudden current change. There is a tendency for a current to ring between the two capacitors in series with their lead inductances (or ESL), as shown in Figure J8a. This type of oscillation can usually be detected by placing the Sniffer Probe between the leads of the paralleled capacitors. The ringing frequency is much lower than with the paralleled diodes (due to the larger capacity), and the effect *may* be benign if the capacitors are sufficiently close together.

If the resultant ringing *is* picked up externally, it can be damped in a similar way as with the parallel diodes as shown in Figure J8b. In either case, the dissipation in the damping resistor tends to be relatively small.

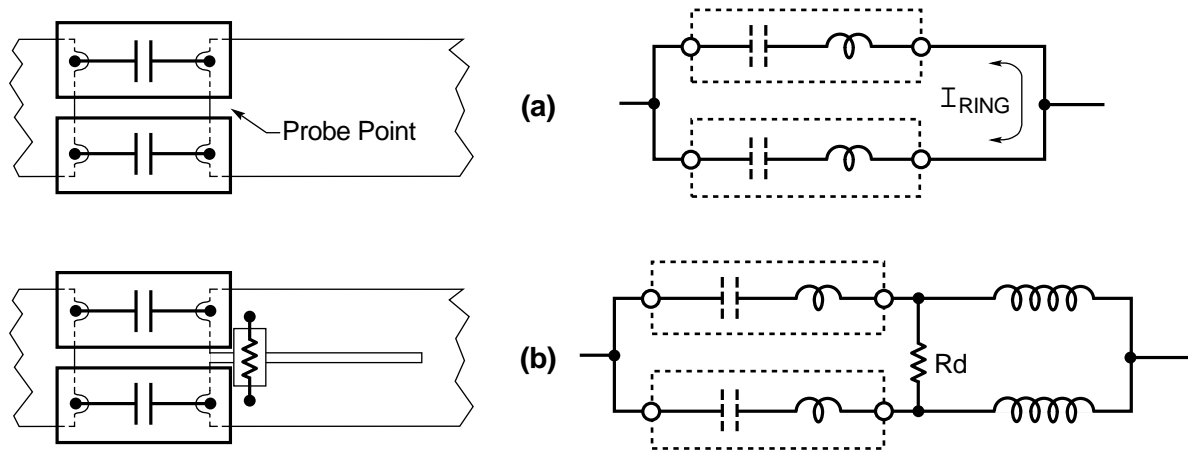


Figure J8. Ringing in Paralleled “Snubber” Capacitors

Ringling in Transformer Shield Leads

The capacity of a transformer shield to other shields or windings (C_S in Figure J9) forms a series resonant circuit with its “drain wire” inductance (L_S) to the bypass point. This resonant circuit is readily excited by typical square wave voltages on windings, and a poorly damped oscillatory current may flow in the drain wire. The shield current may radiate noise into other circuits, and the shield voltage will often show up as common mode conducted noise. The shield voltage is very difficult to detect with a voltage probe in most transformers, but the ringing shield current can be observed by holding the Sniffer Probe near the shield drain wire (Figure J10), or the shield current’s return path in the circuit.

This ringing can be dampened by placing a resistor R_D in series with the shield drain wire, whose value is approximately equal to the surge impedance of the resonant circuit, which may be calculated from the formula in Figure J9.

The shield capacitance (C_S) can readily be measured with a bridge (as the capacity from the shield to all facing shields and/or windings), but L_S is usually best calculated from C_S and the ringing frequency (as sensed by the Sniffer Probe). This resistance is typically on the order of tens of ohms.

One or more small ferrite beads can also be placed on the drain wire instead to provide damping. This option may be preferable as a late “fix” when the PC board has already been laid out.

In either case, the damper losses are typically quite small. The damper resistor has a moderately adverse impact on shield effectiveness below the shield and drain wire resonant frequency; damper beads are superior in this respect as their impedance is less at lower frequencies. The drain wire connection should also be as short as possible to the circuit bypass point, both to minimize EMI and to raise the shield’s maximum effective (i.e., resonant) frequency.

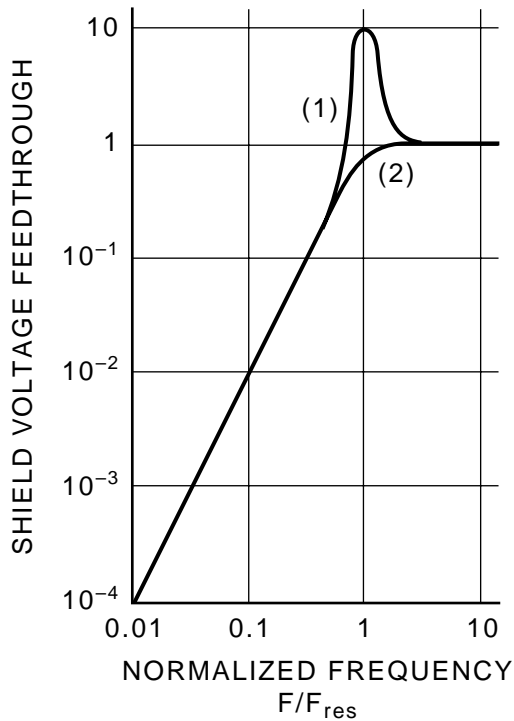
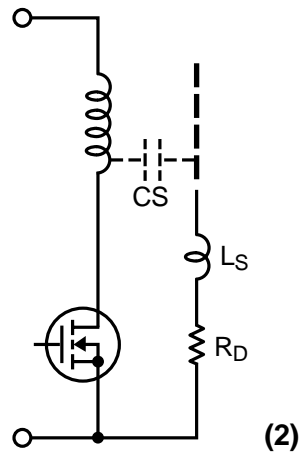
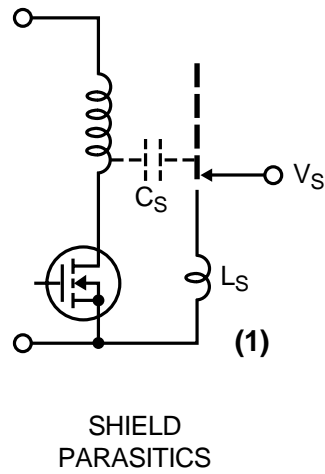
Leakage Inductance Fields

Transformer leakage inductance fields emanate from between primary and secondary windings. With a single primary and secondary, a significant dipole field is created, which may be seen by placing the Sniffer Probe near the winding ends as shown in Figure J11a. If this field is generating EMI, there are two principal fixes:

1. Split the Primary *or* Secondary in two, to “sandwich” the other winding, and/or:
2. Place a shorted copper strap “electromagnetic shield” around the *complete-core and winding* assembly as shown in Figure J12. Eddy currents in the shorted strap largely cancel the external magnetic field.

The first approach creates a “quadrupole” instead of a dipole leakage field, which significantly reduces the distant field intensity. It also reduces the eddy current losses in any shorted strap electromagnetic shield used, which may or may not be an important consideration.

Application Note 70



SHIELD RESONANCE
CAN BE DAMPED WITH
A RESISTOR "R_D" OR A
SMALL FERRITE BEAD:

$$R_D \cong \sqrt{\frac{L_S}{C_S}}$$

Figure J9. Shield Effectiveness at High Frequencies Is Limited by Shield Capacity and Lead Inductance

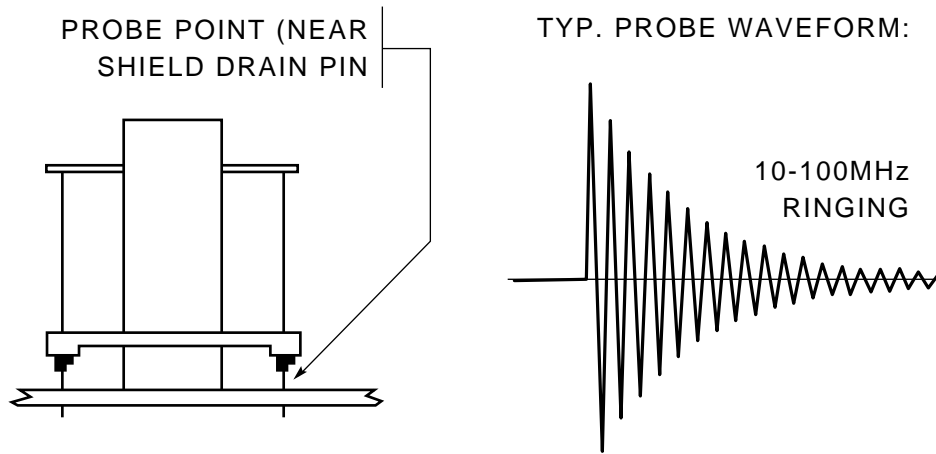


Figure J10. Transformer Shield Ringing
 Typical Fix: 10Ω to 100Ω Resistor
 (or Ferrite Bead in Drain Wire)

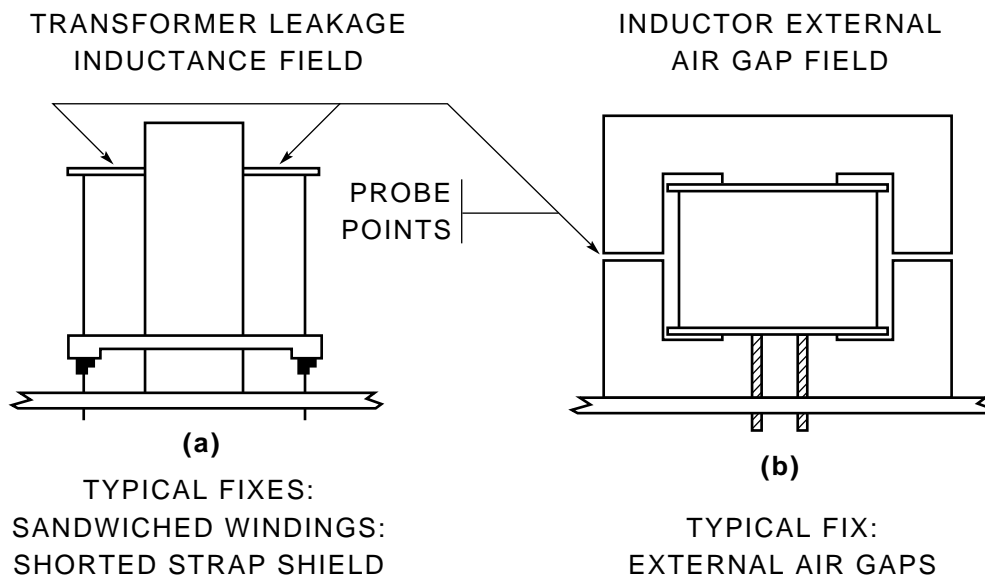


Figure J11. Probe Voltages Resemble the Transformer and Inductor Winding Waveforms

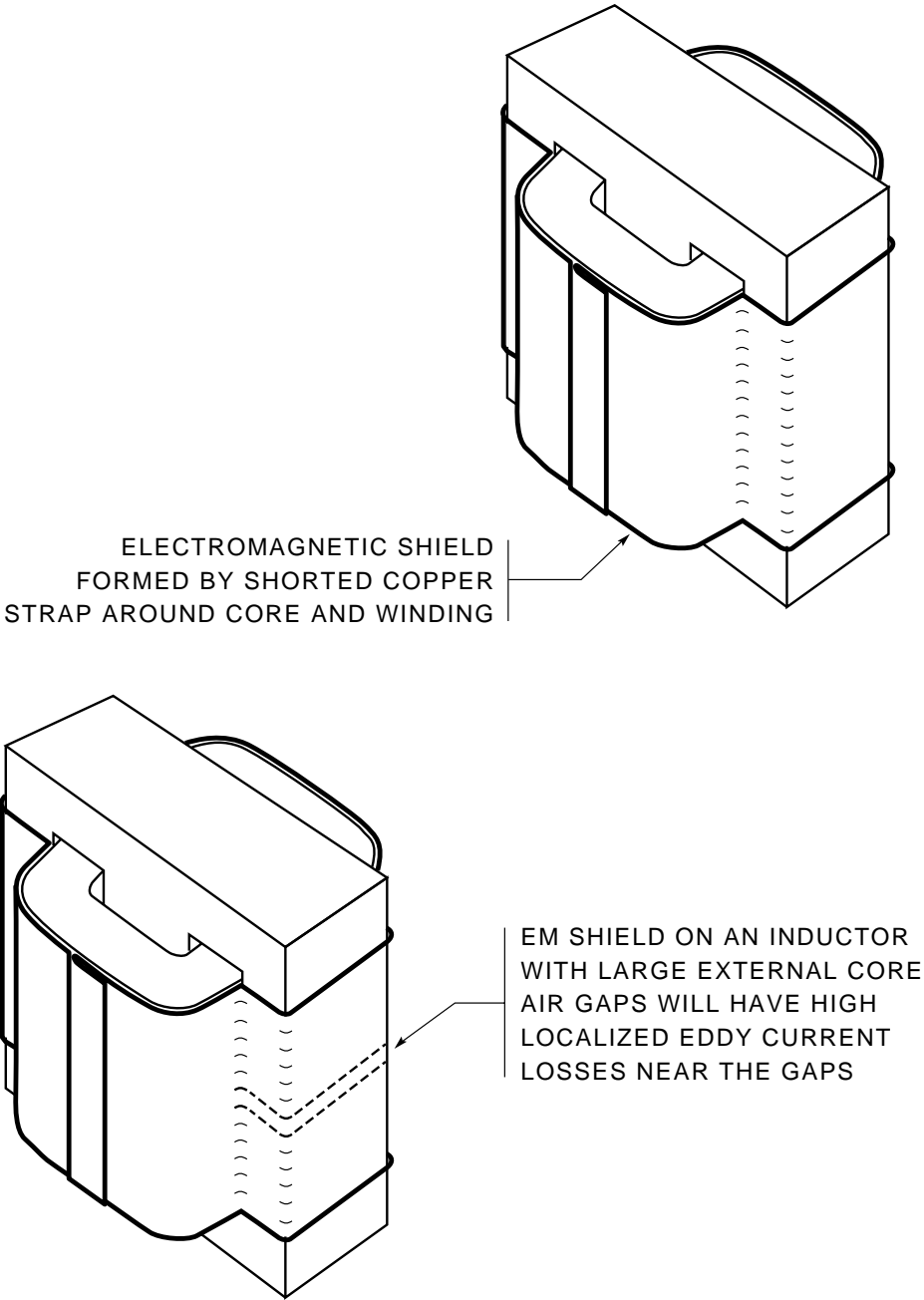


Figure J12. A "Sandwiched" PRI-SEC Transformer Winding Construction Reduces Electromagnetic Shield Eddy Current Losses

External Air Gap Fields

External air gaps in an inductor, such as those in open “bobbin core” inductors or with “E” cores spaced apart (Figure J11b), can be a major source of external magnetic fields when significant ripple or AC currents are present. These fields can also be easily located with the Sniffer Probe; response will be a maximum near an air gap or near the end of an open inductor winding.

“Open” inductor fields are not readily shielded and if they present an EMI problem the inductor must usually be redesigned to reduce external fields. The external field around spaced E cores can be virtually eliminated by placing all of the air gap in the center leg. Fields due to a (possibly intentional) residual or minor outside air gap can be minimized with the shorted strap electromagnetic shield of Figure J12, if eddy current losses prove not to be too high.

A less obvious problem may occur when inductors with “open” cores are used as second stage filter chokes. The minimal ripple current may not *create* a significant field, but such an inductor can “pick up” external magnetic fields and convert them to noise voltages or be an EMI *susceptibility* problem.³

Poorly Bypassed High Speed Logic

Ideally, all high speed logic should have a tightly coupled bypass capacitor for each IC and/or have power and ground distribution planes in a multilayer PCB.

At the other extreme, I have seen *one* bypass capacitor used at the power entrance to a logic board, with power and ground led to the ICs from opposite sides of the board. This created large spikes on the logic supply voltage and produced significant electromagnetic fields around the board.

With a Sniffer Probe, I was able to show which pins of which ICs had the larger current transients *in synchronism* with the supply voltage transients. (The logic design engineers were accusing the power supply vendor of creating the noise. I found that the supplies were fairly quiet; it was the poorly designed logic power distribution system that was the problem.)

Probe Use with a “LISN”

A test setup using the Sniffer Probe with a Line Impedance Stabilization Network (LISN) is shown in Figure J13. The optional “LISN AC LINE FILTER” reduces AC line voltage feedthrough from a few 100mV to microvolt levels, simplifying EMI diagnosis when a suitable DC voltage source is not available or cannot be used.

TESTING THE SNIFFER PROBE

The Sniffer Probe can be functionally tested with a jig similar to that shown in Figure J14, which is used to test probes in production.

Note 3: Ed Note. See Appendix H for additional commentary.

Application Note 70

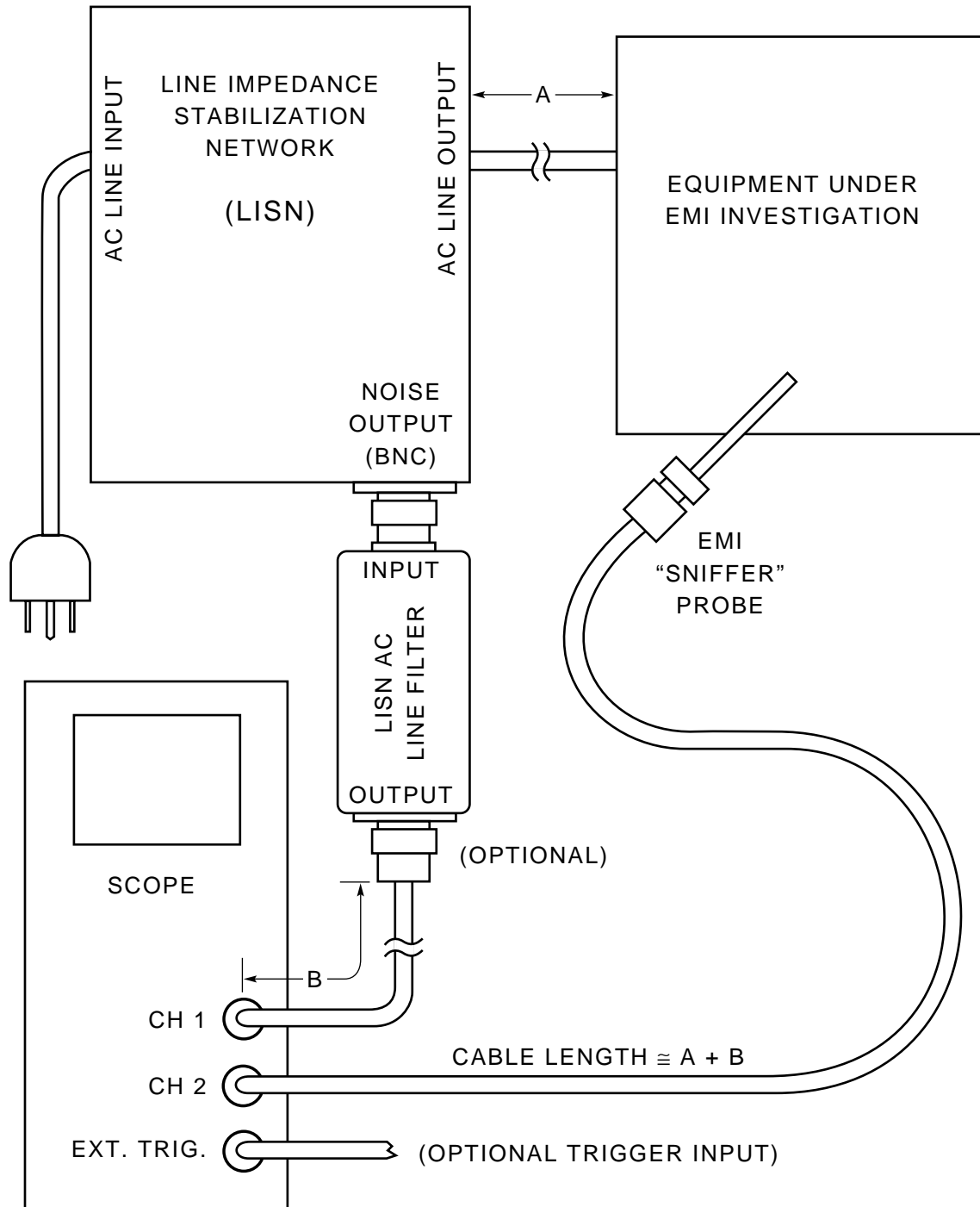
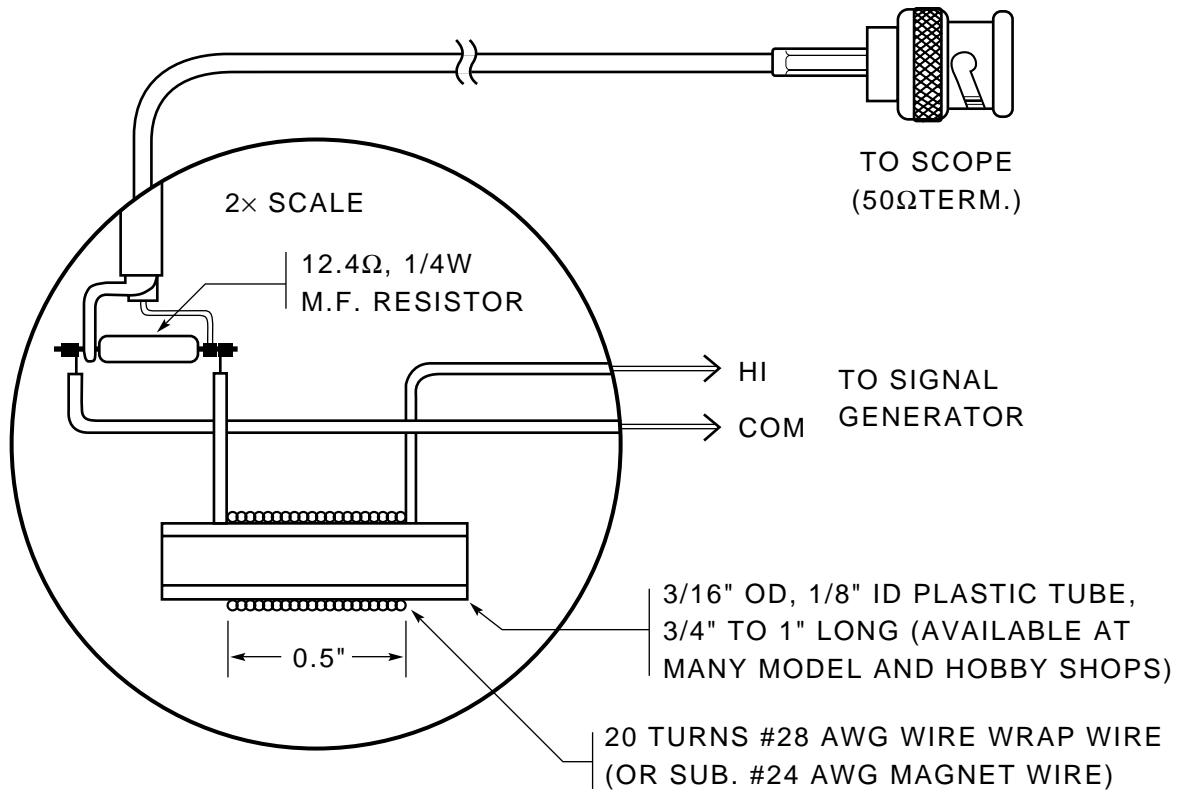


Figure J13. Using the Probe with a "LISN"



The Sniffer Probe Tip is centered inside the test coil where the Probe voltage is greatest. The approximate flux density in the middle of a coil can be calculated from the formula:

$$B = H = 1.257 NI/I \quad (\text{CGS Units})$$

For the 1.27cm long, 20-turn test coil, the flux density is about 20 Gauss per amp. At 1MHz, the Sniffer Probe voltage is 19mV_{P-P} (±10%) per 100mA_{P-P} for a 1MΩ load impedance, and half that for a 50Ω load.

Figure J14. EMI "Sniffer" Probe Test Coil

Application Note 70

CONCLUSION

The Sniffer Probe is a simple, but very fast and effective means to locate di/dt sources of EMI. These EMI sources are very difficult to locate with conventional voltage or current probes.

SUMMARY

A summarized procedure for using the EMI “Sniffer” Probe appears in Figure J15.

- 1) Use a 2-channel scope, preferably one with an external trigger.
- 2) One scope channel is used for the Sniffer Probe, which is not to be used for triggering.
- 3) The second channel is used to view the noise transient whose source is to be located, which may also be used for triggering if practical.
- 4) More stable and reliable triggering is achieved with an “external trigger” (or a 3rd channel) on a transistor drive waveform (or preceding logic transition), allowing immediate precursors to the transient to be viewed. (Nearly all noise transients occur during, or just after, a power transistor turn-on or turn-off.
- 5) Start with the Probe at some distance from the circuit with maximum sensitivity and “sniff around” for something happening in *precise sync* with the noise transient. The Probe waveform will not be identical to the noise transient, but will usually have a strong resemblance.
- 6) Move the Probe closer to the suspected source while decreasing sensitivity. The conductor carrying the responsible current is located by the sharp response null on top of the conductor with inverted polarity on each side.
- 7) Trace out the noise current path as much as possible. Identify the current path on the schematic.
- 8) The source of the noise transient is usually evident from the current path and the timing information.

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Figure J15. EMI “Sniffer” Probe Procedure Outline

SNIFFER PROBE AMPLIFIER

Figure J16 shows a 40MHz amplifier for the Sniffer Probe. A gain of 200 allows an oscilloscope to display probe output over a wide range of sensed inputs. The amplifier is built into a small aluminum box. The probe should connect to the amplifier via BNC cable, although the 50Ω

termination does not have to be a high quality coaxial type. The probe's uncalibrated, relative output means high frequency termination aberrations are irrelevant. A simple film resistor, contained in the amplifier box, is adequate. Figure J17 shows the Sniffer Probe and the amplifier.

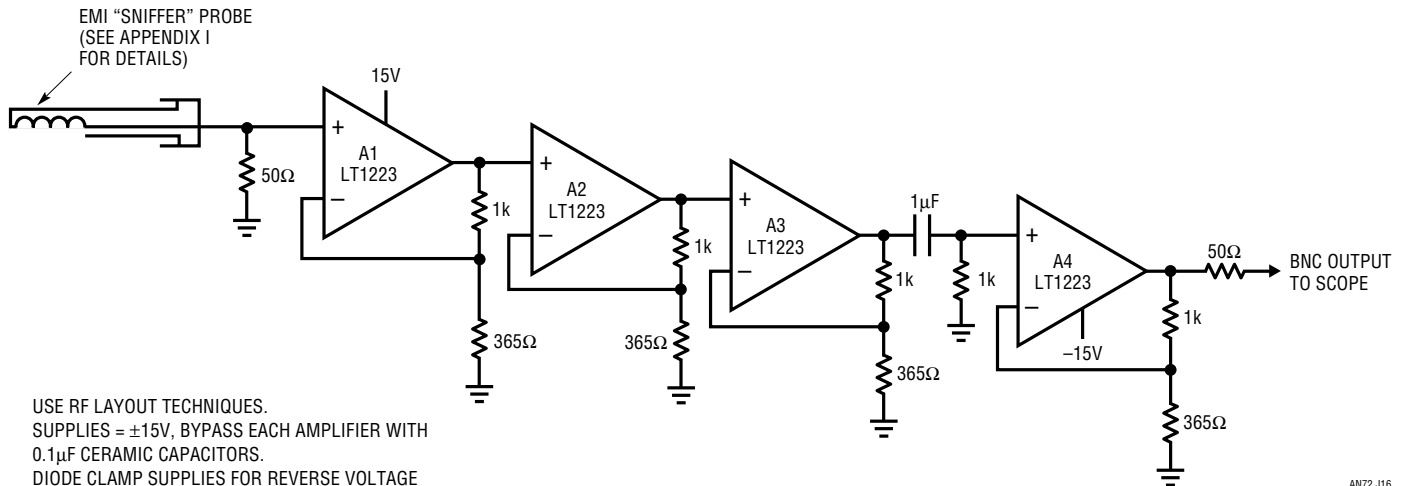


Figure J16. 40MHz Amplifier for EMI Probe

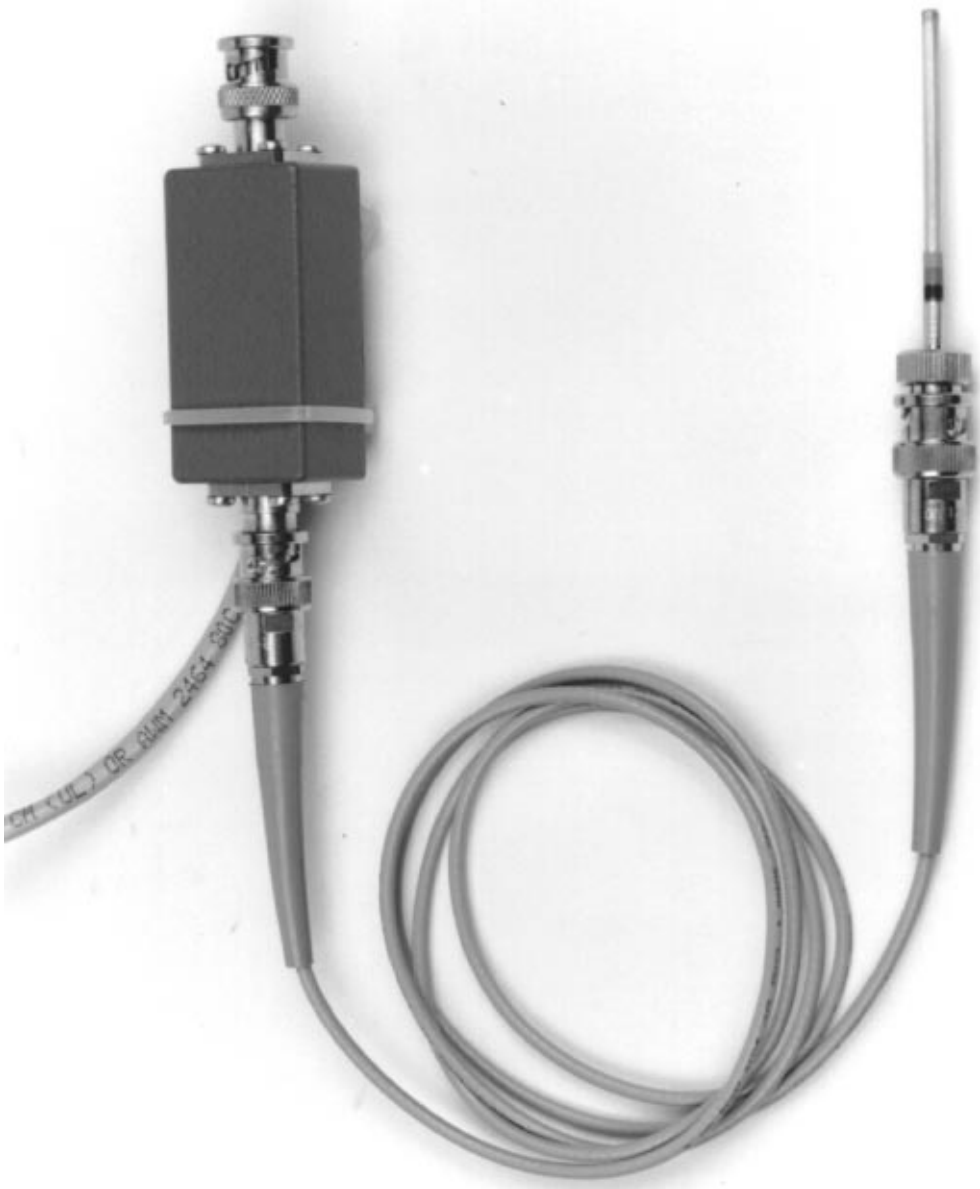


Figure J17. Sniffer Probe and Amplifier. Note All BNC-Based Signal Transmission.
±15V Power Enters Box via Separate Cable

APPENDIX K

SYSTEM-BASED NOISE "MEASUREMENT"

The ultimate test of switching regulator noise is its effect on the system being powered. The data below was taken using an LT1533 powering an LT1605 16-bit A/D converter. Crossplots for integral and differential nonlinearity

are shown for bench supply vs LT1533 supply powered operation. The difference is within the test systems limit-of-error.

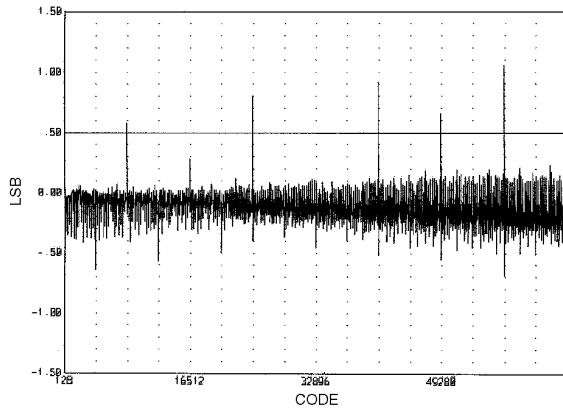


Figure K1. Differential Nonlinearity Using Bench Supply

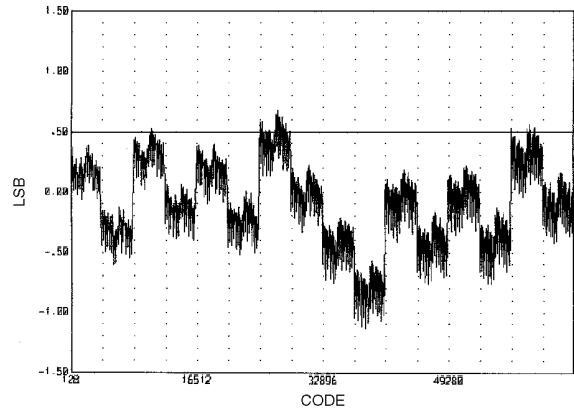


Figure K4. Integral Nonlinearity Using Bench Supply

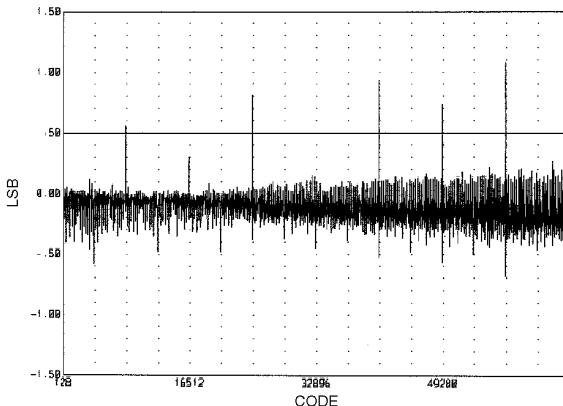


Figure K2. Differential Nonlinearity Using LT1533 Supply

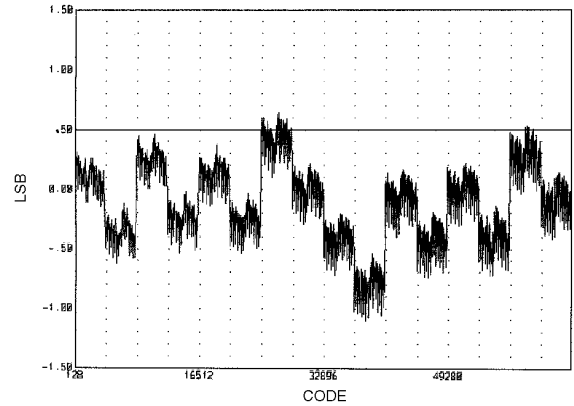


Figure K5. Integral Nonlinearity Using LT1533 Supply

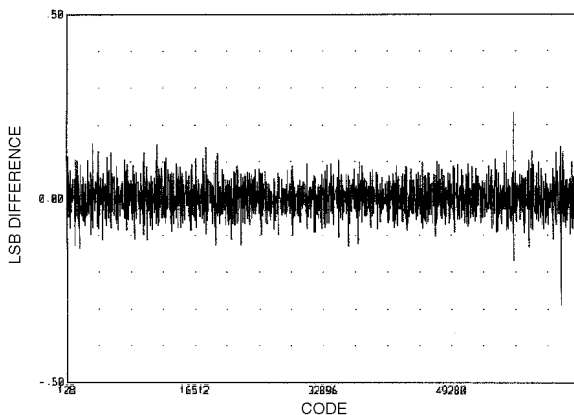


Figure K3. Subtraction of Above Plots. Residual Error Is Test System Limited

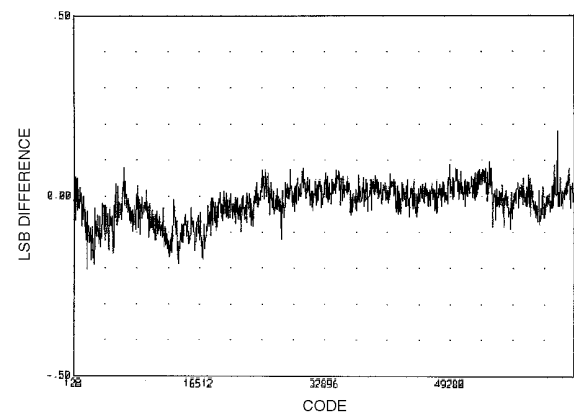
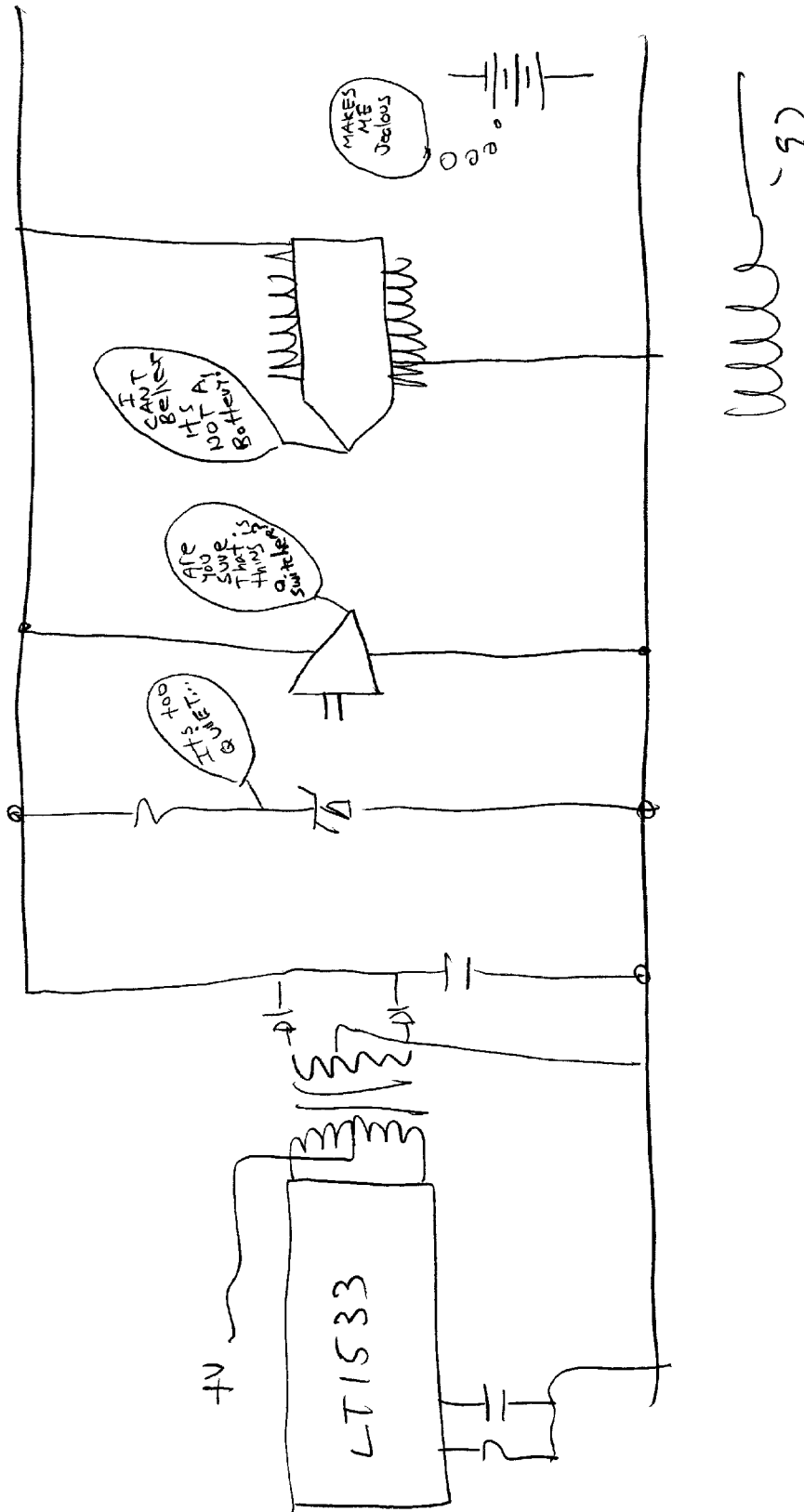


Figure K6. Subtraction of Above Plots. Residual Error Is Test System Limited

Application Note 70



A Seven-Nanosecond Comparator for Single Supply Operation

Guidance for Putting Civilized Speed to Work

Jim Williams

INTRODUCTION

In 1985 Linear Technology Corporation introduced the LT[®]1016 Comparator. This device was the first readily usable, high speed TTL comparator. Previous ICs were either too slow or unstable, preventing widespread acceptance. The LT1016 was, and is, a highly successful product.

Recent technology trends have emphasized low power, single supply operation. The LT1016, although capable of such operation, does not include ground in its input range. As such, it must be biased into its operating common mode range for practical single supply use. A new device, the LT1394, maintains the speed and application civility of its predecessor while including ground in its input operating range. Additionally, the new comparator is faster and pulls significantly lower operating current than the LT1016.

This publication borrows shamelessly from earlier LTC efforts, while introducing new material.¹ It approximates, affixes, appends, abridges, amends, abbreviates, abrogates, ameliorates and augments the previous work.² More specifically, the applications section has been almost entirely refurbished, reflecting the LT1394's single supply agility. Additionally, tutorial content has been expanded beyond previous efforts. This approach is necessitated by the continuing need for tutorial guidance in the application of high speed linear devices. The rules of

the game are never obviated by new components; rather, they become even more significant as performance increases.


Comparators may be the most underrated and underutilized monolithic linear component. This is unfortunate because comparators are one of the most flexible and universally applicable components available. In large measure the lack of recognition is due to the IC op amp, whose versatility allows it to dominate the analog design world. Comparators are frequently perceived as devices that crudely express analog signals in digital form—a 1-bit A/D converter. Strictly speaking, this viewpoint is correct. It is also wastefully constrictive in its outlook. Comparators don't "just compare" in the same way that op amps don't "just amplify."

Comparators, in particular high speed comparators, can be used to implement linear circuit functions which are as sophisticated as any op amp-based circuit. Judiciously combining a fast comparator with op amps is a key to achieving high performance results. In general, op amp-based circuits capitalize on their ability to close a feedback loop with precision. Ideally, such loops are maintained continuously over time. Conversely, comparator circuits are often based on speed and have a discontinuous output over time. While each approach has its merits, a fusion of both yields the best circuits.

This effort's initial sections are devoted to familiarizing the reader with the realities and difficulties of high speed

Note 1: In particular LTC Application Note 13, "High Speed Comparator Techniques." Additional text has been similarly purloined from other LTC sources. See the References section following the main text for specifics.

Note 2: An alliterative amalgamated assemblage.

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Application Note 72

comparator circuit work. The mechanics and subtleties of achieving precision circuit operation at DC and low frequency have been well documented. Relatively little has appeared that discusses, in practical terms, how to get fast circuitry to work. In developing such circuits, even the most veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high speed circuits can only work if negotiated compromises with nature are arranged. Ignorance of, or contempt for, physical law is a direct route to frustration. In this regard, much of the text and appendices are directed at developing awareness of, and respect for, circuit parasitics and fundamental limitations. This approach is maintained in the applications

section, where the notion of “negotiated compromises” is expressed in terms of resistor values and compensation techniques. Many of the application circuits use the LT1394’s speed to improve on a standard circuit. Some utilize the speed to implement a traditional function in a nontraditional way, with attendant advantages. A (very) few operate at or near the state-of-the-art for a given circuit type, regardless of approach. Substantial effort has been expended in developing these examples and documenting their operation. The resultant level of detail is justified in the hope that it will be catalytic. The circuits should stimulate new ideas to suit particular needs, while demonstrating the LT1394’s capabilities in an instructive manner.

TABLE OF CONTENTS

INTRODUCTION	AN72-1
THE LT1394—AN OVERVIEW	AN72-4
The Rogue’s Gallery of High Speed Comparator Problems	AN72-5
Bypassing	AN72-5
Probe Compensation	AN72-5
Probe Bandwidth	AN72-5
Probe Grounding	AN72-6
FET Probe Considerations	AN72-6
Comparator Grounding	AN72-6
Ground Planes	AN72-7
Source Impedance Considerations	AN72-7
Stray Capacitance at Inputs	AN72-7
Output Loading	AN72-7
Output Termination	AN72-8
Input Common Mode Level	AN72-8
TUTORIAL SECTION	
About Pulse Generators	AN72-8
About Cables, Connectors and Terminations	AN72-9
About Probes and Probing Techniques	AN72-10
About Oscilloscopes	AN72-14
About Ground Planes	AN72-18
About Bypass Capacitors	AN72-19
Breadboarding Techniques	AN72-20
APPLICATIONS	
Crystal Oscillators	AN72-21
Switchable Output Crystal Oscillator	AN72-21
Temperature-Compensated Crystal Oscillator	AN72-22
Voltage-Controlled Crystal Oscillator	AN72-23
Voltage-Tunable Clock Skew Generator	AN72-23
Simple 10MHz Voltage-to-Frequency Converter	AN72-25
Precision 1Hz to 10MHz Voltage-to-Frequency Converter	AN72-26
Fast, High Impedance, Variable Threshold Trigger	AN72-28
High Speed Adaptive Trigger Circuit	AN72-29
18ns, 500 μ V Sensitivity Comparator	AN72-29
Voltage-Controlled Delay	AN72-31
10ns Sample-and-Hold	AN72-32
Programmable Sub-Nanosecond Delayed Pulse Generator	AN72-32
Fast Pulse Stretcher	AN72-34
20ns Response Overvoltage Protection Circuit	AN72-36
REFERENCES	AN72-37
APPENDICES	
A: About Level Shifts	AN72-38
B: Measuring Probe-Oscilloscope Response	AN72-40

Application Note 72

THE LT1394 — AN OVERVIEW

A new ultrahigh speed comparator, the LT1394, features TTL-compatible complementary outputs and 7ns response time. Other capabilities include a latch pin and good DC input characteristics (see Figure 1). The LT1394's outputs directly drive all 5V families, including the higher speed ASTTL, FAST and HC parts. Additionally, TTL outputs make the device easier to use in linear circuit applications where ECL output levels are often inconvenient.

A substantial amount of design effort has made the LT1394 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1394 is stable in its linear region. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. Finally, current consumption is

far lower than previous devices. These features make the 200GHz gain bandwidth LT1394 considerably easier to apply than other fast comparators. Unfortunately, laws of physics dictate that the circuit *environment* the LT1394 works in must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance and layout. Some of these considerations are present in digital systems, where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1394 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1394's (Trace B) response to the pulse generator (Trace A) is faster than a TTL inverter (Trace C)! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

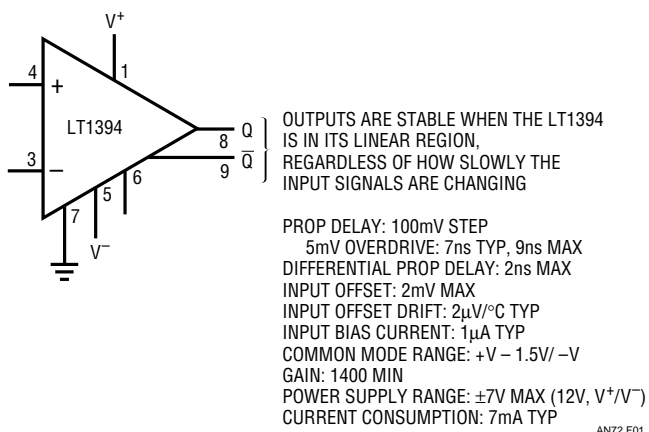


Figure 1. The LT1394 at a Glance

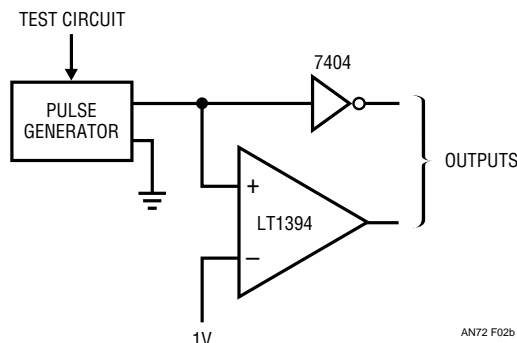
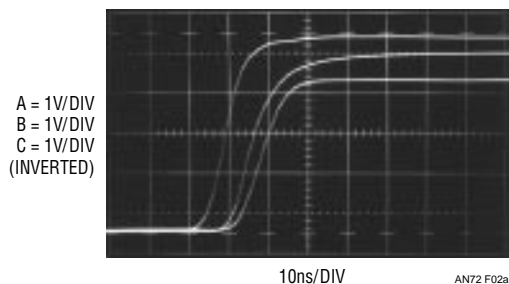


Figure 2. LT1394 vs a TTL Gate

The Rogue's Gallery of High Speed Comparator Problems

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can “communicate” through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully (see “About Bypass Capacitors” in the Tutorial section). An unbypassed LT1394 is shown responding to a pulse input in Figure 3. The power supply the LT1394 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1394, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. Although the LT1394 re-

sponds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

In Figure 4 the LT1394's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount them as close as possible to the LT1394. An inch of wire between the capacitor and the LT1394 can cause problems.*

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V—quite a trick for a device running from a 5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes that match your oscilloscope's input characteristics and compensate them properly* (for a discussion on probes, see “About Probes and Probing Techniques” in the Tutorial section). Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 7ns response time LT1394 appears to have 50ns edges! In this case, the probe used is too heavily compensated or slow for the oscilloscope.

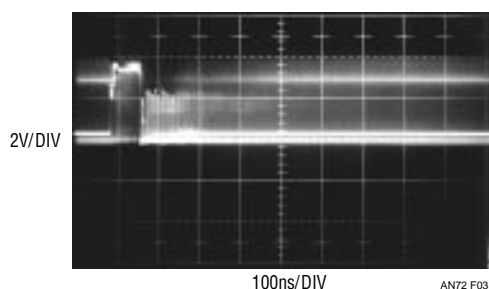


Figure 3. Unbypassed LT1394 Response

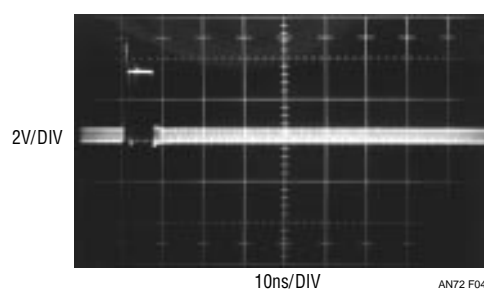


Figure 4. LT1394 Response with Poor Bypassing

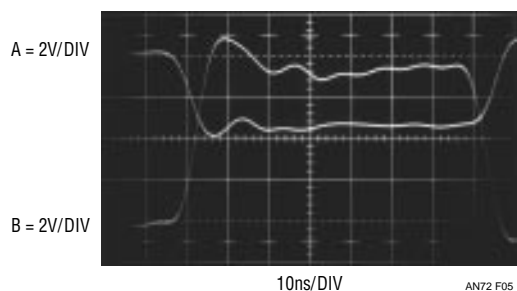


Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

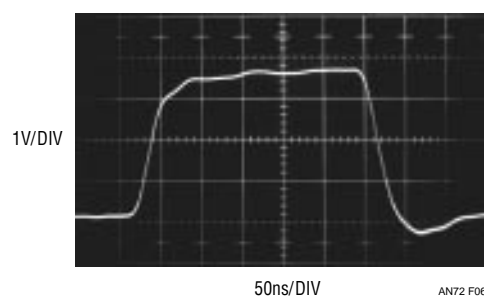


Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

Application Note 72

Never use 1× or “straight” probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure that it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

In Figure 7 the probes are properly selected and applied but the LT1394’s output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about six inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips that fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed one inch in length. *Keep the probe ground connection as short as possible.*

The difficulty in Figure 8 is delay and inadequate amplitude (Trace B). A small delay on the leading edge is followed by

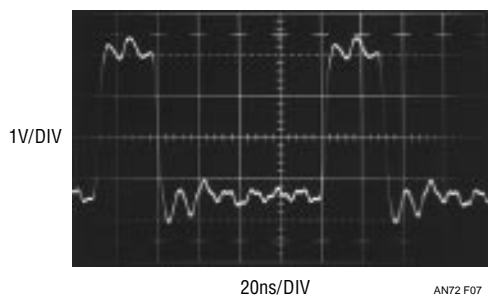


Figure 7. Typical Results Due to Poor Probe Grounding

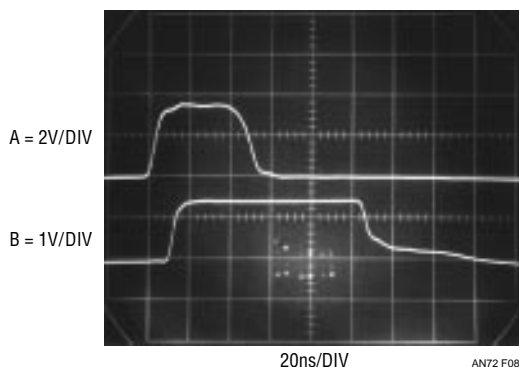


Figure 8. Overdriven FET Probe Causes Delayed, Tailing Response

a large delay before the falling edge begins. Additionally, a lengthy, tailing response stretches 70ns before finally settling out. The amplitude only rises to 1.5V. A common oversight is responsible for these conditions.

A FET probe monitors the LT1394 output in this example. The probe’s common mode input range has been exceeded, causing it to overload and clip the output badly. The small delay on the rising edge is characteristic of active probes and is legitimate. During the time the output is high, the probe is driven deeply into saturation. When the output falls, the probe’s overload recovery is lengthy and uneven, causing the delay and tailing.

Know your FET probe. Account for the delay of its active circuitry. Avoid saturation effects due to common mode input limitations (typically $\pm 1V$). Use 10× and 100× attenuator heads when required.

Figure 9 shows the LT1394’s output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1394’s ground pin connection is one inch long. The ground lead of the LT1394 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1394’s ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1394’s ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

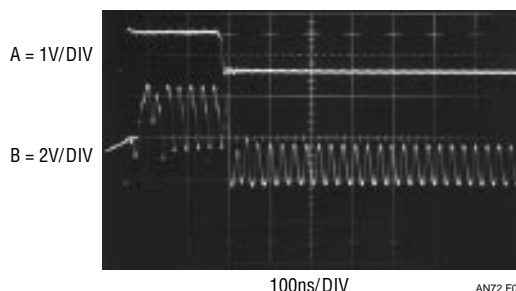


Figure 9. Excessive LT1394 Ground Path Resistance Causes Oscillation

Figure 10 addresses the issue of the “low impedance ground,” referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1394 without a “ground plane.” A ground plane is formed by using a continuous conductive plane over the surface of the circuit board (ground plane theory is discussed in the Tutorial section). The only breaks in this plane are for the circuit’s necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1394.*

“Fuzz” on the edges is the difficulty in Figure 11. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A $3\text{k}\Omega$ input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedance as low as possible, preferably $1\text{k}\Omega$ or less. Route output and input pins and components away from each other.*

The opposite of stray-caused oscillations appears in Figure 12. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input and output delay occurs. An RC combination of $2\text{k}\Omega$ source resistance and 10pF to ground gives a 20ns time constant—significantly longer than the LT1394’s response time. *Keep source impedance low and minimize stray input capacitance to ground.*

Figure 13 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few circumstances

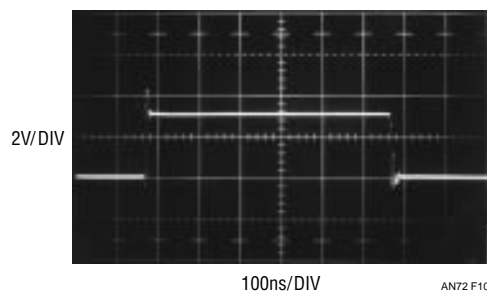


Figure 10. Transition Instabilities Due to No Ground Plane

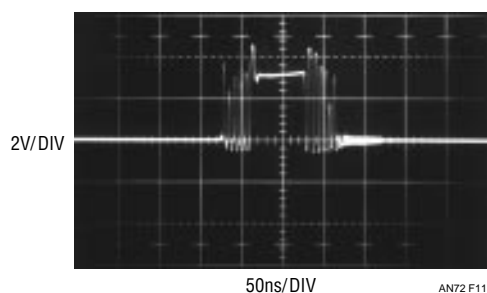


Figure 11. 3pF Stray Capacitive Feedback with $3\text{k}\Omega$ Source Can Cause Oscillation

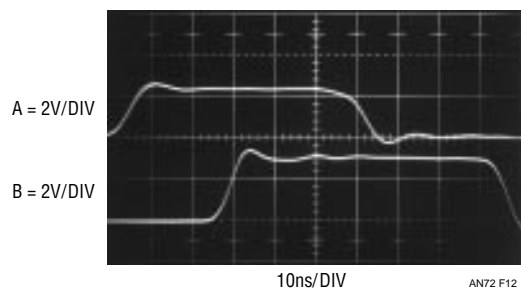


Figure 12. Stray 5pF Capacitance from Input to Ground Causes Delay

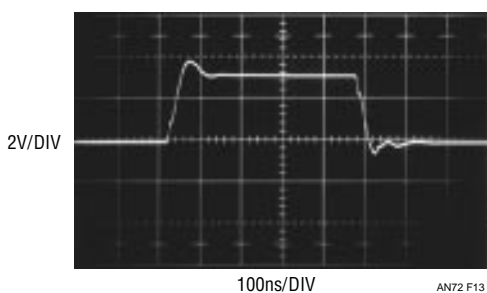


Figure 13. Excessive Load Capacitance Forces Edge Distortion

Application Note 72

it may not affect overall circuit operation and is tolerable. Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.

Another output-caused fault is shown in Figure 14. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead that is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. Similarly, outputs and inputs can see excursions outside supply bounds due to poorly terminated lines, causing device misfunction or failure. Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typi-

cally 250Ω to 400Ω). Ensure that device terminals remain inside supply limits at all times.

A final malady is presented in Figure 15. These waveforms are reminiscent of Figure 12's input RC-induced delay. The output waveform initially responds to the input's leading edge, but then returns to zero before going high again. When it does go high, it slews slowly. Additional odd characteristics include pronounced overshoot and pulse top aberration. The fall time is also slow and well delayed from the input. This is certainly strange behavior from a TTL output. What is going on here? The input pulse is responsible for all these anomalies. Its 10V amplitude is well outside the 5V-powered LT1394's common mode input range. Internal input clamps prevent this pulse from damaging the LT1394, but an overdrive of this magnitude results in poor response. Keep input signals inside the LT1394's common mode range at all times.

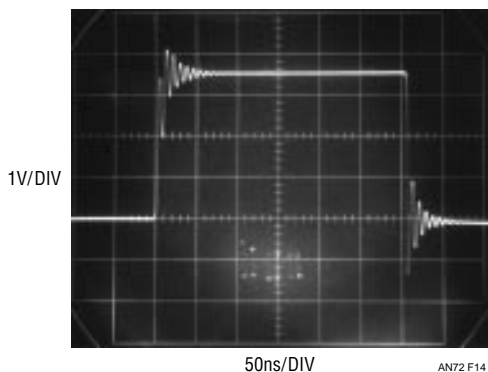


Figure 14. Lengthy, Unterminated Output Lines Ring from Reflections

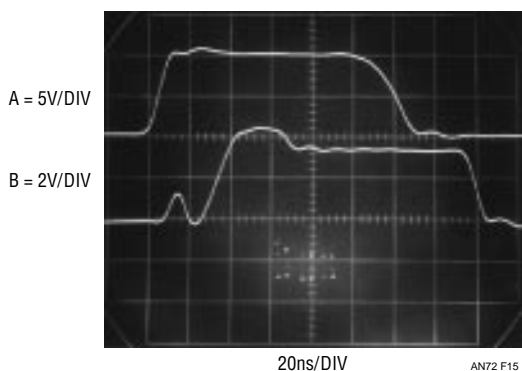


Figure 15. Input Common Mode Overdrive Generates Odd Outputs

TUTORIAL SECTION

An implied responsibility in raising the aforementioned issues is their solution or elimination. What good is all the rabble-rousing without suggestions for fixes? It is in this spirit that this tutorial section is presented. Theory, techniques, prejudice and just plain gossip are offered as tools that may help avoid or deal with difficulties.

About Pulse Generators

A significant consideration for fast comparator development work is the pulse generator. Features such as variable rise and fall time, output DC biasing capability, triggering facilities and amplitude range are highly desirable. General purpose pulse generators usually provide some or all of these capabilities, and little editorial comment is required. Less common, however, particularly at any reasonable price, are really fast pulse generators suitable for LT1394 work. Relatively few generators have transition times below 2.5ns. This kind of speed is highly desirable and some noteworthy instruments bear mention.

The current production Hewlett-Packard 8110A has a fairly complete set of features and 2ns transition times, and is typical of modern, high speed instruments. The older HP-8082A is more versatile, has clean subnanosecond transitions and the "knob driven" panel controls are intuitively easy to use. The Phillips PM-5771, also

well endowed with features, has 2.4ns transitions and is quite inexpensive. Finally, the HP215A, long out of manufacture, is a special case. This instrument has a restricted 0 to 100ns width range and no rise time control, but other features make it uniquely useful. The output has sub-nanosecond transitions with extraordinarily well-controlled and specified pulse shape parameters. The trigger is very agile, permitting continuous time phase adjustment from before to after the main output. External trigger impedance, polarity and sensitivity are also variable. The output, controlled by a stepped attenuator, will put $\pm 10V$ into 50Ω in 800ps.

In general, select a pulse generator with the features needed for the circuit of interest. Also, take the time to acquaint yourself with output pulse characteristics, particularly at the highest speeds. Finally, (this is unadulterated author prejudice), instruments with knobs remain easier and faster to set up and modify than “menu-driven” types. This is important in bench work where the ability to quickly and easily change instrument operating point is paramount. In this regard knobs have no equal. Menus belong in restaurants.

About Cables, Connectors and Terminations

High speed signals should always be routed to and from the circuit board with good quality coaxial cable. The cable should be driven and terminated in the system’s characteristic impedance at the drive and load points. The driven end is usually an instrument (e.g., pulse or signal generator), presumably endowed with proper characteristics by its manufacturer. It is the cable and its termination, selected by the experimenter, that often cause problems.

All coaxial cable is not the same. Use cable appropriate to the system’s characteristic impedance and of good quality. Poorly chosen cable materials or construction methods can introduce odd effects at very high speeds, resulting in observed waveform distortion. A poor cable choice can adversely affect 0.01% settling in the 100ns to 200ns region. Similarly, poor cable can preclude maintenance of even the cleanest pulse generator’s 1ns rise time or purity. Typically, inappropriate cable can introduce tailing, rise time degradation, aberrations following transitions, non-linear impedance and other undesirable characteristics.

Termination choice is equally important. Good quality BNC coaxial type terminators are usually the best choice

for breadboarding. Their impedance vs frequency is flat into the GHz range. Additionally, their construction ensures that the (often substantial) drive current returns directly to the source, instead of being dumped into the breadboard’s ground system. BNC coaxial terminators are not simply resistors in a can. Good grade 50Ω terminators maintain true coaxial form. They use a carefully designed 50Ω resistor with significant effort devoted to connections to the actual resistive element. In particular, the largest possible connection surface area is utilized to minimize high speed losses. These construction techniques ensure optimum wideband response. Figures 16 and 17 demonstrate this nicely. In Figure 16 a 1ns pulse with 350ps rise and fall times³ is monitored on a 1GHz sampling ‘scope (Tektronix 556 with 1S1 sampling

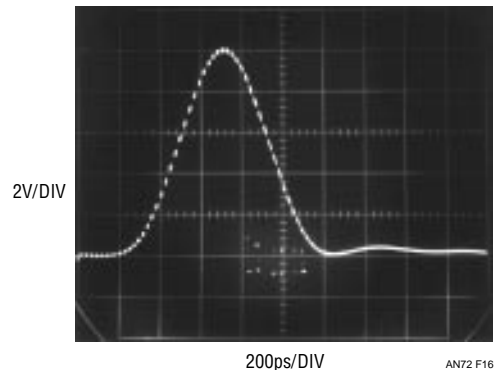


Figure 16. 350ps Rise and Fall Times Are Preserved by a Good Quality Termination

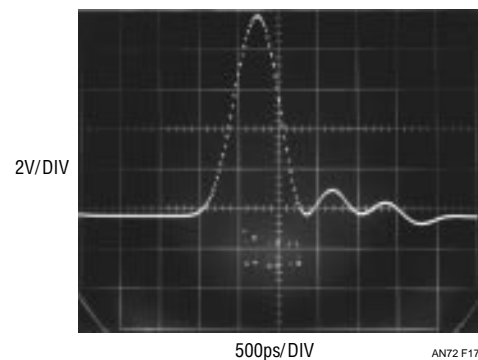


Figure 17. Poor Grade Termination Produces Pronounced Ringing and Tailing in the GHz Range

Note 3: The ability to generate such a pulse proves useful for a variety of tasks, including testing terminators, cables, probes and oscilloscopes for response. The requirements for this pulse generator are surprisingly convenient and inexpensive. For a discussion and construction details see Appendix B “Measuring Probe-Oscilloscope Response.”

Application Note 72

plug-in and P6032 probe). The waveform is clean, with only a slight hint of ring after the falling edge. This photo was taken with a high grade BNC coaxial type terminator in use. Figure 17 does not share these attributes. Here, the generator is terminated with a 50Ω carbon composition resistor with lead lengths of about 1/8 inch. The waveform rings and tails badly on turn-off before finally settling. Note that the sweep speed required a 2.5× reduction to capture these unwanted events. Variable attenuators must provide performance similar to fixed types for meaningful results. The HP-355 series are excellent units, with high fidelity response to 1GHz.

Connectors, such as BNC barrel extensions and tee-type adaptors, are convenient and frequently employed. Remember that these devices represent a discontinuity in the cable, and can introduce small but undesirable effects. In general it is best to employ them as close as possible to a terminated point in the system. Use in the middle of a cable run provides minimal absorption of their mismatch and reflections. The worst offenders among connectors are adaptors. This is unfortunate, as these devices are necessitated by the lack of connection standardization in wideband instrumentation. The mismatch caused by a BNC-to-GR874 adaptor transition at the input of a wideband sampling 'scope is small, but clearly discernible in the display. Similarly, mismatches in almost all adaptors, and even in "identical" adaptors of different manufacture, are readily measured on a high frequency network analyzer such as the Hewlett-Packard 4195A⁴ (for additional wisdom and terror along these lines see Reference 1).

BNC connections are easily the most common, but not necessarily the most desirable, wideband connection mechanism. The ingenious GR874 connector has notably superior high frequency characteristics, as does the type N. Unfortunately, it's a BNC world out there.

About Probes and Probing Techniques

The choice of which oscilloscope probe to use in a measurement is absolutely crucial. The probe must be considered as an inherent part of the circuit under test. Rise time, bandwidth, resistive and capacitive loading, delay and other limitations must be kept in mind.

Sometimes, the best probe is no probe at all. In some circumstances it is possible and preferable to connect critical breadboard points *directly* to the oscilloscope (see

Figure 18). This arrangement provides the highest possible grounding integrity, eliminates probe attenuation, and maintains bandwidth. In most cases this is mechanically inconvenient, and often the oscilloscope's electrical characteristics (particularly input capacitance) will not permit it. This is why oscilloscope probes were developed, and why so much effort has been put into their development (Reference 11 is excellent).

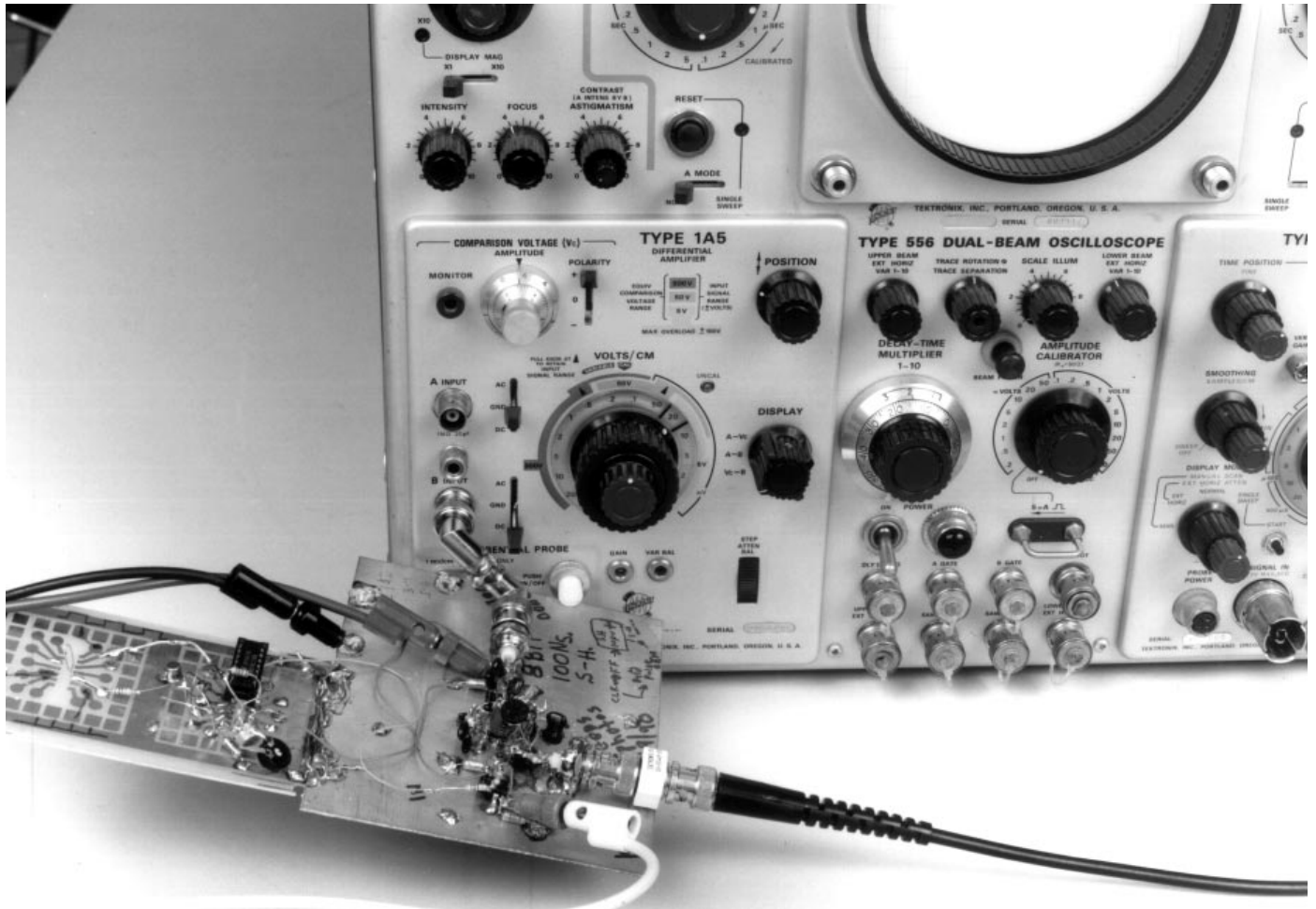
Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the point they are measuring. The most obvious is input resistance, but input capacitance usually dominates in a high speed measurement. Much time can be lost chasing circuit events that are actually due to improperly selected or applied probes. An 8pF probe looking at a 1kΩ source impedance forms an 8ns lag— longer than the LT1394's delay time! Pay particular attention to the probe's input capacitance. Standard 10MΩ, 10× probes typically have 8pF to 10pF of input capacitance, with 1× types being much higher. In general, 1× probes are not suitable for fast work because their bandwidth is limited to about 20MHz. Remember that all 10× probes cannot be used with all oscilloscopes; the probe's compensation range must match the oscilloscope's input capacitance. Low impedance probes (with 500Ω to 5kΩ resistance) designed for 50Ω inputs, usually have input capacitance of 1pF or 2pF. They are a very good choice if you can stand the low resistance. FET probes maintain high input resistance and keep capacitance at the 1pF level but have substantially more delay than passive probes. FET probes also have limitations on input common mode range which must be adhered to or serious measurement errors will result. Contrary to popular belief, FET probes *do not* have extremely high input resistance— some types are as low as 100kΩ.

Regardless of which type probe is selected, remember that they all have bandwidth and rise time restrictions. The displayed rise time on the oscilloscope is the vector sum of source, probe and 'scope rise times.

$$t_{\text{RISE}} = \sqrt{(t_{\text{RISE Source}})^2 + (t_{\text{RISE Probe}})^2 + (t_{\text{RISE Oscilloscope}})^2}$$

This equation warns that some rise time degradation must occur in a cascaded system. In particular, if probe and

Note 4: Almost no one believes any of this until they see it for themselves. I didn't. Photos of the network analyzer's display aren't included in the text because no one would believe them. I wouldn't.



AN72 F18

Figure 18. Sometimes the Best Probe Is No Probe. Direct Connection to the Oscilloscope Eliminates a 10× Probe's Attenuation and Possible Grounding Problems

oscilloscope are rated at the same rise time, the system response will be slower than either.

Current probes are useful and convenient.⁵ The passive transformer-based types are fast and have less delay than the Hall effect stabilized versions. The Hall types, however, respond at DC and low frequency and the transformer types typically roll off around 100Hz to 1kHz. Both types have saturation limitations, which, when exceeded, cause odd results on the CRT, confusing the unwary. The Tektronix type CT-1 current probe, although not nearly as versatile as the clip-on probes, bears mention. Although this is not a clip-on device, it may be the least electrically intrusive way of extracting wideband signal information. Rated at 1GHz bandwidth, it produces 5mV/mA output with only

0.6pF loading. Decay time constant of this AC current probe is $\approx 1\%/50\text{ns}$, resulting in a low frequency limit of 35kHz.

A very special probe is the differential probe. A differential probe may be thought of as two matched FET probes contained within a common probe housing. This probe literally brings the advantage of a differential input oscilloscope to the circuit board. The probes matched, active circuitry provides greatly improved high frequency common mode rejection over single-ended probing or even matched passive probes used with a differential amplifier. The resultant ability to reject common mode signals and ground noise at high frequency allows this probe to deliver exceptionally clean results when monitoring small, fast signals. Figure 19 shows a differential probe being used to verify the waveshape of a 2.5mV circuit input.

Note 5: A more thorough discussion of current probes is given in LTC Application Note 35, "Step-Down Switching Regulators." See Reference 2.

Application Note 72

When using different probes, remember that they all have different delay times, meaning that apparent timing errors will occur on the CRT. Know what the individual probe delays are and account for them in interpreting the CRT display.

By far the greatest source of error in probe use is grounding. Poor probe grounding can cause ripples and discontinuities in the observed waveform. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is parasitic inductance in the probe's ground connection. In most oscilloscope measurements this is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and

accessories designed to aid in making the lowest possible inductive connection to ground. Most of these attachments assume a ground plane is in use, which it should be. Always try to make the shortest possible connection to ground—anything longer than one inch may cause trouble. Sometimes it's difficult to determine if probe grounding is the cause of observed waveform aberrations. One good test is to disturb the grounding setup and see if changes occur. Nominally, touching the ground plane or jiggling probe ground connectors or wires should have no effect. If a ground strap wire is in use try changing its orientation or simply squeezing it together to change and minimize its loop area. *If any waveform change occurs while doing this the probe grounding is unacceptable, rendering the oscilloscope display unreliable.*

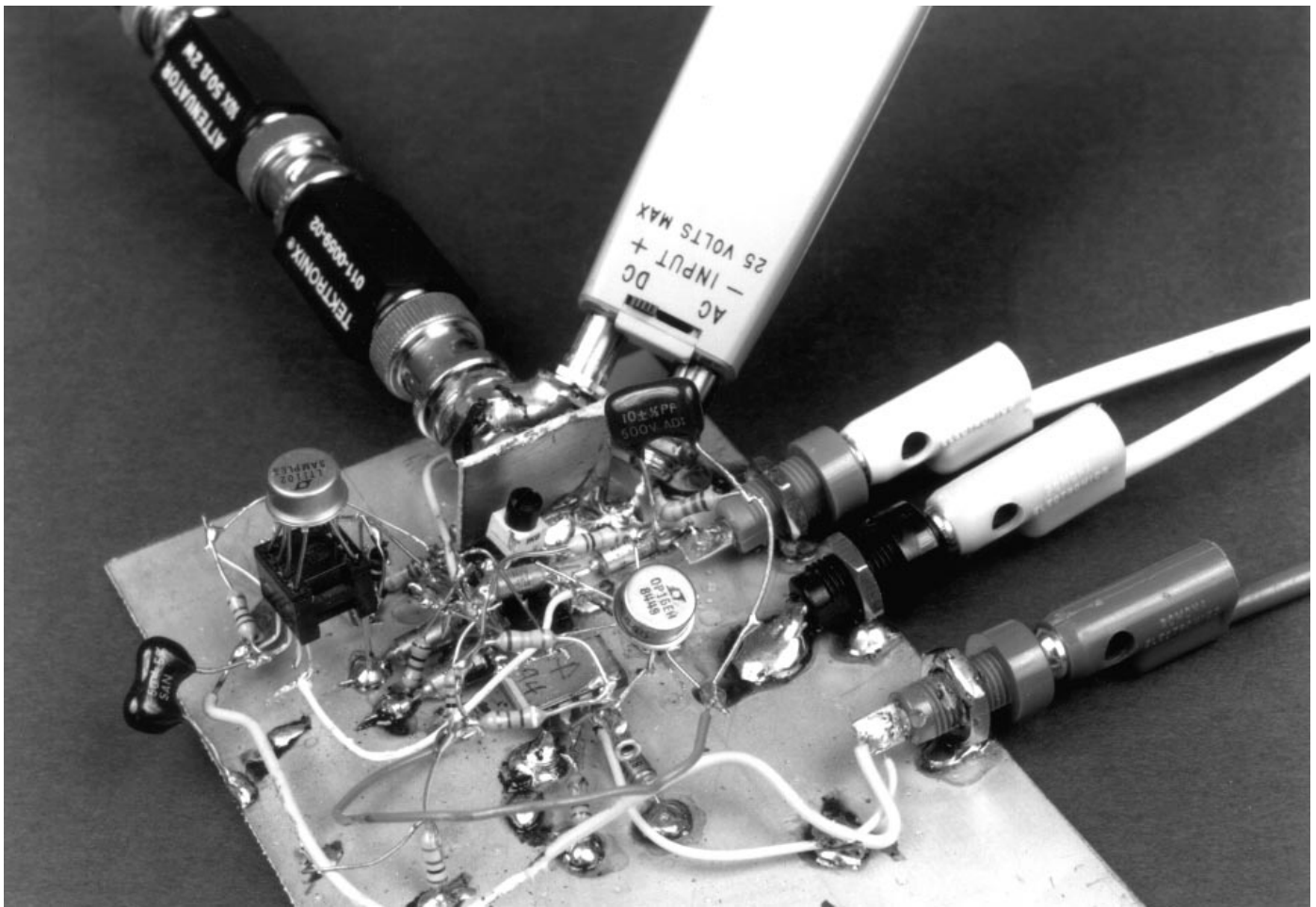


Figure 19. Using a Differential Probe to Verify the Integrity of a 2.5mV High Speed Input Pulse

AN72 F19

The simple network of Figure 20 shows just how easy it is for poorly chosen or used probes to cause bad results. A 9pF input capacitance probe with a 4-inch long ground strap monitors the output (Trace B, Figure 21). Although the input (Trace A) is clean, the output contains ringing. Using the same probe with a 1/4-inch spring tip ground connection accessory seemingly cleans up everything

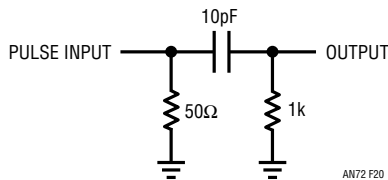


Figure 20. Probe Test Circuit

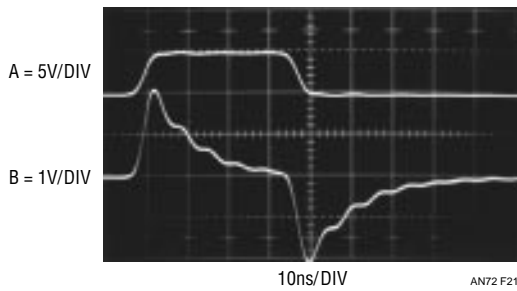


Figure 21. Test Circuit Output with 9pF Probe and 4-Inch Ground Strap

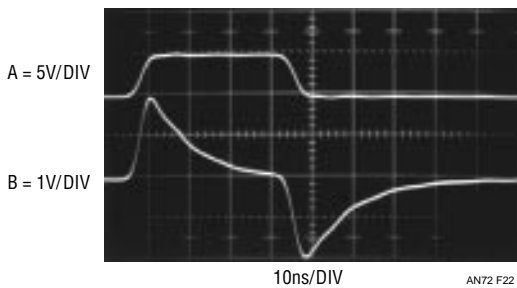


Figure 22. Test Circuit Output with 9pF Probe and 1/4-Inch Ground Strap

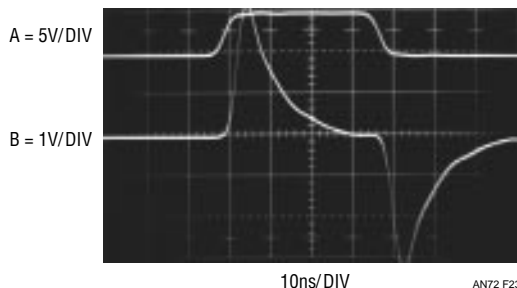


Figure 23. Test Circuit Output with FET Probe

(Figure 22). However, substituting a 1pF FET probe (Figure 23) reveals a 50% output amplitude error in Figure 22! The FET probe's low input capacitance allows a more accurate version of circuit action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5ns due to delay in its active circuitry. Hence, separate measurements with each probe are required to determine the output's amplitude and timing parameters. An alternative would employ two matched FET probes to minimize delay uncertainty.

A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can be used to introduce stray capacitance to a suspected circuit node while observing results on the CRT. Two fingers, lightly moistened, can be used to provide an experimental resistance path. Some high speed engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

Examples of some of the probes discussed, along with different forms of grounding implements, are shown in Figure 24. Probes A, B, E and F are standard types equipped with various forms of low impedance grounding attachments. The conventional ground lead used on G is more convenient to work with but will cause ringing and other effects at high frequencies, rendering it useless. H

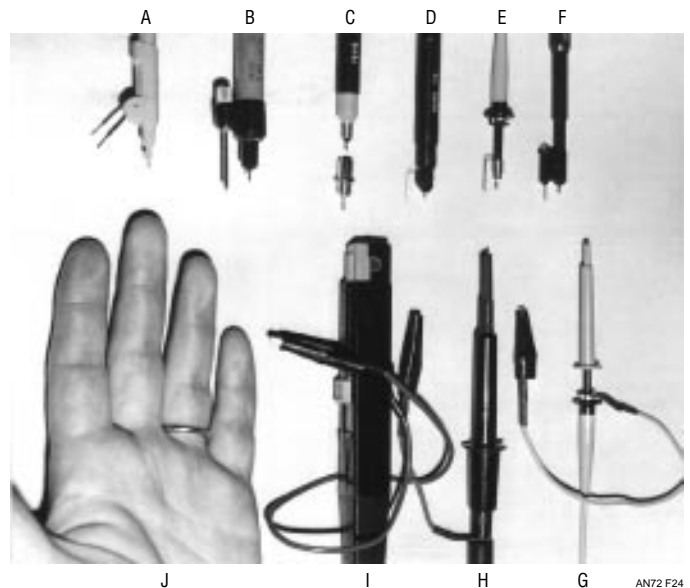


Figure 24. Various Probe-Ground Strap Configurations

Application Note 72

has a very short ground lead. This is better, but can still cause trouble at high speeds. D is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. C is a separated FET probe attenuator head. Such heads allow the probe to be used at higher voltage levels (e.g., $\pm 10\text{V}$ or $\pm 100\text{V}$). The miniature coaxial connector shown can be mounted on the circuit board and the probe mated with it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended. I is a current probe. A ground connection is not usually required. However, at high speeds the ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible. J is typical of the finger probes described in the text. Note the ground strap on the third finger.

The low inductance ground connectors shown are available from probe manufacturers and are always supplied with good quality, high frequency probes. Because most oscilloscope measurements do not require them, they invariably become lost. There is no substitute for these devices when they are needed, so it is prudent to take care of them. This is especially applicable to the ground strap on the finger probe.

About Oscilloscopes

The modern oscilloscope is one of the most remarkable instruments ever constructed. The protracted and intense development effort put toward these machines is perhaps equaled only by the fanaticism devoted to timekeeping.⁶ It is a tribute to oscilloscope designers that instruments manufactured over 30 years ago still suffice for over 90% of today's measurements. The oscilloscope-probe combination used in high speed work is the most important equipment decision the designer must make. Ideally, the oscilloscope should have at least 150MHz bandwidth, but slower instruments are acceptable if their limitations are well understood. Be certain of the characteristics of the probe-oscilloscope combination. Rise time, bandwidth, resistive and capacitive loading, delay, noise, channel-to-channel feedthrough, overdrive recovery, sweep nonlinearity, triggering, accuracy and other limitations must be kept in mind. High speed linear circuitry demands a great deal from test equipment and countless hours can be saved if the characteristics of the instruments used are

well known. Obscene amounts of time have been lost pursuing "circuit problems" that in reality are caused by misunderstood, misapplied or out-of-spec equipment. Intimate familiarity with your oscilloscope is invaluable in getting the best possible results with it. In fact, it is possible to use seemingly inadequate equipment to get good results if the equipment's limitations are well known and respected. All of the circuits in the Applications section involve rise times and delays well above the 100MHz to 200MHz region, but 90% of the development work was done with a 50MHz oscilloscope. Familiarity with equipment and thoughtful measurement technique permit useful measurements seemingly beyond instrument specifications. A 50MHz oscilloscope cannot track a 5ns rise time pulse, but it can measure a 2ns delay between two such events. Using such techniques, it is often possible to deduce the desired information. There are situations where no amount of cleverness will work and the right equipment (e.g., a faster oscilloscope) must be used. Sometimes, "sanity-checking" a limited bandwidth instrument with a higher bandwidth oscilloscope is all that is required. For high speed work, brute force bandwidth is indispensable when needed, and no amount of features or computational sophistication will substitute. Most high speed circuitry does not require more than two traces to get where you are going. Versatility and many channels are desirable, but if the budget is limited, spend for bandwidth!

Dramatic differences in displayed results are produced by probe-oscilloscope combinations of varying bandwidths. Figure 25 shows the output of a very fast pulse⁷ monitored with a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in). At this bandwidth the 10V amplitude appears clean, with just a small hint of ringing after the falling edge. The rise and fall times of 350ps are suspicious, as the sampling oscilloscope's rise time is also specified at 350ps.⁸

Note 6: In particular, the marine chronometer received ferocious and abundant amounts of attention. See References 4, 5 and 6. For an enjoyable stroll through the history of oscilloscope vertical amplifiers, see Reference 3.

Note 7: See Appendix B "Measuring Probe-Oscilloscope Response," for complete details on this pulse generator.

Note 8: This sequence of photos was shot in my home lab. I'm sorry, but 1GHz was the fastest 'scope in my house at the time. See Appendix B for a higher speed representation of this pulse.

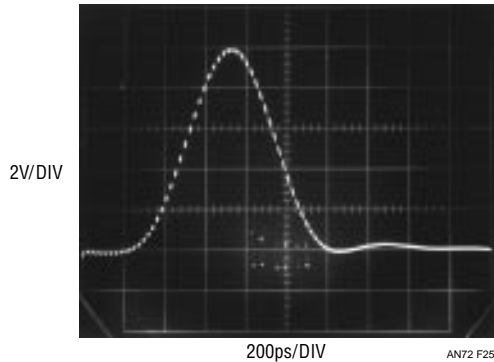


Figure 25. A 350ps Rise/Fall Time 10V Pulse Monitored on 1GHz Sampling Oscilloscope. Direct 50Ω Input Connection Is Used

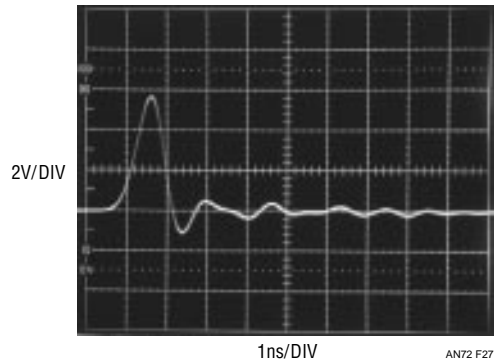


Figure 27. Test Pulse on the Same 350MHz Oscilloscope Using a 3GHz 10× Probe. Deliberate Poor Grounding Maintains Rippling Residue

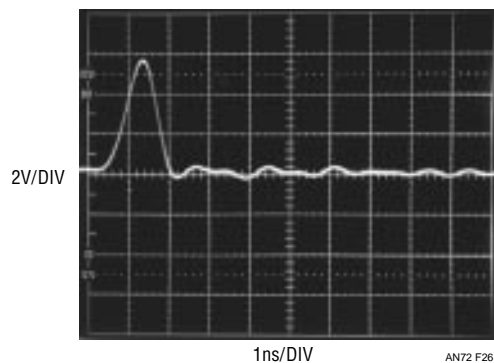


Figure 26. The Test Pulse Appears Smaller and Slower on a 350MHz Instrument ($t_{RISE} = 1ns$). Deliberate Poor Grounding Creates Rippling After the Pulse Falls. Direct 50Ω Connection Is Used

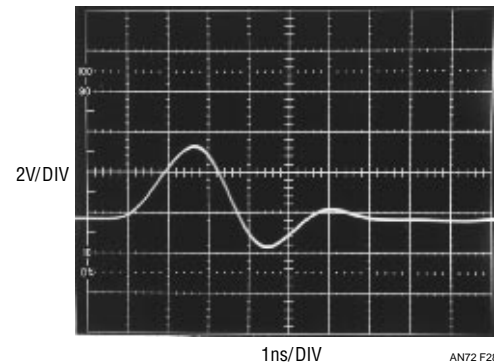


Figure 28. Test Pulse Measures Only 3V High on a 250MHz 'Scope with Significant Waveform Distortion. 290MHz 10× Probe Used

Figure 26 shows the same pulse observed on a 350MHz instrument with a direct connection to the input (Tektronix 485/50Ω input). Indicated rise time balloons to 1ns, while displayed amplitude shrinks to 6V, reflecting this instrument's lesser bandwidth. To underscore earlier discussion, poor grounding technique (1 1/2" of ground lead to the ground plane) created the prolonged rippling after the pulse fall.

Figure 27 shows the same 350MHz (50Ω input) oscilloscope with a 3GHz 10× probe (Tektronix P6056). Displayed results are nearly identical, as the probe's high bandwidth contributes no degradation. Again, deliberate poor grounding causes overshoot and rippling on the pulse fall.

Figure 28 equips the same oscilloscope with a 10× probe specified at 290MHz bandwidth (Tektronix P6047). Additionally, the oscilloscope has been switched to its 1MΩ input mode, reducing bandwidth to a specified 250MHz. Amplitude degrades to less than 4V and edge times

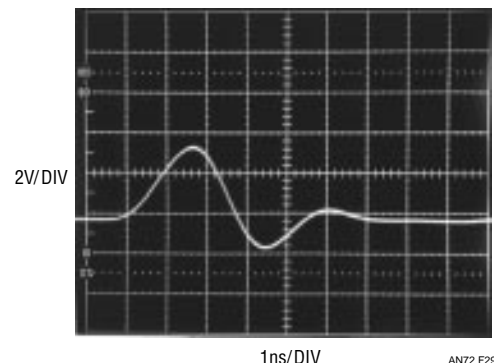


Figure 29. Test Pulse Measures Under 2V High Using 250MHz 'Scope and a 100MHz Probe

similarly increase. The deliberate poor grounding contributes the undershoot and underdamped recovery on pulse fall.

In Figure 29, a 100MHz 10× probe (Hewlett-Packard Model 10040A) has been substituted for the 290MHz unit. The oscilloscope and its setup remain the same. Ampli-

Application Note 72

tude shrinks below 2V, with commensurate rise and fall times. Cleaned-up grounding eliminates aberrations.

A Tektronix 454A (150MHz) produced Figure 30's trace. The pulse generator was directly connected to the input. Displayed amplitude is about 2V, with appropriate 2ns edges. Finally, a 50MHz instrument (Tektronix 556 with 1A4 plug-in) just barely grunts in response to the pulse (Figure 31). Indicated amplitude is 0.5V, with edges reading about 7ns. That's a long way from the 10V and 350ps that's really there!

A final oscilloscope characteristic is overload performance. It is often desirable to view a small amplitude portion of a large waveform. In many cases the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overload before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overload varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100× overload at 0.005V/division may be very different than at 0.1V/division. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overload must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity which eliminates all off-screen activity. Figure 32 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure 33) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure 34, gain has been further increased and all the features of Figure 33 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see.

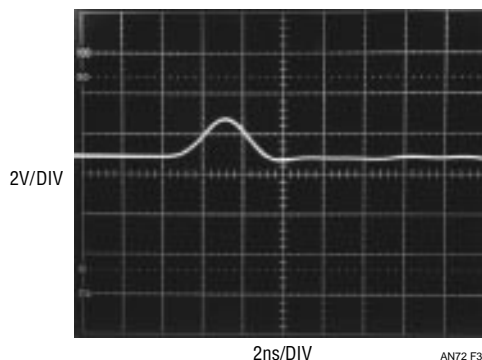


Figure 30. 150MHz Oscilloscope ($t_{RISE} = 2.4ns$) with Direct Connection Responds to the Test Pulse

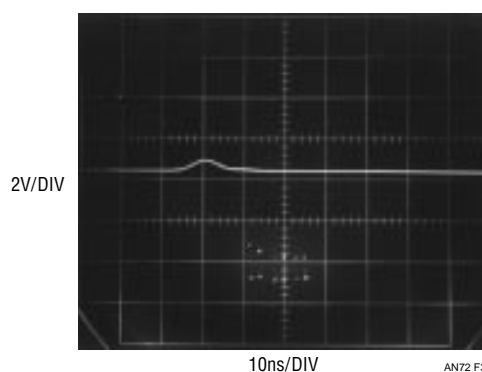


Figure 31. A 50MHz Instrument Barely Grunts. 10V, 350ps Test Pulse Measures Only 0.5V High with 7ns Rise and Fall Times!

No new waveform characteristics are observed. Figure 35 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure 34. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure 36 the gain remains the same, but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point, which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure 37). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

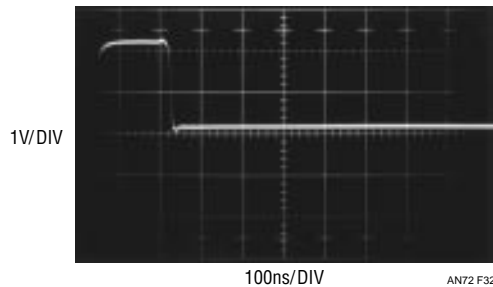


Figure 32

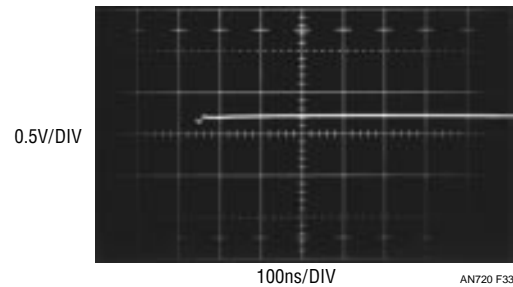


Figure 33

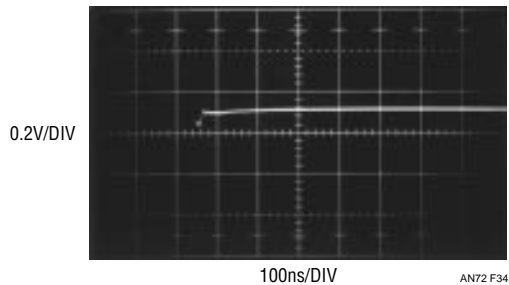


Figure 34

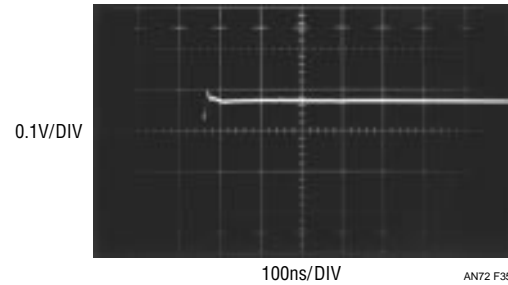


Figure 35

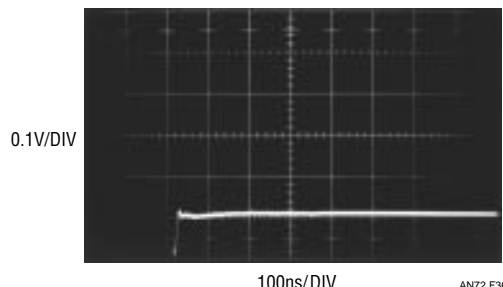


Figure 36

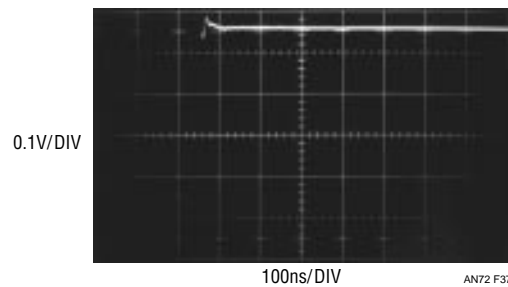


Figure 37

Figures 32 to 37: The Overdrive Limit Is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

Differential plug-ins can address some of the issues associated with excessive overdrive, although they cannot solve all problems. Two differential plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7, 1A7A and 7A22 feature 10 μ V sensitivity, although bandwidth is limited to 1MHz. The units also have selectable highpass and lowpass filters and good high frequency common mode rejection. Tektronix type 1A5, W and 7A13 are differential comparators. They have calibrated DC nulling (slide back) sources, allowing observation of small, slowly moving events on top of common mode DC or fast events riding on a waveform.

A special case is the sampling oscilloscope. By nature of its operation, a sampling 'scope in proper working order

is inherently immune to input overload, providing essentially instantaneous recovery between samples. See Reference 8 for additional details.

The best approach to measuring small portions of large waveforms, however, is to eliminate the large signal swing seen by the oscilloscope. Reference 17 discusses applicable techniques in detail.

In summary, although the oscilloscope provides remarkable capability, its limitations must be well understood when interpreting results.⁹

Note 9: Additional discourse on oscilloscopes will be found in References 1 and 7 through 10.

Application Note 72

About Ground Planes

Many times in high frequency circuit layout, the term “ground plane” is used, most often as a mystical and ill-defined cure to spurious circuit operation. In fact, there is little mystery to the usefulness and operation of ground planes, and like many phenomena, their fundamental operating principle is surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a wire carrying current (Figure 38) surrounded by radii of magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the wire's current. To compute the wire's inductance requires integrating the field over the wire's length and the total radial area of the field. This implies integrating on the radius from $R = R_W$ to infinity, a very large number. However, consider the case where we have two wires in space carrying the same current in either direction (Figure 39). The fields produced cancel.

In this case, the inductance is much smaller than in the simple wire case and can be made arbitrarily smaller by

reducing the distance between the two wires. This reduction of inductance between current carrying conductors is the underlying reason for ground planes. In a normal circuit, the current path from the signal source through its conductor and back to ground includes a large loop area. This produces a large inductance for this conductor which can cause ringing due to LRC effects. It is worth noting that 10nH at 100MHz has an impedance of 6Ω. At 10mA a 60mV drop results.

A ground plane provides a return path directly under the signal carrying conductor through which return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents will always flow through the return path of lowest impedance. In a properly designed ground plane, this path is directly under the signal conductor. In a practical circuit, it is desirable to use one whole side of the PC card (usually the component side for wave solder considerations) as a ground plane and run the signal conductors on the other side. This will give a low inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to AC skin effect (AC currents travel along a conductor's surface). Additionally, they aid the circuit's high frequency stability by referring stray capacitances to ground.

Some practical hints for ground planes are:

1. Utilize a ground plane over as much area as possible on the component side of the board, especially under traces that operate at high frequency.
2. Mount components that conduct substantial fast rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
3. Where common ground potential is important (i.e., at comparator inputs), try to single point the critical components into the ground plane to avoid voltage drops.
4. Keep trace length short. Inductance varies directly with length and no ground plane will achieve perfect cancellation.

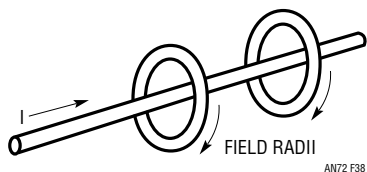


Figure 38. Single Wire Case

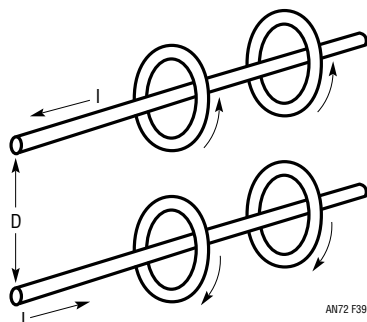


Figure 39. Two Wire Case

About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation were used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure 40. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values so they can absorb long transients, necessitating electrolytic types which have large series R and L.

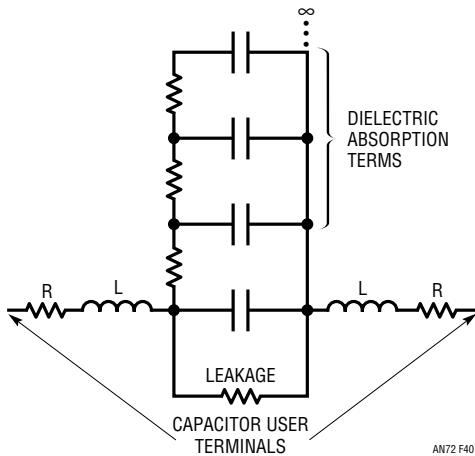


Figure 40. Parasitic Terms of a Capacitor

Different types of electrolytics and electrolytic-nonpolar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure 41) and accompanying photos are useful. The photos show the response of five bypassing methods to the transient generated by the test circuit. Figure 42 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure 43 uses an aluminum 10μF electrolytic to considerably cut the

disturbance, but there is still plenty of potential trouble. A tantalum 10μF unit offers cleaner response in Figure 44 and the 10μF aluminum combined with a 0.01μF ceramic type is even better in Figure 45. Combining electrolytics with nonpolarized capacitors is a popular way to get good

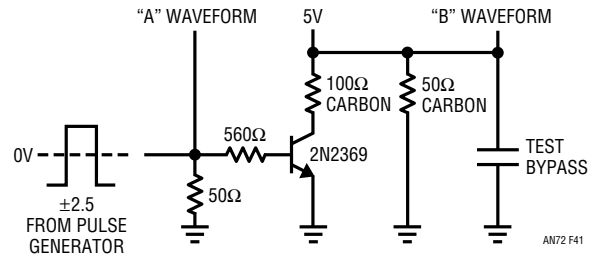


Figure 41. Bypass Capacitor Test Circuit

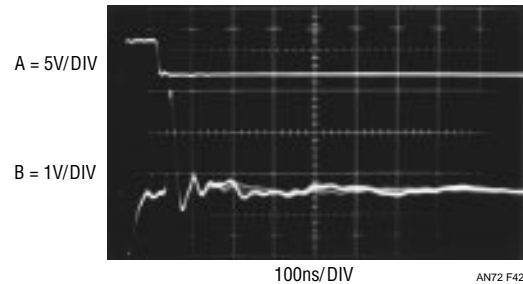


Figure 42. Response of Unbypassed Line

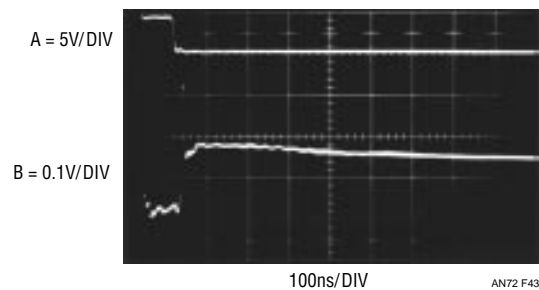


Figure 43. Response of 10μF Aluminum Capacitor

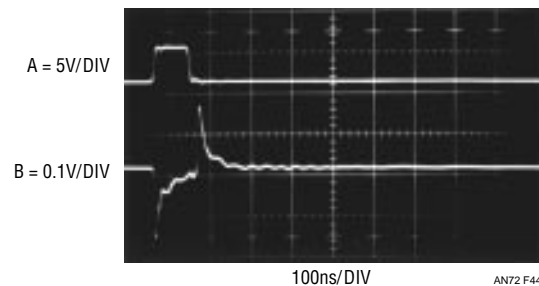


Figure 44. Response of 10μF Tantalum Capacitor

Application Note 72

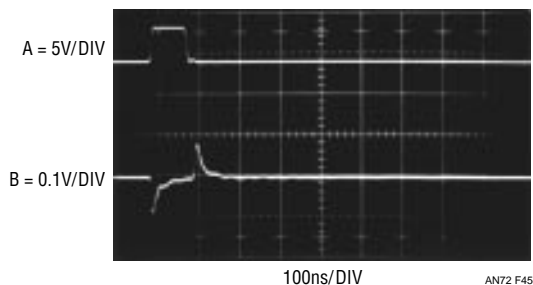


Figure 45. Response of 10 μ F Aluminum Paralleled by 0.01 μ F Ceramic

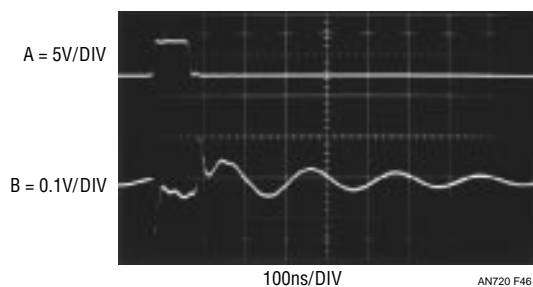


Figure 46. Some Paralleled Combinations Can Ring. Try Before Specifying!

response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in Figure 46. Caveat!

Breadboarding Techniques

The breadboard is both the designer's playground and proving ground. It is there that Reality resides, and paper (or computer) designs meet their ruler. More than anything else, breadboarding is an iterative procedure, an odd amalgam of experience guiding an innocent, ignorant, explorative spirit. A key is to be willing to try things out, sometimes for not very good reasons. Invent problems and solutions, guess carefully and wildly, throw rocks and see what comes loose. Invent and design experiments, and follow them wherever they lead. Reticence to try things is probably the number one cause of breadboards that "don't work."¹⁰ Implementing the above approach to life begins with the physical construction methods used to build the breadboard.

A high speed breadboard must start with a ground plane. Additionally, bypassing, component layout and connec-

tions should be consistent with high speed operations. Because of these considerations there is a common misconception that breadboarding high speed circuits is time consuming and difficult. This is simply not true. For high speed circuits of moderate complexity a complete and electrically correct breadboard can be assembled in 10 minutes if all necessary components are on hand. The key to rapid breadboarding is to identify critical circuit nodes and design the layout to suit them. This permits most of the breadboard's construction to be fairly sloppy, saving time and effort. Additionally, use all degrees of freedom in making connections and mounting components. Don't be bashful about bending IC pins to suit desired low capacitance connections, or air wiring components to achieve rapid or electrically optimum layout. Save time by using components, such as bypass capacitors, as mechanical supports for other components, such as amplifiers. It is true that eventual printed circuit construction is required, but when initially breadboarding forget about PC and production constraints. Later, when the circuit works, and is well understood, PC adaptations can be taken care of.¹¹

Once the breadboard seems to work, it's useful to begin thinking about PC layout and component choice for production. Experiment with the existing layout to determine just how sensitive nominally critical points are. Add controlled parasitic terms (e.g., resistors, capacitors and physical layout changes) to test for sensitivity. Gentle touching of suspect points with a finger can yield preliminary indication of sensitivity, giving clues that can be quite valuable.

In conclusion, when breadboarding, design the breadboard to be quick and easy to build, work with and modify. Observe the circuit and listen to what it is telling you before trying to get it to some desired state. Finally, don't hesitate to try just about anything; that's what the breadboard is for. Almost anything you do will cause some result—whether it's good or bad is almost irrelevant. Anything you do that enhances your ability to correlate events occurring on the breadboard can only be beneficial.

Note 10: A much more eloquently stated version of this approach is found in Reference 12.

Note 11: See Reference 17 for a pictorially enhanced version of this discussion.

This completes the tutorial section. Hopefully, several notions have been imparted. First, in any measurement situation, test equipment characteristics are an integral part of the circuit. At high speed and high precision this is particularly the case. As such, it is imperative to know your equipment and how it works. There is no substitute for intimate familiarity with your tool's capabilities and limitations.¹²

In general, use equipment you trust and measurement techniques you understand. Keep asking questions and don't be satisfied until everything you see on the oscilloscope is accounted for and makes sense.

The LT1394, combined with the precautionary notes listed above, permits fast linear circuit functions that are difficult or impractical using other approaches. Some of the applications presented in the following section represent the state-of-the-art for a particular circuit function. Others show simplified and/or improved ways to implement standard functions by utilizing the comparator's easily accessed speed. All have been carefully (and painfully) worked out and should serve as good idea sources for potential users of the device. Have fun. I did.

APPLICATIONS

Crystal Oscillators

Figure 47's circuits are crystal oscillators. In the circuit (a) the resistors at the LT1394's positive input set a DC bias point. The 2k-0.068 μ F path sets up phase shifted feedback and the circuit looks like a wideband unity-gain follower at DC. The crystal's path provides resonant positive feedback and stable oscillation occurs. The circuit (b) is similar, but supports oscillation frequencies to 30MHz. Above 10MHz, AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, ensuring proper operation.

Switchable Output Crystal Oscillator

Figure 48 permits crystals to be electronically switched by logic commands. This circuit is similar to the previous examples, except that oscillation is only possible when one of the logic inputs is biased high.

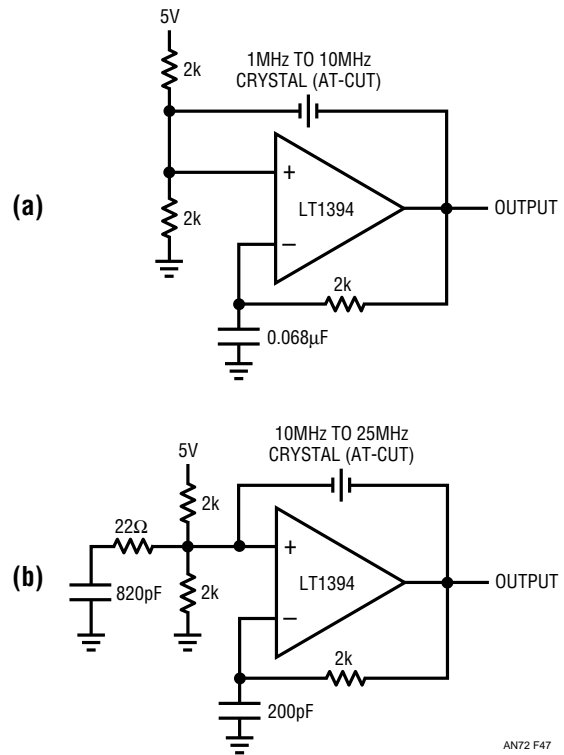


Figure 47. Crystal Oscillators for Outputs to 30MHz. Circuit (b)'s Damper Network Suppresses Overtone Crystal's Harmonic Modes

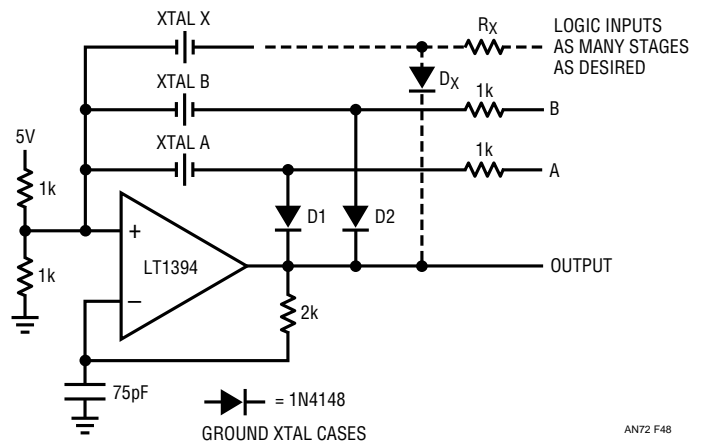


Figure 48. Switchable Output Crystal Oscillator. Biasing A or B High Places Associated Crystal in Feedback Path. Additional Crystal Branches Are Permissible

Note 12: Further exposition and *kvetching* on this point is given in Reference 13.

Application Note 72

Temperature-Compensated Crystal Oscillator (TXCO)

Figure 49 is a temperature-compensated crystal oscillator (TXCO). This circuit reduces oscillator temperature drift by inserting a temperature-dependent compensatory correction into the crystal's frequency trimming network. This open-loop correction technique relies on matching the oscillator's frequency versus temperature characteristic, which is quite repeatable.

The LT1394 and associated components form the crystal oscillator, operating similarly to Figure 47's examples. The LM134, a temperature-dependent current source, biases A1. A1 takes gain referred to the LM134's output and the negative offset supplied via the 470kΩ-LT1004 reference path. Note that the LT1004's negative voltage bias is bootstrapped from the oscillator's output, maintaining single supply operation. This arrangement delivers temperature-dependent bias to the varactor diode, causing a scaled variation in the crystal's resonance versus ambient temperature. The varactor's bias-dependent capacitance shift pulls crystal frequency to complement the circuit's temperature drift. The simple first order fit provided by the compensation is very effective. Figure 50 shows results.

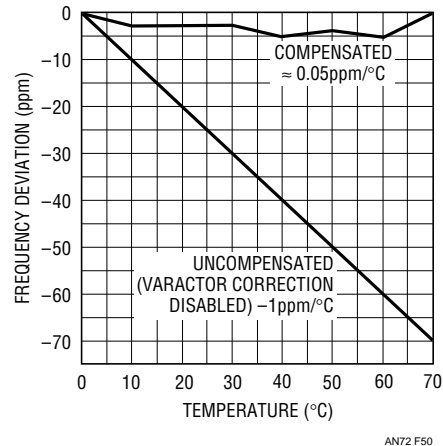


Figure 50. Figure 49's Compensated vs Uncompensated Temperature Dependence. First Order Compensation Reduces Oscillator Drift to 0.05ppm/°C

The -70ppm frequency shift over 0°C to 70°C is corrected within a few ppm. The "FREQ SET" trim also biases the varactor, allowing accurate output frequency setting. It is worth noting that better compensation is possible by including higher order terms in the temperature-to-voltage conversion.

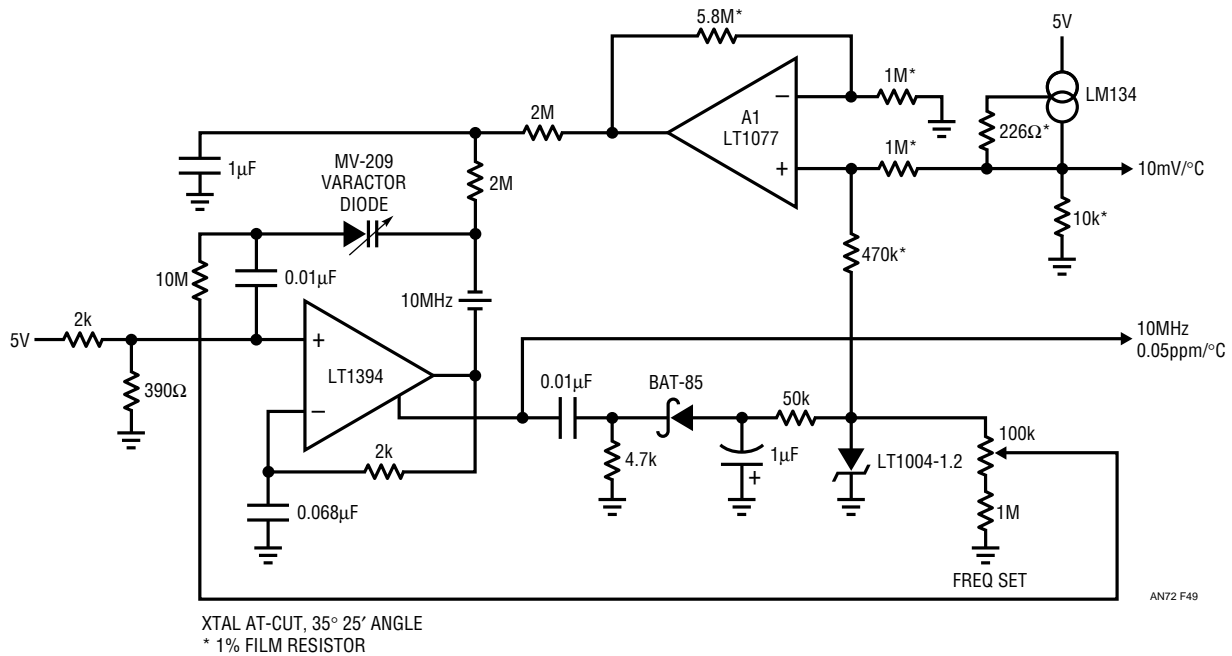


Figure 49. Temperature-Compensated 10MHz Crystal Oscillator. Temperature-Dependent Varactor Bias Reduces Drift by 20:1

Voltage-Controlled Crystal Oscillator (VCXO)

Figure 51, also a variant of the basic crystal oscillator, permits voltage tuning the output frequency. Such voltage-controlled crystal oscillators (VCXO) are often employed where slight variation of a stable carrier is required. This example is specifically intended to provide a $4 \times$ NTSC sub-carrier tunable oscillator suitable for phase locking.

The LT1394 is set up as a crystal oscillator, operating similarly to Figure 47(a). The varactor diode is biased from the tuning input. The tuning network is arranged so a 0V to 5V drive provides a reasonably symmetric, broad tuning range around the 14.31818MHz center frequency. The indicated selected capacitor sets tuning bandwidth. It should be picked to complement loop response in phase locking applications. Figure 52 is a plot of tuning input voltage versus frequency deviation. Tuning deviation from the $4 \times$ NTSC 14.31818MHz center frequency exceeds ± 240 ppm for a 0V to 5V input.

Voltage-Tunable Clock Skew Generator

It is sometimes necessary to generate pairs of identical clock signals that are phase skewed in time. Further, it is desirable to be able to set the amount of time skew via a tuning voltage. Figure 53's circuit does this by utilizing

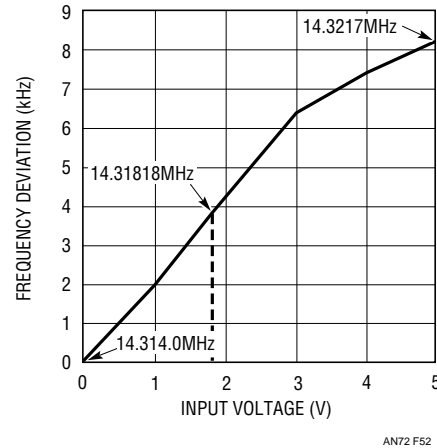


Figure 52. Control Voltage vs Output Frequency for Figure 51. Tuning Deviation from Center Frequency Exceeds ± 240 ppm

comparators to digitize phase information from a varactor-tuned time domain bridge. A 0V to 2V control signal provides $\approx \pm 10$ ns of output skew. The input is applied to the CMOS inverters, which deliver noninverting drive to the bridge network (Trace A, Figure 54). The bridge, essentially composed of two RC sections, responds in ramp fashion at both of its outputs (Trace B is "fixed" output, Trace C is "skewed" output). The "skewed" bridge half's capacitance is tuned by a varactor diode, biased

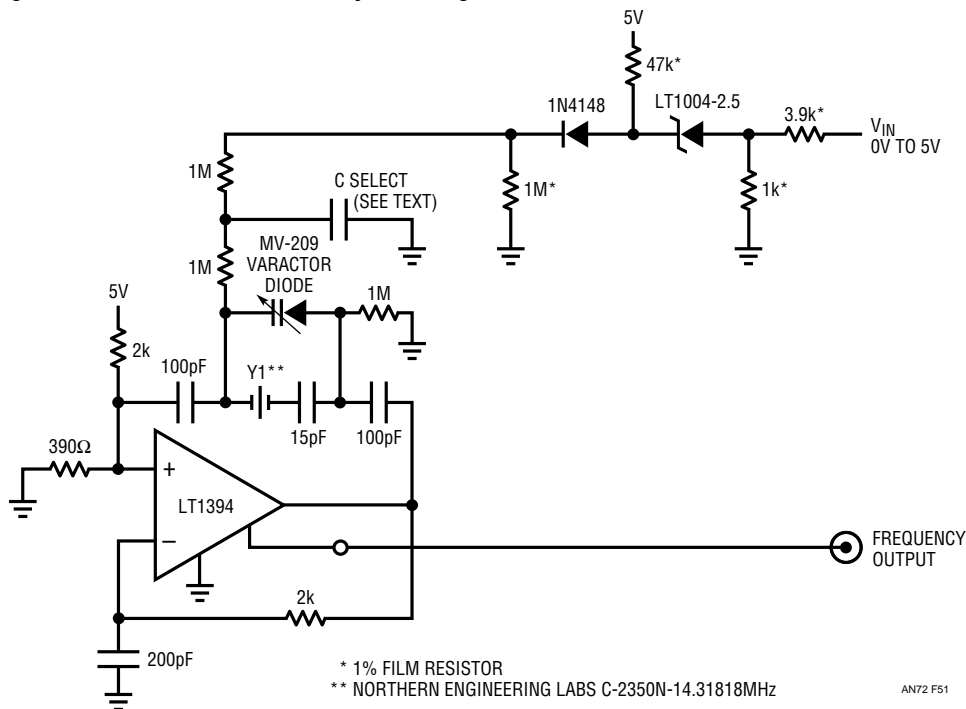


Figure 51. A $4 \times$ NTSC Sub-Carrier Voltage-Tunable Crystal Oscillator. Tuning Range and Bandwidth Accommodate Variety of Phase Locked Loops

Application Note 72

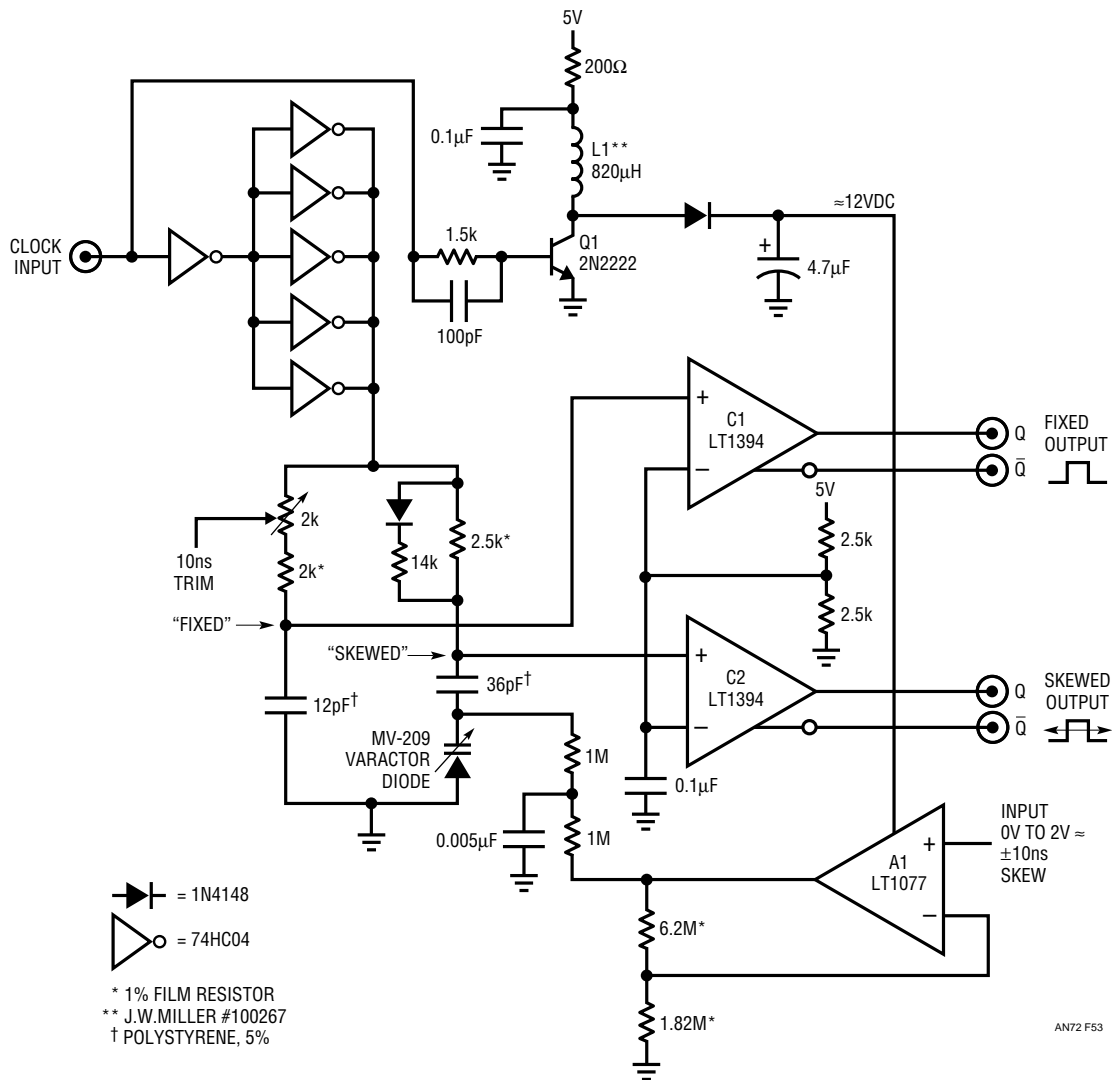


Figure 53. Comparators Extract Phase Difference from Varactor-Tuned Bridge, Permitting Controllable Clock Skew

from A1, and hence the control input. The comparators, referenced to 1/2 supply voltage, trigger (Traces D and E are C1 and C2 output, respectively) when their positive inputs exceed the reference point. The time skew of this response is determined by imbalance in the bridge's RC time constants, which is controlled via the voltage input. The diode-resistor network across the 2.5k bridge resistor compensates for ramp-induced variation of varactor capacitance, enhancing control symmetry. Q1 and associated components form a simple voltage boost stage, enabling A1 to supply adequate varactor bias. The bridge's ratiometric operation permits almost 100:1 power supply rejection ratio over a $4.5V_{IN}$ to $5.5V_{IN}$ range. To trim this circuit, put in 2V and adjust the 2k potentiometer for 10ns

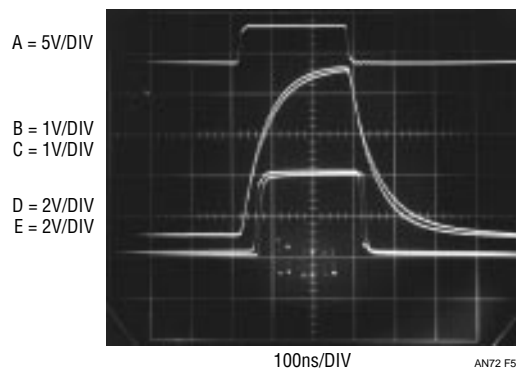


Figure 54. Clocked (Trace A), Varactor-Tuned Bridge Has Phase Shifted Outputs (Traces B and C). Comparators (Traces D and E) Digitize Information, Providing Output

skew in the outputs. Over a 0V to 2V range, output skew will continuously vary from -10ns through 0, to 10ns.

Simple 10MHz Voltage-to-Frequency Converter

Figure 55 is a voltage-to-frequency converter. A 0V to 2.5V input produces a 0Hz to 10MHz output with 40dB of dynamic range, 1% linearity and 400ppm/°C gain drift. Power supply rejection is 0.5% for 4.75V to 5.25V supply excursions.

To understand circuit operation, assume C1's positive input is slightly below its negative input. The input voltage causes a positive-going ramp at C1's positive input (Trace A, Figure 56). C1's output is low, biasing the CMOS inverters high. This allows current flow from diode Q1's collector, through the CMOS inverter supply pin to the 10pF capacitor. The 4.7μF capacitor provides high frequency bypass, maintaining low impedance at Q1's collector. Diode connected Q3 provides a path to ground. The voltage the 10pF capacitor charges to is a function of Q1's collector potential and Q3's drop. When the ramp at C1's positive input goes high enough, C1's output goes high and the paralleled inverters switch low (Trace B). This action pulls current from C1's positive input capacitor via the Q4-10pF route (Trace D). This current removal resets

C1's positive input ramp to a potential slightly below ground, forcing C1's output low and the paralleled inverters high. The 8pF capacitor at C1's inverting output furnishes AC positive feedback to C1's negative input (Trace C). This ensures that C1's output remains high long enough for a complete discharge of the 10pF unit. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 8pF capacitor's feedback decays, C1 again switches high and the entire cycle repeats. The oscillation frequency depends directly on the input-derived current.

The LT1004 is the circuit's voltage reference, with Q1 and Q2 temperature compensating Q3 and Q4.

Start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high, causing the paralleled inverters to go low. After a time determined by the 1M-1000pF RC the associated lone inverter goes high. This lifts C1's negative input and grounds the positive input with Q5, initiating normal circuit action.

To calibrate this circuit, apply 2.5V and adjust the 10k potentiometer for a 10MHz output.

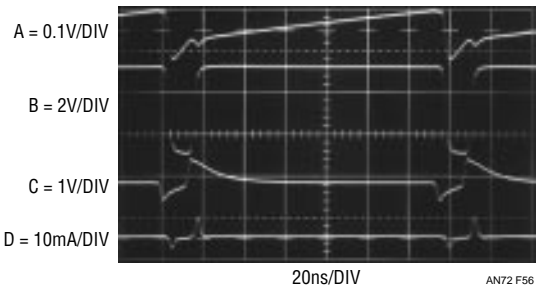
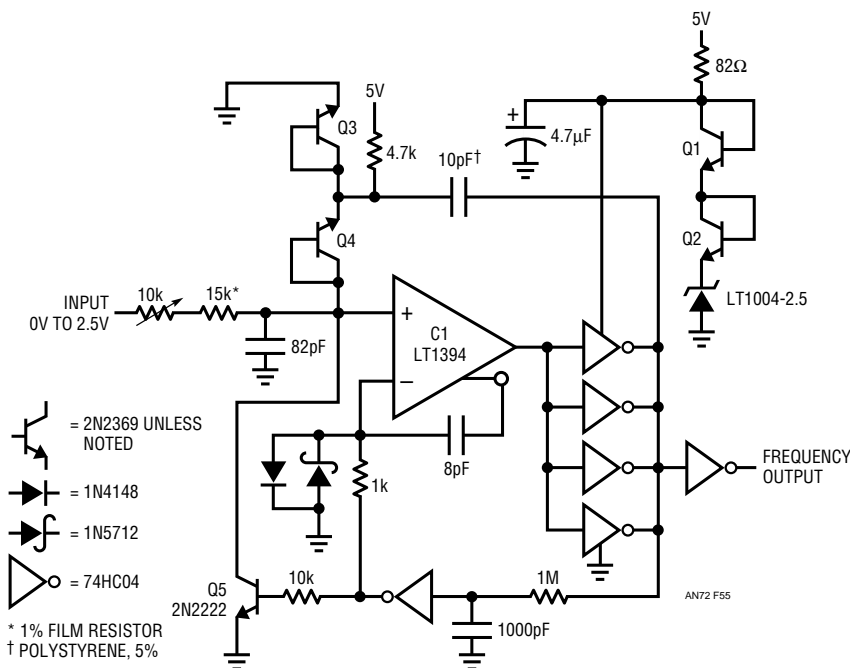


Figure 56. Waveforms for the 10MHz Voltage-to-Frequency Converter. Charge Pump-Based Feedback Provides Linearity and Fast Response to Input

Figure 55. Simple Charge Pump-Based 10MHz Voltage-to-Frequency Converter Has 40dB Dynamic Range, Operates from 5V Supply

Application Note 72

Precision 1Hz to 10MHz Voltage-to-Frequency Converter

Significant performance improvements over the previous circuit are achievable if increased complexity is tolerable. The LT1394 and the LT1122 high speed FET amplifier combine to form a high speed V/F converter in Figure 57. A variety of circuit techniques are used to achieve a 1Hz to 10MHz output. Overrange to 12MHz ($V_{IN} = 12V$) is provided. This circuit has a wider dynamic range (140dB or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is ten times faster than currently available monolithic V/Fs. The theory of operation is based on the identity $Q = CV$.

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse

generator runs at a frequency that permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

0.05 $\mu V/^\circ C$ offset drift performance is obtained by stabilizing A1 with A2, a chopper-stabilized op amp. A2 measures the DC value of the negative input, compares it to ground, and forces the positive input to maintain offset balance in A1. Note that A2 is configured as an integrator and cannot see high frequency signals. It functions only at DC and low frequency.

A1 is arranged as an integrator with a 68pF feedback capacitor. When a positive voltage is applied to the input, A1's output integrates in a negative direction (Trace A, Figure 58). During this period, C1's inverting output is low. The paralleled HCMOS inverters form a reference voltage switch. The reference voltage is established by the LM134 current source driven LT1034's and the Q3-Q4 combination. Additionally, a small input voltage-related term is summed into the reference, improving overall circuit linearity. A3-A4 provides low drift buffering, presenting a

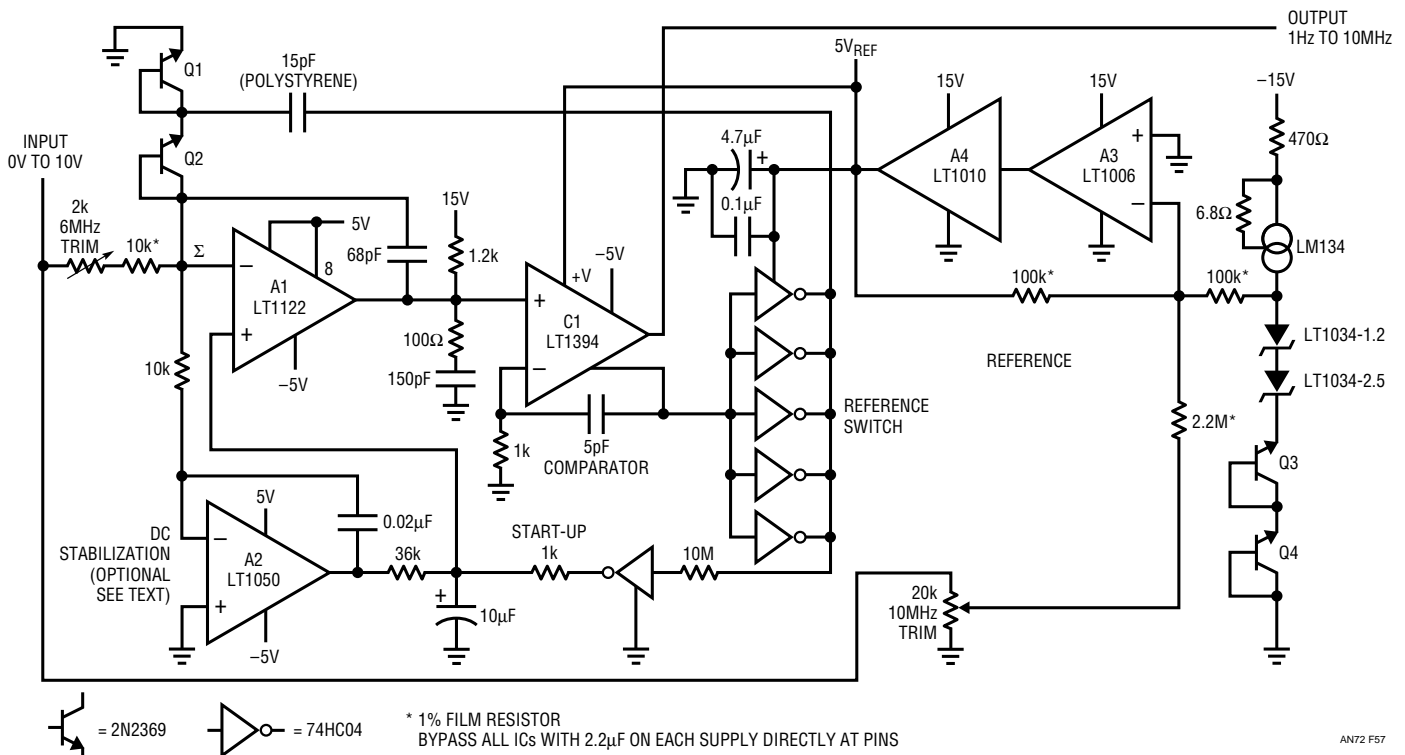


Figure 57. A Very High Performance 1Hz to 10MHz Voltage-to-Frequency Converter. Linearity is 0.03% with 50ppm/ $^\circ C$ Drift

low impedance reference to the paralleled inverter's supply pin. The HCMOS outputs give low resistance, essentially errorless switching. The reference switch's output charges the 15pF capacitor via Q1's path.

When A1's output crosses zero, C1's inverting output goes high and the reference switch (Trace B) goes to ground. This causes the 15pF unit to dispense charge into the summing node via Q2's V_{BE} . The amount of charge dispensed is a direct function of the voltage the 15pF unit was charged to ($Q = CV$). Q1 and Q2 are temperature compensated by Q3 and Q4 in the reference string. The current through the 15pF unit (Trace C) reflects the charge pumping action. The removal of current from A1's summing junction (Trace D) causes the junction to be driven very quickly negative. The initial negative-going 15ns transient at A1's output is due to amplifier delay. The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (Trace A) slew limits as it attempts to regain control of the summing node. The class A 1.2k Ω pull-up and the RC damper at A1's output minimize erroneous output movement, enhancing this slew recovery. The amount of time the reference switch remains at ground depends on how long it takes A1 to recover and the 5pF-1000 Ω time constant at C1. This 60ns interval is long enough for the 15pF unit to fully discharge. After this, C1 changes state, the reference switch swings positive, the capacitor is recharged and the entire cycle repeats. The frequency at which this oscillation occurs is directly related to the voltage input-derived current into the summing junction. Any input current will require a corresponding oscillation frequency to hold the summing point at an average value of 0V.

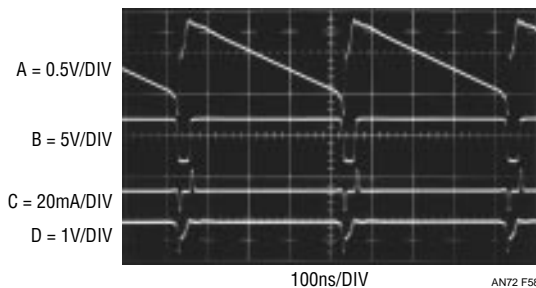


Figure 58. Precision 10MHz Voltage-to-Frequency's Operating Waveforms. LT1122 Integrator Is Completely Reset in 60ns

Maintaining this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to achieving 10MHz full-scale operating frequency is the ability to transmit information around the loop as quickly as possible. The discharge-reset sequence is particularly critical and is detailed in Figure 59. Trace A is the A1 integrator output. Its ramp output crosses 0V at the first left vertical graticule division. A few nanoseconds later, C1's inverting output begins to rise (Trace B), switching the reference switch to ground (Trace C). The reference switch begins to head towards ground about 16ns after A1's output crosses 0V. 2ns later, the summing point (Trace D) begins to go negative as current is pulled from it through the 15pF capacitor. At 25ns, C1's inverting output is fully up, the reference switch is at ground, and the summing point has been pulled to its negative extreme. Now, A1 begins to take control. Its output (Trace A) slews rapidly in the positive direction, restoring the summing point. At 60ns, A1 is in control of the summing node and the integration ramp begins again.

Start-up and overdrive conditions could force A1's output to go to the negative rail and stay there. The AC-coupled nature of the charge dispensing loop can preclude normal operation and the circuit may latch. The remaining HCMOS inverter provides a watchdog function for this condition. If A1's output remains negative the reference switch tries to stay at ground. The remaining inverter goes high, lifting A1's positive input. This causes A1's output to slew positive, initiating normal circuit action. The 1k-10 μ F combination and the 10M-inverter input capacitance limit start-up loop bandwidth, preventing unwanted outputs.

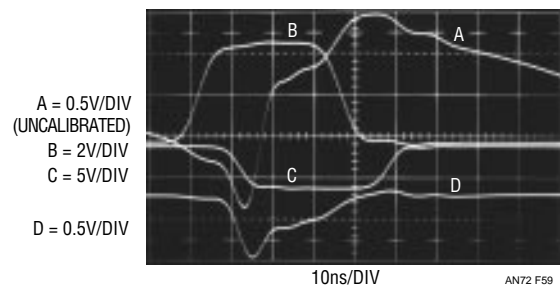


Figure 59. Detail of 60ns Reset Sequence (Whoosh!)

Application Note 72

The LM134 current source driving the reference string has a built in 0.33%/°C thermal coefficient, causing slight voltage modulation in the Q3-Q4 pair over temperature. This small change ($\approx 120\text{ppm}/^\circ\text{C}$) opposes the $-120\text{ppm}/^\circ\text{C}$ drift in the 15pF polystyrene capacitor, aiding overall circuit tempo.

To trim this circuit, apply exactly 6V at the input and adjust the 2k Ω potentiometer for 6.000MHz output. Next, put in exactly 10V and trim the 20k unit for 10.000MHz output. Repeat these adjustments until both points are fixed. A2's low drift eliminates a zero adjustment. If operation below 600Hz is not required, A2 and its associated components may be deleted.

Linearity of this circuit is 0.03% with full-scale drift of 50ppm/°C. Zero point error, controlled by A2, is 0.05Hz/°C.

Fast, High Impedance, Variable Threshold Trigger

A frequent requirement in instrumentation is a fast trigger with a variable threshold. Often, a high impedance input is also required. Figure 60 meets these requirements. Comparator C1 is the basic trigger, with threshold voltage set at its negative input. Source follower Q1 provides high impedance with about 2pF input capacitance and 50pA bias current. Normally, Q1's source bias point would be uncertain and drifts, but stabilization techniques eliminate this

concern. A1 measures filtered versions of Q1's gate and source voltages. A1's output biases Q2, forcing Q1's channel current to whatever value is required to equalize A1's inputs, and hence Q1's gate and source voltages. A1's input filtering and roll-off are far slower than input frequencies of interest; its action does not interfere with the circuit's main signal path. The 330pF capacitor prevents fast edges coupled through Q2's collector base junction from influencing A1's operation.

Q1 should contribute negligible timing error to minimize overall delay. Figure 61's photo verifies Q1's wideband operation. Trace B, Q1's source, lags the input (Trace A) by only 300ps. Input, FET buffer output and C1 output appear as Traces A, B and C, respectively in Figure 62. As before, the FET buffer is seen to contribute small timing error, and C1's output is about 8ns delayed from the input.

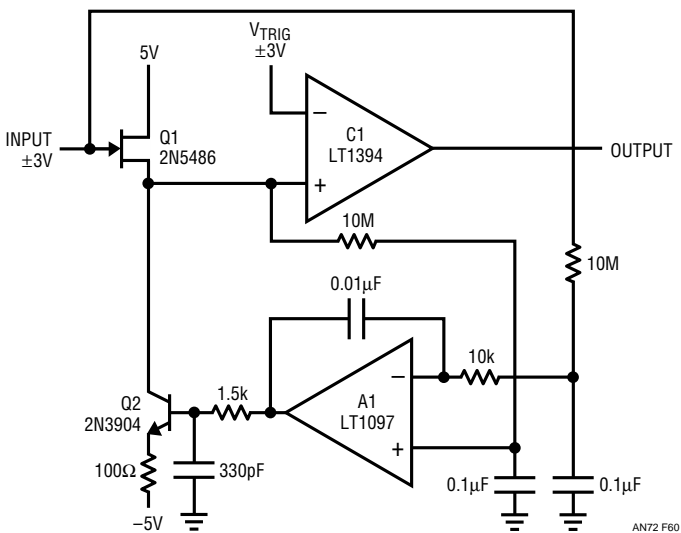
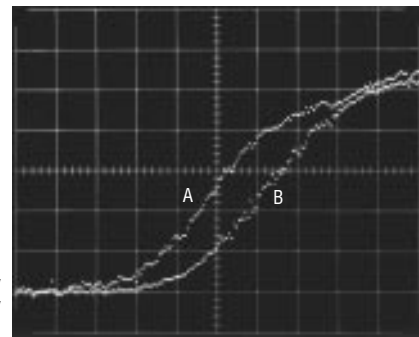


Figure 60. Buffer Provides 2pF, 50pA Input Characteristics for Fast Trigger. Amplifier-Stabilized Biasing Eliminates FET Offset

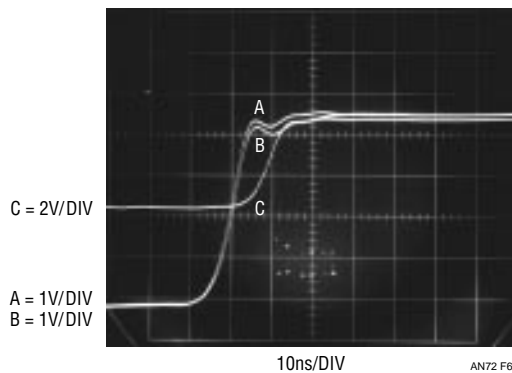


A = 1V/DIV
B = 1V/DIV

200ps/DIV

AN72 F61

Figure 61. Trigger Buffer's 300ps Delay Minimizes Timing Error. 4GHz Sampling Oscilloscope's Output Is a Series of Dots



C = 2V/DIV

A = 1V/DIV
B = 1V/DIV

10ns/DIV

AN72 F62

Figure 62. Input (Trace A), FET Source (Trace B) and Output (Trace C) Waveforms for the Trigger. Total Delay Is 8ns

High Speed Adaptive Trigger Circuit

Line and fibre-optic receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 63 triggers on 2mV to 175mV signals from 100Hz to 45MHz while operating from a single 5V rail. A1, operating at a gain of 15, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394's positive input. The LT1394's negative input is biased directly from A1's output. The LT1394's output, the circuit's output, is unaffected by >85:1 signal amplitude variations. Bandwidth limiting in A1 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

Figure 64 shows operating waveforms at 45MHz. Trace A's input produces Trace B's amplified output at A1. The comparator's output is Trace C.

Split supply versions of this circuit can achieve bandwidths to 50MHz with wider input operating range (see Reference 17).

18ns, 500μV Sensitivity Comparator

The ultimate limitation on comparator sensitivity is available gain. Unfortunately, increasing gain invariably involves giving up speed. The gain vs. speed trade-off in a fast comparator is usually a practical compromise designed to satisfy most applications. Some situations, however, require more sensitivity (e.g., higher gain) with

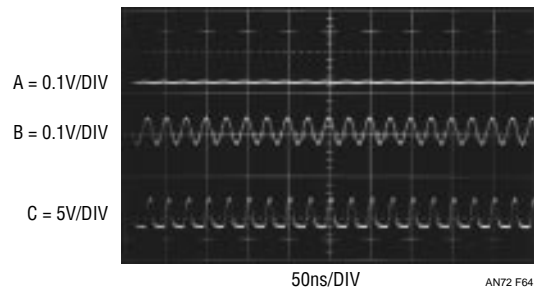


Figure 64. Adaptive Trigger Responding to a 40MHz, 5mV Input. Input Amplitude Variations from 2mV to 175mV Are Accommodated

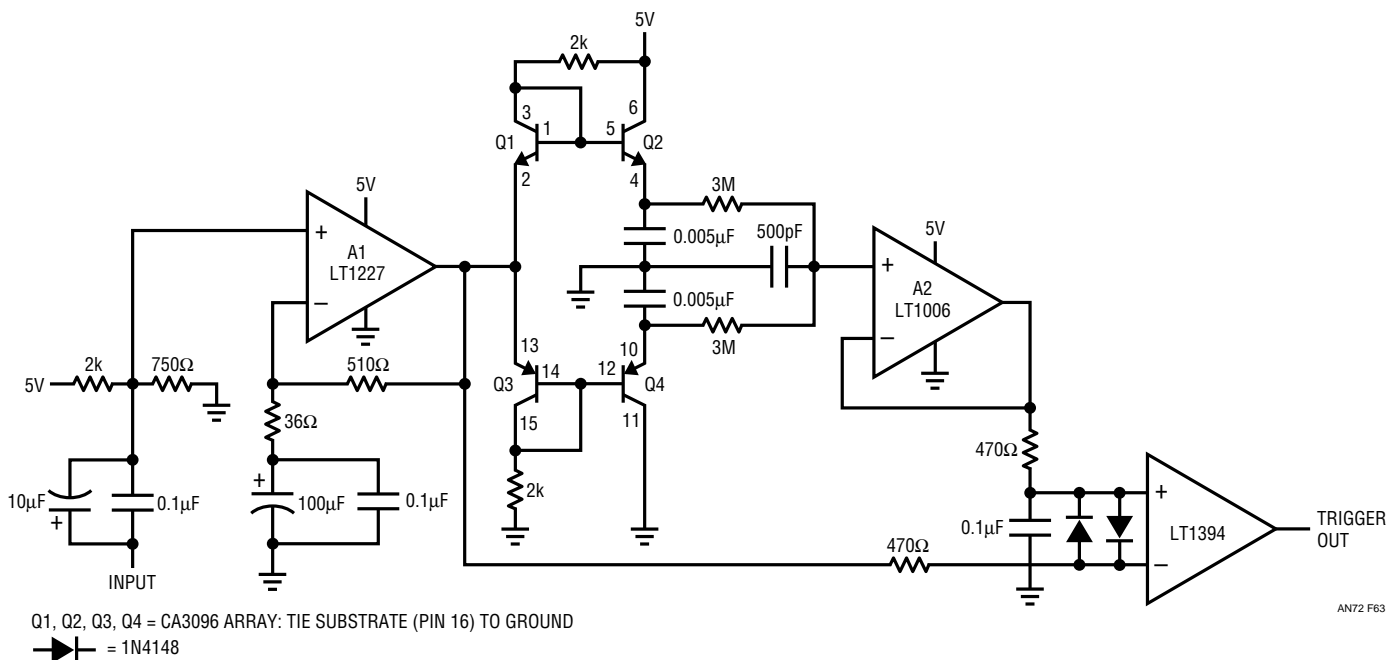


Figure 63. 45MHz Single Supply Adaptive Trigger. Output Comparator's Threshold Varies Ratiometrically with Input Amplitude, Maintaining Data Integrity over >85:1 Input Amplitude Range

Application Note 72

minimal impact on speed. Figure 65's circuit adds a differential preamplifier ahead of the LT1394, increasing gain. This permits 500 μ V comparisons in 18ns. A parallel path DC stabilization approach eliminates preamplifier drift as an error source. A1 is the differential preamplifier, operating at a gain of 100. Its output is AC-coupled to the LT1394. A1 has poorly defined DC characteristics, necessitating some form of DC correction. A2 and A3, operating at a differential gain of 100, provide this function. They differentially sense a band limited version of A1's inputs and feed DC and low frequency amplified information to the comparator. The low frequency roll-off of A1's signal path complements A2-A3's high frequency roll-off. The summation of these two signal channels at the LT1394 inputs results in flat response from DC to high frequency.

Figure 66 shows waveforms for the high gain comparator. Trace A is a 500 μ V overdrive on a 1mV step applied to the circuit's positive input (negative input grounded). Trace B shows the resulting amplified step at A1's positive output. Trace C is A2's band limited output. A1's wideband output combines with A2's DC corrected information to yield the correct, amplified composite signal at the LT1394's positive input in Trace D. The LT1394's output is Trace E. Figure

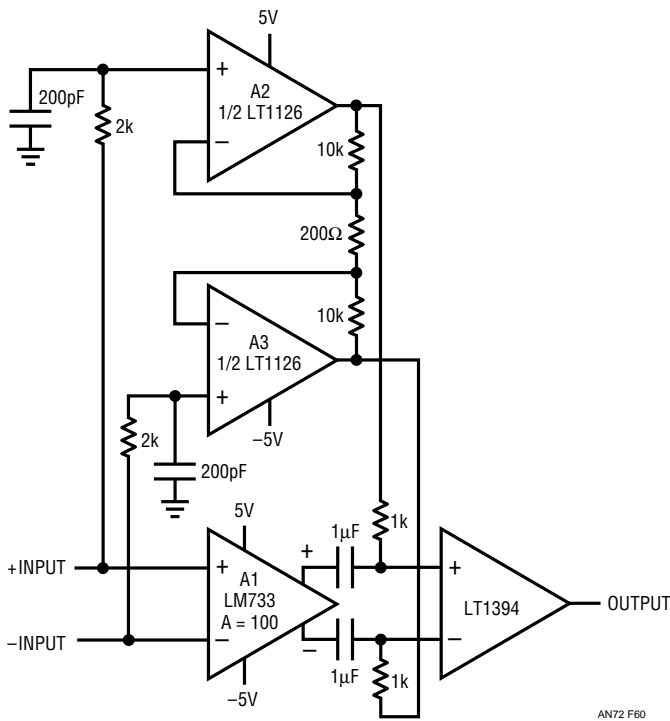


Figure 65. Parallel Preamplified Paths Allow 18ns Comparator Response to 500 μ V Overdrive

67 details circuit propagation delay. The output responds in 18ns to a 500 μ V overdrive on a 1mV step. Figure 68 plots response time versus overdrive. As might be expected, propagation delay decreases at higher overdrives. A1's noise limits usable sensitivity.

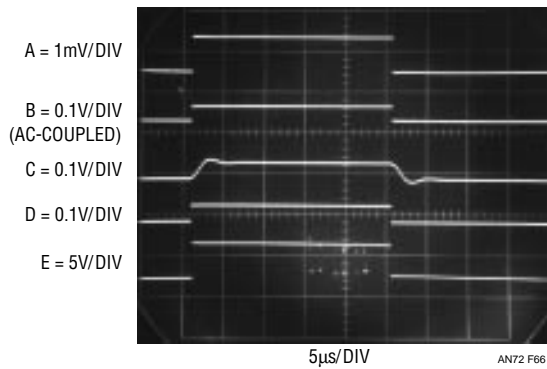


Figure 66. 500 μ V Input (Trace A) Is Split into Wideband and Low Frequency Gain Paths (Traces B and C) and Recombined (Trace D). Comparator Output Is Trace E

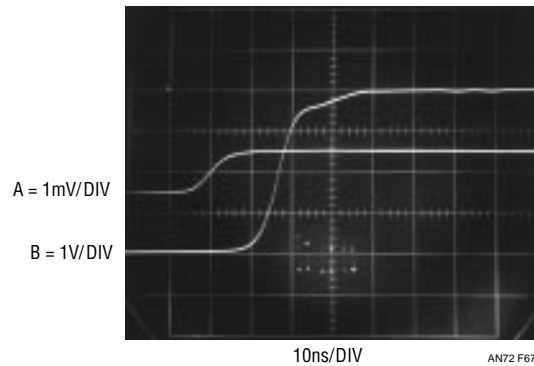


Figure 67. Parallel Path Comparator Shows 18ns Response (Trace B) to 500 μ V Overdrive (Trace A)

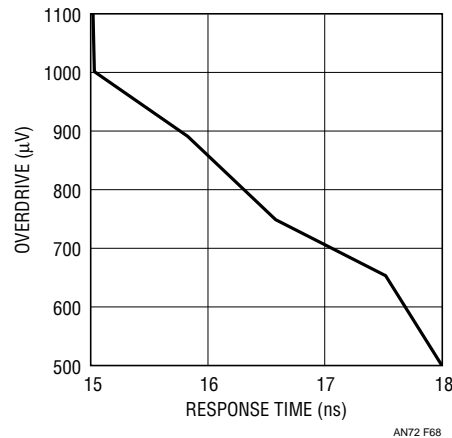


Figure 68. Response Time vs Overdrive for the Composite Comparator

Voltage-Controlled Delay

The ability to set a precise, predictable delay has broad application in pulse circuitry. Figure 69's configuration sets a 0 to 300ns delay from a corresponding 0V to 3V control voltage. It takes advantage of the LT1394's speed and the clean dynamics of an emitter switched current source.

Q1 and Q2 form a current source that charges the 1000pF capacitor. When the trigger input is high (Trace A, Figure 70) both Q3 and Q4 are on. The current source is off and Q2's collector (Trace B) is at ground. The latch input at the LT1394 prevents it from responding and its output remains high. When the trigger input goes low, the LT1394's latch input is disabled and its output drops low. Q4's collector (Trace C) lifts and Q2 comes on, delivering constant current to the 1000pF capacitor (Trace B). The resulting linear ramp at the LT1394's positive input is compared to the delay programming voltage input. When a crossing occurs, the comparator goes high (Trace D). The length of time the comparator was low is directly proportional to the delay programming voltage. The fast switching and ramp linearity permits 1ns accuracy and 100ps repeatability. Figure 71, a high speed expansion of the current source turn-on, details the clean switching. Q4 goes off within 2ns of the trigger input (Trace A) dropping low, enabling the

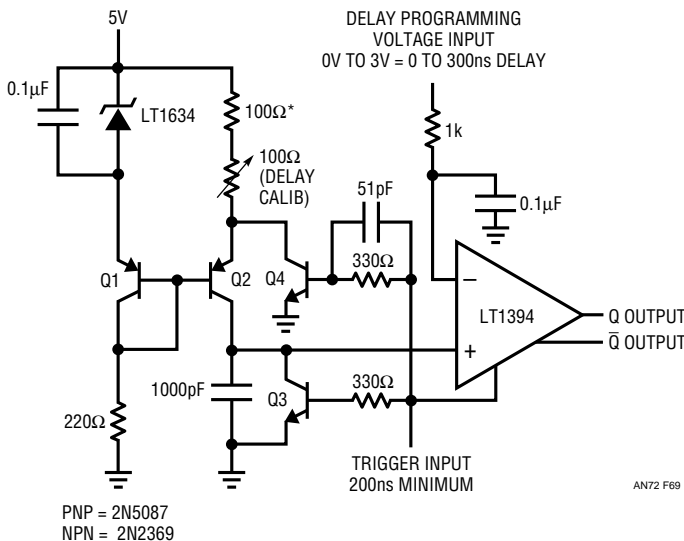


Figure 69. Fast, Precise, Voltage-Controlled Delay. Emitter Switched Current Source Has Clean, Predictable Dynamics

current source (Q2's emitter is Trace C). Concurrently, the 1000pF capacitor's ramp (Trace B) begins. The LT1394's output (Trace D) drops low about 7ns later, returning high after crossing (in this case) a relatively low programming voltage. Figure 72 juxtaposes the waveforms differently, permitting enhanced study of circuit timing. Switching begins with the input trigger falling low (Trace A). The ramp (Trace C) begins 3ns after the current source turns on (Q2 emitter is Trace D). The output pulse (Trace B) begins about 4ns later.

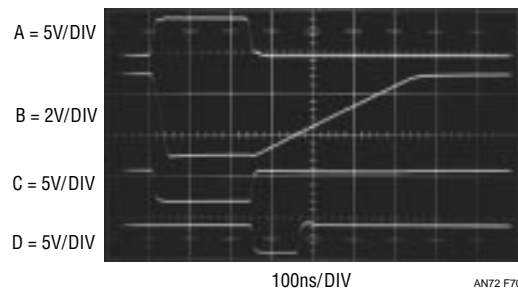


Figure 70. Voltage-Controlled Delay's Waveforms. Programming Voltage Determines Delay Between Input (Trace A) Falling Edge and Output (Trace D) Rising Edge. High Linearity Timing Ramp (Trace B) Permits 1ns Accuracy and 100ps Repeatability

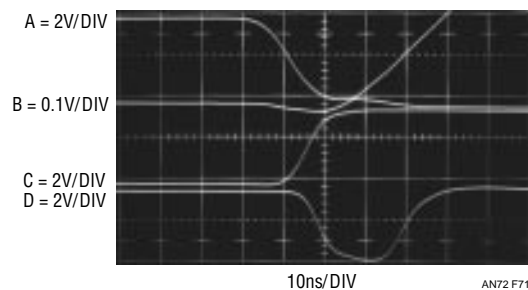


Figure 71. High Speed Expansion of Figure 70. Ramp (Trace B) Begins When Trigger (Trace A) Falls and Current Source Turns On (Trace C). Trace D is Output

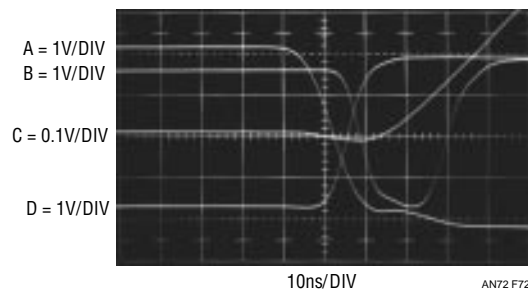


Figure 72. Delay's Output Switching Begins with Trigger Falling Low (Trace A). Ramp (Trace C) Starts 3ns After Current Source Turn-On (Trace D). Output (Trace B) Begins 4ns Later

Application Note 72

To calibrate this circuit apply a trigger input and 3V to the programming input. Adjust the 100Ω trim for a 300ns width at the LT1394's output.

10ns Sample-and-Hold

Figure 73's 10ns sample-and-hold applies the previous circuit. This sample-and-hold circuit is extremely fast, although it can only be used with repetitive signals. Here, C1 drives differential integrator A1's input. Feedback from the integrator back to C1 closes a loop around the circuit. Figure 74 shows what happens when a waveform (Trace A) is applied to the input. C2 generates a trigger signal for a programmable delay generator identical to the previously described circuit. The 74121 one-shot is triggered from the delay's output. Its Q output produces a 30ns pulse which is fed into a logic network with its \bar{Q} signal. The two inverter delays in Q's path give its associated gate a shorter duration output (Trace C) than Q's gate (Trace B). The last gate subtracts these two signals and generates a 10ns spike. This is inverted (Trace D) and fed to C1's latch pin. Each time the latch is enabled the comparator responds to the condition of the summing junction at its "+" input. If summing error is positive, A1 pulls current. If the error is negative, A1 sources current to the junction. After a number of input cycles, A1's output settles at a DC value that is the same as the level sampled during the time the latch is

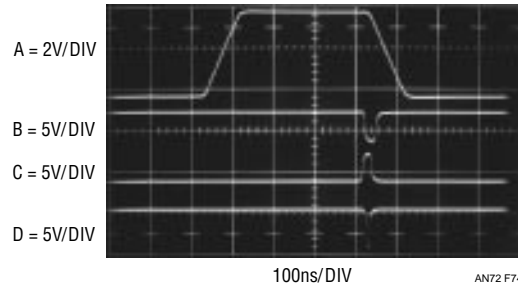


Figure 74. Sampling Pulse (Trace D) May Be Positioned at Desired Point on Input Waveform (Trace A)

enabled. The delay's voltage programming allows the 10ns sampling "window" to be positioned anywhere on the input waveform.

Programmable, Sub-Nanosecond Delayed Pulse Generator

The preceding circuit's 10ns wide sampling window limits sampling speed. Faster sampling requires narrower pulses. This circuit uses an avalanche pulse generator¹³ to create extremely short duration events. The combination of a controllable, calibrated delay and a very fast pulse generator has broad applicability in fast sampling circuitry.

Note 13: See References 17, 20, 22, 27 and 28 for background on avalanche pulse generator theory and practice.

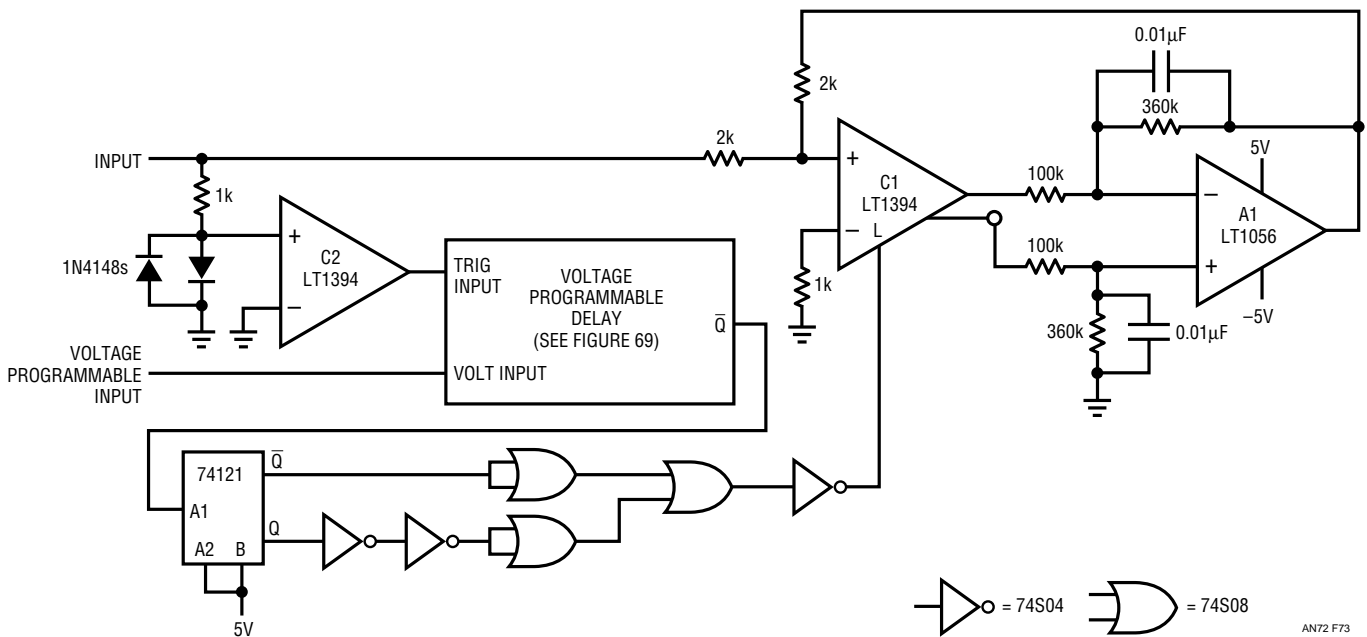


Figure 73. 10ns Sample-and-Hold for Repetitive Signals. Feedback Loop Around Comparator and Programmable Delay Allow Controllable Sampling of Input

In Figure 75, C1 and Q1 through Q4 form a voltage programmable delay identical to the one described in Figure 69. Q5, the LT1082 switching regulator and associated components comprise the avalanche pulse generator. The generator provides an 800ps pulse with rise and fall times inside 250ps. Pulse amplitude is 10V with a 50Ω source impedance.

The pulse generator requires high voltage bias for operation. The LT1082 switching regulator forms a high voltage switched mode control loop. The LT1082 pulse width modulates at its 40kHz clock rate. L1's inductive events are rectified and stored in the 2μF output capacitor. The adjustable resistor divider provides feedback to the LT1082. The 10k-1μF RC provides noise filtering.

The high voltage is applied to Q5, a 40V breakdown device, via the R3-C1 combination. The high voltage "bias adjust" control should be set at the point where free running pulses across R4 *just* disappear. This puts Q5 slightly below its avalanche point. When C1's output pulse is applied to Q5's base, it avalanches. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges to just below the avalanche point. At C1's next pulse this action repeats¹⁴.

Figure 76 shows the circuit input trigger (Trace A) that initiates the delay. After a time set by the programming input voltage, C1 goes high (Trace B). The avalanche pulse output is indicated in Trace C, but probe and oscilloscope bandwidth limitations prevent an accurate representation.

Note 14: This circuit is based on the operation of the Tektronix Type 111 pulse generator. See Reference 20.

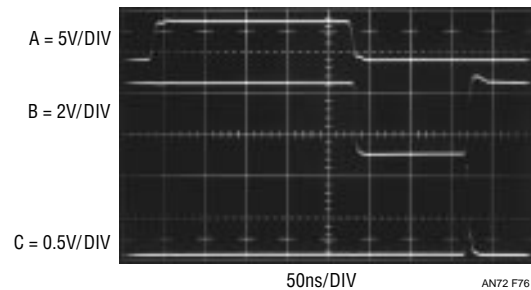


Figure 76. Input Trigger (Trace A) Initiates Delay (Trace B) with Resultant Output Pulse (Trace C). Oscilloscope Bandwidth Limitations Prevent Accurate Output Pulse Representation

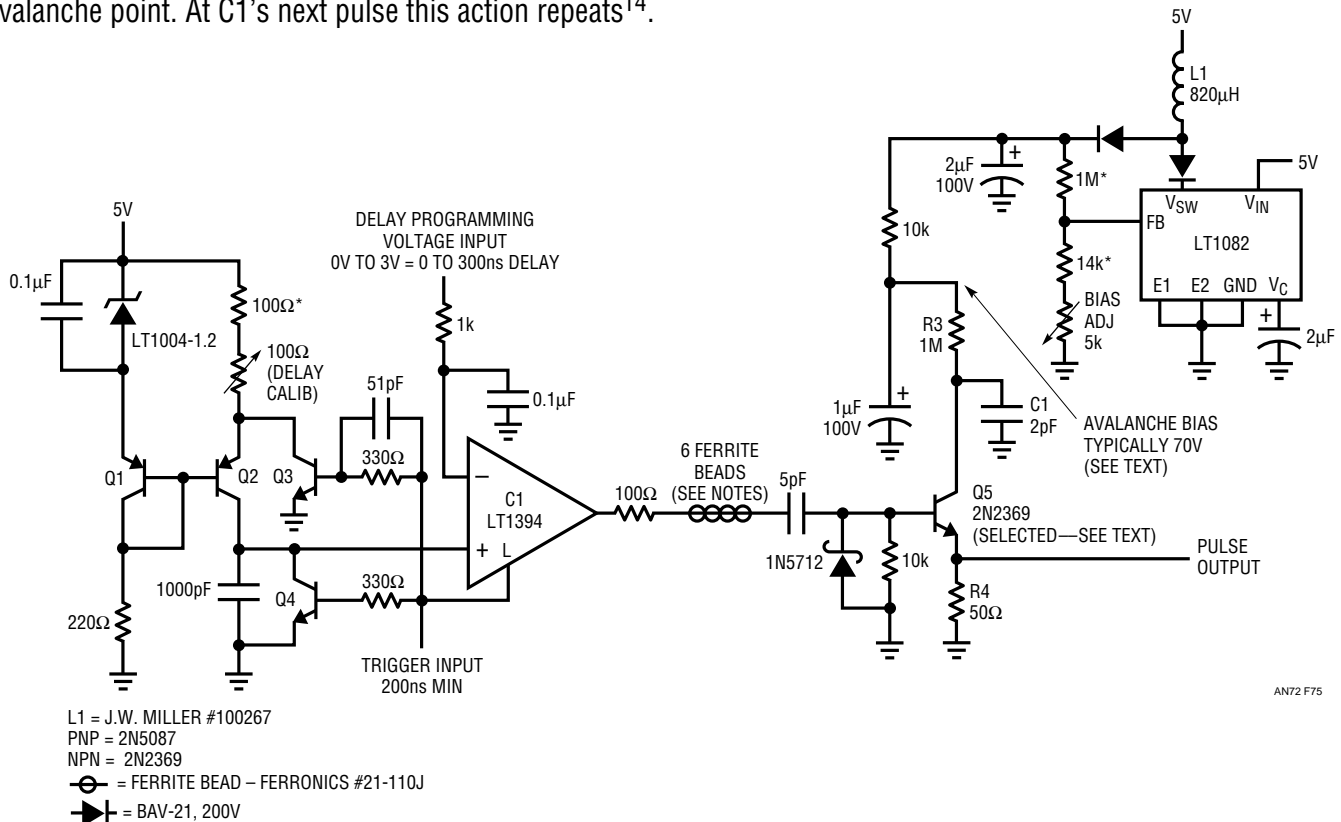


Figure 75. Figure 69's Programmable Delay Triggers a Sub-Nanosecond Pulse Generator

Application Note 72

Figure 77, taken with a 3.9GHz bandpass instrument (Tektronix 661 with 4S2 sampling plug-in) shows more detail. Trace A is C1's output, and Trace B is the avalanche pulse. When avalanche occurs, Q5's reverse base current rises so abruptly that C1's output cannot directly absorb it. The 100Ω resistor and the ferrite beads present impedance at frequency, allowing C1 to handle the load. Without this network, C1's positive-going output will completely reverse direction and ring severely before completing its transition, corrupting avalanche behavior. Even with these

components, artifacts of the avalanche induced base current are clearly visible in C1's trace.

The avalanche pulse measures 8V high with a 1.2ns base. Rise time is 250ps, with fall time indicating 200ps. The times are probably slightly faster, as the oscilloscope's 90ps rise time influences the measurement.¹⁵

Q5 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12-year date code span, yielded 82%. All "good" devices switched in less than 600ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout, connection and termination techniques is essential for good results from this circuit.

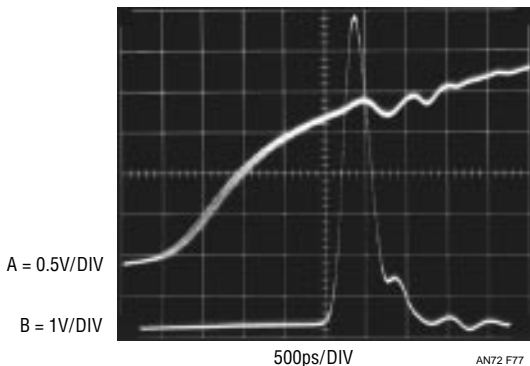


Figure 77. 3.9GHz Sampling Oscilloscope Measures Delay Output and Avalanche Pulse. Pulse-Induced Loading Is Buffered by Ferrite Beads, but Artifacts Appear in Delay Output

Fast Pulse Stretcher

The minimum input pulse width required to operate a pulse stretcher is usually in the 5ns to 10ns range. Additionally, the rise and delay times are of the same order. Figure 78's circuit is considerably faster. It produces a stretched pulse from a 2ns width input with rise and delay times of 650ps.

Note 15: I'm sorry, but 3.9GHz is the fastest 'scope in my house (as of November 1996).

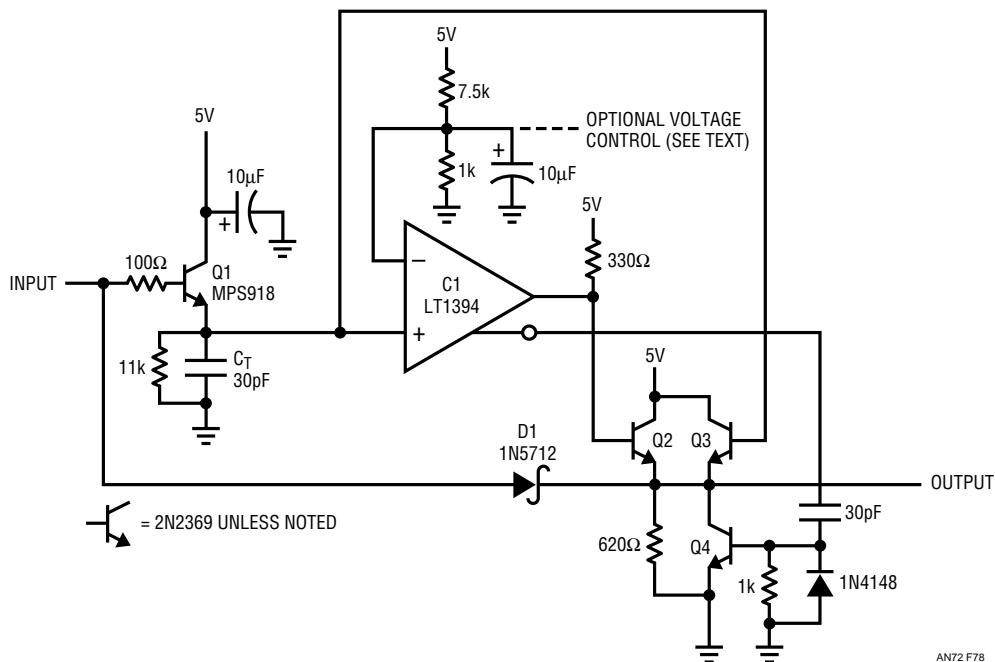


Figure 78. High Speed Pulse Stretcher Has Sub-Nanosecond Delay and Rise Time

The input pulse (Trace A, Figure 79) causes Q1 to conduct, charging the timing capacitor, C_T (Trace B). The input pulse is also fed forward around C1, via D1, to the output (Trace C). Additionally, C_T 's potential, buffered by Q3, is similarly fed forward to the output. C1 responds to C_T 's charging by going high. Its output turns Q2 on, augmenting the outputs high state. C1's 7ns delay does not affect output delay or waveshape because the feedforward paths "fill in" the dead time before the comparator responds. The output pulse is a composite of the input and comparator-based response. The small change in output amplitude when the input ceases is related to this, but is not deleterious. When the input pulse falls, C1's output, and hence the circuit's output, remains high until C_T discharges below C1's negative input. When C1 goes low its inverting output goes high, pulsing Q4 to pull the output down in 5ns.

The feedforward paths are crucial to circuit operation. The effect of D1's path is readily understood, but the C_T -originated route is less obvious. A good way to see the effect of C_T 's path is to eliminate it. Figure 80's photo, taken with Q3's base open, is quite revealing. Trace A is the input pulse, Trace B the output and Trace C is C1's output. The absence of the C_T -based feedforward path is clearly evident. The output (again, Trace B) sags for 8ns before the comparator responds, restoring output amplitude.

Evaluating circuit operation requires a fast pulse generator and a wideband oscilloscope. Figure 81's photo, taken at 100x Figure 79's sweep rate, shows the pulse stretcher's input-output relationship in a 3.9GHz sampled bandpass. Trace A is the input pulse and Trace B the output. As in Figure 79, output amplitude drops slightly when the input ceases, but the logical high state is maintained. Also visible on the inputs leading edge is a 0.5V amplitude 500ps aberration which occurs about 3V into the transition.

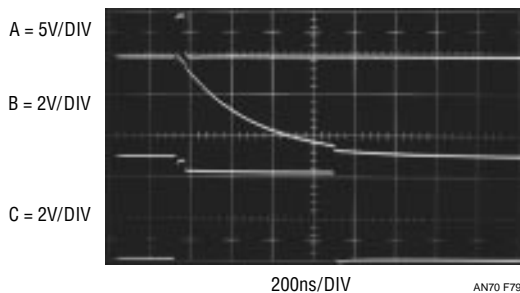


Figure 79. Waveforms for the Pulse Stretcher. Input (Trace A) Triggers Ramp Decay (Trace B), Resulting in Stretched Output (Trace C). Output Is a Composite of Input and Comparator-Based Response

Figure 82 further increases sweep rate to examine the input (Trace A) and output (Trace B) leading edges. The output is delayed from the input by only 650ps, with rise time also

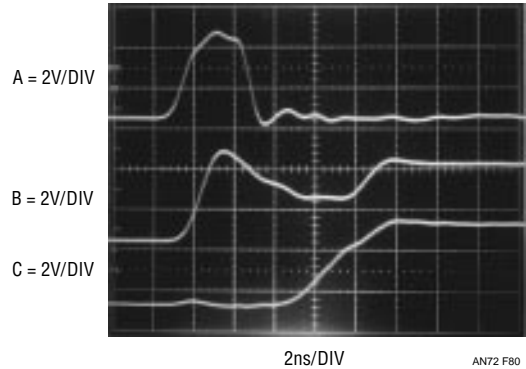


Figure 80. Results of Disconnecting C_T -Originated Feedforward Path. Output (Trace B) Sags for 8ns Before C1 (Trace C) Can Restore Its Amplitude

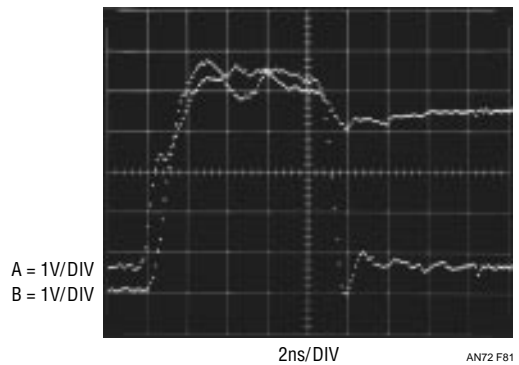


Figure 81. Pulse Stretcher's Input-Output Relationship in a 3.9GHz Bandpass. Output Amplitude Drops When Input Decays, but Logic Level Is Maintained. Sampling Oscilloscope Display Is a Series of Dots

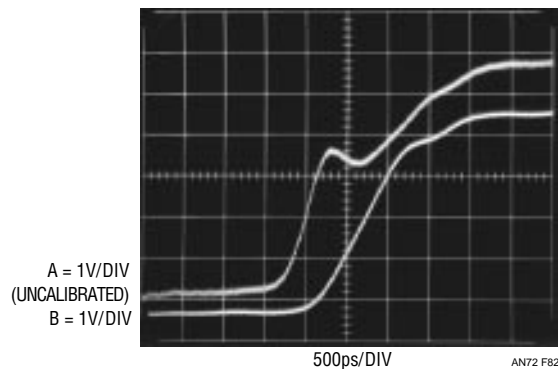


Figure 82. Pulse Stretcher Waveforms in 3.9GHz Bandpass Show 650ps Output Rise and Delay Times (Trace B). Nonlinear Loading Causes Input Transition Aberration (Trace A), but Is Not Deleterious. Trace Granularity Derives from Sampling Oscilloscope Operation

Application Note 72

about 650ps. The input transition aberration, now clearly visible, is due to the circuit's nonlinear input impedance. It occurs above a logical high level, and is acceptable.

Output pulse width is approximately equal to the input pulse width added to 25ns/pF of C_T . The ratiometric biasing of C1's inputs provides supply variation immunity from $5V \pm 5\%$. The output width can be voltage controlled by biasing C1's negative input, but supply immunity will be compromised. The minimum input trigger width to maintain programmed output width within 1% is 2ns.

20ns Response Overvoltage Protection Circuit

It is often desirable to protect an expensive load from supply overvoltage. Overvoltage events may derive from supply failure or poor transient response. In Figure 83, Q1, a source follower, receives gate overdrive bias from the 12V bias supply and is saturated. The regulator driving Q1's drain takes feedback from the source, eliminating Q1's saturation resistance as an output impedance term.

C1 monitors the 3V output feeding the protected load. Under normal conditions C1's positive input is below its negative input, and its output is low. Q2 through Q5 are off and the load receives drive via Q1. Figure 84 shows what

happens when an overvoltage event occurs. The 3V output (Trace A) begins to rise (note upward excursion beginning about center screen). This is detected at C1, and its output (Trace B) goes high. Q2 and Q3 come on very quickly, pulling down Q1's gate (Trace C). Q4 and Q5, slower devices, turn on after Q2-Q3, and shunt Q1's residual output to ground without experiencing excessive current. C1's output is fed via a 330Ω resistor to its latch pin. This causes C1 to latch high, preventing any output until the overvoltage cause is corrected. Reset is accomplished by breaking the latch with the normally open reset switch.

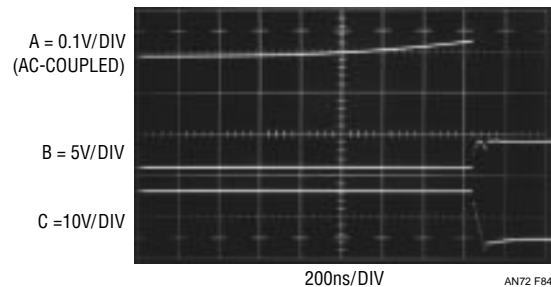


Figure 84. Overvoltage Event (Note Upward Excursion, Trace A) Triggers Comparator (Trace B), Resulting in Gate Bias Collapse (Trace C)

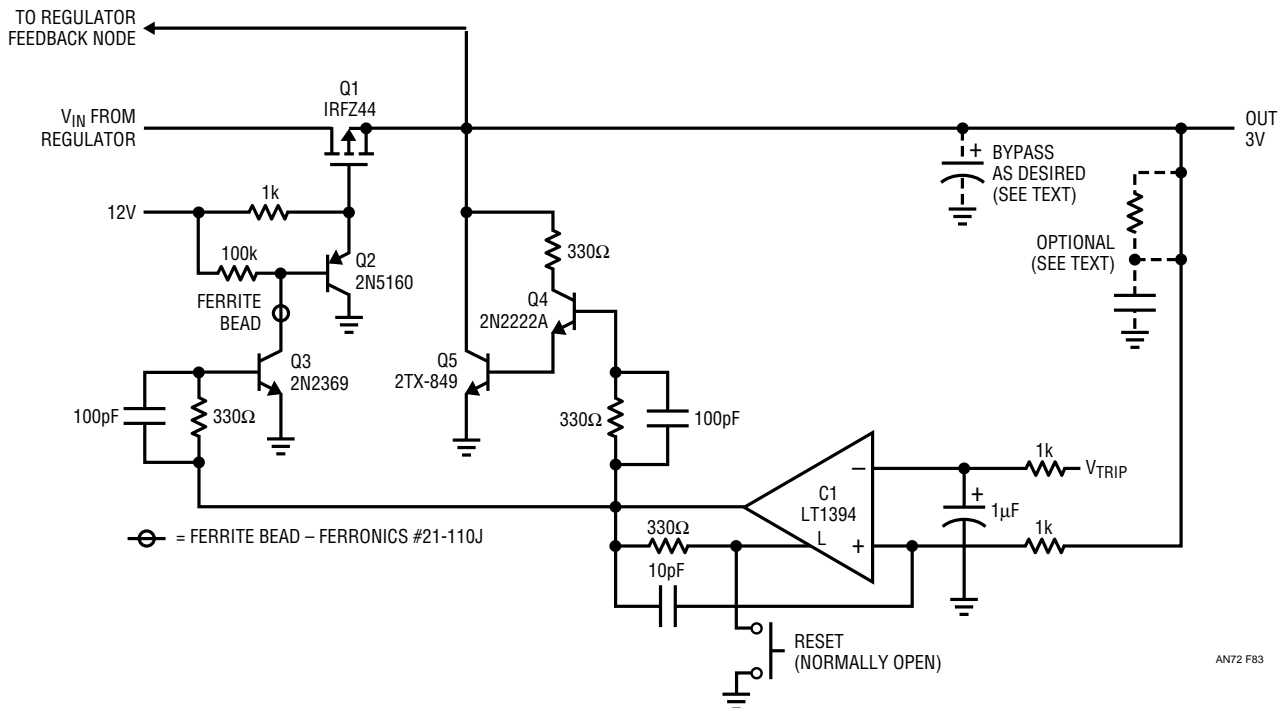


Figure 83. A 20ns Response Time Overvoltage Protection Circuit. Latching Comparator Drives a Turn-Off Optimized Series—Shunt Switch

The switching is arranged to optimize turn-off time; Figure 85 shows just how fast the circuit is. As before, Trace A is the 3V output; Trace B, C1's output and Trace C, Q1's gate. The output's amplitude (Trace A) excursion begins just prior to the second vertical division. C1 responds (Trace B) by going high, turning on Q2 and Q3. This initial turn-on pulls Q1's gate downwards (Trace C), arresting the output excursion in 20ns. As Q2 pulls charge out of Q1, gate bias decays. When Q4 and Q5 come on, Q1 is out of saturation and the output drops rapidly. The overvoltage event is arrested in 20ns with total shutdown taking 150ns. Bypassing of Q1's source is optional—it will slow down the overvoltage rise time, but also restricts turn-off time. Similarly, the optional RC filter will eliminate noise-induced nuisance tripping at the expense of response time.

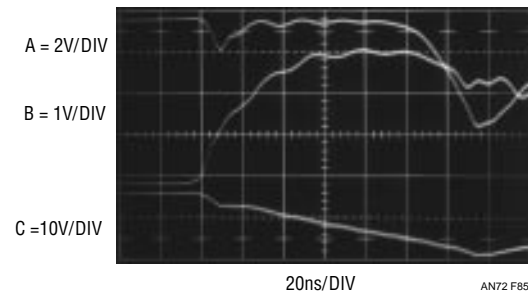


Figure 85. Detail of Protection Circuits Behavior. Output Amplitude Excursion (Trace A) Triggers Comparator (Trace B), Resulting Gate Drive Removal (Trace C). Overvoltage is Arrested in 20ns, Complete Shutdown Requires 150ns

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APPENDIX A

About Level Shifts

The LT1394's logic output will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1394-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1394 is a sink-source pair (Figure A1) with good ability

to drive capacitance (such as feedforward capacitors). Figure A2 shows a noninverting voltage gain stage with a 15V output. When the LT1394 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

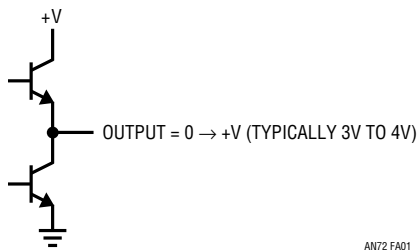


Figure A1. Simplified LT1394 Output Stage

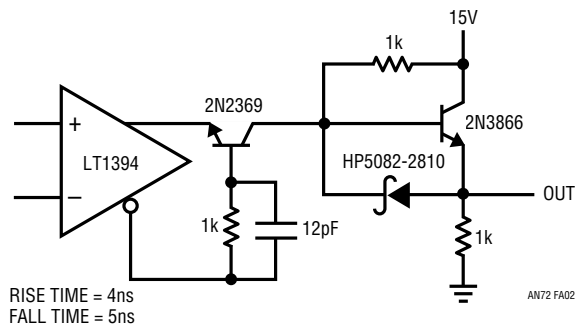


Figure A2. Level Shift Has Noninverting Voltage Gain

Figure A3 is a very versatile stage. It features a bipolar swing that is set by the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1394 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1394's output transition (Trace A, Figure A5), but Q2's switching is clean (Trace B, Figure A5) with 3ns delay on the rise and

fall of the pulse. Figure A4 is similar to A2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET that switches 1A at 15V. Most of the 7ns to 9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T s. To get the kind of results shown, switching times in the nanosecond range and f_T s approaching 1GHz are required.

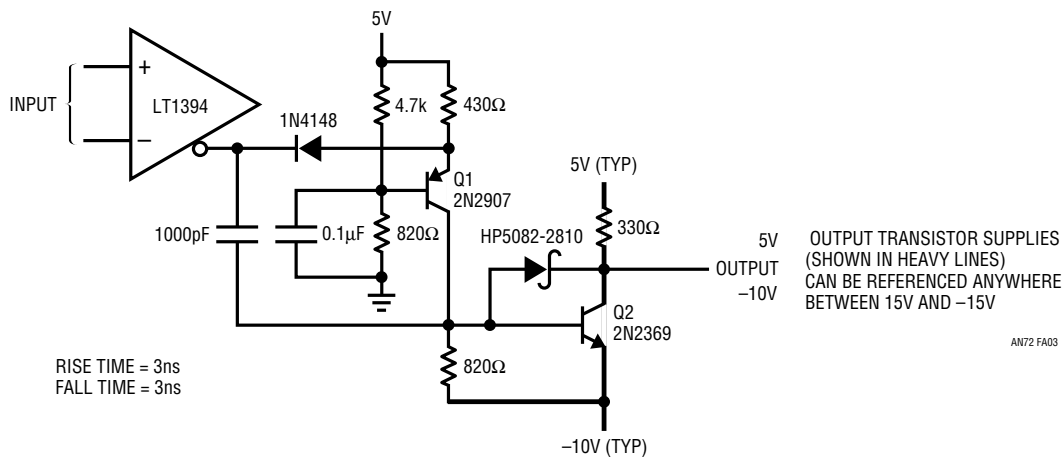


Figure A3. Level Shift with Inverting Voltage Gain—Bipolar Swing

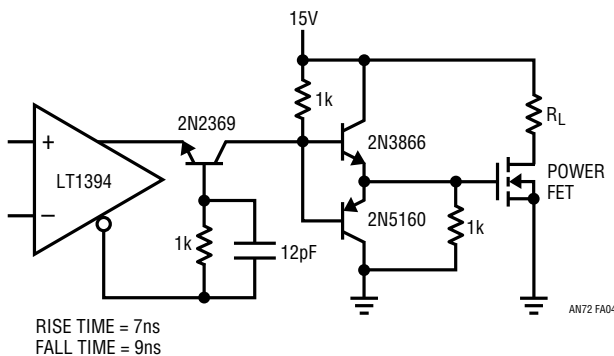


Figure A4. Noninverting Voltage Gain Level Shift

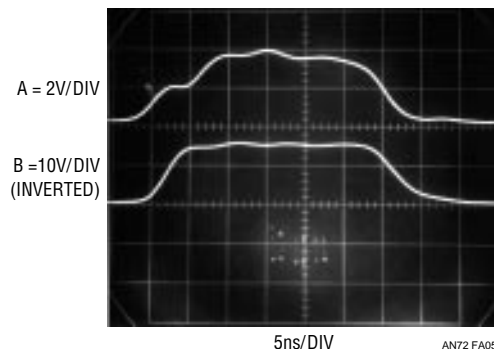


Figure A5. Figure A3's Waveforms

Application Note 72

APPENDIX B

Measuring Probe-Oscilloscope Response

The LT1394's 7ns response time and the circuitry it is used in will challenge the best test equipment. Many of the measurements made utilize equipment near the limit of its capabilities. It is a good idea to verify parameters such as probe and scope rise time and differences in delays between probes and even oscilloscope channels. Verifying the limits of wideband test equipment setups is a difficult task. In particular, the end-to-end rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure B1 circuit does this, providing a 1ns pulse with rise and fall times inside 250ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage step-

up network. L1 periodically receives charge and its flyback discharge delivers high voltage events to the step-up network. A portion of the step-up network's DC output is fed back to the LT1073 via the 10M-24k divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the 1M-2pF combination. Q1, a 40V breakdown device, nondestructively avalanches when C1 charges high enough. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free running oscillation at about 200kHz.^{1, 2} Figure B2 shows the output pulse. A 12.4GHz sampling oscilloscope measures the double-terminated pulse at 4.8V high with about a 700ps base. Rise time is 216ps, with fall time 232ps. There is a slight hint of ring after the falling edge, but it is well controlled.

Note 1: This method of generating fast pulses borrows heavily from the Tektronix type 111 Pretrigger Pulse Generator. See References 17, 20, 22, 27 and 28.

Note 2: If desired, the avalanche pulse generator may be externally triggered. See Figure 75 and associated text. See also References 20 and 22.

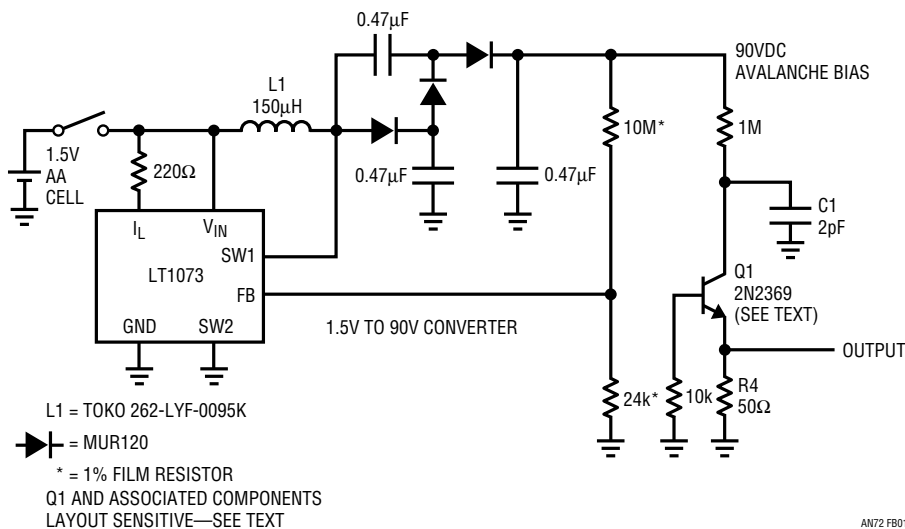


Figure B1. 250ps Rise/Fall Time Avalanche Pulse Generator

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12-year date code span, yielded 82%. All good devices switched in less than 650ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout techniques is essential for good results from this circuit. Current drain from the 1.5V battery is about 5mA.

Figure B3 shows the physical construction of the actual generator. Power, supplied from a separate box, is fed into the generator's enclosure via a BNC connector. Q1 is mounted *directly* at the output BNC connector, with grounding and layout appropriate for wideband operation. Lead length, particularly Q1's and C1's, should be experimented with to get best output pulse purity. Figure B4 is the complete unit.

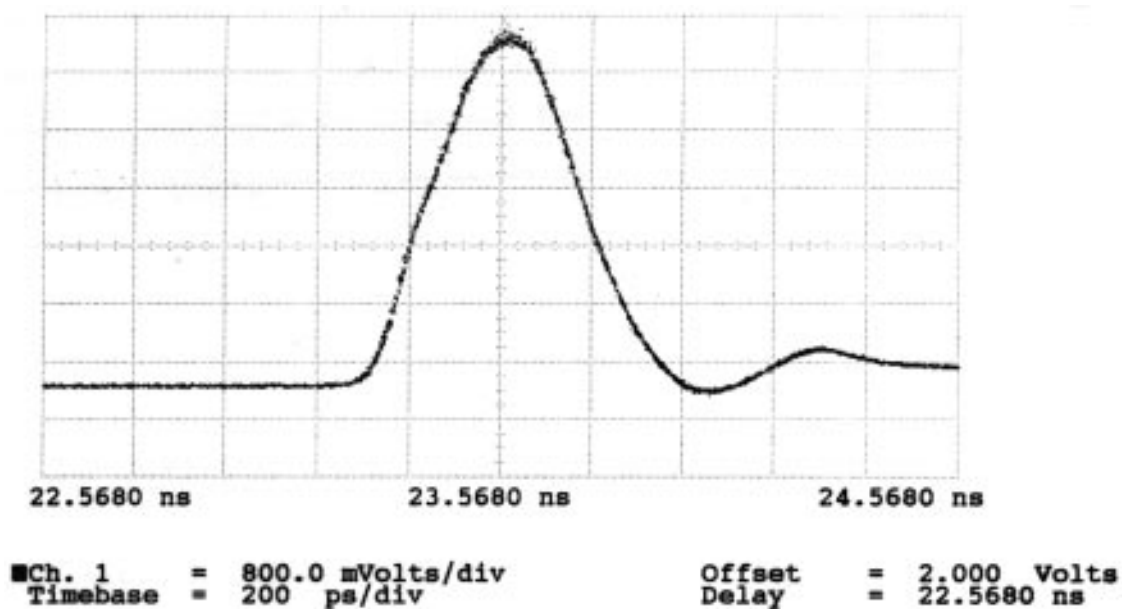
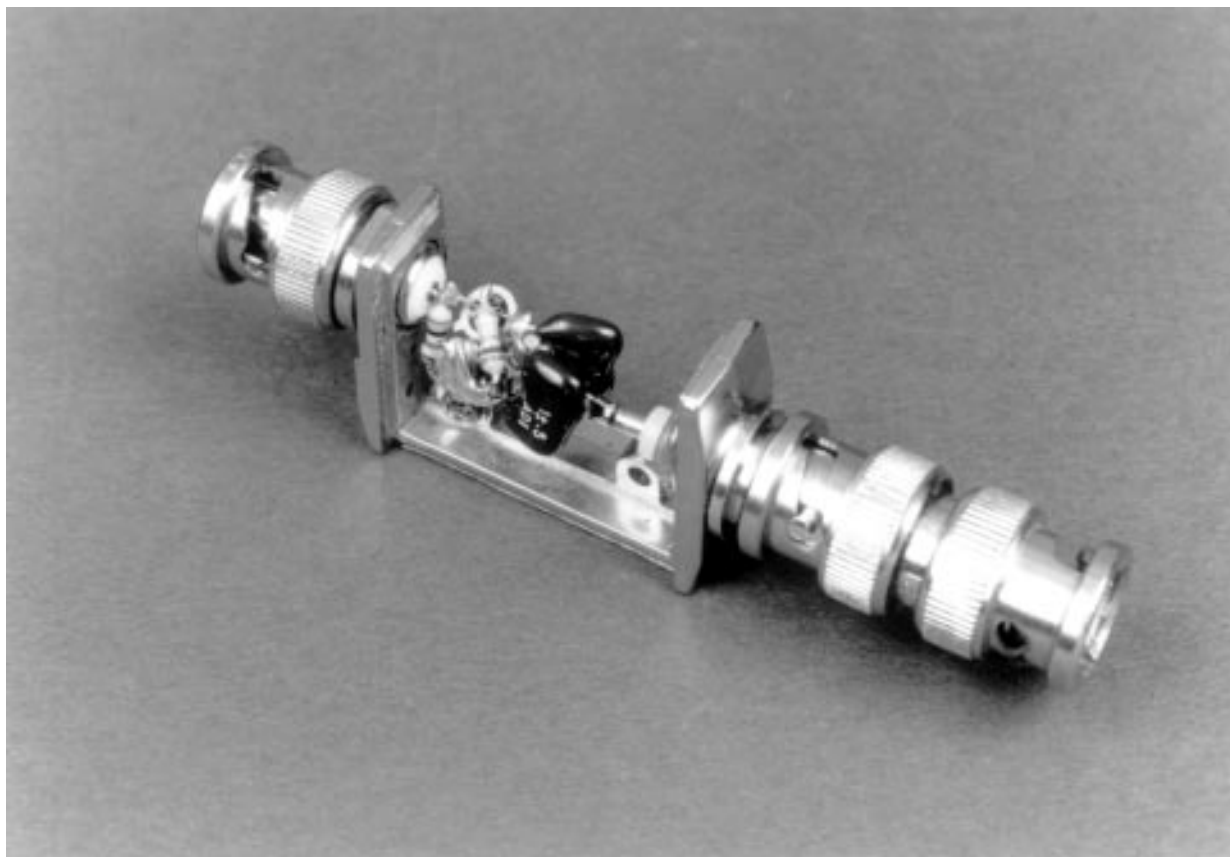


Figure B2. The Avalanche Pulse Generator's Output Monitored on a Hewlett-Packard 54120B 12GHz Sampling Oscilloscope. Double-Terminated Output Reduces Pulse Amplitude

(Courtesy of T. Hornak, Hewlett-Packard Laboratories)



AN72 FB03

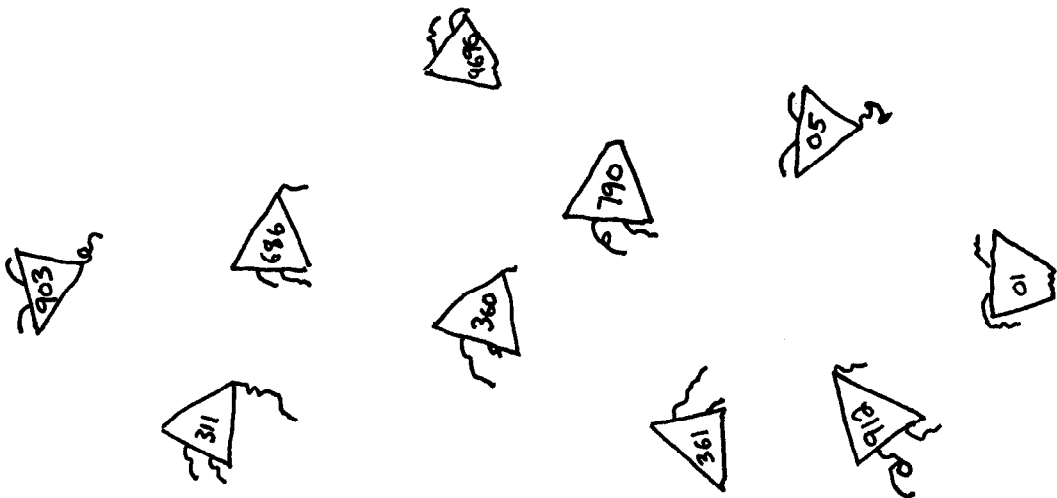
Figure B3. Details of the Avalanche Pulse Generator's Head. 90VDC Enters at Lower Right BNC, Pulse Exits at Top Left BNC. Note Short Lead Lengths Associated with Output



AN72 FB04

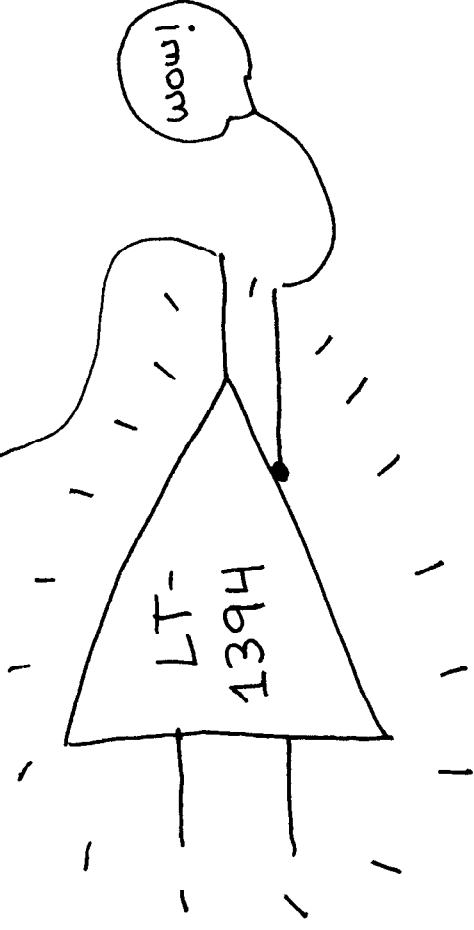
Figure B4. The Packaged Avalanche Pulser. 1.5V-to-90V Converter Is in the Black Box. Avalanche Head Is at Left

COMPARABLE



INCOMPARABLE

- 7 NS Response Time
- Single supply operation - Common Mode Range Includes GROUND
- COMPLEMENTARY OUTPUTS
- 7 MA supply Current
- Stable in Linear Region - NO Oscillations or Glitching
- $V_{OS} = 2mV, 24V/\Omega$
- LATCH PIN
- $I_B = 1.4A$
- $A = 1400$



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Component and Measurement Advances Ensure 16-Bit DAC Settling Time

The art of timely accuracy

Jim Williams

Introduction

Instrumentation, waveform generation, data acquisition, feedback control systems and other application areas are beginning to utilize 16-bit data converters. More specifically, 16-bit digital-to-analog converters (DACs) have seen increasing use. New components (see Components for 16-Bit Digital-to-Analog Conversion, page 2) have made 16-bit DACs a practical design alternative¹. These ICs provide 16-bit performance at reasonable cost compared to previous modular and hybrid technologies. The DC and AC specifications of the monolithic DAC's approach or equal previous converters at significantly lower cost.

DAC Settling Time

DAC DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, the settling time of the DAC and its output amplifier is extraordinarily difficult to determine to 16-bit resolution. DAC settling time is the elapsed time from input code application until the output arrives at and remains within a specified error band around the final value. It is usually specified for a full-scale 10V transition. Figure 1 shows that DAC settling time has three distinct components. The *delay time* is very small and is almost entirely due to propagation delay through the DAC and output amplifier. During this interval there is no output movement. During *slew time* the output amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and

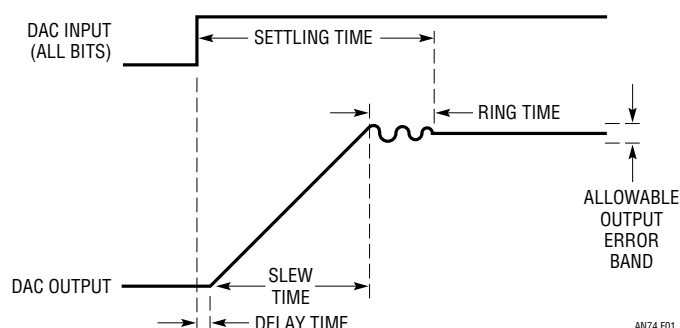


Figure 1. DAC Settling Time Components Include Delay, Slew and Ring Times. Fast Amplifiers Reduce Slew Time, Although Longer Ring Time Usually Results. Delay Time is Normally a Small Term

ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs which degrade DC error terms.²

Measuring anything at any speed to 16 bits ($\approx 0.0015\%$) is hard. Dynamic measurement to 16-bit resolution is particularly challenging. Reliable 16-bit settling time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique.

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Note 1. See Appendix A, "A History of High Accuracy Digital-to-Analog Conversion".

Note 2. This issue is treated in detail in latter portions of the text. Also see Appendix D "Practical Considerations for DAC-Amplifier Compensation."

Application Note 74

COMPONENTS FOR 16-BIT D/A CONVERSION

Components suitable for 16-bit D/A conversion are members of an elite class. 16 binary bits is one part in 65,536—just 0.0015% or 15 parts-per-million. This mandates a vanishingly small error budget and the demands on components are high. The digital-to-analog converters listed in the chart all use Si-Chrome thin-film resistors for high stability and linearity over

temperature. Gain drift is typically 1ppm/°C or about 2LSBs over 0°C to 70°C. The amplifiers shown contribute less than 1LSB error over 0°C to 70°C with 16-bit DAC driven settling times of 1.7µs available. The references offer drifts as low as 1LSB over 0°C to 70°C with initial trimmed accuracy to 0.05%

Short Form Descriptions of Components Suitable for 16-Bit Digital-to-Analog Conversion

COMPONENT TYPE	ERROR CONTRIBUTION OVER 0°C TO 70°C	COMMENTS
LTC [®] 1597 DAC	≈2LSB Gain Drift 1LSB Linearity	Full Parallel Inputs Current Output
LTC1595 DAC	≈2LSB Gain Drift 1LSB Linearity	Serial Input 8-Pin Package Current Output
LTC1650 DAC	≈3.5LSB Gain Drift 6LSB Offset 4LSB Linearity	Complete Voltage Output DAC
LT [®] 1001 Amplifier	<1LSB	Good Low Speed Choice 10mA Output Capability
LT1012 Amplifier	<1LSB	Good Low Speed Choice Low Power Consumption
LT1468 Amplifier	<2LSB	1.7µs Settling to 16 Bits Fastest Available
LM199A Reference-6.95V	≈1LSB	Lowest Drift Reference in This Group
LT1021 Reference-10V	≈4LSB	Good General Purpose Choice
LT1027 Reference-5V	≈4LSB	Good General Purpose Choice
LT1236 Reference-10V	≈10LSB	Trimmed to 0.05% Absolute Accuracy
LT1461 Reference-4.096V	≈10LSB	Recommended for LTC1650 DACs (see Above)

Considerations for Measuring DAC Settling Time

Historically, DAC settling time has been measured with circuits similar to that in Figure 2. The circuit uses the “false sum node” technique. The resistors and DAC-amplifier form a bridge type network. Assuming ideal resistors, the amplifier output will step to V_{IN} when the DAC inputs move to all ones. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage

should be zero. Note that the resistor divider’s attenuation means the probe’s output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. A 10pF probe alleviates this problem but

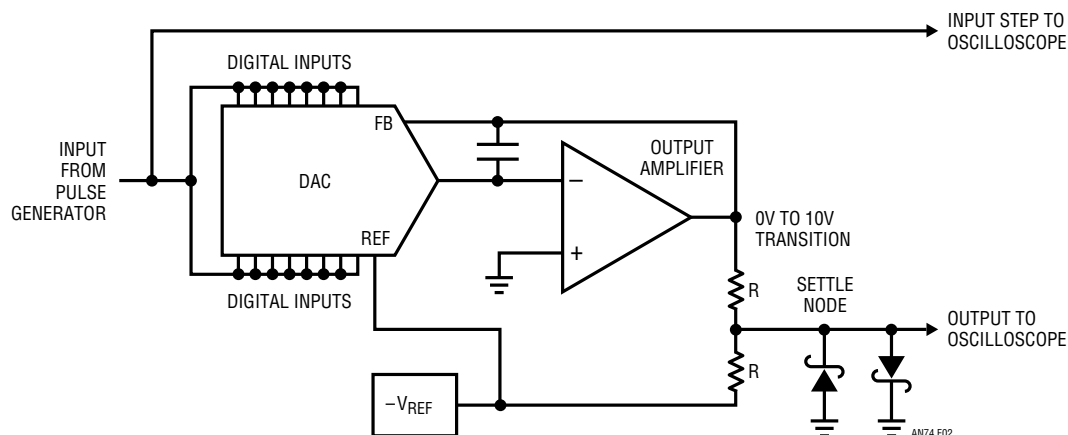


Figure 2. Popular Summing Scheme for DAC Settling Time Measurement Provides Misleading Results. 16-Bit Measurement Causes >200× Oscilloscope Overdrive. Displayed Information is Meaningless

its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An active 1× FET probe will work, but another issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question.³

At 10-bit resolution (10mV at the DAC output—5mV at the oscilloscope), the oscilloscope typically undergoes a 2× overdrive at 50mV/DIV, and the desired 5mV baseline is just discernible. At 12-bit or higher resolution, the measurement becomes hopeless with this arrangement. Increasing oscilloscope gain brings commensurate increased vulnerability to overdrive induced errors. At 16 bits, there is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring 16-bit settling time requires a high gain oscilloscope that is somehow immune to overdrive. The gain issue is addressable with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling 'scope.⁴ Unfortunately, these instruments are no longer manufac-

tured (although still available on the secondary market). It is possible, however, to construct a circuit that borrows the overload advantages of classical sampling 'scope technology. Additionally, the circuit can be endowed with features particularly suited for measuring 16-bit DAC settling time.

Practical DAC Settling Time Measurement

Figure 3 is a conceptual diagram of a 16-bit DAC settling-time-measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the preamplified oscilloscope is connected to the settle point by a switch. The switch state is determined by a delayed pulse generator, which is triggered from the same pulse that controls the DAC. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

Note 3: For a discussion of oscilloscope overdrive considerations, see Appendix B, "Evaluating Oscilloscope Overdrive Performance".

Note 4: Classical sampling oscilloscopes should not be confused with modern era digital sampling 'scopes that have overdrive restrictions. See Appendix B, "Evaluating Oscilloscope Overload Performance" for comparisons of various type 'scopes with respect to overdrive. For detailed discussion of classical sampling 'scope operation see references 14 through 17 and 20 through 22. Reference 15 is noteworthy; it is the most clearly written, concise explanation of classical sampling instruments the author is aware of. A 12 page jewel.

Application Note 74

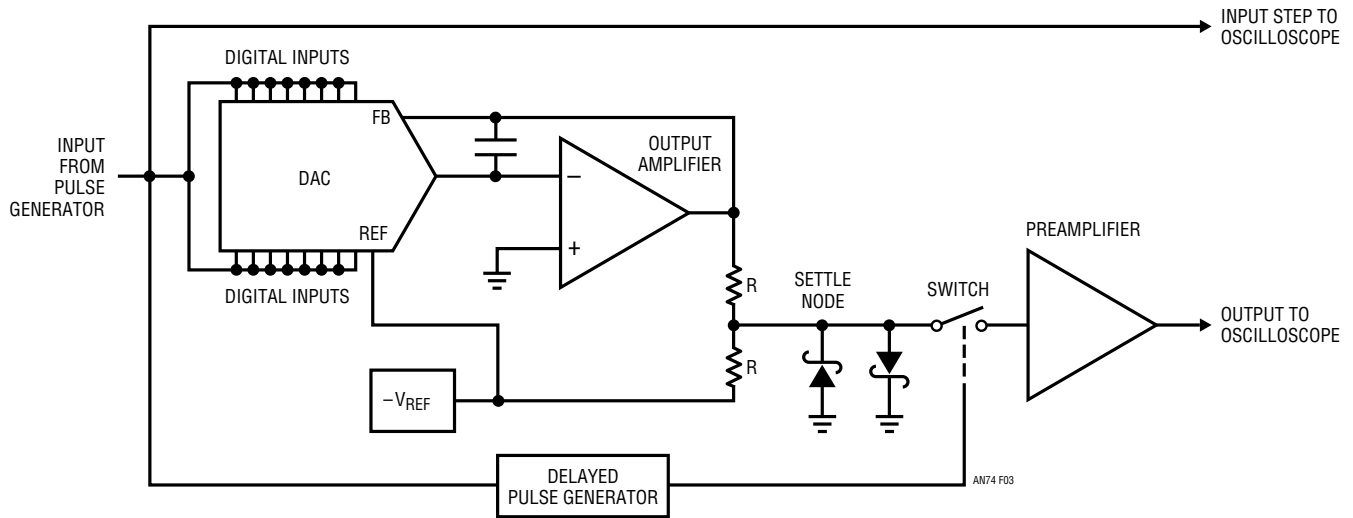


Figure 3. Conceptual Arrangement Eliminates Oscilloscope Overdrive. Delayed Pulse Generator Controls Switch, Preventing Oscilloscope from Monitoring Settle Node Until Settling is Nearly Complete

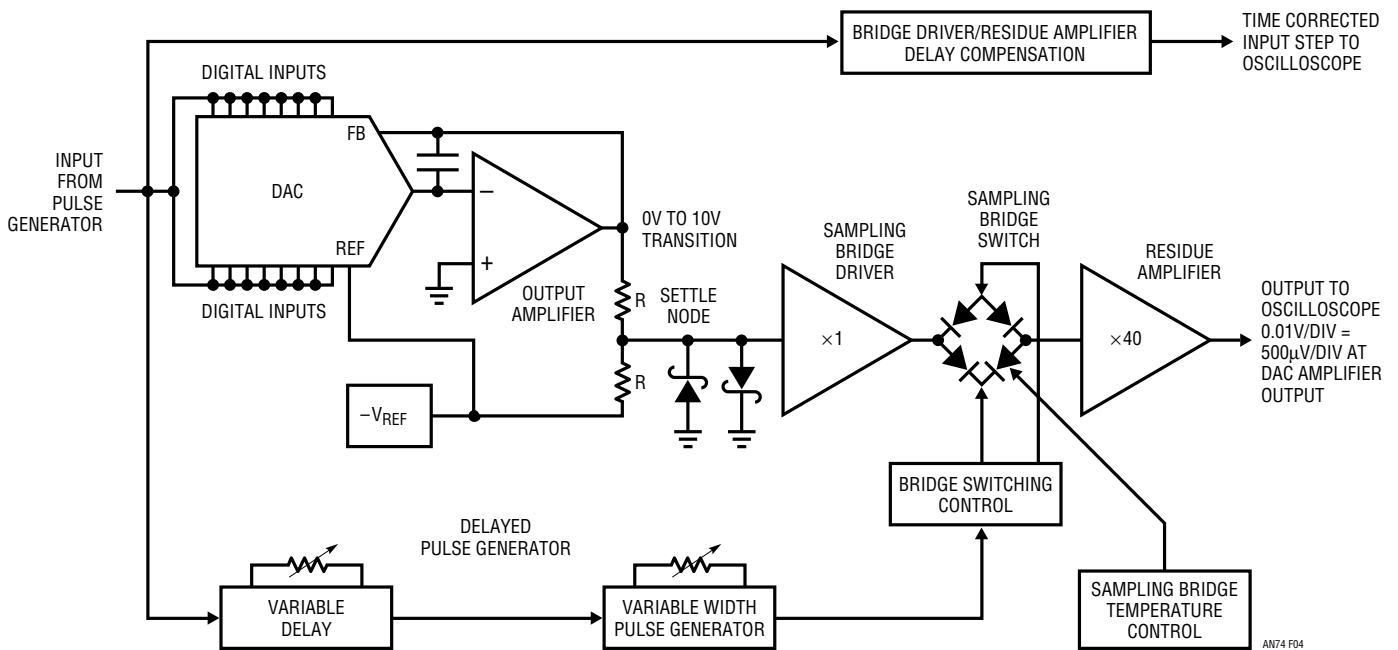


Figure 4. Block Diagram of DAC Settling Time Measurement Scheme. Diode Bridge Switch Minimizes Switching Feedthrough, Preventing Residue Amplifier-Oscilloscope Overdrive. Temperature Control Maintains 10µV Switch Offset Baseline. Input Step Time Reference is Compensated for ×1 and ×40 Amplifier Delays

Figure 4 is a more complete representation of the DAC settling time scheme. Figure 3's blocks appear in greater detail and some new refinements show up. The DAC-amplifier summing area is unchanged. Figure 3's delayed pulse generator has been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that

compensates for the propagation delay of the settling-time-measurement path. The most striking new aspect of the diagram is the diode bridge switch. Borrowed from classical sampling oscilloscope circuitry, it is the key to the measurement. The diode bridge's inherent balance eliminates charge injection based errors in the output. It is far superior to other electronic switches in this

characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt the oscilloscope display, inducing overload and defeating the switches purpose.

The diode bridge's balance, combined with matched, low capacitance monolithic diodes and complementary high speed switching, yields a cleanly switched output. The monolithic diode bridge is also temperature controlled, providing a bridge offset error below $10\mu\text{V}$, stabilizing the measurement baseline. The temperature control is implemented using uncommitted diodes in the monolithic array as heater and sensor.

Figure 5 details considerations for the diode bridge switch. The bridge diodes tend to cancel each other's temperature coefficient—unstabilized bridge drift is about $100\mu\text{V}/^\circ\text{C}$ and the temperature control reduces residual drift to a few microvolts/ $^\circ\text{C}$.

Bridge temperature control is achieved by using one diode as a sensor. Another diode, running in reverse breakdown ($V_Z \approx 7\text{V}$), serves as the heater. The control amplifier, comparing the sensor diode to a voltage at its negative terminal, drives the heater diode to temperature stabilize the array.

DC balance is achieved by trimming the bridge on-current for zero input-output offset voltage. Two AC trims are required. The “AC balance” corrects for diode and layout capacitive imbalances and the “skew compensation” corrects for any timing asymmetry in the nominally complementary bridge drive. These AC trims compensate small dynamic imbalances that could result in parasitic bridge outputs.

Detailed Settling Time Circuitry

Figure 6 is a detailed schematic of 16-bit DAC settling-time-measurement circuitry. The input pulse switches all DAC bits simultaneously and is also routed to the oscilloscope via a delay-compensation network. The delay network, composed of CMOS inverters and an adjustable RC network, compensates the oscilloscope's input step signal for the 12ns delay through the circuit's measurement path.⁵ The DAC amplifier's output is compared against the LT1236-10V reference via the precision 3k summing resistor ratio set. The LT1236 also furnishes the DAC reference, making the measurement ratiometric. The clamped settle node is unloaded by A1, which drives the sampling bridge. Note the additional clamp diodes at A1's output. These diodes prevent any possibility of abnormal A1 outputs (due to lost supply or supply sequencing

Note 5: See Appendix C, “Measuring and Compensating Residue Amplifier Delay.”

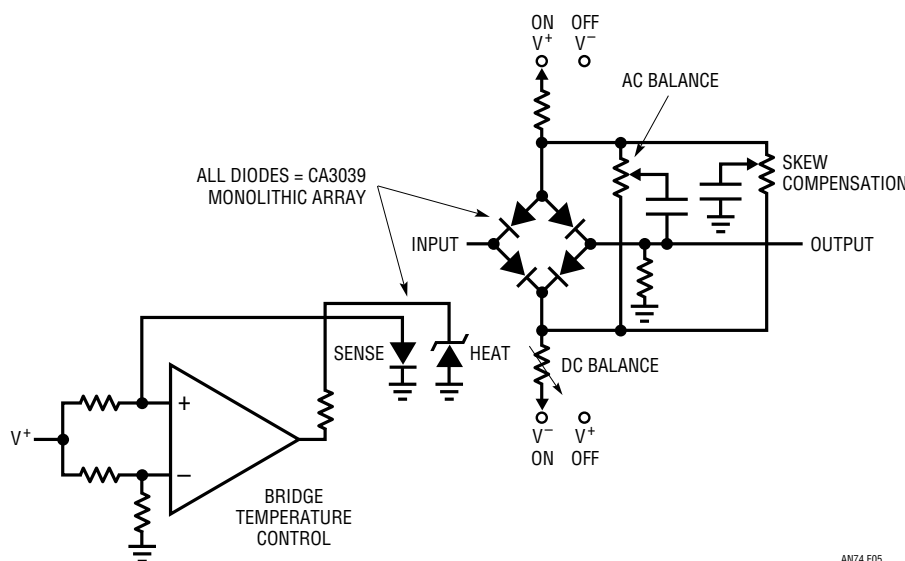


Figure 5. Diode Bridge Switch Trims Include AC and DC Balance and Switch Drive Timing Skew. Remaining Diodes in Monolithic Array are Used for Temperature Control

anomalies) from damaging the diode array.⁶ A3 and associated components temperature control the sampling diode bridge by comparing a diodes's forward drop to a stable potential derived from the -5V regulator. Another diode, operated in the reverse direction ($V_Z \approx 7V$) serves as a chip heater. The pin connections shown on the schematic have been selected to provide best temperature control performance.

The input pulse triggers the 74HC123 one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way the oscilloscope's output is reliable and meaningful data may be taken. The one shot's output is level shifted by the Q1-Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1-Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.⁷

A2 monitors the bridge output, provides gain and drives the oscilloscope. Figure 7 shows circuit waveforms. Trace A is the input pulse, trace B the DAC amplifier output, trace C the sample gate and trace D the residue amplifier output. When the sample gate goes low, the bridge switches cleanly, and the last 1.5mV of slew are easily observed. Ring time is also clearly visible, and the amplifier settles nicely to final value. When the sample gate goes high, the bridge switches off, with only 600µV of feedthrough. The

100µV peak before bridge switching (at ≈ 3.5 vertical divisions) is feedthrough from A1's output, but it is similarly well controlled. Note that there is no off-screen activity at any time—the oscilloscope is never subjected to overdrive.

The circuit requires trimming to achieve this level of performance. The bridge temperature control point is set by grounding Q5's base prior to applying power. Next, apply power and measure A3's positive input with respect to the -5V rail. Select the indicated resistor (1.5k nominal) for a voltage at A3's negative input (again, with respect to -5V) that is 57mV below the positive input's value. Unground Q5's base and the circuit will control the sampling bridge to about 55°C:

$$25^\circ\text{C room} + \frac{57\text{mV}}{1.9\text{mV}/^\circ\text{C diode drop}} = 30^\circ\text{C rise} = 55^\circ\text{C}$$

The DC and AC bridge trims are made once the temperature control is functional. Making these adjustments requires disabling the DAC and amplifier (disconnect the input pulse from the DAC and set all DAC inputs low) and shorting the settle node directly to the ground plane. Figure 8 shows typical results before trimming. Trace A is the input pulse, trace B the sample gate and trace C the residue amplifier output. With the DAC-amplifier disabled

Note 6: This can and did happen. The author was unfit for human companionship upon discovering this mishap. Replacing the sampling bridge was a lengthy and highly emotionally charged task. To see why, refer to Appendix G, "Breadboarding, Layout and Connection Techniques."

Note 7: The bridge switching scheme was developed at LTC by George Feliz.

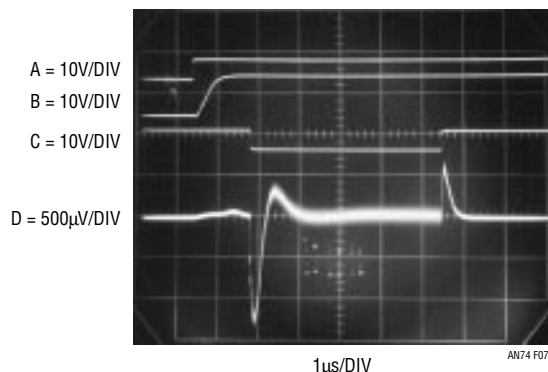


Figure 7. Settling Time Circuit Waveforms Include Time Corrected Input Pulse (Trace A), DAC Amplifier Output (Trace B), Sample Gate (Trace C) and Settling Time Output (Trace D). Sample Gate Window's Delay and Width are Variable

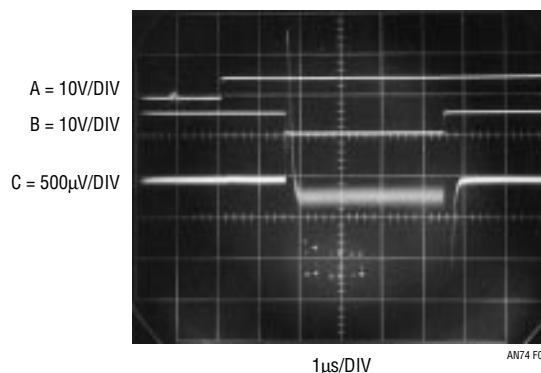


Figure 8. Settling Time Circuit's Output (Trace C) with Unadjusted Sampling Bridge AC and DC Trims. DAC is Disabled and Settle Node Grounded for This Test. Excessive Switch Drive Feedthrough and Baseline Offset are Present. Traces A and B are Input Pulse and Sample Window, Respectively

Application Note 74

and the settle node grounded, the residue amplifier output should (theoretically) always be zero. The photo shows this is not the case for an untrimmed bridge. AC and DC errors are present. The sample gate's transitions cause large, off-screen residue amplifier swings (note residue amplifier's response to the sample gate's turn-off at the ≈ 8.5 vertical division). Additionally, the residue amplifier output shows significant DC offset error during the sampling interval. Adjusting the AC balance and skew compensation minimizes the switching induced transients. The DC offset is adjusted out with the baseline zero trim. Figure 9 shows the results after making these adjustments. All switching related activity is now well on-screen and offset error reduced to unreadable levels. Once this level of performance has been achieved, the circuit is ready for use.⁸ Unground the settle node and restore the input pulse connection to the DAC.

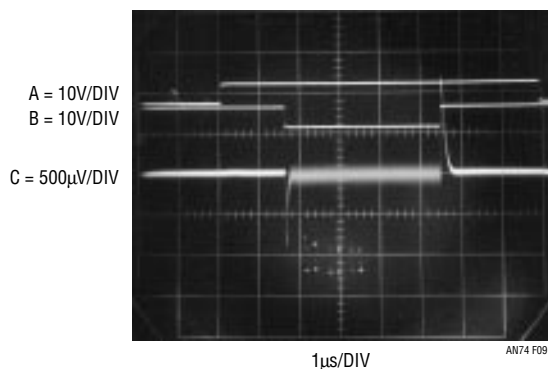


Figure 9. Settling Time Circuit's Output (Trace C) with Sampling Bridge Trimmed. As in Figure 8, DAC is Disabled and Settle Node Grounded for This Test. Switch Drive Feedthrough and Baseline Offset are Minimized. Traces A and B are Input Pulse and Sampling Gate, Respectively

Using the Sampling-Based Settling Time Circuit

Figures 10 through 12 underscore the importance of positioning the sampling window properly in time. In Figure 10 the sample gate delay initiates the sample window (trace A) too early and the residue amplifier's output (trace B) overdrives the oscilloscope when sampling commences. Figure 11 is better, with only slight off-screen activity. Figure 12 is optimal. All amplifier residue is well inside the screen boundaries.

Note 8: Achieving this level of performance also depends on layout. The circuit's construction involves a number of subtleties and is absolutely crucial. Please see Appendix G, "Breadboarding, Layout and Connection Techniques."

In general, it is good practice to "walk" the sampling window up to the last millivolt or so of amplifier slewing so that the onset of ring time is observable. The sampling based approach provides this capability and it is a very powerful measurement tool. Additionally, remember that

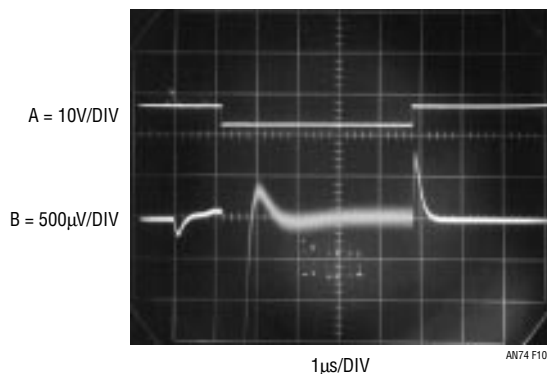


Figure 10. Oscilloscope Display with Inadequate Sample Gate Delay. Sample Window (Trace A) Occurs Too Early, Resulting in Off-Screen Activity in Settle Output (Trace B). Oscilloscope is Overdriven, Making Displayed Information Questionable

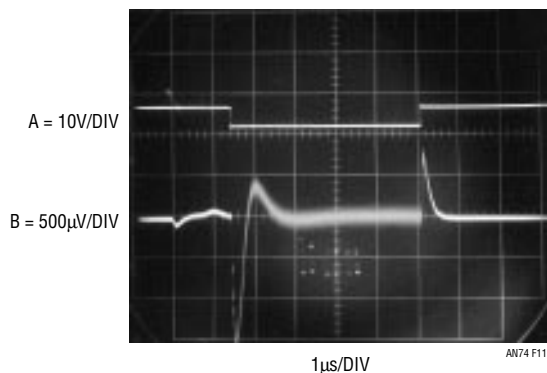


Figure 11. Increasing Sample Gate Delay Positions Sample Window (Trace A) So Settle Output (Trace B) Activity is On-Screen

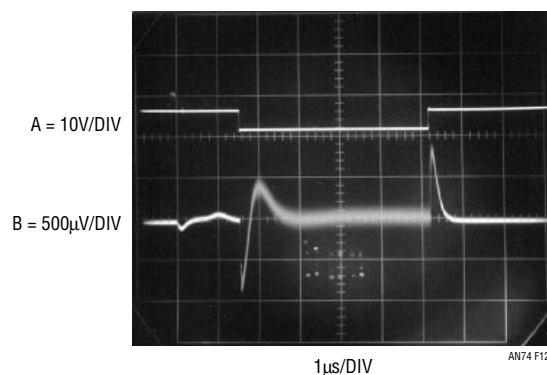


Figure 12. Optimal Sample Gate Delay Positions Sampling Window (Trace A) So All Settle Output (Trace B) Information is Well Inside Screen Boundaries

slower amplifiers may require extended delay and/or sampling window times. This may necessitate larger capacitor values in the 74H123 one-shot timing networks.

Compensation Capacitor Effects

The DAC amplifier requires frequency compensation to get the best possible settling time. The DAC has appreciable output capacitance, complicating amplifier response and making careful compensation capacitor selection even more important.⁹ Figure 13 shows effects of very light compensation. Trace A is the time corrected input pulse and trace B the residue amplifier output. The light compensation permits very fast slewing but excessive ringing amplitude over a protracted time results. The ringing is so severe that it feeds through during a portion of the sample gate off-period, although no overdrive results. When sampling is initiated (just prior to the sixth vertical division) the ringing is seen to be in its final stages, although still offensive. Total settling time is about 2.8 μ s. Figure 14 presents the opposite extreme. Here a large value compensation capacitor eliminates all ringing but slows down the amplifier so much that settling stretches out to 3.3 μ s. The best case appears in Figure 15. This photo was taken with the compensation capacitor carefully chosen for the best possible settling time. Damping is tightly controlled and settling time goes down to 1.7 μ s.

Note 9: This section discusses frequency compensation of the DAC amplifier within the context of sampling-based settling time measurement. As such, it is necessarily brief. Considerably more detail is available later in the text and in Appendix D, "Practical Considerations for DAC-Amplifier Compensation."

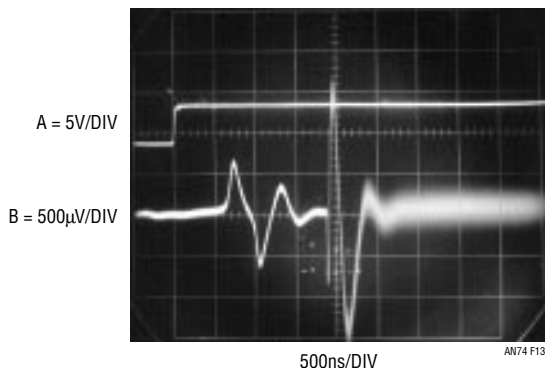


Figure 13. Settling Profile with Inadequate Feedback Capacitance Shows Underdamped Response. Excessive Ringing Feeds Through During Sample Gate Off-Period (Second Through \approx Sixth Vertical Divisions) But is Tolerable. $t_{SETTLE} = 2.8\mu$ s

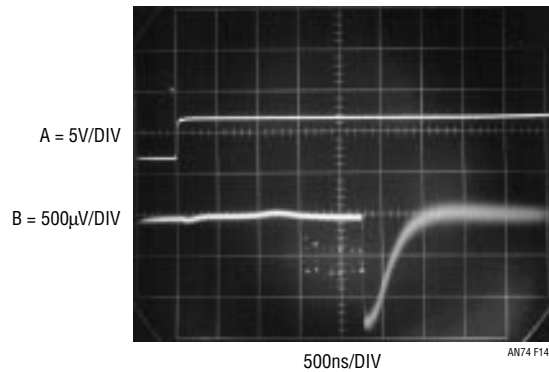


Figure 14. Excessive Feedback Capacitance Overdamps Response. $t_{SETTLE} = 3.3\mu$ s

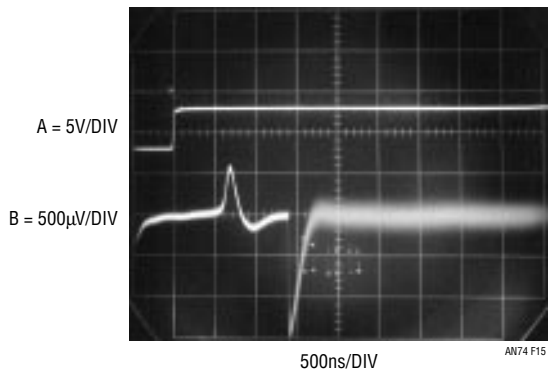


Figure 15. Optimal Feedback Capacitance Yields Tightly Damped Signature and Best Settling Time. $t_{SETTLE} = 1.7\mu$ s

Verifying Results—Alternate Methods

The sampling-based settling time circuit appears to be a useful measurement solution. How can its results be tested to ensure confidence? A good way is to make the same measurement with alternate methods and see if results agree. To begin this exercise we return to the basic diode-bounded settle circuit.

Figure 16 repeats Figure 2's basic settling time measurement, with the same problem. The Schottky-bounded settle node forces a 400mV overdrive to the oscilloscope,

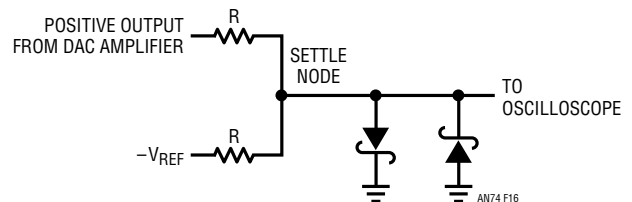


Figure 16. Clamped Settle Node Permits Oscilloscope Overdrive Because Diodes Have 400mV Drop

Application Note 74

rendering all measurements useless. Now, consider Figure 17. This arrangement is similar, but the diodes are returned to bias voltages that are slightly lower than the diode drops. Theoretically, this has the same effect as ground-referred diodes with an inherently lower forward drop, greatly reducing oscilloscope overdrive. In practice, diode V-I characteristics and temperature effects limit achievable performance to uninteresting levels. Clamping reduction is minimal and diode forward leakage when the settle node reaches zero causes signal amplitude errors. Although impractical, this approach does hint at the way to a more useful method.

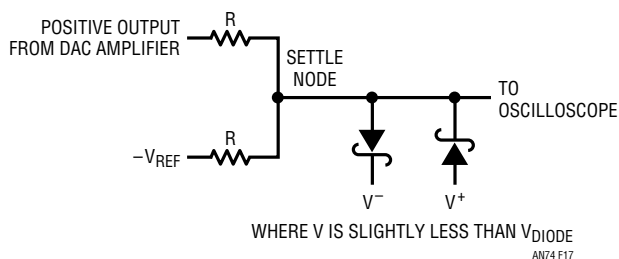


Figure 17. Biasing Diodes Theoretically Lowers Clamp Voltage. In Practice, V-I Characteristics and Temperature Effects Limit Performance

Alternate Method I—Bootstrapped Clamp

Figure 18's approach returns the diodes to amplifier-generated voltages bootstrapped from the settle-node input signal. In this way, the diode bias is actively maintained at the optimum point with respect to the signal to be clamped.

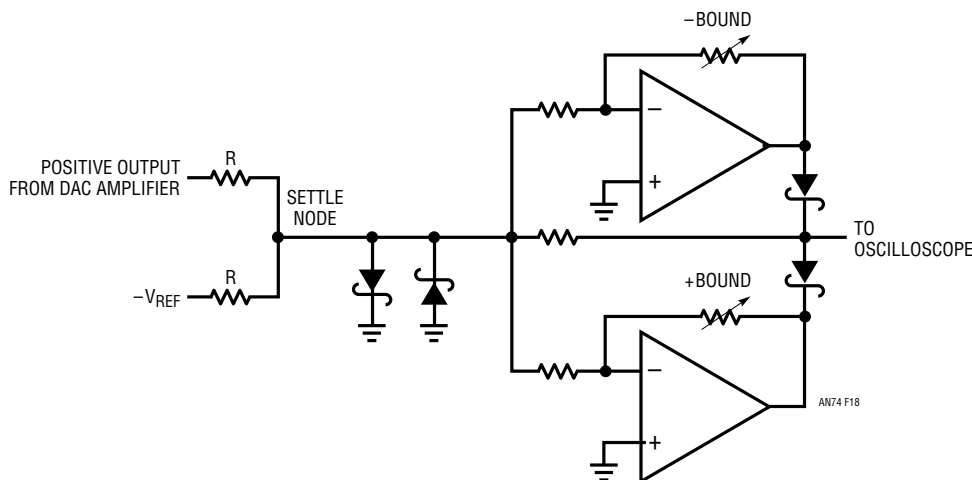


Figure 18. Conceptual Bootstrapped Clamp Biases Diodes From Input Signal, Minimizing Effects of V-I Characteristics and Temperature.

During DAC amplifier slew, the settle-node signal is large and the amplifiers supply a resultant large bias to the diodes, forcing the desired small clamp voltage. When the DAC amplifier comes out of slew, the settle-node signal very nearly approaches zero, the amplifiers supply almost no diode bias and the oscilloscope monitors the uncorrupted settle node output. Adjustable amplifier gains permit optimal setting of positive and negative bound limits. This scheme offers the possibility of minimizing oscilloscope overdrive while preserving signal-path integrity.

A practical bootstrapped clamp appears in Figure 19. The actual clamp circuit, composed of A3 and A4, is nearly identical to the previous figure's theoretical incarnation. A1 and A2 are added, supplying a nonsaturating gain of 80 to the clamp. This permits a $500\mu\text{V}/\text{DIV}$ oscilloscope scale factor with respect to the DAC amplifier output. In Figure 20 the amplifier-bound voltages are set equal to the diode drops, and bootstrapping does not occur. The response is essentially identical to that of a simple diode clamp. In Figure 21 A4's gain is adjusted, reducing the positive clamp excursion. A3's gain is similarly trimmed in Figure 22, producing a corresponding reduction in the negative clamp limit. Note that in both photos, the small amplitude settle signal waveform (beginning about the fifth vertical division) is unaffected. Further refinement of the positive and negative trims produces Figure 23. The trims are optimized for minimal peak-to-peak amplitude while maintaining settle-signal waveform fidelity. This permits an oscilloscope running at $20\text{mV}/\text{DIV}$ ($500\mu\text{V}$ at the DAC

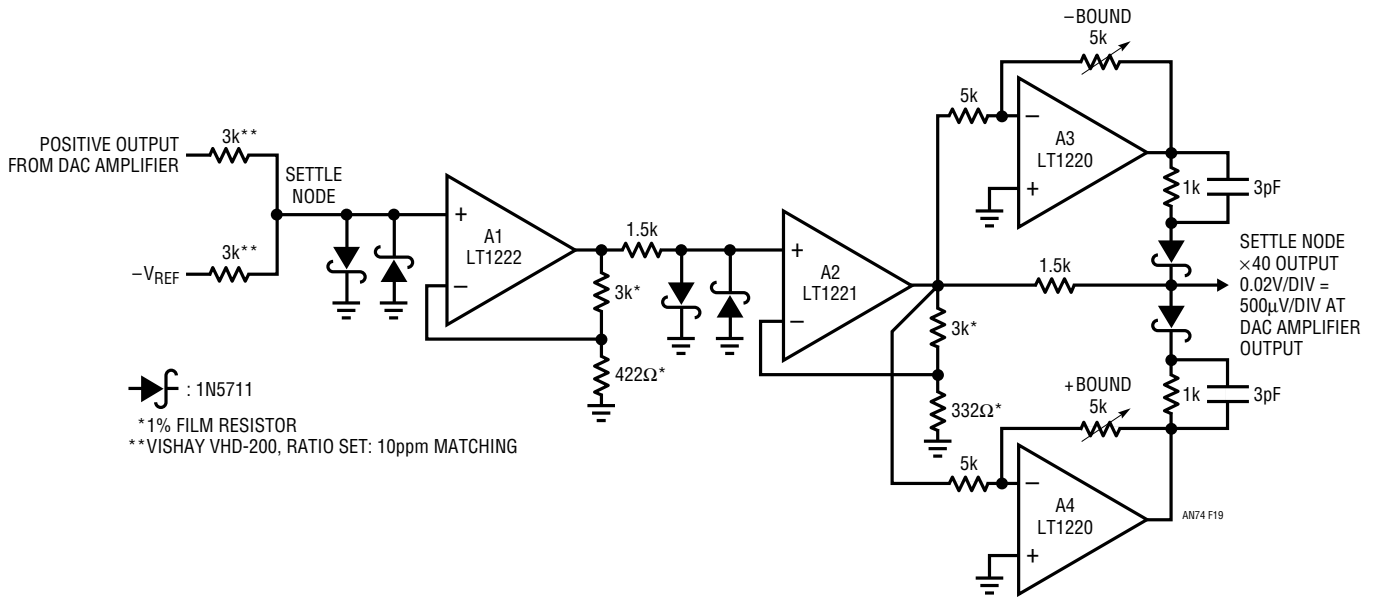


Figure 19. A Practical Bootstrapped Clamp. A1 and A2 Provide Gain to Bootstrapped Section. Positive and Negative Bounds are Adjustable

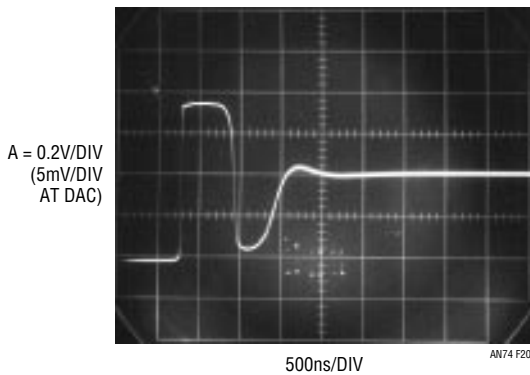


Figure 20. Bootstrapped Clamp Waveform with Bound Limits Equal to Diode Drops. Bootstrap Action Does Not Occur. Response is Identical to Diode Clamp

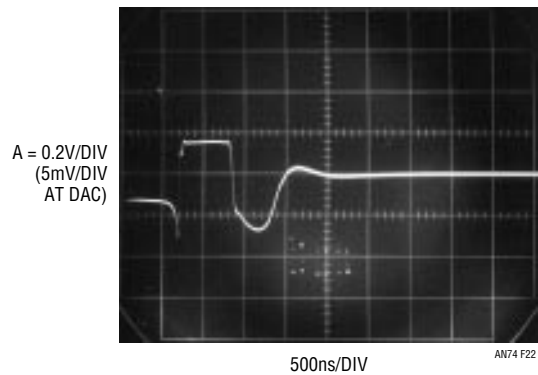


Figure 22. The Negative Bound is Trimmed, Reducing Negative Clamp Limit

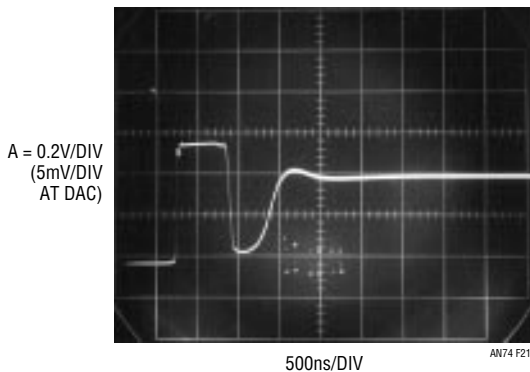


Figure 21. The Positive Bound is Adjusted, Reducing Positive Clamp Excursion

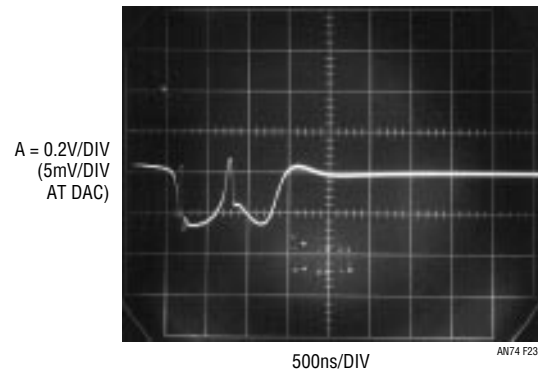


Figure 23. Positive and Negative Bound Adjustments are Optimized for Minimal Peak-to-Peak Amplitude. Waveform Information in Settling Region (Right of Fourth Vertical Division) is Undistorted and Identical to Figure 20

Application Note 74

amplifier) to monitor the settle signal with only a 2.5× overdrive. This is not as ideal a situation as the sampling approach, which has no overdrive, but is markedly improved over the simple diode clamp. The monitoring oscilloscope selected must be verified to produce reliable displays while withstanding the 2.5× overdrive.¹⁰

Figure 24 shows the bootstrapped clamp adapted to Figure 6’s settling-time test circuit. The settle node feeds

the residue amplifier, which drives the bootstrapped clamp. As before, the input pulse is time corrected for signal path delays.¹¹ Additionally, similar type FET probes at the outputs ensure overall delay matching.¹² Figure 25 shows the results. Trace A is the time-corrected input step and trace B the settle signal. The oscilloscope undergoes about a 2.5× overdrive, although the settling signal appears undistorted.

Note 10: This limitation is surmountable by improving the bootstrapped clamp’s dynamic operating range. Future work will be directed towards this end. For the present, the following oscilloscopes have been found to produce faithful results under the 2.5× overdrive conditions noted in the text. The instruments include Tektronix types 547 and 556 (type 1A1 or 1A4 plug-in) and types 453, 454, 453A and 454A. See also Appendix B, “Evaluating Oscilloscope Overload Performance.”

Note 11: Characterization of signal path delay is treated in Appendix C, “Measuring and Compensating Residue Amplifier Delay.”

Note 12: The bootstrapped clamp’s output impedance mandates a FET probe. A second FET probe monitors the input step, but only to maintain channel delay matching.

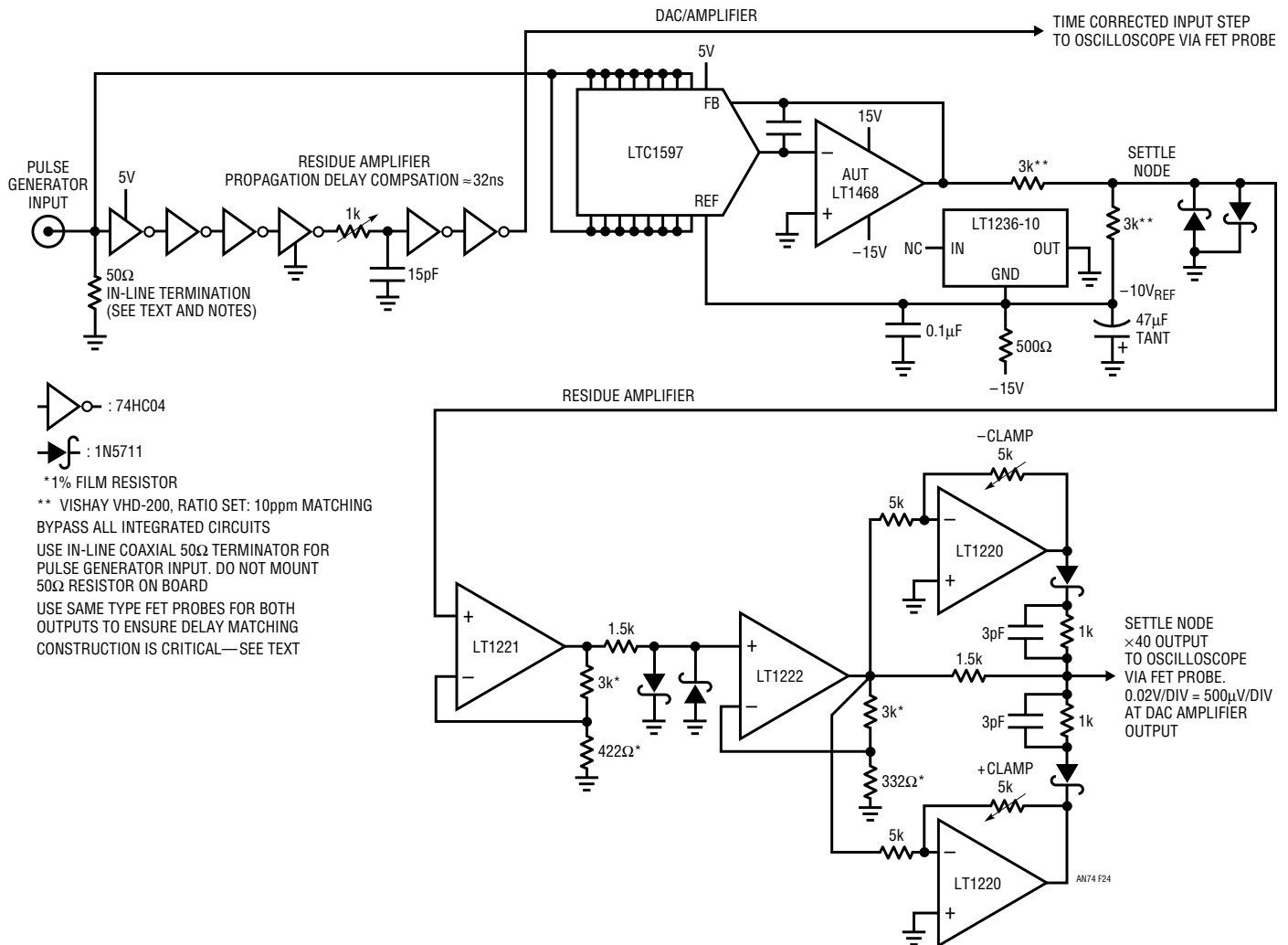


Figure 24. Complete Bootstrapped Clamp-Based DAC Settling Time Measurement Circuit. Overdrive is Substantially Reduced Over Conventional Diode Clamp, But Oscilloscope Must Tolerate ≈2.5× Screen Overdrive

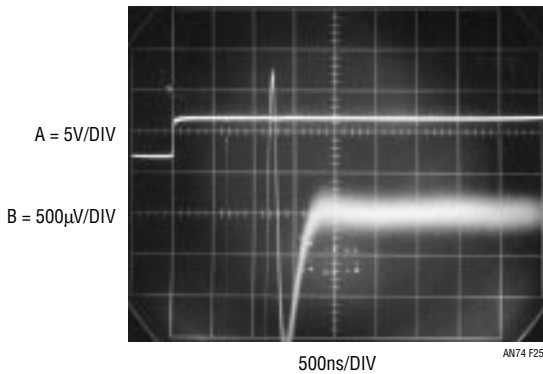


Figure 25. The Bootstrapped Clamp-Amplifier Measuring Settling Time. Oscilloscope Must Tolerate 2.5× Screen Overdrive for Meaningful Results

Alternate Method II—Sampling Oscilloscope

It was stated earlier that classical sampling oscilloscopes were inherently immune to overdrive.¹³ If this is so, why not utilize this feature and attempt settling time measurement with a simple diode clamp? Figure 26 does this. The schematic is identical to Figure 24 except that the bootstrapped clamp has been replaced with a simple diode clamp. Under these conditions the sampling ‘scope¹⁴ is

heavily overdriven, but is ostensibly immune to the insult. Figure 27 puts the sampling oscilloscope to the test. Trace A is the time corrected input pulse and trace B the settle signal. Despite a brutal overdrive, the ‘scope appears to respond cleanly, giving a very plausible settle signal presentation.

Note 13: See Appendix B, “Evaluating Oscilloscope Overdrive Performance,” for in-depth discussion.

Note 14: Tektronix type 661 with 4S1 vertical and 5T3 timing plug-ins.

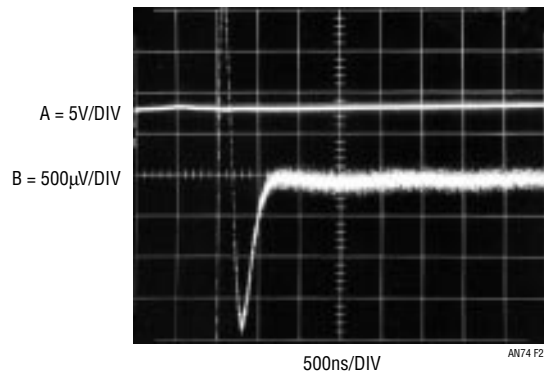


Figure 27. DAC Settling Time Measurement with the Classical Sampling ‘Scope. Oscilloscope’s Overload Immunity Permits Accurate Measurement Despite Extreme Overdrive

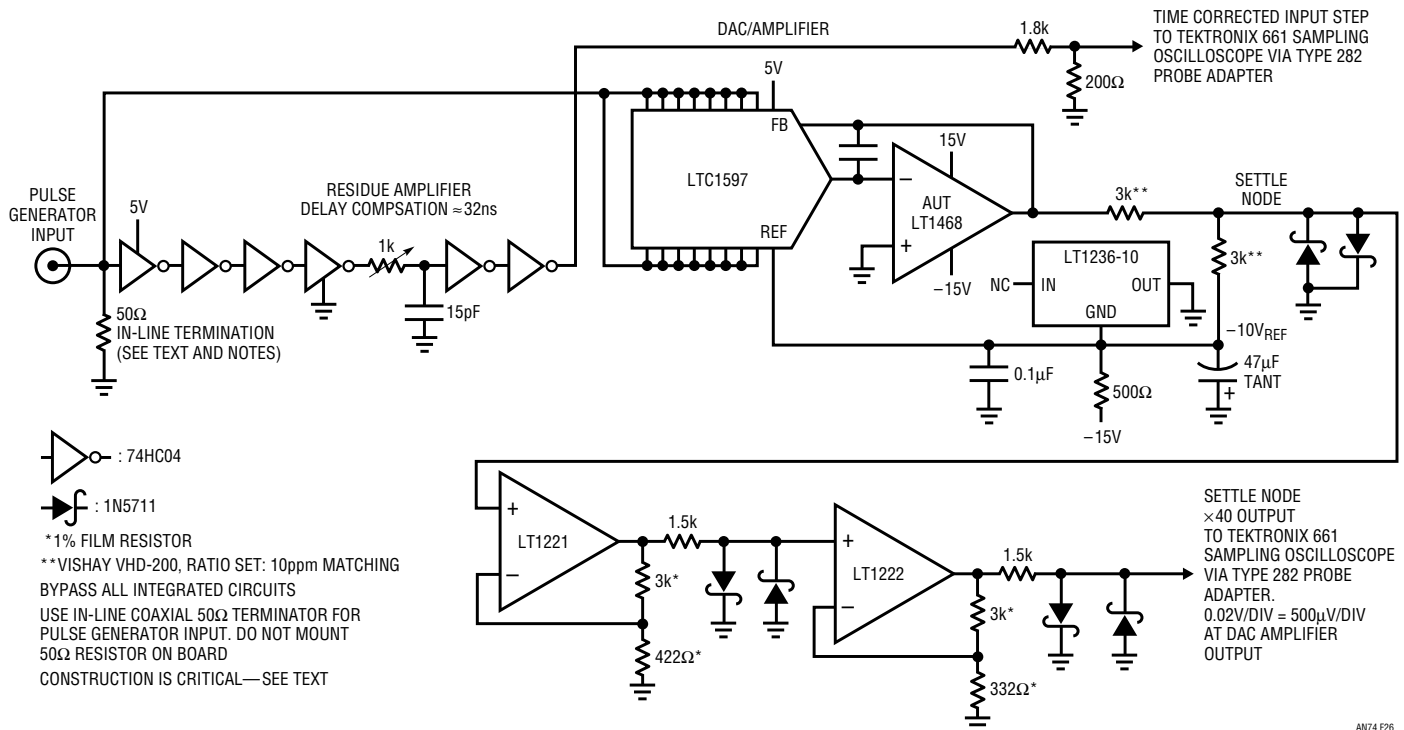


Figure 26. DAC Settling Time Test Circuit Using Classical Sampling Oscilloscope. Circuit is Similar to Figure 24. Sampling ‘Scope’s Inherent Overload Immunity Eliminates Bootstrapped Clamp Requirement

Application Note 74

Alternate Method III—Differential Amplifier

In theory, a differential amplifier with one input biased at the expected settled voltage can measure settling time to 16-bit resolution. In practice, this is an extraordinarily demanding measurement for a differential amplifier. The amplifier's overload recovery characteristics must be pristine. In fact, no commercially produced differential amplifier or differential oscilloscope plug-in has been available that meets this requirement. Recently, an instrument has appeared that, although not fully specified at these levels, appears to have superb overload recovery performance. Figure 28 shows the differential amplifier (type and manufacturer appear in the schematic notes) monitoring the DAC output amplifier. The amplifier's negative input is biased from its internal adjustable reference to the expected settled voltage. The diff. amp's clamped output, operating at a gain of 10, feeds A1-A2, a bounded, nonsaturating gain of 40. Note that the monitoring oscilloscope, operating at 0.2V/DIV (500 μ V/DIV at the DAC amplifier) cannot be overdriven. Figure 29 shows the

results. Trace A is the time corrected input step and trace B the settle signal. The settle signal is seen to come smoothly out of bound, entering the amplified linear region between the third and fourth vertical divisions. The settling signature appears reasonable and complete settling occurs just beyond the fourth vertical division.

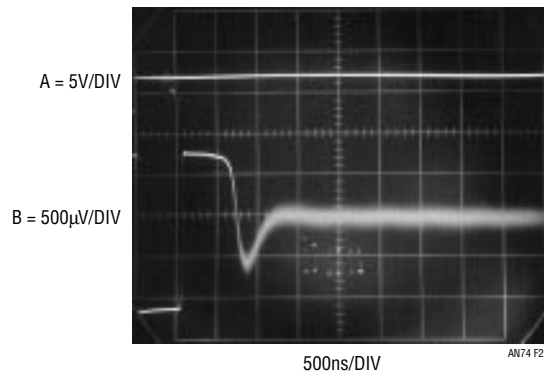


Figure 29. DAC Settling Time Measurement with the Differential/Clamped Amplifiers. All Oscilloscope Input Signal Excursions are On-Screen.

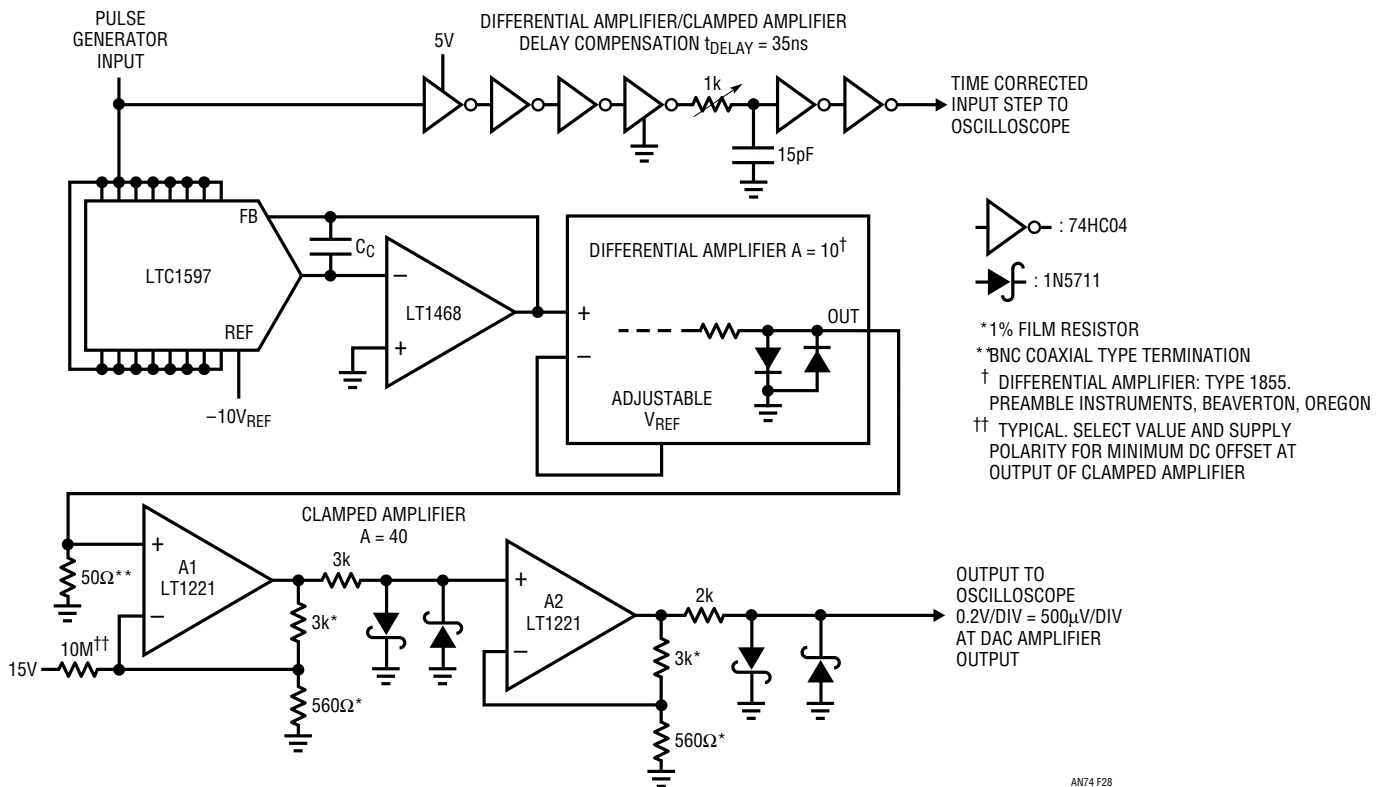


Figure 28. Settling Time Measurement Using a Differential Amplifier. Amplifier Must Have Excellent Input Overload Recovery. Clamped Amplifier's Bounded Gain Stages Limit Amplitude While Maintaining Linear Region Operation. Oscilloscope is Not Overdriven

Summary of Results

The simplest way to summarize the four different method's results is by visual comparison. Figures 30 through 33 repeat previous photos of the four different settling-time methods. If all four approaches represent good measurement technique and are constructed properly, results should be identical.¹⁵ If this is the case, the identical data produced by the four methods has a high probability of being valid.

Examination of the four photographs shows identical 1.7 μ s settling times and settling waveform signatures. The shape of the settling waveform, in every detail, is identical in all four photos. This kind of agreement provides a high degree of credibility to the measured results. It also provides the confidence necessary to characterize a wide variety of amplifiers. Figure 34 lists various LTC amplifiers and their measured settling times to 16 bits.

About This Chart

The writer despises charts. In their attempt to gain authority they simplify, and glib simplification is the host of mother nature's surprise party. Any topic as complex as DAC-amplifier settling time to 16 bits is a dangerous place for oversimplification. There are simply too many variables and exceptions to accommodate the categorical statement a chart implies. It is with these reservations that Figure 34 is presented.¹⁶ The chart lists measured settling times to 16 bits for various LTC amplifiers used with the LTC1595-7 16-bit DACs. A number of conditions and comments apply to interpreting the chart's information.

Note 15: Construction details of the settling time fixtures discussed here appear (literally) in Appendix G, "Breadboarding, Layout and Connection Techniques."

Note 16: Readers detecting author ambivalence about the inclusion of Figure 34's chart are not hallucinating.

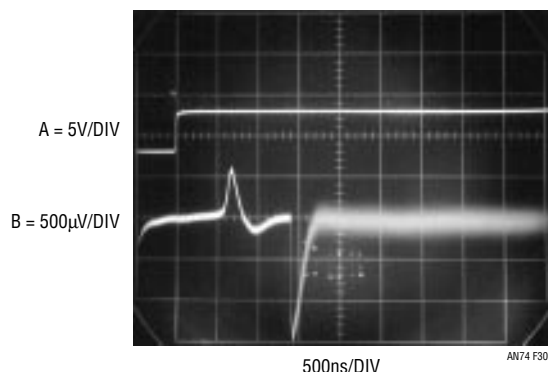


Figure 30. DAC Settling Time Measurement Using the Sampling Bridge Circuit. $t_{SETTLE} = 1.7\mu s$

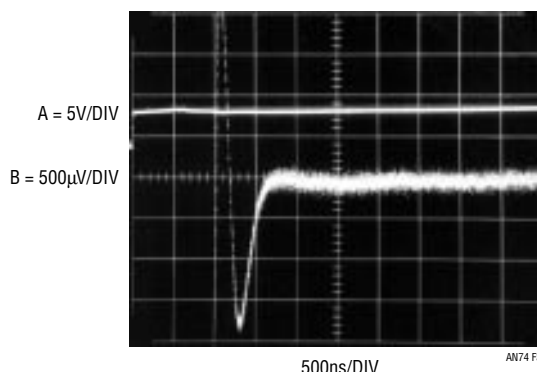


Figure 32. DAC Settling Time Measurement Using the Classical Sampling 'Scope. $t_{SETTLE} = 1.7\mu s$

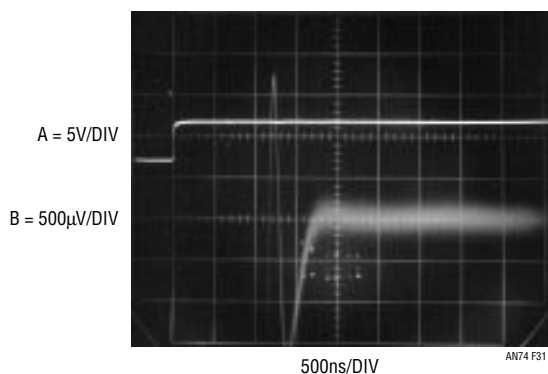


Figure 31. DAC Settling Time Measurement with the Bootstrapped Clamp Method. $t_{SETTLE} = 1.7\mu s$

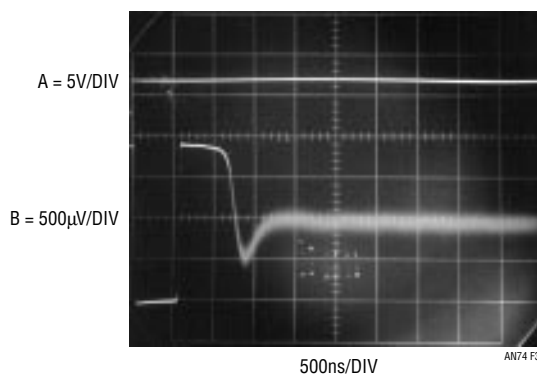


Figure 33. DAC Settling Time Measurement with the Differential Amplifier. $t_{SETTLE} = 1.7\mu s$

DAC Settling Time Measurement Using Four Different Methods. Waveform Signatures and Settling Times Appear Identical

Application Note 74

AMPLIFIER	OPTIMIZED SETTLING TIME AND TYPICAL COMPENSATION VALUE		CONSERVATIVE SETTLING TIME AND COMPENSATION VALUE		COMMENTS
LT1001	65μs	100pF	120μs	100pF	Good Low Speed Choice
LT1006	26μs	66pF	50μs	150pF	
LT1007	17μs	100pF	19μs	100pF	I _B Gives ≈1LSB Error at 25°C
LT1008	64μs	100pF	115μs	100pF	
LT1012	56μs	75pF	116μs	75pF	Good Low Speed Choice
LT1013	50μs	150pF	75μs	150pF	≈1LSB Error Due to V _{OS} over Temperature
LT1055	3.7μs	54pF	5μs	75pF	V _{OS} Gives ≈2 to 3LSB Error over Temperature
LT1077	110μs	100pF	200μs	100pF	
LT1097	60μs	75pF	120μs	75pF	Good Low Speed Choice
LT1122	3μs	51pF	3.5μs	68pF	V _{OS} Induced Errors
LTC1150	7ms	100pF	10ms	100pF	Special Case. See Appendix E. Needs Output Booster, e.g., LT1010
LT1178	330μs	100pF	450μs	100pF	
LT1179	330μs	100pF	450μs	100pF	
LT1211	5.5μs	73pF	6.5μs	82pF	I _B and V _{OS} Based Errors
LT1213	4.6μs	58pF	5.8μs	68pF	I _B and V _{OS} Based Errors
LT1215	3.6μs	53pF	4.7μs	68pF	I _B and V _{OS} Based Errors
LT1218	110μs	100pF	200μs	100pF	≈1.5LSB Error Due to V _{OS} . ≈4 to 5LSB I _B Based Errors
LT1220	2.3μs	41pF	3.1μs	56pF	V _{OS} and I _B Based Errors
LT1366	64μs	100pF	100μs	150pF	V _{OS} and I _B Based Errors
LT1413	45μs	100pF	75μs	120pF	≈2LSB Error Due to V _{OS}
LT1457	7.4μs	100pF	12μs	120pF	5 to 6LSB Error From V _{OS} over Temperature
LT1462	78μs	100pF	130μs	120pF	7 to 8LSB Error Due to V _{OS} over Temperature
LT1464	19μs	90pF	30μs	110pF	See LT1462 Comments Above
LT1468	1.7μs	20pF	2.5μs	30pF	Fastest Settling with 16-Bit Performance
LT1490	175μs	100pF	300μs	100pF	V _{OS} Based Errors
LT1492	7.5μs	80pF	10μs	100pF	V _{OS} and I _B Based Errors
LT1495	10ms	100pF	25ms	100pF	Measured with Hourglass and Differential Voltmeter. Needs Output Booster, e.g., LT1010
LT1498	5μs	60pF	7.3μs	82pF	V _{OS} and I _B Based Errors
LT1630	4.5μs	63pF	6.7μs	82pF	Significant I _B Based Error
LT1632	4μs	55pF	5.2μs	68pF	Significant I _B Based Error
LTC1650	6μs		7.3μs		DAC On-Board. ±4V Step. ≈10LSB V _{OS} Related Error Over Temperature
LT2178	330μs	100pF	450μs	100pF	1 to 2LSB V _{OS} Based Error

Figure 34. 16-Bit Settling Time for Various Amplifiers Driven by the LT1597 DAC. Optimized Settling Times Require Trimming Compensation Capacitor, Conservative Times are Untrimmed. LT1468 (Shaded) Offers Fastest Settling Time While Maintaining Accuracy Over Temperature

The amplifiers selected are not all accurate to 16 bits over temperature, or (in some cases) even at 25°C. However, many applications, such as AC signal processing, servo loops or waveform generation, are insensitive to DC offset error and, as such, these amplifiers are worthy candidates. Applications requiring DC accuracy to 16 bits (10V full scale) must keep input errors below 15nA and 152 μ V to maintain performance.

The settling times are quoted for “optimized” and “conservative” cases. The optimized case uses a typical amplifier-DAC combination. This implies “design centered” values for amplifier slew rate and DAC output resistance and capacitance. It also permits trimming the amplifier’s feedback capacitor to obtain the best possible settling time. The conservative category assumes worst-case amplifier slew rate, highest DAC output impedances and untrimmed, standard 5% feedback capacitors. This worst-case error summation is perhaps unduly pessimistic; RMS summing may represent a more realistic compromise. However, such a maudlin outlook helps avoid unpleasant surprises in production. Settling times are quoted using ± 15 V supplies, a -10 V DAC reference and a 10V positive output step. The sole exception to this is the LTC1650, a 16-bit DAC with amplifier onboard. This device is powered by ± 5 V supplies and settling is measured with a 4V reference and a ± 4 V swing.¹⁷ All feedback capacitances listed were determined with a General Radio model 1422-CL precision variable air capacitor.¹⁸

In general, the slower amplifiers’ extended slew times make their ring times vanishingly small settling-time contributors. This is reflected in identical feedback capacitor values for the optimized and conservative cases. Conversely, faster amplifiers’ ring times are significant terms, resulting in different compensation values for the two categories. Additional considerations for compensation are discussed in Appendix D, “Practical Considerations for DAC-Amplifier Compensation.”

Note 17: See Appendix F, “Settling Time Measurement of Serially Loaded DACs.”

Note 18: A thing of transcendent beauty. It is worth owning this instrument just to look at it. It is difficult to believe humanity could fashion anything so perfectly gorgeous.

Thermally Induced Settling Errors

A final category of settling-time error is thermally based. Some poorly designed amplifiers exhibit a substantial “thermal tail” after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking settling at high speed it is always a good idea to slow the oscilloscope sweep down and look for thermal tails. Figure 35 shows such a tail. The amplifier slowly (note horizontal sweep speed) drifts 200 μ V after settling has apparently occurred. Often, the thermal tail’s effect can be accentuated by loading the amplifier’s output. Figure 36 doubles the error by increasing amplifier loading.

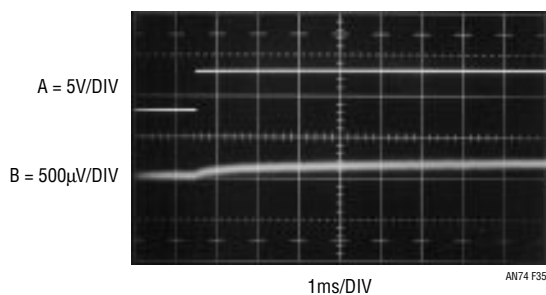


Figure 35. Typical Thermal Tail in a Poorly Designed Amplifier. Device Drifts 200 μ V (>1LSB) After Settling Apparently Occurs

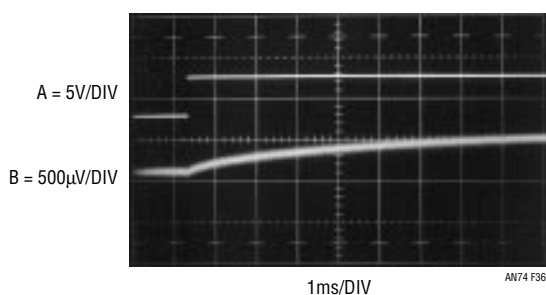


Figure 36. Loading the Amplifier Increases Thermal Tail Error to 400 μ V (>2.5LSB)

Application Note 74

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APPENDIX A

A HISTORY OF HIGH ACCURACY
DIGITAL-TO-ANALOG CONVERSION

People have been converting digital-to-analog quantities for a long time. Probably among the earliest uses was the summing of calibrated weights (Figure A1, left center) in weighing applications. Early electrical digital-to-analog conversion inevitably involved switches and resistors of different values, usually arranged in decades. The application was often the calibrated balancing of a bridge or reading, via null detection, some unknown voltage. The most accurate resistor-based DAC of this type is Lord Kelvin's Kelvin-Varley divider (Figure, large box). Based on switched resistor ratios, it can achieve ratio accuracies of 0.1ppm (23+ bits) and is still widely employed in standards laboratories. High speed digital-to-analog conversion resorts to electronically switching the resistor network. Early electronic DACs were built at the board level using discrete precision resistors and germanium transistors (Figure, center foreground, is a 12-bit DAC from a

Minuteman missile D-17B inertial navigation system, circa 1962). The first electronically switched DACs available as standard product were probably those produced by Pastoriza Electronics in the mid 1960s. Other manufacturers followed and discrete- and monolithically-based modular DACs (Figure, right and left) became popular by the 1970s. The units were often potted (Figure, left) for ruggedness, performance or to (hopefully) preserve proprietary knowledge. Hybrid technology produced smaller package size (Figure, left foreground). The development of Si-Chrome resistors permitted precision monolithic DACs such as the LTC1595 (Figure, immediate foreground). In keeping with all things monolithic, the cost-performance trade off of modern high resolution IC DACs is a bargain. Think of it! A 16-bit DAC in an 8-pin IC package. What Lord Kelvin would have given for a credit card and LTC's phone number.

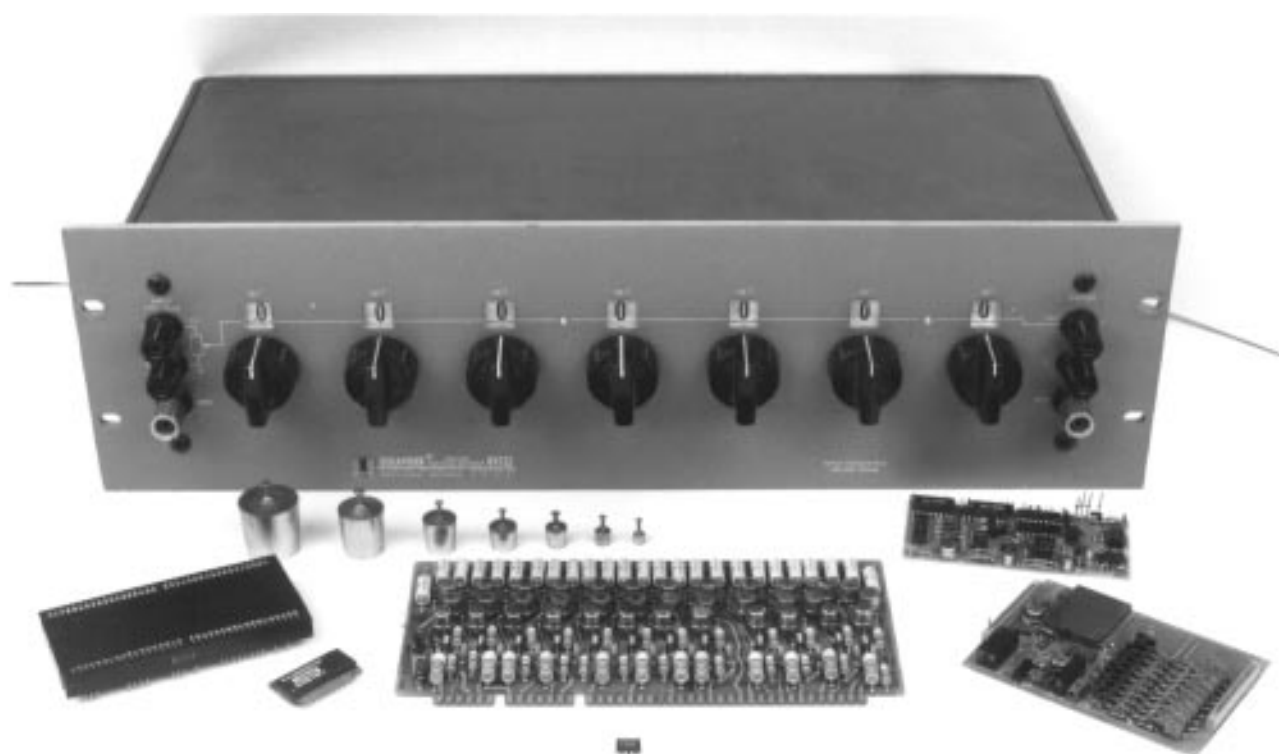


Figure A1. Historically Significant Digital-to-Analog Converters Include: Weight Set (Center Left), 23+ Bit Kelvin-Varley Divider (Large Box), Hybrid, Board and Modular Types, and the LTC1595 IC (Foreground). Where Will It All End?

APPENDIX B

EVALUATING OSCILLOSCOPE OVERDRIVE PERFORMANCE

Most of the settling-time circuits are heavily oriented towards providing little or no overdrive to the monitoring oscilloscope. This is done to avoid overdriving the oscilloscope. Oscilloscope recovery from overdrive is a grey area and almost never specified. Some of the settling time measurement methods require the oscilloscope to be overdriven. In these cases, the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overdrive before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overdrive, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overdrive varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100× overload at 0.005V/DIV may be very different than at 0.1V/DIV. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overdrive must be approached with caution.

Why do most oscilloscopes have so much trouble recovering from overdrive? The answer to this question requires some study of the three basic oscilloscope types' vertical paths. The types include analog (Figure B1A), digital (Figure B1B) and classical sampling (Figure B1C) oscilloscopes. Analog and digital 'scopes are susceptible to overdrive. The classical sampling 'scope is the only architecture that is inherently immune to overdrive.

An analog oscilloscope (Figure B1A) is a real time, continuous linear system.¹ The input is applied to an attenuator, which is unloaded by a wideband buffer. The vertical preamp provides gain, and drives the trigger pick-off, delay line and the vertical output amplifier. The attenuator and delay line are passive elements and require little comment. The buffer, preamp and vertical output amplifier are complex linear gain blocks, each with dynamic operating range restrictions. Additionally, the operating point of each block may be set by inherent circuit balance, low frequency stabilization paths or both. When the input is overdriven, one or more of these stages may saturate,

forcing internal nodes and components to abnormal operating points and temperatures. When the overload ceases, full recovery of the electronic and thermal time constants may require surprising lengths of time.²

The digital sampling oscilloscope (Figure B1B) eliminates the vertical output amplifier, but has an attenuator buffer and amplifiers ahead of the A/D converter. Because of this, it is similarly susceptible to overdrive recovery problems.

The classical sampling oscilloscope is unique. Its nature of operation makes it inherently immune to overload. Figure B1C shows why. The sampling occurs *before* any gain is taken in the system. Unlike Figure B1B's digitally sampled 'scope, the input is fully passive to the sampling point. Additionally, the output is fed back to the sampling bridge, maintaining its operating point over a very wide range of inputs. The dynamic swing available to maintain the bridge output is large and easily accommodates a wide range of oscilloscope inputs. Because of all this, the amplifiers in this instrument do not see overload, even at 1000× overdrives, and there is no recovery problem. Additional immunity derives from the instrument's relatively slow sample rate—even if the amplifiers were overloaded, they would have plenty of time to recover between samples.³

The designers of classical sampling 'scopes capitalized on the overdrive immunity by including variable DC offset generators to bias the feedback loop (see Figure B1C, lower right). This permits the user to offset a large input, so small amplitude activity on top of the signal can be accurately observed. This is ideal for, among other things, settling time measurements. Unfortunately, classical sampling oscilloscopes are no longer manufactured, so if you have one, take care of it!

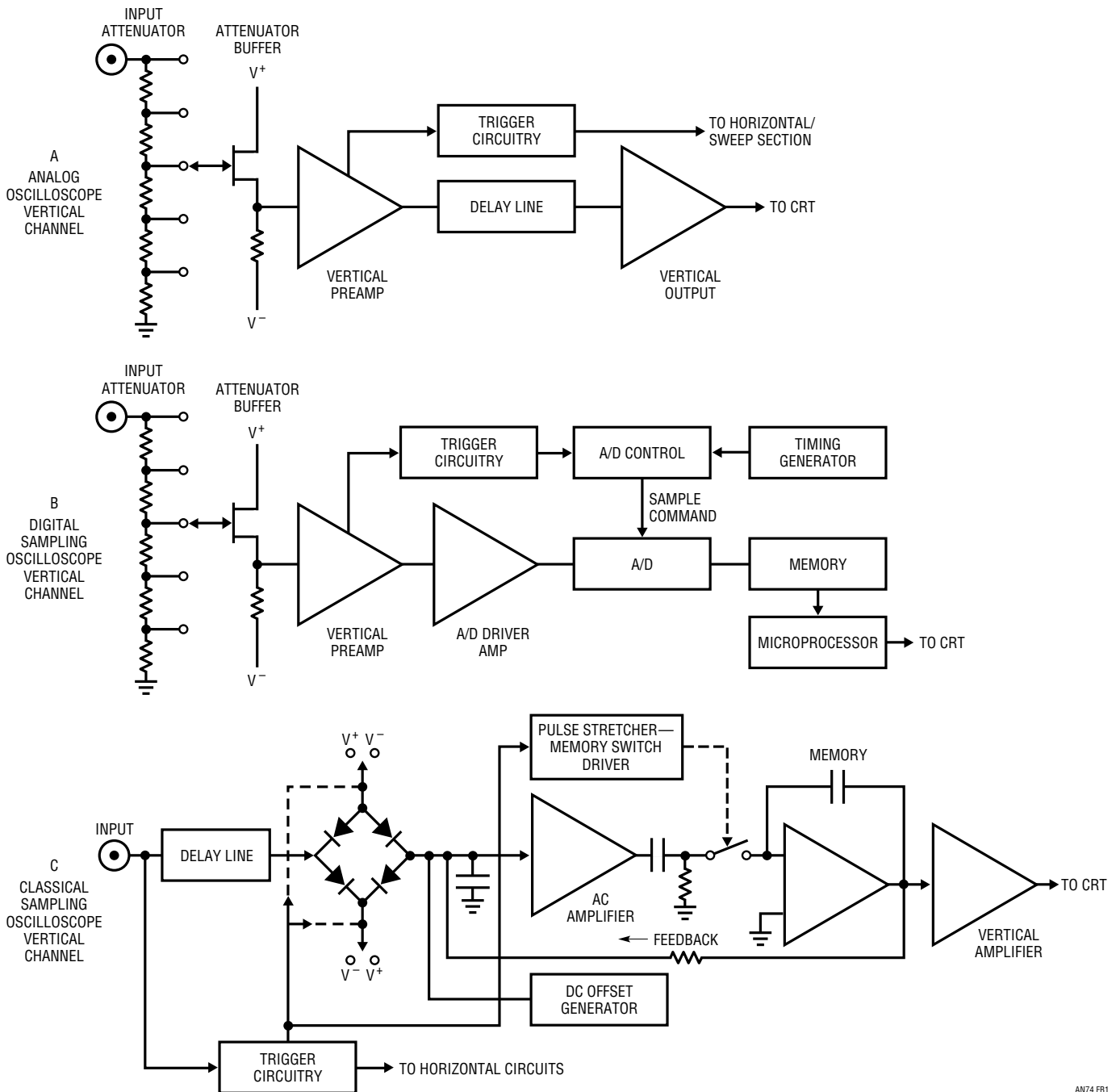
Note 1: Ergo, the Real Thing. Hopelessly bigoted residents of this locale mourn the passing of the analog 'scope era and frantically hoard every instrument they can find.

Note 2: Some discussion of input overdrive effects in analog oscilloscope circuitry is found in reference 10.

Note 3: Additional information and detailed treatment of classical sampling oscilloscope operation appears in references 14-17 and 20-22.

Although analog and digital oscilloscopes are susceptible to overdrive, many types can tolerate some degree of this abuse. The early portion of this appendix stressed that measurements involving oscilloscope overdrive must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity that eliminates all off-screen activity. Figure B2 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure B3) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original



AN74 FB1

Figure B1. Simplified Vertical Channel Diagrams for Different Type Oscilloscopes. Only the Classical Sampling 'Scope (C) Has Inherent Overdrive Immunity. Offset Generator Allows Viewing Small Signals Riding On Large Excursions

Application Note 74

display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure B4, gain has been further increased, and all the features of Figure B3 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure B5

brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure B4. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure B6 the

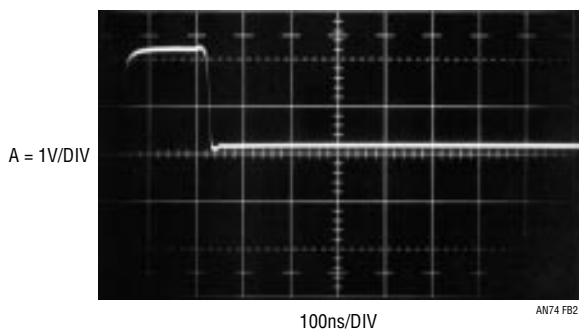


Figure B2

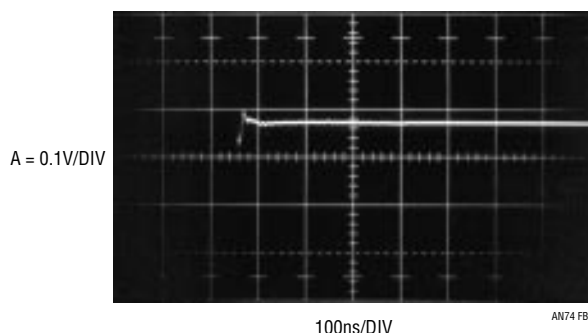


Figure B5

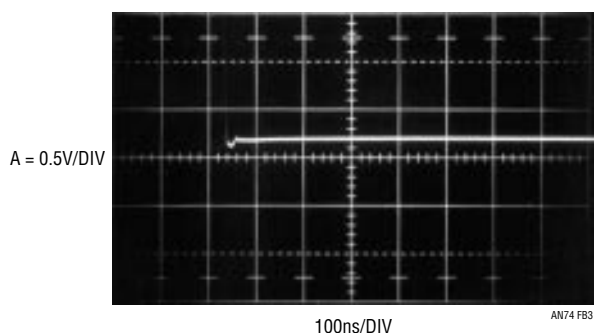


Figure B3

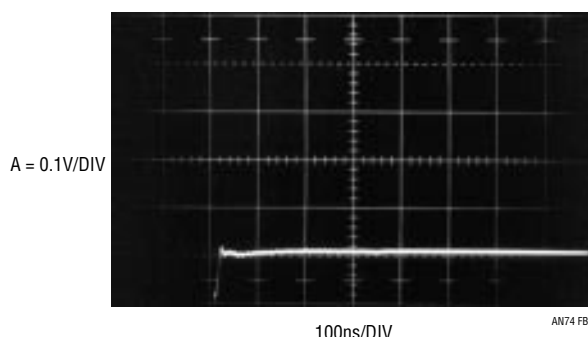


Figure B6

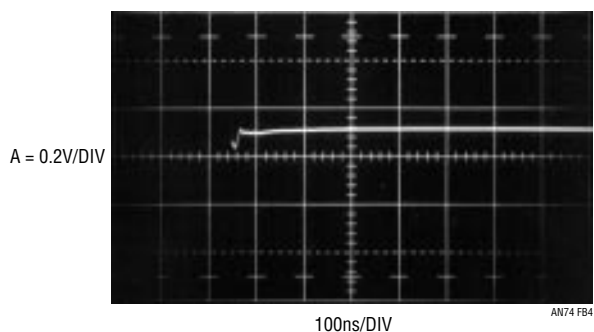


Figure B4

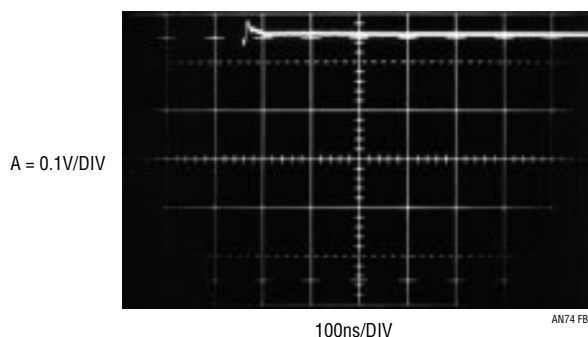


Figure B7

Figures B2-B7. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

gain remains the same but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform

amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure B7). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

APPENDIX C

MEASURING AND COMPENSATING RESIDUE-AMPLIFIER DELAY

The settling-time circuits utilize an adjustable delay network to time correct the input pulse for delays in the signal-processing path. Typically, these delays introduce errors of a few percent, so a first-order correction is adequate. Setting the delay trim involves observing the network's input-output delay and adjusting for the appropriate time interval. Determining the "appropriate" time interval is somewhat more complex. Measuring the sampling bridge-based circuit's signal path delay involves modifications to Figure 6, shown in Figure C1. These changes lock the circuit into its "sample" mode, permitting an input-to-output delay measurement under signal-level conditions similar to normal operation. In Figure C2, trace A is the pulse-generator input at 200 μ V/DIV (note 10k-1 Ω divider feeding the settle node). Trace B shows the circuit output at A2, delayed by about 12ns. This delay is a small error, but is readily corrected by adjusting the delay network for the same time lag.

Figure C3 takes a similar approach with Figure 26's sampling 'scope-based measurement. Modifications permit a small amplitude pulse to drive the settle node, mimicking normal operation signal level conditions. Circuit output at A2 is monitored for delay with respect to the input pulse. Note that A2's high impedance output requires a FET probe to avoid loading. As such, the input pulse must be routed to the oscilloscope via a similar FET probe to maintain delay matching. Figure C4 shows results. The output (trace B) lags the input by 32ns. This factor is used to calibrate text Figure 26's delay network, compensating the circuit's signal path propagation time error.

Delay compensation values for the bootstrapped clamp (text Figure 24) and differential amplifier (text Figure 28) circuits were determined in similar fashion.

Application Note 74

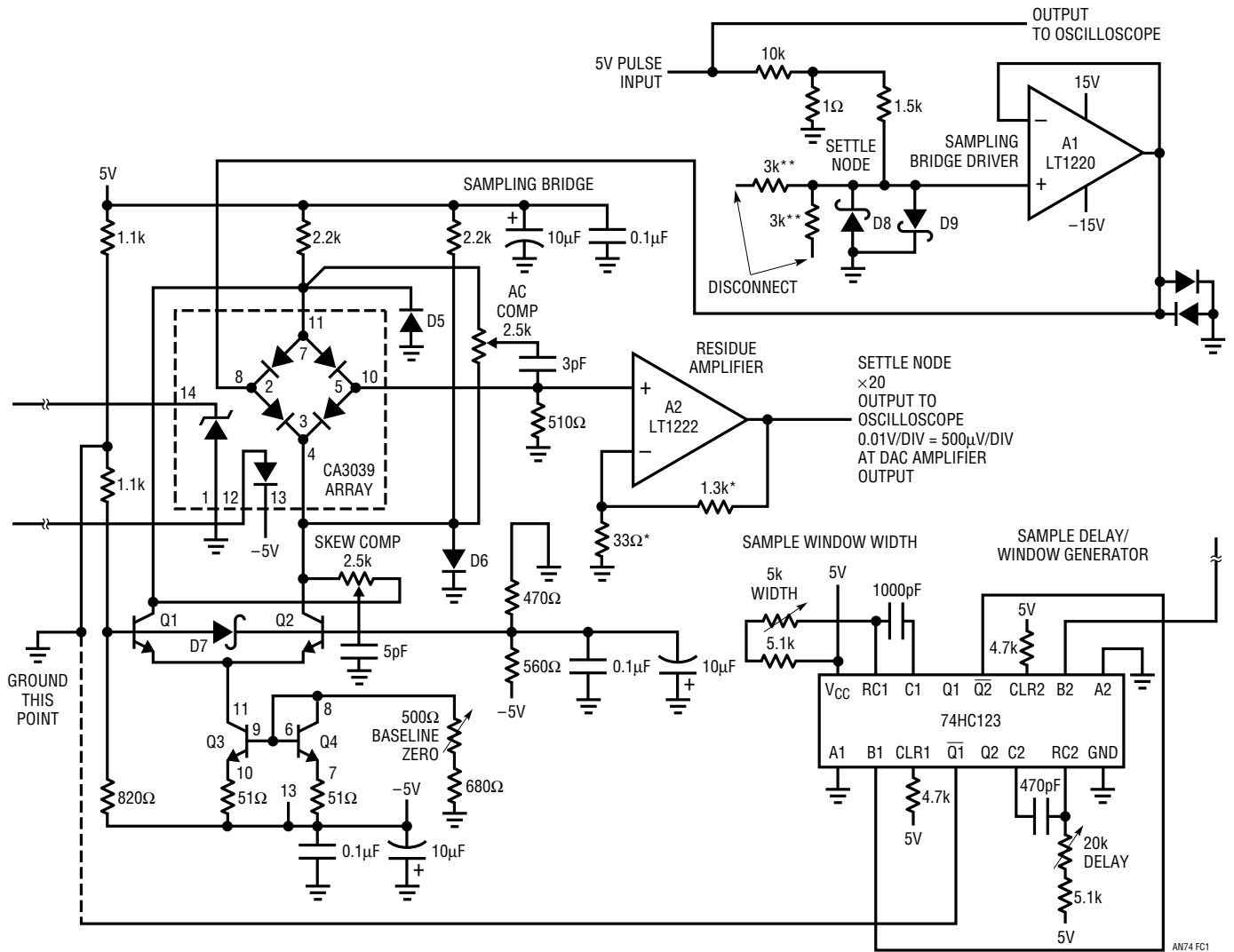


Figure C1. Sampling Bridge Circuit Modifications for Measuring Amplifier Delay. Changes Lock Circuit into Sample Mode, Permitting Input-to-Output Delay Measurement

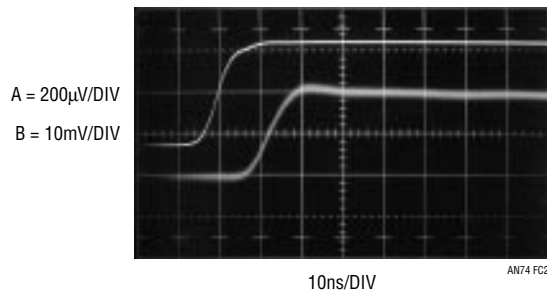


Figure C2. Input-Output Delay for Sampling Bridge Circuit Measures About 12ns

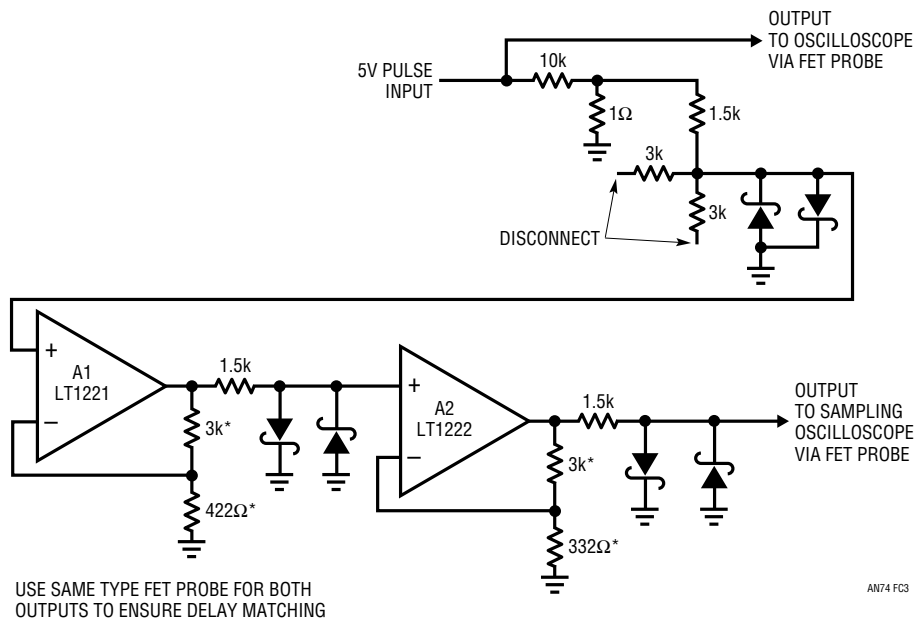


Figure C3. Partial Version of Figure 26 Showing Modifications Permitting Delay Time Measurement. FET Probes are the Same Type, Eliminating Time Skewing Error

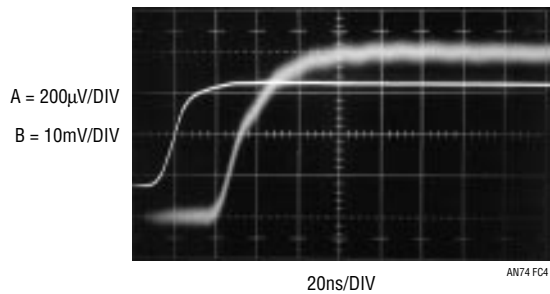


Figure C4. Delay Measurement Results for Figure C3. Input-Output Time Lag is About 32ns

Application Note 74

APPENDIX D

PRACTICAL CONSIDERATIONS FOR DAC-AMPLIFIER COMPENSATION

There are a number of practical considerations in compensating the DAC-amplifier pair to get fastest settling time. Our study begins by revisiting text Figure 1 (repeated here as Figure D1). Settling time components include delay, slew and ring times. Delay is due to propagation time through the DAC-amplifier and is a very small term. Slew time is set by the amplifier's maximum speed. Ring time defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. Once a DAC-amplifier pair have been chosen, only ring time is readily adjustable. Because slew time is usually the dominant lag, it is tempting to select the fastest slewing amplifier available to obtain best settling. Unfortunately, fast slewing amplifiers usually have extended ring times, negating their brute force speed advantage. The penalty for raw speed is, invariably, prolonged ringing, which can only be damped with large compensation capacitors. Such compensation works, but results in protracted settling times. The key to good settling times is to choose an amplifier with the right balance of slew rate and recovery characteristics and compensate it properly. This is harder than it sounds because amplifier settling time cannot be predicted or extrapolated from any combination of data sheet specifications. It must be measured in the intended configuration. In the case of a DAC-amplifier, a number of terms combine to influence settling time. They include amplifier slew rate and AC dynamics, DAC output resistance and capacitance, and the compensation

capacitor. These terms interact in a complex manner, making predictions hazardous.¹ If the DAC's parasitics are eliminated and replaced with a pure resistive source, amplifier settling time is still not readily predictable. The DAC's output impedance terms just make a difficult problem more messy. The only real handle available to deal with all this is the feedback compensation capacitor, C_F . C_F 's purpose is to roll off amplifier gain at the frequency that permits best dynamic response. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the DAC's parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to "hunt" and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, typically 100pF, and it varies with code.

Best settling results when the compensation capacitor is selected to functionally compensate for all the above parasitics. Figure D2 shows results for an optimally selected feedback capacitor. Trace A is the DAC input pulse and trace B the amplifier's settle signal. The amplifier is seen to come cleanly out of slew (sample gate opens just prior to fifth vertical division) and settle very quickly.

Note 1: Spice aficionados take notice.

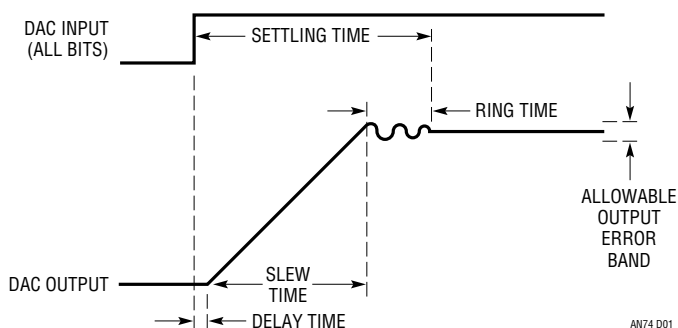


Figure D1. DAC-Amplifier Settling Time Components Include Delay, Slew and Ring Times. For Given Components, Only Ring Time is Readily Adjustable

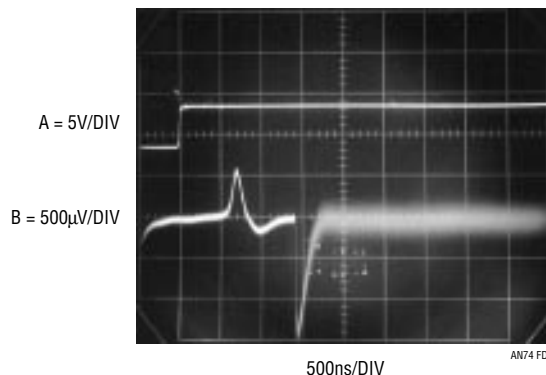


Figure D2. Optimized Compensation Capacitor Permits Nearly Critically Damped Response, Fastest Settling Time. $t_{SETTLE} = 1.7\mu s$

In Figure D3, the feedback capacitor is too large. Settling is smooth, although overdamped, and a 600ns penalty results. Figure D4's feedback capacitor is too small, causing a somewhat underdamped response with resultant excessive ring time excursions. Settling time goes out to 2.3 μ s.

When feedback capacitors are individually trimmed for optimal response, the DAC, amplifier and compensation capacitor tolerances are irrelevant. If individual trimming is not used, these tolerances must be considered to determine the feedback capacitor's production value. Ring time is affected by DAC capacitance and resistance, as well as the feedback capacitor's value. The relationship is nonlinear, although some guidelines are possible. The DAC impedance terms can vary by $\pm 50\%$ and the feedback capacitor is typically a $\pm 5\%$ component. Additionally, amplifier slew rate has a significant tolerance, which is stated on the data sheet. To obtain a production feedback

capacitor value, determine the optimum value by individual trimming *with the production board layout* (board layout parasitic capacitance counts too!). Then, factor in the worst-case percentage values for DAC impedance terms, slew rate and feedback capacitor tolerance. Add this information to the trimmed capacitors measured value to obtain the production value. This budgeting is perhaps unduly pessimistic (RMS error summing may be a defensible compromise), but will keep you out of trouble.² Figure 34's "conservative" settling time values were arrived at in this manner. Note that the chart's slow slewing amplifiers have the same compensation capacitor for "optimal" and "conservative" cases. This reflects the fact that their ring times are very small compared to their slew intervals.

Note 2: The potential problems with RMS error summing become clear when sitting in an airliner that is landing in a snowstorm.

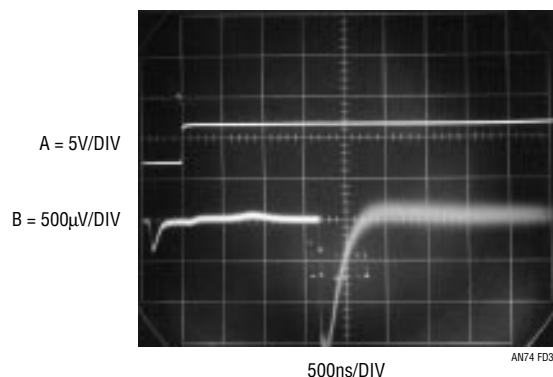


Figure D3. Overdamped Response Ensures Freedom from Ringing, Even with Component Variations in Production. Penalty is Increased Settling Time. $t_{SETTLE} = 2.3\mu$ s

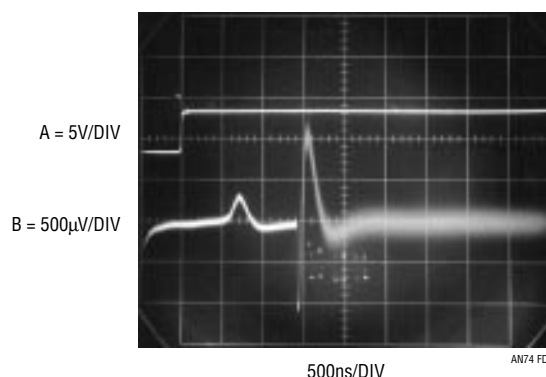


Figure D4. Underdamped Response Results from Undersized Capacitor. Component Tolerance Budgeting Will Prevent This Behavior. $t_{SETTLE} = 2.3\mu$ s

Application Note 74

APPENDIX E

A VERY SPECIAL CASE—MEASURING SETTLING TIME OF CHOPPER-STABILIZED AMPLIFIERS

Figure 34's table lists the LTC1150 chopper-stabilized amplifier. The term "special case" appears in the "comments" column. A special case it is! To see why requires some understanding of how these amplifiers work. Figure E1 is a simplified block diagram of the LTC1150 CMOS chopper-stabilized amplifier. There are actually two amplifiers. The "fast amp" processes input signals directly to the output. This amplifier is relatively quick, but has poor DC offset characteristics. A second, clocked, amplifier is employed to periodically sample the offset of the fast channel and maintain its output "hold" capacitor at whatever value is required to correct the fast amplifier's offset errors. The DC stabilizing amplifier is clocked to permit it to operate (internally) as an AC amplifier, eliminating its DC terms as an error source.¹ The clock chops the stabilizing amplifier at about 500Hz, providing updates to the hold capacitor-offset control every 2ms.²

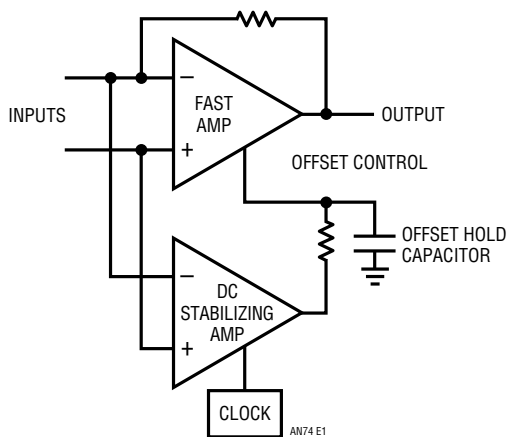


Figure E1. Highly Simplified Block Diagram of Monolithic Chopper-Stabilized Amplifier. Clocked Stabilizing Amplifier and Hold Capacitor Cause Settling Time Lag

The settling time of this composite amplifier is a function of the response of the fast and stabilizing paths. Figure E2 shows short-term settling of the amplifier. Trace A is the DAC input pulse and trace B the settle signal. Damping is reasonable and the 10 μ s settling time and profile appear typical. Figure E3 brings an unpleasant surprise. If the DAC

slewing interval happens to coincide with the amplifier's sampling cycle, serious error is induced. In Figure E3, trace A is the amplifier output and trace B the settle signal. Note the slow horizontal scale. The amplifier initially settles quickly (settling is visible in the 2nd vertical division region) but generates a huge error 200 μ s later when its internal clock applies an offset correction. Successive clock cycles progressively chop the error into the noise but 7 *milliseconds* are required for complete recovery. The error derives from the fact that the amplifier sampled its

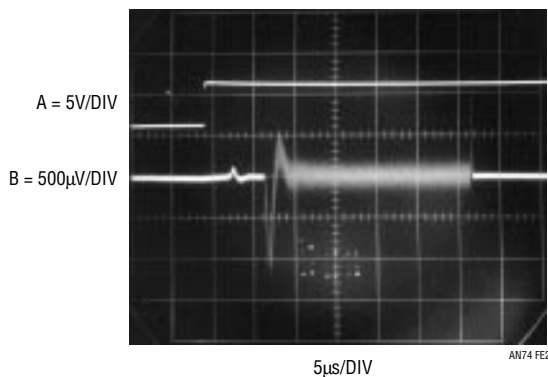


Figure E2. Short-Term Settling Profile of Chopper-Stabilized Amplifier Seems Typical. Settling Appears to Occur in 10 μ s

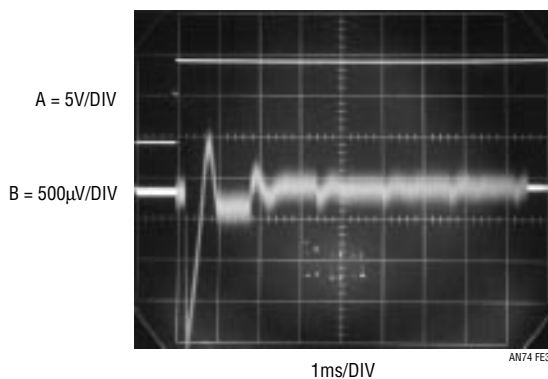


Figure E3. Surprise! Actual Settling Requires 700 \times More Time Than Figure E2 Indicates. Slow Sweep Reveals Monstrous Tailing Error (Note Horizontal Scale Change) Due to Amplifier's Clocked Operation. Stabilizing Loop's Iterative Corrections Progressively Reduce Error Before Finally Disappearing Into Noise

offset when its input was driven well outside its bandpass. This caused the stabilizing amplifier to acquire erroneous offset information. When this “correction” was applied, the result was a huge output error.

This is admittedly a worst case. It can only happen if the DAC slewing interval coincides with the amplifier’s internal clock cycle, but it can happen.^{3, 4}

Note 1: This AC processing of DC information is the basis of all chopper and chopper-stabilized amplifiers. In this case, if we could build an inherently stable CMOS amplifier for the stabilizing stage, no chopper stabilization would be necessary.

Note 2: Those finding this description intolerably brief are commended to reference 23.

Note 3: Readers are invited to speculate on the instrumentation requirements for obtaining Figure E3’s photo.

Note 4: The spirit of Appendix D’s footnote 2 is similarly applicable in this instance.

APPENDIX F

SETTLING TIME MEASUREMENT OF SERIALLY LOADED DACS

LTC models LTC1595 and LTC1650 are serially loaded 16-bit DACs. The LTC1650 includes an onboard output amplifier. Measuring these device’s settling time with the methods described in the text requires additional circuitry. The circuitry must provide a “start” pulse to the settling time measurement after serially loading a full-scale step into the DAC. Figure F1’s circuitry, designed and constructed by Jim Brubaker, Kevin Hoskins, Hassan Malik and Tuyet Pham (all of LTC) does this. The “start” pulse is taken from U1B’s Q output. The DAC amplifier is moni-

tored in the normal manner. This permits Figure F2 to display settling results in (what should be by now) familiar fashion. Settling time (trace B) is measured from the rising edge of trace A’s start pulse. Figure F3 is a similar circuit configured for the LTC1650 voltage output DAC. Reference voltage and other changes are required to accommodate the DAC’s $\pm 4V$ output swing and different architecture, but overall operation is similar. Figure F4 shows settling results.

Application Note 74

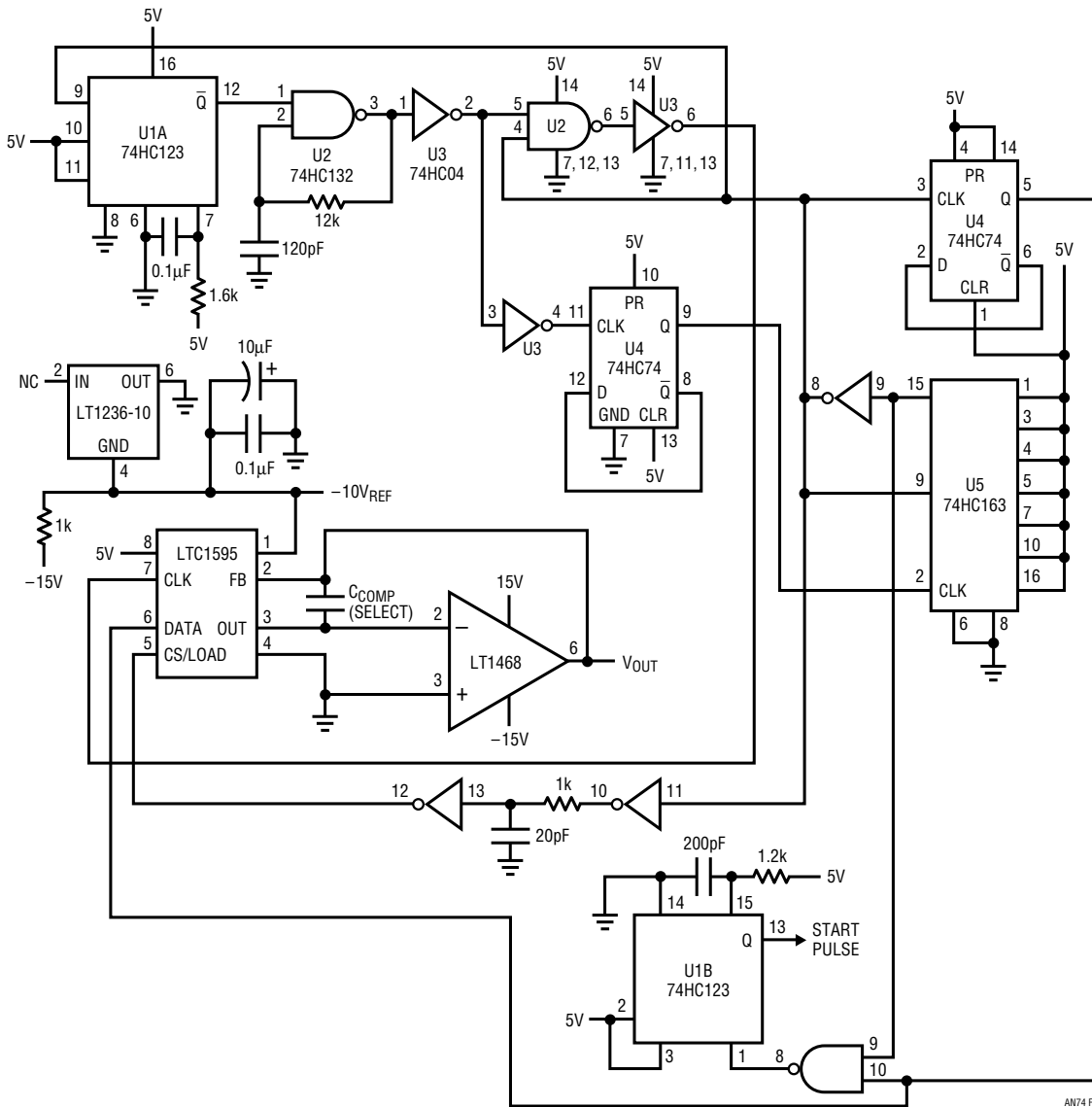


Figure F1. Logic Circuitry Permits Measuring Settling Time of Serially Loaded LTC1595 DAC

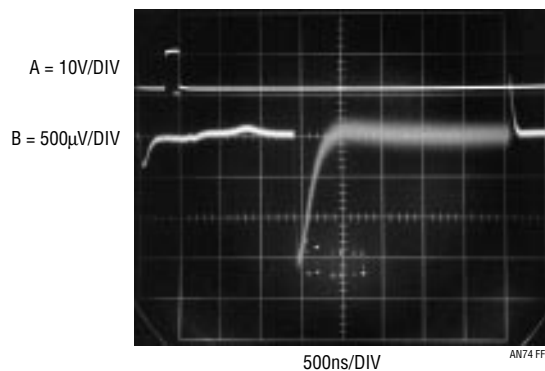


Figure F2. Oscilloscope Display of Serially Loaded DAC Settling Time Measurement. Settling Time is Measured from "Start Pulse" (See Schematic) Rising Edge (Trace A)

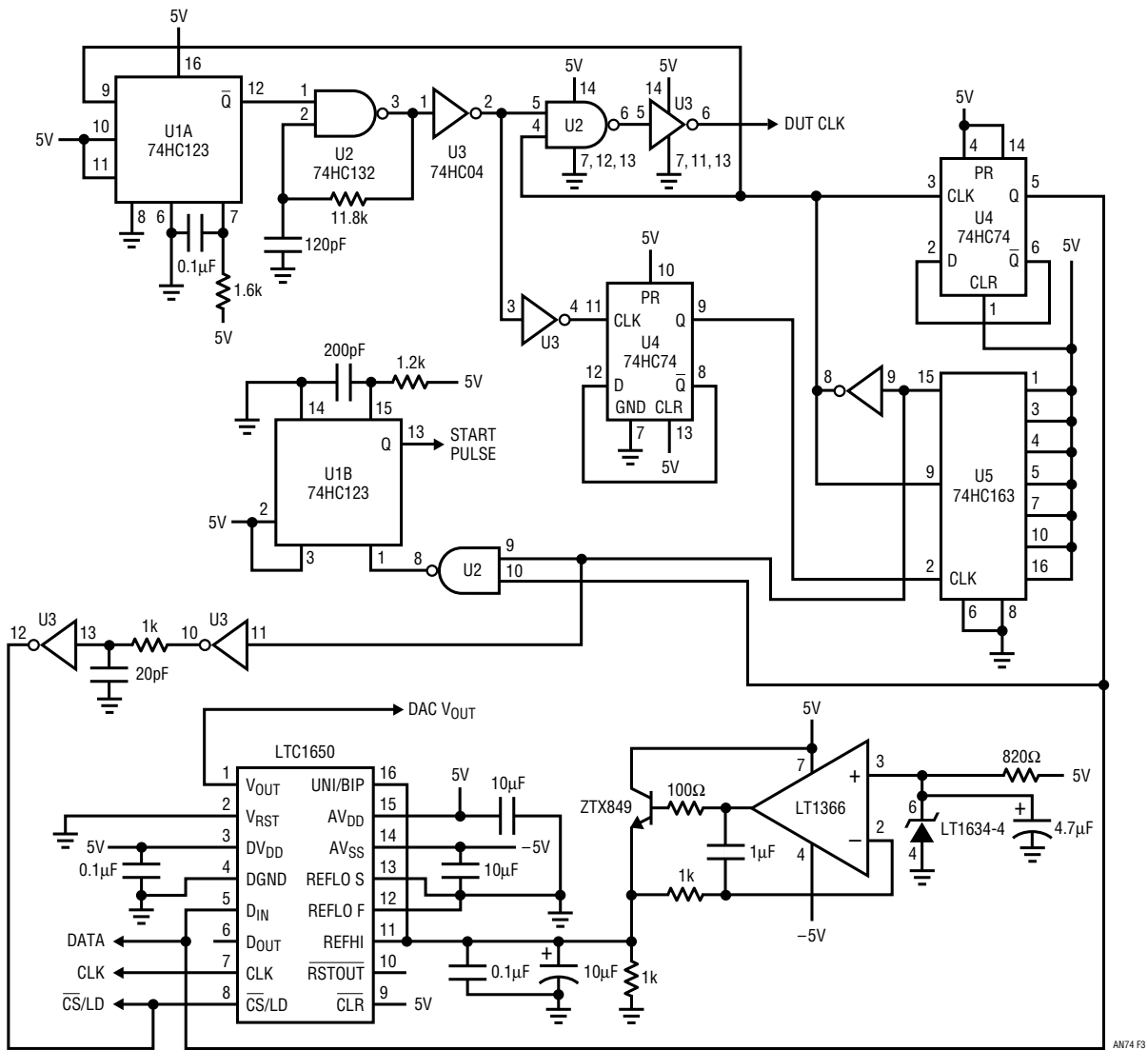


Figure F3. Reconfigured Figure F1 Allows LTC1650 Settling Time Measurement

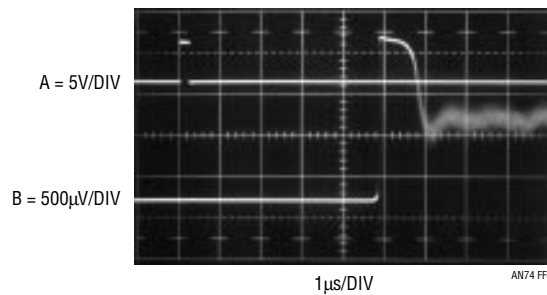


Figure F4. LTC1650 Voltage Output DAC Shows 6μs Settling Time. A is Start Pulse, B the Settle Signal

APPENDIX G

BREADBOARDING, LAYOUT AND CONNECTION TECHNIQUES

The measurement results presented in this publication required painstaking care in breadboarding, layout and connection techniques. Wideband, 100 μ V resolution measurement does not tolerate cavalier laboratory attitude. The oscilloscope photographs presented, devoid of ringing, hops, spikes and similar aberrations, are the result of an exhaustive (and frustrating) breadboarding exercise.¹ The sampler-based breadboard (Figures G1, G2) was rebuilt six times and required days of layout and shielding experimentation before obtaining a noise/uncertainty floor worthy of 16-bit measurement.

Ohm's Law

It is worth considering that Ohm's law is a key to successful layout.² Consider that 1mA running through 0.1 Ω generates 100 μ V—almost 1LSB at 16 bits! Now, run that milliampere at 5 to 10 nanosecond rise times (\approx 75MHz) and the need for layout care becomes clear. A paramount concern is disposal of circuit ground return current and disposition of current in the ground plane. The impedance of the ground plane between any two points is *not* zero, particularly as frequency scales up. This is why the entry point and flow of “dirty” ground returns must be carefully placed within the grounding system. In the sampler-based breadboard, the approach was separate “dirty” and “signal” ground planes (see Figures G1 to G7), tied together at the supply ground origin.

A good example of the importance of grounding management involves delivering the input pulse to the breadboard. The pulse generator's 50 Ω termination *must* be an in-line coaxial type, and it cannot be directly tied to the signal ground plane. The high speed, high density (5V pulses through the 50 Ω termination generate 100mA current spikes) current flow must return directly to the pulse generator. The coaxial terminator's construction ensures this substantial current does this, instead of being dumped into the signal ground plane (100mA termination current flowing through 1 *milliohm* of ground plane produces \approx 1LSB of error!). Figure G3 shows that the BNC

shield floats from the signal plane, and is returned to “dirty” ground via RF braid. Additionally, Figure G1 shows the pulse generator's 50 Ω termination physically distanced from the breadboard via a coaxial extension tube. This further ensures that pulse generator return current circulates in a tight local loop at the terminator, and does not mix into the signal plane.

It is worth mentioning that every ground return in the entire circuit must be evaluated with these concerns in mind. A paranoiac mindset is quite useful.

Shielding

The most obvious way to handle radiation-induced errors is shielding. Various following figures show shielding. Determining where shields are required should come *after* considering what layout will minimize their necessity. Often, grounding requirements conflict with minimizing radiation effects, precluding maintaining distance³ between sensitive points. Shielding⁴ is usually an effective compromise in such situations.

A similar approach to ground path integrity should be pursued with radiation management. Consider what points are likely to radiate, and try to lay them out at a distance from sensitive nodes. When in doubt about odd effects, experiment with shield placement and note results, iterating towards favorable performance.⁵ *Above all, never rely on filtering or measurement bandwidth limiting to “get rid of” undesired signals whose origin is not fully understood.* This is not only intellectually dishonest, but may produce wholly invalid measurement “results,” even if they look pretty on the oscilloscope.

Note 1: “War” is perhaps a more accurate descriptive.

Note 2: I do not wax pedantic here. My abuse of this postulate runs deep.

Note 3: Distance is the physicist's approach to reducing radiation induced effects.

Note 4: Shielding is the engineer's approach to reducing radiation induced effects.

Note 5: After it works, you can figure out why.

Connections

All signal connections to the breadboard must be coaxial. Ground wires used with oscilloscope probes are forbidden. A 1" ground lead used with a 'scope probe can easily generate several LSBs of observed "noise"! Use coaxially mounting probe tip adapters!⁶

Figures G1 to G10 restate the above sermon in visual form while annotating the text's measurement circuits.

Note 6: See Reference 26 for additional nagging along these lines.

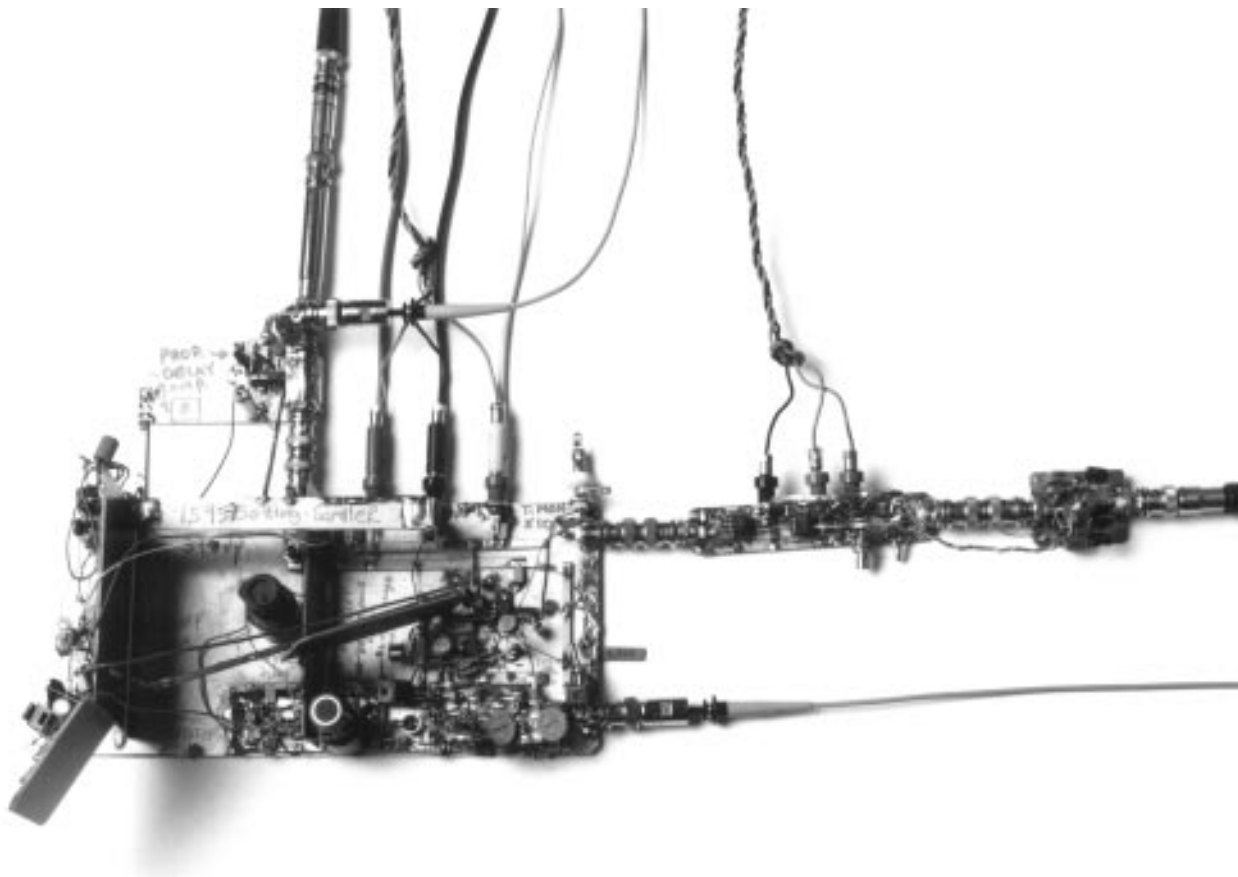


Figure G1. Overview of Settling Time Breadboard. Pulse Generator Input Enters Top Left—50Ω Coaxial Terminator Mounted On Extension Minimizes Pulse Generator Return Current Mixing Into Signal Ground Plane (Bottom Board Facing Viewer). “Dirty” Ground Paths Return Separately from Signal Ground Plane Via Planed Horizontal Strip (Upper Left of Main Board). DAC-Amplifier and Support Circuitry are at Extreme Left on Vertical Board. Sampler Circuitry Occupies Board Lower Center. Nonsaturating Amplifier-Bootstrapped Clamp is Thin Board, Extreme Right. Note Coaxial Board Signal and Probe Connections

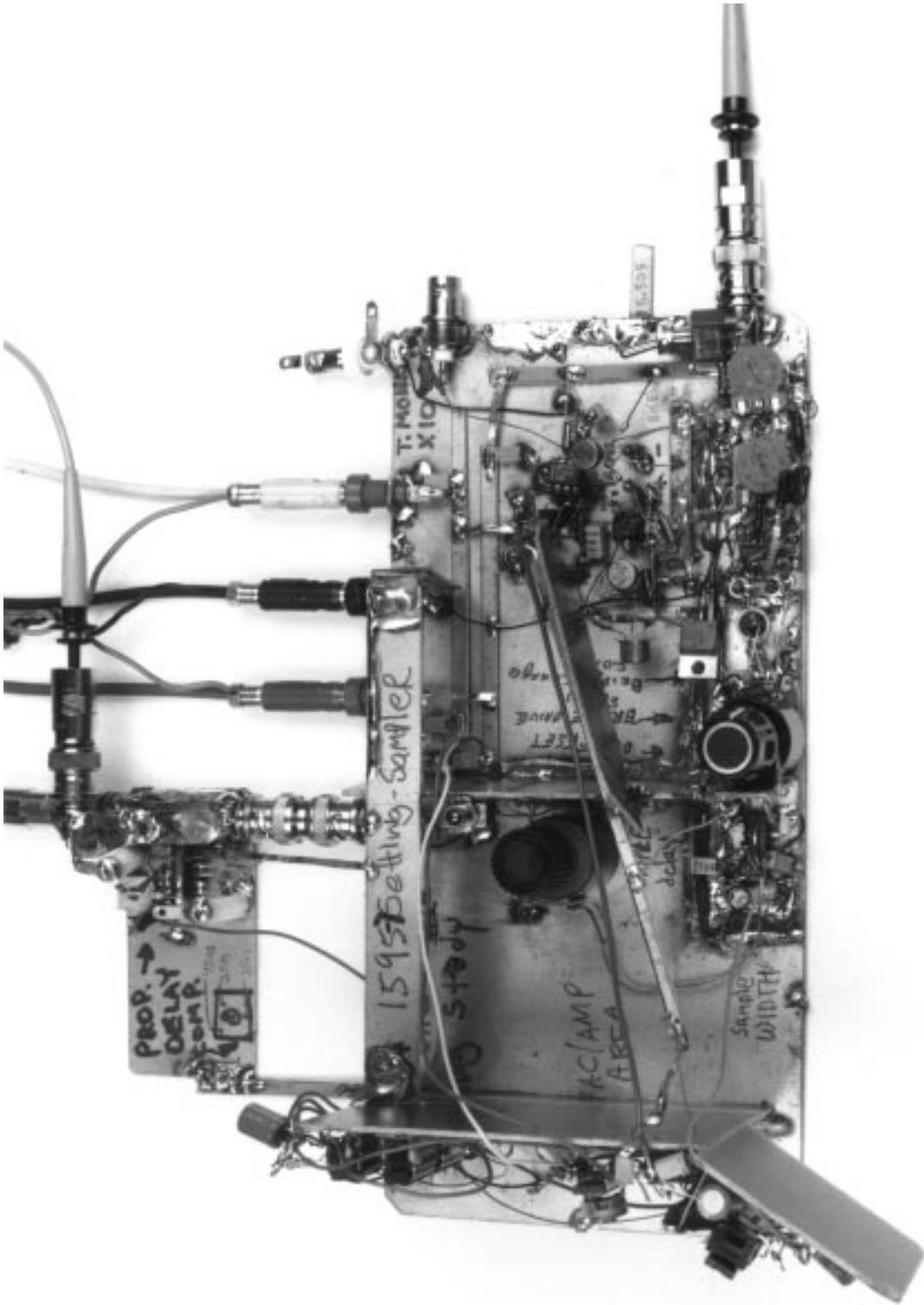


Figure G2. Settling Time Breadboard Detail. Note Radiation Shielding at Delayed Pulse Generator (Lower Left Center), Sampling Bridge Area (Lower Center Right) and DAC-Amplifier Board (Extreme Left). "Dirty" Grounds Return Via Separate Plane (Horizontal Strip, Photo Center Left). Vertical Shield (Center) Bisects Board, Separating Delayed Pulse Generator's (Lower Left Center) Fast Edges from Sampling Bridge Circuitry. DAC Amplifier Output is Routed Via Thin Copper Strip (Angled, Running Left-Right) to Settle Node (Board Center Right). Shield (Angled, Center) Prevents Radiation Into Bridge Area

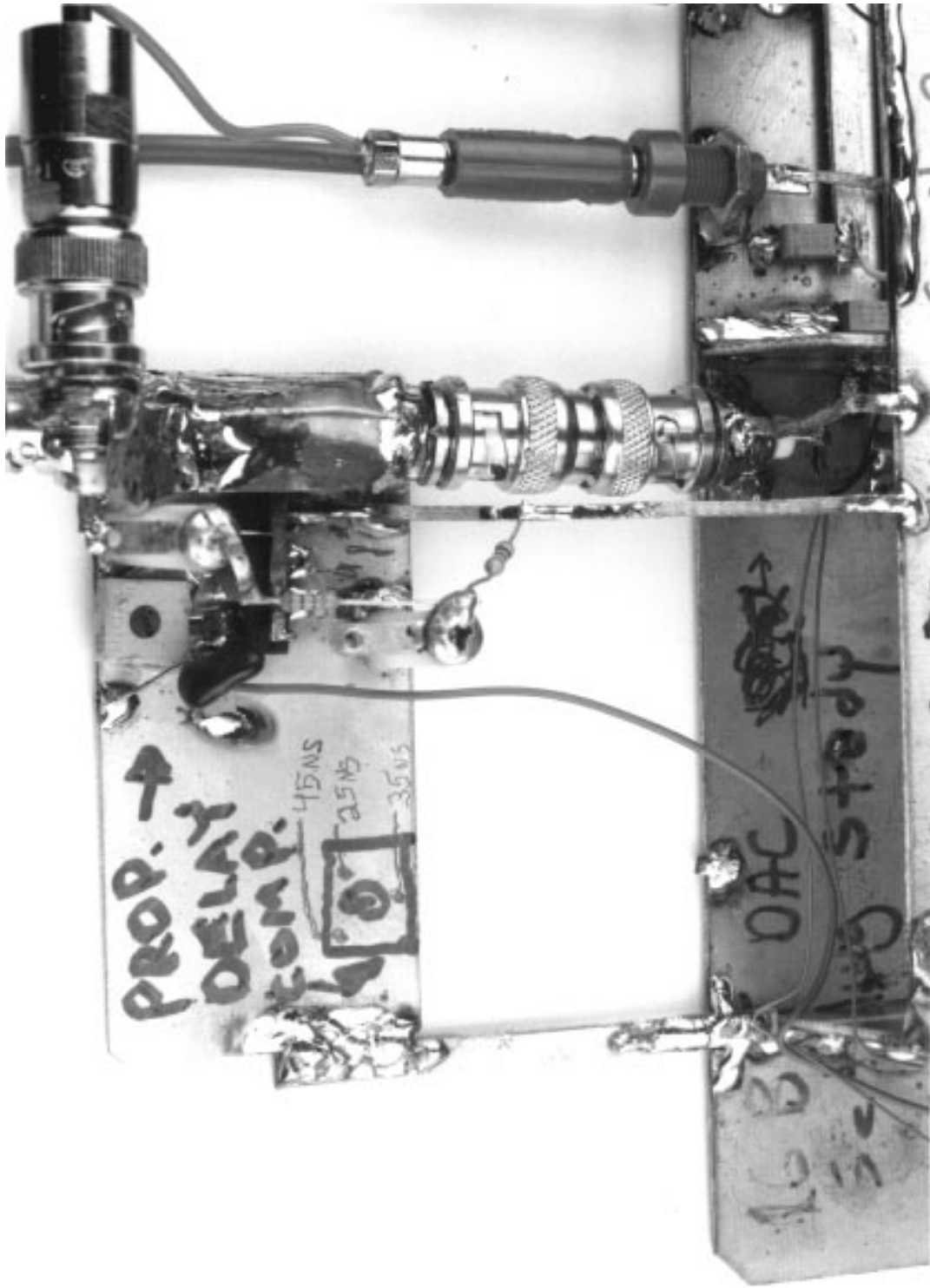


Figure G3. Detail of Pulse Generator Input—Delay Compensation Section and Interface to Main Board. Time Correction Delay Circuitry is at Photo Upper Center. Coaxial Probe Pick-Off Upper Right. Time Corrected Pulse Enters Main Board at Lower Center Plane (Clad Stand-Off Just Visible at Lower Connector Right). Connector Shell Ground is Tied To “Dirty” Ground Plane Via RF Braid (Lower Right Center), Preventing High Speed Return Currents from Corrupting Main Board Signal Ground Plane. Active Current Returns Flow Through Separate Braid (Long Vertical Run, Photo Center Right) to Main Board “Dirty” Ground Plane

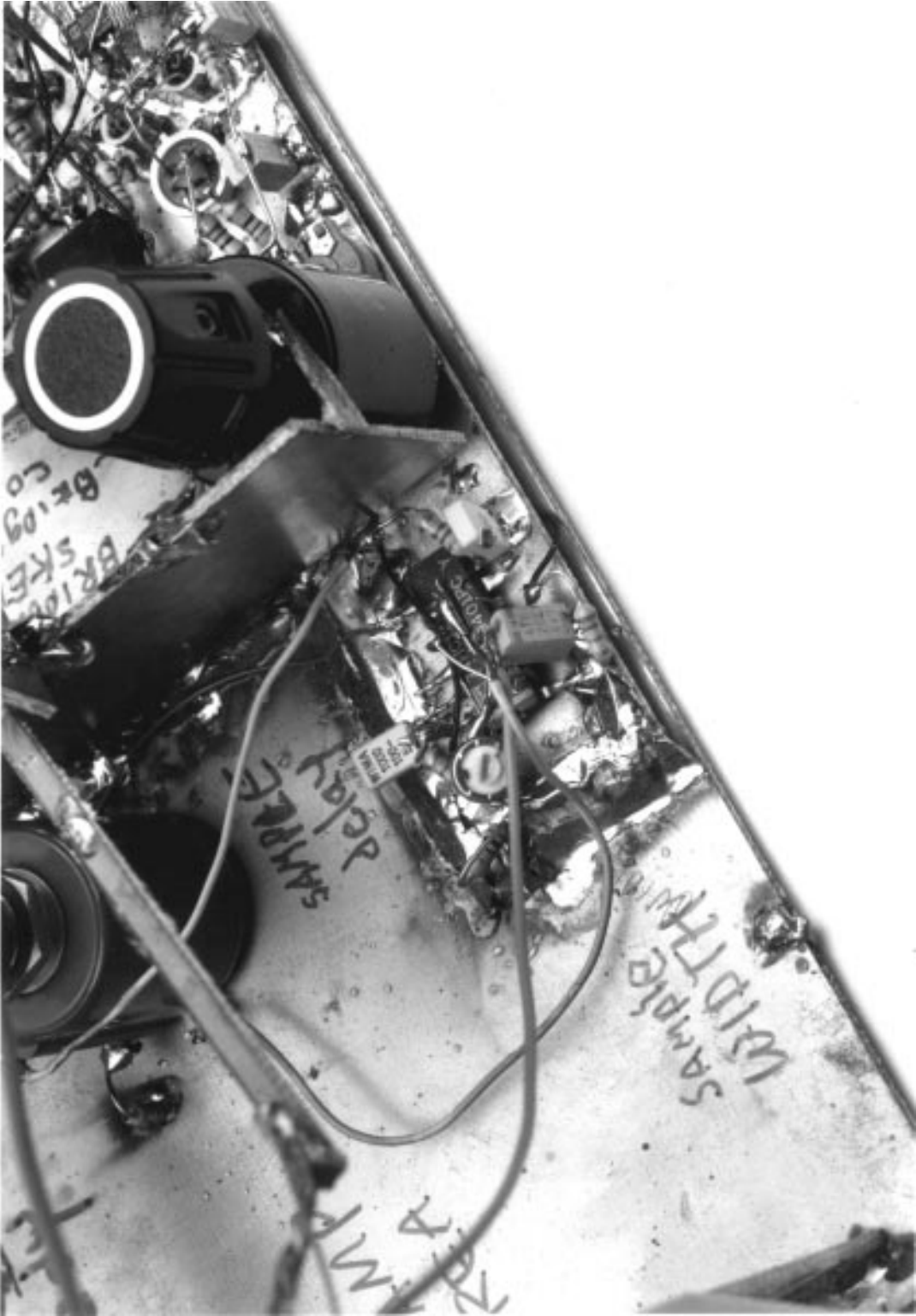


Figure G4. Delayed Pulse Generator is Fully Shielded (Vertical Shield, Photo Center Right) from Sampling Circuitry (Partial, to Right of Vertical Shield). Delayed Pulse Generators Output Lead (Photo Center) Sneaks Under Main Ground Plane to Minimize Radiation Into Sampling Bridge. Screw Adjustment (Photo Center Left) Sets Delayed Pulse Width, Large Potentiometer (Partial, Photo Upper Left Center) Sets Delay

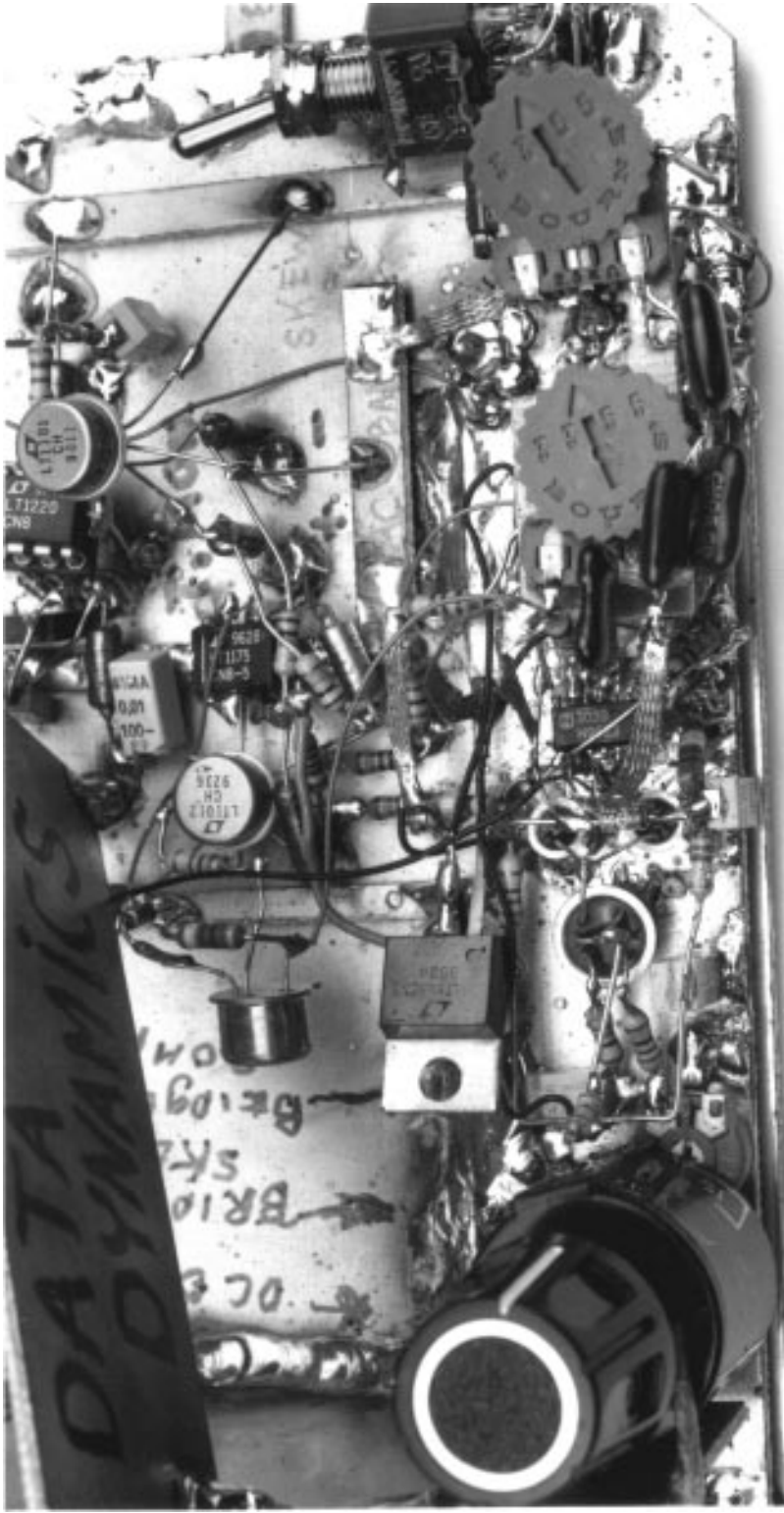


Figure G5. Sampling Bridge and Support Circuitry. Delayed Pulse Generator Output Arrives from Under Ground Plane (Photo Center, Just to Right of TO-220 Power Package), Triggers Complementary Level Shifters (Center Left). Sampling Bridge is SOT-16 Package at Photo Center. Skew Compensation and Bridge AC Balance Trimpots are at Photo Center Right. Baseline Zero is Large Knob at Left. Sampling Bridge Temperature Control Circuitry Appears Upper Right Center



Figure G6. Side-On View of Sampling Bridge Circuitry. Delayed Pulse Generator Output Line is Just Visible in Shielded Space Under Ground Plane ($\approx 45^\circ$ Angle, Photo Extreme Left, Running Towards Center). SOT-16 Packaged Sampling Bridge (Exact Photo Center) Floats on Flying Leads to Maximize Thermal Resistance, Aiding Temperature Control. Upper Board (Photo Right) Mechanically Supports AC Bridge Trimpots

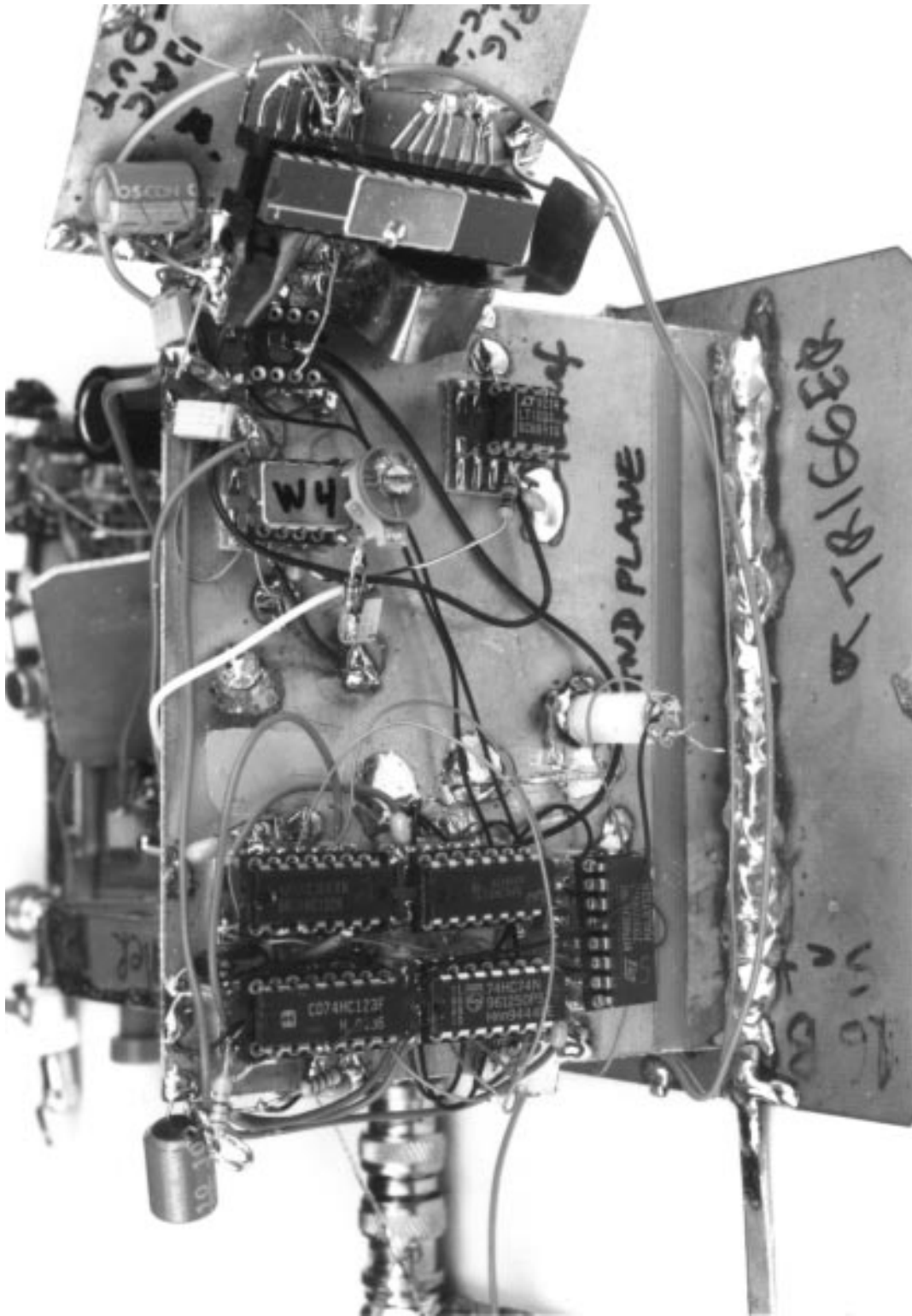


Figure G7. DAC-Amplifier Board Contains DAC (Right), Amplifier (“W4” at Center Right) and Reference (Lower Right). Digital IC Packages at Left are Serial DAC Interface, Potential Noise Generators. Insulating Strip Across Entire Board Bottom Fully Isolates it from Main Board Signal Ground Plane. Individual Board Returns are Routed Separately to Main Board Power Common

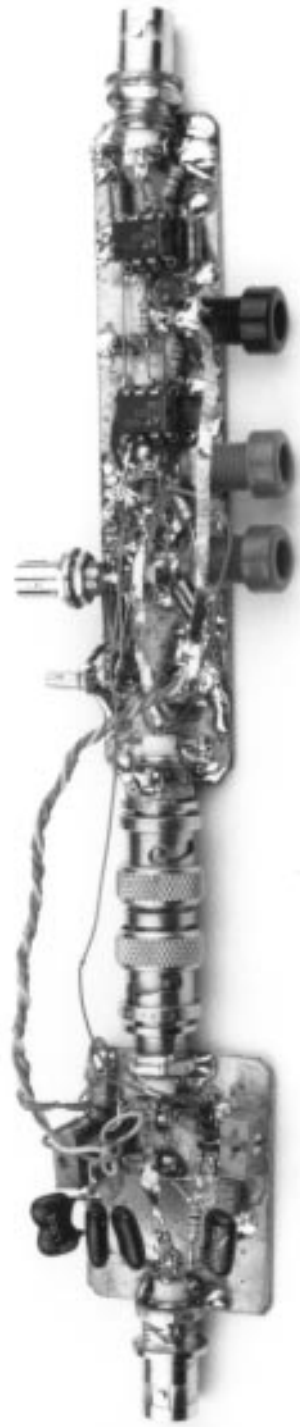


Figure G8. Gain-of-80 Nonsaturating Amplifier (Right of BNC Adapter) and Bootstrapped Clamp (Left of BNC Adapter). Ground Planed Construction and Minimized Summing Point Capacitances Aid Wideband Response

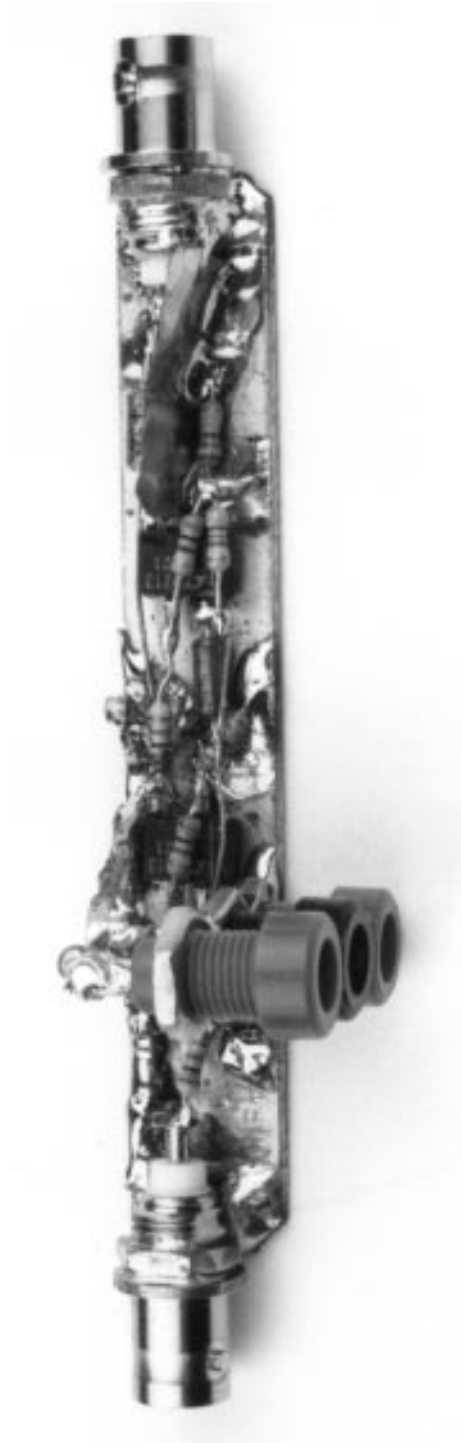


Figure G9. Wideband Nonsaturating Gain of 40 for Figure 28's Differential Amplifier. Layout Ensures Minimal Feedthrough, Particularly When Amplifier is Outside Gain Region. Note Input Shield (Photo Right)

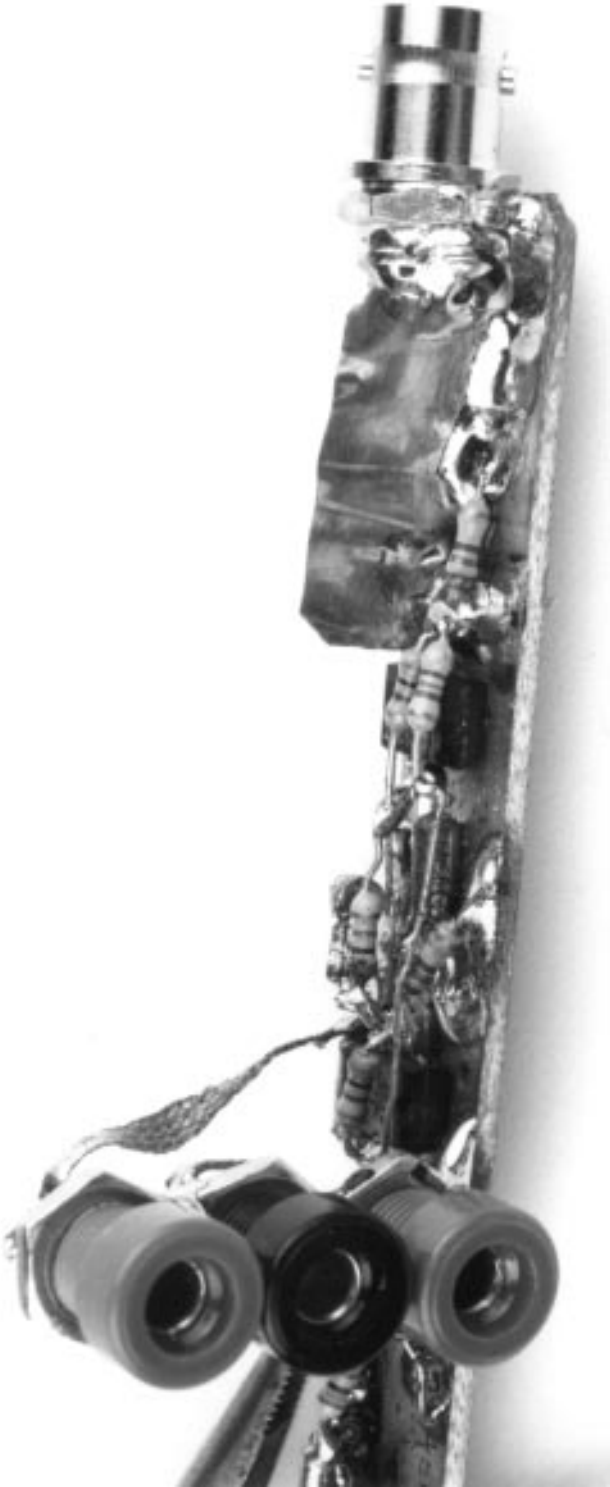


Figure G10. Detail of Nonsaturating Gain of 40 Input Shielding (Photo Right). Shield Prevents Input Excursions Outside Amplifier's Gain Region from Feeding Through to Output, Corrupting Data

APPENDIX H

POWER GAIN STAGES FOR HEAVY LOADS
AND LINE DRIVING

Some applications require driving heavy loads. The load may be static, transient or both. Practical examples of loads include actuators, cables and power voltage/current sources in test equipment. Required load currents may range from tens of milliamperes to amperes, while simultaneously maintaining 16-bit performance. Figure H1 summarizes the system problems involved in applying a power gain stage, sometimes referred to as a booster.

The booster stage's output impedance must be low enough to accurately drive complex loads at all frequencies of interest. "Complex" loads may include interconnecting cable capacitance, pure resistance, capacitive and inductive components. Significant effort should be expended to characterize the load prior to designing the booster. Note that reactive load components will almost certainly add a stability term, complicating wideband loop dynamics. These considerations dictate that the booster's output impedance must be exceptionally low at all frequencies encountered.

Also, the booster must be fast to avoid delay-induced stability problems. Any booster included in an amplifier's loop must be transparent to the amplifier to preserve dynamic performance.¹

Grounding and connection considerations mandate special attention in a high current, 16-bit, DAC driven system. A 1A load current returning through 1m Ω of parasitic resistance causes almost 7LSBs of error. Similar errors occur if feedback sensing is improperly arranged. As such, single-point grounding, in the strictest sense of the word, is mandatory. In particular, the load-return conductor should be thick, short, flat and highly conductive. Feedback sensing should be arranged so that the DAC's R_{FB} terminal is connected *directly* to the load via a low impedance conductor.

Note 1: This discussion must suffer brevity in this forum. For more detail, see References 26 and 27.

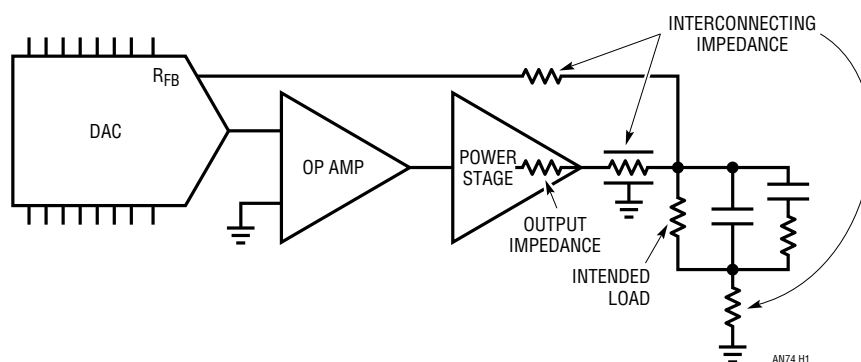


Figure H1. Conceptual Power Gain Stage for DAC-Amplifier. System Issues Involve Booster Output Impedance, Interconnections, Load Characteristics and Grounding

Application Note 74

Booster Circuits

Figure H2 is a simple power output stage using the LT1010 IC booster. Output currents to 125mA are practical. Figure H3 is similar, although offering higher speed operation and more output power. The LT1206 op amp, configured

as a unity-gain follower, permits 250mA outputs; the LT1210 extends current capacity to 1.1A. The indicated optional capacitor improves dynamic performance with capacitive loading (see data sheets). Figure H4 extends current output capacity to 2A by utilizing a wideband

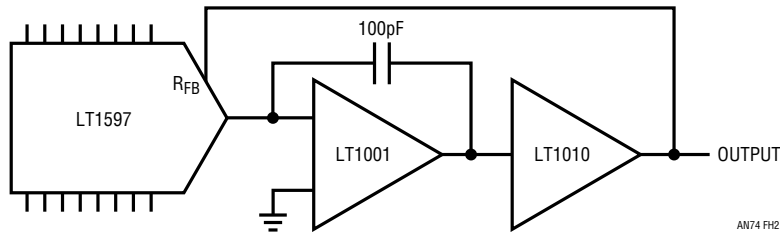


Figure H2. LT1010 Permits 125mA Output Currents

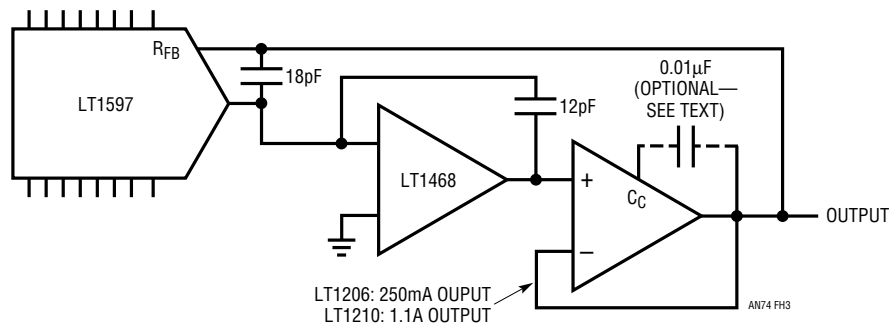


Figure H3. LT1206/LT1210 Output Stages Supply 250mA and 1.1A Loads, Respectively

discrete state. In the positive signal-path output transistor Q4 is an RF power type, driven by Darlington connected Q3. The diode in Q1's emitter compensates the additional V_{BE} introduced by Q3, preventing crossover distortion.

The negative signal path substitutes the Q5-Q6 connection to simulate a fast PNP power transistor. This arrangement is necessitated by the lack of availability of wideband PNP

power transistors. Although this configuration acts like a fast PNP follower, it has voltage gain and tends to oscillate. The local 2pF feedback capacitor suppresses these parasitic oscillations and the composite transistor is stable.

This circuit also includes a feedback capacitor to optimize AC response. Current limiting is provided by Q7 and Q8, which sense across the 0.2Ω shunts.

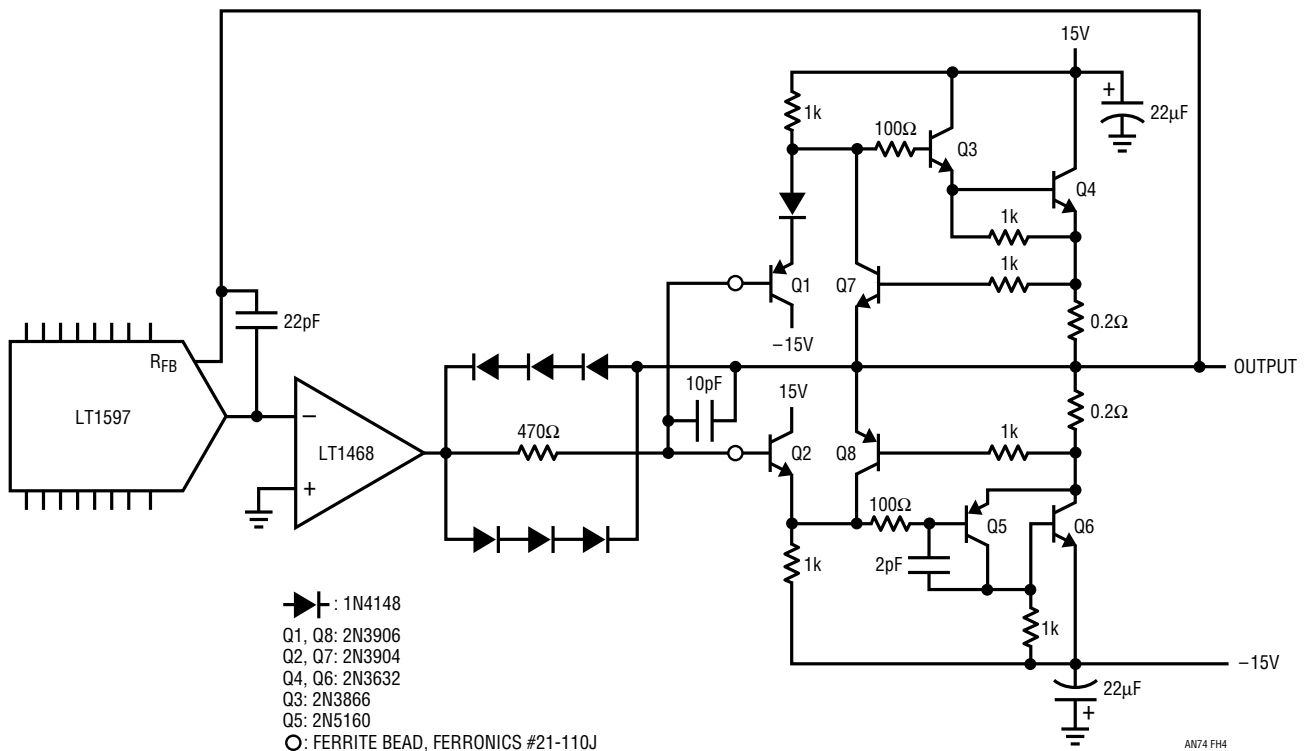


Figure H4. Wideband Discrete Component Booster is More Complex, But Supplies 2A Output

Application Note 74

Figure H5 is a voltage gain stage. The high voltage stage is driven in closed-loop fashion by A2, instead of being included in the DAC-amplifier (A1) loop. This avoids driving the DAC's monolithic feedback resistor from the 100V output, preserving DAC temperature coefficient and, not incidentally, the DAC. Q1 and Q2 furnish voltage gain, and feed the Q3-Q4 emitter follower outputs. Q5 and Q6 set current limit at 25mA by diverting output drive when voltages across the 27Ω shunts become too high. The local 1M-50k feedback pairs set stage gain at 20, allowing ±12V A2 drives to cause full ±120V output swing. The local feedback reduces stage gain-bandwidth, making dynamic control easier. This stage is relatively simple to frequency compensate because only Q1 and Q2 contribute voltage gain. Additionally, the high voltage transistors have large junctions, resulting in low f_{Tj} , and no special high fre-

quency roll-off precautions are needed. Because the stage inverts, feedback is returned to A2's positive input. Frequency compensation is achieved by rolling off A2 with the local 330pF-10k pair. The 15pF capacitor in the feedback peaks edge response and is not required for stability. If over compensation is required, it is preferable to increase the 330pF value, instead of increasing the 15pF loop-feedback capacitor. This prevents excessive high voltage energy from coupling to A2's inputs during slew. If it is necessary to increase the feedback capacitor, the summing point should be diode clamped to ground or to the ±15V supply terminals. Trimming involves selecting the indicated resistor for exactly 100.000V output with the DAC at full scale.

The dynamic response issues discussed in the text apply to all the above circuits.

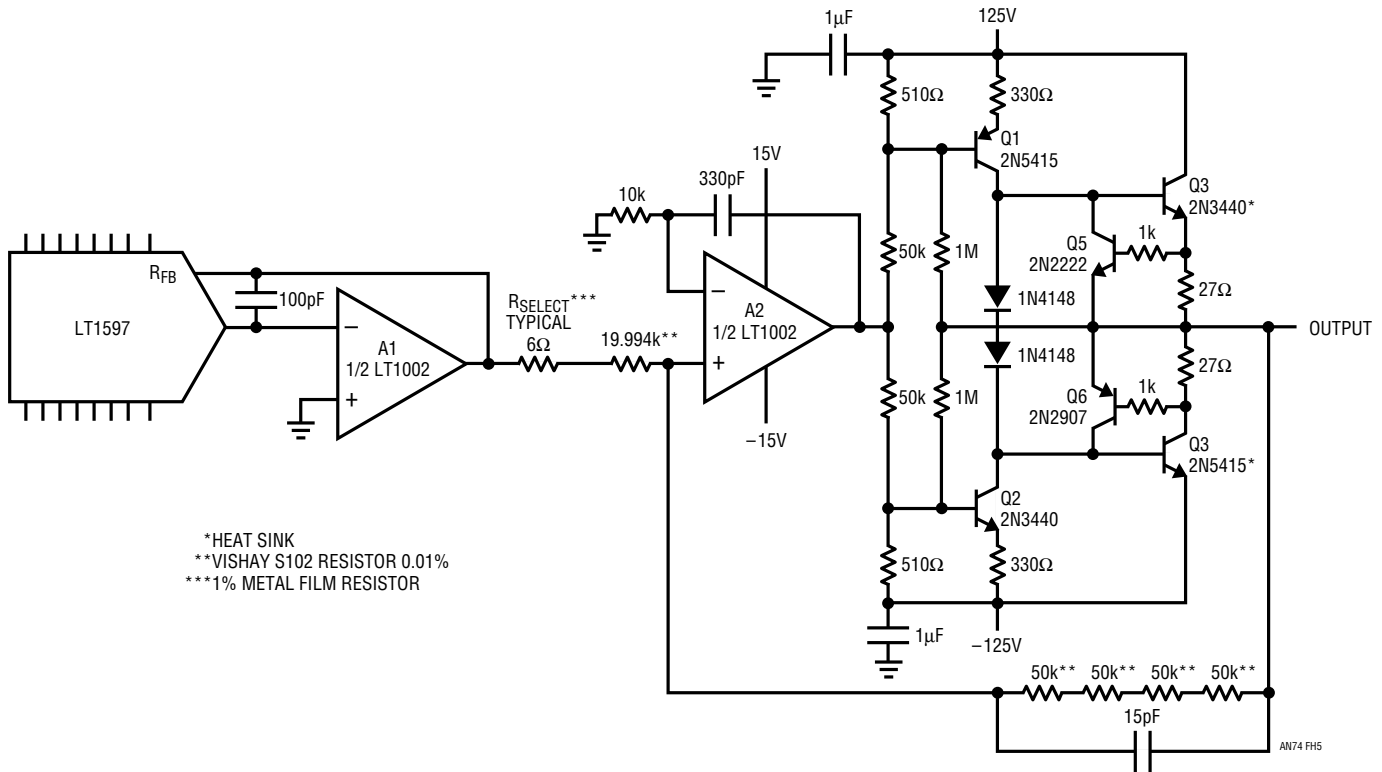


Figure H5. High Voltage Output Stage Delivers 100V at 25mA. Stage Uses Separate Amplifier and Feedback Resistors to Preserve DAC's Gain Temperature Coefficient

Figure H6 summarizes the booster stage's characteristics. The IC-based stages offer simplicity while the complex discrete designs provide more output power.

FIGURE	VOLTAGE GAIN	CURRENT GAIN	COMMENTS
H2	No	Yes	Simple 125mA Stage
H3	No	Yes	Simple 250mA/1.1A Stage
H4	No	Yes	Complex 2A Output
H5	Yes	Minimal	Complex $\pm 120V$ Output

Figure H6. Summary of Booster Stage Characteristics



Measuring 16 Bit Settling Time is NOT A 1 week Project.

— WMM — 98

Circuitry for Signal Conditioning and Power Conversion

Designs From a Once Lazy Sabbatical

Jim Williams

Introduction

Linear Technology has a sabbatical program. Every five years employees are granted sabbatical leave, which may last up to six weeks. You have 18 months from each five year employment anniversary to take the leave. Sabbatical is fully company paid and has no restrictions. The time is yours to do with as you please.

People exercise all degrees of freedom with their sabbaticals. They go sailing, they go to South Sea islands, they ski some mountain nobody ever heard of, they trek in Nepal. Houses get fixed, cars restored and children played with.

For my third sabbatical I resolved to do absolutely nothing. For the first time in my life I was really tired, and I knew it. A six week rest sounded just fine. I'd walk the dog and spend time with my wife and son. That's it. No transistors, no resistors, no op amps and, above all, *no writing*. I was so written out the thought of picking up a pencil produced an instant headache.

The first week I really did do nothing but sleep, walk the dog, read and hang around with my wife and kid. Later, on the weekend, I went for a long, cold (top down) ride in the countryside, which, via some convoluted route, ended up at an electronic junk store. There I found a wonderfully pristine, albeit nonfunctional, Hewlett-Packard 215A pulse generator. This instrument, utilizing an exotic, step recovery diode based output stage, has clean, sub-nanosecond transitions. After the requisite economic arm wrestling at the counter, I bought the thing for twenty-five bucks.

I took it home, repaired it, and used it to characterize a fast coincidence detector (Figures 14–18 and associated text) I had previously abandoned. This exercise proved fatally catalytic. Things rapidly proceeded in a predictable direction. The result was a three week binge in the middle of my formerly restful sabbatical. Many of the circuits presented


here are refinements or adaptations of previous efforts, although some are new. Also included, and annotated as such, are other authors' works that seemed appropriate.

This publication's title is cursorily descriptive of its contents. A more studied accounting includes categories of data converters and signal conditioners, transducer circuits, oscillators and power converters. They begin immediately.

Micropower Voltage-to-Frequency Converters

Figure 1 is a voltage-to-frequency converter. A 0V to 5V input produces a 0Hz to 10kHz output, with a linearity of 0.02%. Gain drift is 60ppm/°C. Maximum current consumption is only 21 μ A, over 100 times lower than currently available monolithic ICs.

To understand circuit operation, assume that C1's negative input is slightly below its positive input (C2's output is low). The input voltage causes a positive-going ramp at C1's input (trace A, Figure 2). C1's output is high, allowing current flow from Q1's emitter, through C1's output stage to the 100pF capacitor. The 2.2 μ F capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The voltage to which the 100pF unit charges is a function of Q1's emitter potential and Q6's drop. C1's CMOS output, purely ohmic, contributes no voltage error. When the ramp at C1's negative input goes high enough, C1's output (trace B) goes low and the inverter switches high (trace C). This action pulls current from C1's negative input capacitor via the Q5 route (trace D). This current removal resets C1's negative input ramp to a potential slightly below ground. The 50pF capacitor furnishes AC positive feedback (C1's positive input is trace E) ensuring that C1's output remains negative long enough for a

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Application Note 75

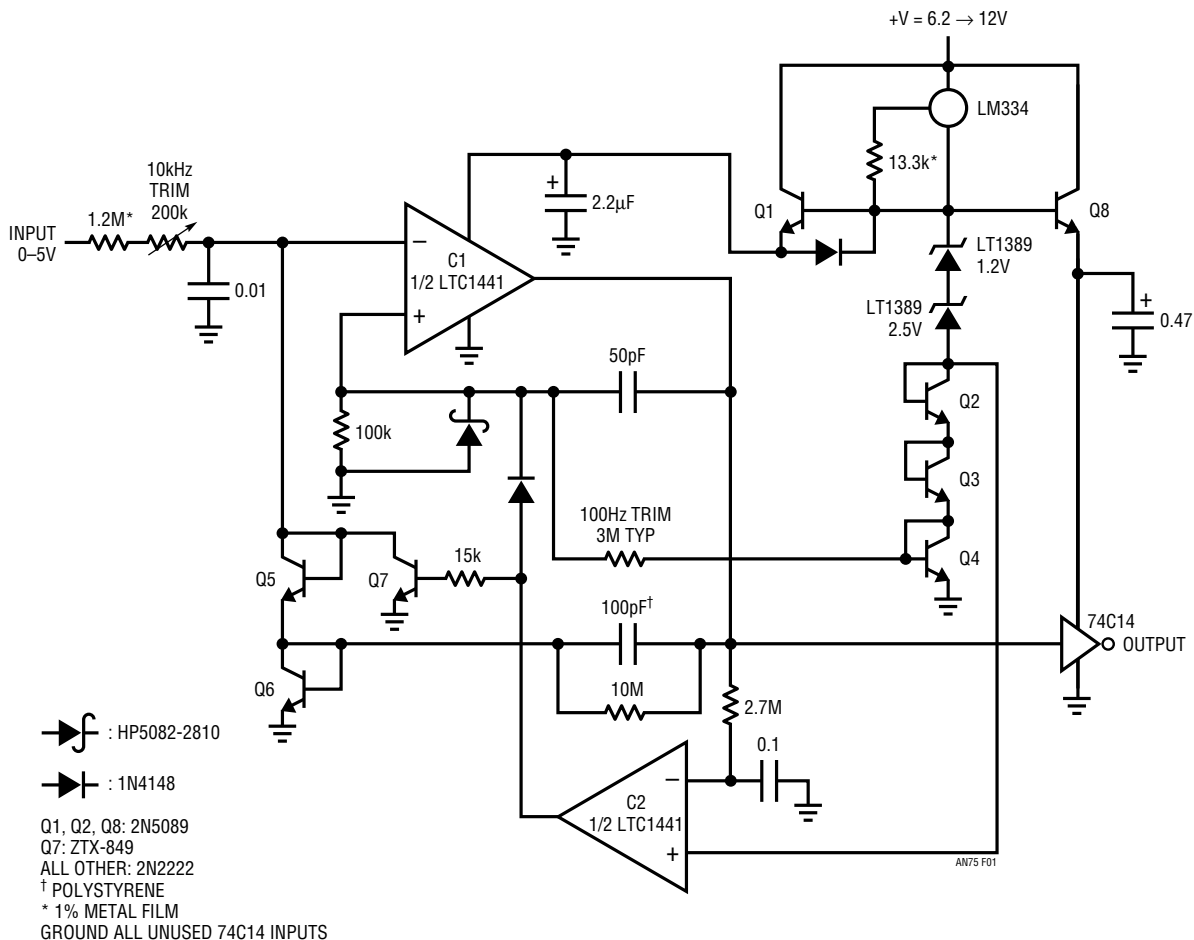


Figure 1. 0.02%, 0Hz to 10kHz Voltage-to-Frequency Converter Requires Only 21µA Supply Current

complete discharge of the 100pF capacitor. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 50pF units' feedback decays, C1 again switches high and the entire cycle repeats. The oscillation frequency depends directly on the input-voltage-derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE} . The two LT1389s are the actual voltage reference and the LM334 current source provides 5µA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by using the LM334's 0.3%/°C tempco to slightly temperature modulate the voltage drop in the Q2-Q4 trio. This correction's sign and magnitude directly oppose the -120ppm/°C 100pF polystyrene capacitor's drift, aiding overall circuit stability. Q8's isolated drive to the CMOS inverter prevents output loading from influencing Q1's

operating point. This makes circuit accuracy independent of loading.

The Q1 emitter-follower delivers charge to the 100pF capacitor efficiently. Both base and collector current end up in the capacitor. The 100pF capacitor, as small as desired performance permits, draws only small transient currents during its charge and discharge cycles. The 50pF-100k positive feedback combination draws insignificantly small switching currents. Figure 3, a plot of supply current vs operating frequency, reflects the low power design. At zero frequency, comparator quiescent current and the 5µA reference stack bias account for all current drain. There are no other paths for loss. As frequency scales up, the 100pF capacitor's charge-discharge cycle introduces the 1.1µA/kHz increase shown. A smaller value capacitor would cut power, but effects of stray capacitance and charge imbalance would introduce linearity and drift errors. Similarly, reduced reference stack drive would save current at the expense of drift.

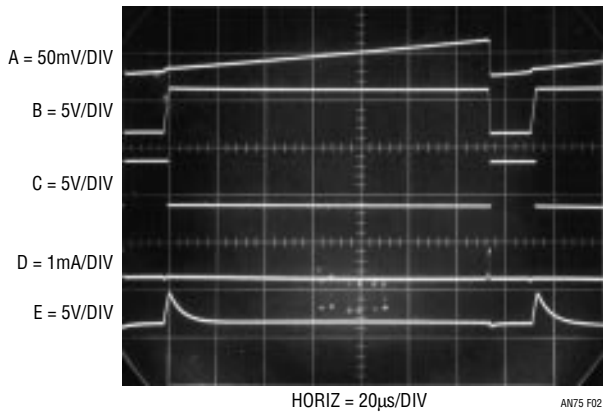


Figure 2. Waveforms for the Micropower Voltage-to-Frequency Converter. Charge-Based Feedback Provides Precision Operation with Extremely Low Power Consumption

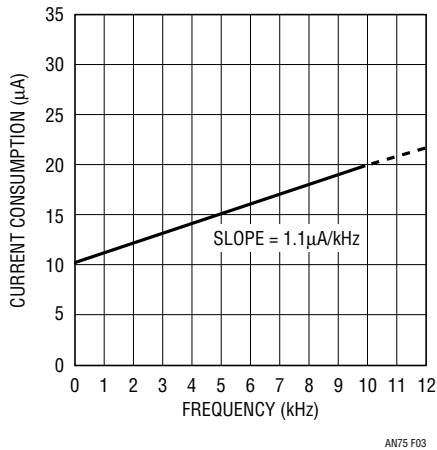


Figure 3. Current Consumption vs Frequency for the Voltage-to-Frequency Converter. Charge Dispensing Cycles Dominate 1.1µA/kHz Current Drain Increase

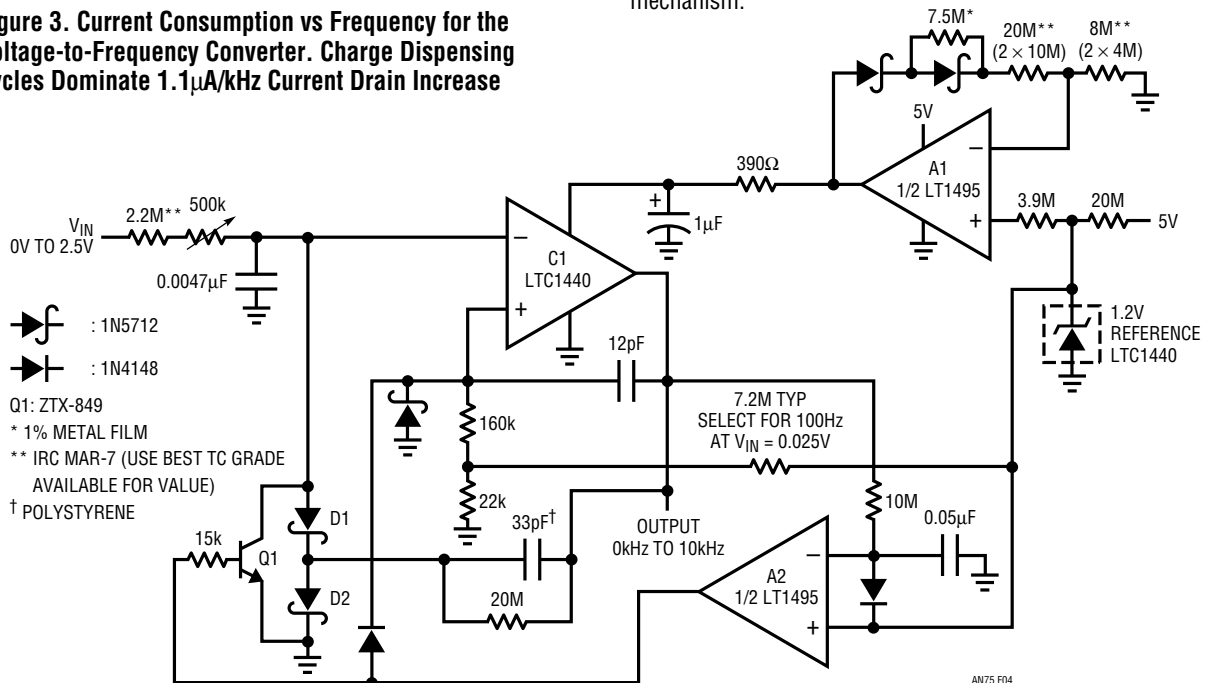


Figure 4. 0Hz to 10kHz Voltage-to-Frequency Converter Consumes Only 8.8µA. Circuit Is Similar to Figure 1. Reworked Reference Cuts Power, Although Linearity and Drift Degrade

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; C2, detecting this via the 2.7M–0.1µF lag, goes high. This lifts C1's positive input and grounds the negative input with Q7, initiating normal circuit action.

To calibrate this circuit, apply 50mV and select the indicated resistor at C1's positive input for a 100Hz output. Complete the calibration by applying 5V and trimming the input potentiometer for a 10kHz output.

Figure 4's circuit is quite similar, although a reworked reference cuts current drain to just 8.8µA and permits operation from a 5V supply (V_{IN} 3.4V to 36V). The penalty is degraded linearity and drift performance. A 0V to 2.5V input produces a 0Hz to 10kHz output, with 0.03% linearity, 250ppm/°C drift and 10ppm/V supply rejection. Maximum current consumption is only 8.8µA, 300 times lower than currently available ICs. Circuit AC operation is nearly identical to Figure 1, although a brief description follows.

Comparator C1 switches a charge pump comprising D1, D2 and the 33pF capacitor to maintain its negative input at 0V. A1 and associated components form a temperature compensating reference supply for the C1 based charge pump¹.

Note 1: Okay all you SPICE types out there, start your computers and model the charge pump drift and the reference compensation mechanism.

Application Note 75

The 1.2V reference biasing A1 is contained within C1's package. As such, a bootstrapped start-up is required. The 20M resistor provides this, while wasting less than 200nA.

The 33pF capacitor charges to a fixed voltage; hence, the switching repetition rate is the circuit's only degree of freedom to maintain feedback. Comparator C1 pumps uniform packets of charge to its negative input at a repetition rate precisely proportional to the input voltage derived current. This action ensures that circuit output frequency is strictly and solely determined by the input voltage.

Current consumption is extraordinarily low. Figure 4 shows only 5.4 μ A quiescent current, rising to 8.8 μ A at 10kHz. The 340nA/kHz slope directly relates to the charge dispensing losses.

Start-up or input overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; A2, detecting this via the 10M/0.05 μ F lag, goes high. This lifts C1's positive input and grounds the negative input with Q1, initiating normal circuit action.

It is worth noting that these voltage-to-frequency circuits are the beneficiaries of considerable attention over a protracted period of time. The evolution of these designs is detailed in Appendix A, "Some Guidelines for Micropower Design and an Example."

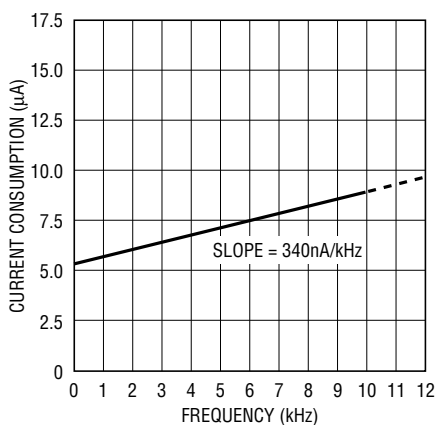


Figure 5. Current Consumption vs Frequency for Figure 4. Charge Dispensing Cycles Dictate 340nA/kHz Current Drain Increase

Micropower A/D Converters

In general, monolithic A/D converters have replaced discrete types. Occasionally, specific desirable circuit characteristics dictate a discrete design. Examples of such special cases include the need for a passive analog input, output data format, control protocol or economic constraints. Figure 6's 8-bit design consumes 12 μ A maximum, has 70ppm/ $^{\circ}$ C drift (<1 LSB 0° C to 70° C) and converts in 90ms. The circuit consists of a switched current source, an integrating capacitor, a comparator and a synchronized clock. When a pulse is applied to the convert command input (trace A, Figure 7) Q6 resets the 0.22 μ F capacitor to zero (trace B). Simultaneously, C1A goes low and Q5 conducts, biasing the LM334 based current source on. Additionally, Q4 conducts, causing the C1B based clock (trace D) to stop oscillating. During this interval the current source stabilizes, delivering its output to ground via Q6. When the convert command pulse falls the 0.22 μ F capacitor begins to ramp linearly. Concurrently, Q4 goes off, allowing the C1B clock to produce data output pulses (trace D). When the ramp voltage equals the E_x input, C1A switches high (trace C), biasing Q3 to stop the C1A clock. C1A's high state also cuts off Q5, shutting down the current source. Q5's gate going high bleeds a sub-microampere current through the 20M-Q1 path, maintaining ramp charging, but at a greatly reduced rate (this action is not readily discernible in Figure 7, but will be detailed). This insures overdrive for C1A while minimizing current source on-time, saving power. C1A's output pulse width (again, trace C) varies linearly with E_x 's value. The Q3-Q4 gating of C1B prevents the convert command induced portion of C1A's output from allowing clock pulses. Thus, the clock bursts appearing at the data output (trace D) are directly and solely proportional to E_x . For the arrangement shown, 256 pulses appear for a 2.5V full-scale input.

Some subtleties are involved to achieve stated circuit performance. Q2 and associated biasing values combine with the LM334's inherent 3300ppm/ $^{\circ}$ C temperature coefficient to keep current source drift inside 60ppm/ $^{\circ}$ C. Q2, lacking gold doping, temperature tracks the LM334 more closely than a small signal diode would. The 0.22 μ F integrating and 220pF clock capacitors, both polystyrene, ratiometrically cancel their temperature coefficients to within 5ppm/ $^{\circ}$ C. The specified resistors in the current

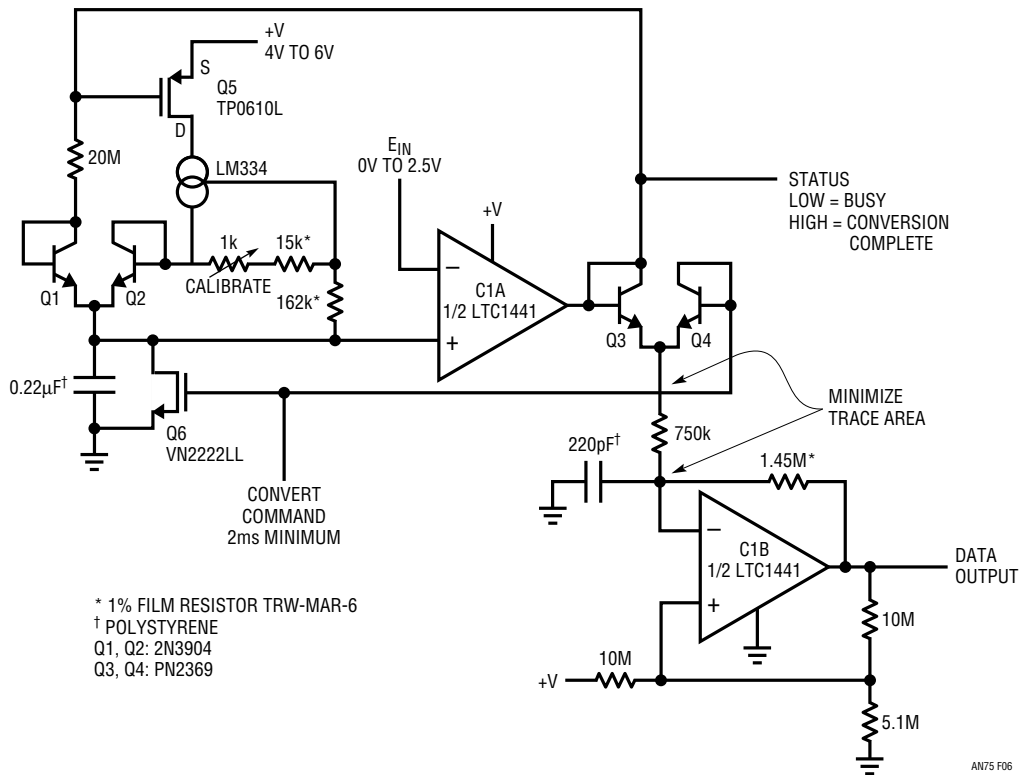


Figure 6. 8-Bit A/D Converter Consumes 12µA and Has Passive Input. Additional Features Include 7µA Quiescent Current, 70ppm/°C Drift and 90ms Conversion Time

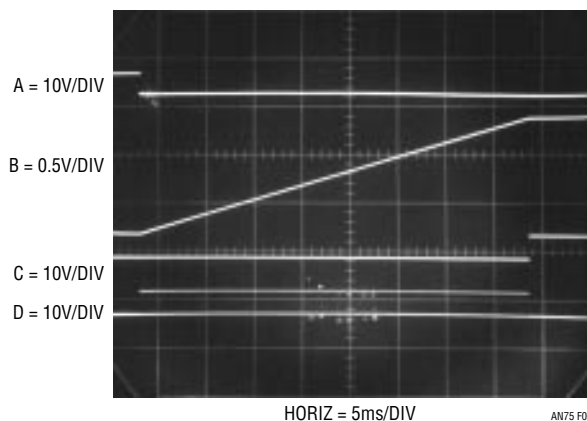


Figure 7. Waveforms for the 12µA A/D Converter ($E_{IN} = 1.25V$) Include Convert Command (A), Reference Ramp (B), Status Output (C) and Data Output (D). Segmented Ramp Slope Characteristic Is Not Discernable in Trace B

Application Note 75

source and clock have very low drift. The biasing at C1B's negative input synchronizes the clock oscillator to the conversion sequence, eliminating a ± 1 count error source. It also enforces predictable, optimum oscillator start-up, minimizing data jitter. Q3 and Q4 provide lower AC parasitics than diodes, enhancing clean oscillator gating. The converter typically holds 1LSB accuracy over 0°C to 70°C . Achievable conversion time varies with input. At tenth scale 16ms is possible, decreasing to 90ms at full scale.

Figure 8 details operation at $E_X = 80\text{mV}$. The segmented slope operation due to current source switching is easily seen under these conditions. Trace A is convert command, trace B Q5's drain, trace C the ramp, trace D C1A's output ("status" line), trace E C1B's negative input² and trace F the data output. Trace E shows the benefit of the aforementioned optimized biasing at C1B's negative input. Clock oscillations start immediately, with no untoward dynamics.

Figure 9 is a study of the segmented slope operation. The photograph, taken at a 180mV input, shows the ramp zero reset and clean switching. When Q5 is on, its drain (trace A, Figure 9) is high, turning on the current source. The current source linearly ramps the $0.22\mu\text{F}$ capacitor (trace

B) until C1A switches Q5 off. The current source then goes off, leaving the $20\text{M}\text{--}Q1$ path to continue the charging at a sub-microampere rate. This continued charging ensures that C1A is overdriven, preventing spurious outputs.

The current source operates at almost $5\mu\text{A}$. Turning it off after C1A switches saves considerable power, particularly at modest E_X values at high conversion rates. When Q5 switches the current source off, charging continues via the $20\text{M}\text{--}Q1$ path, but far less than a microampere is lost.

A/D power consumption is extremely low, due to the low power components and circuit configuration. Current consumption is $12\mu\text{A}$ for $E_X = 2.5\text{V}$ at a 10Hz conversion rate. Intermediate values of E_X and conversion rate result in less current drain, down to a minimum of $7\mu\text{A}$ at quiescence. Additional power savings are theoretically possible by running a lower current source value, but dynamics and temperature coefficient suffer. Further power economy is possible by shutting off the current source during capacitor reset, but accuracy degrades due to current source settling time requirements.

Note 2: Monitoring this high impedance AC node without incurring probe induced error involves special considerations. See Appendix B, "Parasitic Effects of Test Equipment in Micropower Circuits."

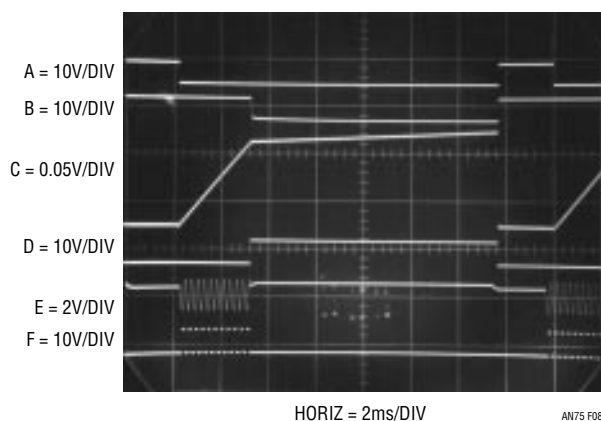


Figure 8. Detailed Operating Waveforms at $E_{IN} = 80\text{mV}$. Trace A Is Convert Command, B, Q5 Drain, C, Ramp, D, Status, E, Clock Capacitor and F, Data Out. Optimized Capacitor Biasing Ensures Immediate, Predictable Clock Start-Up. Segmented Ramp Slope is Viewable in Trace C

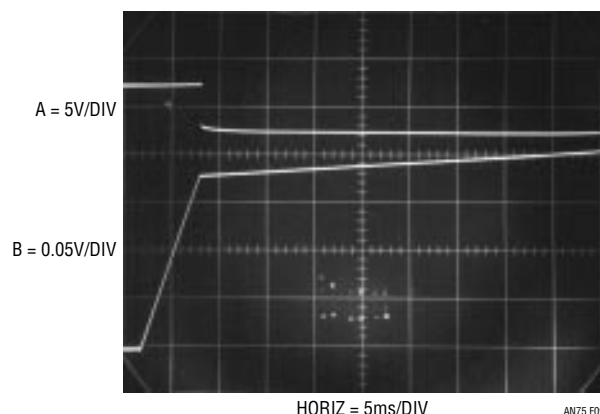


Figure 9. Expanded Detail of Segmented Slope Ramp (B) and Q5 Drain (A) at $E_{IN} = 180\text{mV}$. When Q5 Goes Off, Ramp Current Source Ceases, Saving Power. Ramp Capacitor Charging Continues at Greatly Reduced Rate Via 20M Resistor, Insuring Comparator Overdrive

10-Bit, Micropower A/D Converter

Figure 10 extends accuracy to 10 bits, while increasing conversion speed to 35ms. The trade off is current consumption, which increases to 29 μ A. The circuit's operation is nearly identical to the 8-bit version, although the current source and clock are redesigned for higher accuracy. The LT1389–2N3809 combination is the current source, with the 301k resistor specified to oppose the integrating capacitor's –120ppm/°C temperature coefficient. The clock employs a 32.768kHz “watch” crystal for stability³. The quartz crystal's high Q, resonant characteristic precludes direct oscillator gating as was done in the previous circuit. Instead, the clock is synchronized to the conversion sequence with a flip-flop, which in turn transmits the convert command to the converter.

These stability improvements allow 10-bit resolution with 1LSB of drift over 0°C to 70°C. At a 10Hz conversion rate with $E_{IN} = 3V$ current drain is 29 μ A, decreasing to 21 μ A at quiescence. As in the previous circuit, different values of E_{IN} and conversion rate result in intermediate amounts of current consumption.

Differential Input, 10MHz RMS/DC Converter

Wideband, thermally based RMS/DC conversion has previously been described, utilizing single-ended inputs⁴. Figure 11's 10MHz RMS/DC converter has differential inputs while maintaining 1% accuracy beyond 10MHz. A 1V_{RMS} differential input produces 10V DC at the output.

The wideband LT1207 dual power op amp receives the differential inputs. The amplifiers, connected for a differential gain of 10, feed the LT1088 RMS/DC converter. The 24pF–5k trim provides a high frequency gain boost, preserving accuracy at the highest frequencies.

The LT1088 based RMS/DC converter is made up of matched pairs of heaters and diodes and a control amplifier. The A1–A2 amplifiers drive R1, producing heat which lowers D1's voltage. Differentially connected A3 responds by driving R2, via Q3, to heat D2, closing a loop around the amplifier. Because the diodes and heater resistors are matched, A3's DC output is related to the RMS value of the input, regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain

Note 3: A detailed description of this clock circuit appears in the text associated with Figure 27.

Note 4: For examples, see references 10 through 13.

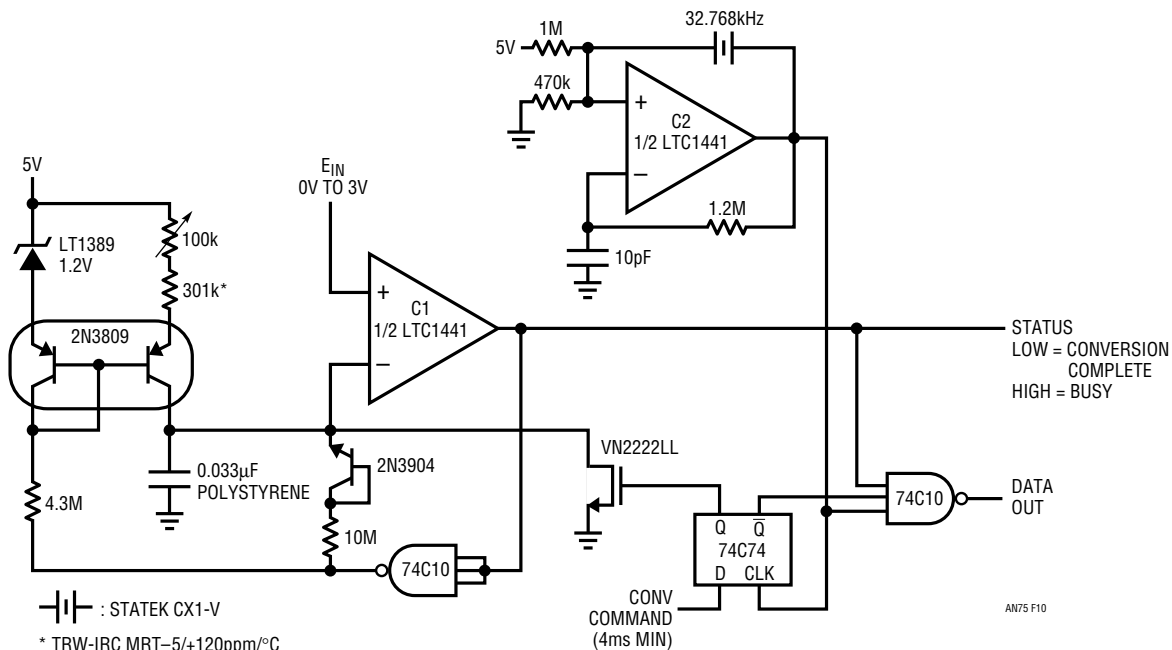


Figure 10. A 10-Bit Version of Figure 6. Improvements Include Higher Stability Clock and Current Source. Modifications Permit 1LSB Drift (0°C to 70°C) and 35ms Conversion Speed, Although Current Drain Increases to 29 μ A

Application Note 75

trim, which is implemented at A4. A4's output is the circuit output. The LT1004 and associated components frequency compensate the loop and provide good settling time over wide ranges of operating conditions.

Start-up or input overdrive can cause A2 to deliver excessive current to the LT1088 with resultant damage. C1 and C2 prevent this. Overdrive forces D1's voltage to an abnormally low potential. C1 triggers low under these conditions, pulling C2's input low. This causes C2's output to go high, putting A1 and A2 into shutdown and terminating the overload. After a time determined by the RC at C2's input, A1 and A2 will be enabled. If the overload condition

still exists the loop will almost immediately shut A1 and A2 down again. This oscillatory action will continue, protecting the LT1088 until the overload condition is removed.

Performance for the circuit is quite impressive. Figure 12 plots error with one input driven at two different gain boost network trims. The graph (B) shows 1% error bandwidth to 11MHz. The slight peaking out to 5MHz is due to the A1–A2 gain boost network. This peaking is minimal compared to the total error envelope, and a small price to pay to get 1% accuracy to 11MHz. One percent accuracy to 14MHz is available if the gain trim and boost network are set to accentuate peaking at the expense of flatness (A).

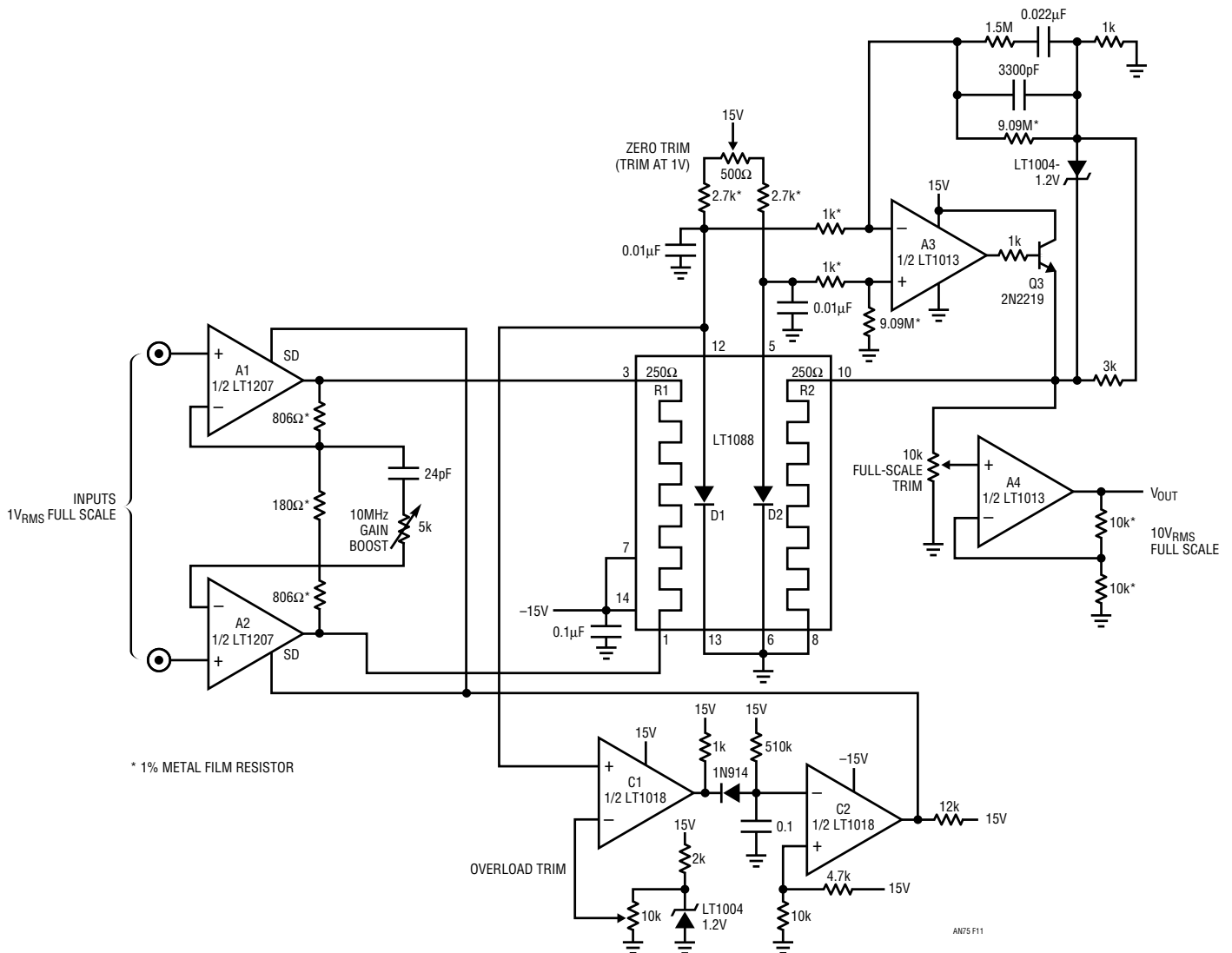
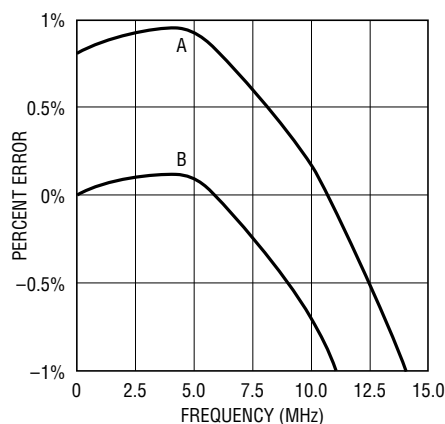


Figure 11. Differential Input 10MHz RMS/DC Converter Has 1% Accuracy, High Input Impedance and Overload Protection. Single-Ended Operation Extends 1% Error Bandwidth to 14MHz

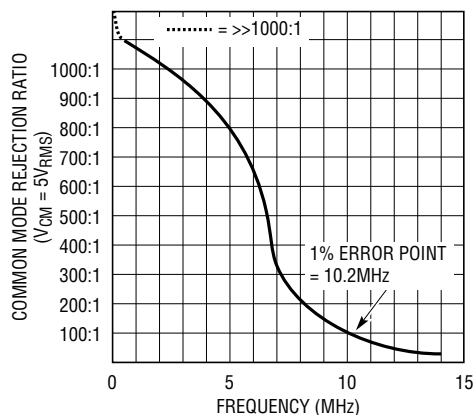
Figure 13 shows effects of common mode signals on accuracy. This data was taken with a well shielded, carefully layed out breadboard. Common mode rejection ratio remains high as frequency scales, contributing negligible error until 10.2MHz. The indicated 5V_{RMS} common mode drive is a demanding test, with smaller values permitting better performance.

To trim this circuit put the 5kΩ potentiometer at its maximum resistance position and apply a 100mV, 5MHz signal. Trim the 500Ω adjustment for exactly 1V_{OUT}. Next, apply a 5MHz 1V input and trim the 10k potentiometer for 10.00V_{OUT}. Finally, put in 1V at 10MHz and adjust the 5kΩ trimmer for 10.00V_{OUT}. Repeat this sequence until circuit output is within 1% accuracy for DC–10MHz inputs. Two passes should be sufficient. The overload trim is set at 10% below D1's voltage with the circuit operating at full scale.



AN75 F12

Figure 12. Error Plot for the Differential Input RMS/DC Converter with One Input Driven. Frequency Dependent Gain Boost Preserves 1% Accuracy, But Causes Slight Peaking Before Roll-Off. Boost Is Settable for Maximum Bandwidth (A) or Minimum Error (B)



AN75 F13

Figure 13. Common Mode Rejection Ratio vs Frequency for the Differential Input RMS/DC Converter. Layout, Amplifier Bandwidth and AC Matching Characteristics Determine Curve

Application Note 75

3 Nanosecond Coincidence Detector

Figure 14's circuit, detecting coincident voltage levels at its inputs, responds with a logical high at its output. The detection trigger level is settable between zero and 4.0V. The circuit will resolve coincidence down to 3ns and has a decision delay time of 4.5ns. The circuit is composed of a pair of fast level discrimination comparators and a sub-nanosecond AND gate. The comparators balance each input against a level threshold, in this case about 1V. The

comparator outputs feed Q1 and associated components, which form a 300ps AND gate. Figure 15's waveforms show circuit operation. Trace A is one input, while trace B is the remaining input. Trace C is the circuit output. When trace B crosses the 1V recognition threshold the output goes high, remaining high until either input (in this case trace B) drops below 1V. The key to this circuit's speed is the fast comparators and the discrete AND gates extremely low delay.

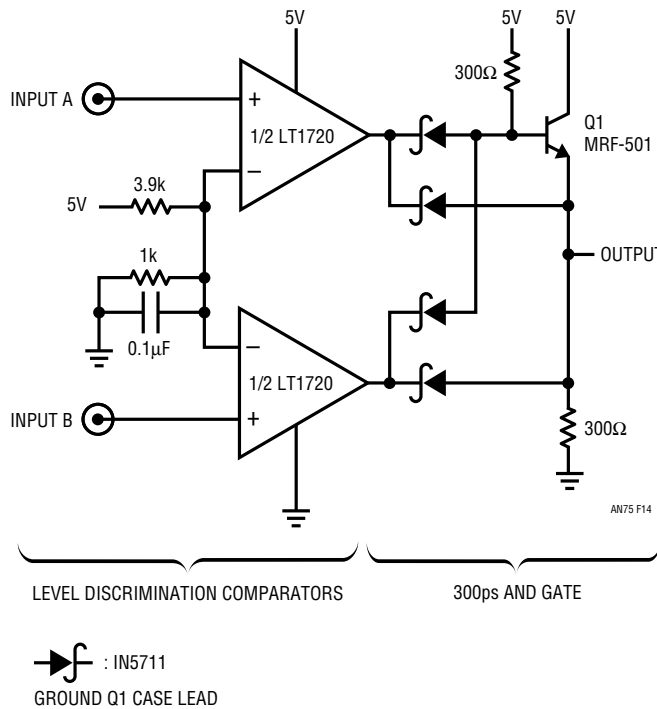


Figure 14. Coincidence Detector Has 3ns Recognition Threshold. Discrete Components Form 300ps AND Gate, Maintaining High Speed Signal Path

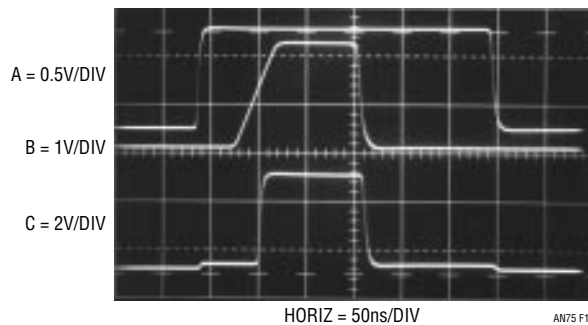


Figure 15. Coincidence Detector Waveforms. Trace A Is Input A, B Is Input B. Trace C Indicates Coincidence When A and B Are Both >1V

Evaluating circuit performance requires a sub-nanosecond rise-time pulse generator and a very fast oscilloscope⁵. Figure 16, taken in a 3.9GHz sampled bandpass, shows a comparator output (trace A) and the resultant circuit output (trace B). The Schottky diodes and gigahertz range transistor provide very fast response, and delay is inside 300ps.

Figure 17 shows circuit response in a 3.9GHz sampled bandpass with the inputs simultaneously driven by a 3ns, 2V pulse (trace A). This pulse width is just inside the recognition limit, and the output (trace B) responds cleanly.

The 4.5ns decision delay characteristic is also readily apparent. Further input pulse width reduction has dramatic results⁶. In Figure 18 input width (trace A) is shortened by 600ps. The output (trace B) is caught not quite fully responding. It rises about 2V before falling back in a noisy but controlled decay. The rise slope, degraded from Figure 17's, is additional evidence of circuit gain-bandwidth limitations.

Note 5: Refer to this publication's introduction.

Note 6: I offer no apology for the choice of verbiage. Nerds like me find drama in these things.

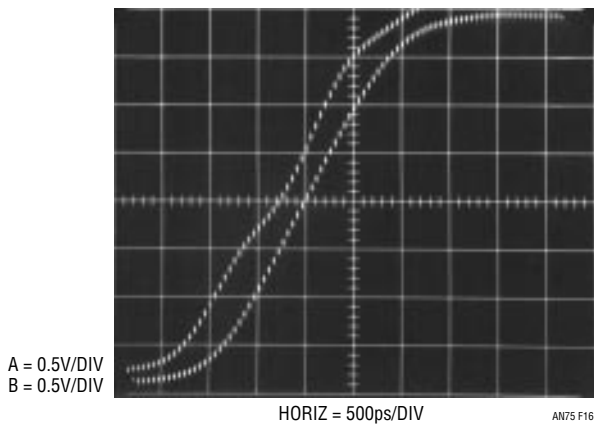


Figure 16. 300ps AND Gate Delay Measured from Comparator Output (A) to Q1 Emitter (B). Fall Time Delay Is Similar. Sampling Oscilloscope Display Presents as a Series of Dots

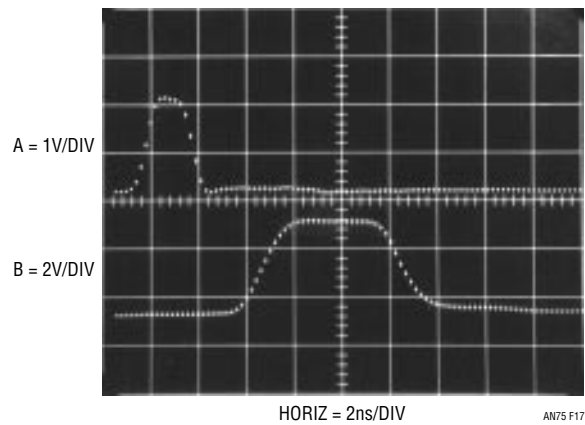


Figure 17. Output (B) Recognizing a 3ns Coincident Pulse (A) at Inputs. Response Is Clean, with Decision Delay of 4.5ns. Segmented Display Is Characteristic of Sampling 'Scope Operation

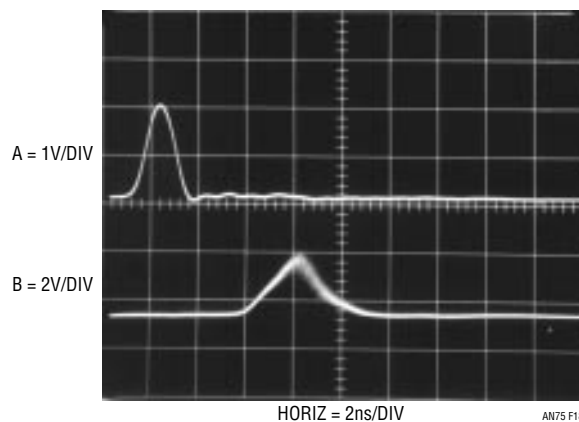


Figure 18. An Unrecognized Coincidence. Output (B) Cannot Fully Respond to ≈ 2.5 ns Coincident Pulse (A). Additional 500ps of Coincidence Would Permit Valid Recognition (See Previous Figure)

Application Note 75

15 Nanosecond Waveform Sampler

Figure 19 is another high speed circuit. This waveform sampler has 15ns response and a gain of 10. The circuit is made up of a fast, low parasitic switch, its drive components and an output amplifier. The switch is formed by the diode bridge. Borrowed from classical sampling oscilloscope circuitry, it is the key to circuit performance⁷. The diode bridge's inherent balance eliminates charge injection based errors in the output. It is far superior to other electronic switches in this characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive

artifacts to corrupt switch output. The diode bridge's balance, combined with matched, low capacitance monolithic diodes and complementary high speed switching, yields a cleanly switched output. Trims optimize switch performance. DC balance is achieved by trimming the bridge on-current for zero input-output offset voltage. Two AC trims are required. The "AC balance" corrects for diode and layout capacitive imbalances and the "skew compensation" corrects for any timing asymmetry in the nominally complementary bridge drive. These AC trims compensate small dynamic imbalances that could result in parasitic switch outputs.

Note 7: See references 14 and 15 for design details of diode bridge switches.

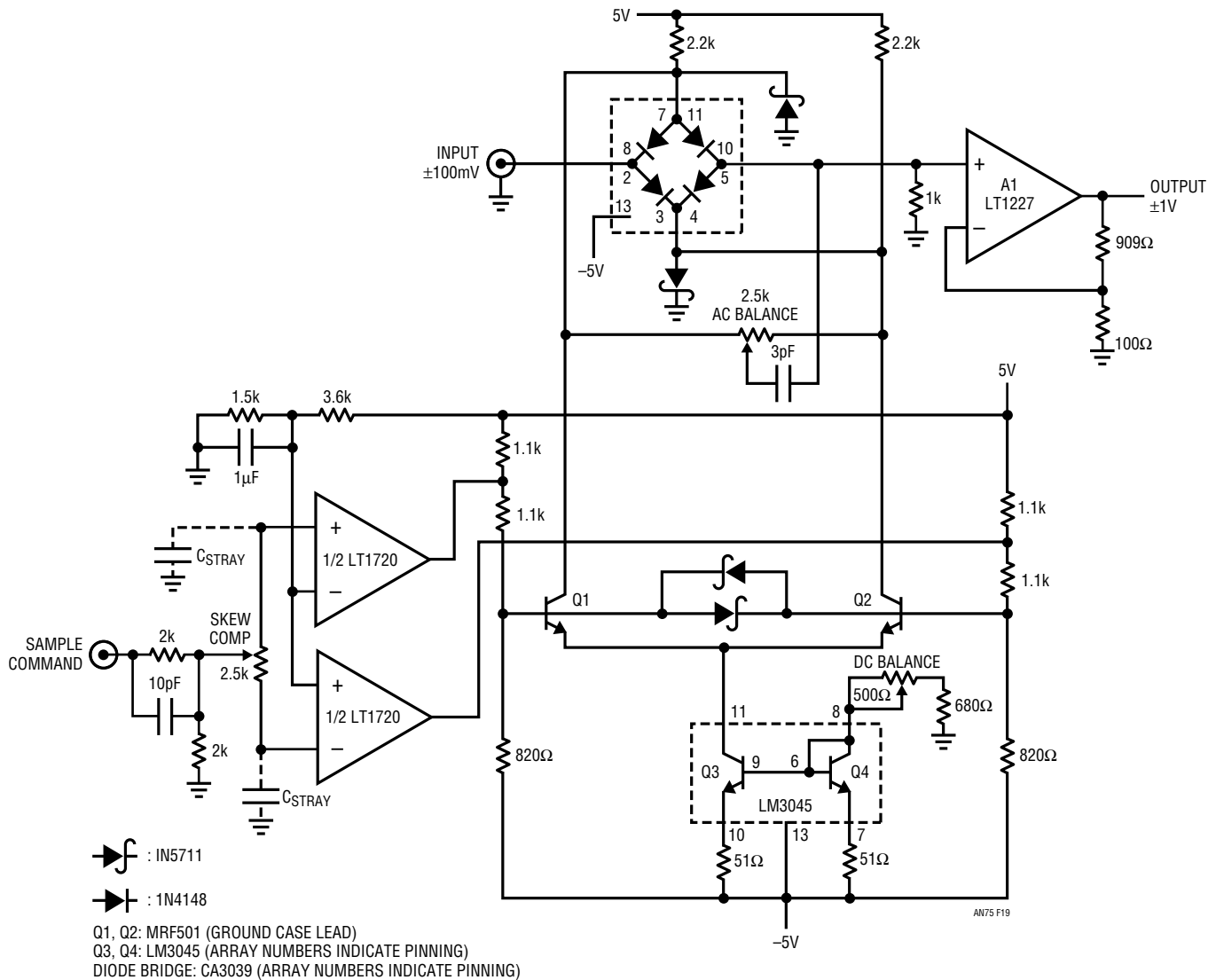


Figure 19. 15ns Waveform Sampler Utilizes Diode Bridge Switch and Wideband x10 Amplifier. Comparators and Associated Components Provide Optimized Diode Bridge Switching

The sample command biases the LT1720 comparators, which furnishes complementary levels to the Q1–Q2 switch drivers. The “skew compensation” trim, working differentially against stray and device capacitance, provides a way to slightly time skew the comparators response. The comparator outputs bias current sink loaded Q1–Q2⁸. These devices provide level shifted drive to the bridge. Bridge output feeds A1, a wideband amplifier, operating at a gain of 10. Figure 20 presents waveforms. Trace A is the sample command, trace B and C complementary bridge drives at the Q1–Q2 collectors and trace D the output.

Figure 21, an amplitude and time expanded view, shows more detail. Trace assignments are identical, although scale factors are changed. A small delay occurs between the sample command (trace A) and the complementary bridge drives (traces B and C), although no drive time skewing is evident. Trace D, the output, responds cleanly, with some switch induced pre-shoot before falling.

Trimming is required to optimize sampler performance. DC balance is adjusted first. Ground the input and connect the sample command to the 5V supply. Monitor the output

and adjust the “DC balance” for 0V. The AC trims are made dynamically. Connect the input to a *well bypassed* 50mV DC source and drive the sample command with a 1MHz square wave. A typical pre-trim sampler output appears in Figure 22. The pre-shoot (waveform bottom) is due to poor AC balance. The mid-transition discontinuity is characteristic of untrimmed skew compensation. In general, poor AC balance shows up as pronounced pre or post transition events, while unadjusted skew compensation causes distortion during the transition. When properly trimmed, circuit output should be devoid of all such behavior. Figure 23 shows this; only very slight disturbances (probably due to residual AC imbalance) are visible.

Pertinent performance specifications include 100 μ V/ $^{\circ}$ C drift, 15ns delay time, 10MHz full-power bandwidth and a minimum sample window for full-power response of 30ns.

Note 8: The bridge drive scheme presented here is variant of a circuit developed by George Feliz (LTC). See LTC Application Note 74, “Component and Measurement Advances Ensure 16-Bit DAC Settling Time.”

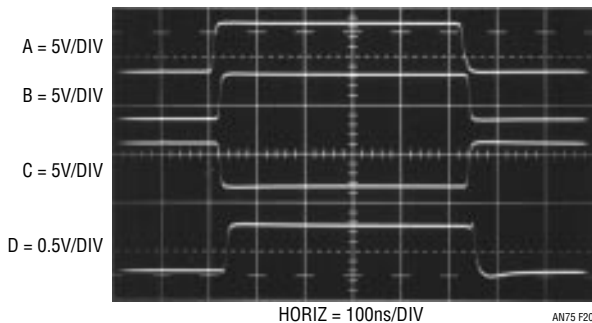


Figure 20. Sampler Operation at 50mV Input. Trace A Is Sample Command, B and C Complementary Bridge Drives. Trace D Is Output

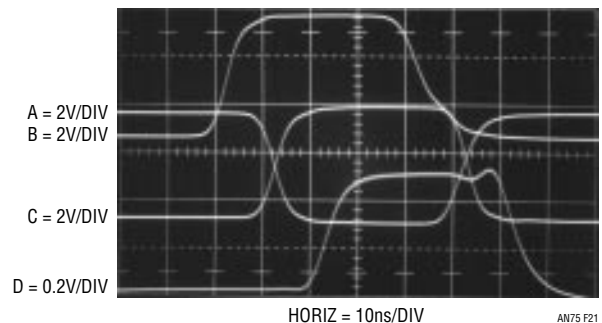


Figure 21. Highly Expanded View of Figure 20 Has Same Trace Assignments. Bridge Switching Appears Unskewed and Output Responds Cleanly

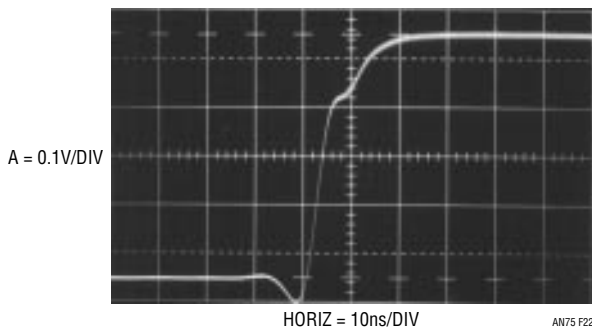


Figure 22. Sampler Output Before Trimming. Aberration at Bottom Is Due to Misadjusted AC Balance. Mid-Transition Discontinuity Derives from Untrimmed Skew Compensation

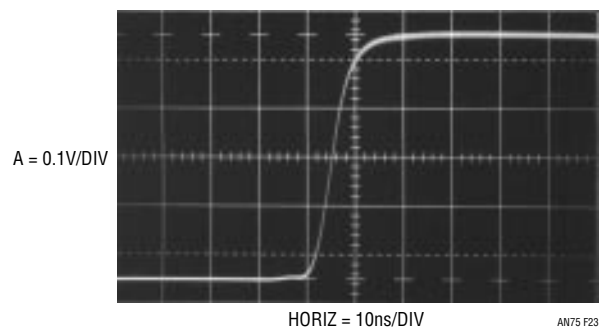


Figure 23. Sampler Output After Optimizing AC Balance and Skew Compensation

Application Note 75

5.5 μ A Powered, 0.05 μ V/ $^{\circ}$ C Chopped Amplifier

Figure 24 shows a chopped amplifier that requires only 5.5 μ A supply current. Offset voltage is 5 μ V, with 0.05 μ V/ $^{\circ}$ C drift. A gain of 10^8 affords high accuracy, even at large closed-loop gains.

The micropower comparators form a biphas 5Hz clock. The clock drives the input related switches, causing an amplitude-modulated version of the DC input to appear at A1A's input. AC-coupled A1A takes a gain of 1000, presenting its output to a switched demodulator similar to the aforementioned modulator.

The demodulator output, a reconstructed, DC-amplified version of the circuit's input, is fed to A1B, a DC gain stage. A1B's output is fed back, via gain setting resistors, to the

input modulator, closing a feedback loop around the entire amplifier. The configuration's DC gain is set by the feedback resistor's ratio, in this case 1000.

The circuit's internal AC coupling prevents A1's DC characteristics from influencing overall DC performance, accounting for the extremely low offset uncertainty noted. The high open-loop gain permits 10ppm gain accuracy at a closed-loop gain of 1000.

The desired micropower operation and A1's bandwidth dictate the 5Hz clock rate. As such, resultant overall bandwidth is *low*. Full-power bandwidth is 0.05Hz with a slew rate of about 1V/s. Clock-related noise, about 5 μ V, can be reduced by increasing C_{COMP} , with commensurate bandwidth reduction.

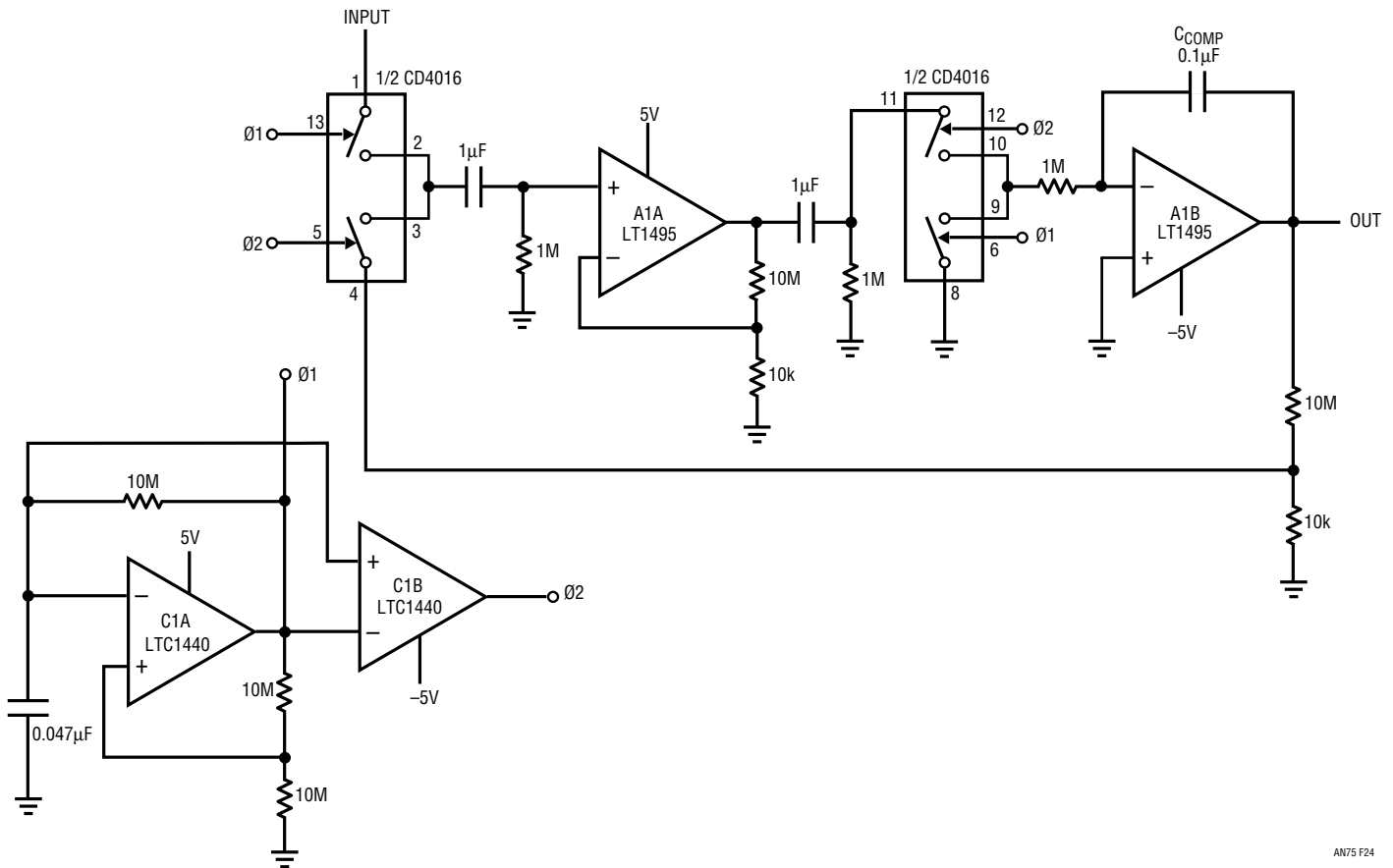


Figure 24. 0.05 μ V/ $^{\circ}$ C Chopped Amplifier Consumes Only 5.5 μ A Supply Current

Pilot Light Flame Detector with Low-Battery Lockout

Figure 25 shows a pilot light flame detector with low-battery lockout. The amplifier (“A”), running open loop, compares a small portion of the reference with the thermocouple-generated voltage. When the thermocouple is hot, the amplifier’s output swings high, biasing Q1 on. Hysteresis, provided by the 10M resistor, ensures clean transitions, while the diodes clamp static generated voltages to the rails. The 100k–2.2μF RC filters the signal to the amplifier.

The comparator (“C”) monitors the battery voltage via the 2M–1M divider and compares it to the 1.2V reference. A battery voltage above 3.6V holds C’s output high, biasing Q2 on and maintaining the small potential at A’s negative input. When the battery voltage drops too low, C goes low, signaling a low-battery condition. Simultaneously, Q2 goes off, causing A’s negative input to move to 1.2V. This biases A low, shutting off Q1. The low outputs alert downstream circuitry to shut down gas flow.

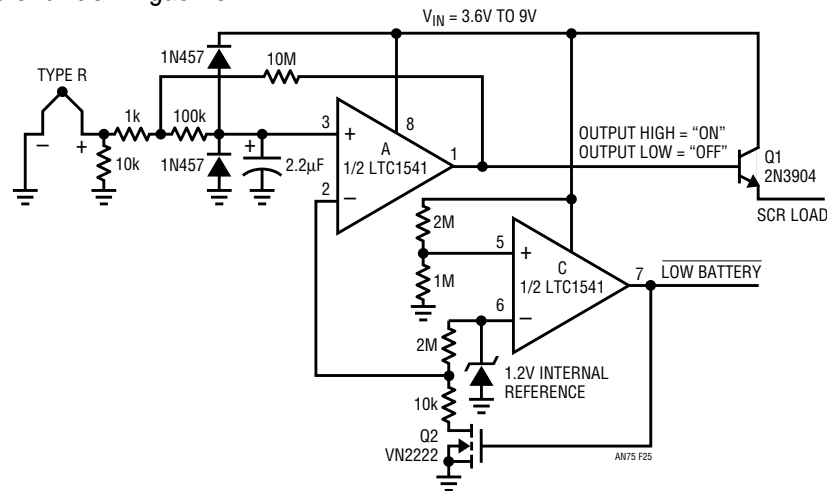
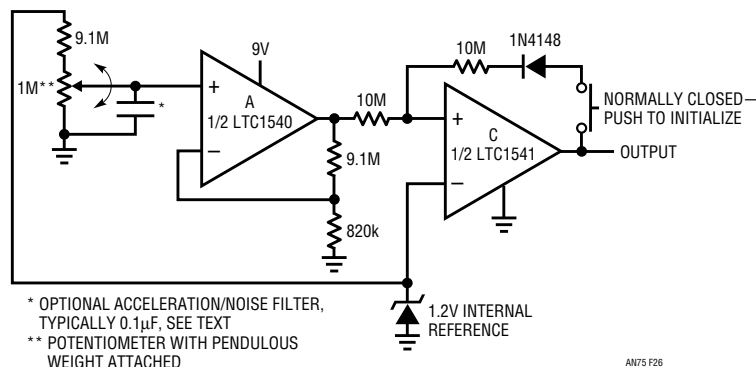


Figure 25. Pilot Light Flame Detector with Low-Battery Lockout



* OPTIONAL ACCELERATION/NOISE FILTER, TYPICALLY 0.1μF, SEE TEXT
 ** POTENTIOMETER WITH PENDULOUS WEIGHT ATTACHED

Figure 26. Tip-Acceleration Detector for Shipping Containers Retains Output If Triggered. Sensitivity Is Adjustable Via Amplifier Feedback Values. Capacitor Sets Acceleration Response Bandwidth

Application Note 75

32.768kHz “Watch Crystal” Oscillator

Figure 27’s quartz oscillator, using a standard 32.768kHz “watch crystal,” starts under all conditions with no spurious modes. Current draw is only 9 μ A at a 2V supply.

The circuit is best understood by initially ignoring the crystal. Resistors at the positive input establish a DC bias point. The 1.2M–10pF path sets up phase shifted negative feedback and the circuit looks like a marginally stable unity gain follower at DC. When the crystal is realized, positive feedback occurs and oscillation commences at the crystal’s resonant frequency.

Power consumption is low. The LTC1441’s output stage design eliminates “totem” currents, maintaining low drain even as supply increases. Figure 28’s plot shows 9 μ A drain at 2V supply, increasing linearly to 18 μ A at 5V supply. Current drain is reducible by altering component values, but erratic crystal start-up or parasitic modes may result. This is particularly the case if various brands of crystal are employed. The values given represent a compromise between minimized current drain and assured operation.

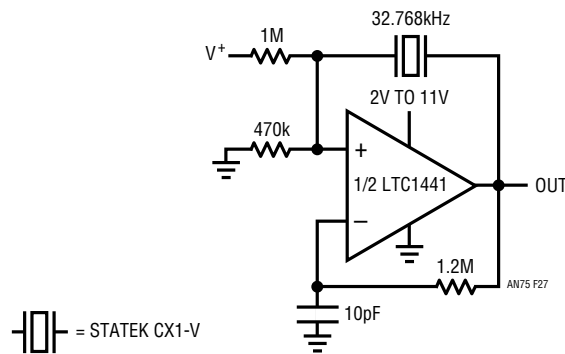


Figure 27. 32.768kHz “Watch Crystal” Oscillator Has No Spurious Modes. Circuit Pulls 9 μ A at $V_S = 2V$

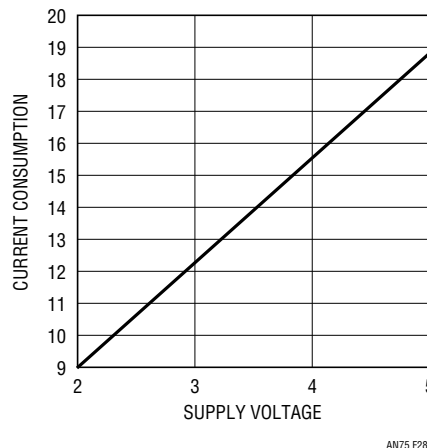


Figure 28. Current Consumption vs Supply Voltage for the 32.768kHz Crystal Oscillator. Characteristic Is Essentially Linear

Complementary Output, 50% Duty Cycle Crystal Oscillator

Figure 29's circuit, developed jointly by Joe Petrofsky (LTC) and the author, uses the LT1720 dual comparator in a 50% duty cycle crystal oscillator. Output frequencies to 10MHz are practical.

Resistors at C1's positive input set a DC bias point. The 2k–0.068μF path furnishes phase-shifted feedback and C1 acts like a wideband, unity-gain follower at DC. The crystal's path provides resonant positive feedback and stable oscillation occurs. C2, sensing C1's input, provides a delay matched, low skew, complementary output. A1 compares band limited versions of the outputs and biases C1's negative input.

Because frequency is fixed, C1's only degree of freedom to respond is variation of pulse width; hence, the outputs are forced to 50% duty cycle.

The circuit operates with AT-cut fundamental crystals from 1MHz to 10MHz, over a 2.7V to 6V power supply range. All biasing is supply derived, and hence ratiometric. As such, 50% duty cycle is maintained at all supply voltages, with output skew below 800ps. Figure 30 plots skew, which is seen to vary by about 800ps over a 2.7V to 6V supply excursion.

It is noteworthy that any desired duty cycle may be obtained by summing current into either of A1's inputs. If this is done, the current should derive directly from the supply or supply rejection will be compromised.

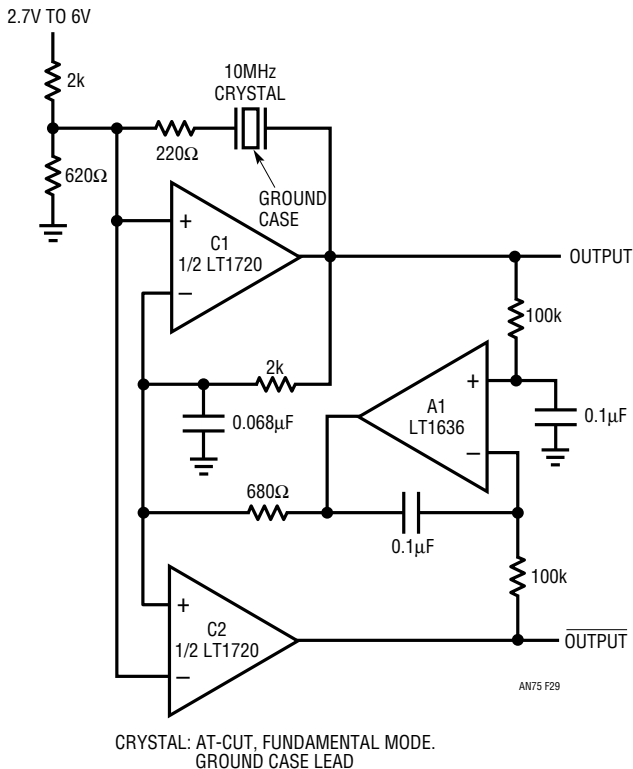


Figure 29. Crystal Oscillator Has Complementary Outputs and 50% Duty Cycle. A1's Feedback Maintains Output Duty Cycle Despite Supply Variations

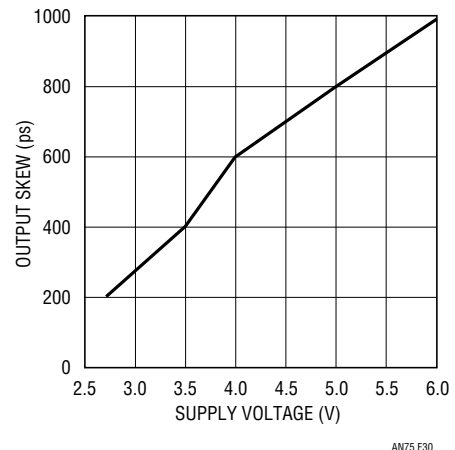


Figure 30. Output Skew vs Supply for 10MHz Clock. Skew Varies Only 800ps Over 2.7V to 6V Supply Excursion

Application Note 75

Nonoverlapping, Complementary Output Crystal Oscillator

Figure 31, an extension of the previous design, generates a nonoverlapping, complementary output crystal clock. The circuit is essentially identical to Figure 29, with the exception that C2 receives attenuated bias. This causes the outputs to have a nonoverlapping characteristic. Under these conditions, the only way A1 can balance its

inputs is if the circuit outputs have identical output duty. The nonoverlapping operation is verified in Figure 32, which shows the circuit's output. The outputs transition crisply, with no detectable overlap. This circuit shares the previous version's supply immunity due to ratiometric biasing. If the A1 network is deleted output duty will be unequal, but nonoverlapping operation retained.

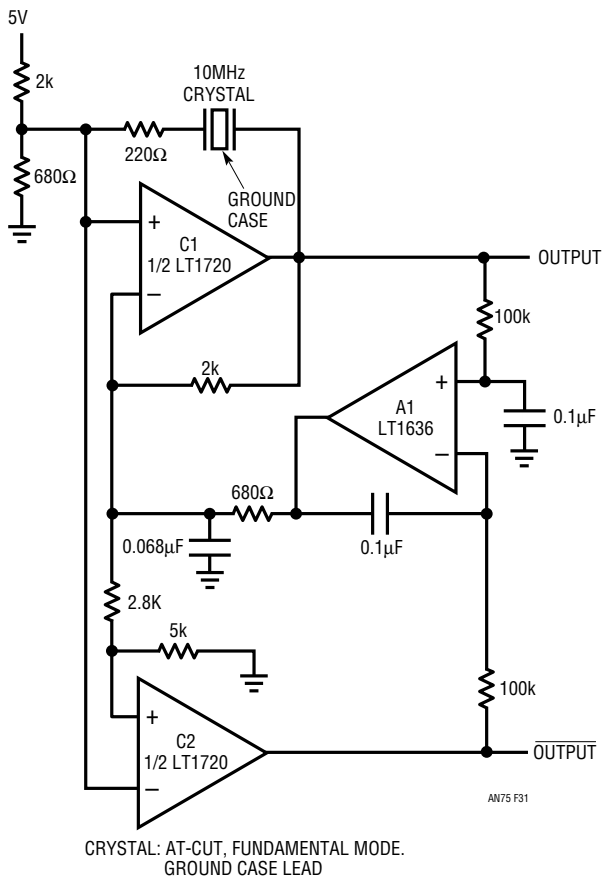


Figure 31. Rearranging Figure 29's Comparator Biasing Provides Nonoverlapping Complementary Outputs

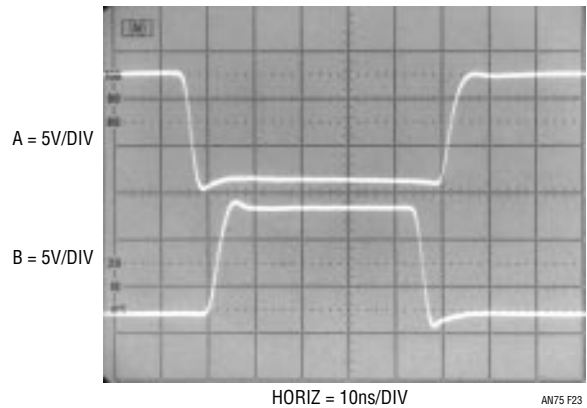


Figure 32. Nonoverlap Characteristic Verified in a 275MHz Bandpass

High Power CCFL Backlight Inverter for Desktop Displays

Large LCD (liquid crystal display) displays designed to replace CRTs (cathode ray tubes) in desktop computer applications are becoming available. The LCD's reduced size and power requirements allow much smaller product size, a highly desirable feature.

CRT replacement requires a 10W to 20W inverter to drive the CCFL (cold cathode fluorescent lamp) that illuminates the LCD. Additionally, the inverter must provide the wide dimming range associated with CRTs, and it must have safety features to prevent catastrophic failures.

Figure 33's circuit meets these requirements. It is a modified, high power variant of an approach employed in laptop computer displays⁹. T1, Q1, Q2 and associated components form a current fed, resonant Royer converter that produces high voltage at T1's secondary. Current flows through the CCFL tubes and is summed, rectified and filtered, providing a feedback signal to the LT1371 switching regulator. The LT1371 delivers switched mode power to the L1-D1 node, closing a control loop around the Royer converter. The 182Ω resistor provides current-to-voltage conversion, setting the lamp current operating

Note 9: See reference 21.

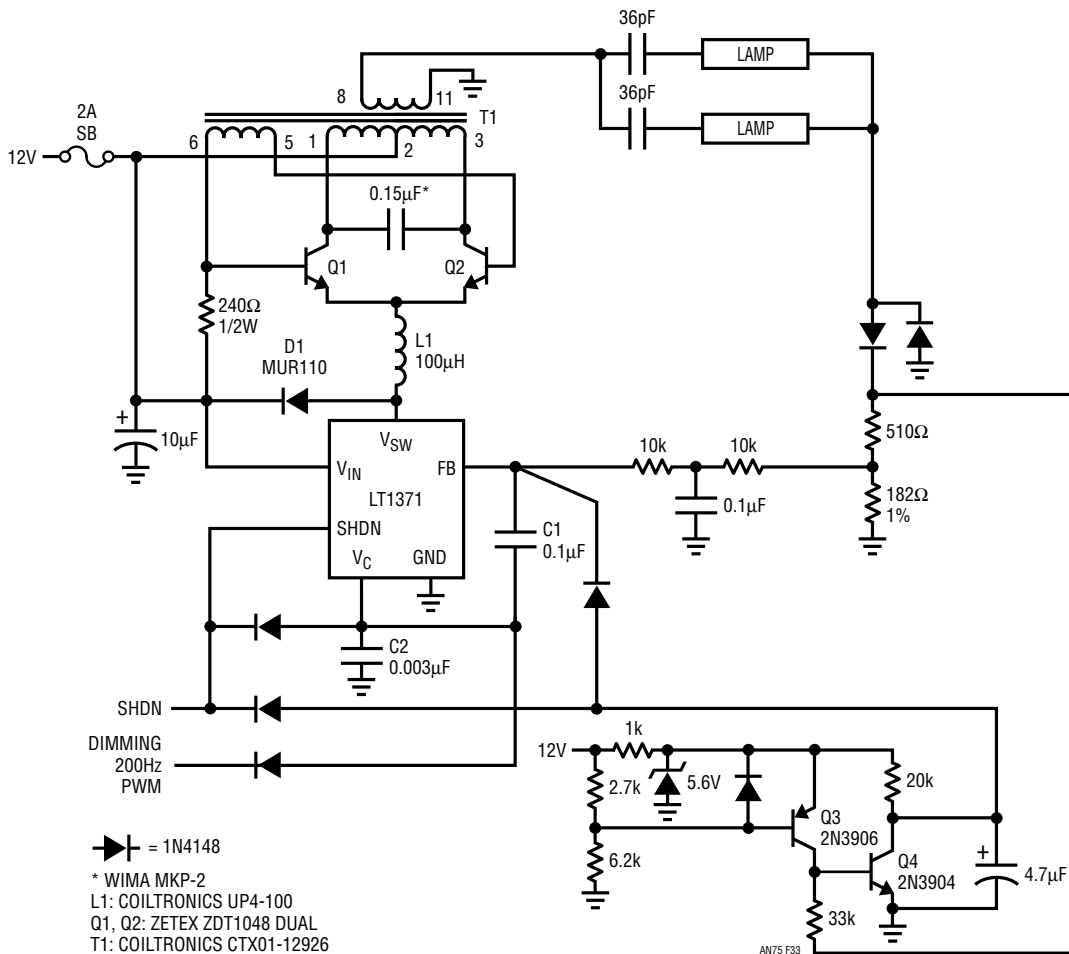


Figure 33. 12W CCFL Backlight Inverter for Desktop Displays Provides Wide Range Dimming and Safety Features

Application Note 75

point. The loop stabilizes lamp current against variations in time, supply, temperature and lamp characteristics. The LT1371's frequency compensation is set by C1 and C2. The compensation responds quickly enough to permit the 200Hz PWM input to control dimming over a 30:1 range with no degradation in loop regulation. Applicable waveforms appear in Figure 34.

Q3 and Q4 shut down the circuit if lamp current ceases (open or shorted lamps or leads, T1 failure or similar malfunction). Normally, Q4's collector is held near ground by the lamp-current-derived base biasing. If lamp current ceases, Q4's collector voltage increases, overdriving the feedback node and shutting down the circuit. Q3 prevents unwanted shutdown during power supply turn-on by driving Q4's base until supply voltage is above about 7V.

Figure 35 shows the shutdown circuit reacting to the loss of lamp feedback. When lamp feedback ceases, the voltage across the 182Ω current sense resistor drops to zero (visible between Figure 35's third and fourth vertical graticule lines, trace A). The LT1371 responds to this open-loop condition by driving the Royer converter to full power (Q1's collector is trace B). Simultaneously, Q4's collector (trace C) ramps up, overdriving the LT1371's feedback node in about 50ms. The LT1371 stops switching, shutting off the Royer converter drive. The circuit remains in this state until the failure has been rectified.

This circuit's combination of features provides a safe, simple and reliable high power CCFL lamp drive. Efficiency is in the 85% to 90% range. The closed-loop operation ensures maximum lamp life while permitting extended dimming range. The safety feature prevents excessive heating in the event of malfunction and the use of off-the-shelf components allows ease of implementation.

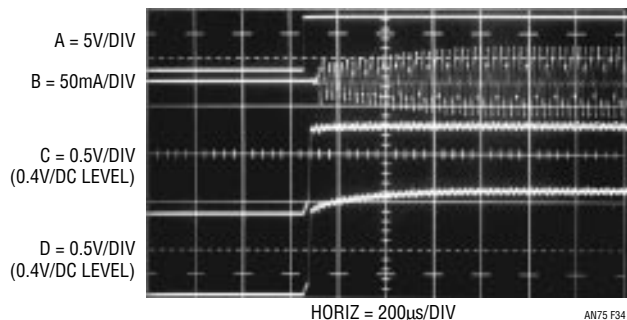


Figure 34. Fast Loop Response Maintains Regulation at 200Hz PWM Rate. Waveforms Include PWM Command (A), Lamp Current (B), LT1371 Feedback (C) and Error Amplifier V_C (D) Pins. Loop Settling Occurs in 500μs

Ultralow Noise Power Converters¹⁰

Today's circuit designer is often challenged to assemble a high performance system by combining sensitive analog electronics with potentially noisy power converters. Requirements for a small, efficient, cost effective solution are in conflict with acceptable noise performance—noisy switching regulators call for filtering, shielding and layout revisions that add bulk and expense. Most electromagnetic interference (EMI) problems associated with DC/DC converters are due to high speed switching of large currents and voltages. To maintain high efficiency, these switch transitions are designed to occur as quickly as possible. The result is input and output ripple that contains very high harmonics of the switching frequency. These fast edges also couple through stray magnetic and electric fields to nearby signal lines, making efforts to filter the supply lines ineffective.

The LT1534 ultralow noise switching regulator provides an effective and flexible solution to this problem. Using two external resistors, the user can program the slew rates of the current through the internal 2A power switch and the voltage on it. Noise performance can be evaluated and improved with the circuit operating in the final system. The system designer need sacrifice only as much efficiency as is necessary to meet the required noise performance. With the controlled slew rates, system performance is less sensitive to layout, and shielding requirements can be greatly reduced; expensive layout and mechanical revisions can be avoided.

Note 10: Figures 36 to 39 and all associated text are authored by Jeff Witt of LTC. Their original presentation is annotated in reference 22.

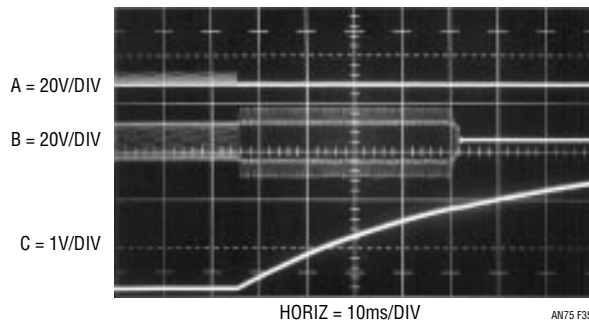


Figure 35. Safety Feature Reacts to Lamp Feedback Loss by Shutting Down Power. Lamp Current Dropout (A) Allows Monitoring Circuit to Ramp Up (C), Shutting Off Drive (B)

The LT1534's internal oscillator can be programmed over a broad frequency range (20kHz to 250kHz) with good initial accuracy. It can also be synchronized to an external signal placing the switching frequency and its harmonics away from sensitive system frequencies.

Low Noise Boost Regulator

In Figure 36, the LT1534 boosts 3.3V to supply 650mA at 5V with its oscillator synchronized to an external 50kHz clock. The circuit relies on the low ESR of capacitor C2 to keep the output ripple low at the fundamental frequency; slew rate control reduces the high frequency ripple. Figure 37 shows waveforms of the circuit as it delivers 500mA. The top trace shows the voltage on the collector of the internal bipolar power switch (the COL pins), and the middle trace shows the switch current. The lowest trace is

the output ripple. The slew rates are programmed to their fastest here, resulting in good efficiency (83%), but also generating excessive high frequency ripple. Figure 38 shows the same waveforms with the slew rates reduced. The large high frequency transients have been eliminated.

Low Noise Bipolar Supply

Many high performance analog systems require quiet bipolar supplies. This circuit (Figure 39) will generate $\pm 5V$ from a wide input range of 3V to 12V, with a total output power of 1.5W. By using a 1:1:1 transformer, the primary and secondary windings can be coupled using capacitors C2 and C3, allowing the LT1534 to control the switch transitions at the output rectifiers as well as at the switch collector. Secondary damping networks are not required.

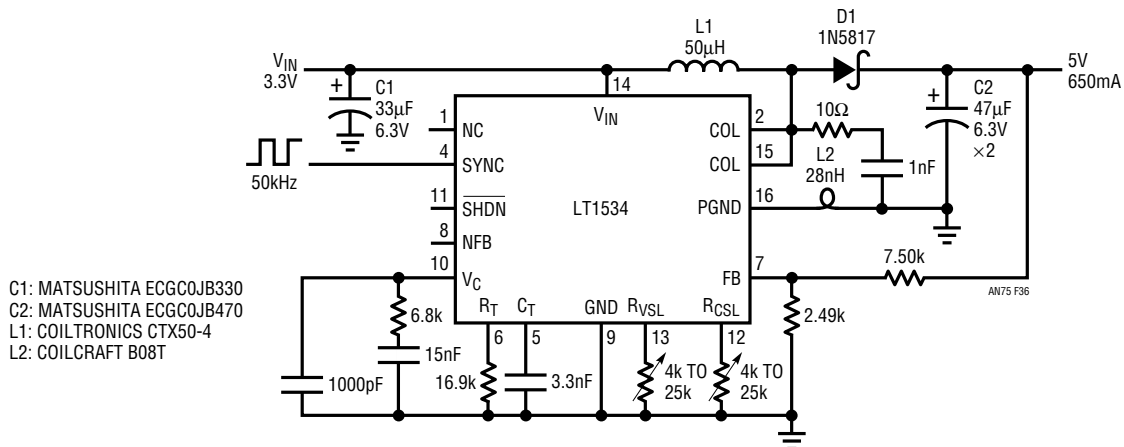


Figure 36. The LT1534 Boosts 3.3V to 5V. The Resistors On the R_{VSL} and R_{CSL} Pins Program the Slew Rates of the Voltage On the Power Switch (COL Pins) and the Current Through It

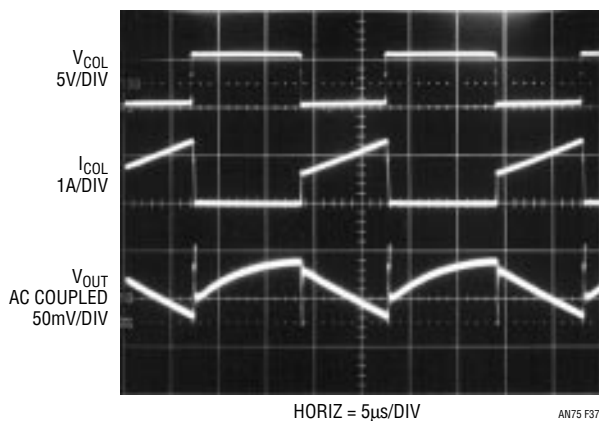


Figure 37. High Slew Rates ($R_{CSL} = R_{VSL} = 4k$) Result in Good Efficiency But Excess High Frequency Ripple

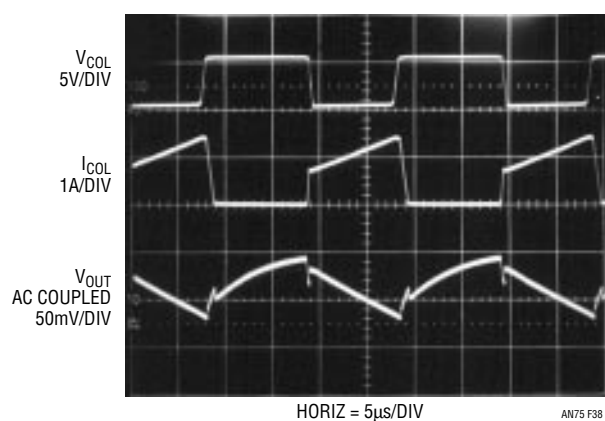


Figure 38. Low Slew Rates ($R_{CSL} = R_{VSL} = 24k$) Result in an Output Without Troublesome High Frequency Transients

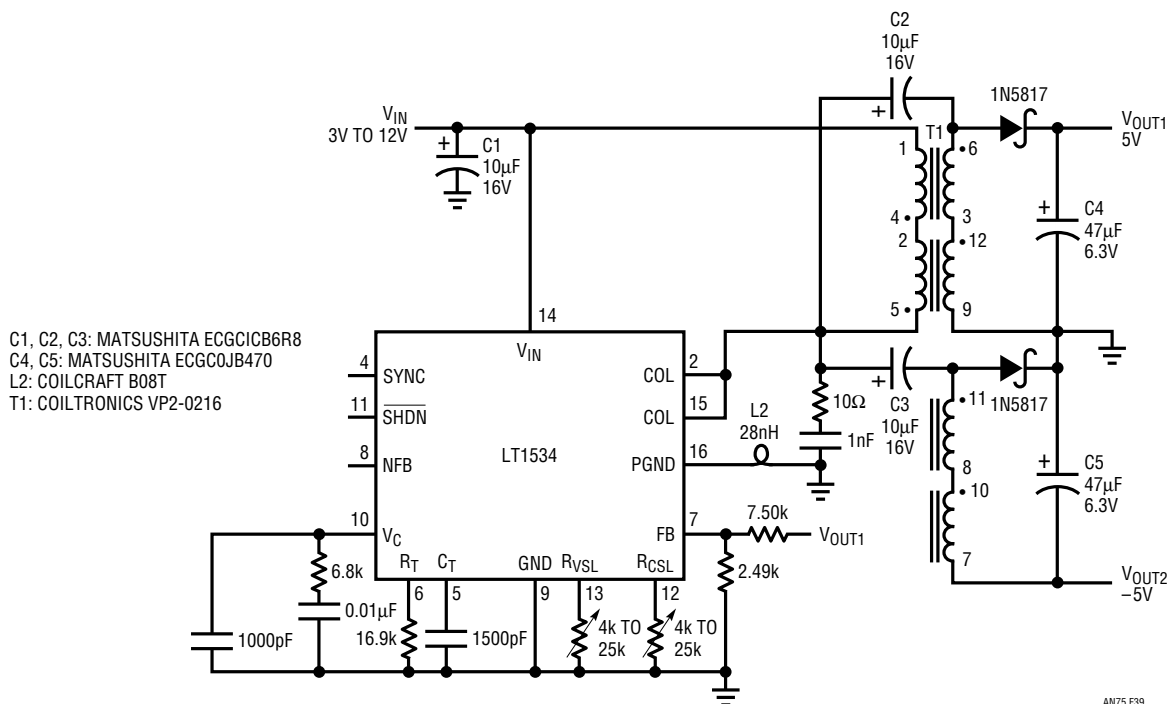


Figure 39. A Low Noise, Wide Input Range $\pm 5V$ Supply

Ultralow Noise Off-Line Power Supply

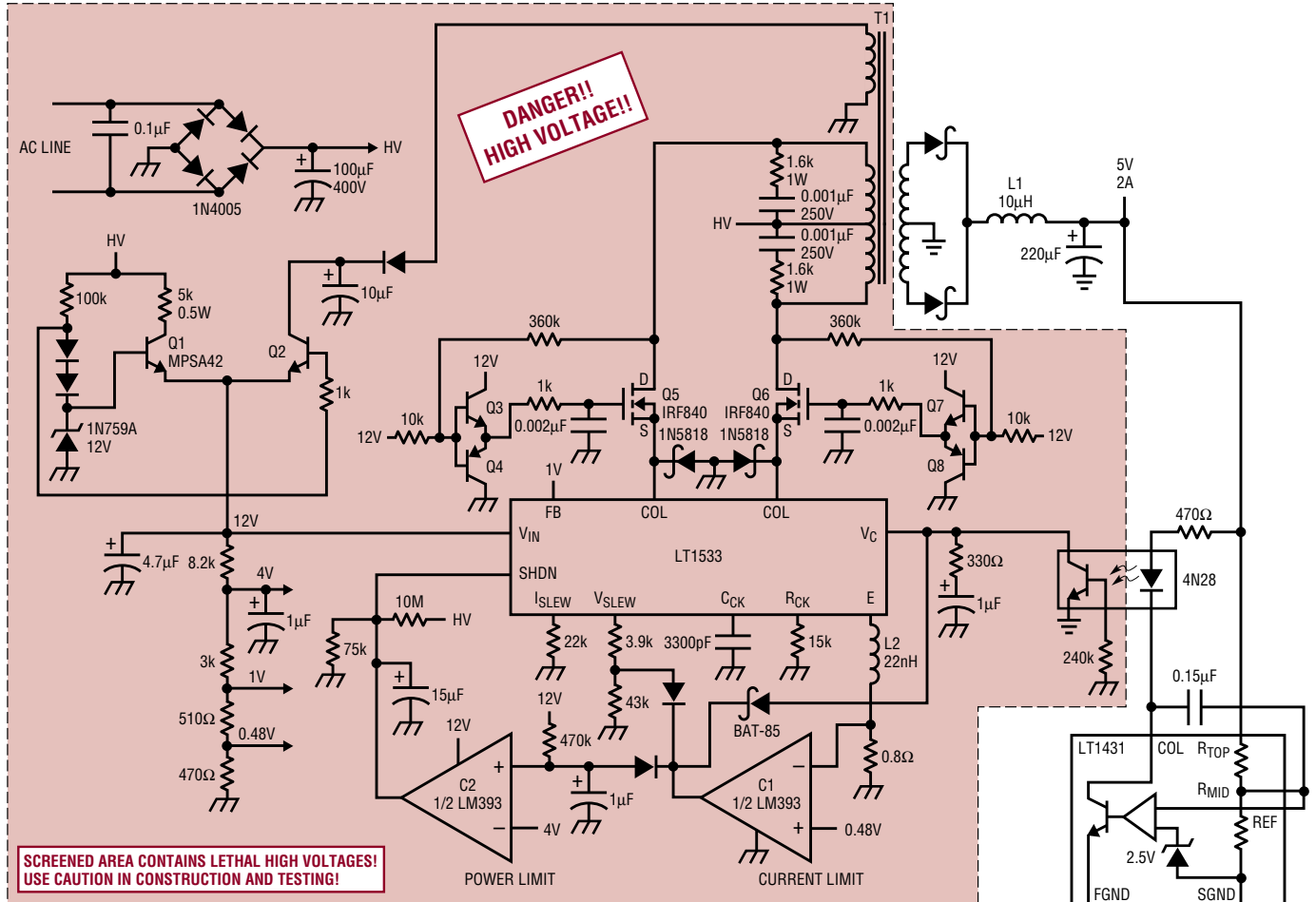
Off-line power supplies require input filtering components to meet FCC emission requirements. Additionally, board layout is usually quite critical, requiring considerable experimentation even for experienced off-line supply designers. These considerations derive from the wideband harmonic energy generated by the fast switching of traditional off-line supplies. A new device, the LT1533 low noise switching regulator, eliminates these issues by continuous, closed-loop control of voltage and current switching times.¹¹ Additionally, the device's push-pull output drive eliminates the flyback interval of conventional approaches. This further reduces harmonics and smoothes input current drain characteristics. Although intended for DC/DC conversion, the LT1533 adapts nicely to off-line service, while eliminating emission, filtering, layout and noise concerns.

Figure 40 shows the supply. Q5 and Q6 drive T1, with a rectifier-filter, the LT1431 and the optocoupler closing an isolated loop back to the LT1533. The LT1533 drives Q5 and Q6 in cascode fashion to achieve high voltage switching capability. It also continuously controls their current and voltage switching times, using the resistors at the I_{SLEW} and V_{SLEW} pins to set transition rates. FET current

information is directly available, although FET voltage status is derived via the 360k–10k dividers and routed to the gates via the NPN-PNP followers. The source wave shapes, and hence the voltage slewing information at the LT1533 collector terminals, are nearly identical in shape to the drain waveforms.

Q1, Q2 and associated components provide a bootstrapped bias supply, with start-up transistor Q1 turning off once T1 begins supplying power to Q2. The resistor string at Q2's emitter furnishes various "housekeeping" bias potentials. The LT1533's internal 1A current limit is too high for effective overcurrent protection. Instead, current is sensed via the 0.8Ω shunt at the LT1533's emitter pin (E). C1, monitoring this point, goes low when current limit is exceeded. This pulls the V_C pin low and also accelerates voltage slew rate, resulting in fast limiting while minimizing instantaneous FET stress. Prolonged short-circuit conditions result in C2 going low, putting the circuit into shutdown. Once this occurs, the C1–C2 loop oscillates in a controlled manner, sampling current for about a millisecond every second or so. This action forms a power limit, preventing FET heating and eliminating heat sink requirements.

Note 11: In depth coverage of this device, its use and performance verification appears in reference 23.



- L1: COILTRONICS UP-4
 L2: COILCRAFT B07T
 NPN: 2N3904 UNLESS OTHERWISE NOTED
 PNP: 2N3906
 T1: COILTRONICS CTX02-13978-X3
- : 20CJQ045(I.R.) UNLESS OTHERWISE NOTED
 : 1N4148
 : AC(HOT) RETURN
 : OUTPUT COMMON

Figure 40. 10W Off-Line Power Supply Passes FCC Emission Requirements Without Filter Components

Application Note 75

Figure 41 shows waveforms for the power supply. Trace A is one FET source; traces B and C are its gate and drain waveforms, respectively. FET current is trace D. The cascoded drive maintains waveshape fidelity, even as the LT1533 tightly regulates voltage and current transition rates. The wideband harmonic activity typical of off-line supply waveforms is entirely absent. Power delivery to T1 (center screen, trace C) is particularly noteworthy. The

waveshapes are smoothly controlled, and no high frequency content is observable. Figure 42 increases sweep speed by a factor of 5, but high frequency components are still undetectable. Figure 43 shows supply input monitored with a wideband current probe at the “HV” node. The current drain profile is smooth, with complete absence of high frequency content.

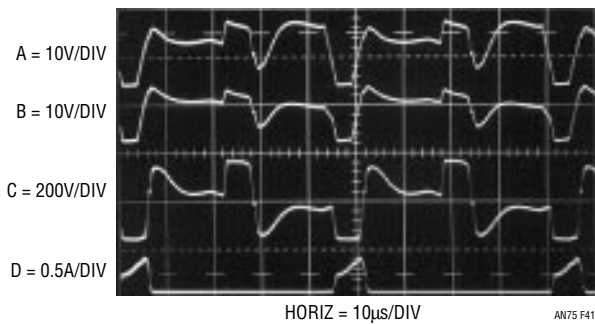


Figure 41. Waveforms for One of the Power Supplies' FETs Show No Wideband Harmonic Activity. LT1533 Provides Continuous Control of Voltage and Current Slewing. Result Is Smoothly Controlled Waveshapes for FET Source (A), Gate (B) and Drain (C). FET Current is Trace D

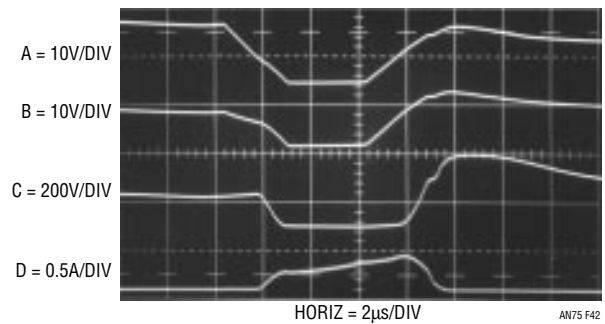


Figure 42. Time Expanded Version of Figure 41, with Same Trace Assignments. No Wideband Components Are Detectable

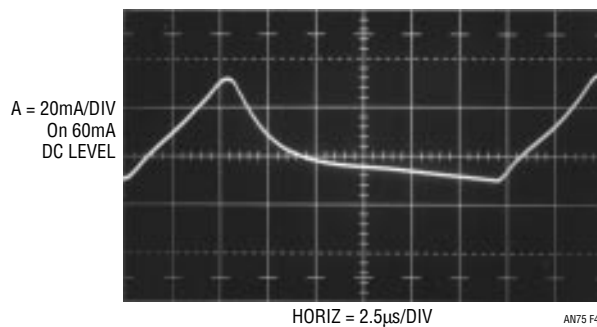


Figure 43. Circuit's Input Current Drain Profile Is Smooth, with No High Frequency Content

Figure 44, a 30MHz wide spectral plot, shows circuit emissions well below FCC requirements. This data was taken with no input filtering LC components and a nominally nonoptimal layout.

Output noise is composed of fundamental ripple residue, with essentially no wideband components. Typically, the low frequency ripple is below 50mV. If additional ripple

attenuation is desired a 100 μ H–100 μ F LC section permits <100 μ V output noise. Figure 45 shows this in a 100MHz bandpass. Ripple and noise are so low that the oscilloscope requires a 40dB low noise preamplifier to even register a display (see Note 11).

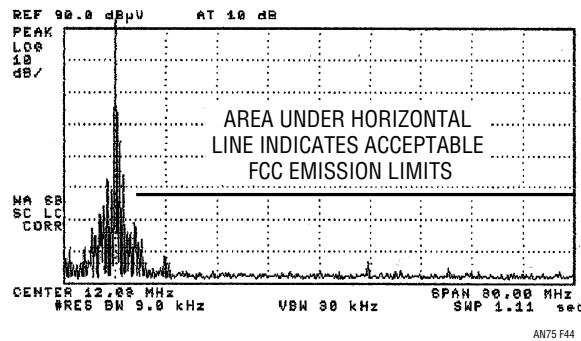


Figure 44. 30MHz Wide Spectral Plot Shows Circuit Emissions Well Below FCC Requirements Despite Lack of Conventional Filter Components

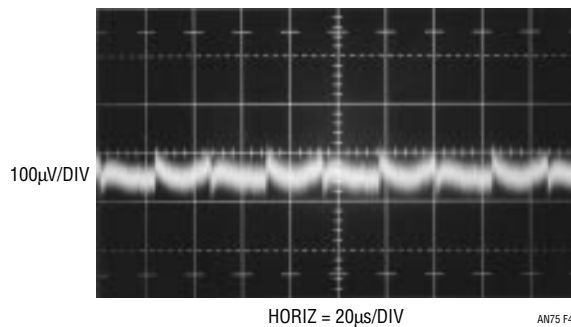


Figure 45. Power Supply Output Noise Below 100 μ V (100MHz Measurement Bandwidth) Is Obtainable Using Additional Output LC Section. Without LC Section Wideband Harmonic Is Still Absent, Although Fundamental Ripple Is 50mV

Application Note 75

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Note 12: Veterans of LTC Application Notes, a weary brigade, may recognize this reference as the object of Application Note 70's (Footnote 14) champagne prize offer. The mystery solved, the messenger was compensated as specified (Veuve Clicquot Ponsardin).

APPENDIX A

SOME GUIDELINES FOR MICROPOWER DESIGN AND AN EXAMPLE

As with all engineering, micropower circuitry requires attention to detail, awareness of trade-offs and an opportunistic bent towards achieving the design goal.

The most obvious way to save power is to choose components which require little energy. Additional savings require more effort.

Circuits should be examined in terms of current flow. Consider such flow in all DC and AC paths. For example, do DC base currents go where they can do some useful work, or are they thrown away? Try to keep AC signal swings down, particularly if capacitors (parasitic or intended) must be continually charged and discharged. Examine the circuit for areas where power strobing may be allowable.

Consider quiescent vs dynamic power requirements of components to avoid unpleasant surprises. Data sheets usually specify quiescent power because the manufacturer doesn't know what the user's circuit conditions are. For example, everyone "knows" that "MOS devices draw no current." Unfortunately, Mother Nature dictates that as frequency and signal swings go up, the capacitances associated with MOS devices begin to require more power. It is often a mistake to automatically associate low power operation with a process technology. While it's likely that CMOS will provide lower power operation for a given function than 12AX7s, a bipolar approach may be even better. Consider individual situations on the basis of their specific requirements before committing to a technology. Very often, circuits require several technologies (i.e., CMOS, bipolar and discrete) for best results.

Usually, achieving low power operation requires performance trade-offs. Minimizing signal swings and current saves power, but moves circuit operation closer to the noise floor. Offsets, drift, bias currents and noise become increasingly significant error factors as signal amplitudes are constricted to save power. This is a fundamental trade-off and must be carefully considered. Circuits employing power strobing can sometimes get around this problem by utilizing low duty cycles.

Text Figures 1 and 4, voltage-to-frequency converters, furnish an example of the evolution of a low power design. Design goals included a 10kHz maximum output, low drift, fast step response, linearity inside 0.05% and minimum supply current. Other specifications appear in the text.

Figure A1 shows an early (1986) version of this circuit. Operation is similar to the text described for Figure 1, but a brief description follows. When the input current-derived ramp at C1's negative input crosses zero, C1's output drops low, pulling charge through C1. This forces the negative input below zero. C2 provides positive feedback, allowing a complete discharge for C1. When C2 decays, C1A's output goes high, clamping at the level set by D1, D2 and V_{REF} . C1 receives charge and recycling occurs when C1A's negative input again arrives at zero. The frequency of this action is related to the input voltage. Diodes D3 and D4 provide steering, and are temperature compensated by D1 and D2. C1A's sink saturation voltage is uncompensated, but small. C1B is a start-up loop.

Although the LT1017 and LT1034 have low operating currents, this circuit pulls almost 400 μ A. The AC current paths include C1's charge-discharge cycle, and C2's branch. The DC path through D2 and V_{REF} is particularly costly. C1's charging must occur quickly enough for 10kHz operation, meaning the clamp seen by C1A's output must have low impedance at this frequency. C3 helps, but significant current still must come from somewhere to keep impedance low. C1A's current limited output cannot do the job unaided, and the resistor from the supply is required. Even if C1A could supply the necessary current, V_{REF} 's settling time would be an issue. Dropping C1's value will reduce impedance requirements proportionally, and would seem to solve the problem. Unfortunately, such reduction magnifies the effects of stray capacitance at the D3–D4 junction. It also mandates increasing R_{IN} 's value to keep scale factor constant. This lowers operating currents at C1A's negative input, making bias current and offset more significant error sources.

Figure A2 shows an initial attempt at dealing with these issues. This scheme is similar to Figure A1, except that Q1 and Q2 appear. V_{REF} receives switched bias via Q1, instead of being on all the time. Q2 provides the sink path for C1. These transistors invert C1A's output, so its input pin assignments are exchanged. R1 provides a light current from the supply, improving reference settling time. This

Application Note 75

arrangement decreases supply current to about 300 μ A, a significant improvement. Several problems do exist, however. Q1's switched operation is really effective only at higher frequencies. In the lower ranges, C1A's output is low most of the time, biasing Q1 on and wasting power. Additionally, when C1A's output switches, Q1 and Q2 simultaneously conduct during the transition, effectively shunting R2 across the supply. Finally, the base currents of both transistors flow to ground and are lost. The basic temperature compensation is as before, except that Q2's saturation term replaces the comparator's.

Figure A3 is better. Q1 is gone, Q2 remains but Q3, Q4 and Q5 have been added. V_{REF} and its associated diodes are biased from R1. Q3, an emitter-follower, is used to source current to C1. Q4 temperature compensates Q3's V_{BE} , and Q5 switches Q3.

This method has some distinct advantages. The V_{REF} string can operate at greatly reduced current because of Q3's current gain. Also, Figure A2's simultaneous conduction problem is largely alleviated because Q5 and Q2 are switched at the same voltage threshold out of C1A. Q3's base and emitter currents are delivered to C1. Q5's currents are wasted, although they are much smaller than Q3's. Q2's small base current is also lost. The values for C2 and R3 have been changed. The time constant is the same, but some current reduction occurs due to R3's increase.

If C1 cannot be reduced, then its AC currents cannot be avoided. This leaves only the aforementioned Q5 and Q2 currents as significant wasted terms, along with R3's now smaller loss. Current drain for this circuit is about 200 μ A maximum.

Figure A4 (1987) is very similar, but eliminates Q5 and Q2's losses to get maximum operating current below 150 μ A with quiescent current under 80 μ A. The basic improvement is the use of CMOS inverters for reference switching—the inverters supply pin is driven by the reference buffer NPN and their paralleled outputs switch between V_{REF} and ground. Other enhancements provide better temperature compensation and improved power supply rejection. The modified LM334 driven reference stack begins to look very similar to Figure 1's arrangement. This circuit provided excellent precision—0.02% linearity, 40ppm/ $^{\circ}$ C drift and 40ppm/V PSRR.

A variant (1991) of this circuit, Figure A5, reduced supply current to only 90 μ A maximum, by minimizing the number of CMOS inverters, eliminating their AC input currents. The charge dispensing capacitor was also reduced to 100pF, necessitating a larger input resistance value. The price for the current saving was degradation of drift and linearity by factors of 2 and 3, respectively.

Text Figures 1 and 4 (1997 and 1999, respectively) are direct extensions of the last two circuits. Their markedly decreased operating currents are obtained with minimal performance compromises by utilizing contemporary components. The LTC1440/LTC1441 comparators and the LT1389 reference are the heroes. Some other refinements are involved, but the text's voltage-to-frequency circuits are the final (for now) iteration of the five versions shown here.

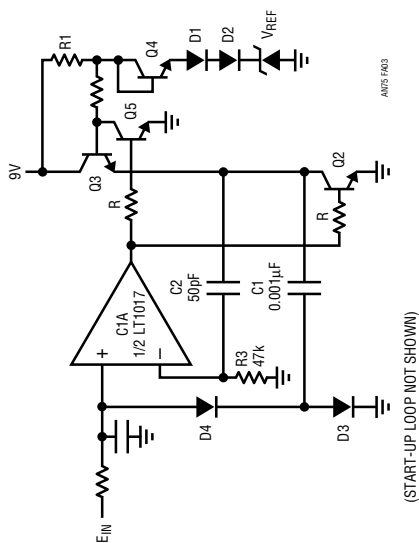


Figure A1

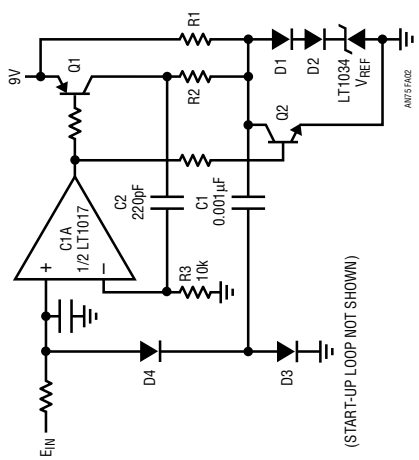


Figure A2

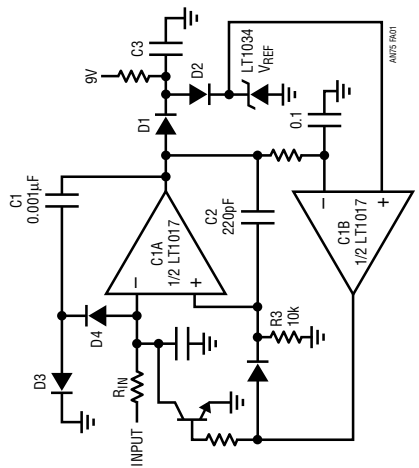


Figure A3

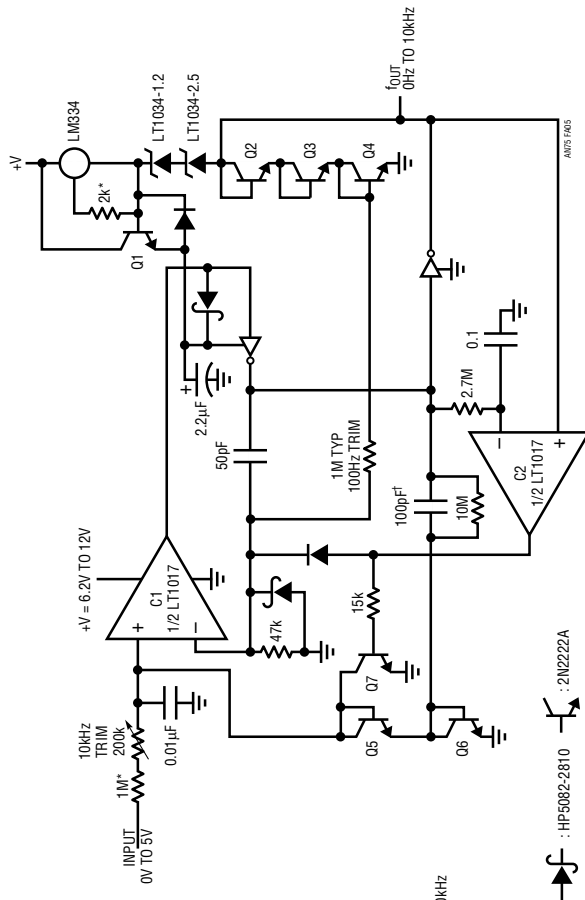


Figure A4

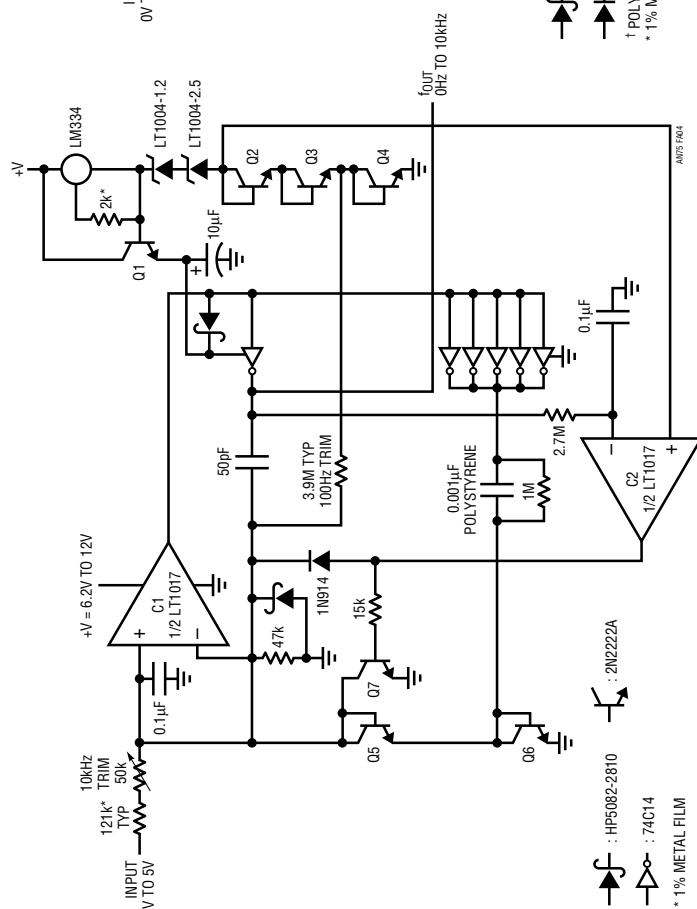


Figure A5

- HP5082-2810
- 1N4148
- POLYSTYRENE
- * 1% METAL FILM
- 2N2222A
- 74C14

APPENDIX B

PARASITIC EFFECTS OF TEST EQUIPMENT ON MICROPOWER CIRCUITS

The energy absorbed by test equipment connections to micropower circuits can be significant. Under normal circumstances test equipment and probes have negligible power drain, but microampere level operating currents mandate care. Test instrumentation should be regarded as an integral part of the circuit. DC and AC loading and parasitic effects must be kept in mind to avoid unpleasant surprises. Such instrument connection errors can make the circuit under test look unfairly bad or good.

The DC resistance of oscilloscope probes varies from hundreds of ohms (1X types) to $10\text{M}\Omega$ (10X), with some 10X types as low as $1\text{M}\Omega$. Contrary to some expectations, FET probes do not have high input resistance—some types are as low as $100\text{k}\Omega$, although most are about $10\text{M}\Omega$. The DC loading of a 10X 1M probe could introduce as much as $5\mu\text{A}$ of loss, almost 60% of Figure 4's total! The AC loading of a 10pF probe looking at Figure 27's 30kHz clock will cause apparent circuit consumption of $1\mu\text{A}$, a significant loss in a low power circuit. 1X type probes present about 50pF of loading, with $1\text{M}\Omega$ DC resistance when connected to the 'scope. This kind of probe loading can cause large errors in micropower circuits, while virtually disabling some. Such a probe, introduced at C1B's negative input in text Figure 6, would stop the circuit's oscillator. If placed across the supply of Figure 6 it would consume almost as much current as the circuit.

Probe AC and DC loading are not the only effects. Some DVMs produce "charge spitting" at their inputs. Such parasitic charge, introduced into high impedance nodes, can cause substantial errors. It's also worth remembering that DVM DC loading may change with range. Lower ranges may have very high input impedance, but higher ranges are typically $10\text{M}\Omega$. A $10\text{M}\Omega$ DVM reading Figure 6's supply introduces almost 10% supply current error.

Figure B1 shows a way test equipment can make the circuit look too good, instead of too bad. If the pulse generator is adjusted more than a diode drop above the regulator's output, the bypass capacitor peak detects the charge delivered through the IC's internal diode. The regulator can't sink current, and with its output forced high it won't source anything. Under these conditions the circuit functions while the current meter reads zero...a very low power circuit indeed¹!

Figure B2 shows a very simple, but useful circuit which greatly aids probe loading problems in micropower circuits. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows DVM cable and probe driving and also biases the circuit's input shield. This bootstraps the input capacitance, reducing its effect. DC and AC errors of this circuit are low enough for almost all work, with enough bandwidth for just about any low power circuit. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.

Figure B3 is a very fast high impedance probe for those occasions which require it. A1, a hybrid FET buffer, forms the electrical core of the probe. This device is a low input capacitance, wideband FET source follower driving a fast bipolar output stage. The input of the probe goes to this device via a 51Ω resistor, reducing the possibility of oscillations in the follower input stage when the probe sees low AC impedance. A1's output drives a guard shield around the probe's input line, reducing effective input capacitance to about 4pF. A ground referred shield encircles the guard shield, reducing pickup and making high quality ground connections to the circuit under test easy. Back-terminated A1 drives the output BNC cable, feeding a 50Ω termination at the oscilloscope. Specifications are noted in the figure. Note that the back termination mandates an attenuation of 2, while the buffer's open-loop architecture introduces a small gain error. The probe's physical construction is critical to achieving stated performance. See reference 25 for details.

Note 1: Practically speaking, most regulators and power supplies can sink small amounts of current. Because of this, the current meter may actually read negative.

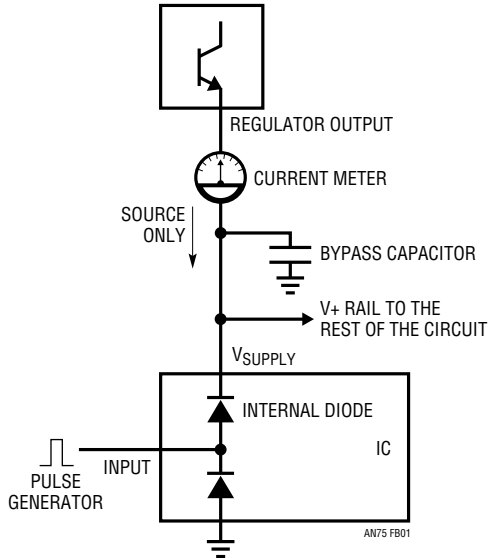
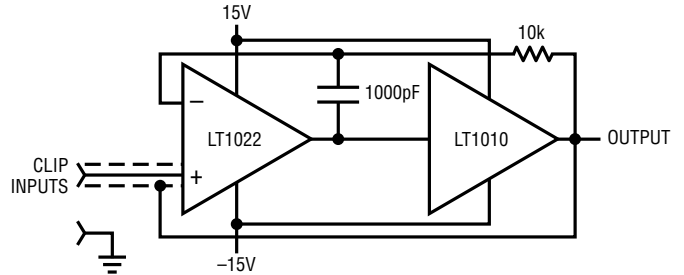


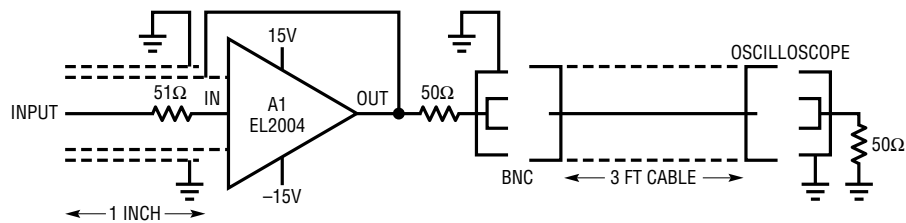
Figure B1. Parasitic Currents Flowing Into Circuit From Pulse Generator Produce Misleading Current Meter Indications



A = 1
 INPUT CAPACITANCE \approx 8pF
 $I_B = 50\text{pA}$
 GBW = 8.5MHz
 SLEW = 23V/ μ s
 $E_{OS} = 250\mu\text{V}$
 $E_{OS}\Delta\text{TC} = 5\mu\text{V}/^\circ\text{C}$

AN75 FB02

Figure B2. High Impedance Probe Introduces Minimal Loading. Speed Is Adequate for Most Micropower Circuits

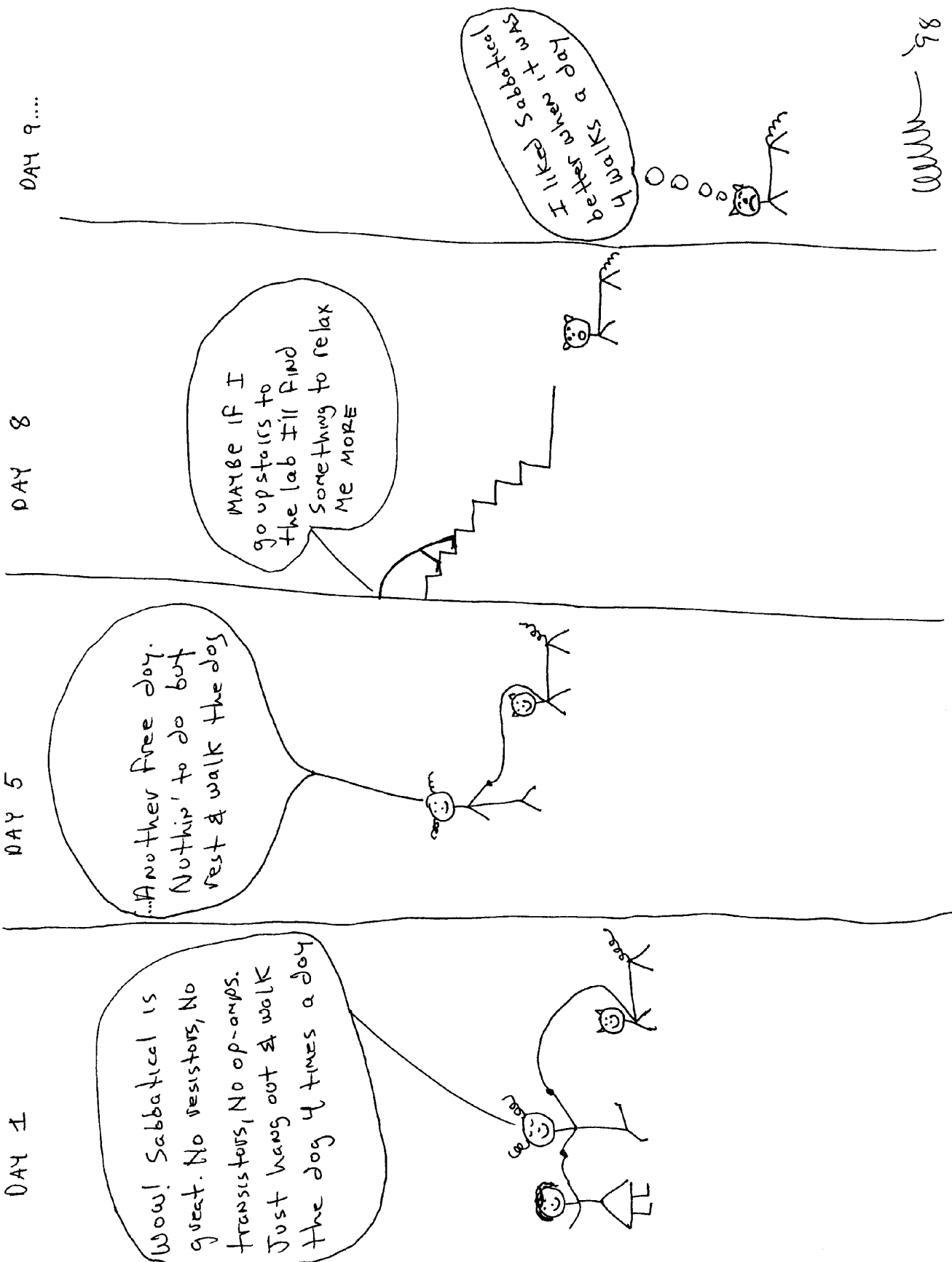


ATTN = NOMINAL 2, TYPICAL 2.1 (SEE TEXT)
 INPUT CAPACITANCE = 4pF
 $I_B = 400\text{pA}$
 GBW = 50MHz
 SLEW = 1000V/ μ s
 $E_{OS} = 10\text{mV}$
 $E_{OS}\Delta\text{TC} = 50\mu\text{V}/^\circ\text{C}$

AN75 FB03

Figure B3. Ultrafast Buffer Probe Maintains Minimal Loading with 50MHz Bandwidth

Application Note 75



www.linear.com 98

30 Nanosecond Settling Time Measurement for a Precision Wideband Amplifier

Quantifying Prompt Certainty

Jim Williams

Introduction

Instrumentation, waveform generation, data acquisition, feedback control systems and other application areas utilize wideband amplifiers. New components (see page 2 “A Precision Wideband Dual Amplifier with 30ns Settling Time”) have introduced precision while maintaining high speed operation. The amplifier’s DC and AC specifications approach or equal previous devices at significantly lower cost while saving power.

Settling Time Defined

Amplifier DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, amplifier settling time is extraordinarily difficult to determine. Settling time is the elapsed time from input application until the output arrives at and remains within a specified error band around the final value. It is usually specified for a full-scale transition. Figure 1 shows that settling time has three distinct components. The *delay time* is small and is almost entirely due to amplifier propagation delay. During this interval there is no output movement. During *slew time* the amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency com-

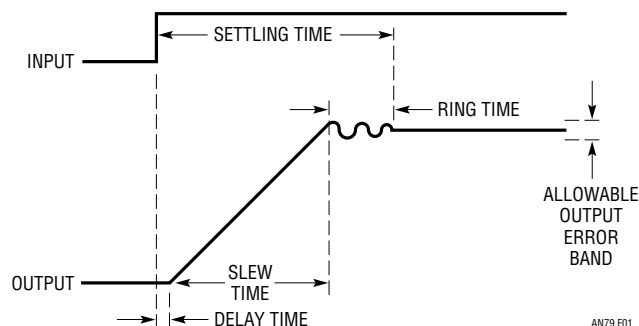


Figure 1. Settling Time Components Include Delay, Slew and Ring Times. Fast Amplifiers Reduce Slew Time, Although Longer Ring Time Usually Results. Delay Time is Normally a Small Term

pensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs which degrade DC error terms.¹

Measuring anything at any speed requires care. Dynamic measurement is particularly challenging. Reliable nanosecond region settling time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique.²

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Note 1: This issue is treated in detail in latter portions of the text. Also see Appendix D “Practical Considerations for Amplifier Compensation.”

Note 2: The approach used for settling time measurement and its description borrows heavily from a previous publication. See Reference 1.

A PRECISION WIDEBAND DUAL AMPLIFIER WITH 30ns SETTLING TIME

Until recently, wideband amplifiers provided speed, but sacrificed precision, power consumption and, often, settling time. The LT[®]1813 dual op amp does not require this compromise. It features low offset voltage and bias current and high DC gain while operating at low supply current. Settling time is 30ns to 0.1% for a 5V step. The output will drive a 100Ω load to ±3.5V with ±5V supplies, and up to 100pF capacitive loading is permissible. The table below provides short form specifications.

LT1813 Short Form Specifications

CHARACTERISTIC	SPECIFICATION
Offset Voltage	0.5mV
Offset Voltage vs Temperature	10μV/°C
Bias Current	1.5μA
DC Gain	3000
Noise Voltage	8nV/√Hz
Output Current	60mA
Slew Rate	750V/μs
Gain-Bandwidth	100MHz
Delay	2.5ns
Settling Time	30ns/0.1%
Supply Current	3mA per Amplifier

Considerations for Measuring Nanosecond Region Settling Time

Historically, settling time has been measured with circuits similar to that in Figure 2. The circuit uses the “false sum node” technique. The resistors and amplifier form a bridge type network. Assuming ideal resistors, the amplifier output will step to $-V_{IN}$ when the input is driven. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider’s attenuation means the probe’s output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. Several flaws exist. The circuit requires the input pulse to have a flat top within the required measurement limits. Typically, settling within 5mV or less for a 5V step is of interest. No general purpose pulse generator is meant to hold output amplitude and noise within these limits. Generator output-caused aberrations appearing at the oscilloscope probe will be indistinguishable from amplifier output movement, producing unreliable results. The oscilloscope connection also presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. A 10pF probe alleviates this problem but its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An

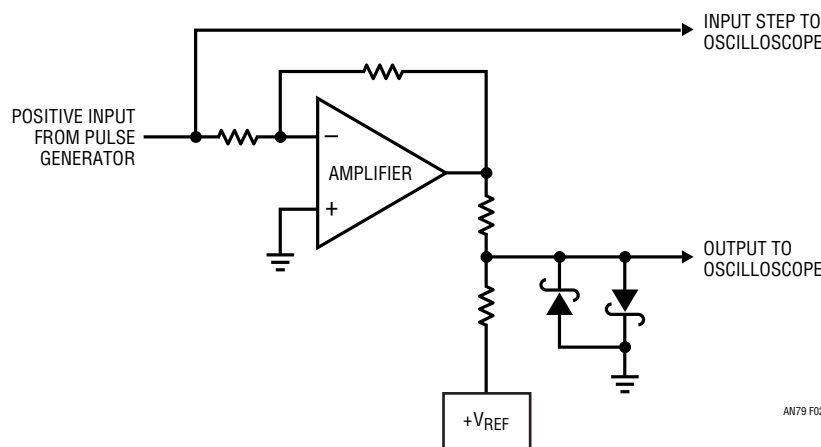


Figure 2. Popular Summing Scheme for Settling Time Measurement Provides Misleading Results. Pulse Generator Posttransition Aberrations Appear at Output. 10× Oscilloscope Overdrive Occurs. Displayed Information Is Meaningless

active $1\times$ FET probe will work, but another issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope will undergo an unacceptable overload, bringing displayed results into question.³

At 0.1% resolution (5mV at the output—2.5mV at the oscilloscope), the oscilloscope typically undergoes a $10\times$ overdrive at 10mV/DIV, and the desired 2.5mV baseline is unattainable. At nanosecond speeds, the measurement becomes hopeless with this arrangement. There is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring amplifier settling time requires an oscilloscope that is somehow immune to overdrive and a “flat-top” pulse generator. These become the central issues in wideband amplifier settling time measurement.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling ‘scope.⁴ Unfortunately, these instruments are no longer manufactured (although still available on the secondary market). It is possible, however, to construct a circuit that borrows the overload advantages of classical sampling ‘scope technology. Additionally, the circuit can be endowed with

features particularly suited for measuring nanosecond range settling time.

The “flat-top” pulse generator requirement can be avoided by switching current, rather than voltage. It is much easier to gate a quickly settling current into the amplifier's summing node than to control a voltage. This makes the input pulse generator's job easier, although it still must have a rise time of 1 nanosecond or less to avoid measurement errors.⁵

Practical Nanosecond Settling Time Measurement

Figure 3 is a conceptual diagram of a settling time measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the oscilloscope is connected to the settle point by a

Note 3: For a discussion of oscilloscope overdrive considerations, see Appendix A, “Evaluating Oscilloscope Overdrive Performance.”

Note 4: Classical sampling oscilloscopes should not be confused with modern era digital sampling ‘scopes that have overdrive restrictions. See Appendix A, “Evaluating Oscilloscope Overload Performance” for comparisons of various type ‘scopes with respect to overdrive. For detailed discussion of classical sampling ‘scope operation see References 16 through 19 and 22 through 24. Reference 17 is noteworthy; it is the most clearly written, concise explanation of classical sampling instruments the author is aware of—a 12-page jewel.

Note 5: Subnanosecond rise time pulse generators are considered in Appendix B, “Subnanosecond Rise Time Pulse Generators for the Rich and Poor.”

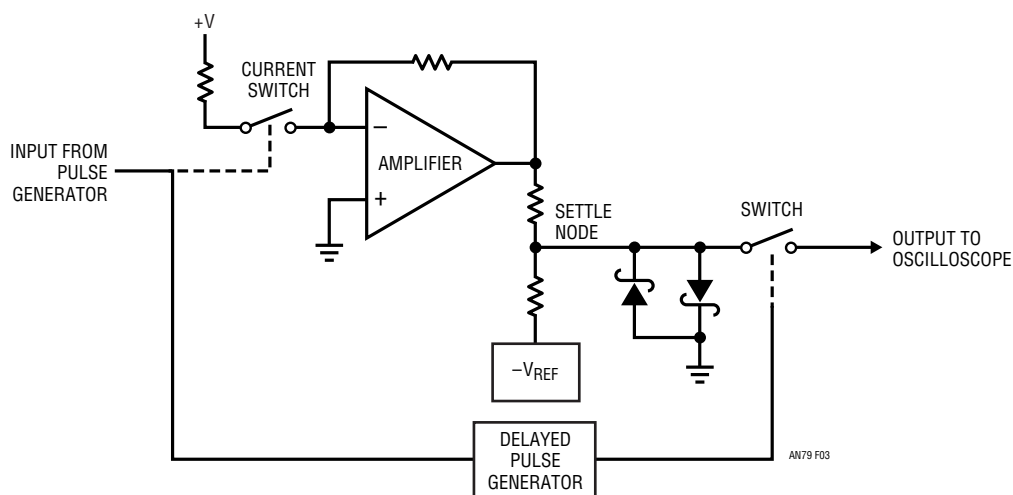


Figure 3. Conceptual Arrangement is Insensitive to Pulse Generator Aberrations and Eliminates Oscilloscope Overdrive. Switch at Input Gates Current Step to Amplifier. Second Switch is Controlled by Delayed Pulse Generator, Preventing Oscilloscope from Monitoring Settle Node Until Settling is Nearly Complete

Application Note 79

switch. The switch state is determined by a delayed pulse generator, which is triggered from the input pulse. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

A switch at the amplifier's summing junction is controlled by the input pulse. This switch gates current to the amplifier via a voltage-driven resistor. This eliminates the "flat-top" pulse generator requirement, although the switch must be fast and devoid of drive artifacts.

Figure 4 is a more complete representation of the settling time scheme. Figure 3's blocks appear in greater detail and some new refinements show up. The amplifier summing area is unchanged. Figure 3's delayed pulse generator has been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that compensates for the propagation delay of the settling time measure-

ment path. The most striking new aspect of the diagram are the diode bridge switches. Borrowed from classical sampling oscilloscope circuitry, they are the key to the measurement. The diode bridge's inherent balance eliminates charge injection based errors. It is far superior to other electronic switches in this characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt switching, defeating the switches purpose.

The diode bridge's balance, combined with matched, low capacitance monolithic diodes and high speed switching, yields clean switching. The input-driven bridge switches current into the amplifier's summing point very quickly, with settling inside a few nanoseconds. The diode clamp to ground prevents excessive bridge drive swings and ensures that input pulse characteristics are irrelevant.

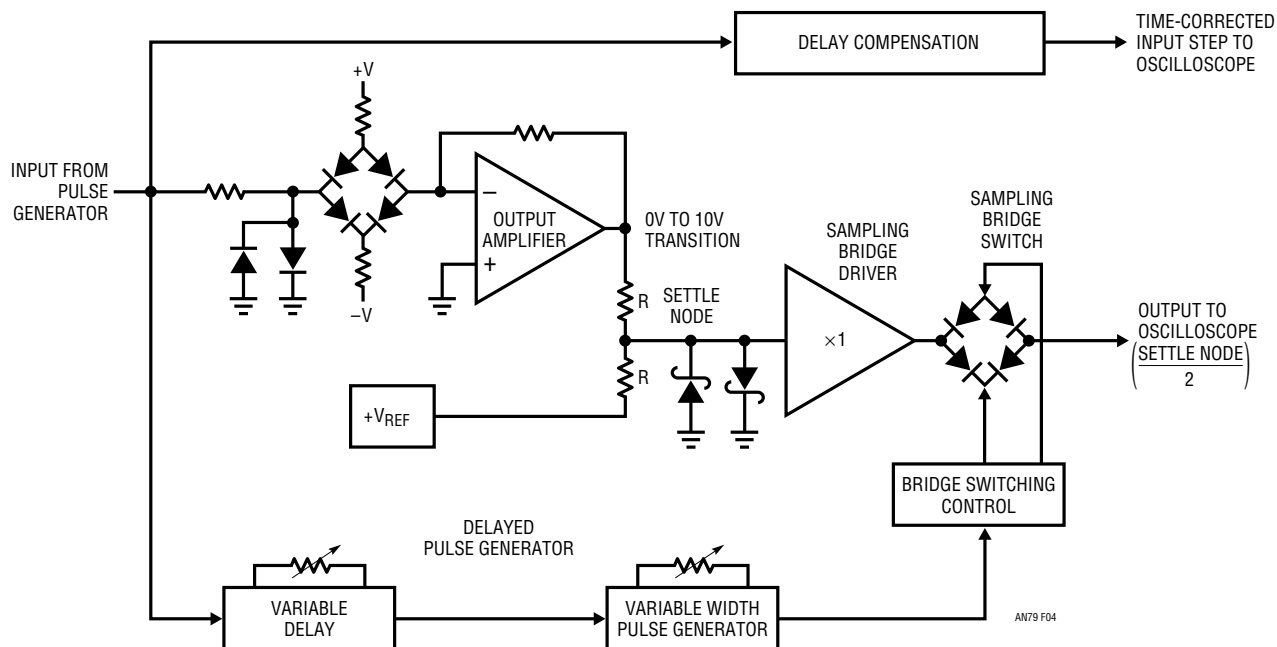


Figure 4. Block Diagram of Settling Time Measurement Scheme. Diode Bridge Switches Input Current to Amplifier. Second Diode Bridge Switch Minimizes Switching Feedthrough, Preventing Oscilloscope Overdrive. Input Step Time Reference is Compensated for Test Circuit Delays

Figure 5 details considerations for the output diode bridge switch. This bridge requires considerable attention to achieve desired performance. The monolithic bridge diodes tend to cancel each other's temperature coefficient—drift is only about $100\mu\text{V}/^\circ\text{C}$ —but a DC balance is required to minimize offset.

DC balance is achieved by trimming the bridge on-current for zero input-output offset voltage. Two AC trims are required. The “AC balance” corrects for diode and layout capacitive imbalances and the “skew compensation” corrects for any timing asymmetry in the nominally complementary bridge drive. These AC trims compensate small dynamic imbalances, minimizing parasitic bridge outputs.

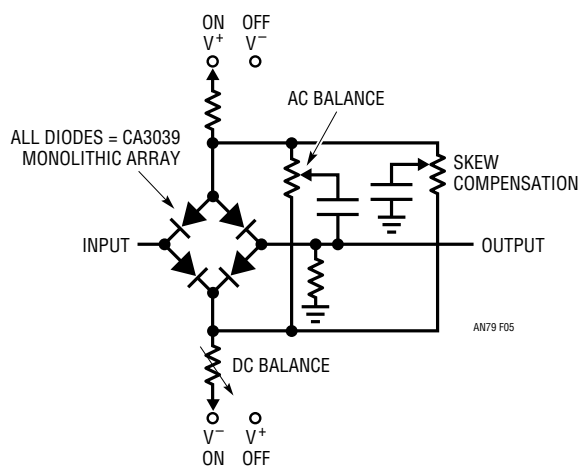


Figure 5. Diode Sampling Bridge Switch Trims Include AC and DC Balance and Switch Drive Timing Skew

Detailed Settling Time Circuitry

Figure 6 is a detailed schematic of the settling time measurement circuitry. The input pulse switches the input bridge and is also routed to the oscilloscope via a delay-compensation network. The delay network, composed of a fast comparator and an adjustable RC network, compensates the oscilloscope's input step signal for the 6ns delay through the circuit's measurement path.⁶ The amplifier's output is compared against the 5V reference via the summing resistors. The 5V reference also furnishes the bridge input current, making the measurement ratiometric. The -5V reference supply pulls a current from the summing point, allowing the amplifier a 5V step from 2.5V to -2.5V . The clamped settle node is unloaded by A1, which drives the sampling bridge.

The input pulse triggers the C2-C3 based delayed pulse generator. This circuitry is arranged to produce a delayed (controllable by the 10k potentiometer) pulse whose width (controllable by the 2k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way the oscilloscope's output is reliable and meaningful data may be taken. The delayed generator's output is level shifted by the Q1-Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1-Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.⁷

Figure 7 shows circuit waveforms. Trace A is the time-corrected input pulse, trace B the amplifier output, trace C the sample gate and trace D the settling time output. When the sample gate goes low, the bridge switches cleanly, and the last 10mV of slew are easily observed. Ring time is also clearly visible, and the amplifier settles nicely to final value. When the sample gate goes high, the bridge switches off, with only millivolts of feedthrough. Note that there is no off-screen activity at any time—the oscilloscope is never subjected to overdrive.

Figure 8 expands vertical and horizontal scales so that settling detail is more visible.⁸ Trace A is the time-corrected input pulse and trace B the settling output. The last 15mV of slew (beginning at the center-screen vertical marker) are easily observed, and the amplifier settles inside 5mV (0.1%) in 30 nanoseconds.

The circuit requires trimming to achieve this level of performance. DC and AC trims are required. Making these adjustments requires disabling the amplifier (disconnect the input current switch and the 1k resistor at the amplifier), and shorting the settle node directly to the ground plane. Figure 9 shows typical results before trimming.

Note 6: See Appendix C, “Measuring and Compensating Settling Circuit Delay.”

Note 7: The bridge switching scheme was developed at LTC by George Feliz.

Note 8: In this and all following photos, settling time is measured from the onset of the time-corrected input pulse. Additionally, settling signal amplitude is calibrated with respect to the amplifier, not the sampling bridge output. This eliminates ambiguity introduced by the summing resistor's $\div 2$ ratio.

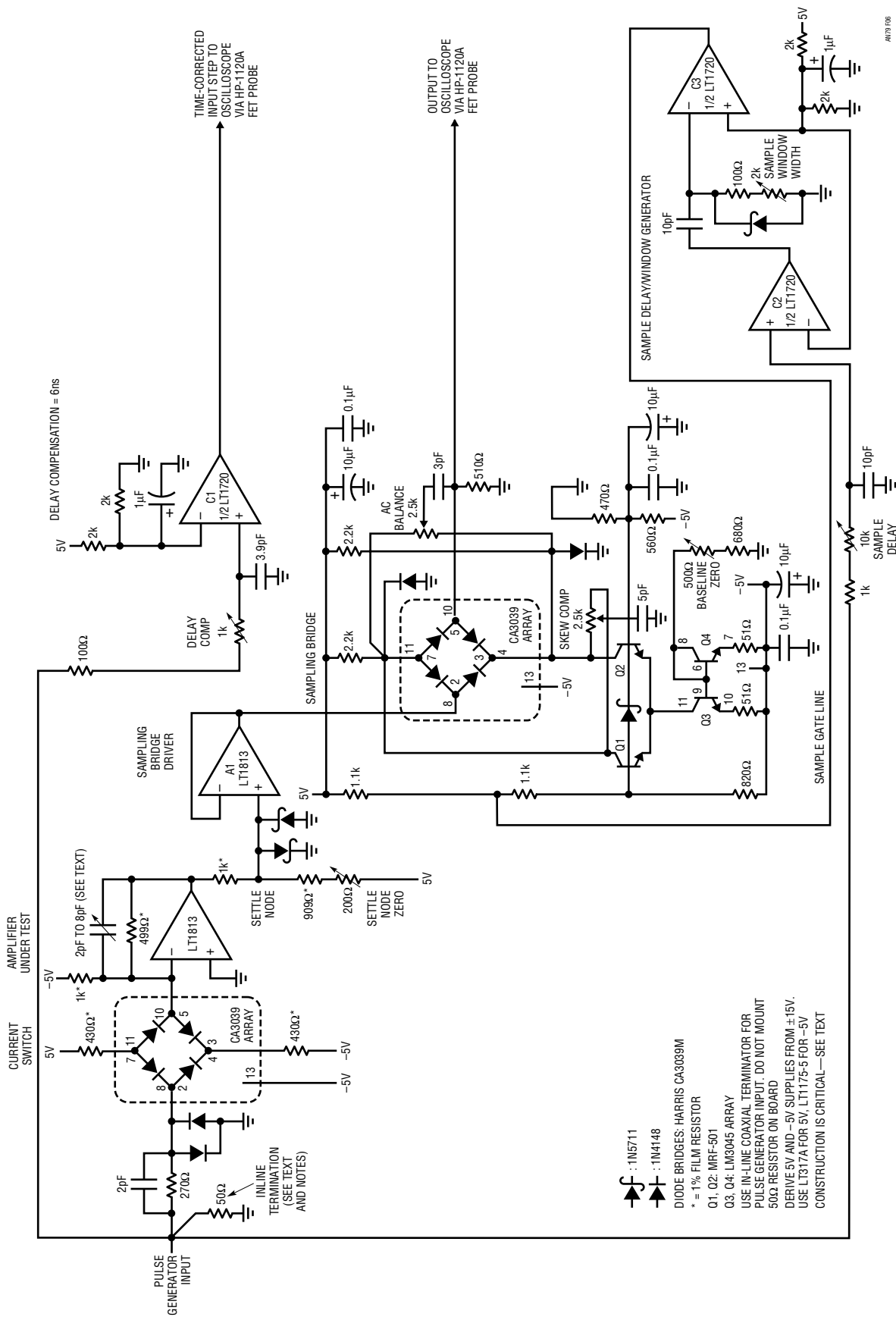


Figure 6. Detailed Schematic of Settling Time Measurement Circuit Closely Follows Block Diagram. Optimum Performance Requires Attention to Layout

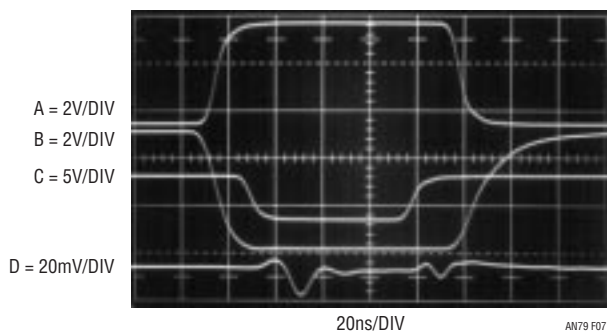


Figure 7. Settling Time Circuit Waveforms Include Time-Corrected Input Pulse (Trace A), Amplifier-Under-Test Output (Trace B), Sample Gate (Trace C) and Settling Time Output (Trace D). Sample Gate Window's Delay and Width are Variable

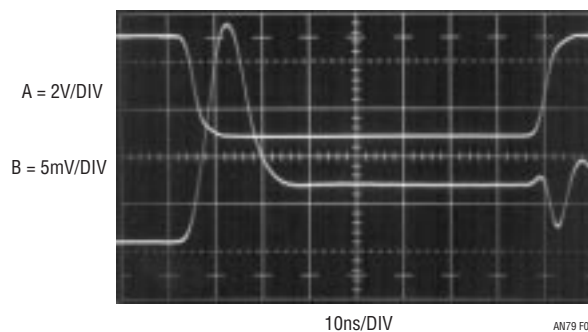


Figure 9. Settling Time Circuit's Output (Trace B) with Unadjusted Sampling Bridge AC and DC Trims. Settle Node is Grounded for This Test. Excessive Switch Drive Feedthrough and Baseline Offset are Present. Trace A is the Sample Gate

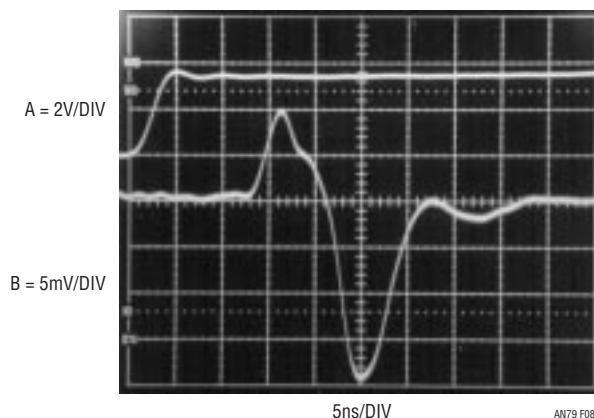


Figure 8. Expanded Vertical and Horizontal Scales Show 30ns Amplifier Settling Within 5mV (Trace B). Trace A is Time-Corrected Input Step

Trace A is the input pulse and trace B the settle signal output. With the amplifier disabled and the settle node grounded, the output should (theoretically) always be zero. The photo shows this is not the case for an untrimmed bridge. AC and DC errors are present. The sample gate's transitions cause large swings. Additionally, the output shows significant DC offset error during the sampling interval. Adjusting the AC balance and skew compensation minimizes the switching induced transients. The DC offset is adjusted out with the baseline zero trim. Figure 10 shows the results after making these adjustments. All switching related activity is minimized and offset error reduced to unreadable levels. Once this level of performance has been achieved, the circuit is nearly ready for use.⁹ Unground the settle node and restore the current switch and resistor connections to the amplifier. Any

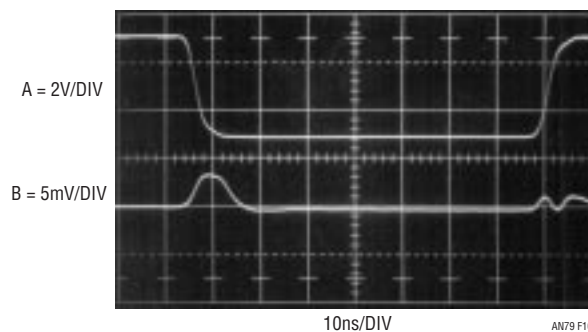


Figure 10. Settling Time Circuit's Output (Trace B) with Sampling Bridge Trimmed. As in Figure 9, Settle Node is Grounded for This Test. Switch Drive Feedthrough and Baseline Offset are Minimized. Trace A is the Sample Gate

further differences between pre- and postsettling baseline are corrected with the "settle node zero" trim.

Using the Sampling-Based Settling Time Circuit

Figures 11 and 12 underscore the importance of positioning the sampling window properly in time. In Figure 10 the sample gate delay initiates the sample window (trace A) too early and the residue amplifier's output (trace B) overdrives the oscilloscope when sampling commences. Figure 12 is better, with no off-screen activity. All amplifier settling residue is well inside the screen boundaries.

Note 9: Achieving this level of performance also depends on layout. The circuit's construction involves a number of subtleties and is absolutely crucial. Please see Appendix E, "Breadboarding, Layout and Connection Techniques."

Application Note 79

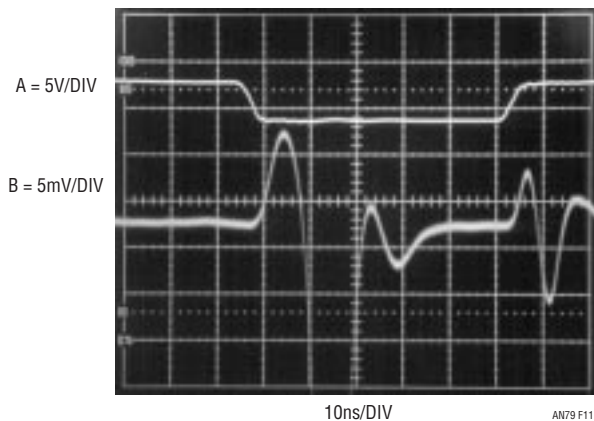


Figure 11. Oscilloscope Display with Inadequate Sample Gate Delay. Sample Window (Trace A) Occurs Too Early, Resulting in Off-Screen Activity in Settle Output (Trace B). Oscilloscope is Overdriven, Making Displayed Information Questionable

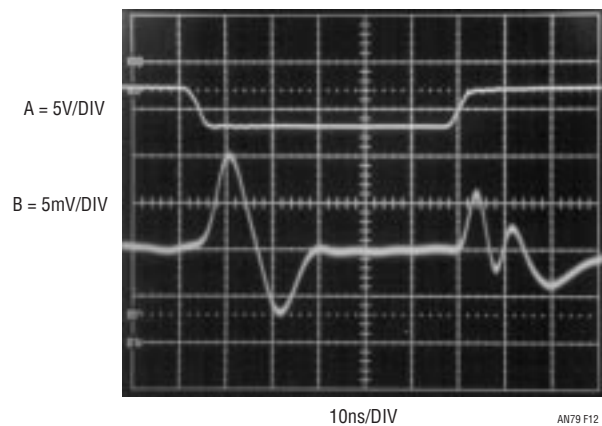


Figure 12. Optimal Sample Gate Delay Positions Sampling Window (Trace A) So All Settle Output (Trace B) Information is Well Inside Screen Boundaries

In general, it is good practice to “walk” the sampling window up to the last ten millivolts or so of amplifier slewing so that the onset of ring time is observable. The sampling based approach provides this capability and it is a very powerful measurement tool. Additionally, remember that slower amplifiers may require extended delay and/or sampling window times. This may necessitate larger capacitor values in the delayed pulse generator timing networks.

Compensation Capacitor Effects

The amplifier requires frequency compensation to get the best possible settling time.¹⁰ Figure 13 shows effects of

very light compensation. Trace A is the time-corrected input pulse and trace B the settling residue output. The light compensation permits very fast slewing but excessive ringing amplitude over a protracted time results. When sampling is initiated (just prior to the fourth vertical division) the ringing is seen to be in its final stages, although still offensive. Total settling time is about 43ns. Figure 14 presents the opposite extreme. Here a large value compensation capacitor eliminates all ringing but slows down the amplifier so much that settling stretches

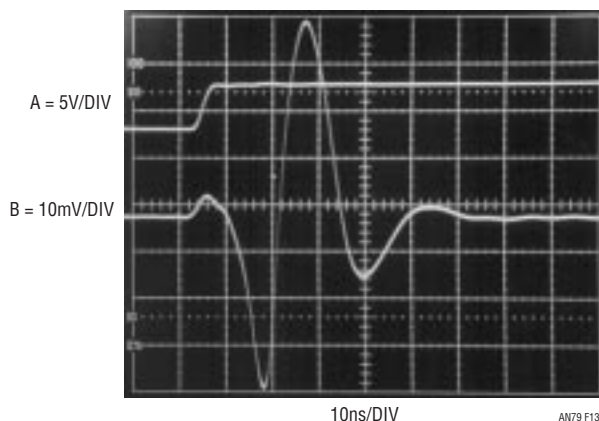


Figure 13. Settling Profile with Inadequate Feedback Capacitance Shows Underdamped Response. Trace A is Time-Corrected Input Pulse. Trace B is Settling Residue Output. $t_{SETTLE} = 43ns$

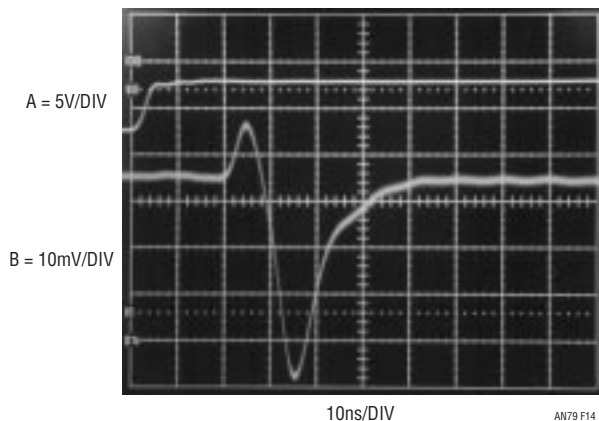


Figure 14. Excessive Feedback Capacitance Overdamps Response. $t_{SETTLE} = 50ns$

Note 10: This section discusses frequency compensation of the amplifier within the context of sampling-based settling time measurement. As such, it is necessarily brief. Considerably more detail is available in Appendix D, “Practical Considerations for Amplifier Compensation.”

out to 50ns. The best case appears in Figure 15. This photo was taken with the compensation capacitor carefully chosen for the best possible settling time. Damping is tightly controlled and settling time goes down to 30ns.

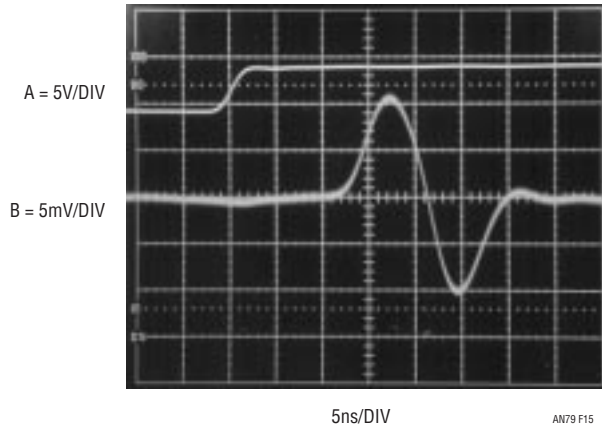


Figure 15. Optimal Feedback Capacitance Yields Tightly Damped Signature and Best Settling Time. Optimum Response Allows Expanded Horizontal and Vertical Scales. $t_{SETTLE} \leq 30ns$

Verifying Results—Alternate Method

The sampling-based settling time circuit appears to be a useful measurement solution. How can its results be tested to ensure confidence? A good way is to make the same measurement with an alternate method and see if results agree. It was stated earlier that classical sampling oscilloscopes were inherently immune to overdrive.¹¹ If this is so, why not utilize this feature and attempt settling time measurement directly at the clamped settle node? Figure 16 does this. Under these conditions, the sampling ‘scope¹² is heavily overdriven, but is ostensibly immune to the insult. Figure 17 puts the sampling oscilloscope to the test. Trace A is the time corrected input pulse and trace B the settle signal. Despite a brutal overdrive, the ‘scope appears to respond cleanly, giving a very plausible settle signal presentation.

Note 11: See Appendix A, “Evaluating Oscilloscope Overdrive Performance,” for in-depth discussion.

Note 12: Tektronix type 661 with 4S1 vertical and 5T3 timing plug-ins.

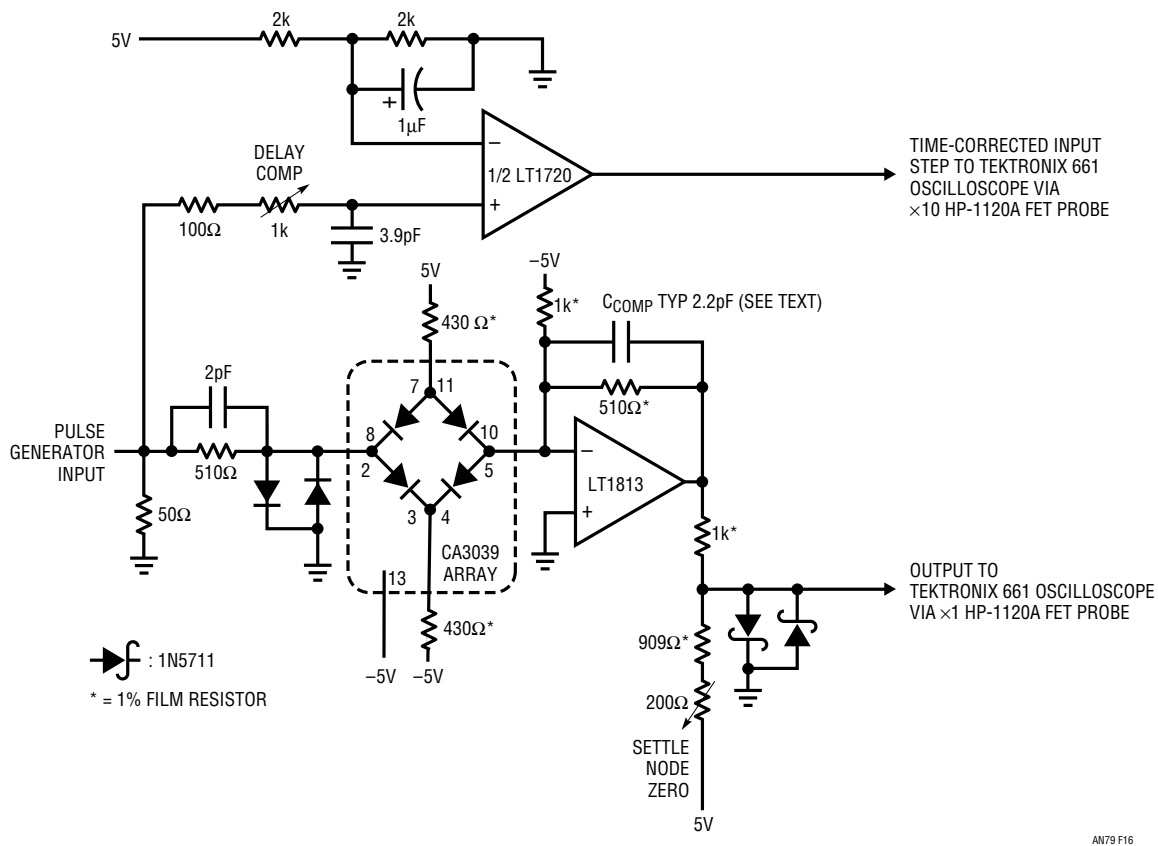


Figure 16. Settling Time Test Circuit Using Classical Sampling Oscilloscope. Sampling ‘Scope’s Inherent Overload Immunity Permits Large Off-Screen Excursions

Application Note 79

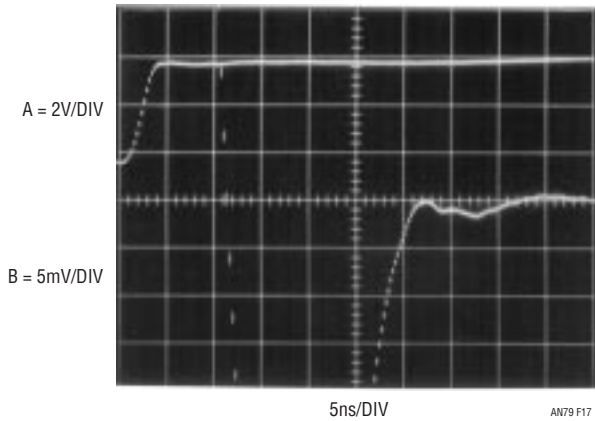


Figure 17. Settling Time Measurement with the Classical Sampling 'Scope. Oscilloscope's Overload Immunity Allows Accurate Measurement Despite Extreme Overdrive

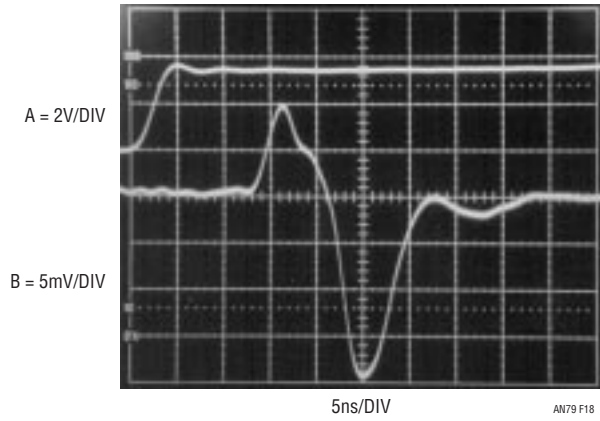


Figure 18. Settling Time Measurement Using the Sampling Bridge Circuit. $t_{SETTLE} = 30ns$

Summary of Results

The simplest way to summarize the different method's results is by visual comparison. Figures 18 and 19 repeat previous photos of the two different settling-time methods. If both approaches represent good measurement technique and are properly constructed, results should be identical.¹³ If this is the case, the identical data produced by the two methods has a high probability of being valid.

Examination of the photographs shows nearly identical settling times and settling waveform signatures. The shape of the settling waveform is essentially identical in both photos.¹⁴ This kind of agreement provides a high degree of credibility to the measured results.

Note 13: Construction details of the settling time fixtures discussed here appear (literally) in Appendix E, "Breadboarding, Layout and Connection Techniques."

Note 14: The slightly rougher appearance of figure 19's final settling movement (7th through 9th vertical divisions) may be due to the sampling 'scope's substantially higher bandwidth. Figure 18 was taken with a 150MHz instrument; sampling oscilloscope bandwidth is 1GHz.

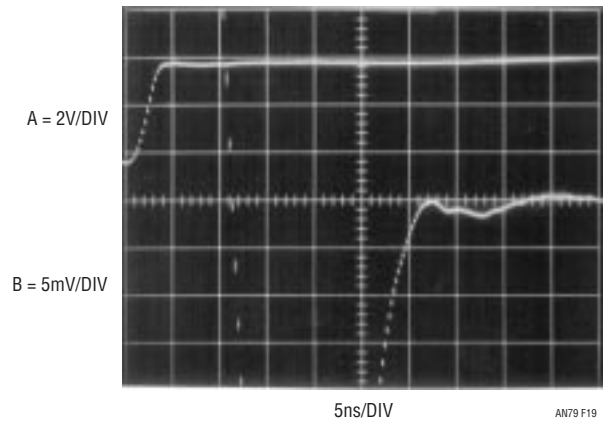


Figure 19. Settling Time Measurement using the Classical Sampling 'Scope. $t_{SETTLE} = 30ns$

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Application Note 79

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APPENDIX A

EVALUATING OSCILLOSCOPE OVERDRIVE PERFORMANCE

The sampling bridge-based settling time circuit is heavily oriented towards preventing overdrive to the monitoring oscilloscope. This is done to avoid overdriving the oscilloscope. Oscilloscope recovery from overdrive is a grey area and almost never specified. How long must one wait after an overdrive before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overdrive, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overdrive varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100× overload at 0.005V/DIV may be very different than at 0.1V/DIV. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overdrive must be approached with caution.

Why do most oscilloscopes have so much trouble recovering from overdrive? The answer to this question requires some study of the three basic oscilloscope types' vertical paths. The types include analog (Figure A1A), digital (Figure A1B) and classical sampling (Figure A1C) oscilloscopes. Analog and digital 'scopes are susceptible to overdrive. The classical sampling 'scope is the only architecture that is inherently immune to overdrive.

An analog oscilloscope (Figure A1A) is a real time, continuous linear system.¹ The input is applied to an attenuator, which is unloaded by a wideband buffer. The vertical preamp provides gain, and drives the trigger pick-off, delay line and the vertical output amplifier. The attenuator and delay line are passive elements and require little comment. The buffer, preamp and vertical output amplifier are complex linear gain blocks, each with dynamic operating range restrictions. Additionally, the operating point of each block may be set by inherent circuit balance, low frequency stabilization paths or both. When the input is overdriven, one or more of these stages may saturate, forcing internal nodes and components to abnormal operating points and temperatures. When the overload ceases, full recovery of the electronic and thermal time constants may require surprising lengths of time.²

The digital sampling oscilloscope (Figure A1B) eliminates the vertical output amplifier, but has an attenuator buffer and amplifiers ahead of the A/D converter. Because of this, it is similarly susceptible to overdrive recovery problems.

The classical sampling oscilloscope is unique. Its nature of operation makes it inherently immune to overload. Figure A1C shows why. The sampling occurs *before* any gain is taken in the system. Unlike Figure A1B's digitally sampled 'scope, the input is fully passive to the sampling point. Additionally, the output is fed back to the sampling bridge, maintaining its operating point over a very wide range of inputs. The dynamic swing available to maintain the bridge output is large and easily accommodates a wide range of oscilloscope inputs. Because of all this, the amplifiers in this instrument do not see overload, even at 1000× overdrives, and there is no recovery problem. Additional immunity derives from the instrument's relatively slow sample rate—even if the amplifiers were overloaded, they would have plenty of time to recover between samples.³

The designers of classical sampling 'scopes capitalized on the overdrive immunity by including variable DC offset generators to bias the feedback loop (see Figure A1C, lower right). This permits the user to offset a large input, so small amplitude activity on top of the signal can be accurately observed. This is ideal for, among other things, settling time measurements. Unfortunately, classical sampling oscilloscopes are no longer manufactured, so if you have one, take care of it!⁴

Note 1: Ergo, the Real Thing. Hopelessly bigoted residents of this locale mourn the passing of the analog 'scope era and frantically hoard every instrument they can find.

Note 2: Some discussion of input overdrive effects in analog oscilloscope circuitry is found in Reference 11.

Note 3: Additional information and detailed treatment of classical sampling oscilloscope operation appears in References 16–19 and 22–24.

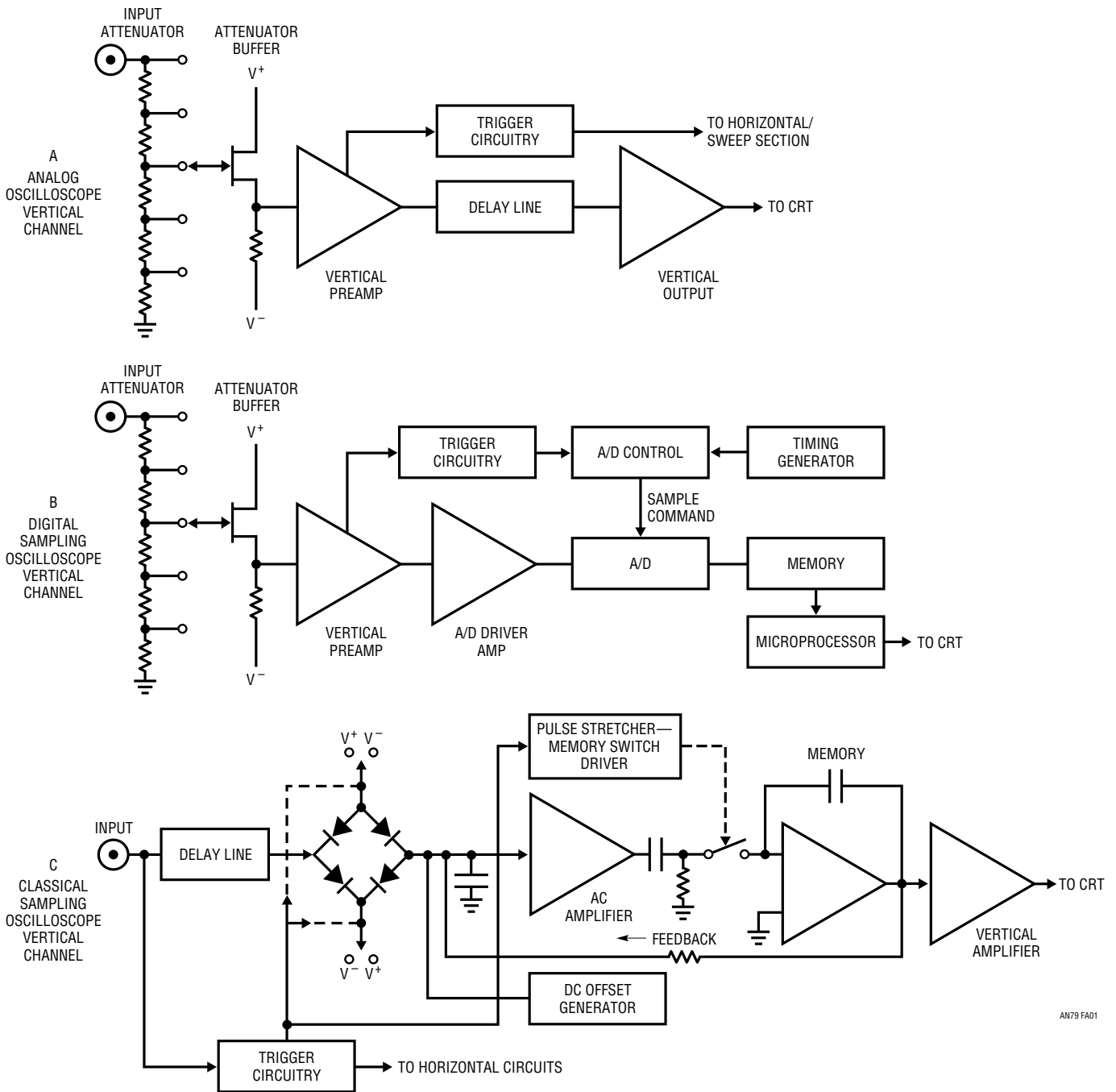
Note 4: Modern variants of the classical architecture (e.g., Tektronix 11801B) may provide similar capability, although we have not tried them.

Application Note 79

Although analog and digital oscilloscopes are susceptible to overdrive, many types can tolerate some degree of this abuse. The early portion of this appendix stressed that measurements involving oscilloscope overdrive must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity that eliminates all off-screen activity. Figure A2 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure A3) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure A4, gain has been further increased, and all the features of Figure A3 are amplified accordingly. The basic waveshape appears clearer

and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure A5 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure A4. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure A6 the gain remains the same but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure A7). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.



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Figure A1. Simplified Vertical Channel Diagrams for Different Type Oscilloscopes. Only the Classical Sampling 'Scope (C) Has Inherent Overdrive Immunity. Offset Generator Allows Viewing Small Signals Riding On Large Excursions

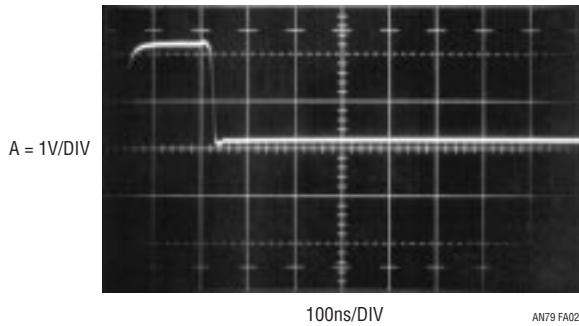


Figure A2

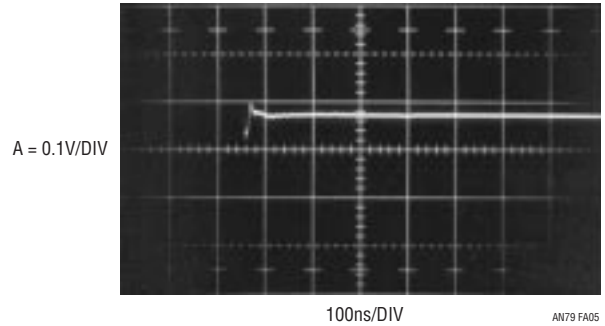


Figure A5

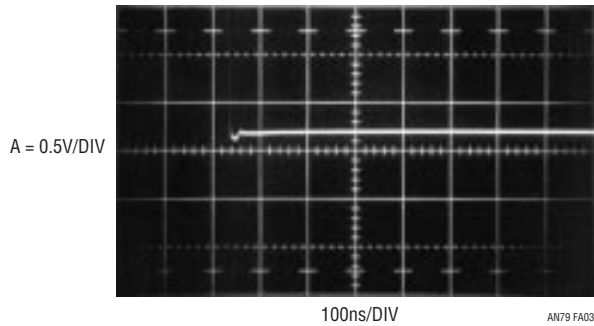


Figure A3

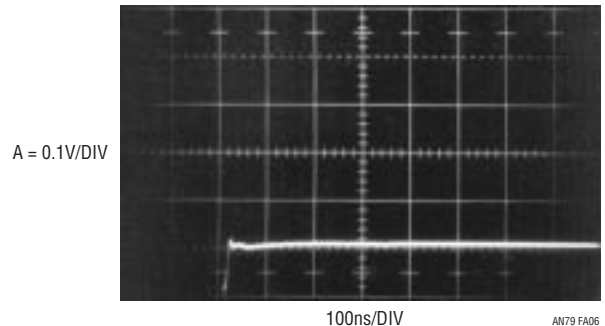


Figure A6

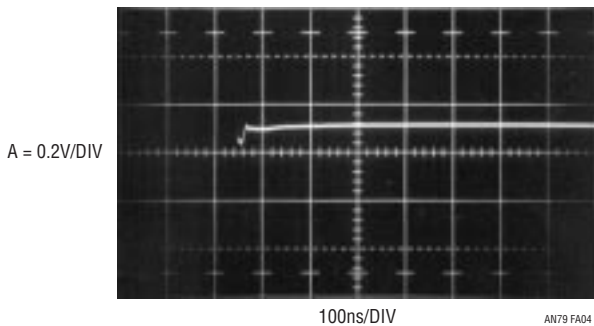


Figure A4

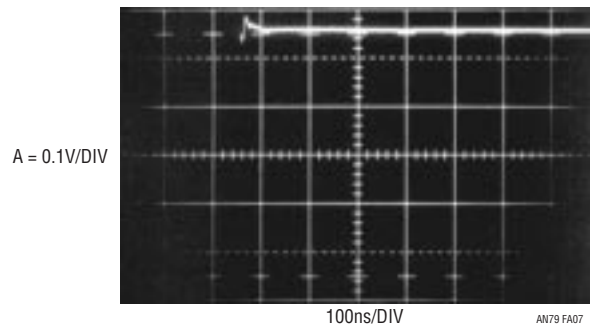


Figure A7

Figures A2–A7. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

APPENDIX B

SUBNANOSECOND RISE TIME PULSE GENERATORS FOR THE RICH AND POOR

The input diode bridge requires a subnanosecond rise time pulse to cleanly switch current to the amplifier under test. The ranks of pulse generators providing this capability are thin. Instruments with rise times of a nanosecond or less are rare, and costs are, in this author's view, excessive. Current production units can easily cost \$10,000, with prices rising towards \$30,000 depending on features. For bench work, or even production testing, there are substantially less expensive approaches.

The secondary market offers subnanosecond rise time pulse generators at attractive cost. The Hewlett-Packard HP-8082A transitions in under 1ns, has a full complement of controls, and costs about \$500. The HP-215A, long out of manufacture, has 800-picosecond edge times and is a clear bargain, with typical price below \$50. This instrument also has a very versatile trigger output, which permits continuous time phase adjustment from before to after the main output. External trigger impedance, polarity and sensitivity are also variable. The output, controlled by a stepped attenuator, will put $\pm 10V$ into 50Ω in 800ps.

The Tektronix type 109 switches in 250 picoseconds. Although amplitude is fully variable, charge lines are required to set pulse width. This reed-relay based instrument has a fixed $\approx 500Hz$ repetition rate and no external trigger facility, making it somewhat unwieldy to use. Price is typically \$20. The Tektronix type 111 is more practical. Edge times are 500 picoseconds, with fully variable repetition rate and external trigger capabilities. Pulse width is set by charge line length. Price is usually about \$25.

A potential problem with older instruments is availability.¹ As such, Figure B1 shows a circuit for producing subnanosecond rise time pulses. Rise time is 500ps, with fully adjustable pulse amplitude. An external input determines repetition rate, and output pulse occurrence is settable from before-to-after a trigger output. This circuit uses an avalanche pulse generator to create extremely fast rise-time pulses.²

Q1 and Q2 form a current source that charges the 1000pF capacitor. When the trigger input is high (trace A, Figure B2) both Q3 and Q4 are on. The current source is off and Q2's collector (trace B) is at ground. C1's latch input prevents it from responding and its output remains high. When the trigger input goes low, C1's latch input is disabled and its output drops low. Q4's collector lifts and Q2 comes on, delivering constant current to the 1000pF capacitor (trace B). The resulting linear ramp is applied to C1 and C2's positive inputs. C2, biased from a potential derived from the 5V supply, goes high 30 nanoseconds after the ramp begins, providing the "trigger output" (trace C) via its output network. C1 goes high when the ramp crosses the "delay programming voltage" input, in this case about 250ns. C1 going high triggers the avalanche-based output pulse (trace D), which will be described. This arrangement permits the delay programming voltage to vary output pulse occurrence from 30 nanoseconds before to 300 nanoseconds after the trigger output. Figure B3 shows the output pulse (trace D) occurring 30ns before the trigger output when the delay programming voltage is zero. All other waveforms are identical to Figure B2.

When C1's output pulse is applied to Q5's base, it avalanches. The result is a quickly rising pulse across R4. C1 and the charge line discharge, Q5's collector voltage falls and breakdown ceases. C1 and the charge line then recharge. At C1's next pulse, this action repeats.

Avalanche operation requires high voltage bias. The LT1082 switching regulator forms a high voltage switched mode control loop. The LT1082 pulse width modulates at its 40kHz

Note 1: Residents of Silicon Valley tend towards inbred techno-provincialism. Citizens of other locales cannot simply go to a flea market, junk store or garage sale and buy a subnanosecond pulse generator.

Note 2: The circuits operation essentially duplicates the aforementioned Tektronix type 111 pulse generator (see Reference 29). Information on avalanche operation appears in References 25–32.

Application Note 79

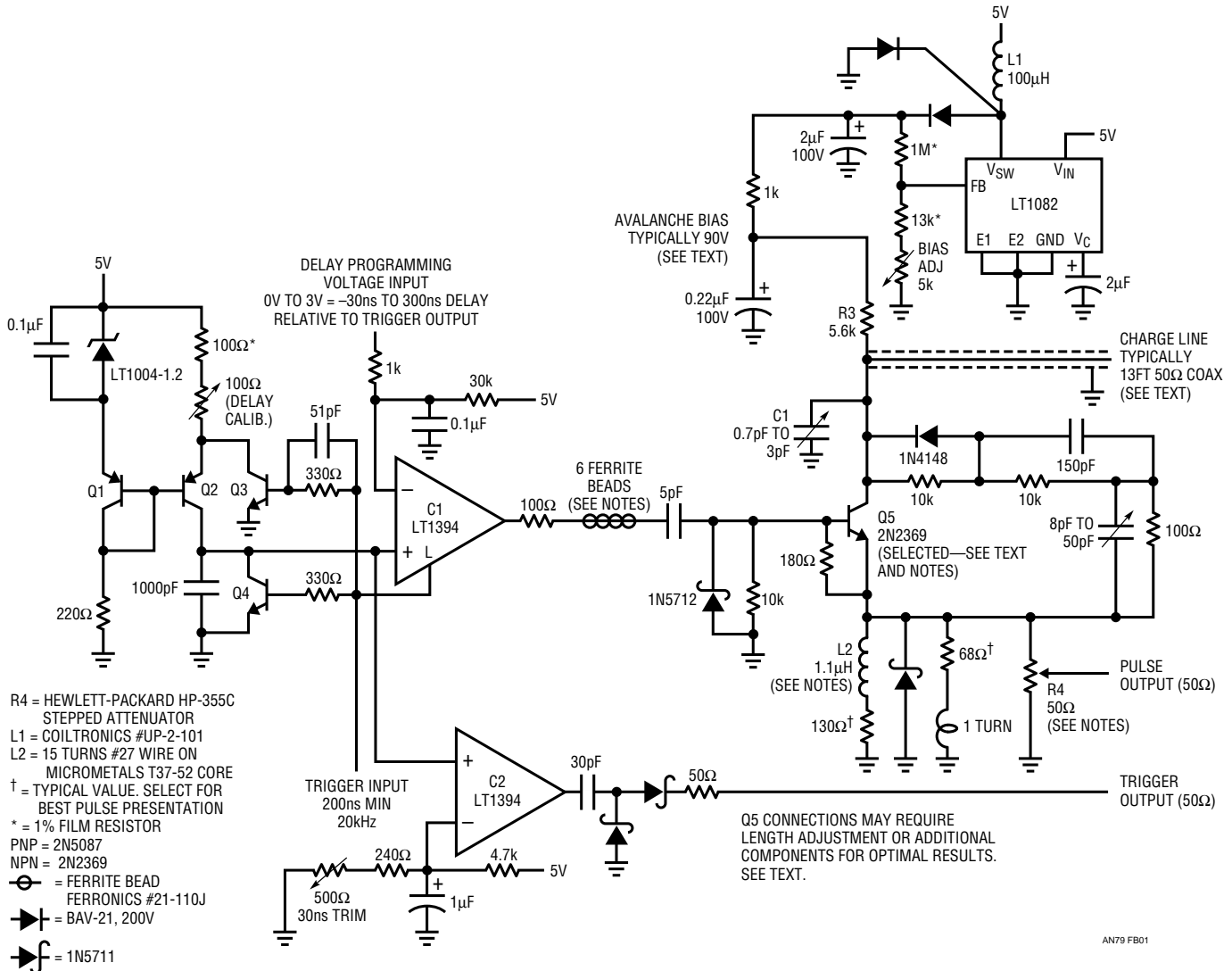


Figure B1. Programmable Delay Triggers a Subnanosecond Rise Time Pulse Generator. Charge Line at Q5's Collector Determines 40 Nanosecond Output Width. Output Pulse Occurance is Settable from Before-to-After Trigger Output

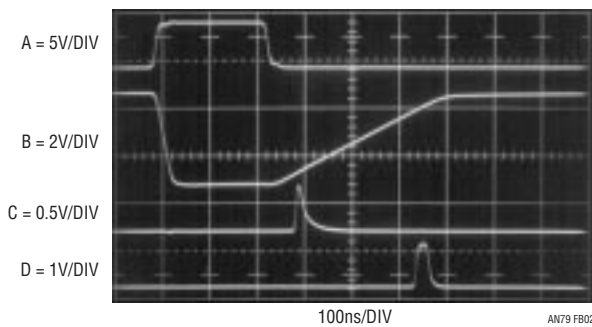


Figure B2. Pulse Generator's Waveforms Include Trigger Input (Trace A), Q2's Collector Ramp (Trace B), Trigger Output (Trace C) and Pulse Output (Trace D). Delay Sets Output Pulse ≈250ns After Trigger Output

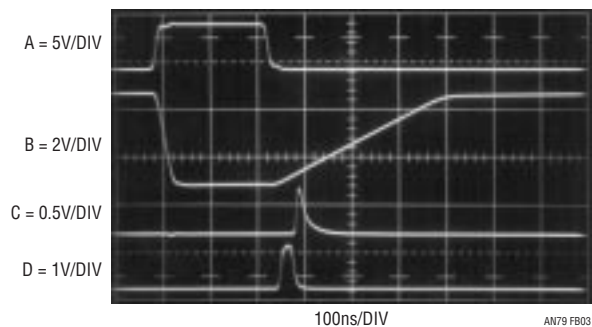


Figure B3. Pulse Generator's Waveforms with Delay Programmed for Output Pulse Occurance (Trace D) 30ns Before Trigger Output (Trace C). All Other Activity is Identical to Previous Figure

clock rate. L1's inductive events are rectified and stored in the 2 μ F output capacitor. The adjustable resistor divider provides feedback to the LT1082. The 1k-0.22 μ F RC provides noise filtering.

Figure B4, taken with a 3.9GHz bandpass oscilloscope (Tektronix 547 with 1S2 sampling plug-in) shows output pulse purity and rise time. Rise time is 500 picoseconds, with minimal preshoot and pulse top aberrations. This level of cleanliness requires considerable layout experimentation, particularly with Q5's emitter and collector lead lengths and associated components.³ Additionally, small inductances or RC networks may be required between Q5's emitter and R4 to get best pulse presentation.⁴ The charge line sets output pulse width, with 13 feet giving a 40ns wide output.

Q5 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12-year date code span, yielded 82%. All "good" devices switched in less than 600ps.

Circuit adjustment involves setting the "30ns trim" so C2 goes high 30ns after the trigger input goes low. Next, apply 3V to the delay programming input and set the "delay calibration" so C1 goes high 300ns after the trigger input goes low. Finally, set the high voltage "bias adjust" to the point where free running pulses across R4 *just* disappear with no trigger input applied.

Note 3: See References 29 and 32 for pertinent discussion.

Note 4: Ground plane type construction with high speed layout, connection and termination technique is essential for good results from this circuit. Reference 29 contains extremely useful and detailed procedures for optimizing pulse purity.

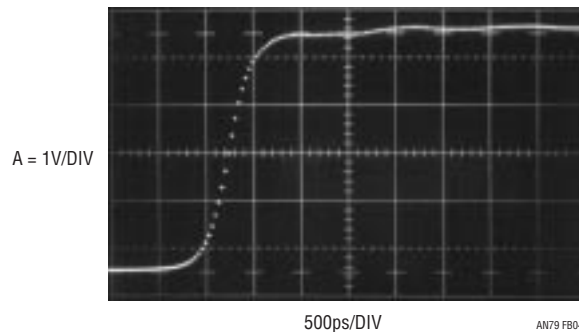


Figure B4. Pulse Generator Output Shows 500 Picosecond Rise Time with Minimal Pulse-Top Aberrations. Dot Constructed Display is Characteristic of Sampling Oscilloscope Operation

APPENDIX C

MEASURING AND COMPENSATING SETTling CIRCUIT DELAY

The settling time circuit utilizes an adjustable delay network to time correct the input pulse for delays in the signal-processing path. Typically, these delays introduce errors of 20%, so an accurate correction is required. Setting the delay trim involves observing the network's input-output delay and adjusting for the appropriate time interval. Determining the "appropriate" time interval is somewhat more complex. A wideband oscilloscope with FET probes is required. To ensure accuracy in the following delay measurements probe time skew must be verified. The probes are both connected to a fast rise ($< 1\text{ns}$) pulse generator to measure the skew. Figure C1 shows less than 50 picoseconds skewing. This ensures small error for the delay measurements, which will be in the nanosecond range.

Referring to text Figure 6, it is apparent that three delay measurements are of interest. The pulse generator to amplifier-under-test, the amplifier-under-test to settle node,

and the amplifier-under-test to output. Figure C2 shows 800 picoseconds delay from the pulse generator input to the amplifier-under-test. Figure C3 indicates 2.5 nanoseconds from the amplifier-under-test to the settle node. Figure C4 indicates 5.2 nanoseconds from the amplifier-under-test to the output. In Figure C3's measurement, the probes see severe source impedance mismatch. This is compensated by adding a series 500Ω resistor to the probe monitoring the amplifier-under-test. This provision approximately equalizes probe source impedances, negating the probe's input capacitance ($\approx 1\text{pF}$) term.

The measurements reveal a circuit input-to-output delay of 6 nanoseconds, and this correction is applied by adjusting the 1k trim at the C1 delay compensation comparator. Similarly, when the sampling 'scope is used, the relevant delays are Figures C2 and C3, a total of 3.3ns. This figure is applied to the delay compensation adjustment when the sampling 'scope-based measurement is taken.

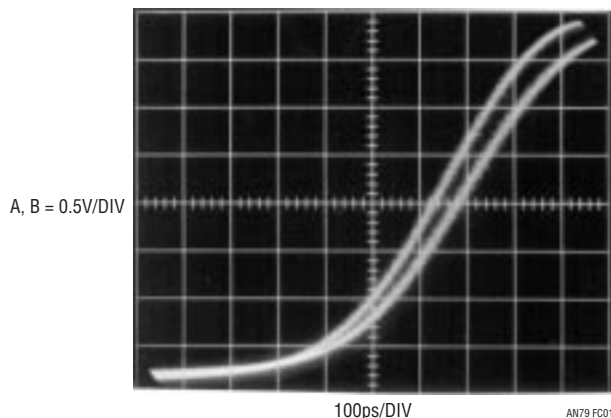


Figure C1. FET Probe-Oscilloscope Channel-to-Channel Timing Skew Measures 50 Picoseconds

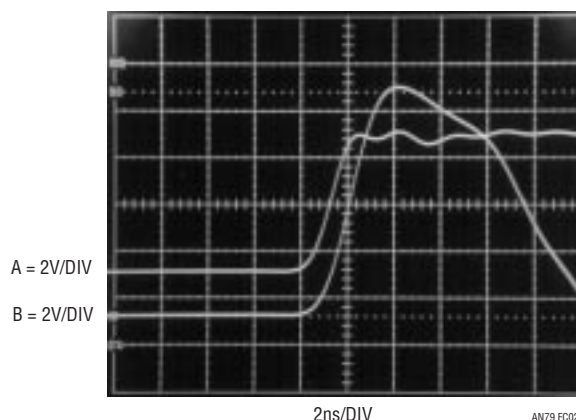


Figure C2. Pulse Generator (Trace A) to Amplifier-Under-Test Negative Input (Trace B) Delay is 800 Picoseconds

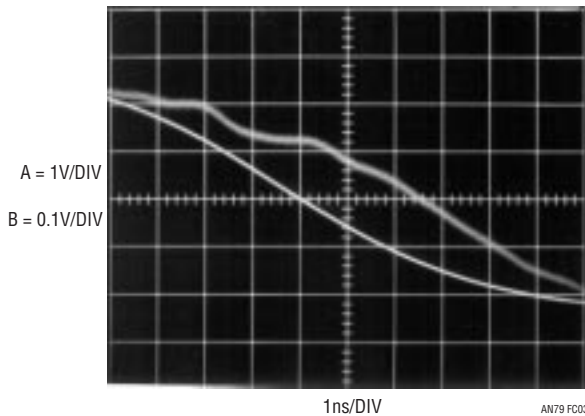


Figure C3. Amplifier-Under-Test Output (Trace A) to Settle Node (Trace B) Delay is 2.5 Nanoseconds

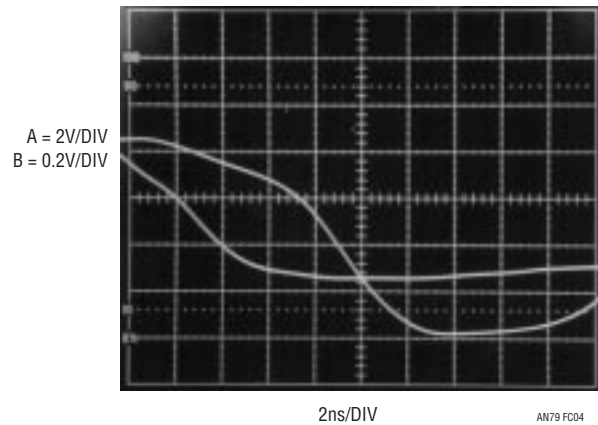


Figure C4. Amplifier-Under-Test (Trace A) to Output (Trace B) Delay Measures 5.2 Nanoseconds

APPENDIX D

PRACTICAL CONSIDERATIONS FOR AMPLIFIER COMPENSATION

There are a number of practical considerations in compensating the amplifier to get fastest settling time. Our study begins by revisiting text Figure 1 (repeated here as Figure D1). Settling time components include delay, slew and ring times. Delay is due to propagation time through the amplifier and is a relatively small term. Slew time is set by the amplifier's maximum speed. Ring time defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. Once an amplifier has been chosen, only ring time is readily adjustable. Because slew time is usually the dominant lag, it is tempting to select the fastest slewing amplifier available to obtain best settling. Unfortunately, fast slewing amplifiers usually have extended ring times, negating their brute force speed advantage. The penalty for raw speed is, invariably, prolonged ringing, which can only be damped with large compensation capacitors. Such compensation works, but results in protracted settling times. The key to good settling times is to choose an amplifier with the right balance of slew rate and recovery characteristics and compensate it properly. This is harder than it sounds because amplifier settling time cannot be predicted or extrapolated from any combination of data sheet speci-

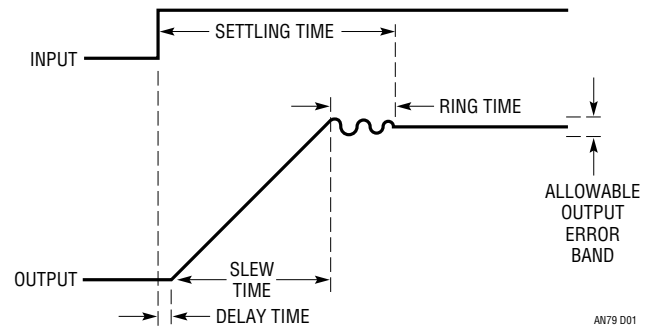


Figure D1. Amplifier Settling Time Components Include Delay, Slew and Ring Times. For Given Components, Only Ring Time is Readily Adjustable

cations. It must be measured in the intended configuration. A number of terms combine to influence settling time. They include amplifier slew rate and AC dynamics, layout capacitance, source resistance and capacitance, and the compensation capacitor. These terms interact in a complex manner, making predictions hazardous.¹ If the parasitics are eliminated and replaced with a pure resistive source, amplifier settling time is still not readily predictable. The parasitic impedance terms just make a difficult problem more messy. The only real handle available to deal with all this is the feedback compensation capacitor, C_F . C_F 's purpose is to roll off amplifier gain at the frequency that permits best dynamic response.

Note 1: Spice aficionados take notice.

Application Note 79

Best settling results when the compensation capacitor is selected to functionally compensate for all the above terms. Figure D2 shows results for an optimally selected feedback capacitor. Trace A is the time-corrected input pulse and trace B the amplifier's settle signal. The amplifier is seen to come cleanly out of slew (sample gate opens just prior to sixth vertical division) and settle very quickly.

In Figure D3, the feedback capacitor is too large. Settling is smooth, although overdamped, and a 20ns penalty results. Figure D4's feedback capacitor is too small, causing a somewhat underdamped response with resultant excessive ring time excursions. Settling time goes out to 43ns. Note that Figures D3 and D4 require reduction of vertical and horizontal scales to capture nonoptimal response.

When feedback capacitors are individually trimmed for optimal response, the source, stray, amplifier and compensation capacitor tolerances are irrelevant. If individual trimming is not used, these tolerances must be considered to determine the feedback capacitor's production value. Ring time is affected by stray and source capaci-

tance and output loading, as well as the feedback capacitor's value. The relationship is nonlinear, although some guidelines are possible. The stray and source terms can vary by $\pm 10\%$ and the feedback capacitor is typically a $\pm 5\%$ component.² Additionally, amplifier slew rate has a significant tolerance, which is stated on the data sheet. To obtain a production feedback capacitor value, determine the optimum value by individual trimming *with the production board layout* (board layout parasitic capacitance counts too!). Then, factor in the worst-case percentage values for stray and source impedance terms, slew rate and feedback capacitor tolerance. Add this information to the trimmed capacitors measured value to obtain the production value. This budgeting is perhaps unduly pessimistic (RMS error summing may be a defensible compromise), but will keep you out of trouble.³

Note 2: This assumes a resistive source. If the source has substantial parasitic capacitance (photodiode, DAC, etc.), this number can easily enlarge to $\pm 50\%$.

Note 3: The potential problems with RMS error summing become clear when sitting in an airliner that is landing in a snowstorm.

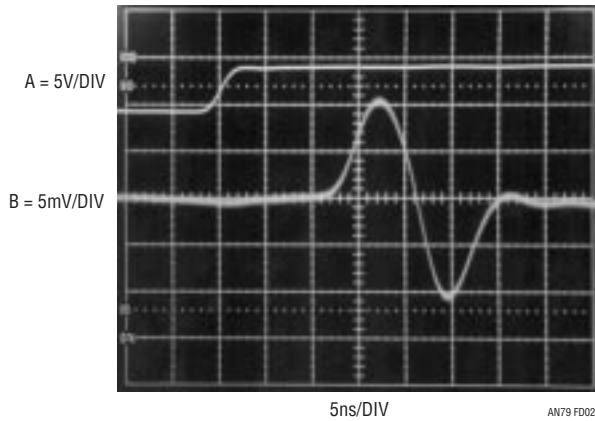


Figure D2. Optimized Compensation Capacitor Permits Nearly Critically Damped Response, Fastest Settling Time. $t_{SETTLE} = 30ns$

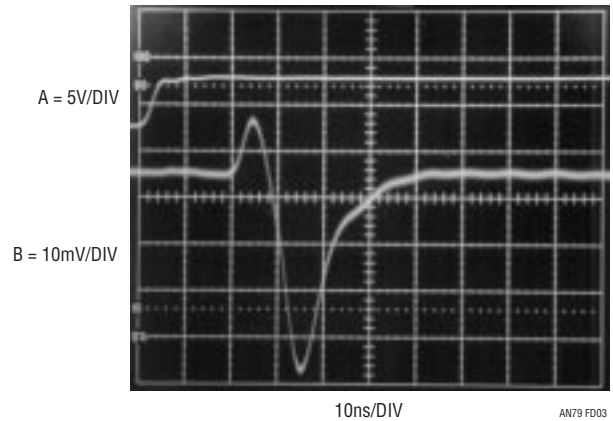


Figure D3. Overdamped Response Ensures Freedom from Ringing, Even with Component Variations in Production. Penalty is Increased Settling Time. Note Horizontal and Vertical Scale Changes vs Figure D2. $t_{SETTLE} = 50ns$

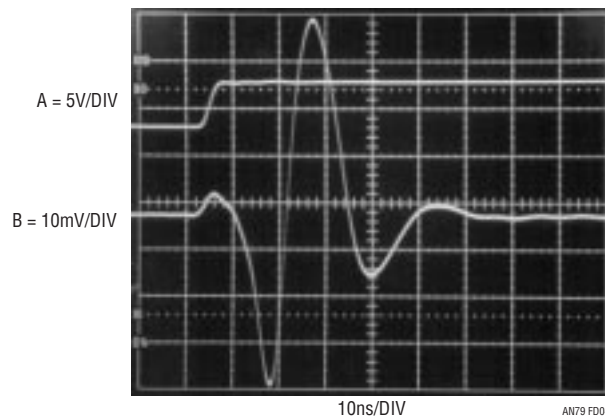


Figure D4. Underdamped Response Results from Undersized Capacitor. Component Tolerance Budgeting Will Prevent This Behavior. Note Vertical and Horizontal Scale Changes vs Figure D2. $t_{SETTLE} = 43ns$

APPENDIX E

BREADBOARDING, LAYOUT AND CONNECTION TECHNIQUES

The measurement results presented in this publication required painstaking care in breadboarding, layout and connection techniques. Nanosecond domain, high resolution measurement does not tolerate cavalier laboratory attitude. The oscilloscope photographs presented, devoid of ringing, hops, spikes and similar aberrations, are the result of a careful breadboarding exercise. The sampler-based breadboard required considerable experimentation before obtaining a noise/uncertainty floor worthy of the measurement.

Ohm's Law

It is worth considering that Ohm's law is a key to successful layout.¹ Consider that 10mA running through 1 Ω generates 10mV—twice the measurement limit! Now, run that current at 1 nanosecond rise times (≈ 350 MHz) and the need for layout care becomes clear. A paramount concern is disposal of circuit ground return current and disposition of current in the ground plane. The impedance of the ground plane between any two points is *not* zero, particularly at nanosecond speeds. This is why the entry point and flow of “dirty” ground returns must be carefully placed within the grounding system. In the sampler-based breadboard, the approach was separate “dirty” and “signal” ground planes tied together at the supply ground origin.

A good example of the importance of grounding management involves delivering the input pulse to the breadboard. The pulse generator's 50 Ω termination *must* be an in-line coaxial type, and it cannot be directly tied to the signal ground plane. The high speed, high density (5V pulses through the 50 Ω termination generate 100mA current spikes) current flow must return directly to the pulse generator. The coaxial terminator's construction ensures this substantial current does this, instead of being dumped into the signal ground plane (100mA termination current flowing through 50 *milliohms* of ground plane produces ≈ 5 mV of error!). Figure E3 shows that the BNC shield floats from the signal plane, and is returned to “dirty” ground via a copper strip. Additionally, Figure E1 shows the pulse generator's 50 Ω termination physically distanced from the breadboard via a coaxial extension tube. This further ensures that pulse generator return current circulates in a tight local loop at the terminator, and does not mix into the signal plane.

It is worth mentioning that, because of the nanosecond speeds involved, inductive parasitics may introduce more error than resistive terms. This often necessitates using flat wire braid for connections to minimize parasitic inductive and skin effect-based losses. Every ground return and signal connection in the entire circuit must be evaluated with these concerns in mind. A paranoiac mindset is quite useful.

Note 1: I do not wax pedantic here. My guilt in this matter runs deep.

Shielding

The most obvious way to handle radiation-induced errors is shielding. Various following figures show shielding. Determining where shields are required should come *after* considering what layout will minimize their necessity. Often, grounding requirements conflict with minimizing radiation effects, precluding maintaining distance between sensitive points. Shielding is usually an effective compromise in such situations.

A similar approach to ground path integrity should be pursued with radiation management. Consider what points are likely to radiate, and try to lay them out at a distance from sensitive nodes. When in doubt about odd effects, experiment with shield placement and note results, iterating towards favorable performance.² *Above all, never rely on filtering or measurement bandwidth limiting to “get rid of” undesired signals whose origin is not fully understood.* This is not only intellectually dishonest, but may produce wholly invalid measurement “results,” even if they look pretty on the oscilloscope.

Connections

All signal connections to the breadboard must be coaxial. Ground wires used with oscilloscope probes are forbidden. A 1" ground lead used with a ‘scope probe can easily generate large amounts of observed “noise” and seemingly inexplicable waveforms. Use coaxially mounting probe tip adapters!³

Figures E1 to E6 restate the above sermon in visual form while annotating the text’s measurement circuits.

Note 2: After it works, you can figure out why.

Note 3: See Reference 35 for additional nagging along these lines.

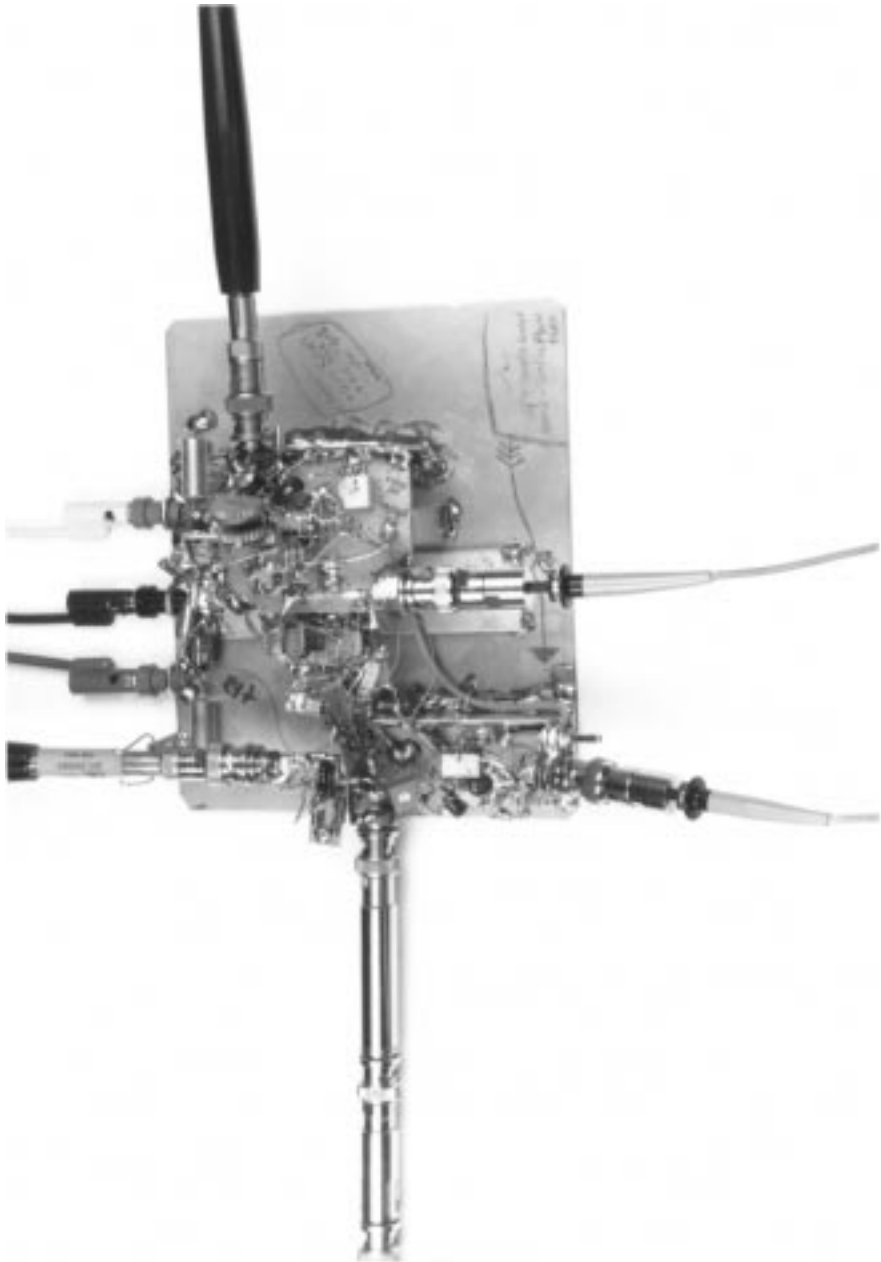


Figure E1. Overview Of Settling Time Breadboard. Pulse Generator Enters Left Side—50Ω Coaxial Terminator Mounted On Extension Tube Minimizes Pulse Generator Return Current Mixing Into Signal Ground Planes (Bottom and Raised Center Boards). Delayed Pulse Generator is Lower Left. Delay Compensation Is Small Board Above Extension Tube (Center Left). Input Bridge-Amplifier-Under-Test Is Between Raised Board (Center) and Delay Pulse Generator (Lower Left). Raised Board Is Sampling Bridge and Drive Circuitry. Note All Coaxial Signal and Probe Connections

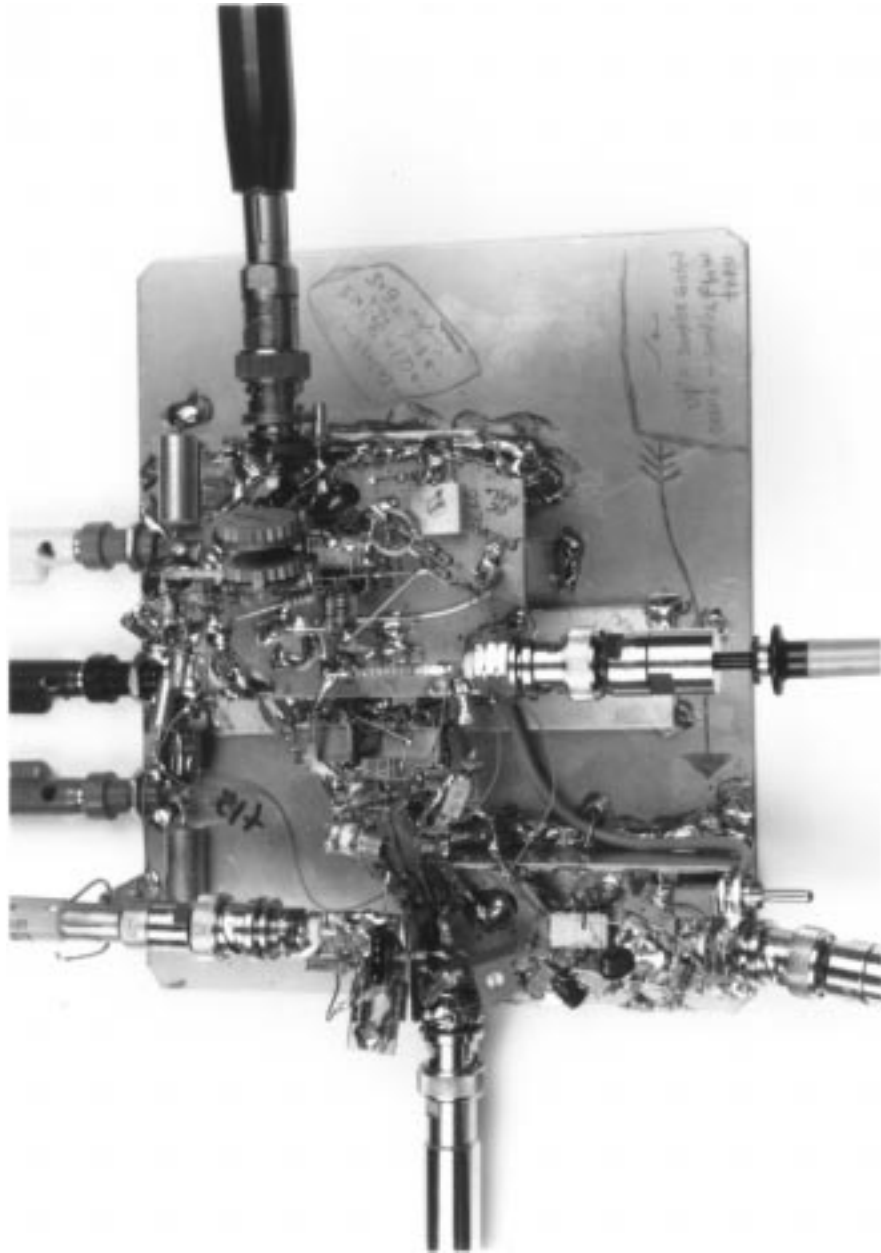


Figure E2. Settling Time Breadboard Detail. Note Radiation Shield (Vertical Board Lower Left) at Delayed Pulse Generator (Lower Left). "Dirty" Ground Return Is Wide Copper Strip Running from Board Lower Center to Banana Jack (Photo Upper Center). Sampling Bridge Circuitry Is Raised Board (Photo Center Right, Foreground). AC Trims (Raised Board Center Right) and DC Adjustment (Raised Board Lower Right) Are Visible

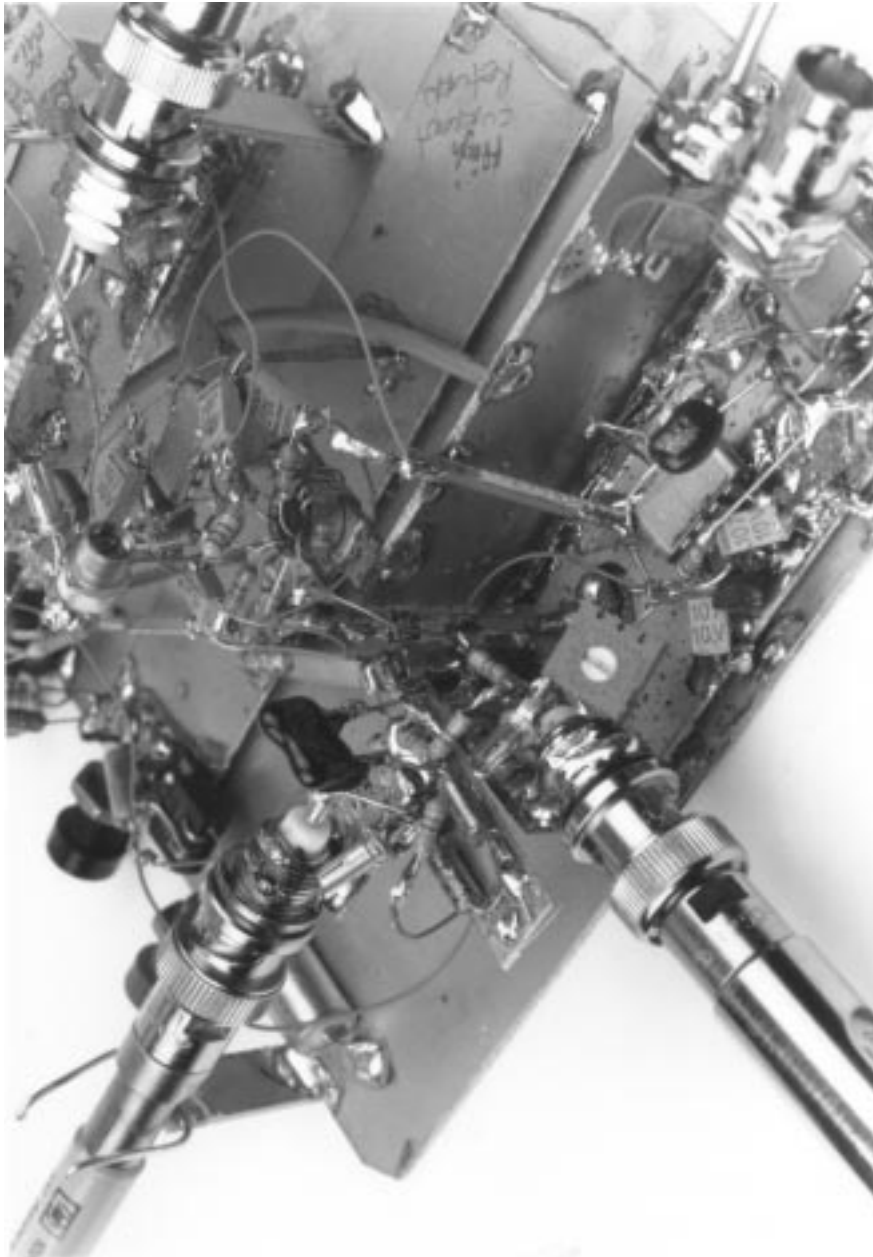


Figure E3. Detail of Pulse Generator Input and Delay Compensation. Delay Compensation Circuitry is Small Board Above Pulse Generator Coaxial BNC Fitting (Photo Center Left). Pulse Generator BNC Common Floats from Main Board Via Insulated Vertical Support (Soldered to BNC—Photo Lower Center Left). BNC Is Tied to Ground “Mecca” By Thin Copper Strip (Photo Center Left) Running at Angle to Main Board. Input Bridge and Amplifier-Under-Test Occupy Photo Center Right. “Dirty” Ground Return Bus (Large Rectangular Board) Runs Across Main Board, Ends at Banana Jack

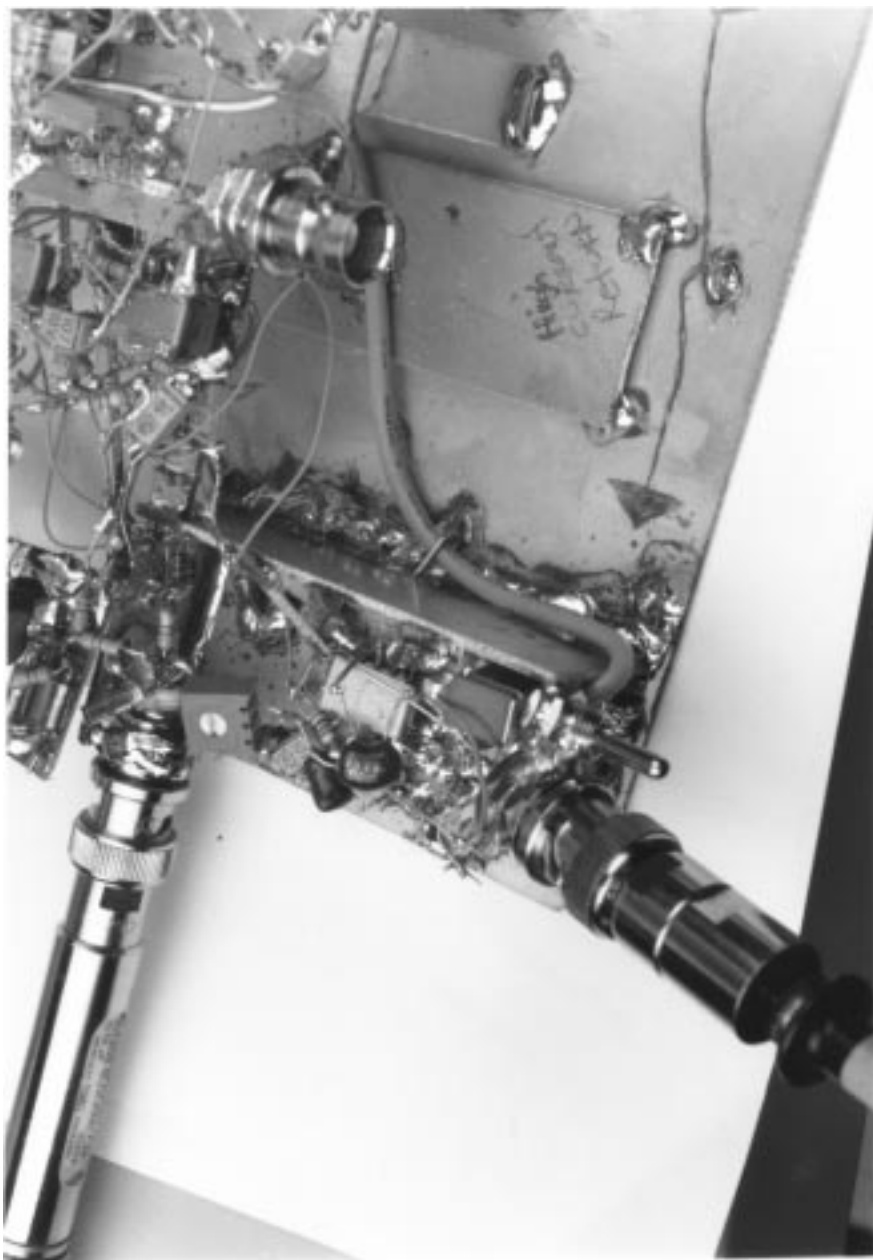


Figure E4. Delayed Pulse Generator Is Fully Shielded from Input Bridge and Sampler Circuitry (Both Partially Visible, Photo Upper Right). Shield Is Vertical Board (Photo Center). Delayed Pulse Generator Output Routes to Sampling Bridge Via Coaxial Cable (Photo Center Right), Minimizing Radiation



Figure E5. Input Bridge and Amplifier-Under-Test (AUT) Detail. Pulse Generator Enters Lower Left. Input Bridge Is IC Can (Photo Center); AUT Just Above. AUT Feedback Trim Capacitor Is Upper Center. IC Behind Trim Capacitor Is Bridge Driver Amplifier. Sampling Bridge (Partial) Is Photo Upper. Probe (Photo Extreme Right) Monitors Sampler Input. FET Probe (Photo Extreme Left) Measures Delay Compensated Input Pulse

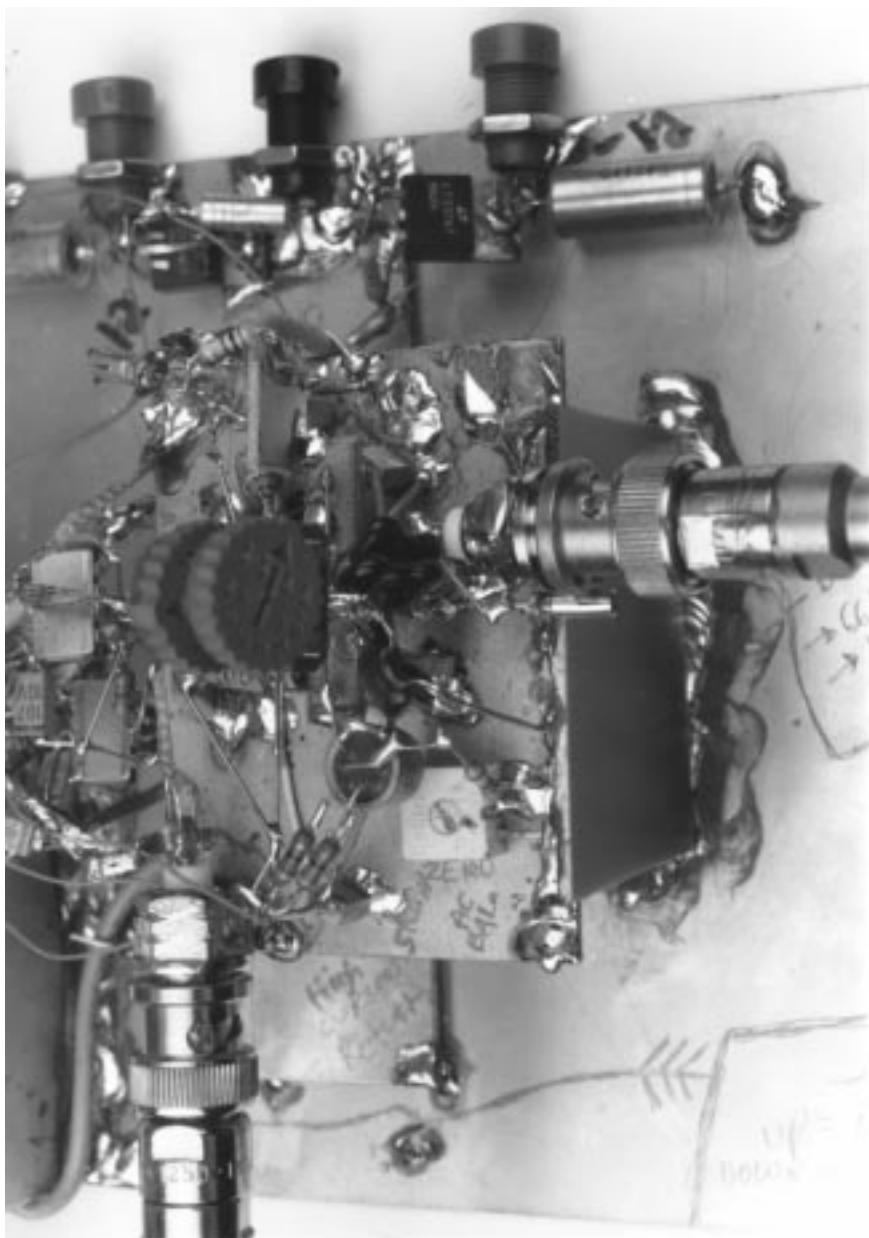
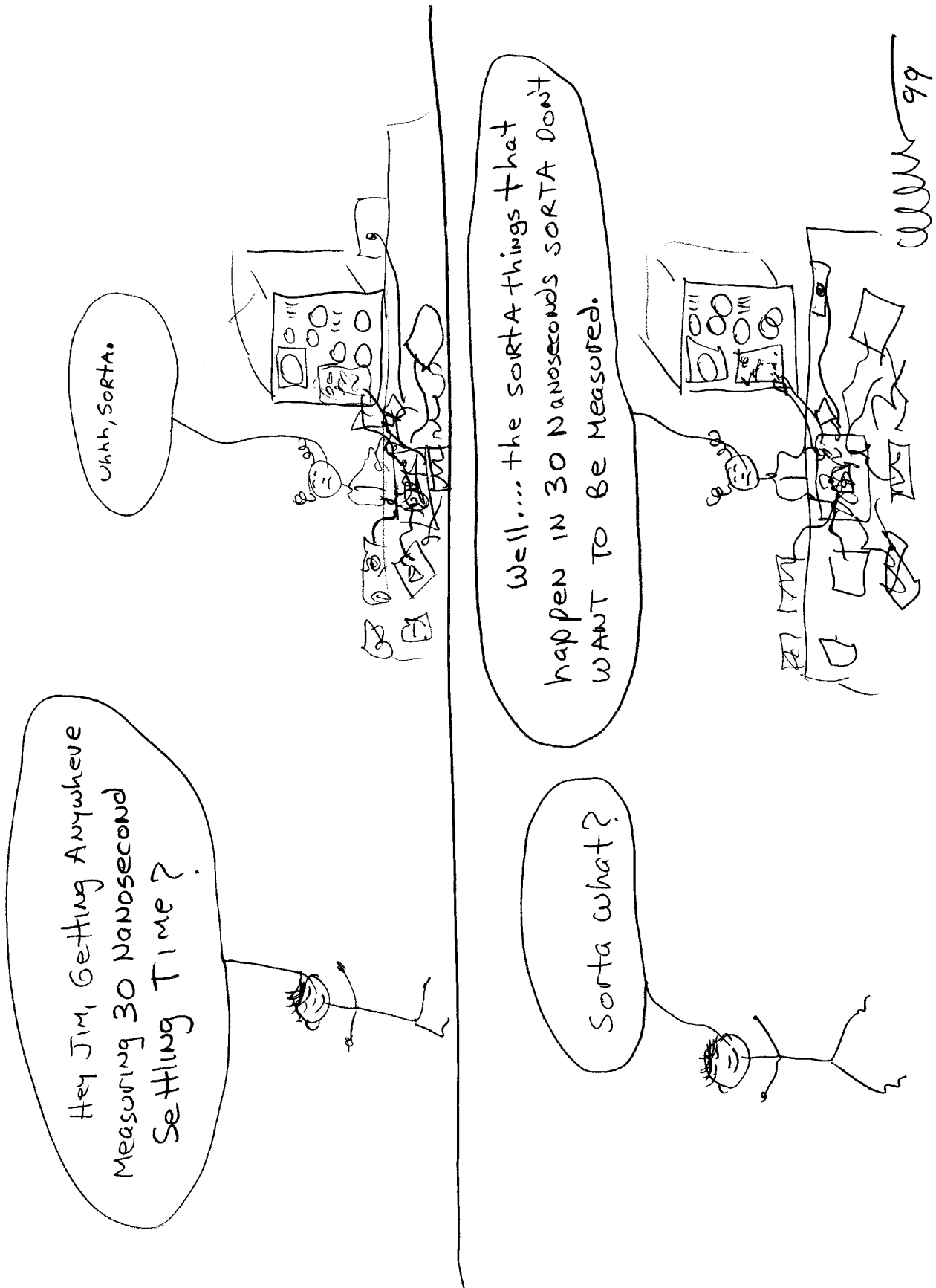


Figure E6. Sampling Bridge Viewed from Above. Sample Gate Coaxial Cable Starts at Delayed Pulse Generator (Photo Extreme Upper Left), Goes Under Sampler Board (Photo Center), Reappears at Sample Board Right Side. Note Vertical Shield Preventing Sample Gate Pulse Radiation from Corrupting Sampler Output. Sampler DC Zero Trim Is Square Potentiometer (Sampler Board Lower Left); Skew and AC Balance Adjustments Are Photo Upper Center. Sampling Bridge Diodes (Not Visible) Are Directly Beneath Shielded Section Below Skew and Balance Trims



Ultracompact LCD Backlight Inverters

A Svelte Beast Cuts High Voltage Down to Size

Jim Williams, Linear Technology Corporation

Jim Phillips, Gary Vaughn, CTS Wireless Components

INTRODUCTION

The liquid crystal display (LCD) has become ubiquitous. It is in use everywhere, from personal computers of all sizes to point-of-sale terminals as well as instruments, autos and medical apparatus. The LCD utilizes a cold cathode fluorescent lamp (CCFL) as a light source to back light the display. The CCFL requires a high voltage AC supply for operation. Typically, over 1000 volts RMS is required to initiate lamp operation, with sustaining voltages ranging from 200VAC to 800VAC. To date, the high voltage section of backlight "inverters" has been designed around magnetic transformers. A great deal of effort has been directed towards these ends, accompanied by a large volume of descriptive material.¹ Unfortunately, as available circuit board space continues to shrink, magnetic transformer based approaches begin to encounter difficulty. In particular, it is highly desirable to fashion laptop computers with large area screens, leaving little room for the backlight inverter board. In many cases there is so little space available that building the inverter function inside the LCD panel has become attractive, although to date impractical.

Limitations and Problems of Magnetic CCFL Transformers

Construction and high voltage breakdown characteristics of magnetic transformers present barriers to implementing them in these forthcoming space intensive designs. Additionally, as refined as magnetic technology is, other inverter problems associated with it also exist. Such problems include the necessity to optimize and calibrate the inverter for best performance with a given display type. Practically, this means that the manufacturer must, via either hardware or software, adjust inverter parameters to achieve optimum performance with a given display type. Changes in display choice must be accompanied by com-

mensurate adjustments in inverter characteristics. Another problem area is fail-safe protection due to self-destructive transformer malfunctions. Finally, the magnetic field provided by conventional transformers can interfere with operation of adjacent circuitry. With the exception of size, all of these problems are addressable, although incurring economic and circuit/system penalties.² What is really needed is high voltage generating capability that is inherently better suited to coming generations of backlight inverters. Piezoceramic transformers, an arcane and little known technology, has been tamed and made available for CCFL inverter use. This publication summarizes results of an extensive collaborative development effort between LTC and CTS Wireless Components (formerly Motorola Ceramic Products).

Piezoelectric Transformers

Piezoelectric Transformers (PZT), like magnetic devices, are basically energy converters. A magnetic transformer operates by converting an electrical input to magnetic energy and then reconverting the magnetic energy back to an electrical output. A PZT has an analogous operating mechanism. It converts an electrical input into *mechanical* energy and subsequently reconverts this mechanical energy back to an electrical output. The mechanical transport causes the PZT to vibrate, similar to quartz crystal operation, although at acoustic frequencies. The resonance associated with this acoustic activity is extraordinarily high; Q factors over 1000 are typical. This transformer action is accomplished by utilizing properties of certain

Note 1: See References 1 through 3 for examples.

Note 2: Again, see References 1 through 3.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

Piezoceramic inverter circuits and techniques are covered by LTC patents issued and pending. CTS Wireless Components (formerly Motorola Ceramic Products) patents, issued and pending, also apply.

Application Note 81

ceramic materials and structures. A PZT transformer's voltage gain is set by its physical configuration and the number of layers in its construction. This is obviously very different from a magnetic transformer, although some (very rough) magnetic analogs are turns ratio and core configuration. Also very different, and central to any serious drive scheme attempt, is that a PZT has a large input capacitance, as opposed to a magnetic transformer's input inductance.³

Figures 1 and 2 show PZTs; the surprisingly small size is readily apparent. The form factor is ideal for constructing space efficient CCFL backlight inverters. A complete, practical inverter appears in Figure 3.

Note 3: To call this description of PZT operation abbreviated is the kindest of verbiage. Those interested in piezoceramic theory, whether savant or scholar, will find tutorial in Appendices A and B. Appendix A is a brief treatment; B is considerably more detailed. Both sections were written by Jim Phillips of CTS Wireless Components.

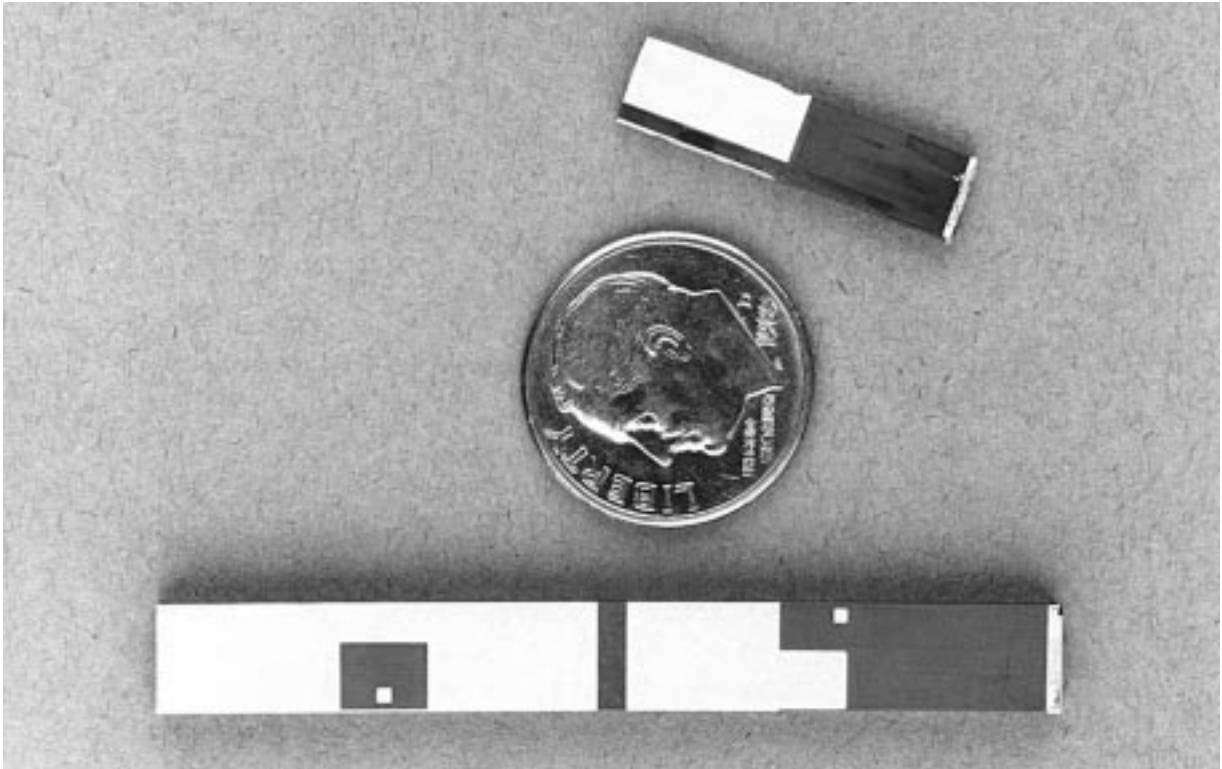


Figure 1. Piezoceramic Transformers Compared to a Dime for Size. 1.5 Watt (Photo Upper) and 10 Watt (Photo Lower) Units Are Shown. Devices Are Narrower Than Magnetic Transformers

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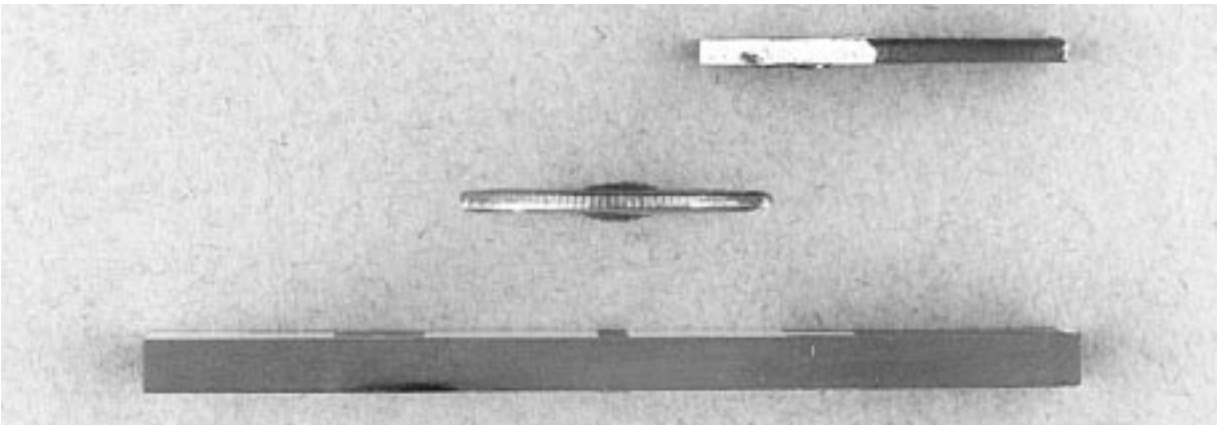


Figure 2. Figure 1's Piezoceramic Transformers Rotated to Show Height. Dime Is Photo Center. Height Is Smaller Than Magnetic Types

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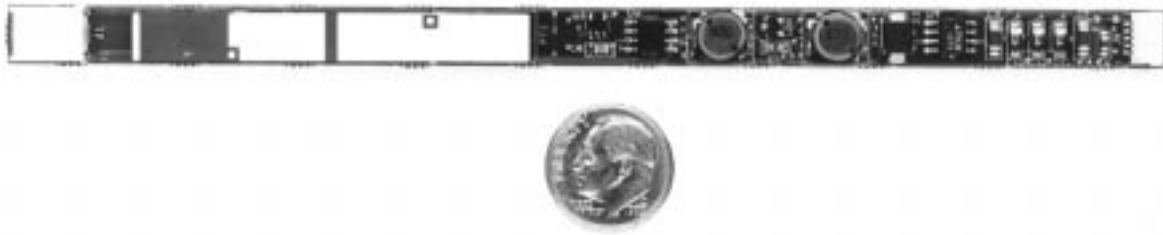


Figure 3. Complete LCD Backlight Inverter Compared to Dime for Size. Piezoceramic Transformer (Photo Left) Permits Significantly Thinner Board Size

Piezoelectric transformer technology is not new. It has been employed before, in various forms.⁴ More familiar examples of piezoelectrics are barbecue grill ignitors (direct mechanical input to the PZT produces an electrical discharge) and marine sonar transducers (electrical input produces a pronounced sonic output). Piezoelectrics are also used in speakers (tweeters), medical ultrasound transducers, mechanical actuators and fans. Piezoelectric based backlight inverters have been attempted, but previous transformer and circuit approaches could not provide power, efficiency and wide dynamic range of operation. Transformer operating regions were restricted, with complex and ill-performing electronic control schemes. Additionally, the PZT mounting schemes employed enlarged size, negating the PZT's size advantage.

Developing a PZT Transformer Control Scheme

It is instructive to review the path to a practical circuit. Figure 4 treats the PZT like a quartz crystal, placing it in a Pierce type oscillator.⁵ Self-resonance occurs and a sinusoidal AC high voltage drives the lamp. This circuit has a number of unpleasant features. Very little power is available, due to the circuit's high output impedance. Additionally, the PZT has a number of other spurious modes besides its desired 60kHz fundamental. Changes in drive level or load characteristics induce "mode-hopping," manifested by PZT resonance jumping to subharmonics or harmonics. Sometimes, several modes occur simultaneously! Operation in these modes is characterized by low efficiency and instability. Practically, this circuit was never intended as a serious candidate, only an exploratory exercise. Its contribution is demonstrating that PZT self-resonance is a potentially viable path. Figure 5, a feedback oscillator, addresses the high output impedance problem with a totem style pair. This is partially successful, al-

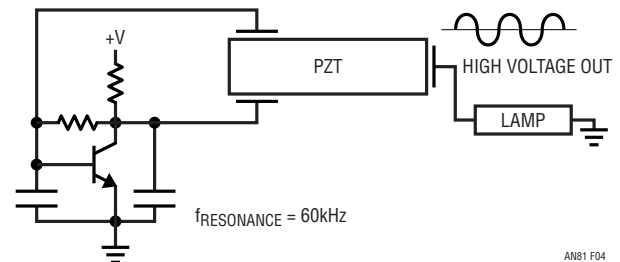


Figure 4. Pierce Type Circuit Sustains Resonance, But Cannot Deliver Power Efficiently. Circuit Also "Mode-Hops" Due to Transformer's Parasitic Resonances

though efficient totem drive devoid of simultaneous conduction requires care. Mode-hopping persists, in this case aggravated by the long acoustic transit time through the PZT and the wideband feedback. The sonic transit time produces enormous feedback phase error. Even worse, this phase error varies with line and load conditions. The alternate feedback scheme shown senses current, as opposed to voltage. This eliminates the voltage divider induced loading but does nothing to address the phase uncertainties and mode-hopping. A final problem, common to all resonant oscillators, concerns start-up. Gentle tapping of the PZT will usually start a reticent circuit but this is hardly reassuring.⁶ Figure 6 is similar but uses a ground-referred push-pull power stage, simplifying the drive scheme. This is a better approach but phase, mode-hopping and start-up problems are as before.

Figure 7 retains the drive scheme and solves the remaining problems. Central to circuit operation is a new transformer terminal labeled "feedback." This connection, precisely positioned on the transformer, provides constant-phase resonance information regardless of operating conditions.

Note 4: For examples, see References 4 through 11.

Note 5: See References 12 through 14.

Note 6: At the low voltage end, please!

Application Note 81

When power is applied, the RC oscillator drives Q1 and Q2 at a frequency outside resonance. The PZT, excited off-resonance, at first responds very inefficiently, although voltage-amplified resonant waveforms appear at the feedback and output terminals. The resonant information present at the feedback terminal injection-locks the RC oscillator, pulling it to the PZT's resonance. Now, the PZT is supplied with on-resonance drive and efficient operation commences.⁷ The feedback terminal's constant-phase characteristic is maintained over all line and load conditions, and the loop enforces resonance.

Figure 8, retaining the resonance loop, adds an amplitude control loop to stabilize lamp intensity. Lamp current is sensed and fed back to a voltage regulator to control PZT drive power. The regulator's reference point is variable, permitting lamp intensity to be set at any desired level. The amplitude and resonance loops operate simultaneously, although fully independent of each other. This two loop operation is the key to high power, wide range, reliable control.

Figure 9 is a detailed schematic of Figure 8's concept. The resonance loop is comprised of Q4 and the CMOS inverter based oscillator. The amplitude loop centers around the LT1375 switching regulator. Figure 10 shows waveforms. Traces A and B are Q2 and Q1 gate drives, respectively. Resultant Q1 and Q2 drain responses are traces C and D. The LT1375 step-down switching regulator, responding to the rectified and averaged lamp current, closes the amplitude loop by driving the L1-L2 junction (trace E). The 4.7 μ F capacitor at the V_C pin stabilizes the loop.⁸ Note that no filtering is used—the raw LT1375 500kHz PWM output directly drives the L1-L2-PZT network. This is permissible because the PZT Q factor is so high that it responds only at resonance (again, see traces C and D).

Note 7: This is the heart and soul of a bootstrapped start-up.

Note 8: This is a deceptively innocent sentence. The PZT's acoustic transport speed furnishes an almost pure delay in the loop, making compensation an interesting exercise. See Appendix C, "A Really Interesting Feedback Loop."

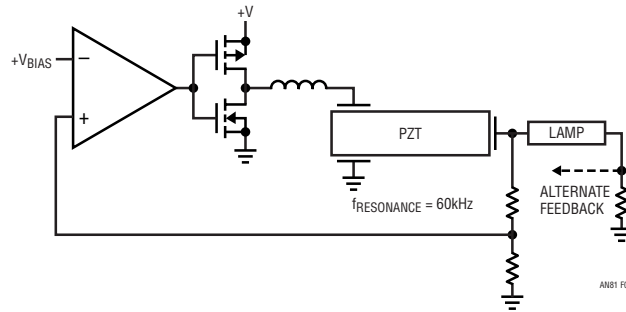


Figure 5. Feedback Based Oscillator Has More Efficient Drive Stage. Poorly Defined Transformer Phase Characteristics Cause Spurious Modes with Line and Load Variations

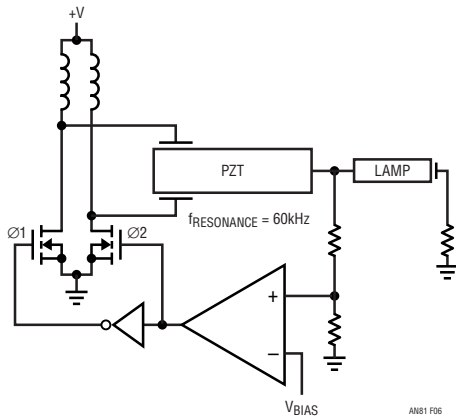


Figure 6. Push-Pull Version of Figure 5 Retains Efficiency While Permitting Simple All N-Channel Drive. Poor Phase Characteristics Still Preclude Stable Loop Operation

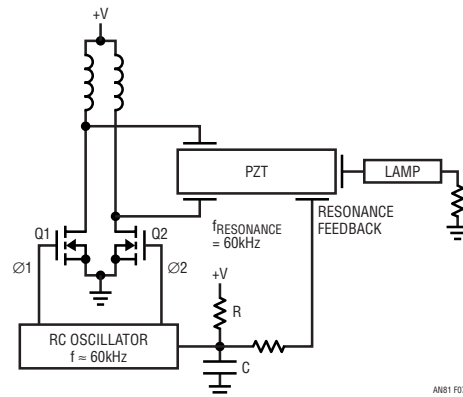


Figure 7. Feedback Tap On Transformer Synchronizes RC Oscillator, Providing Stable Phase Characteristics. Loop Maintains Fundamental Resonance Under All Conditions

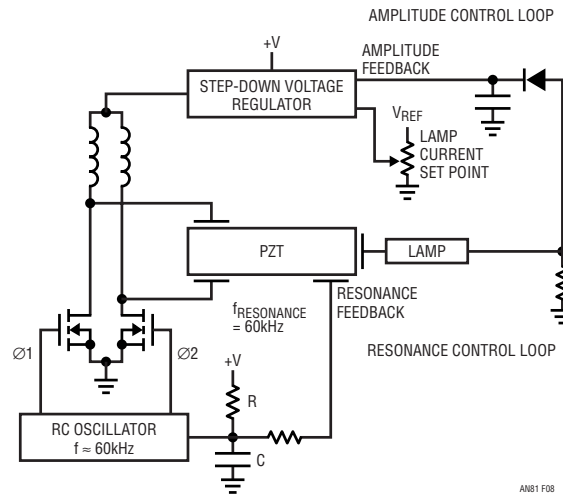


Figure 8. Previous Circuit with Amplitude Control Loop Added. New Circuitry Senses Lamp Current, Accordingly Controls PZT Drive Power. Resonance and Amplitude Control Loops Do Not Interact

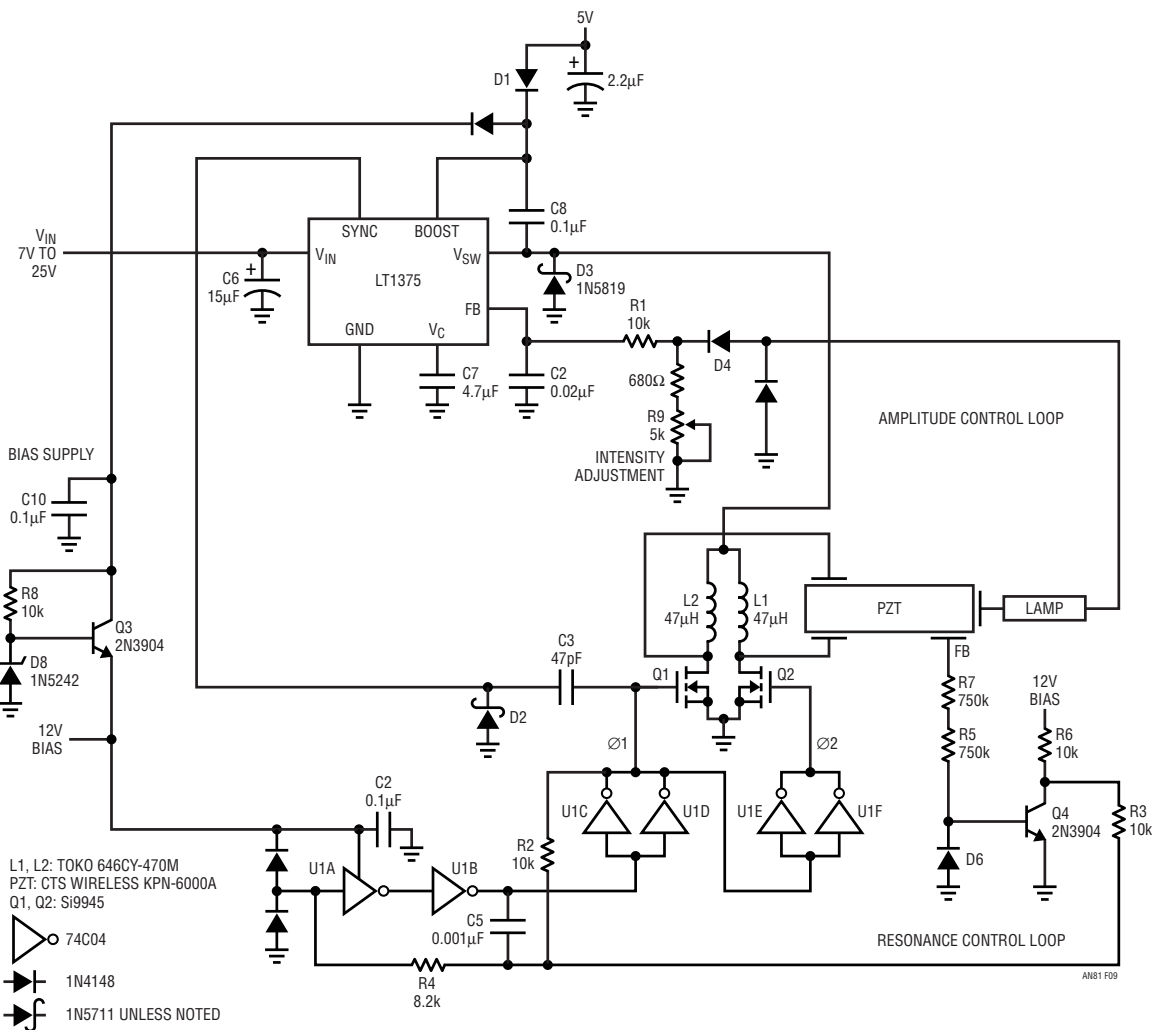


Figure 9. Complete Piezoceramic Transformer (PZT) Based Backlight Inverter. PZT's Resonant Feedback Synchronizes Inverter Based RC Oscillator Via Q4. Amplitude Control Loop Powers PZT Via LT1375 Switching Regulator

Application Note 81

The feedback tap (trace F), supplying phase coherent information, looks like a current source to Q4 under all conditions (note trace F's vertical scale factor). The 750k resistors in series minimize parasitic capacitance at the transformer feedback terminal. Q4's collector (trace G) clamps this information to a lower voltage and injection-locks the CMOS inverter based oscillator, closing the resonance loop. The oscillator insures start-up (refer to text associated with Figure 7) and effectively filters the already narrow band resonant feedback, further insuring resonance loop fidelity under all conditions. Trace H is the PZT's high voltage output delivered to the lamp.

In this example dimming is set with a potentiometer, although simple current summing to the LT1375 feedback pin allows electronic control.⁹

Additional Considerations and Benefits

As previously mentioned, the PZT has other benefits besides small size. One of these is safety. A PZT cannot fail due to output shorts or opens. Short circuits knock the PZT off-resonance and it simply stops, absorbing no energy. Open circuits do not cause arc-induced PZT failures because the PZT cannot "arc turns" like a magnetic transformer. However, it is always wise to sense and arrest an overvoltage condition. The PZT is capable of large outputs, despite its small size. Powered by a 10 volt supply, it can easily produce 3000V_{RMS} if uncontrolled. This mandates some form of overvoltage protection in a

Note 9: See Reference 1 for information on various dimming control schemes.

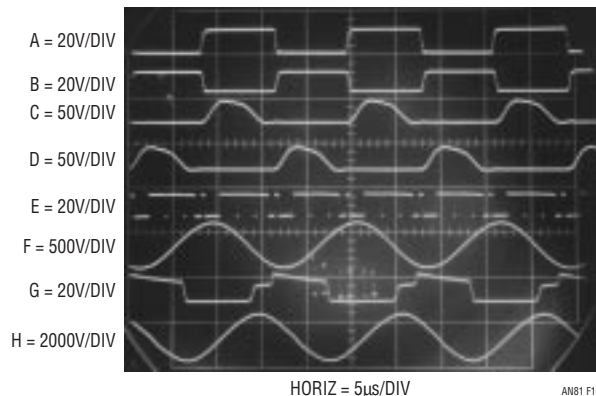


Figure 10. Waveforms for Figure 9. Traces A and B Are Q2 and Q1 Drive, Respectively. Resultant Q1 and Q2 Drain Responses Are Traces C and D. LT1375 V_{SW} Output Is Trace E. PZT Resonance Tap Is Trace F; Q4's Collector, Trace G. PZT High Voltage Output Is Trace H. PZT Acts As a Mechanical Filter, Producing Low Distortion Sine Waves

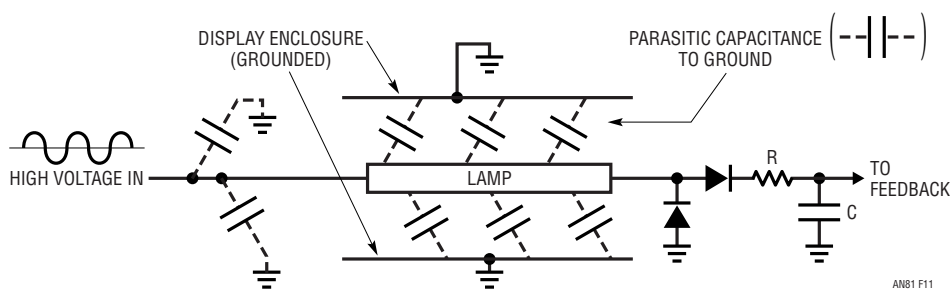


Figure 11. Parasitic Capacitance Absorbs Energy and Corrupts Drive Waveform Due to Finite Source Impedance vs Frequency in Magnetic Based Inverters. Differing Amounts of Capacitance with Various Displays Cause RC Averaging Errors, Necessitating Calibration for Each Display Type. PZT's Highly Resonant Characteristics Eliminate Calibration Requirement

production circuit. Another significant attribute is that amplitude control loop scale factor is almost completely independent of load, including parasitic capacitance. The practical advantage is that a wide range of displays may be used with no recalibration of any kind. This is in direct opposition to magnetically based inverters which require some form (either hardware or software based) of scale factor recalibration when displays are changed. Understanding why this is so requires some study.

Display Parasitic Capacitance and Its Effects

Almost all displays introduce some amount of parasitic capacitance between the lamp, its leads and electrically conductive elements within the display. Such elements may include the display enclosure, the lamp reflector or both. Figure 11 diagrams this situation. The parasitic capacitance to ground has two major impacts. It absorbs energy, causing lost power. This raises overall inverter input power because the inverter must supply both parasitic and intended load paths. Some techniques can minimize the effects of parasitic capacitance loss paths but they cannot be completely compensated.¹⁰

A second effect of parasitic capacitance, manifested in magnetically based inverters, is much more subtle. Magnetically based inverters have finite source impedance at frequency, corrupting the produced sinusoid. The amount of parasitic capacitance influences the degree of corruption. Different displays have varying amounts of parasitic capacitance, resulting in varying degrees of waveform distortion with different displays. The RC averaging time constant is *not* an RMS to DC converter and produces different outputs as distortion content in its input wave-

form changes. The amplitude loop acts on the DC output of the RC averager and the assumption is that the input waveform distortion content is constant. In a well designed magnetically based inverter this is essentially true, even as operating conditions vary. The averager's output error is consistent and can be "calibrated away" by scale factor adjustments. However, if the display type is changed, the averager is subjected to a differently distorted waveform and scale factor adjustments are required. This necessitates some form of calibration constant adjustment for each display type, complicating production and inventory requirements. PZT based inverters are largely immune to this problem because of their extraordinarily high Q factor, typically over 1000. The PZT forces the output waveform to have a consistent amount of distortion, nominally zero. The PZT's resonant mechanical filtering produces an almost pure sinusoidal output, even with widely varying parasitic and intended loads. Figure 12 shows PZT output voltage (trace A) and current (trace B) with a low parasitic loss display. Waveshapes are essentially ideal sinusoids. In Figure 13 a display with much higher parasitic losses has been substituted. Minor waveform distortion, particularly in the current trace (B), is evident, although minimal. The RC averager produces little error vs Figure 12 and less than 0.5% lamp current difference occurs between the two cases. In contrast, a magnetically based inverter can easily suffer 10% to 15% lamp current differences, impacting display luminosity and/or lamp lifetime.

Note 10: Complete treatment of this issue is sacrificed here to maintain focus. A more thorough investigation appears in Reference 1.

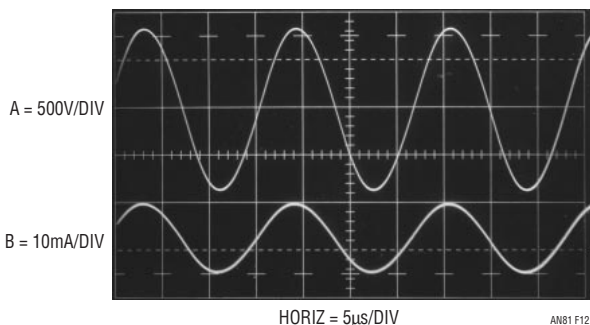


Figure 12. PZT Inverter Driving a Low Parasitic Capacitance Display. Trace A Is Lamp Voltage, Trace B Lamp Current. Waveforms Are Nearly Ideal Sinusoids

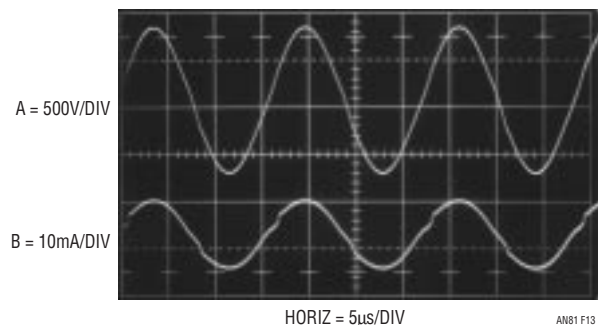


Figure 13. Display with Higher Capacitive Loss Causes Minor Distortion. Lamp RMS Current Varies Only 0.5% vs Figure 12.

Application Note 81

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APPENDIX A

PIEZOELECTRIC TRANSFORMERS “Good Vibrations”

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Piezoelectric transformers are, in fact, not transformers. There are no wires or magnetic fields. A better analogy would actually be that of a dynamo. The piezoelectric “transformer” works exactly like a motor mechanically coupled to a generator. In order to understand this concept, one must start by understanding the basics of piezoelectricity.

Piezowhat?

Many materials exhibit some form of piezoelectric effect. The ones most commonly used are Quartz, Lithium Niobate, and PZT or Lead Zirconate Titanate with the transformer using the latter. There are two piezoelectric effects, the direct effect and the inverse effect. In the case of the direct effect, placing a force or vibration (*stress*) on the piezoelectric element will result in the generation of a charge. (Figure A1) The polarity of this charge depends upon the orientation of the stress when compared to the direction of polarization in the piezoelectric element. The polarization direction, for PZT, is set by poling or applying a high D.C. field in the range of 45KV/cm to the element during the manufacturing process.

The inverse piezoelectric effect is, as the name implies, the opposite of the direct effect. (Figure 2) Applying an electric field (voltage) to the piezoelectric element results in a dimensional change. (*strain*) The direction of the change is likewise linked to the polarization direction. Fields applied at the same polarity of the element result in a

dimensional increase, while those of opposite polarity result in a decrease. It should be noted that an increase in one dimension in a structure would result in a decrease in the other two through Poisson’s coupling. This phenomenon is an important factor in the operation of the transformer.

The piezoelectric transformer uses both the direct and inverse effects in concert to create high voltage step-up ratios. (Figure 3) The input portion of the transformer is driven by a sine wave voltage, which causes it to vibrate. (*inverse effect-motor*) The vibration is coupled through the structure to the output, which results in the generation of an output voltage. (*direct effect-generator*)

Alchemy and Black Magic

The piezoelectric transformer is constructed of PZT ceramic, but more exactly, a multilayer ceramic. The manufacture of the transformer is similar to the manufacture of ceramic chip capacitors. Layers of flexible, unfired PZT ceramic tape are printed with metallic patterns and then aligned and stacked to form the required structure. The stacks are then pressed, diced and fired to create the final ceramic device.

The input section of the transformer has, in fact, a multilayer ceramic capacitor structure. (Figure 4) The metal electrodes are patterned in such a way as to create an interdigitated plate configuration. (*section A-A*) The output section of the transformer has no electrode plates between the ceramic layers and, as a result, fires into a single ceramic structure. The end of the output section is coated with a conductive material, which forms the output electrode for the transformer.

The next step in the construction is to establish the polarization directions in the two halves of the transformer. The input section of the transformer is poled across the inter-digitated electrodes resulting in a polarization direction aligned vertically to the thickness. The output section is poled to create a horizontal or length oriented polarization direction. During operation, the input is driven in thickness mode. This means that a voltage is applied between the parallel plates of the input causing it to become thicker and thinner on alternate halves of the

Application Note 81

sine wave. The change in input thickness couples through to the output section causing it to become longer and shorter, generating the output voltage. The resulting voltage step-up ratio is then proportional to the ratio of the output length, which generates the voltage, to the thickness of the input layers, across which the drive voltage is applied.

The Fun Part

The equivalent circuit model for the piezoelectric transformer outwardly looks identical to that of its series resonant magnetic counterpart. (Figure 5) The differences, however, extend past the nominal values to what the various components represent. The input and output capacitance are simply the result of having a dielectric between two metal plates. The effective dielectric constant of PZT runs between 400 and 5,000, depending upon composition. This, unfortunately, is where basic electronics end. The rest of the components are more complicated. The inductance, L_M , is actually the mass of the transformer. The capacitance, C_M , is the compliance of the material or the inverse of spring rate. The compliance is calculated from the applicable generalized beam equation and the Young's modulus. The resistor, R_M , represents the combination of dielectric loss and the mechanical Q of the transformer. It is already obvious to most that truly understanding this device requires background in electronics, mechanics and materials, but we're not quite done yet.

The resonant frequency is related to the product of the capacitance, C_M and inductance, L_M . This, however, represents the acoustic, not electrical, resonate frequency. The transformer is designed to operate in length resonance. The associated motions are identical to that of a vibrating string. The major difference is that the frequencies are in the ultrasonic range and vary, by design, between 50kHz and 2MHz. Like the string, the transformer has displacement nodes and anti-nodes. Mechanically clamping a node will prevent vibration. This will reduce

efficiency in the best case and prevent operation in the worst. Mounting the transformer is crucial. It can not be simply reflowed to a PCB.

The final element in the model is the "ideal" transformer with ratio N. This transformer actually represents three separate transformations. The first is the transformation of electrical energy into mechanical vibration. This is a function of the piezoelectric constant, which is electric field divided by stress, the stress area and the electric field length. The second transformation is the transfer of the mechanical energy from the input section to the output section and is a function of the Poisson's ratio for the material. The final transformation is the transfer of mechanical energy back into electrical energy. This is calculated in a similar fashion to the input side.

A Resonant Personality

Resonant magnetic high voltage transformers have an electrical Q of between 20 and 30. The equivalent for the piezoelectric transformer is its mechanical Q, which approaches 1,000. This is both good and bad. The ultimate efficiency can be higher, but the usable bandwidth of the transformer is only 2.5% of that of the magnetic. In addition, as shown earlier, the resonant frequency is dependent upon the compliance of the material, which, in turn, is a function of the Young's modulus. Piezoelectric materials have the unusual effect that Young's modulus changes with electrical load. In most, if not all, cases, the shift in resonant frequency over rated load is greater than the usable bandwidth. (Figure 6) The piezoelectric transformer must be run at resonance to maintain efficiency and stability. The near-resonance designs used with magnetic transformers work poorly, if at all with piezoelectrics. Tracking oscillators are a requirement.

Rosen¹ first proposed the concept of the piezoelectric transformer in 1956. It is now evident why it took 43 years to get it right.

Note 1: See Reference 4.

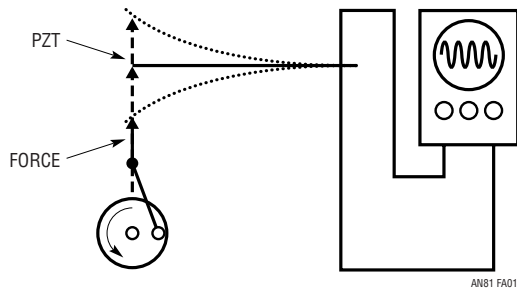


Figure 1. Direct Piezoelectric Effect: Force or Vibration Results in Output Voltage

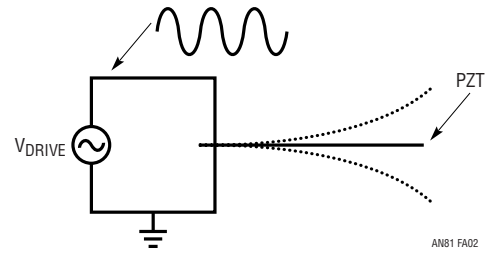


Figure 2. Inverse Piezoelectric Effect: Applied Voltage Results in Vibration or Movement

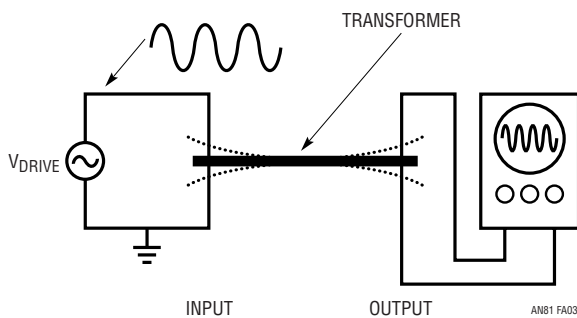


Figure 3. Transformer: Applied Voltage Results in Vibration Which Causes Output Voltage

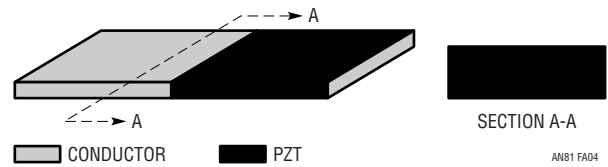


Figure 4. Piezoelectric Transformer: Multilayer PZT Construction

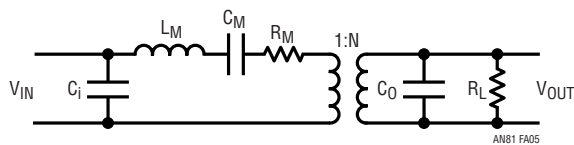


Figure 5. Piezoelectric Transformer: Equivalent Circuit Model

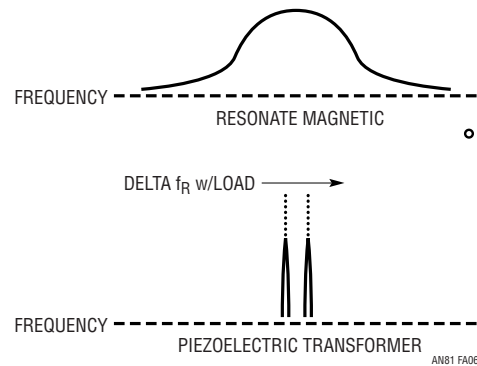


Figure 6. Transformer Bandwidth Comparison: Magnetic vs Piezoelectric

Application Note 81

APPENDIX B

PIEZOELECTRIC TECHNOLOGY PRIMER

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Piezoelectricity

The piezoelectric effect is a property that exists in many materials. The name is made up of two parts; piezo, which is derived from the Greek word for pressure, and electric from electricity. The rough translation is, therefore, pressure- electric effect. In a piezoelectric material, the application of a force or stress results in the development of a charge in the material. This is known as the direct piezoelectric effect. Conversely, the application of a charge to the same material will result in a change in mechanical dimensions or strain. This is known as the indirect piezoelectric effect.

Several ceramic materials have been described as exhibiting a piezoelectric effect. These include lead-zirconate-titanate (PZT), lead-titanate (PbTiO_2), lead-zirconate (PbZrO_3), and barium-titanate (BaTiO_3). These ceramics are not actually piezoelectric but rather exhibit a polarized electrostrictive effect. A material must be formed as a single crystal to be truly piezoelectric. Ceramic is a multi crystalline structure made up of large numbers of randomly orientated crystal grains. The random orientation of the grains results in a net cancelation of the effect. The ceramic must be polarized to align a majority of the individual grain effects. The term piezoelectric has become interchangeable with polarized electrostrictive effect in most literature.

Piezoelectric Effect

It is best to start with an understanding of common dielectric materials in order to understand the piezoelectric effect. The defining equations for high permittivity dielectrics are:

$$C = \frac{K\epsilon_r A}{t} = \frac{\epsilon_0 \epsilon_r A}{t} = \frac{\epsilon A}{t} \quad \text{and} \quad Q = CV \rightarrow Q = \frac{\epsilon AV}{t}$$

where:

C = Capacitance

A = Capacitor plate area

ϵ_r = Relative dielectric constant

ϵ_0 = Dielectric constant of air
= 8.85×10^{-12} farads/meter

ϵ = Dielectric constant

V = Voltage

t = Thickness or plate separation

Q = Charge

In addition, we can define electric displacement, D, as charge density or the ratio of charge to the area of the capacitor:

$$D = \frac{Q}{A} = \frac{\epsilon V}{t}$$

and further define the electric field as:

$$E = \frac{V}{t} \quad \text{or} \quad D = \epsilon E$$

These equations are true for all isotropic dielectrics. Piezoelectric ceramic materials are isotropic in the unpolarized state, but they become anisotropic in the poled state. In anisotropic materials, both the electric field and electric displacement must be represented as vectors with three dimensions in a fashion similar to the mechanical force vector. This is a direct result of the dependency of the

ratio of dielectric displacement, D , to electric field, E , upon the orientation of the capacitor plate to the crystal (or poled ceramic) axes. This means that the general equation for electric displacement can be written as a state variable equation:

$$D_i = \epsilon_{ij}E_j$$

The electric displacement is always parallel to the electric field, thus each electric displacement vector, D_i , is equal to the sum of the field vector, E_j , multiplied by its corresponding dielectric constant, ϵ_{ij} :

$$\begin{aligned} D_1 &= \epsilon_{11}E_1 + \epsilon_{12}E_2 + \epsilon_{13}E_3 \\ D_2 &= \epsilon_{21}E_1 + \epsilon_{22}E_2 + \epsilon_{23}E_3 \\ D_3 &= \epsilon_{31}E_1 + \epsilon_{32}E_2 + \epsilon_{33}E_3 \end{aligned}$$

Fortunately, the majority of the dielectric constants for piezoelectric ceramics (as opposed to single crystal piezoelectric materials) are zero. The only non-zero terms are:

$$\epsilon_{11} = \epsilon_{22}, \epsilon_{33}$$

Axis Nomenclature

The piezoelectric effect, as stated previously, relates mechanical effects to electrical effects. These effects, as shown above, are highly dependent upon their orientation to the poled axis. It is, therefore, essential to maintain a constant axis numbering scheme (Figure B1).

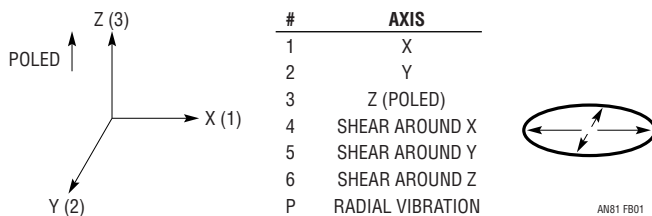


Figure B1

For electro-mechanical constants:

$$d_{ab}, a = \text{Electrical direction}; b = \text{Mechanical direction}$$

Electrical-Mechanical Analogies

Piezoelectric devices work as both electrical and mechanical elements. There are several electrical-mechanical analogies that are used in designing modeling the devices.

ELECTRICAL UNIT		MECHANICAL UNIT	
e	Voltage (Volts)	f	Force (Newtons)
i	Current (Amps)	v	Velocity (Meter/Second)
Q	Charge (Coulombs)	s	Displacement (Meters)
C	Capacitance (Farads)	C_M	Compliance (Meters/Newton)
L	Inductance (Henrys)	M	Mass (Kg)
Z	Impedance	Z_M	Mechanical Impedance

$$i = \frac{dQ}{dt}$$

$$v = \frac{ds}{dt}$$

$$e = L \frac{di}{dt} = L \frac{d^2Q}{dt^2}$$

$$f = M \frac{dv}{dt} = M \frac{d^2s}{dt^2}$$

Coupling

Coupling is a key constant used to evaluate the “quality” of an electro-mechanical material. This constant represents the efficiency of energy conversion from electrical to mechanical or mechanical to electrical.

$$k^2 = \frac{\text{Mechanical Energy Covered to Electrical Charge}}{\text{Mechanical Energy Input}}$$

or

$$k^2 = \frac{\text{Mechanical Energy Covered to Mechanical Displacement}}{\text{Electrical Energy Input}}$$

Electrical, Mechanical Property Changes with Load

Piezoelectric materials exhibit the somewhat unique effect that the dielectric constant varies with mechanical load and the Young’s modulus varies with electrical load.

Dielectric Constant:

$$\epsilon_r \text{ FREE} (1 - k^2) = \epsilon_r \text{ CLAMPED}$$

This means that the dielectric “constant” of the material reduces with mechanical load. Here “Free” stands for a state when the material is able to change dimensions with

Application Note 81

applied field. “Clamped” refers to either a condition where the material is physically clamped or is driven at a frequency high enough above mechanical resonance that the device can’t respond to the changing E field.

Elastic Modulus (Young’s Modules):

$$Y_{\text{OPEN}} (1 - k^2) = Y_{\text{SHORT}}$$

This means that the mechanical “stiffness” of the material reduces when the output is electrically shorted. This is important in that both the mechanical Q_M and resonate frequency will change with load. This is also the property that is used in the variable dampening applications.

Elasticity

All materials, regardless of their relative hardness, follow the fundamental law of elasticity (Figure B2). The elastic properties of the piezoelectric material control how well it will work in a particular application. The first concepts, which need to be defined, are stress and strain.

For any given bar of any material:

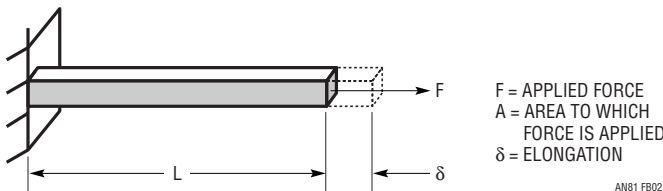


Figure B2

$$\text{Stress} = \sigma = F/A$$

$$\text{Strain} = \lambda = \delta/L$$

The relationship between stress and strain is Hooke’s Law which states that, within the elastic limits of the material, strain is proportional to stress.

$$\lambda = S\sigma$$

or, for an anisotropic material

$$\lambda_i = S_{ij}\sigma_j$$

Note: The constant relating stress and strain is the modulus of elasticity or Young’s modulus and is often represented by S, E or Y.

Piezoelectric Equation

It has been previously shown that when a voltage is applied across a capacitor made of normal dielectric material, a charge results on the plates or electrodes of the capacitor. Charge can also be produced on the electrodes of a capacitor made of a piezoelectric material by the application of stress. This is known as the Direct Piezoelectric Effect. Conversely, the application of a field to the material will result in strain. This is known as the Inverse Piezoelectric Effect. The equation, which defines this relationship, is the piezoelectric equation.

$$D_i = d_{ij}\sigma_j$$

where:

$D_i \equiv$ Electrical displacement (or charge density)

$d_{ij} \equiv$ Piezoelectric modulus, the ratio of strain to applied field or charge density to applied mechanical stress

Stated differently, d measures charge caused by a given force or deflection caused by a given voltage. We can, therefore, also use this to define the piezoelectric equation in terms of field and strain.

$$D_i = \frac{\sigma_j \lambda_i}{E_j}$$

Earlier, electric displacement was defined as

$$D_i = \epsilon_{ij} E_j$$

therefore,

$$\epsilon_{ij} E_j = d_{ij}\sigma$$

and

$$E_j = \frac{d_{ij}\sigma_j}{\epsilon_{ij}}$$

which results in a new constant

$$g_{ij} = \frac{d_{ij}}{\epsilon_{ij}}$$

This constant is known as the piezoelectric constant and is equal to the open circuit field developed per unit of applied stress or as the strain developed per unit of applied charge density or electric displacement. The constant can then be written as:

$$g = \frac{\text{field}}{\text{stress}} = \frac{\text{volts / meter}}{\text{newtons / meter}^2} = \frac{\Delta L / L}{\epsilon V / t}$$

Fortunately, many of the constants in the formulas above are equal to zero for PZT piezoelectric ceramics. The non-zero constants are:

$$s_{11} = s_{22}, s_{33}, s_{12}, s_{13} = s_{23}, s_{44}, s_{66} = 2(s_{11} - s_{12})$$

$$d_{31} = d_{32}, d_{33}, d_{15} = d_{24}$$

Basic Piezoelectric Modes

See Figure B3

Poling

Piezoelectric ceramic materials, as stated earlier, are not piezoelectric until the random ferroelectric domains are aligned. This alignment is accomplished through a process known as “poling”. Poling consists of inducing a D.C. voltage across the material. The ferroelectric domains align to the induced field resulting in a net piezoelectric effect. It should be noted that not all the domains become exactly aligned. Some of the domains only partially align and some do not align at all. The number of domains that align depends upon the poling voltage, temperature, and the time the voltage is held on the material. During poling the material permanently increases in dimension between the poling electrodes and decreases in dimensions parallel to the electrodes. The material can be de-poled by reversing the poling voltage, increasing the temperature beyond the materials Currie point, or by inducing a large mechanical stress.

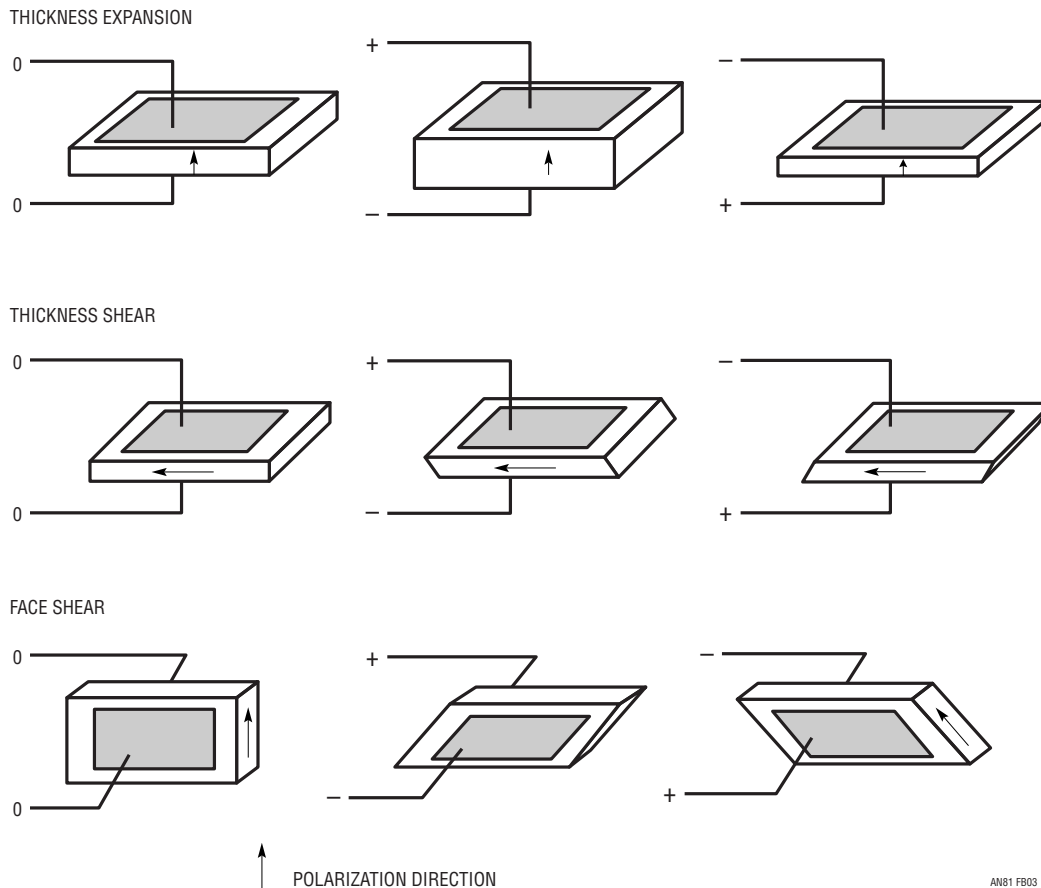


Figure B3

Application Note 81

Post Poling

Applied Voltage:

Voltage applied to the electrodes at the same polarity as the original poling voltage results in a further increase in dimension between the electrodes and decreases the dimensions parallel to the electrodes. Applying a voltage to the electrodes in an opposite direction decreases the dimension between the electrodes and increases the dimensions parallel to the electrodes.

Applied Force:

Applying a compressive force in the direction of poling (perpendicular to the poling electrodes) or a tensile force parallel to the poling direction results in a voltage generated on the electrodes which has the same polarity as the original poling voltage. A tensile force applied perpendicular to the electrodes or a compressive force applied parallel to the electrodes results in a voltage of opposite polarity.

Shear:

Removing the poling electrodes and applying a field perpendicular to the poling direction on a new set of electrodes will result in mechanical shear. Physically shearing the ceramic will produce a voltage on the new electrodes.

Piezoelectric Benders

Piezoelectric benders are often used to create actuators with large displacement capabilities (Figure B4). The bender works in a mode which is very similar to the action of a bimetallic spring. Two separate bars or wafers of piezoelectric material are metallized and poled in the thickness expansion mode. They are then assembled in a + - + - stack and mechanically bonded. In some cases, a thin membrane is placed between the two wafers. The outer electrodes are connected together and a field is applied between the inner and outer electrodes. The result is that for one wafer the field is in the same direction as the poling voltage while the other is opposite to the poling direction. This means that one wafer is increasing in thickness and decreasing in length while the other wafer is decreasing in thickness and increasing in length, resulting in a bending moment.

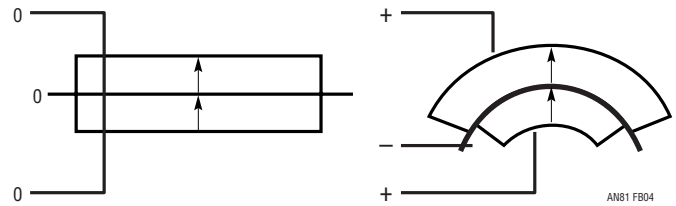


Figure B4

Loss

There are two sources for loss in a piezoelectric device. One is mechanical, the other is electrical.

$$\text{Mechanical Loss: } Q_M = \frac{\text{Mechanical Stiffness or Mass Resistance}}{\text{Mechanical Resistance}}$$

$$\text{Electrical Loss: } \tan\delta = \frac{\text{Effective Series Resistance}}{\text{Effective Series Reactance}}$$

Simplified Piezoelectric Element Equivalent Circuit

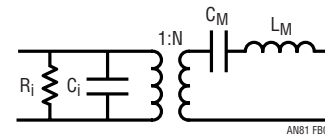


Figure B5

R_i = Electrical resistance

$$C_i = \text{Input capacitance} = \frac{\epsilon_0 \epsilon_r A}{t}$$

$\epsilon_0 = 8.85 \times 10^{-12}$ farads/meter

A = Electrode area

t = Dielectric thickness

L_M = Mass (Kg)

C_M = Mechanical compliance = 1/Spring Rate (M/N)

N = Electro-mechanical Linear Transducer Ratio (newtons/volts or coulomb/meter)

This model (Figure B5) has been simplified and it is missing several factors. It is only valid up to and slightly beyond resonance. The first major problem with the model is related to the mechanical compliance (C_M). Compliance is a function of mounting, shape, deformation mode (thickness, free bend, cantilever, etc.) and modulus of

elasticity. The modulus of elasticity is, however, anisotropic and it varies with electrical load. The second issue is that the resistance due to mechanical Q_M has been left out. Finally, there are many resonant modes in the transformers, each of which has its own C_M as shown in Figure B6.

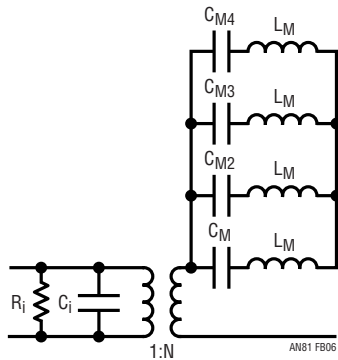


Figure B6

Mechanical Compliance:

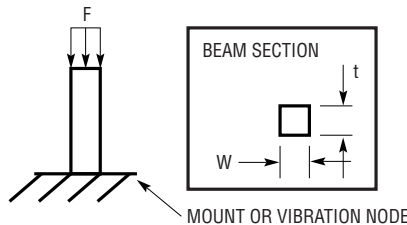
Mechanical compliance, which is the inverse of spring constant, is a function of the shape, mounting method, modulus and type of load. Some simple examples are shown in Figure B7.

The various elements that have been explained can now be combined into the design of a complete piezoelectric device. The simple piezoelectric stack transformer will be used to demonstrate the way they are combined to create a functional model.

Simple Stack Piezoelectric Transformer

The piezoelectric transformer acts as an ideal tool to explain the modeling of piezoelectric devices in that it utilizes both the direct and indirect piezoelectric effects. The transformer operates by first converting electrical energy into mechanical energy in one half of the transformer. This energy is in the form of a vibration at the acoustic resonance of the device. The mechanical energy

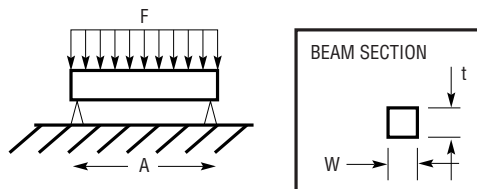
SIMPLE BEAM—UNIFORM END LOAD



$$C_M = \frac{A}{AY_{ij}} = \frac{A}{Wt}$$

$$L_M = \rho AWt$$

SIMPLE BEAM—UNIFORM LOAD—END MOUNTS



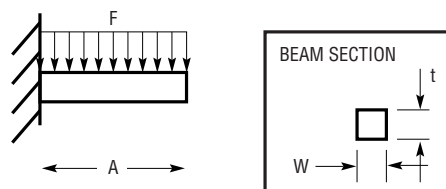
$$C_M = \frac{5A^3}{384Y_{ij}l}$$

$I = \text{MOMENT OF INERTIA}$

$$= \frac{Wt^3}{12}$$

$$C_M = \frac{5A^3}{32Wt^3}$$

SIMPLE BEAM—UNIFORM LOAD—CANTILEVER MOUNTS



$$C_M = \frac{A^3}{8Y_{ij}l}$$

$$= \frac{3A^3}{2Y_{ij}Wt^3}$$

AN81 FB07

Figure B7

Application Note 81

produced is then mechanically coupled into the second half of the transformer. The second half of the transformer then reconverts the mechanical energy into electrical energy. Figure B8 shows the basic layout of a stack transformer. The transformer is driven across the lower half (dimension d_1) resulting in a thickness mode vibration. This vibration is coupled into the upper half and the output voltage is taken across the thinner dimension d_2 .

Equivalent Circuit:

The equivalent circuit model for the transformer (shown in Figure B9) can be thought of as two piezoelectric elements that are assembled back to back. These devices are connected together by an ideal transformer representing the mechanical coupling between the upper and lower halves. The input resistance, R_i , and the output resistance, R_o , are generally very large and have been left out in this model. The resistor R_L represents the applied load. Determining the values of the various components can be calculated as shown previously.

Input/Output Capacitance:

$$C_i = \epsilon_0 \epsilon_r \frac{\text{Input Area}}{\text{Input Thickness}} = \epsilon_0 \epsilon_r \frac{AW}{d_1}$$

similarly,

$$C_o = \epsilon_0 \epsilon_r \frac{\text{Output Area}}{\text{Output Thickness}} = \epsilon_0 \epsilon_r \frac{nAW}{d_2}$$

Mechanical Compliance:

The mechanical compliance, C_M , can be represented by a simple beam subjected to a uniform axial load. This is because the thickness expansion mode will apply uniform stress across the surface. It should be noted that the beam length is measured with respect to the vibration node. The vibration node is used as this is the surface which does not move at resonance and can, therefore, be thought of as a fixed mounting surface.

$$C_M = \frac{\text{Beam Length}}{\text{Beam Area } Y_{33}}$$

$$C_{M1} = \frac{d_1}{AWY_{33}}$$

$$C_{M2} = \frac{d_2}{AWY_{33}}$$

Note: Even if $nd_2 \neq d_1$ the vibration node will still be located in the mechanical center of the transformer.

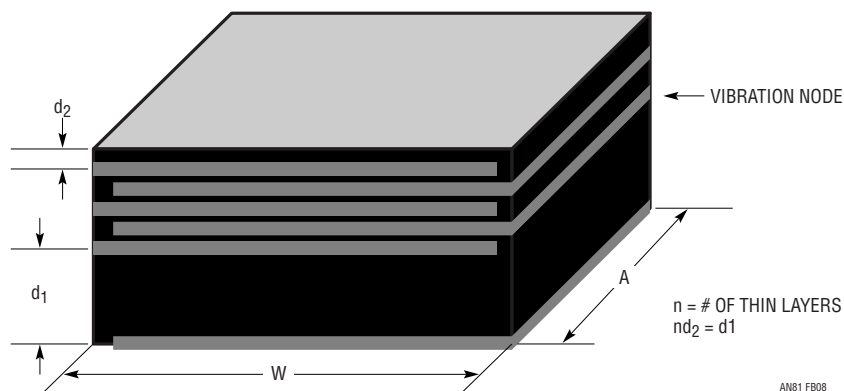


Figure B8

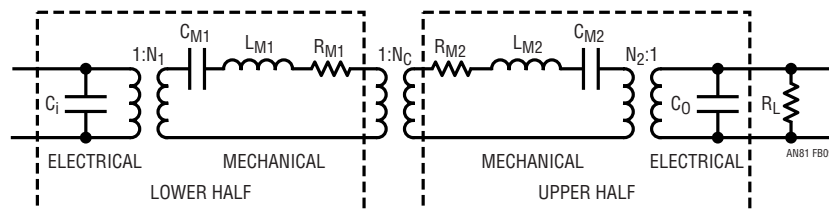


Figure B9

Mass:

$$L_{M1} = \rho A W d_1$$

$$L_{M2} = \rho A W d_2 = \rho A W d_1$$

Resistance:

The resistances in the model are a function of the mechanical Q_M and Q of the material at resonance and will be calculated later.

Ideal Transformer Ratio:

The transformer ratio, N_1 , can be thought of as the ratio of electrical energy input to the resulting mechanical energy output. This term will then take the form of newtons per volt and can be derived from the piezoelectric constant, g .

As before:

$$g = \text{Electrical Field Stress} = \frac{\text{Volts / Meter}}{\text{Newtons / Meter}^2}$$

therefore:

$$\frac{1}{g} = \frac{n / m}{V / m}$$

$$N_1 = \frac{1}{g} = \frac{\text{Area of Applied Force}}{\text{Length of Generated Field}}$$

or

$$N_1 = \frac{AW}{g_{33}d_1}$$

The output section converts mechanical energy back to electrical energy and the ratio would normally be calculated in an inverse fashion to N_1 . In the model, however, the transformer ratio is shown as $N_2 : 1$. This results in a calculation for N_2 that is identical to the calculation of N_1 .

$$N_2 = \frac{1}{g} = \frac{\text{Area of Applied Force}}{\text{Length of Generated Field}}$$

or

$$N_2 = \frac{AW}{g_{33}d_2}$$

The transformer $1 : N_C$, represents the mechanical coupling between the two halves of the transformer. The stack transformer is tightly coupled and the directions of stress are the same in both halves. This results in $N_C \cong 1$.

Model Simplification:

The response of the transformer can be calculated from this model, but it is possible to simplify the model through a series of simple network conversion and end up in an equivalent circuit whose form is the same as that of a standard magnetic transformer (Figure B10).

where, due to translation through the transformer,

$$C_{M2}' = N_C^2 C_{M2} \quad \text{and} \quad L_{M2}' = L_{M2} / N_C^2$$

but $N_C^2 \cong 1$, therefore

$$C_{M2}' = C_{M2} = C_{M1} \quad \text{and} \quad L_{M2}' = L_{M2} = L_{M1}$$

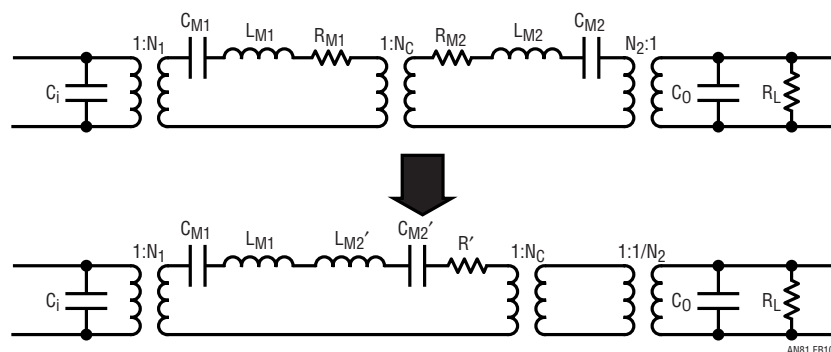


Figure B10

Application Note 81

which allows the next level of simplification (Figure B11)

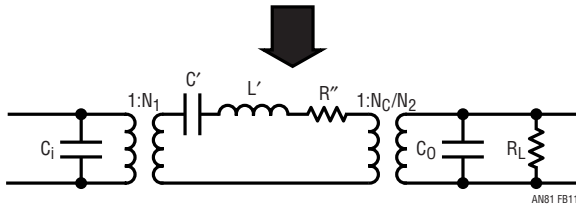


Figure B11

here

$$L' = L_{M1} + L_{M2}' = 2L_1 = 2\rho AWd_1$$

$$C' = \frac{\left(\frac{C_{M1}C_{M2}'}{C_{M1} + C_{M2}'} \right)}{\left(\frac{C_{M1}^2}{2C_{M1}} \right)} = \frac{C_{M1}^2}{2} = \frac{C_{M1}}{2} = \frac{d_1}{2AWY_{33}}$$

Final simplification (Figure B12)

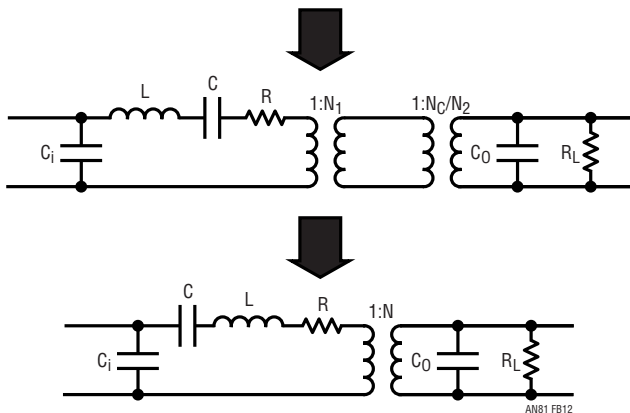


Figure B12

where

$$C = C'N_1^2 \text{ and } L = L'/N_1^2$$

and, from before

$$N_1 = \frac{AW}{g_{33}d_1}$$

therefore

$$C = \frac{d_1}{2WLY_{33}} \frac{A^2W^2}{g_{33}^2 d_1^2} = \frac{AW}{2Y_{33}g_{33}^2 d_1}$$

$$L = 2\rho AWd_1 \frac{g_{33}^2 d_1^2}{A^2W^2} = \frac{2\rho g_{33}^2 d_1^2}{AW}$$

$$N = \frac{N_1 N_C}{N_2} = \frac{AW}{g_{33}d_1} \frac{g_{33}d_2}{AW} = \frac{d_2}{d_1}$$

The last value we need to calculate is the motional resistance. This value is based upon the mechanical QM of the material and the acoustic resonant frequency.

Resonant Frequency

$$\omega_0 = 1/\sqrt{LC}$$

$$= \frac{1}{\sqrt{\frac{2\rho d_1 g_{33}^2}{AW} \frac{AW}{2Y_{33}g_{33}^2 d_1}}}$$

$$= \frac{1}{\sqrt{\frac{\rho d_1^2}{Y_{33}}}} = \frac{1}{d_1 \sqrt{\frac{\rho}{Y_{33}}}}$$

$$c_{PZT} \equiv \text{Speed of Sound in PZT} = \sqrt{Y/\rho}$$

therefore

$$\omega_0 = c_{PZT}/d_1$$

The equation above states that the resonant frequency is equal to the speed of sound in the material divided by the acoustic length of the device. This is the definition of acoustic resonance and acts as a good check of the model. The final derivation is the value of resistance.

$$Q_M \equiv 1/\omega_0 RC$$

or

$$R = 1 / \omega_0 Q_M C$$

$$R = \frac{d_1 \sqrt{\rho Y_{33}}}{Q_M} \frac{2 Y_{33} g_{33}^2 d_1}{AW}$$

$$= \frac{2 d_1^2 g_{33}^2 \sqrt{\rho Y_{33}}}{Q_M AW}$$

Note: C_M and R are both functions of Y_{33} and Y_{33} is a function of R_L

It should be noted that the model is only valid for transformers driven at or near their fundamental resonate frequencies. This is because the initial mechanical model assumed a single vibration node located at the center of the stack which is only true when the transformer is driven at fundamental resonance. There are more nodes when the transformer is driven at harmonic frequencies (Figure B13).

There are no fixed nodes at frequencies other than resonance. This means that the transformer must be designed with the resonate mode in mind or phase cancellations will occur and there will be little or no voltage gain. It is often difficult to understand the concept of nodes and phase cancellation, so a simple analogy can be used. In this case, waves created in a waterbed will be used to explain the effect.

Pressing on the end of a waterbed creates a “wave” of displacement that travels down the length of the bed until it reaches the opposite end and bounces back. The water pressure (stress) is the lowest, or negative with respect to the water at rest, at a point just in front of the wave and highest at a point just behind the wave. The pressures at the crest and in the trough are at the same pressure as the bed at rest. The wave will reflect back and forth until resistance to flow causes it to dampen out. The average pressure over time at any point in the bed will be exactly the same as the pressure at rest. Similarly, the average stress in a transformer off resonance will approach zero and there will be no net output.

Pressing on the end of the same bed repeatedly just after the wave has traveled down the length, reflected off the end, returned and reflected off the “driven” end will result in a standing wave. This means that one half of the bed is getting thicker as the other half is getting thinner and the center of the bed will be stationary. The center is the node and the thickness plotted over time of either end will form a sine wave. There will be no net pressure difference in the center, but the ends will have a pressure wave which form a sine wave 90° out of phase with the displacement. The transformer again works in the same manner with no voltage at the node and an AC voltage at the ends. It is fairly simple to expand this concept to harmonics and to other resonate shapes.

Conclusion

The number of different applications for piezoelectric ceramic, and in particular PZT ceramic, is too great to address in a single paper. The basic principals that have been set forth in this primer can, however, be used to both understand and design piezoelectric structures and devices. The ability to create devices of varying applications and shapes is greatly enhanced by the used of multilayer PZT ceramics.

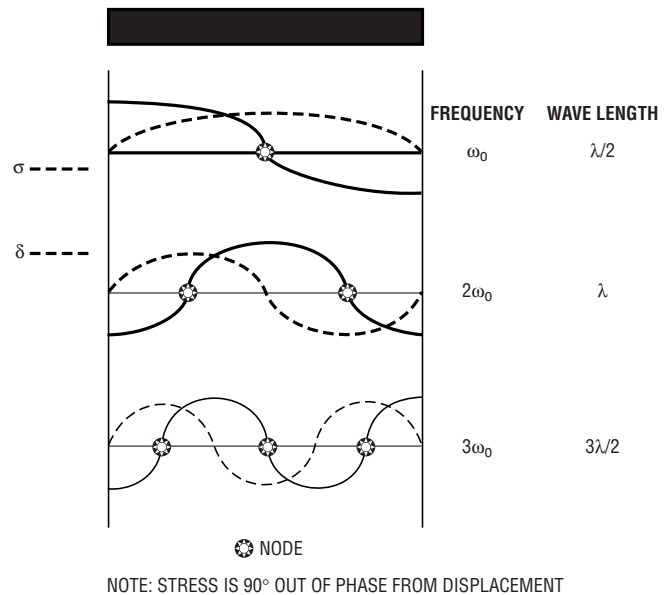


Figure B13

APPENDIX C

A Really Interesting Feedback Loop

The almost pure mechanical delay presented by the PZT's acoustic transport presents a fascinating exercise in loop compensation.¹ Veterans of feedback loop compensation battles will exercise immediate caution when confronted with a pure and lengthy delay in a loop. Neophyte designers will gain a lesson they will not easily forget.

Figure C1 diagrams Figure 9's amplitude control loop, with significant contributions to loop transmission represented. The PZT delivers phase delayed information at about 60kHz to the lamp. This information is smoothed to DC by the RC averaging time constant and delivered to the LT1375's feedback terminal. The LT1375 controls PZT power with its 500kHz PWM output, closing the control loop. The capacitor at the LT1375's V_C pin rolls off gain, nominally stabilizing the loop. This compensation capacitor must roll off gain-bandwidth at a low enough value to prevent loop delays from causing oscillation. Which of these delays is the most significant? From a stability viewpoint, the LT1375's output repetition rate and the PZT's oscillation frequency are sampled data systems. Their information delivery rate is far above the PZT's 200 μ s delay and the averaging time constants, and is not significant. The PZT delay and the RC time constant are the major contributors to loop delay. The RC time constant must be large enough to turn the half wave rectified waveform into DC. The lumped delay of the PZT and the RC thus dominates loop transmission. It must be compensated by the capacitor at the LT1375 V_C pin. A large enough value for this capacitor rolls off loop gain at low enough frequency to provide stability. The loop simply does not have enough gain to oscillate at a frequency commensurate with the RC and PZT delays.²

A good way to begin to establish a value for loop roll-off is to let the loop oscillate. This is facilitated by initially deleting the compensation capacitor and turning the circuit on. Figure C2 shows the V_C pin (trace A) and FB node (trace B). The frequency of oscillation and the phase relationship between these two signals provide valuable insight into achievable closed-loop bandwidth.³ Loop delay sets oscillation frequency at about 2.3kHz. Selecting

the V_C value to roll off bandwidth well below this frequency is appropriate. Figure C3 shows results with Figure 9's 4.7 μ F capacitor installed. Trace A, a step input, is applied to the LT1375's shutdown pin. When the shutdown pin is enabled, V_C (trace B) slews up and the feedback pin (trace C) moves toward its control point as PZT output voltage (trace D) rises. The V_C pin damping causes extended slew time but settling is completed in 25 milliseconds with minimal overshoot. The small overshoot (past mid screen) derives from the lamp's negative resistance characteristic and is easily handled by loop dynamics.

Some situations may require significantly faster loop response than simple first order compensation can provide. An example is wide range dimming via PWM methods. Such methods rely on rapid on-off loop cycling to achieve wide range dimming. Typically, the cycling occurs well above the flicker rate, in the 100Hz to 200Hz region. Loop settling must be very quick with respect to this frequency or line regulation will be poor. This is so because during slew the loop is out of control. If slew time approaches on-time, control is, by definition, poor. Figure C4 uses a feedback lead, allowing very light V_C damping with resultant faster slew time.⁴ Figure C5 shows results. When the shutdown pin (trace A) is enabled, V_C (trace B) slews rapidly, followed by the FB node (trace C). The PZT high voltage envelope is trace D. Loop capture occurs in 1.2 milliseconds—about 20x faster than Figure C3's simple first order compensation. Note that this performance begins to approach the limits implied by Figure C2's information.⁵

Note 1: Perhaps this verbiage indulges drama. Conversely, nerds like me find arcana such as this fascinating.

Note 2: The high priests of feedback refer to this as "Dominant Pole Compensation." The rest of us are reduced to more pedestrian descriptors. As such, this technique is sometimes loosely referred to as "glop comp."

Note 3: Deliberately sustaining loop oscillation is a valuable investigative tool but may encounter problems in some applications. Consider aircraft flap control servos or power plant generator stabilizing loops.

Note 4: Proper Bode for this compensation technique is a "feedback zero."

Note 5: Score one for lightning empiricism.

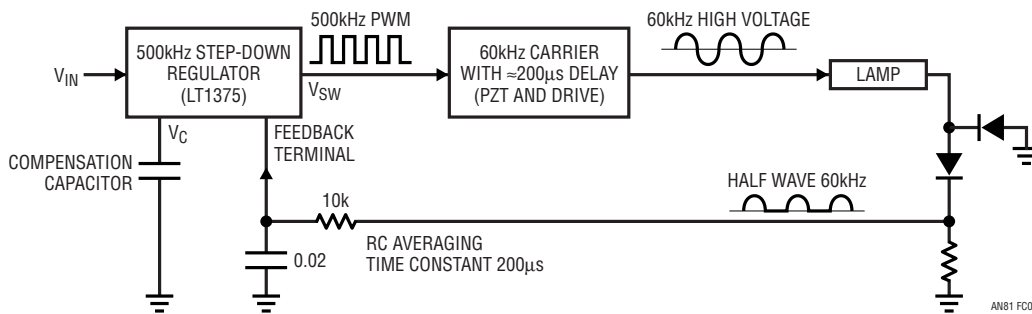


Figure C1. Delay Terms in Figure 9's Amplitude Control Feedback Path. PZT's 200µs Mechanical Delay and RC Time Constant Dominate Loop Transmission and Must Be Compensated for Stable Operation

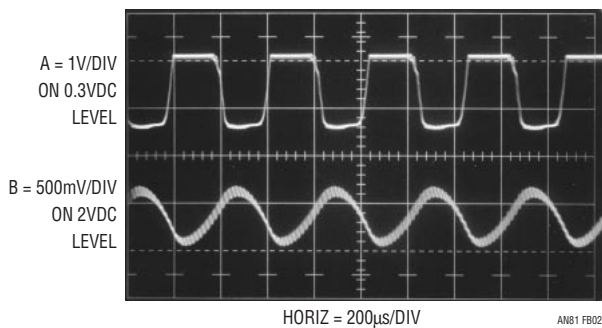


Figure C2. Allowing Loop to Oscillate Hints at Compensation Requirements. 2.3kHz Oscillation Frequency Appears to Derive from Figure C1's Delay Terms. Trace A Is LT1375 V_C Pin, Trace B Its Feedback Terminal. High Frequency Content in Trace B's Outline, PZT Carrier Residue, Is Not Pertinent

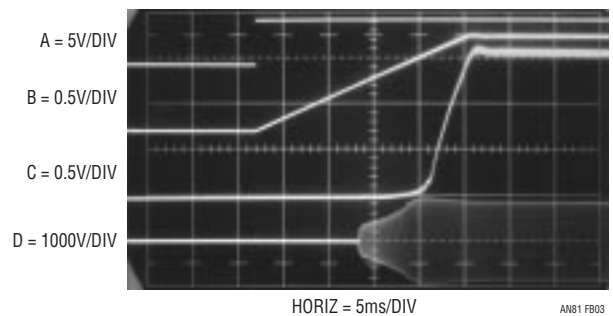


Figure C3. Figure 9's Loop Compensation Is Stable Despite PZT's Mechanically Induced Delay. First Order Roll-Off from Large V_C Pin Capacitor Stabilizes Loop. Trace A Is Step Input at LT1375 Shutdown Pin. Traces B, C and D are V_C , Feedback and PZT Output Nodes, Respectively

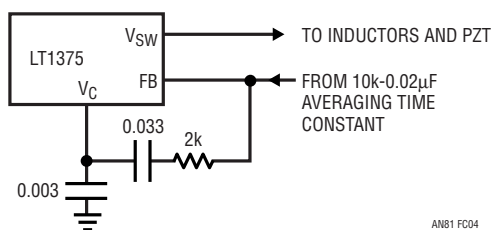


Figure C4. Very Light V_C Damping Augmented by a Feedback Lead Provides 20× Faster Loop Response. Technique Allows Wide Range Lamp Dimming Via PWM without Sacrificing Line Regulation

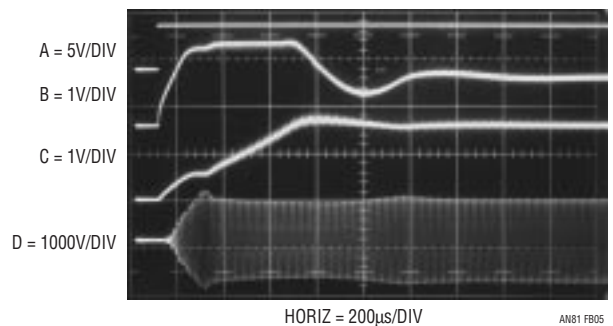
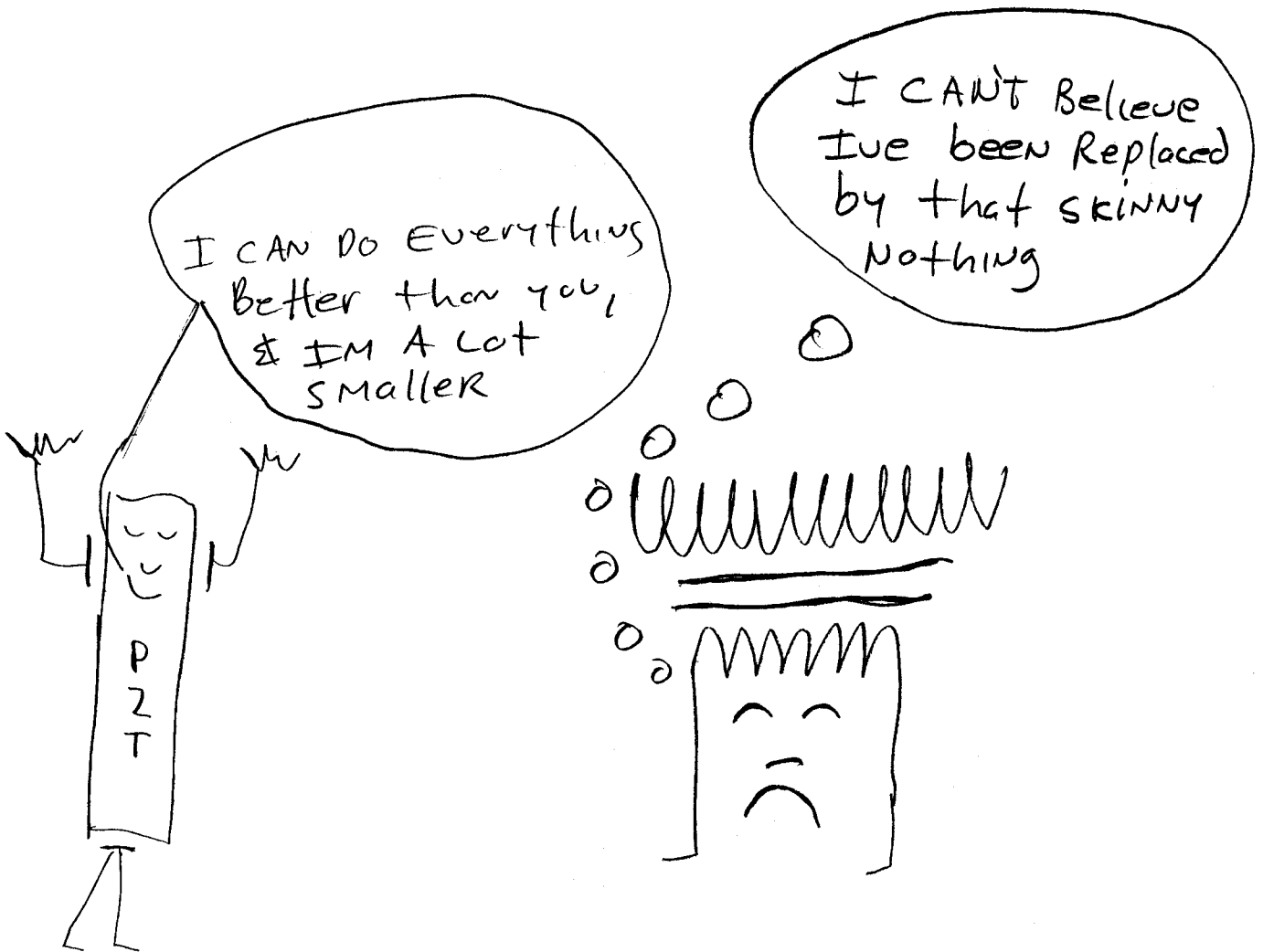


Figure C5. Feedback Based Compensation Waveforms. Trace A Is Step Input at LT1375 Shutdown Pin. Traces B, C and D Are V_C , Feedback and PZT Output Nodes, Respectively. Note 25× Sweep Speed Increase Over Figure C3



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Performance Verification of Low Noise, Low Dropout Regulators

Silence of the Amps

Jim Williams and Todd Owen, Linear Technology Corporation

Introduction

In an increasing trend, telecommunications, networking, audio and instrumentation require low noise power supplies. In particular, there is interest in low noise, low dropout linear regulators (LDO). These components power noise-sensitive circuitry, circuitry that contains noise-sensitive elements or both. Additionally, to conserve power, particularly in battery driven apparatus such as cellular telephones, the regulators must operate with low input-to-output voltages.¹ Devices presently becoming available meet these requirements (see separate section, "A Family of $20\mu\text{V}_{\text{RMS}}$ Noise, Low Dropout Regulators").

Noise and Noise Testing

Establishing and specifying LDO dropout performance is relatively easy to do. Verifying that a regulator meets dropout specification is similarly straightforward. Accomplishing the same missions for noise and noise testing is considerably more involved. The noise bandwidth of interest must be called out, along with operating conditions. Operating conditions can include regulator input and output voltage, load, assorted discrete components, etc. Low noise performance is effected by numerous subtleties; changes in operating conditions can cause unwelcome surprises.² Because of this, LDO noise must be quoted under specified operating and bandwidth conditions to be meaningful. Failure to observe this precaution will result in misleading data and erroneous conclusions.

Noise Testing Considerations

What noise bandwidth is of interest and why is it interesting? In most systems, the range of 10Hz to 100kHz is the information signal processing area of concern. Additionally, linear regulators produce little noise energy outside this region.³ These considerations suggest a measure-

ment bandpass of 10Hz to 100kHz, with steep slopes at the band limits. Figure 1 shows a conceptual filter for LDO noise testing. The Butterworth sections are the key to steep slopes and flatness in the passband. The small input level requires 60dB of low noise gain to provide adequate signal for the Butterworth filters. Figure 2 details the filter scheme. The regulator under test is at the diagram's center.⁴ A1-A3 make up a 60dB gain highpass section. A1 and A2, extremely low noise devices ($<1\text{nV}/\sqrt{\text{Hz}}$), comprise a 60dB gain stage with a 5Hz highpass input. A3 provides a 10Hz, 2nd order Butterworth highpass characteristic. The LTC[®]1562 filter block is arranged as a 4th order Butterworth lowpass. Its output is delivered via the $330\mu\text{F}$ - 100Ω highpass network. The circuit's output drives a thermally responding RMS voltmeter.⁵ Note that all circuit power is furnished by batteries, precluding ground loops from corrupting the measurement.

Instrumentation Performance Verification

Good measurement technique dictates verifying the noise test instrumentation's performance. Figure 3's spectral plot of the filter section shows essentially flat response in the 10Hz to 100kHz passband with abrupt slopes at the band extremes. Figure 4, expanding the vertical scale to


Note 1: See Appendix A, "Architecture of a Low Noise LDO," for design considerations of these devices.

Note 2: See Appendix D, "Practical Considerations for Selecting a Low Noise LDO."

Note 3: Switching regulators are an entirely different proposition, requiring very broadband noise measurement. See Reference 1.

Note 4: Component choice for the regulator, more critical than might be supposed, is discussed in Appendix B, "Capacitor Selection Considerations."

Note 5: The choice of RMS voltmeter is absolutely crucial to obtain meaningful measurements. See Appendix C, "Understanding and Selecting RMS Voltmeters."

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Application Note 83

A FAMILY OF 20 μ V_{RMS} NOISE, LOW DROPOUT REGULATORS

Telecom and instrumentation applications often require a low noise voltage regulator. Frequently this requirement coincides with the need for low regulator dropout and small quiescent current. A recently introduced family of devices addresses this problem. Figure A shows a variety of packages, power ranges and features in three basic regulator types. The SOT-23 packaged LT[®]1761 has only 20 μ V_{RMS} noise with 300mV dropout at 100mA. Quiescent current is only 20 μ A.

Applying the Regulators

Applying the regulators is simple. Figure B shows a minimum parts count, 3.3V output design. This circuit appears similar to conventional approaches with a notable exception: a bypass pin (BYP) is returned to the output via a 0.01 μ F capacitor. This path filters the internal reference's output, minimizing regulator output noise. It is the key to the 20 μ V_{RMS} noise performance. A shutdown pin (SHDN), when pulled low, turns off the regulator output while keeping current drain inside 1 μ A. Dropout characteristics appear in Figure C. Dropout scales with output current, falling to less than 100mV at low currents.

These devices provide the lowest available output noise in a low dropout regulator without compromising other parameters. Their performance, ease of use and versatility allow use in a variety of noise-sensitive applications.

REGULATOR TYPE	OUTPUT CURRENT	RMS NOISE (10Hz to 100kHz) C _{BYP} = 0.01 μ F	PACKAGE OPTIONS	FEATURES	QUIESCENT CURRENT	SHUTDOWN CURRENT
LT1761	100mA	20 μ V _{RMS}	SOT23-5	Shutdown, Reference Bypass, Adjustable Output; SOT23 Package Mandates Selecting Any Two Features	20 μ A	<1 μ A
LT1762	150mA	20 μ V _{RMS}	MSOP-8	Shutdown, Reference Bypass, Adjustable Output	25 μ A	<1 μ A
LT1962	300mA	20 μ V _{RMS}	MSOP-8	Shutdown, Reference Bypass, Adjustable Output	30 μ A	<1 μ A
LT1763	500mA	20 μ V _{RMS}	SO-8	Shutdown, Reference Bypass, Adjustable Output	30 μ A	<1 μ A
LT1963	1.5A	40 μ V _{RMS}	SO-8, SOT223-3, DD-5, TO220	Shutdown, Adjustable Output, Fast Transient Response	1mA	<1 μ A
LT1764	3A	40 μ V _{RMS}	DD-5, TO220	Shutdown, Adjustable Output, Fast Transient Response	1mA	<1 μ A

Figure A. Low Noise LDO Family Short-Form Specifications. Quiescent Current Scales with Output Current Capability, Although Noise Performance Remains Nearly Constant

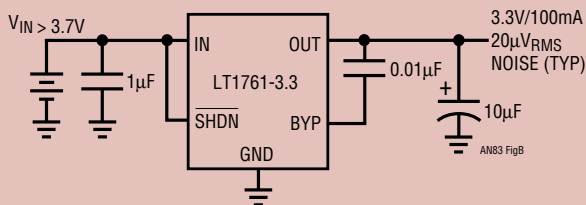


Figure B. Applying the Low Noise, Low Dropout, Micropower Regulator. Bypass Pin and Associated Capacitor are Key to Low Noise Performance

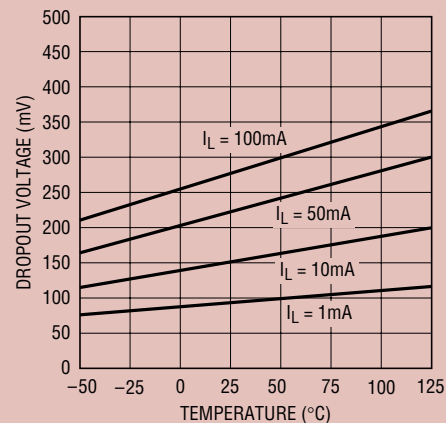


Figure C. Figure B's Dropout Voltage at Various Currents

1dB/division, reveals some flatness deviation but well within 1dB throughout nearly the entire passband. Grounding the filter's input determines the tester's noise floor. Figure 5 shows less than $4\mu\text{V}_{\text{P-P}}$, corresponding to a $0.5\mu\text{V}_{\text{RMS}}$ voltmeter reading. This is only about 0.5% of full scale ($100\mu\text{V}_{\text{RMS}}$), contributing negligible error. These results assure the confidence necessary to proceed with regulator noise measurement.

Regulator Noise Measurement

Regulator noise measurement begins with attention to test setup details. The extremely low signal levels require attention to shielding, cable management, layout and component choice.⁶ Figure 6a is the bench arrangement. The photo shows the completely shielded environment required to obtain faithful noise measurements. The metal can⁷ encloses the regulator under test and its internal battery power supply. A BNC fitting (photo lower center) connects the regulator output to the noise filter test circuit (black box). Note that the monitoring oscilloscope and voltmeter are not simultaneously connected to the output, precluding ground loops which would corrupt the measurement.

Figure 6b details the regulator enclosure with its cover removed. The battery supply is visible; the regulator occupies the can center. The BNC fitting connecting the noise filter box (lower left) eliminates triboelectric disturbances a cable might contribute.

Figure 6c is the noise test circuit box. Functions are as labeled in the photo. The two capped BNC connectors (box lower) are unused box entries.

Figure 7's oscilloscope photo shows an LT1761 regulator's noise measured at the filter output. Monitoring this point with the RMS voltmeter shows a $20\mu\text{V}_{\text{RMS}}$ reading. Figure 8's spectral plot of this noise indicates diminished power above 1kHz, in accordance with expected regulator noise density. Figure 9 shows more complete spectral noise density data for three regulator types. Noise power decays uniformly with increasing frequency, although the three regulators show some dispersion below 200Hz.

Bypass Capacitor (C_{BYP}) Influence

The regulator's internal voltage reference contributes most of the device's noise. The reference bypass capacitor filters reference noise, precluding it from appearing, in amplified form, at the output.⁸ Figure 10 is a study of regulator noise vs various values of C_{BYP} . 10a shows substantial noise for $C_{\text{BYP}} = 0\mu\text{F}$, while 10d displays nearly 9× improvement with $C_{\text{BYP}} = 0.01\mu\text{F}$; intermediate values of C_{BYP} (10b and 10c) produce commensurate results.

Interpreting Comparative Results

Figure 11's photos compare an LT1761-5's output noise (11d) with three other regulators (11a, 11b and 11c). These three devices are manufacturer specified for low noise performance, but the photos do not indicate this. The seeming contradiction is probably due to ambiguity in testing methods or specifications. For example, inappropriate choice of test equipment (see Appendix C) or measurement bandwidth can easily cause huge (5×) errors. This uncertainty mandates the noise testing described to insure realistic conclusions.

Note 6: Capacitor choice is discussed in Appendix B, "Capacitor Selection Considerations."

Note 7: The cookies were excellent, particularly the thin ones with sugar on top.

Note 8: See Appendix A, "Architecture of a Low Noise LDO," for details.

Application Note 83

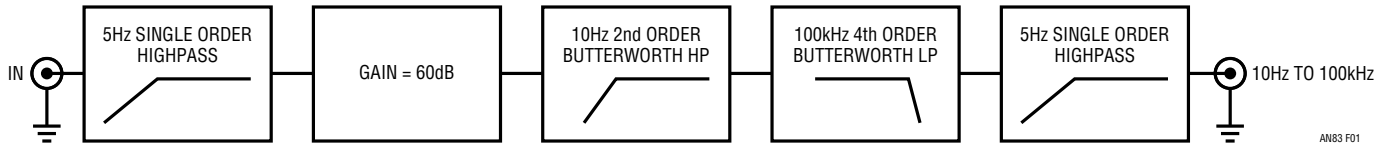
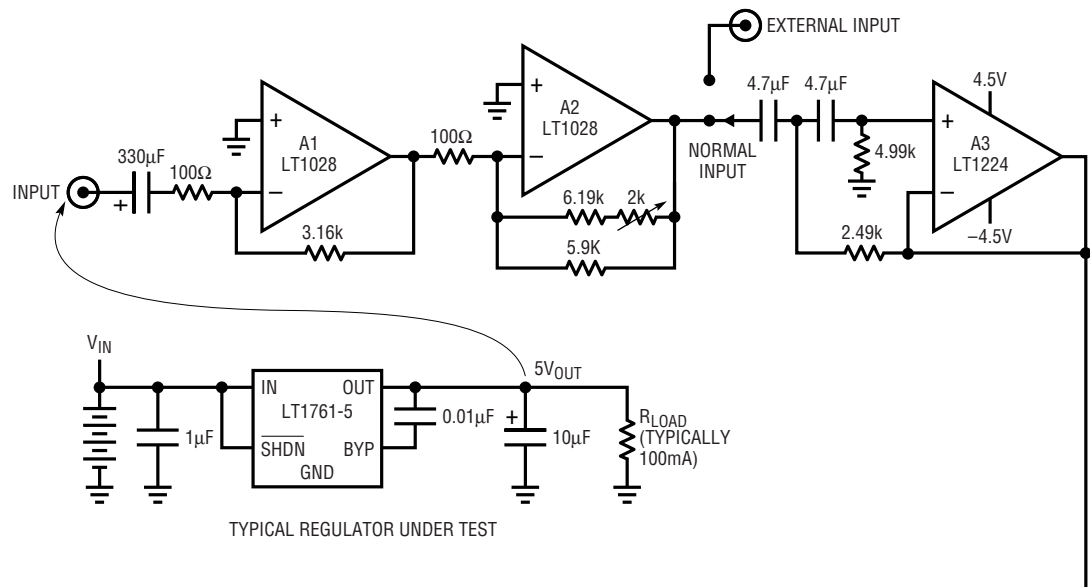


Figure 1. Filter Structure for Noise Testing LDOs. Butterworth Sections Provide Appropriate Response in Desired Frequency Range



ALL RESISTORS 1% METAL FILM
 4.7 μ F CAPACITORS = MYLAR, WIMA MKS-2
 330 μ F CAPACITORS = SANYO OSCON
 \pm 4.5V DERIVED FROM 6AA CELLS
 POWER REGULATOR FROM APPROPRIATE
 NUMBER OF D SIZE BATTERIES

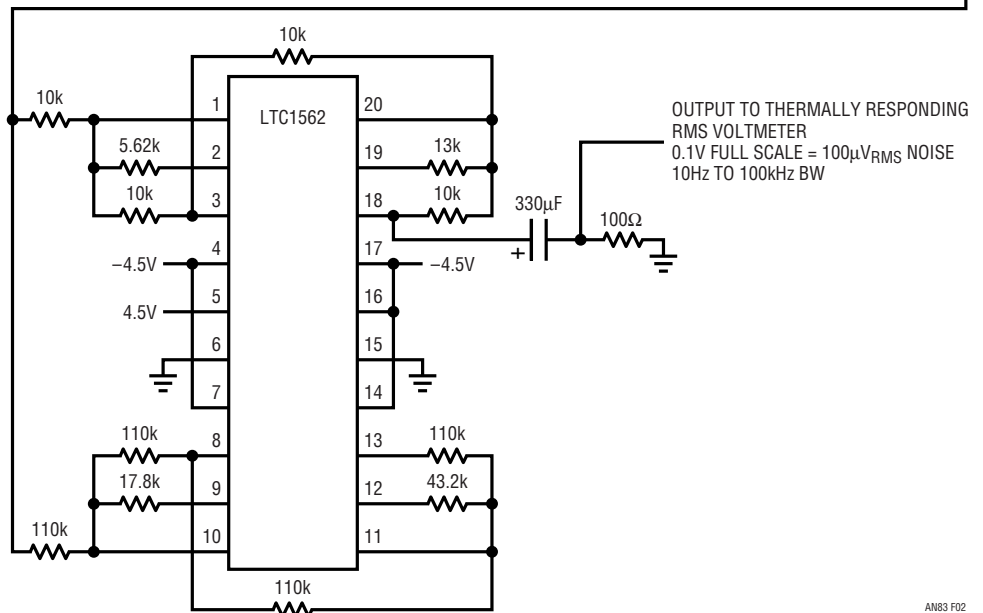


Figure 2. Implementation of Figure 1. Low Noise Amplifiers Provide Gain and Initial Highpass Shaping. LTC1562 Filter Supplies 4th Order Butterworth Lowpass Characteristic

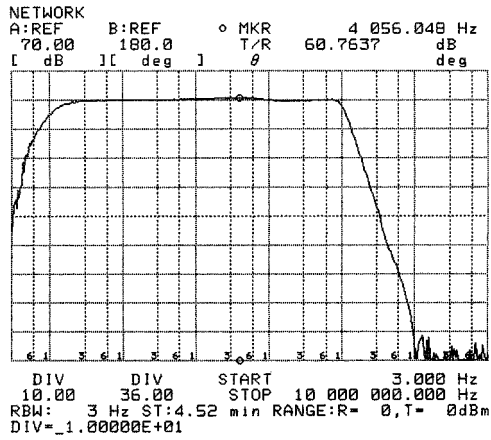


Figure 3. HP-4195A Spectrum Analyzer Plot of Filter Characteristics. Filter Performance Is Nearly Flat Over Desired 10Hz to 100kHz Range with Steep Rolloff Outside Bandpass Region

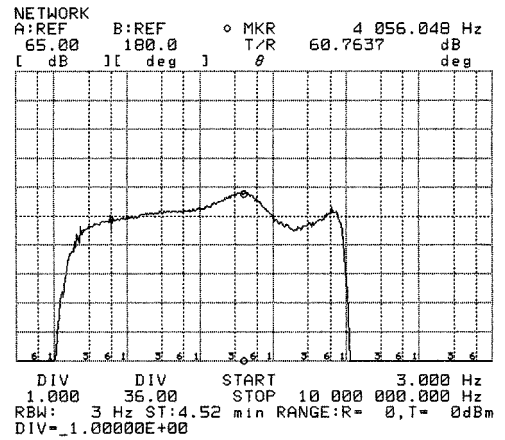


Figure 4. Expanded Scale Examination of Passband Shows Flatness within 1dB Over Almost Entire Measurement Range

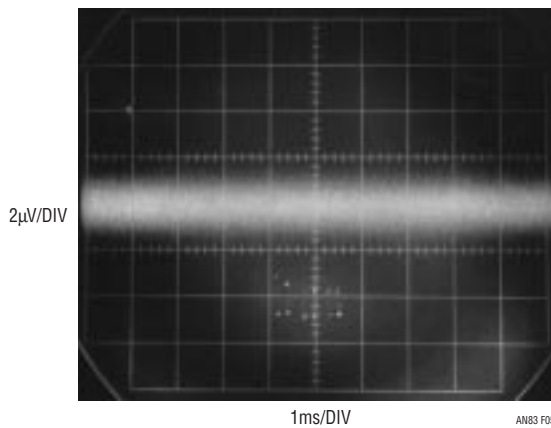


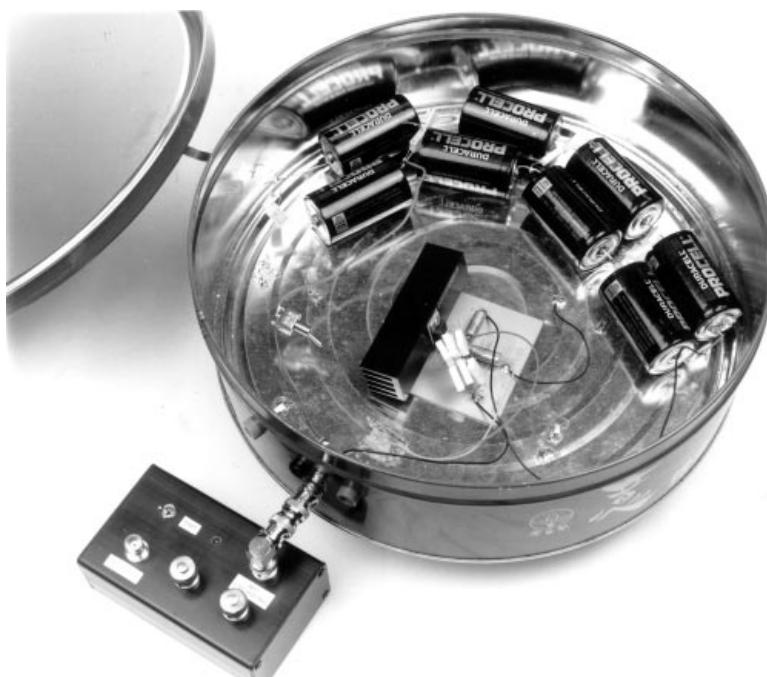
Figure 5. $4\mu\text{V}_{\text{p-p}}$ Test Setup Noise Residue Corresponds to About $0.5\mu\text{V}_{\text{RMS}}$ Measurement Noise Floor

Application Note 83



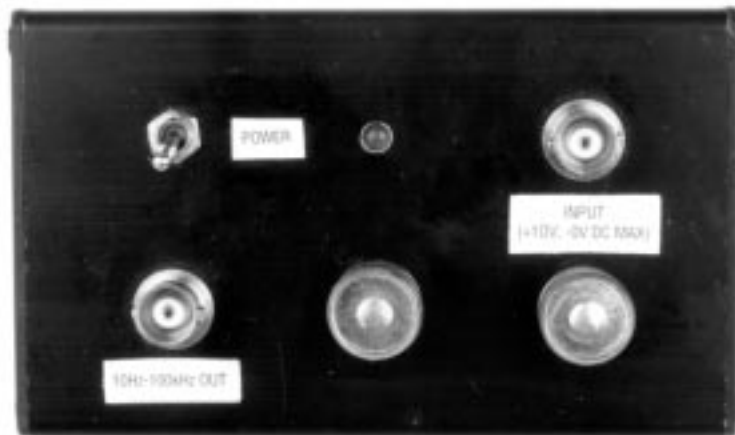
AN83 F06a

Figure 6a. LDO Noise Measurement Bench Setup. Shielded Can Contains Regulator; Noise Filter Circuitry Occupies Box at Photo Lower Center. Oscilloscope and RMS Voltmeter Are Not Simultaneously Connected, Precluding Ground Loop from Corrupting Measurement



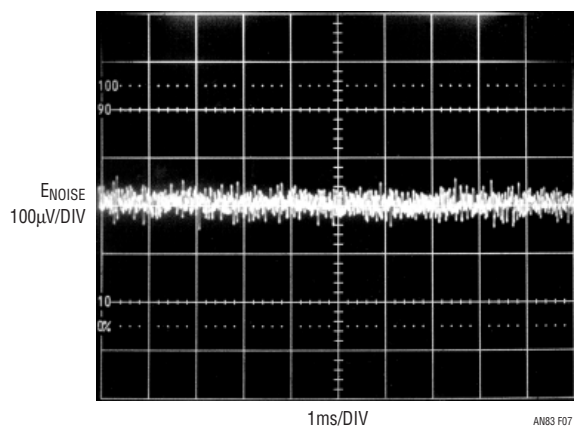
AN83 F06b

Figure 6b. Shielded can with Cover Removed. LDO Under Test Occupies Center. D-Cells Provide Power, Eliminate Potential Ground Loop. BNC Fitting (Photo Lower Left) Connects Output to Filter Circuit Test Box, Minimizing Triboelectric Based Errors



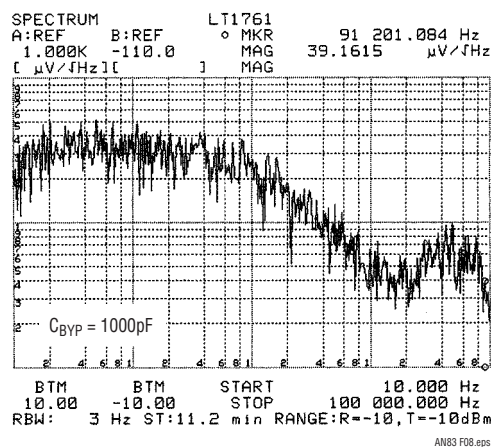
AN83 F06b

Figure 6c. Noise Filter Test Box Is Fully Shielded. Connections Are As Indicated. Capped BNC Fittings (Photo Low Center and Right) Are Unused Entries



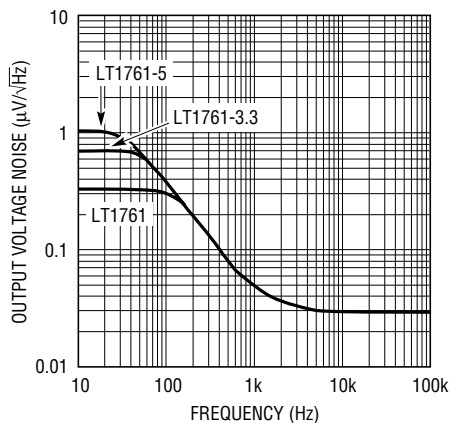
AN83 F07

Figure 7. LT1761 Output Voltage Noise in a 10Hz to 100kHz Bandwidth. RMS Noise Measures $20\mu\text{V}_{\text{RMS}}$



AN83 F08.eps

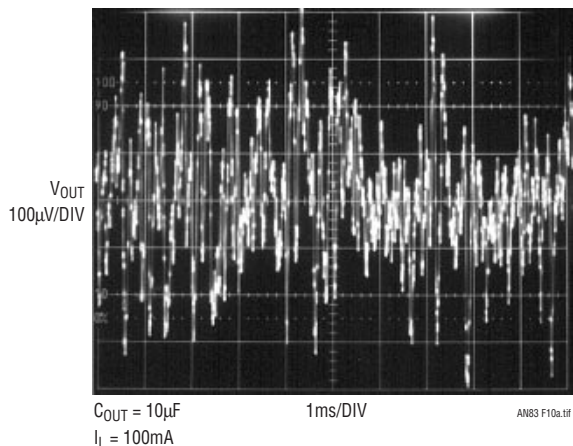
Figure 8. Noise Spectrum Plot Shows Diminishing Power Above 1kHz



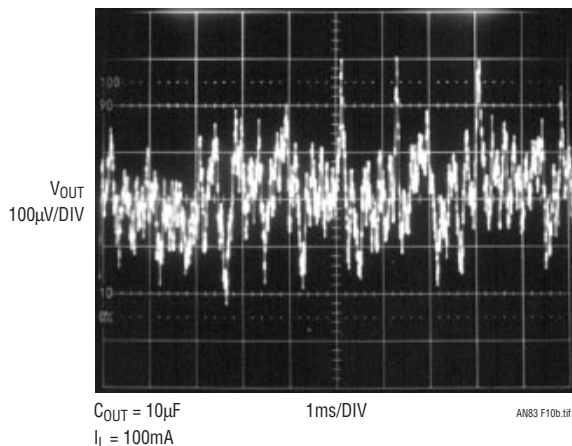
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Figure 9. Output Noise Spectral Density Data Curves for Three Regulators Show Dispersion Below 200Hz

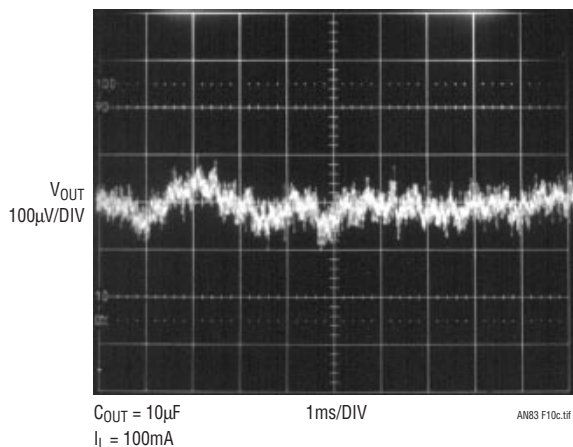
Application Note 83



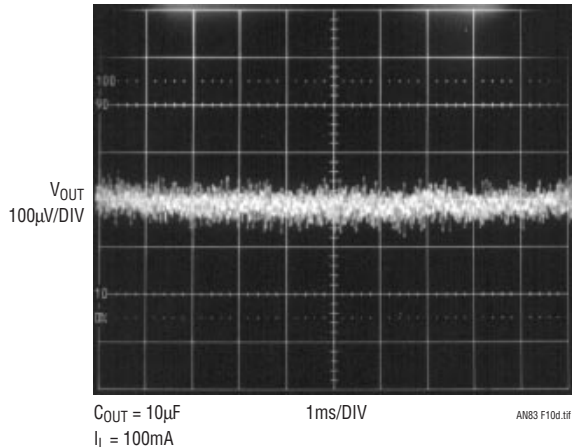
**(10a) LT1761-5
10Hz to 100kHz Output Noise
 $C_{BYP} = 0$**



**(10b) LT1761-5
10Hz to 100kHz Output Noise
 $C_{BYP} = 100$ pF**

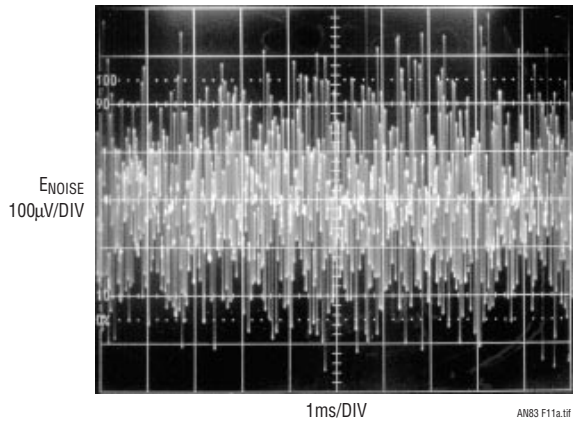


**(10c) LT1761-5
10Hz to 100kHz Output Noise
 $C_{BYP} = 1000$ pF**

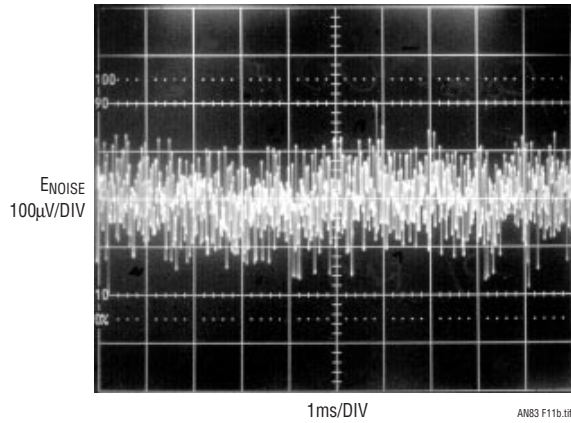


**(10d) LT1761-5
10Hz to 100kHz Output Noise
 $C_{BYP} = 0.01 \mu$ F**

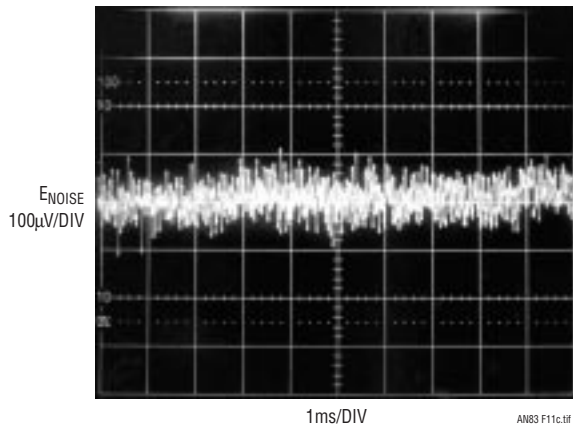
Figure 10. Regulator Noise for Various Bypass Capacitor (C_{BYP}) Values. Noise Decreases with Increasing C_{BYP}



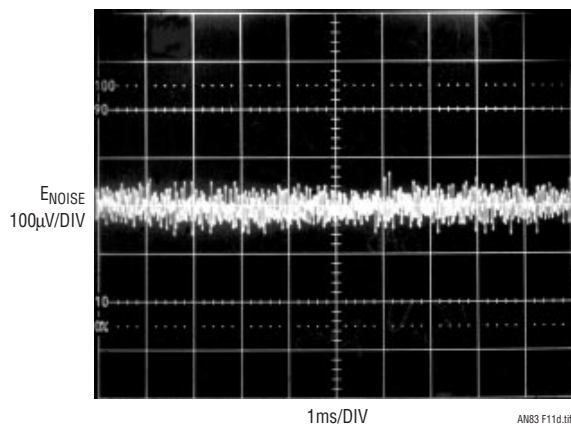
(11a) Manufacturer “MI” Output Voltage Noise (5V Output)



(11b) Manufacturer “NS” Output Voltage Noise (5V Output)



(11c) Manufacturer “MA” Output Voltage Noise (5V Output)



(11d) LT1761-5 Output Voltage Noise (5V Output)

**Figure 11. Noise for LT1761-5 vs Three Other Devices.
 “C” Is Specified for RMS Noise Figure Approaching the LT1761-5,
 but in a Restricted Noise Measurement Bandwidth. Caveat Emptor!**

Application Note 83

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12. O'Neill, P.M., "A Monolithic Thermal Converter," H.P. Journal, May 1980.
13. Williams, J., "A Fourth Generation of LCD Backlight Technology," "RMS Voltmeters," Linear Technology Corporation, Application Note 65, November 1995, pp. 82–83.
14. Tektronix, Inc., "Type 1A7A Differential Amplifier Instruction Manual," Check Overall Noise Level Tangentially, 1968, pp. 5-36 and 5-37.

Note: This application note was derived from a manuscript originally prepared for publication in *EDN* magazine.

APPENDIX A

ARCHITECTURE OF A LOW NOISE LDO

Noise Minimization

The low noise LDOs use Figure A1's scheme, with special attention to minimizing noise transmission within the loop and from unregulated input. The internal voltage reference's noise is filtered by C_{BYP} . Additionally, the error amplifier's frequency response is shaped to minimize noise contribution while preserving transient response and PSRR. Regulators which do not do this have poor noise rejection and transient performance.

Pass Element Considerations

Extremely low dropout voltage requires considering the pass element. Dropout limitations are set by the pass elements on-impedance limits. The ideal pass element has zero impedance capability between input and output and consumes no drive energy.

A number of design and technology options offer various trade-offs and advantages. Figure A2 lists some pass element candidates. Followers offer current gain, ease of loop compensation (voltage gain is below unity) and the drive current ends up going to the load. Unfortunately, saturating a follower requires voltage overdriving the input (e.g. base, gate). Since drive is usually derived directly from V_{IN} , this is difficult. Practical circuits must either generate the overdrive or obtain it elsewhere. Without voltage overdrive, the saturation loss is set by V_{BE} in the bipolar case and channel on-resistance for MOS. MOS channel on-resistance varies considerably under these conditions, although bipolar losses are more predictable. Note that voltage losses in driver stages (Darlington, etc.) add directly to the dropout voltage. The follower output used in conventional 3-terminal IC regulators combines with drive stage losses to set dropout at 3V.

Common emitter/source is another pass element option. This configuration removes the V_{BE} loss in the bipolar case. The PNP version is easily fully saturated, even in IC form. The trade-off is that the base current never arrives at the load, wasting power. At higher currents, base drive losses can negate a common emitter's saturation advantage. As in the follower example, Darlington connections exacerbate the problem. Achieving low dropout in a monolithic PNP regulator requires a PNP structure that attains low dropout while minimizing base drive loss. This is particularly the case at higher pass currents. Considerable effort was expended in this direction in the LT176X through LT196X designs.

Common source connected P-channel MOSFETs are also candidates. They do not suffer the drive losses of bipolars, but typically require volts of gate-channel bias to fully saturate. In low voltage applications this may require generation of negative potentials. Additionally, P-channel devices have poorer saturation than equivalent size N-channel devices.

The voltage gain of common emitter and source configurations is a loop stability concern but is manageable.

Compound connections using a PNP driven NPN are a reasonable compromise, particularly for high power (beyond 250mA) IC construction. The trade-off between the PNP V_{CE} saturation term and reduced drive losses over a conventional PNP structure is favorable. Also, the major current flow is through a power NPN, easily realized in monolithic form. The connection has voltage gain, necessitating attention to loop frequency compensation. Regulators utilizing this pass scheme can supply up to 7.5A with dropouts below 1.5V (LT1083 through LT1086 series).

Readers are invited to submit results obtained with our emeritus thermionic friends, shown out of respectful courtesy.

Application Note 83

Dynamic Characteristics

The LT176X through LT196X's low quiescent currents do not preclude good dynamics. Usually, low quiescent power devices are associated with slow dynamics and instability. The devices are stable (no output oscillation) even with low ESR ceramic output capacitors. This contrasts with conventional LDO regulators that often oscillate with ceramic capacitors.

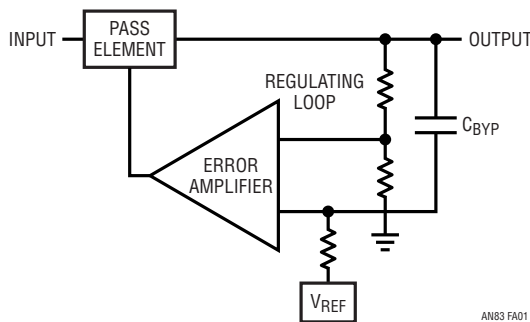


Figure A1. Simplified Low Noise LDO Regulator. Voltage Reference Is Filtered by C_{BYP} , Isolating Noise from Regulating Loop. Error Amplifier's Frequency Compensation Prevents Transmission of Input Noise While Preserving Transient Response

The internal architecture provides an added bonus in transient performance when the $0.01\mu\text{F}$ noise capacitor is added. Transient response for a 10mA to 100mA load step with a $10\mu\text{F}$ output capacitor appears in Figure A3 with the capacitor deleted. Figure A4 shows the same situation with the $0.01\mu\text{F}$ bypass capacitor in place. Settling time and amplitude are markedly reduced.

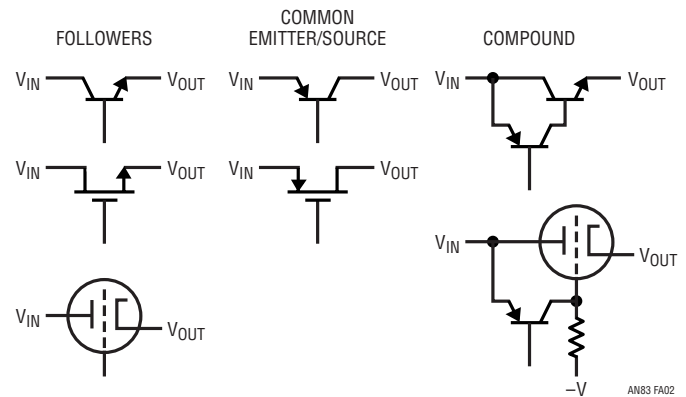


Figure A2. Linear Regulator Pass Element Candidates

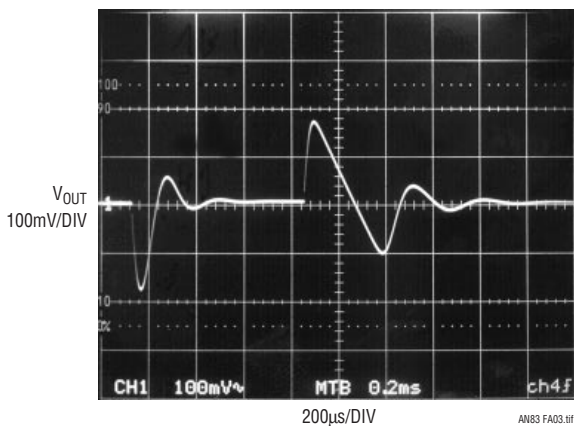


Figure A3. Transient Response without Noise Bypass Capacitor

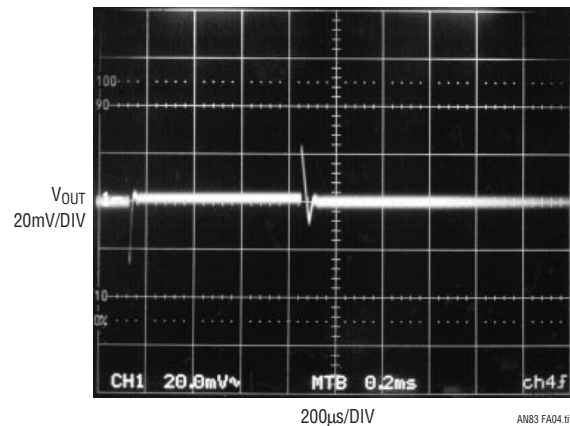


Figure A4. Noise Bypass Capacitor Improves Transient Response. Note Voltage Scale Change

APPENDIX B

CAPACITOR SELECTION CONSIDERATIONS

Bypass Capacitance and Low Noise Performance

Adding a capacitor from the regulators V_{OUT} to BYP pin lowers output noise. A good quality low leakage capacitor is recommended. This capacitor bypasses the regulator’s reference, providing a low frequency noise pole. A 0.01 μ F capacitor lowers the output voltage noise to 20 μ V_{RMS}. Using a bypass capacitor also improves transient response. With no bypassing and a 10 μ F output capacitor, a 10mA to 500mA load step settles within 1% of final value in under 100 μ s. With a 0.01 μ F bypass capacitor, the output settles within 1% for the same load step in under 10 μ s; total output deviation is inside 2.5%. Regulator start-up time is inversely proportional to bypass capacitor size, slowing to 15ms with a 0.01 μ F bypass capacitor and 10 μ F at the output.

Output Capacitance and Transient Response

The regulators are designed to be stable with a wide range of output capacitors. Output capacitor ESR affects stability, most notably with small capacitors. A 3.3 μ F minimum output value with ESR of 3 Ω or less is recommended to prevent oscillation. Transient response is a function of output capacitance. Larger values of output capacitance decrease peak deviations, providing improved transient response for large load current changes. Bypass capacitors, used to decouple individual components powered by

the regulator, increase effective output capacitor value. Larger values of reference bypass capacitance dictate larger output capacitors. For 100pF of bypass capacitance, 4.7 μ F of output capacitor is recommended. With 1000pF of bypass capacitor or larger, a 6.8 μ F output capacitor is required.

Figure B1’s shaded region defines the regulator’s stability range. Minimum ESR needed is set by the amount of bypass capacitance used, while maximum ESR is 3 Ω .

Ceramic Capacitors

Ceramic capacitors require extra consideration. They are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high capacitance in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures B2 and B3. Used with a 5V regulator, a 10 μ F Y5V capacitor shows value as low as 1 μ F to 2 μ F over the operating temperature range. The X5R and X7R dielectrics have more stable characteristics and are more suitable for output capacitor use. The X7R type has better stability over temperature, while the X5R is less expensive and available in higher values.

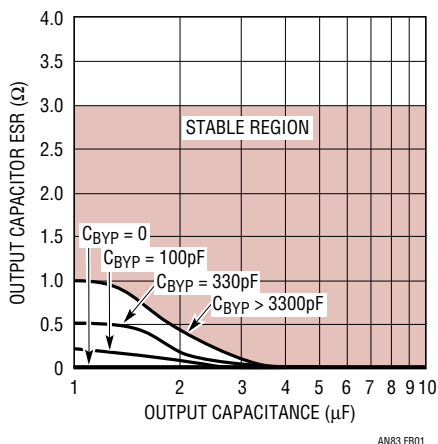


Figure B1. Regulator Stability for Various Output and Bypass (C_{BYP}) Capacitor Characteristics

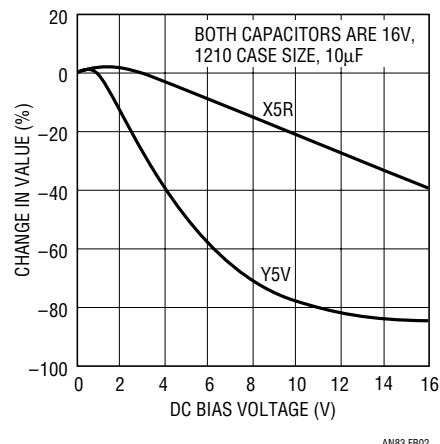


Figure B2. Ceramic Capacitor DC Bias Characteristics Indicate Pronounced Voltage Dependence. Device Must Provide Desired Capacitance Value at Operating Voltage

Application Note 83

Voltage and temperature coefficients are not the only problem sources. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients. The

resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure B4's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

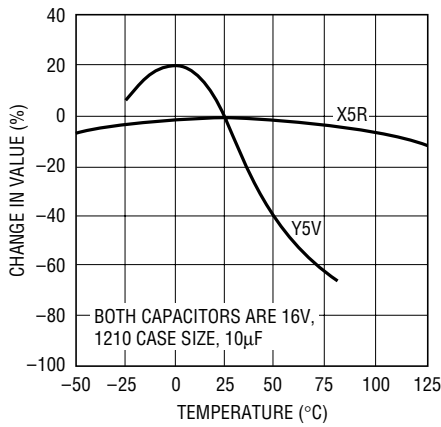


Figure B3. Ceramic Capacitor Temperature Characteristics Show Large Capacitance Shift. Effect Should Be Considered When Determining Circuit Error Budget

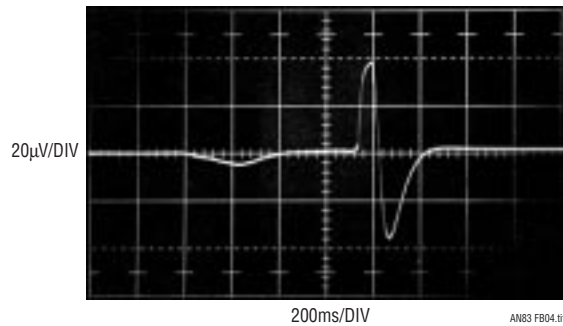


Figure B4. A Ceramic Capacitor Responds to Light Pencil Tapping. Piezoelectric Based Response Approaches 80µV_{p-p}

APPENDIX C

UNDERSTANDING AND SELECTING RMS VOLTMETERS

The choice of AC voltmeter is absolutely crucial for meaningful measurements. The AC voltmeter must respond faithfully to the RMS value of the measured noise. The majority of AC voltmeters (including DVMs with AC ranges) are *not* capable of doing this. This includes instruments with “true RMS” AC scales. As such, selecting an appropriate instrument requires care. The selection process begins with a basic understanding of AC voltmeter types.¹

AC Voltmeter Types

There are three basic AC voltmeter types. They include rectify and average, analog computing and thermal. The thermal approach is the only one that is inherently accurate, regardless of input waveshape. This feature is particularly relevant to noise RMS amplitude determination.

Rectify and Average

The rectify and average scheme (Figure C1) applies the AC input to a precision rectifier. The rectifier output feeds a simple RC averager which is gain scaled, providing the output. In practice, gain is set so the DC output equals the RMS value of a sine wave input. If the input remains a pure sine wave, accuracy can be quite good. However, nonsinusoidal inputs cause large errors. This type voltmeter is only accurate for sine wave inputs, with increasing error as the input departs from sinusoidal.

Note 1: Another way to approximately measure RMS AC noise using an oscilloscope is the tangential method. See Reference 14.

Analog Computation

Figure C2 shows a more sophisticated AC voltmeter method. Here, the instantaneous value is (ideally) continuously computed by an analog computational loop. The DC output follows the equation noted, resulting in much better accuracy as input waveshape varies. Almost all commercial implementations of this approach utilize logarithmically based analog computing techniques. Unfortunately, dynamic limitations in the ZY/X block dictate bandwidth restrictions. These circuits typically develop significant errors beyond 20kHz to 200kHz.

Thermal

The thermally based AC voltmeter is inherently insensitive to input waveshape, particularly suiting it to noise RMS amplitude measurement. Additionally, high accuracy at bandwidths exceeding 100MHz is achievable. Figure C3 diagrams the classic thermal scheme.² It is composed of matched heater-temperature sensor pairs and an amplifier. The AC input drives a heater, warming it. The temperature sensor associated with this heater responds, biasing

the amplifier. The amplifier closes its feedback loop by driving the output heater to warm its associated temperature sensor. When the loop closes, the heaters are at the same temperature. This “force-balance” action results in the DC output equalling the input heater’s RMS heating value—the fundamental definition of RMS. Changes in waveshape have no effect, as they are effectively down-converted to heat. This “first principles” nature of operation makes thermally based AC voltmeters ideal for quantitative RMS noise measurement.

Performance Comparison of Noise Driven AC Voltmeters

The wide performance variation of the above methods, and even within a method, mandates caution in selecting an AC voltmeter. Comparing AC voltmeters intended for use in RMS noise measurements is illuminating. Figure C4 shows a simple evaluation arrangement. The noise generator drives the external input of text Figure 2, producing a suitably band passed input at the voltmeter under test.³

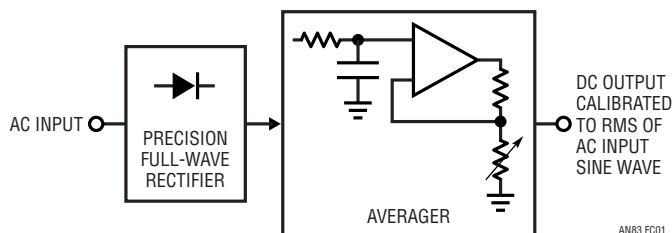


Figure C1. Rectify-and-Average Based AC-DC Converter. Gain Is Set So DC Output Equals RMS Value of Sine Wave Input. Nonsine Inputs Produce Errors

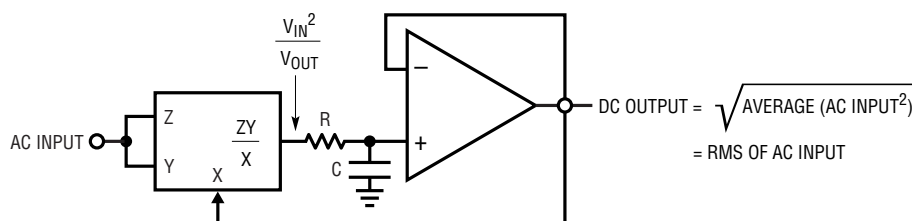


FIGURE DERIVED FROM REFERENCES 2 AND 3

Figure C2. Analog Computer Based AC-DC Converter. Loop Continuously Computes Input’s RMS Value. Bandwidth Limitations Produce High Frequency Errors

Note 2: See the References section for publications covering thermal AC–DC conversion.

Note 3: Noise generators are worthy of study and considered in References 4 and 5.

Application Note 83

Figure C5 shows results for 20 voltmeters. Four of the voltmeters are thermal types; the remainder utilize logarithmic analog computing or rectify and average AC-DC conversion. The four thermal types agreed well within 1%. In fact, three of the thermal types were within 0.2%, while the fourth (HP3400A), a metered instrument, is only readable to 1%. The other 16 voltmeters showed errors up to 48% relative to the thermal group! Note that the errors cause lower readings than are actually warranted; a poorly chosen voltmeter will give unfairly optimistic readings.

The lesson here is clear. It is essential to verify AC voltmeter accuracy before proceeding with RMS noise measurement. Failure to do so may cause highly misleading “results.”

Thermal Voltmeter Circuit

It is sometimes desirable to construct, rather than purchase, a thermal voltmeter. Figure C6’s circuit is applicable to noise measurement. Text Figure 2’s filter feeds A1. A1’s output biases A2, which provides additional AC gain. The LT1088 based RMS/DC converter is made up of matched pairs of heaters and diodes and a control amplifier. The LT1206 drives R1, producing heat which lowers D1’s voltage. Differentially connected A3 responds by driving R2, via Q3, to heat D2, closing a loop around the

amplifier. Because the diodes and heater resistors are matched, A3’s DC output is related to the RMS value of the input, regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain trim, which is implemented at A4. A4’s output is the circuit output.

Start-up or input overdrive can cause A2 to deliver excessive current to the LT1088 with resultant damage. C1 and C2 prevent this. Overdrive forces D1’s voltage to an abnormally low potential. C1 triggers low under these conditions, pulling C2’s negative input low. This causes C2’s output to go high, putting A2 into shutdown and terminating the overload. After a time determined by the RC at C2’s input, A2 will be enabled. If the overload condition still exists, the loop will almost immediately shut A2 down again. This oscillatory action will continue, protecting the LT1088 until the overload condition is removed.

To trim this circuit, connect its input to a 10mV_{RMS} , 100kHz signal. Set the 500Ω adjustment for exactly 100mV DC out. Next, apply a 100kHz , $100\text{mV}_{\text{RMS}}$ input and trim the 10k potentiometer for 1V DC out. Repeat this sequence until the adjustments do not interact. Two passes should be sufficient.

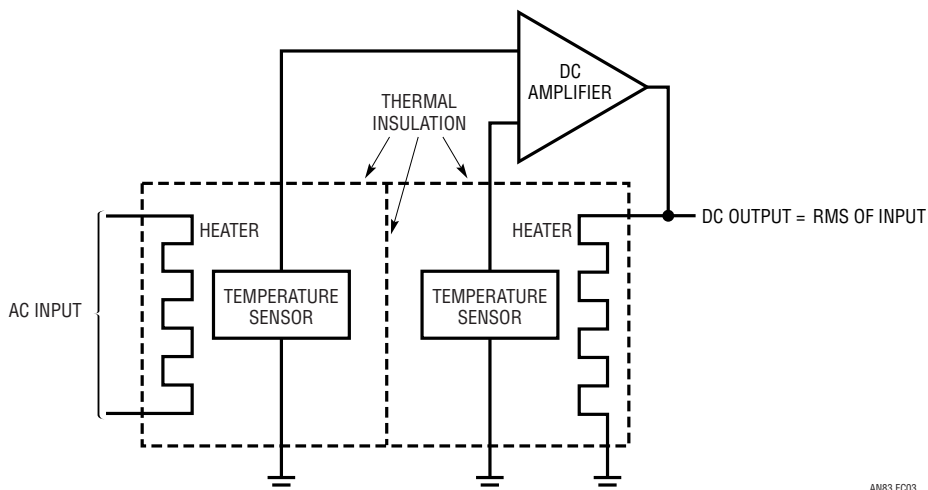


Figure C3. Thermally Based AC-DC Converter Converts AC Input to Heat. Remaining Circuitry Determines DC Value (Output) Required to Produce Identical Heating. Error Is Extraordinarily Low, Even at Waveshape and Bandwidth Extremes

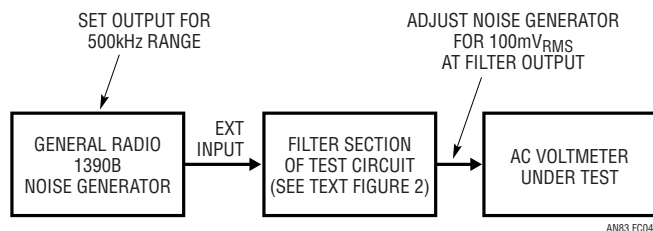


Figure C4. Arrangement for Evaluating AC Voltmeters. Noise Source, Filtered by Figure 2's Circuit, Drives the Voltmeter

VOLTMETER TYPE OR SAMPLE NUMBER	READING IN MILLIVOLTS	ERROR IN %	AC-DC CONVERSION METHOD
HP3403C	100	0	Thermal
HP3400A	100	0	Thermal
Fluke 8920A	100	0	Thermal
LTC Special (See Figure C6)	100	0	Thermal
1	84	-16	Log
2	85	-15	Rect-Avg
3	84	-16	Rect-Avg
4 Fluke 8800A	90	-10	Rect-Avg
5 HP3455	100	0	Log
6 HP334	92	-8	Rect-Avg
7 Handheld	52	-48	Rect-Avg
8 HP3478	100	0	Log
9 Inexpensive Handheld	56	-44	Rect-Avg
10 HP403B	93	-7	Rect-Avg
11 HP3468B	93	-7	Log
12	80	-20	Rect-Avg
13	72	-28	Rect-Avg
14	62	-38	Rect-Avg
15 Fluke 87	95	-5	Log
16 HP34401A	93	-7	Log

Figure C5. Results of AC Voltmeter Evaluation. Four Thermally Based Types Agree within 1%. Other Instruments Show Relative Error As Large As 48%

Application Note 83

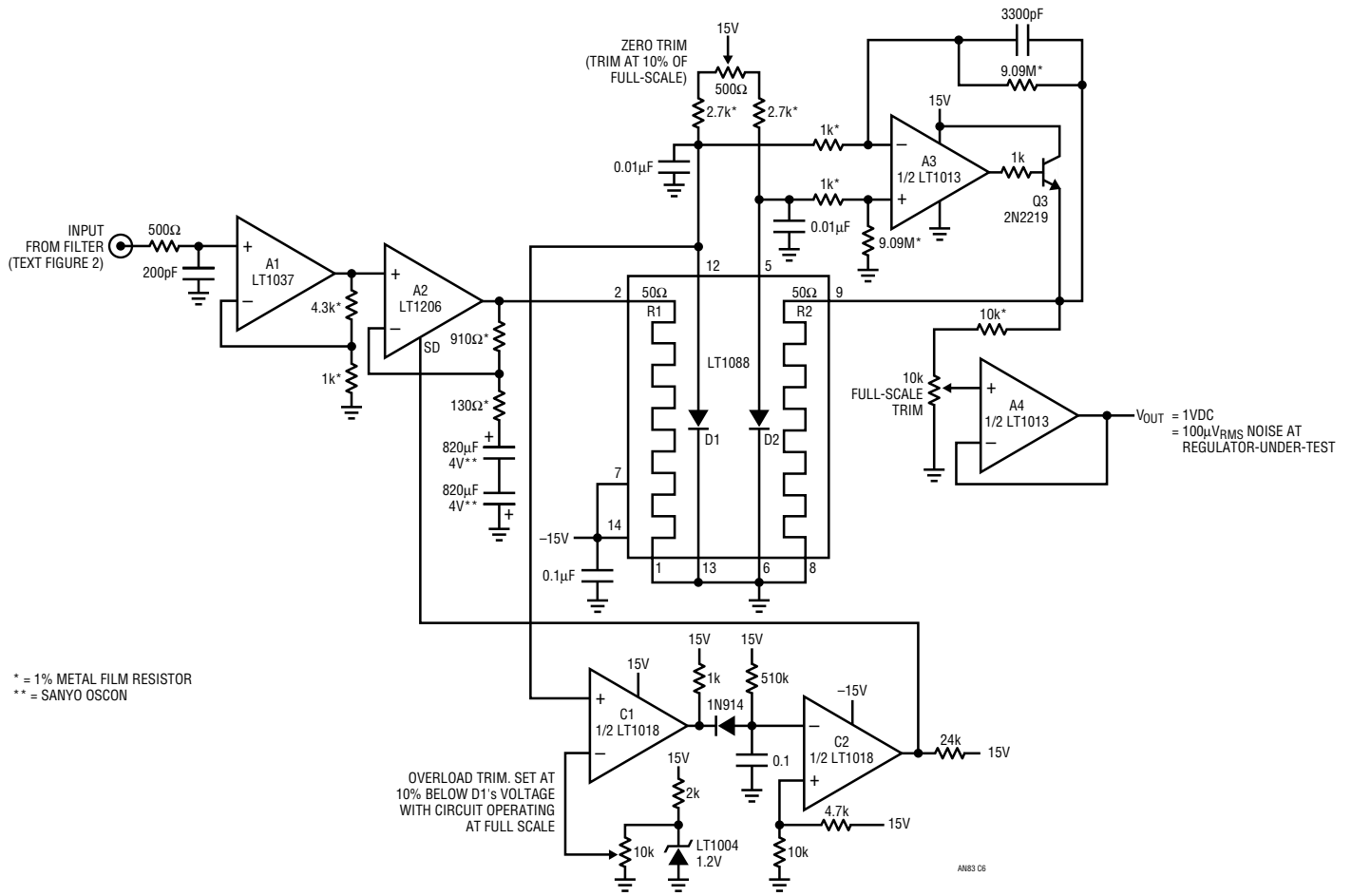


Figure C6. Inexpensive Thermally Based RMS Voltmeter Suitable for LDO Noise Measurement

APPENDIX D

PRACTICAL CONSIDERATIONS FOR SELECTING A LOW NOISE LDO

Any design has particular requirements for a low noise LDO; every individual situation should be carefully examined for specific needs. However, some general guidelines apply in selecting a low noise LDO. Significant issues are summarized below.

Current Capacity

Insure the regulator has adequate output current capacity for the application, including worst-case transient loads.

Power Dissipation

The device must be able to dissipate whatever power is required. This effects package choice. Usually, the $V_{IN}-V_{OUT}$ differential is low in LDO applications, obviating this issue. Prudence dictates checking to be sure.

Package Size

Package size is important in limited space applications. Package size is dictated by current capacity and power dissipation constraints. See the preceding paragraphs.

Noise Bandwidth

Insure that the LDO meets the system's noise requirement over the entire bandwidth of interest. 10Hz to 100kHz is realistic, as information usually occupies this range.

Input Noise Rejection

Insure that the regulator can reject input related disturbances originating from clocks, switching regulators and other power bus users. If the regulator's power supply rejection is poor, its low noise characteristics are useless.

Load Profile

Know the load characteristics. Steady state drain is obviously important, but transient loads must also be evaluated. The regulator must maintain stability and low noise characteristics under all such transient loads.

Discrete Components

The choice of discrete components, particularly capacitors, is important. The wrong capacitor dielectric can adversely effect stability, noise performance, or both. See Appendix B, "Capacitor Selection Considerations."

Application Note 83



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Low Noise Varactor Biasing with Switching Regulators

Vanquishing Villainous Vitiators Vis-à-Vis Vital Varactors

Jim Williams and David Beebe

INTRODUCTION

Telecommunication, satellite links and set-top boxes all require tuning a high frequency oscillator. The actual tuning element is a varactor diode, a 2-terminal device that changes capacitance as a function of reverse bias voltage.¹ The oscillator is part of a frequency synthesizing loop, as detailed in Figure 1. A phase locked loop (PLL) compares a divided down representation of the oscillator with a frequency reference. The PLL's output is level shifted to provide the high voltage necessary to bias the varactor, which closes a feedback loop by voltage tuning the oscillator. This loop forces the voltage controlled oscillator (VCO) to operate at a frequency determined by the frequency reference and the divider's division ratio.

Varactor Biasing Considerations

The high voltage bias is required to achieve wide-range varactor operation. Figure 2 shows varactor capacitance vs reverse voltage curves for a family of devices. A 10:1 capacitance shift is available, although a 0.1V to 30V swing is required. The curves shown are characteristic of typical

“hyperabrupt” devices. Response modification is possible, with compromises in performance, particularly with regard to linearity and sensitivity.²

Note 1. Theoretical considerations of varactor diodes are treated in Appendix A, “Zetex Variable Capacitance Diodes,” guest written by Neil Chadderton of Zetex.

Note 2. The reader is again referred to Appendix A for in-depth discussion of varactor diodes.

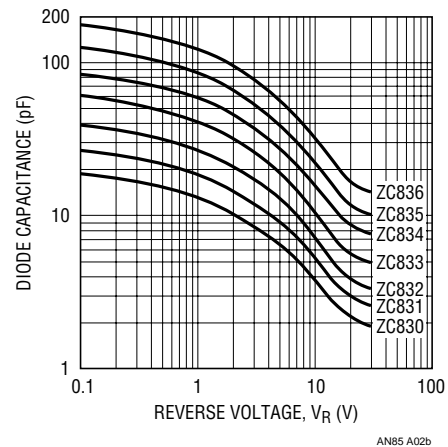


Figure 2. Typical Capacitance Voltage Characteristics for the Zetex ZC830-6 Range. 0.1V to 30V Swing Results in ≈10× Capacitance Shift

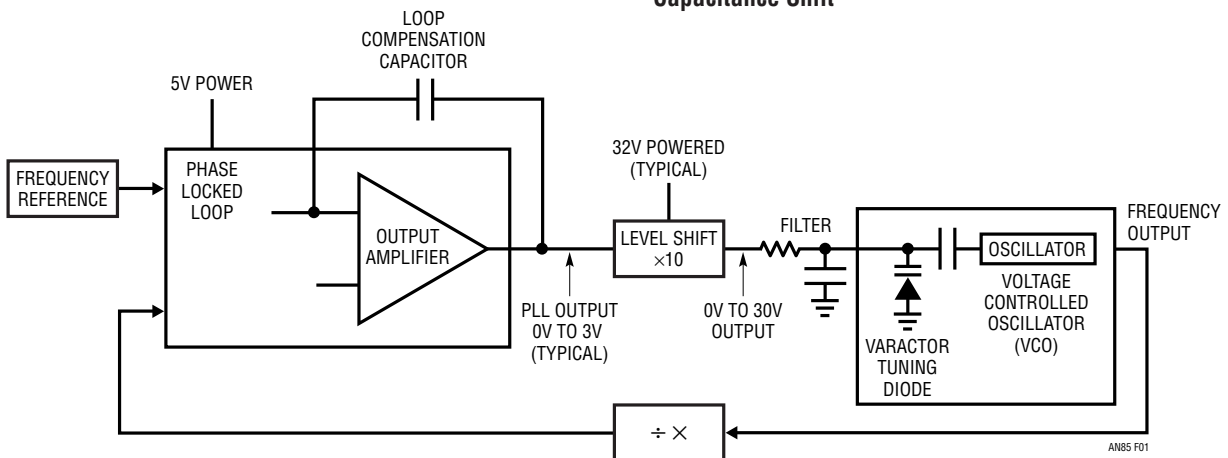


Figure 1. Typical Phase Lock Loop-Based Frequency Synthesizer. Level Shift Furnishes 0V to 30V Bias to VCO Varactor Diode, Although a 32V Supply is Required

Application Note 85

The bias voltage requirement has traditionally been met by utilizing existing high voltage rails. The current trend towards low voltage powered systems means the high voltage bias must be locally generated. This implies some form of voltage step-up switching regulator. This is certainly possible, but varactor noise sensitivity complicates design. In particular, the varactor responds to any form of amplitude variation of its bias, resulting in an undesired capacitance shift. Such a shift causes VCO frequency movement, resulting in spurious oscillator outputs. DC and low frequency shifts are removed by PLL loop action, but activity outside the loop's passband causes undesired outputs. Most applications require spurious oscillator output content to be 80dB or more below the nominal output frequency³. This implies a low noise, high voltage supply, mandating caution in the switching regulator design. Switching regulators are often associated with noisy operation, making a varactor bias application seem hazardous. Careful preparation can eliminate this concern, allowing a practical switching regulator-based approach to varactor biasing.

Low Noise Switching Regulator Design

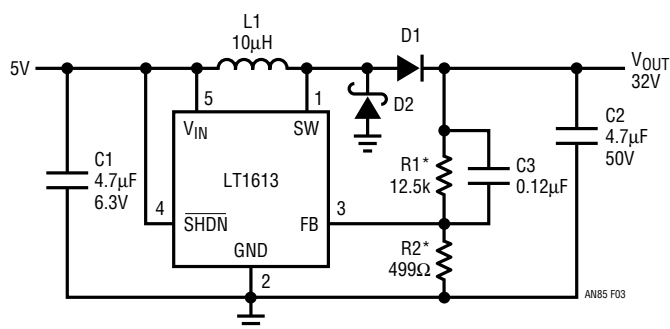
In theory, a simple flyback regulator will work, but component choice and attention to layout are critical to achieving low noise. Additionally, component count, size and cost are usually considerations in varactor bias applications. Figure 3 shows a step-up switching regulator that, properly incarnated, permits low noise varactor biasing. The circuit is a simple boost regulator. L1, in

conjunction with the SW pin's ground-referred switching, provides voltage step-up. D1 and C2 filter the output to DC, D2 clips possible L1 negative excursions and the feedback resistor ratio sets the loop servo point, and hence, the output voltage. C3 tailors loop frequency response, minimizing switching-frequency ripple components at the output. C1 and C2 are specified for low loss dynamic characteristics and the LT[®]1613's 1.7MHz switching frequency allows miniature, small value components. This relatively high switching frequency also means that ancillary "downstream" filtering is possible with similarly miniature, small value components.

Layout Issues

Layout is the most crucial design aspect for obtaining low noise. Figure 4 shows a suggested layout. Ground, V_{IN} and V_{OUT} are distributed in planes, minimizing impedance. The LT1613 GND pin (Pin 2) carries high speed, switched current; its path to the circuit's power exit should be direct and highly conductive at all frequencies. R2's return current, to the extent possible, should not mix with Pin 2's large dynamic currents. C1 and C2 should be located close to Pin 5 and D1 respectively. Their grounded ends

Note 3. Spurious oscillator outputs are referred to as "spurs" in RF parlance.



- *1% METAL FILM RESISTORS
- C1: TAIYO YUDEN JMK212BJ475MG
- C2: MURATA GRM235V5V475Z50
- D1: 1N4148
- D2: ON SEMICONDUCTOR MBR0540 OR LITE ON/DIODES INC. B0540W
- L1: MURATA LQH3C100

Figure 3. LT1613-Based Boost Regulator with Appropriate Component Selection and Layout Has Low Noise Characteristics Needed for Varactor Biasing

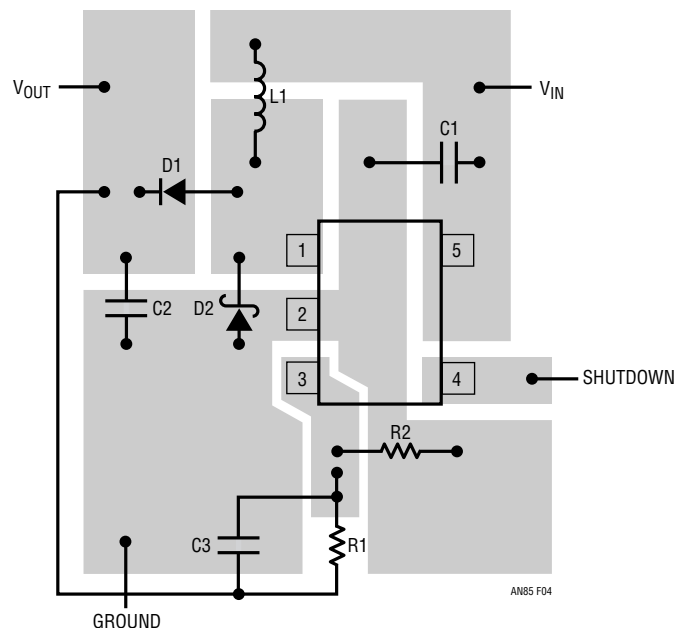


Figure 4. Layout Requires Attention to Component Placement and Ground Current Flow Management. Compact Layout Reduces Parasitic Inductance, Radiation and Crosstalk. Grounding Scheme Minimizes Return Current Mixing

should tie directly to the ground plane. L1 has a low impedance path to V_{IN} ; its driven end returns directly to LT1613 Pin 1. D1 and D2 should have short, low inductance runs to C2 and Pin 2, respectively; their common connection mating tightly with Pin 1 and L1. Pin 1 has a small area, minimizing radiation. Note that this point is enclosed by planes operating at AC ground, forming a shield. The feedback node (Pin 3) is further shielded from switching radiation, preventing unwanted interaction. Finally, L1 should be oriented so its radiation causes minimal circuit disruption.

Level Shifts

The low voltage PLL output (see Figure 1) requires an analog level shift to bias the varactor. Figure 5 shows some alternatives. Figure 5a is an amplifier powered from the LT1613's 32V output. The feedback ratio sets a gain of 10, resulting in a 0V to 30V output for a 0V to 3V input. Figure 5b is a noninverting common base stage. Gain is less well controlled than in Figure 5a, but overall frequency synthesizer loop action obviates this concern. Figure 5c's common emitter circuit is similar except that it inverts.

Test Circuit

Figure 6 combines the above considerations into a realistic test circuit. The 5V powered design is composed of the

LT1613 regulator, an amplifier-based level shift and a GHz range VCO. The amplifier is biased by a filtered LT1004 reference to a 12V output, simulating a typical varactor bias point. The LT1613 configuration's low noise output receives additional filtering via the 100Ω - $0.1\mu\text{F}$ network at the amplifier power pin and by the amplifier's power supply rejection ratio (PSRR). The RC combination provides a theoretical (unloaded) break below 20kHz; the amplifier's PSRR benefit is derived from Figure 7. This graph shows PSRR vs frequency for a typical amplifier. There is a steep roll-off beyond 100Hz, although almost 20dB attenuation is available in the MHz region. This implies that the amplifier provides some beneficial filtering of the LT1613's residual 1.7MHz switching components.

A final RC filter section is placed directly at the VCO varactor bias input. Ideally this filter's break frequency is far removed from the 1.7MHz switching rate for maximum ripple attenuation. In practice, the filter is within the PLL loop, placing restrictions on how much delay it can introduce. A PLL loop bandwidth of 5kHz is usually desirable, dictating a filter point of about 50kHz to ensure closed-loop stability. As such, the final RC filter ($1.6\text{k}\Omega$ - $0.002\mu\text{F}$) is set at this frequency. It is worth noting that the varactor's input resistance is quite high—essentially that of a reverse-biased diode—and no filter buffering is required to drive it.

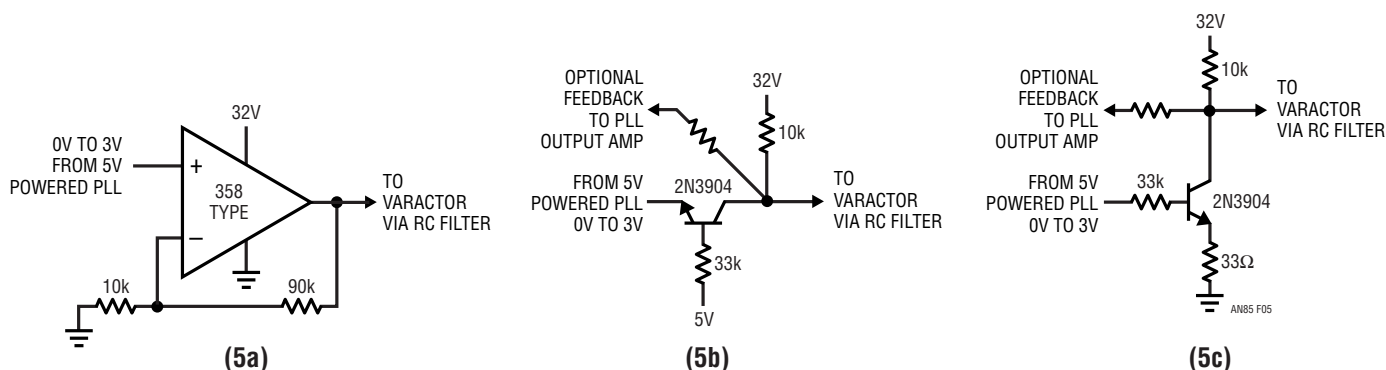


Figure 5. Level Shift Options Include Op Amp (5a), Noninverting Common Base (5b) and Inverting Common Emitter (5c). Op Amp's Operating Point is Inherently Stable; 5b and 5c Rely on PLL Closed-Loop Action Unless Optional Feedback is Used

Application Note 85

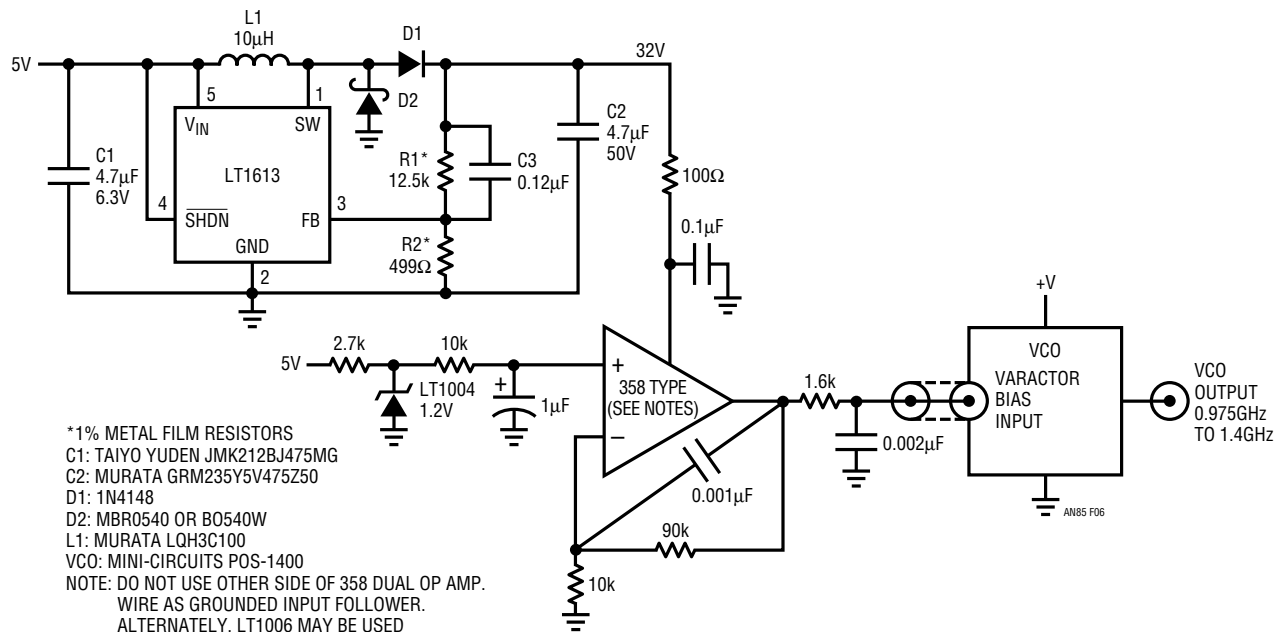


Figure 6. Noise Test Circuit Includes Step-Up Switching Regulator, Biased Op Amp Level Shift, Filtering Elements and GHz Range VCO. Switching Regulator-Associated L1 is the Only Inductor Required

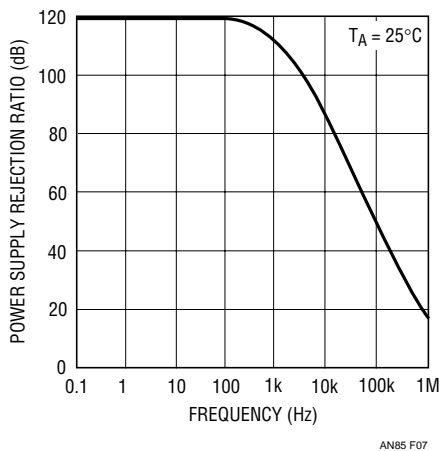


Figure 7. Typical Op Amp Power Supply Rejection Ratio Degrades with Frequency, Although Nearly 20dB is Available in LT1613's MHz Switching Range

Noise Performance

Careful measurements permit verification of circuit noise performance.⁴ Figure 8 shows about 2mV ripple at the LT1613's 32V output. Figure 9, taken at the amplifier power pin, shows the effect of the 100Ω-0.1μF filter. Ripple and noise are reduced to about 500μV. Figure 10, recorded at the amplifier output, shows the influence of amplifier PSRR. Ripple and noise are further reduced to

about 300μV. The actual ripple component is about 100μV. The final RC filter, located directly at the VCO varactor input, gives about 20dB further attenuation. Figure 11 shows ripple and noise inside 20μV with a ripple component of about 10μV.

Effects of Poor Measurement Technique

The above results require good measurement technique. The measurements were taken utilizing a purely coaxial probing environment. Deviations from this regime will produce misleading and unduly pessimistic indications.⁵ For example, Figure 12 shows a 50% amplitude error over Figure 8, even though it nominally monitors the same point. The difference is that Figure 12 utilizes a 3" probe ground lead instead of Figure 8's coaxial ground tip adapter. Similarly, Figure 9's amplifier power pin 500μV measurement degrades to Figure 13's indicated 2mV representation using the 3" probe ground strap. The same

Note 4. See Appendix B, "Preamplifier and Oscilloscope Selection," for equipment recommendations to make the high sensitivity oscilloscope measurements described in this section. See also Appendix C, "Probing and Connection Techniques for Low Level, Wideband Signal Integrity."

Note 5. Additional discourse along these lines is presented in Appendix C, "Probing and Connection Techniques for Low Level, Wideband Signal Integrity." See also Reference 2-5.

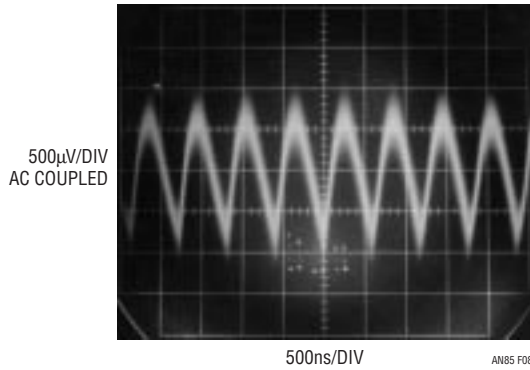


Figure 8. LT1613-Based Output Shows 2mV_{p-p} Ripple and Noise

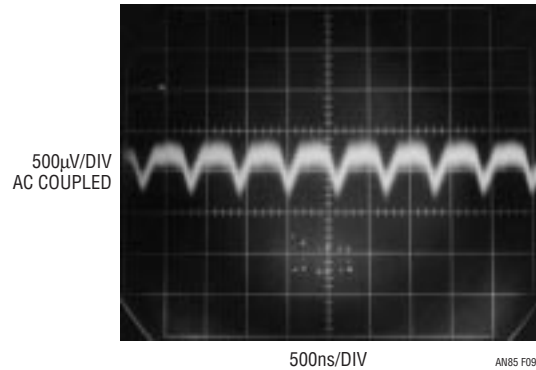


Figure 9. RC Filter at Amplifier's Power Input Pin Reduces Ripple and Noise to 500µV_{p-p}

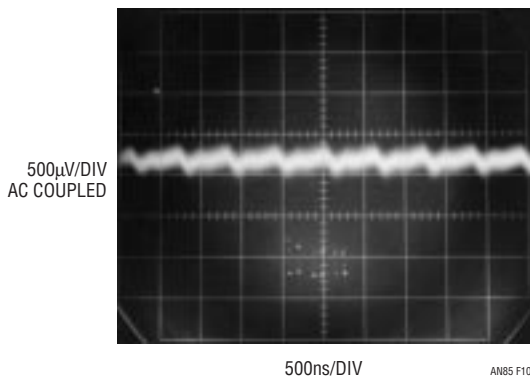


Figure 10. Amplifier Output Shows Additional Filtering Due to Amplifier PSRR. Aberrations Are Inside 300µV

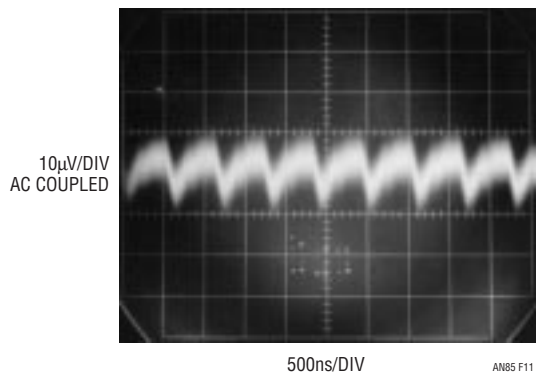


Figure 11. VCO Varactor Bias Input, After 50kHz RC Filter, Displays Less Than 20µV Ripple and Noise. Content Coherent with LT1613's 1.7MHz Switching is Inside 10µV

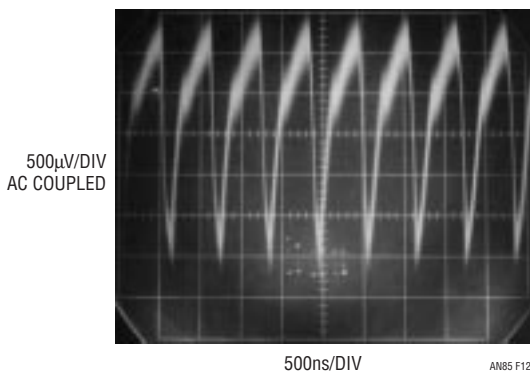


Figure 12. Improper Probing Technique. 3" Ground Lead Causes 50% Display Error vs Figure 8's Purely Coaxial Measurement

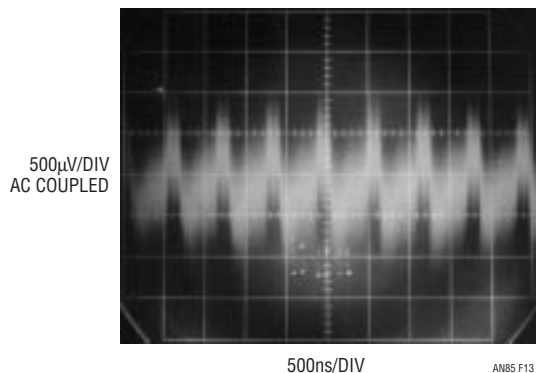


Figure 13. 3" Ground Lead Degrades Figure 9's 500µV Reading to 2mV

Application Note 85

ground strap causes pronounced error in Figure 14's apparent 2mV amplifier output vs Figure 10's correct 300 μ V excursion. Figure 15 shows a 70 μ V indication at the VCO varactor input using the 3" ground strap. That's a long way from Figure 11's 20 μ V data taken with the coaxial ground tip adapter!⁶

In Figure 16 the coaxial ground tip adapter is used but the VCO varactor input shows a blizzard of noise compared to Figure 11's orderly trace. The reason is that a 12" voltmeter lead was connected to the point. Pickup and stray RF act against the node's finite output impedance, corrupting the measurement. Figure 17, also taken at the VCO input, is better but still shows greater than 50% error. The culprit

here is a second probe, located at the LT1613 V_{SW} pin, used to trigger the oscilloscope. Even with coaxial techniques in use at both probe points, the trigger probe dumps transient currents into the ground plane. This introduces small common mode voltages, resulting in the apparent noise increase. The cure is to trigger the oscilloscope with a noninvasive probe.⁷

Note 6. If you don't think 70 μ V is a "long way" from 20 μ V, consider your reaction to a 3.5 \times income tax reduction.

Note 7. The reader is not being requested to indulge wishful thinking. Such a probe is more easily realized than might be supposed. See Appendix C, "Probing and Connection Techniques for Low Level, Wideband Signal Integrity."

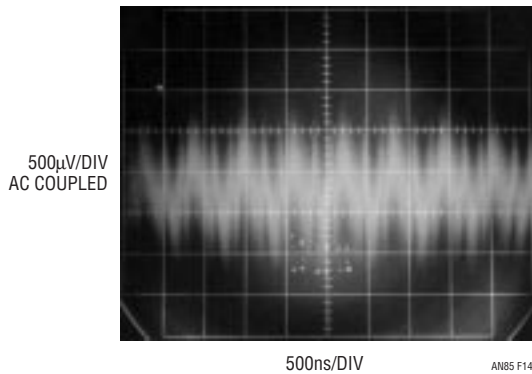


Figure 14. Probe Ground Strap Causes Erroneous 2mV Indication. Actual Value is Figure 10's 300 μ V Reading

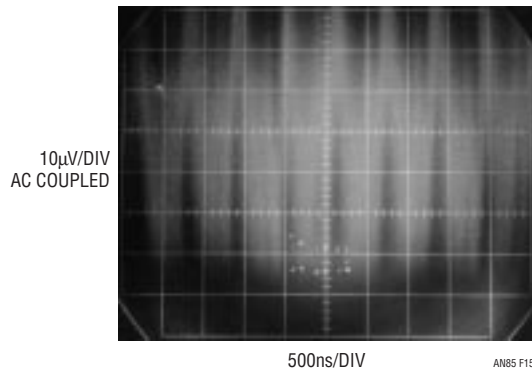


Figure 15. Probe Ground Strap Causes 3.5 \times Readout Error vs Figure 11's Correctly Measured 20 μ V

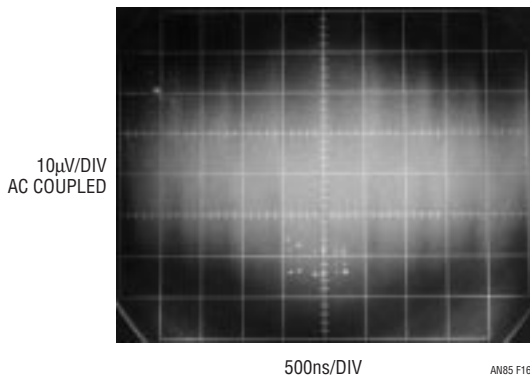


Figure 16. Effect of 12" Voltmeter Probe on VCO Varactor Input. Coaxially Connected 'Scope Probe is in Use. 2.5 \times Measurement Error Referred to Figure 11 Results

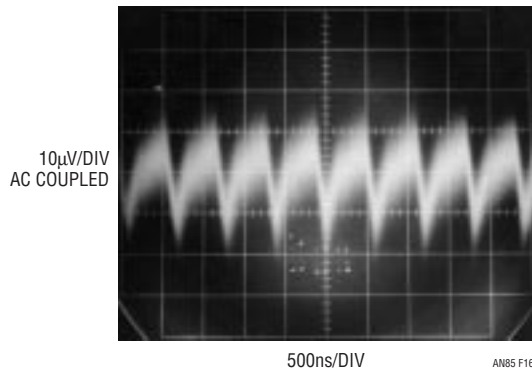
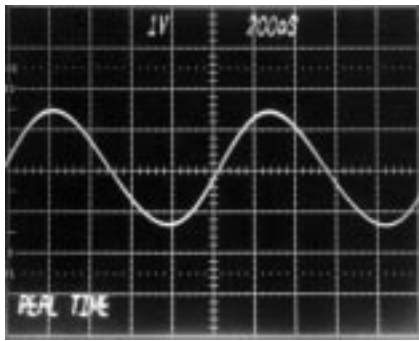


Figure 17. Oscilloscope Trigger Channel Probe at LT1613 SW Pin Causes 50% Measurement Error vs Figure 11

Frequency-Domain Performance

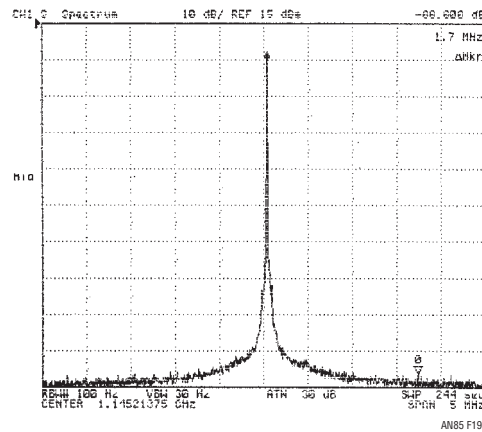
Although the varactor bias noise amplitude measurements are critical, it is difficult to correlate them with frequency-domain performance. Varactor bias noise amplitude translates into spurious VCO outputs and that is the measurement of ultimate concern. Although it is possible to view the GHz range VCO on an oscilloscope (Figure 18), this time domain measurement lacks adequate sensitivity to detect spurious activity. A spectrum analyzer is required. Figure 19, a spectral plot of VCO output, shows a center frequency of 1.14GHz, with no

apparent spurious activity within the ≈ 90 dB measurement noise floor. A marker has been placed at 1.7MHz (3.5 divisions from center), corresponding to the LT1613's switching frequency. No readily distinguishable activity is apparent at about -90 dBc. Succeeding figures "sanity check" this performance by systematically degrading the circuit and noting results. In Figure 20, the VCO varactor input's RC filter has been replaced with a direct connection. Now the 1.7MHz spurious outputs are easily seen, about -62 dBc. In Figure 21, a 12" voltmeter lead as been connected to the measurement point, resulting in a 4dB



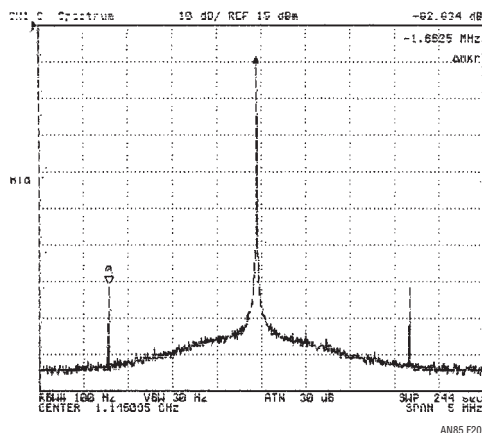
AN85 F18

Figure 18. GHz Range VCO Output is Viewable on Oscilloscope, But Spurious Activity is Undetectable. Spectral Measurements Are Required



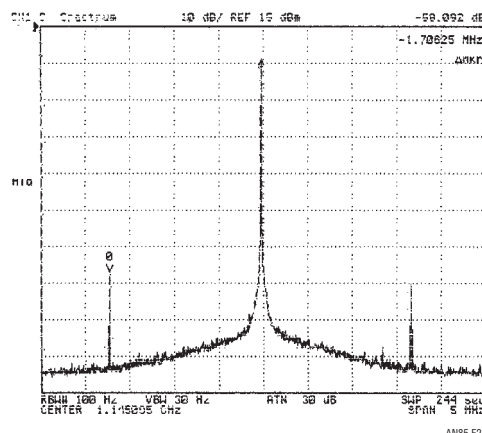
AN85 F19

Figure 19. HP-4396B Spectrum Analyzer Indicates Spurious Outputs at Least -90 dBc Referred to 1.14GHz VCO Center Frequency



AN85 F20

Figure 20. "Sanity Checking" Figure 19's Results by Replacing RC Filter at VCO Varactor Input with Direct Connection. LT1613 1.7MHz Switching Frequency Related Activity Appears at -62 dBc



AN85 F21

Figure 21. Similar Measurement Conditions to Previous Figure with 12" Voltmeter Probe Added. "Spurs" Increase by 4dB to -58 dBc

Application Note 85

degradation, to about -58dBc . Figure 22 shows pronounced effects due to poor LT1613 layout (power ground pin routed circuitously, rather than directly, back to input common) and component choice (lossy capacitor substituted for C2). Spurious activity jumps to -48dBc . In Figure 23 proper layout and components are used, but the varactor bias line has been placed in close proximity to switching inductor L1. Additionally, the bias line and RC filter components have been distanced from the ground plane. The resultant electromagnetic pickup and increase in bias line effective inductance cause

1.7MHz “spurs” at -54dBc . Additional harmonically related activity, although less severe, is also apparent. Figure 24 indicates favorable results when the bias line and RC filter are restored to their proper orientation. The plot is essentially identical to Figure 19. The lesson here is clear. Layout and measurement practice are at least as important as circuit design. As always, the “hidden schematic” dominates performance.⁸

Note 8: Charly Gullett of Intel Corporation originated the quoted descriptive, an author favorite.

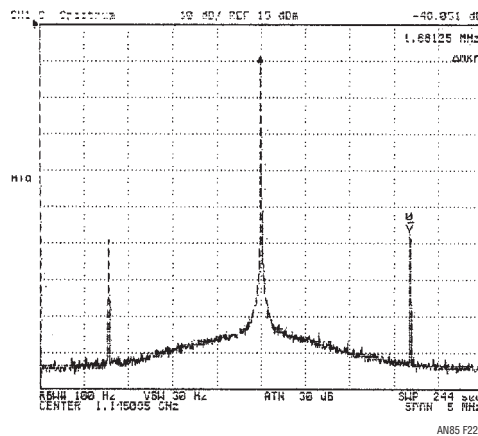


Figure 22. Deliberate Degradation of LT1613's Grounding Scheme and Output Capacitor Raise Spurious Outputs to -48dBc

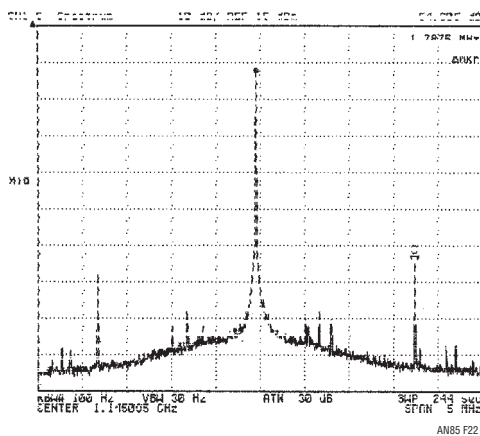


Figure 23. Results with Varactor Bias Line Deliberately Routed Near LT1613's Switching Inductor, and RC Filter Components Lifted from Ground Plane. 1.7MHz “Spurs” at -54dBc ; Other Harmonically Related Components Also Appear

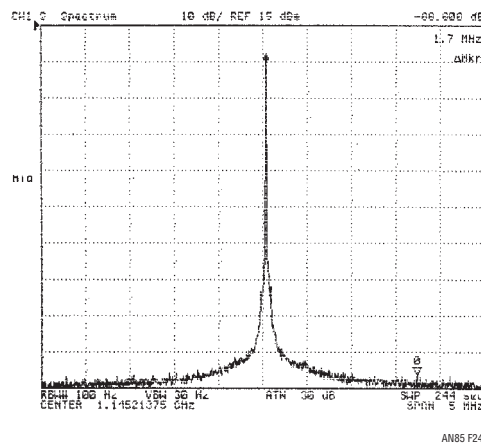


Figure 24. Varactor Bias Line and RC Filter Replaced in Proper Orientation. Figure 19's Silence is Restored

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2. Williams, Jim, "A Monolithic Switching Regulator with 100µV Output Noise," Linear Technology Corporation, Application Note 70, October 1997.
3. Williams, Jim, "High Speed Amplifier Techniques," Linear Technology Corporation, Application Note 47, August 1991.
4. Hurlock, Les, "ABCs of Probes," Tektronix, Inc., 1990
5. McAbel, W. E., "Probe Measurements," Tektronix, Inc., 1971.

APPENDIX A

The following section, excerpted with permission from Zetex Application Note 9 (see Reference 1), reviews theoretical considerations of varactor diodes.

ZETEX VARIABLE CAPACITANCE DIODES

Neil Chadderton, Zetex plc

Background

The varactor diode is a device that is processed so to capitalise on the properties of the depletion layer of a P-N diode. Under reverse bias, the carriers in each region (holes in the P type and electrons in the N type) move away from the junction, leaving an area that is depleted of carriers. Thus a region that is essentially an insulator has been created, and can be compared to the classic parallel plate capacitor model. The effective width of this depletion region increases with reverse bias, and so the capacitance decreases. Thus the depletion layer effectively creates a voltage dependent junction capacitance, that can be varied between the forward conduction region and the reverse breakdown voltage (typically +0.7V to -35V respectively for the ZC830 and ZC740 series diodes).

Different junction profiles can be produced that exhibit different Capacitance-Voltage (C-V) characteristics. The Abrupt junction type of example, shows a small range of capacitance due to its diffusion profile, and as a consequence of this is capable of high Q and low distortion, while the Hyperabrupt variety allows a larger change in capacitance for the same range of reverse bias. So called Hyper-hyperabrupt, or octave tuning variable capacitance diodes show a large change in capacitance for a relatively

small change in bias voltage. This is particularly useful in battery powered systems where the available bias voltage is limited.

The varactor can be modelled as a variable capacitance (C_{jv}), in series with a resistance (R_s). (Please refer to Figure A1.)

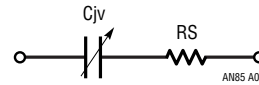


Figure A1. Common Model for the Varactor Diode

The capacitance, C_{jv} , is dependent upon the reverse bias voltage, the junction area, and the doping densities of the semiconductor material, and can be described by:

$$C_{jv} = \frac{C_{j0}}{(1 + V_r/\phi)^N}$$

where:

C_{j0} = Junction capacitance at 0V

C_{jv} = Junction capacitance at applied bias voltage V_r

V_r = Applied bias voltage

ϕ = Contact potential

N = Power law of the junction or slope factor

The series resistance exists as a consequence of the remaining undepleted semiconductor resistance, a contribution due to the die substrate, and a small lead and package component, and is foremost in determining the performance of the device under RF conditions.

Application Note 85

This follows, as the quality factor, Q, is given by:

$$Q = \frac{1}{2\pi f C_{jv} R_S}$$

where:

C_{jv} = Junction capacitance at applied bias voltage V_r

R_S = Series Resistance

f = Frequency

So, to maximise Q, R_S must be minimised. This is achieved by the use of an epitaxial structure so minimising the amount of high resistivity material in series with the junction.

Note: Zetex has produced a set of SPICE models to enable designers to simulate their circuits in SPICE, PSPICE and similar simulation packages. The models use a version of the above capacitance equation and so the model parameters may also be of interest for other software packages. Information is also provided to allow inclusion of parasitic elements to the model. These models are available on request, from any Zetex sales office.

Important Parameters

This section reviews the important characteristics of varactor diodes with particular reference to the Zetex range of variable capacitance diodes.

The characteristic of prime concern to the designer is the Capacitance-Voltage relationship, illustrated by a C-V curve, and expressed at a particular voltage by C_x , where x is the bias voltage. The C-V curve summarises the range of useful capacitance, and also shows the shape of the relationship, which may be relevant when a specific response is required. Figures A2a, A2b and A2c show families of C-V curves for the ZC740-54 (Abrupt), ZC830-6 (Hyperabrupt), and ZC930 (Hyper-hyperabrupt) ranges respectively. Obviously, the choice of device type depends upon the application, but aspects to consider include: the range of frequencies the circuit must operate with, and hence an appropriate capacitance range; the available bias voltage; and the required response.

The capacitance ratio, commonly expressed as C_x/C_y (where x and y are bias voltages), is a useful parameter that shows how quickly the capacitance changes with applied bias voltage. So, for an Abrupt junction device, a

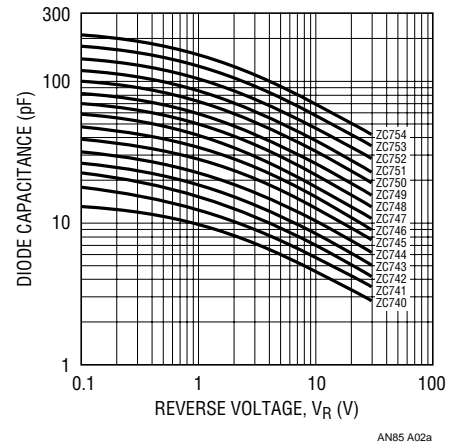


Figure A2a. Typical Capacitance-Voltage Characteristics for the ZC740-54 Range

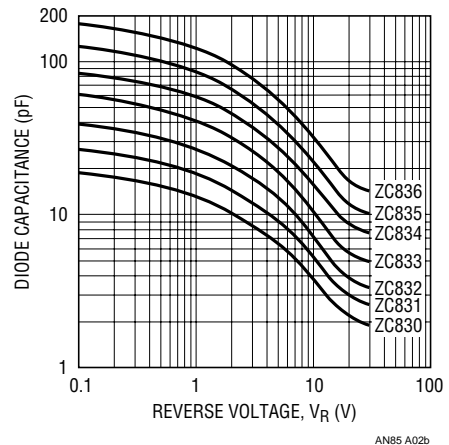


Figure A2b. Typical Capacitance-Voltage Characteristics for the ZC830-6 Range

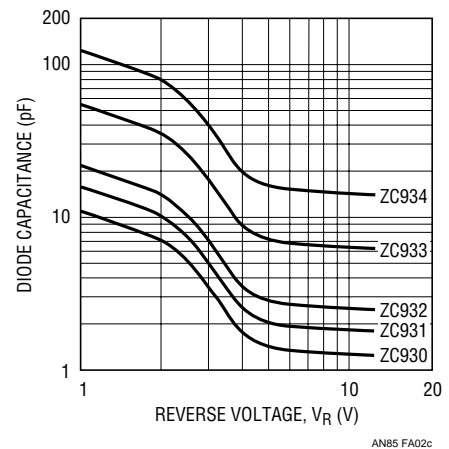


Figure A2c. Typical Capacitance-Voltage Characteristics for the ZC930-4 Range

C2/C20 figure of 2.8 may be typical, whereas a C2/C20 ratio of 6 may be expected for a Hyperabrupt device. This feature of the Hyperabrupt variety can be particularly important when assessing devices for battery-powered applications, where the bias voltage range may be limited. In this instance, the ZC930 series that feature a better than 2:1 tuning range for a 0 to 6V bias may be of particular interest.

The quality factor, Q , at a particular condition is a useful parameter in assessing the performance of a device with respect to tuned circuits, and the resulting loaded Q .

Zetex guarantees a minimum Q at test conditions of 50MHz, and a relatively low V_R of 3 or 4V, and ranges 100 to 450 depending on device type.

The specified V_R is very important in assessing this parameter, because as well as the C-V dependence as detailed previously, a significant part of the series resistance (R_S), is due to the remaining undepleted epitaxial layer, which is also dependant upon V_R . This R_S - V_R relationship is shown in Figure A3 for the ZC830, ZC833 and ZC836 Hyperabrupt devices, measured at frequencies of 470MHz, 300MHz and 150MHz respectively, and also serves to illustrate the excellent performance of Zetex Variable Capacitance Diodes at VHF and UHF.

Also of interest, with respect to stability, is the temperature coefficient of capacitance, as capacitance changes with V_R , and is shown for the three ranges in Figures A4a, A4b and A4c respectively.

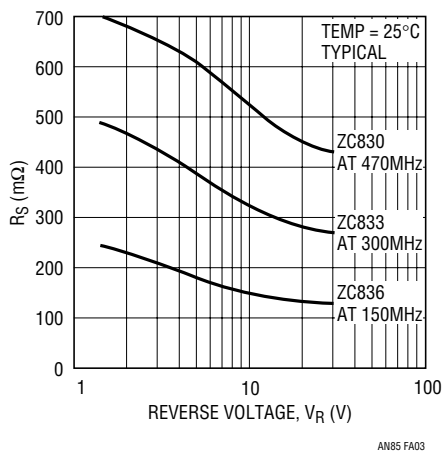


Figure A3. Typical R_S vs V_R Relationship for ZC830 Series Diodes

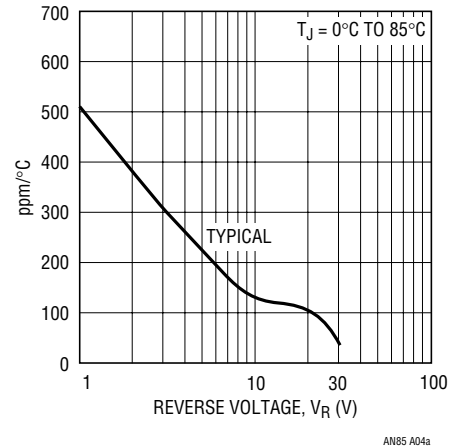


Figure A4a. Temperature Coefficient of Capacitance vs V_R for the ZC740 Series

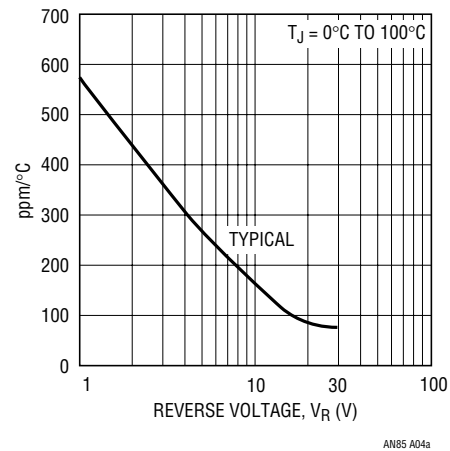


Figure A4b. Temperature Coefficient of Capacitance vs V_R for the ZC830 Series

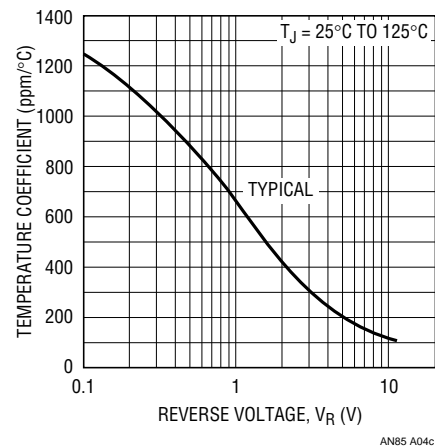


Figure A4c. Temperature Coefficient of Capacitance vs V_R for the ZC930 Series

Application Note 85

The reverse breakdown voltage, $V(BR)$ also has a bearing on device selection, as this parameter limits the maximum V_R that may be used when biasing for minimum capacitance. Zetex variable capacitance diodes typically possess a $V(BR)$ of 35V.

The maximum frequency of operation will depend on the required capacitance and the series resistance (and hence useful Q), that is possessed by a particular device type, but also of consequence are the parasitic components

exhibited by the device package. These depend on the size, material and construction of the package. For example, the Zetex SOT-23 package has a typical stray capacitance of 0.08pF, and a total lead inductance of 2.8nH, while the E-line package shows less than 0.2pF and 5nH respectively. These low values allow a wide frequency application, for example, the ZC830 and ZC930 series, configured as series pairs are ideal for low cost microwave designs extending to 2.5GHz and above.

APPENDIX B

PREAMPLIFIER AND OSCILLOSCOPE SELECTION

The low level measurements described require some form of preamplification for the oscilloscope. Current generation oscilloscopes rarely have greater than 2mV/DIV sensitivity, although older instruments offer more capability. Figure B1 lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These units feature wideband, low noise performance. It is particularly significant that many of these instruments are no longer produced. This is in keeping with current instrumentation trends, which emphasize digital signal acquisition as opposed to analog measurement capability.

The monitoring oscilloscope should have adequate bandwidth and exceptional trace clarity. In the latter regard high quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments is well-suited to low level noise measurement.¹ The digitizing uncertainties and raster scan limitations of DSOs impose display resolution penalties. Many DSO displays will not even register the small levels of switching-based noise.

Note 1: In our work we have found Tektronix types 454, 454A, 547 and 556 excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise floor limited background.

INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	BANDWIDTH	MAXIMUM SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Amplifier	Hewlett-Packard	461A	150MHz	Gain = 100	Secondary Market	50Ω Input, Stand-Alone
Differential Amplifier	Preamble	1855	100MHz	Gain = 10	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Tektronix	1A7/1A7A	1MHz	10μV/DIV	Secondary Market	Requires 500 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	7A22	1MHz	10μV/DIV	Secondary Market	Requires 7000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	5A22	1MHz	10μV/DIV	Secondary Market	Requires 5000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	ADA-400A	1MHz	10μV/DIV	Current Production	Stand-Alone with Optional Power Supply, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 1000	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Stanford Research Systems	SR-560	1MHz	Gain = 50000	Current Production	Stand-Alone, Settable Bandstops, Battery or Line Operation

Figure B1. Some Applicable High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Bandwidth, Sensitivity and Availability

APPENDIX C

PROBING AND CONNECTION TECHNIQUES FOR LOW LEVEL, WIDEBAND SIGNAL INTEGRITY¹

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. The low level, wideband measurements demand care in routing signals to test instrumentation.

Ground Loops

Figure C1 shows the effects of a ground loop between pieces of line-powered test equipment. Small current flow between test equipment's nominally grounded chassis creates 60Hz modulation in the measured circuit output. *This problem can be avoided by grounding all line powered test equipment at the same outlet strip or otherwise ensuring that all chassis are at the same ground potential. Similarly, any test arrangement that permits circuit current flow in chassis interconnects must be avoided.*

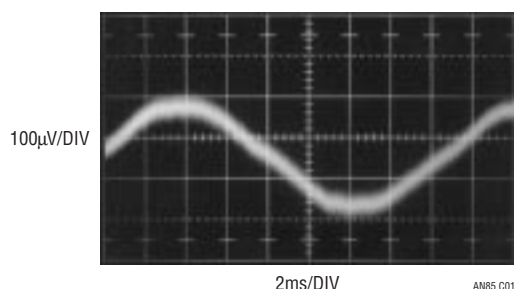


Figure C1. Ground Loop Between Pieces of Test Equipment Induces 60Hz Display Modulation

Pickup

Figure C2 also shows 60Hz modulation of the noise measurement. In this case, a 4-inch voltmeter probe at the feedback input is the culprit. *Minimize the number of test connections to the circuit and keep leads short.*

Poor Probing Technique

Figure C3's photograph shows a short ground strap affixed to a scope probe. The probe connects to a point which provides a trigger signal for the oscilloscope. Circuit output noise is monitored on the oscilloscope via the coaxial cable shown in the photo.

Note 1: Veterans of LTC Application Notes, a hardened crew, will recognize this Appendix from AN70 (see Reference 2). Although that publication concerned considerably more wideband noise measurement, the material is directly applicable to this effort. As such, it is reproduced here for reader convenience.

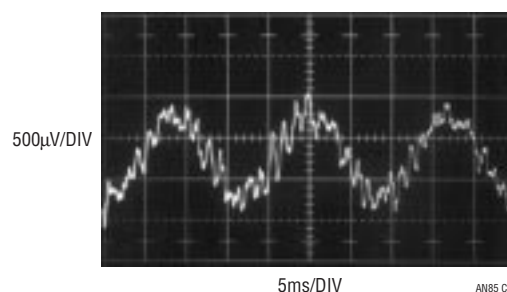


Figure C2. 60Hz Pickup Due to Excessive Probe Length at Feedback Node

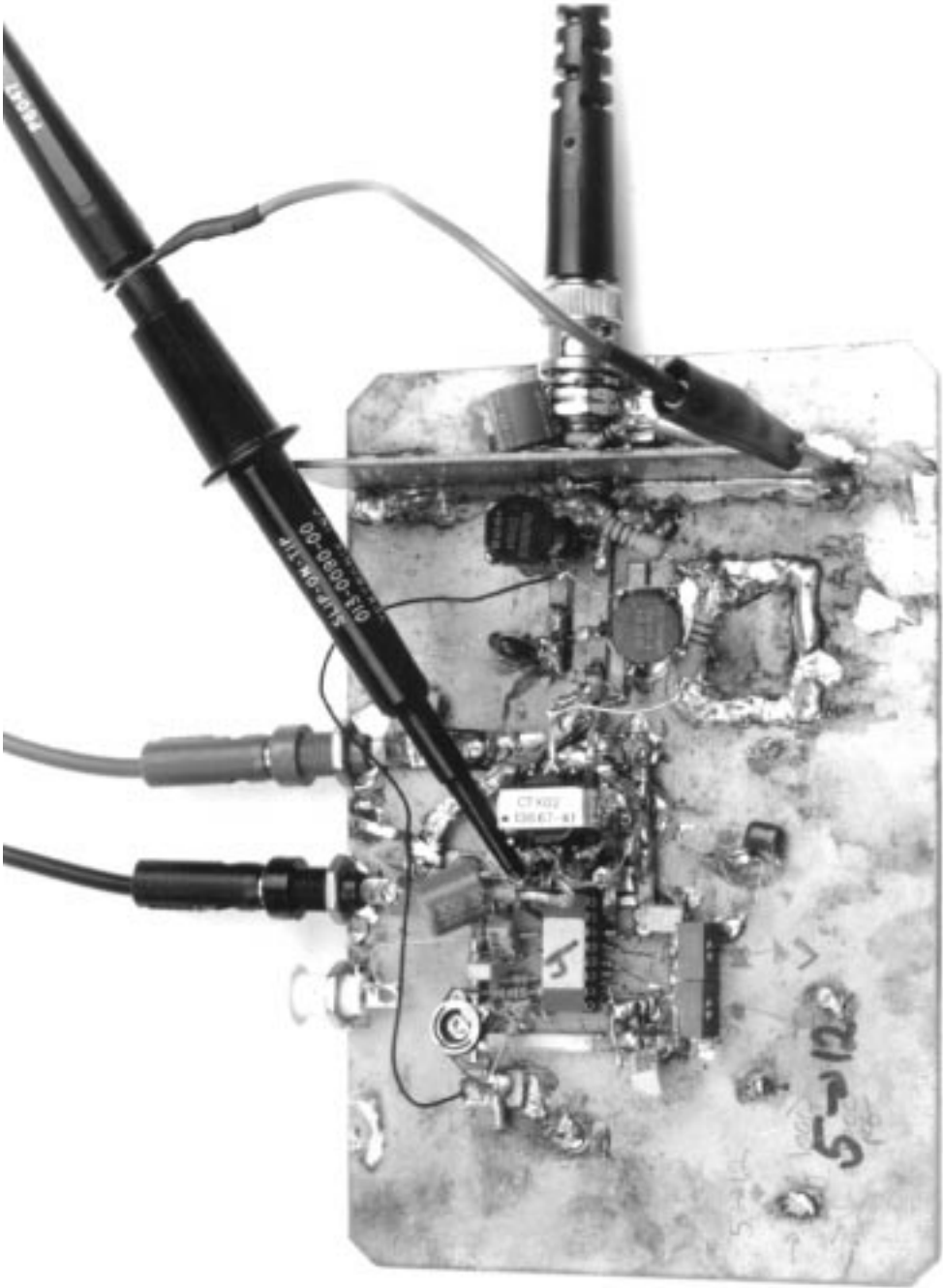


Figure C3. Poor Probing Technique. Trigger Probe Ground Lead Can Cause Ground Loop-Induced Artifacts to Appear in Display

Figure C4 shows results. A ground loop on the board between the probe ground strap and the ground referred cable shield causes apparent excessive ripple in the display. *Minimize the number of test connections to the circuit and avoid ground loops.*

Violating Coaxial Signal Transmission—Felony Case

In Figure C5, the coaxial cable used to transmit the circuit output noise to the amplifier-oscilloscope has been replaced with a probe. A short ground strap is employed as the probe's return. The error inducing trigger channel probe in the previous case has been eliminated; the 'scope is triggered by a noninvasive, isolated probe.² Figure C6 shows excessive display noise due to breakup of the coaxial signal environment. The probe's ground strap violates coaxial transmission and the signal is corrupted by RF. *Maintain coaxial connections in the noise signal monitoring path.*

Violating Coaxial Signal Transmission—Misdemeanor Case

Figure C7's probe connection also violates coaxial signal flow, but to a less offensive extent. The probe's ground strap is eliminated, replaced by a tip grounding attachment. Figure C8 shows better results over the preceding case, although signal corruption is still evident. *Maintain coaxial connections in the noise signal monitoring path.*

Proper Coaxial Connection Path

In Figure C9, a coaxial cable transmits the noise signal to the amplifier-oscilloscope combination. In theory, this affords the highest integrity cable signal transmission.

Figure C10's trace shows this to be true. The former example's aberrations and excessive noise have disappeared. The switching residuals are now faintly outlined in the amplifier noise floor. *Maintain coaxial connections in the noise signal monitoring path.*

Direct Connection Path

A good way to verify there are no cable-based errors is to eliminate the cable. Figure C11's approach eliminates all cable between breadboard, amplifier and oscilloscope. Figure C12's presentation is indistinguishable from Figure C10, indicating no cable-introduced infidelity. *When results seem optimal, design an experiment to test them. When results seem poor, design an experiment to test them. When results are as expected, design an experiment to test them. When results are unexpected, design an experiment to test them.*

Test Lead Connections

In theory, attaching a voltmeter lead to the regulator's output should not introduce noise. Figure C13's increased noise reading contradicts the theory. The regulator's output impedance, albeit low, is not zero, especially as frequency scales up. The RF noise injected by the test lead works against the finite output impedance, producing the 200 μ V of noise indicated in the figure. If a voltmeter lead must be connected to the output during testing, it should be done through a 10k Ω -10 μ F filter. Such a network eliminates Figure C13's problem while introducing minimal error in the monitoring DVM. *Minimize the number of test lead connections to the circuit while checking noise. Prevent test leads from injecting RF into the test circuit.*

Note 2: To be discussed. Read on.

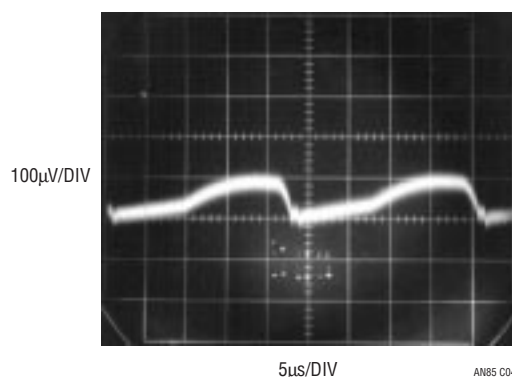


Figure C4. Apparent Excessive Ripple Results from Figure C3's Probe Misuse. Ground Loop on Board Introduces Serious Measurement Error

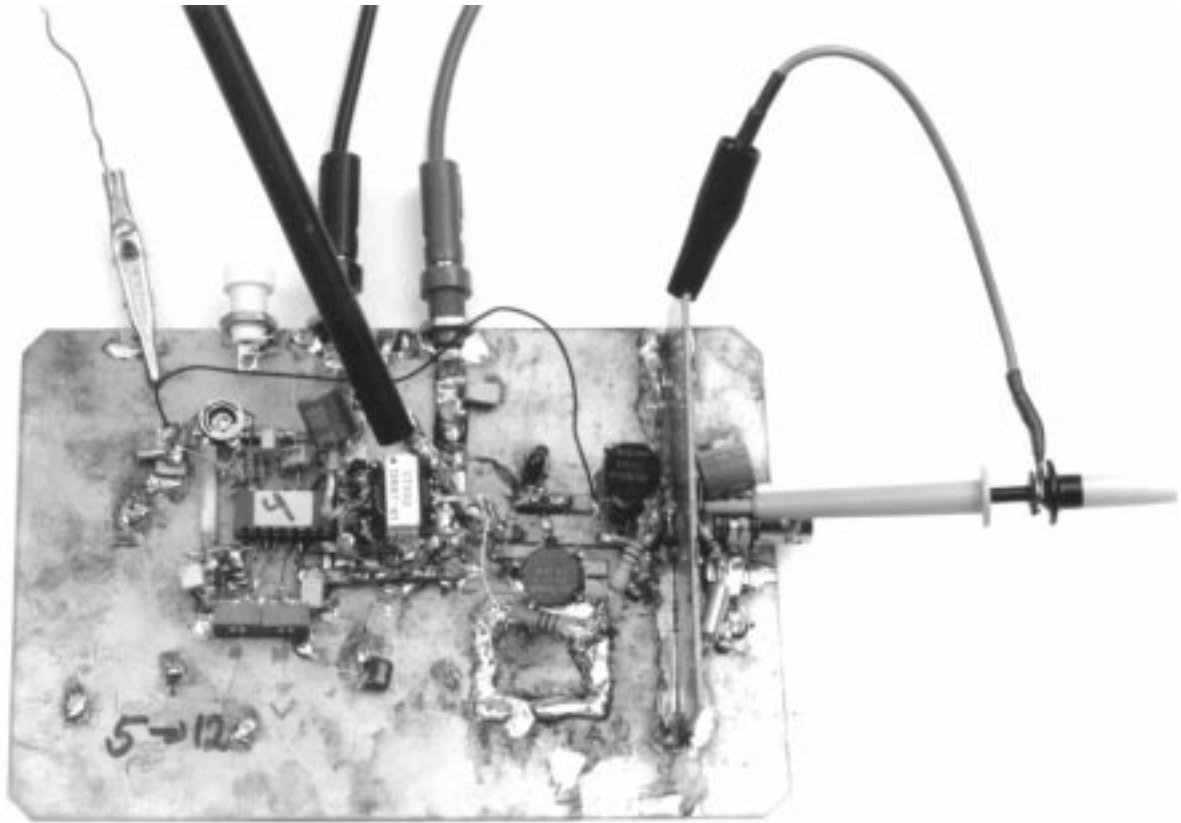


Figure C5. Floating Trigger Probe Eliminates Ground Loop, But Output Probe Ground Lead (Photo Upper Right) Violates Coaxial Signal Transmission

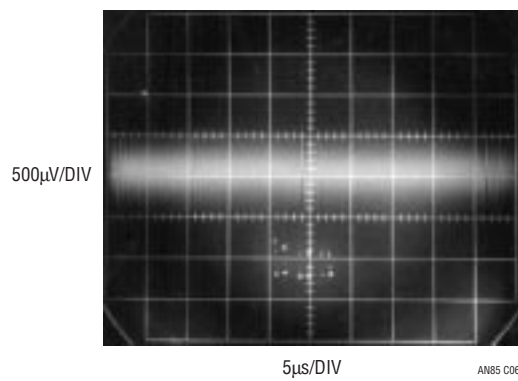


Figure C6. Signal Corruption Due to Figure C5's Noncoaxial Probe Connection

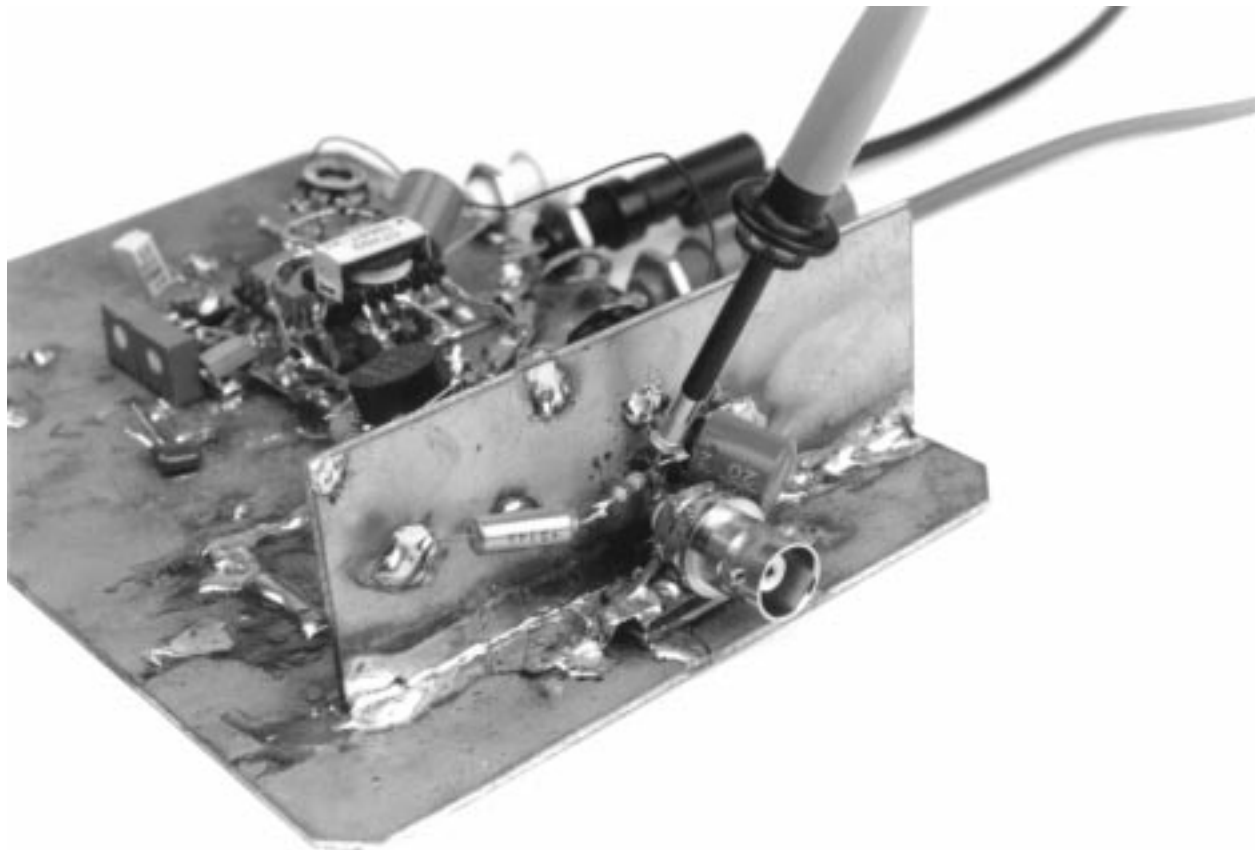


Figure C7. Probe with Tip Grounding Attachment Approximates Coaxial Connection

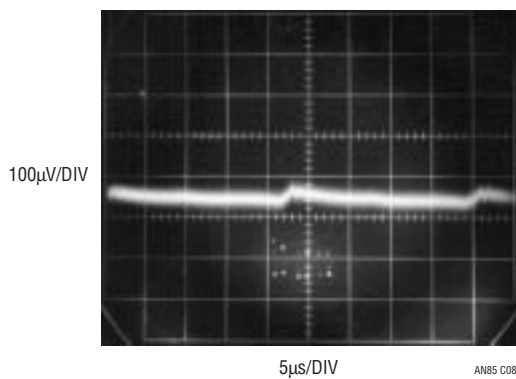


Figure C8. Probe with Tip Grounding Attachment Improves Results. Some Corruption is Still Evident

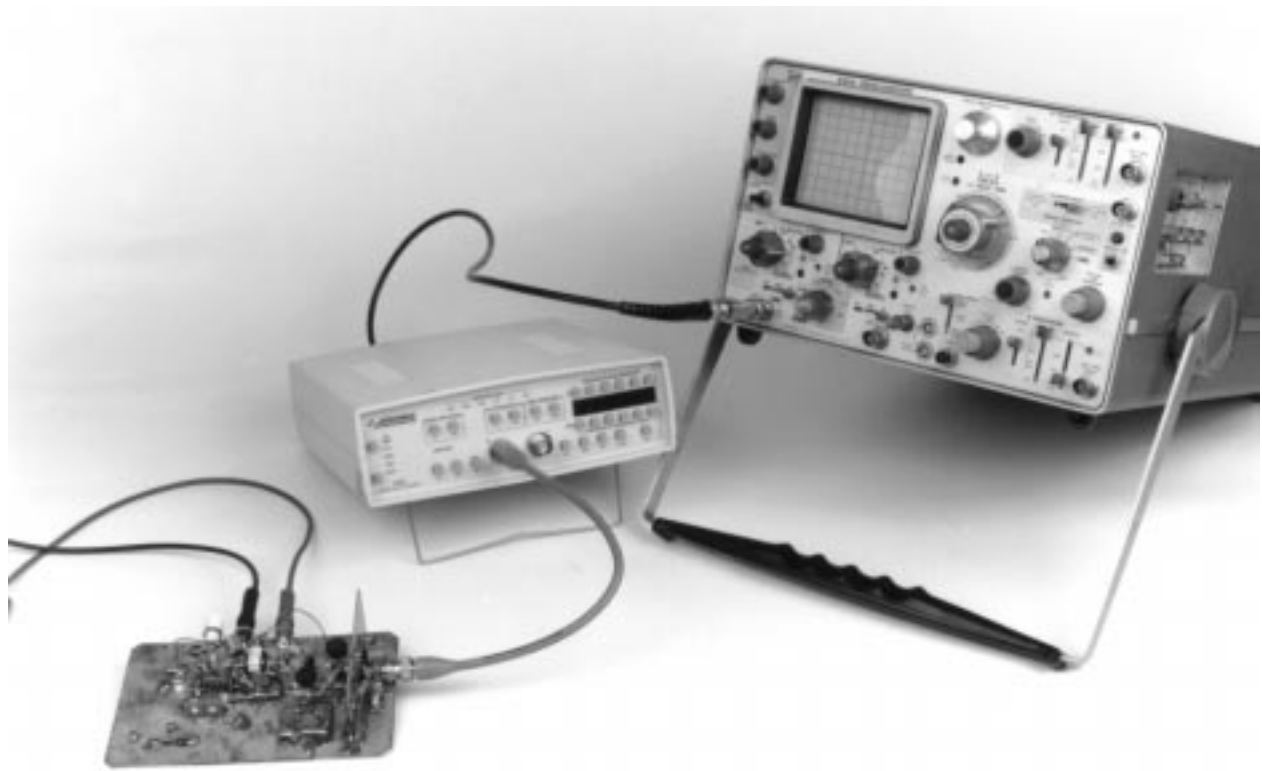


Figure C9. Coaxial Connection Theoretically Affords Highest Fidelity Signal Transmission

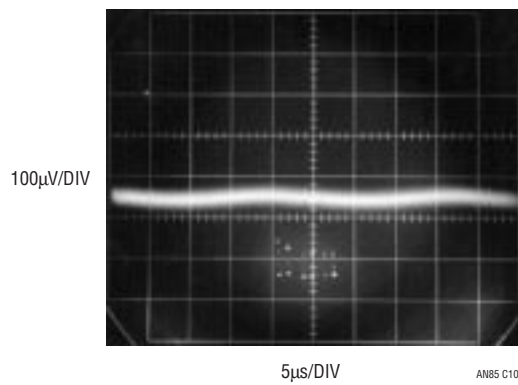


Figure C10. Life Agrees with Theory. Coaxial Signal Transmission Maintains Signal Integrity. Switching Residuals Are Faintly Outlined in Amplifier Noise

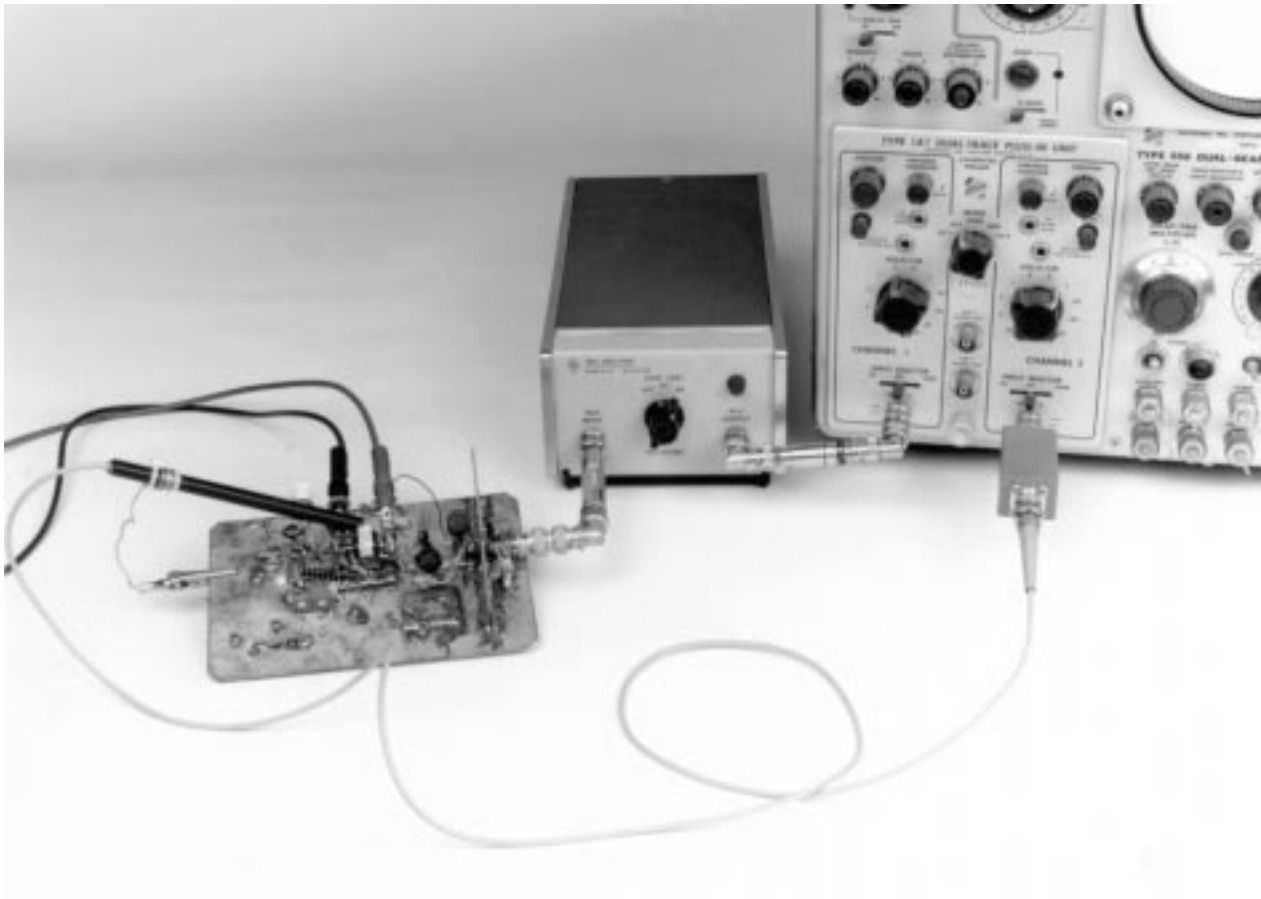


Figure C11. Direct Connection to Equipment Eliminates Possible Cable-Termination Parasitics, Providing Best Possible Signal Transmission

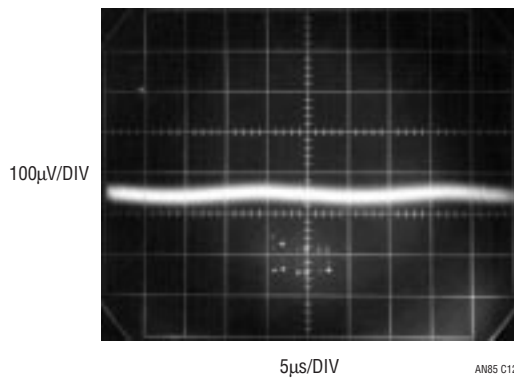


Figure C12. Direct Connection to Equipment Provides Identical Results to Cable-Termination Approach. Cable and Termination Are Therefore Acceptable

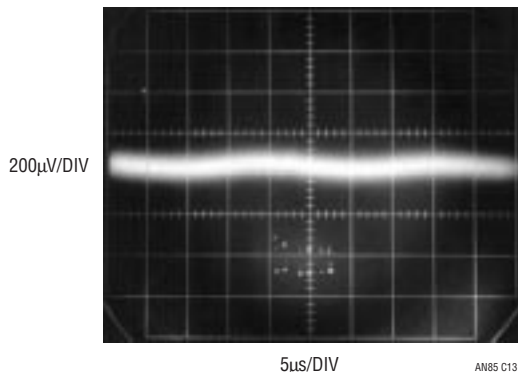


Figure C13. Voltmeter Lead Attached to Regulator Output Introduces RF Pickup, Multiplying apparent Noise Floor

Isolated Trigger Probe

The text associated with Figure C5 somewhat cryptically alluded to an “isolated trigger probe.” Figure C14 reveals this to be simply an RF choke terminated against ringing. The choke picks up residual radiated field, generating an isolated trigger signal. This arrangement furnishes a scope trigger signal with essentially no measurement corruption. The probe’s physical form appears in Figure C15. For good results, the termination should be adjusted for minimum ringing while preserving the highest possible amplitude output. Light compensatory damping produces Figure C16’s output, which will cause poor scope triggering. Proper adjustment results in a more favorable output (Figure C17), characterized by minimal ringing and well-defined edges.

Trigger Probe Amplifier

The field around the switching magnetics is small and may not be adequate to reliably trigger some oscilloscopes. In such cases, Figure C18’s trigger probe amplifier is useful. It uses an adaptive triggering scheme to compensate for variations in probe output amplitude. A stable 5V trigger output is maintained over a 50:1 probe output range. A1, operating at a gain of 100, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2’s emitter capacitor, while the minimum excursion is retained in Q4’s emitter capacitor. The DC value of the midpoint of A1’s

output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal’s excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394’s positive input. The LT1394’s negative input is biased directly from A1’s output. The LT1394’s output, the circuit’s trigger output, is unaffected by >50:1 signal amplitude variations. An X100 analog output is available at A1.

Figure C19 shows the circuit’s digital output (Trace B) responding to the amplified probe signal at A1 (Trace A).

Figure C20 is a typical noise testing setup. It includes the breadboard, trigger probe, amplifier, oscilloscope and coaxial components.

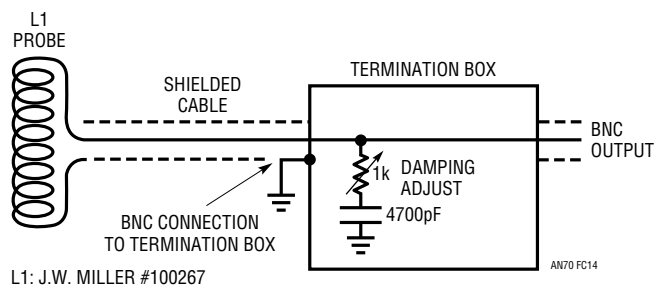


Figure C14. Simple Trigger Probe Eliminates Board Level Ground Loops. Termination Box Components Damp L1’s Ringing Response



Figure C15. The Trigger Probe and Termination Box. Clip Lead Facilitates Mounting Probe, Is Electrically Neutral

Application Note 85

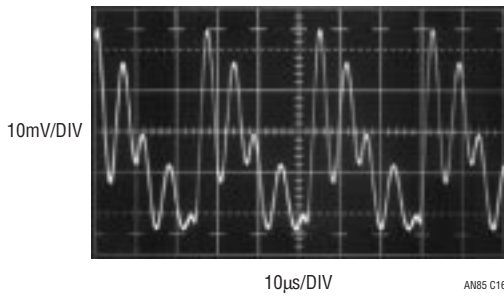


Figure C16. Misadjusted Termination Causes Inadequate Damping. Unstable Oscilloscope Triggering May Result

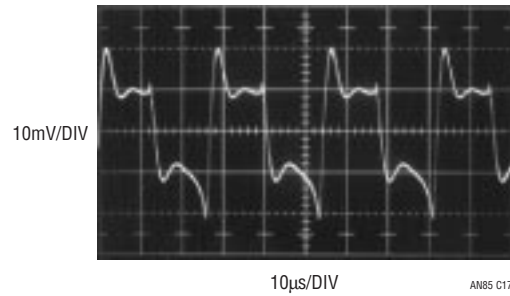


Figure C17. Properly Adjusted Termination Minimizes Ringing with Small Amplitude Penalty

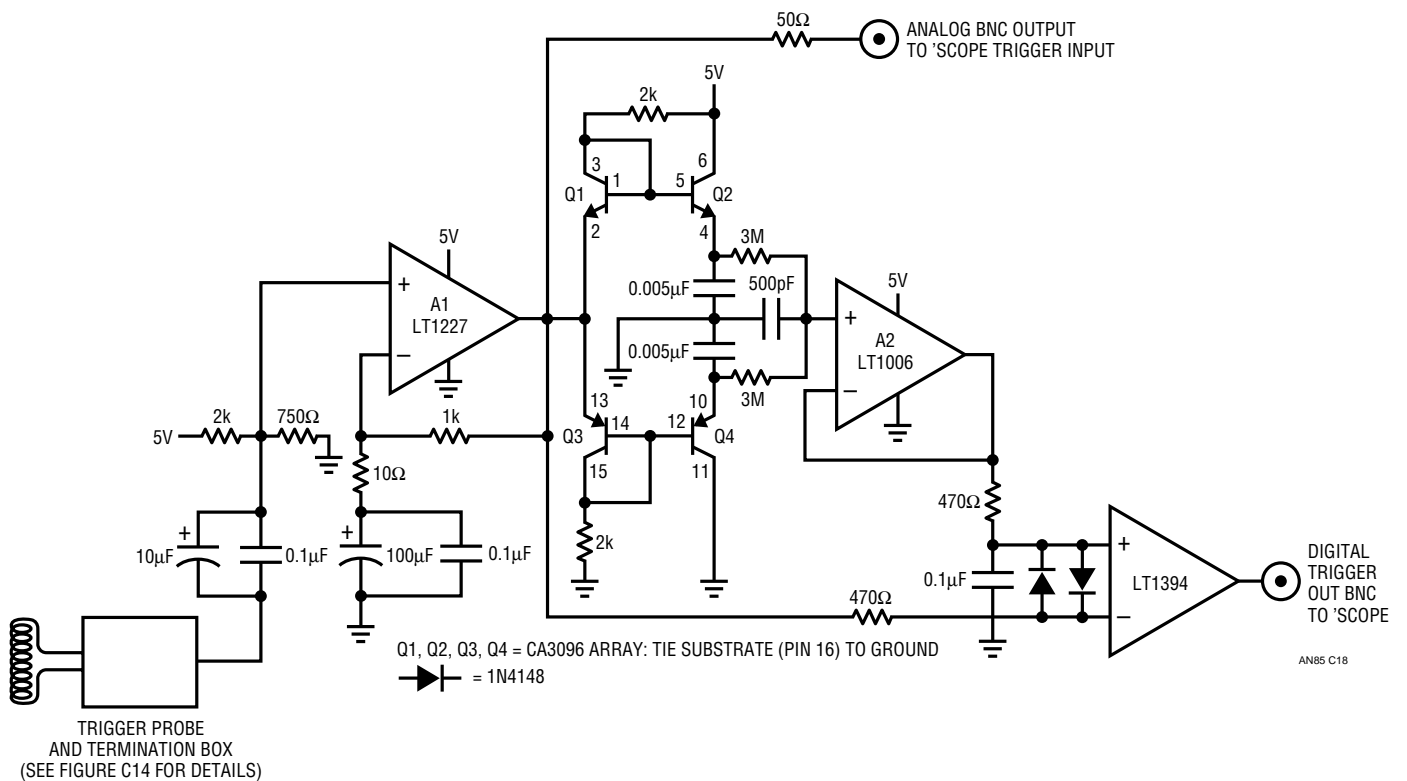


Figure C18. Trigger Probe Amplifier Has Analog and Digital Outputs. Adaptive Threshold Maintains Digital Output Over 50:1 Probe Signal Variations

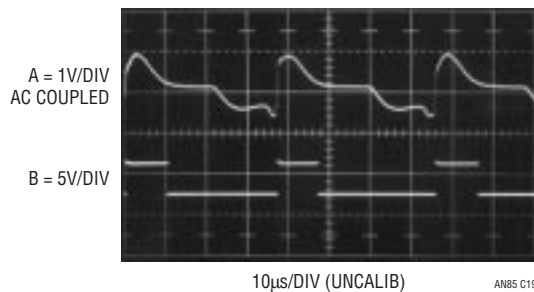


Figure C19. Trigger Probe Amplifier Analog (Trace A) and Digital (Trace B) Outputs

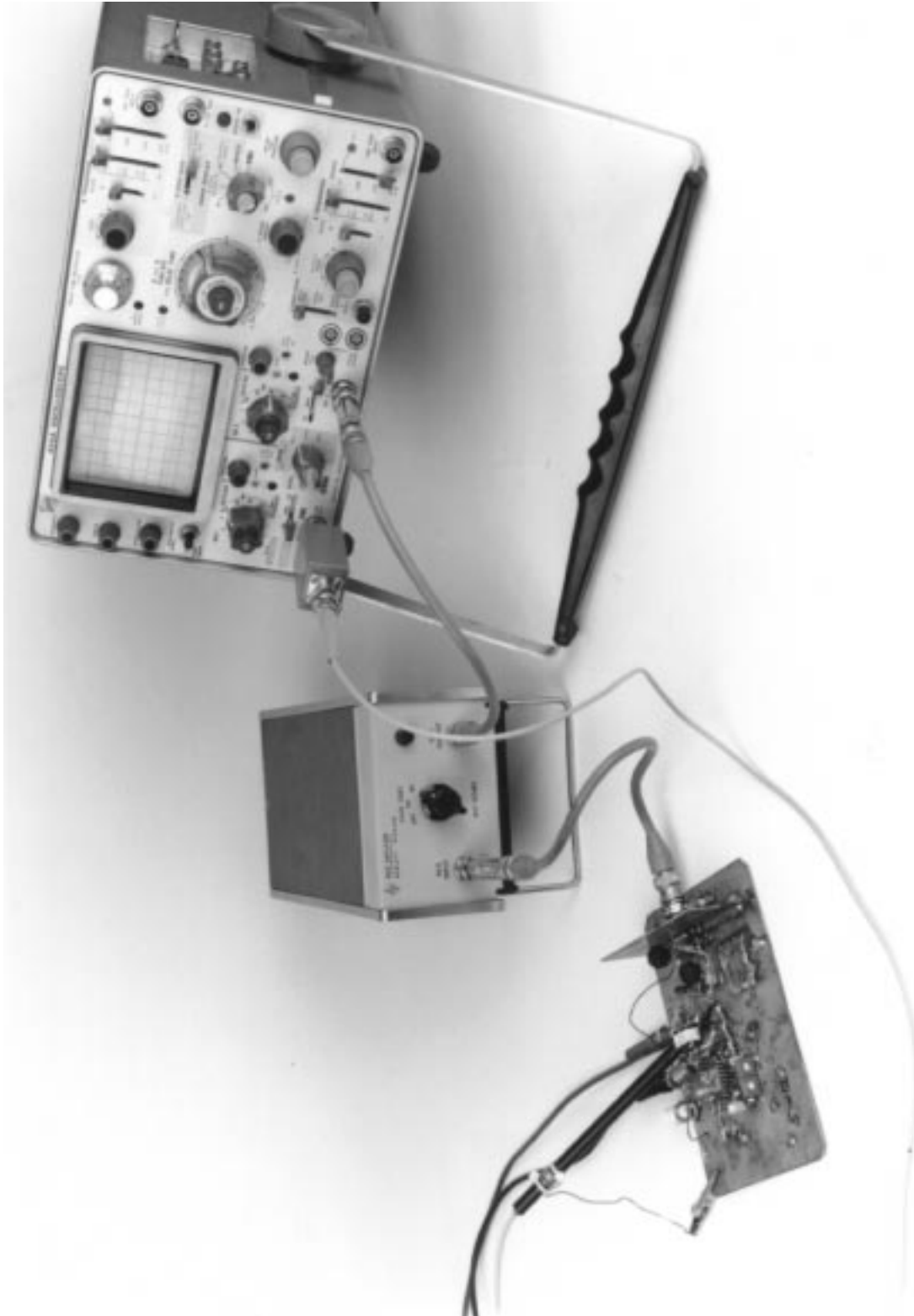
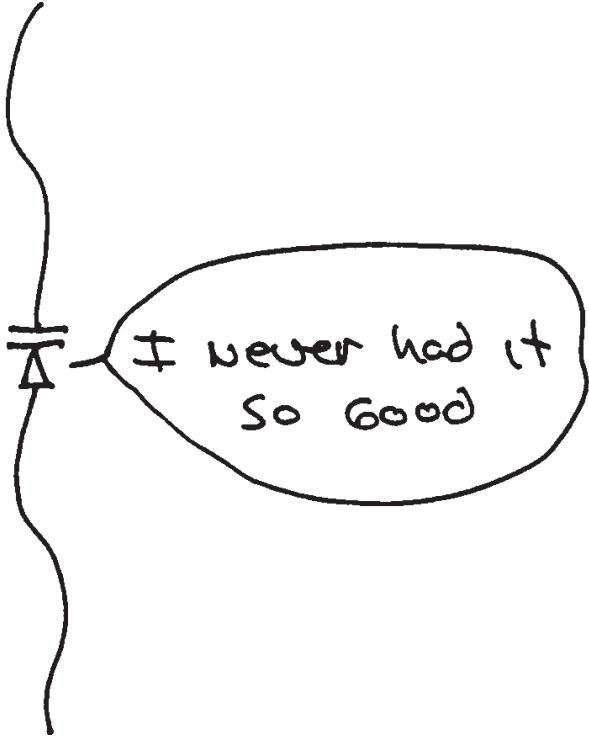


Figure C20. Typical Noise Test Setup Includes Trigger Probe, Amplifier, Oscilloscope and Coaxial Components



Will do

A Standards Lab Grade 20-Bit DAC with 0.1ppm/°C Drift

The Dedicated Art of Digitizing One Part Per Million

Jim Williams
 J. Brubaker
 P. Copley
 J. Guerrero
 F. Oprescu

INTRODUCTION

Significant progress in high precision, instrumentation grade D-to-A conversion has recently occurred. Ten years ago 12-bit D-to-A converters (DACs) were considered premium devices. Today, 16-bit DACs are available and increasingly common in system design. These are true precision devices with less than 1LSB linearity error and 1ppm/°C drift.¹ Nonetheless, there are DAC applications that require even higher performance. Automatic test equipment, instruments, calibration apparatus, laser trimmers, medical electronics and other applications often require DAC accuracy beyond 16 bits. 18-bit DACs have been produced in circuit assembly form, although they are expensive and require frequent calibration. 20 and even 23+ (0.1ppm!) bit DACs are represented by manually switched Kelvin-Varley dividers. These devices, although amazingly accurate, are large, slow and extremely costly. Their use is normally restricted to standards labs.² A useful development would be a practical, 20-bit (1ppm) DAC that is easily constructed and does not require frequent calibration.

20-Bit DAC Architecture

Figure 1 diagrams the architecture of a 20-bit (1ppm) DAC. This scheme is based on the availability of a true 1ppm analog-to-digital converter with scale and zero drifts below 0.02ppm/°C. This device, the LTC[®]2400, is used as a feedback element in a digitally corrected loop to realize a 20-bit DAC.³

In practice, the “slave” 20-bit DAC’s output is monitored by the “master” LTC2400 A-to-D, which feeds digital information to a code comparator. The code comparator

differences the user input word with the LTC2400 output, presenting a corrected code to the slave DAC. In this fashion, the slave DAC’s drifts and nonlinearity are continuously corrected by the loop to an accuracy determined by the A-to-D converter and V_{REF} .⁴ The sole DAC requirement is that it be monotonic. No other components in the loop need to be stable.

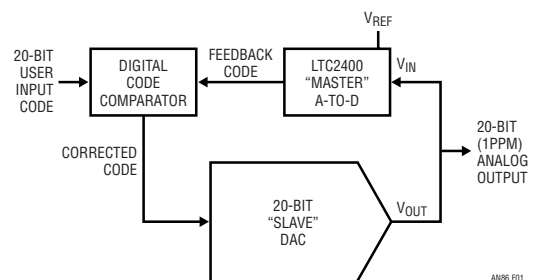


Figure 1. Conceptual Loop-Based 20-Bit DAC. Digital Comparison Allows A-to-D to Correct DAC Errors. LTC2400 A-to-D’s Low Uncertainty Characteristics Permit 1ppm Output Accuracy

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

Note 1: See Appendix A, “A History of High Accuracy Digital-to-Analog Conversion,” for a review of high accuracy digital-to-analog conversion.

Note 2: Consult Appendix C, “Verifying Data Converter Linearity to 1ppm,” for discussion on Kelvin-Varley dividers. Also, see Appendix A, “A History of High Accuracy Digital-to-Analog Conversion.”

Note 3: The LTC2400 analog-to-digital converter is profiled in Appendix B, “The LTC2400—A Monolithic 24-Bit Analog-to-Digital Converter.”

Note 4: D-to-A converters have been placed in loops to make A-to-D converters for a long time. Here, an A-to-D converter feeds back a loop to form a D-to-A converter. There seems a certain justified symmetry to this development. Turnabout is indeed fair play.

Application Note 86

This loop has a number of desirable attributes. As mentioned, accuracy limitations are set by the A-to-D converter and its reference. No other components need be stable. Additionally, loop behavior averages low order bit indexing and jitter, obviating the loop's inherent small-signal instability. Finally, classical remote sensing may be used or digitally based sensing is possible by placing the A-to-D converter at the load. The A-to-D's SO-8 package and lack of external components makes this digitally incarnated Kelvin sensing scheme practical.⁵

Circuitry Details

Figure 2 is a detailed schematic of the 1ppm DAC. The slave DAC is comprised of two DACs. The upper 16 bits of the code comparator's output are fed to a 16-bit DAC ("MSB DAC"), while the lower bits are converted by a separate DAC ("LSB DAC"). Although a total of 32 bits are presented to the two DACs, there are 8 bits of overlap, assuring loop capture under all conditions. The composite

DACs' resultant 24-bit resolution provides 4 bits of indexing range below the 20th bit, ensuring a stable LSB of 1ppm of scale. A1 and A2 transform the DAC's output currents into voltages, which are summed at A3. A3's scaling is arranged so that the correction loop can always capture and correct any combination of zero- and full-scale errors. A3's output, the circuit output, feeds the LTC2400 A-to-D. The LT[®]1010 provides buffering to drive loads and cables. The A-to-D's digital output is differenced against the input word by the code comparator, which produces a corrected code. This corrected code is applied to the MSB and LSB DACs, closing a feedback loop.⁶ The loop's integrity is determined by A-to-D converter and voltage reference errors.⁷ The resistor and diodes at the 5V powered A-to-D protect it from inadvertent A3 outputs (power up, transient, lost supply, etc.). A4 is a reference inverter and A5 provides a clean ground potential to both DACs.

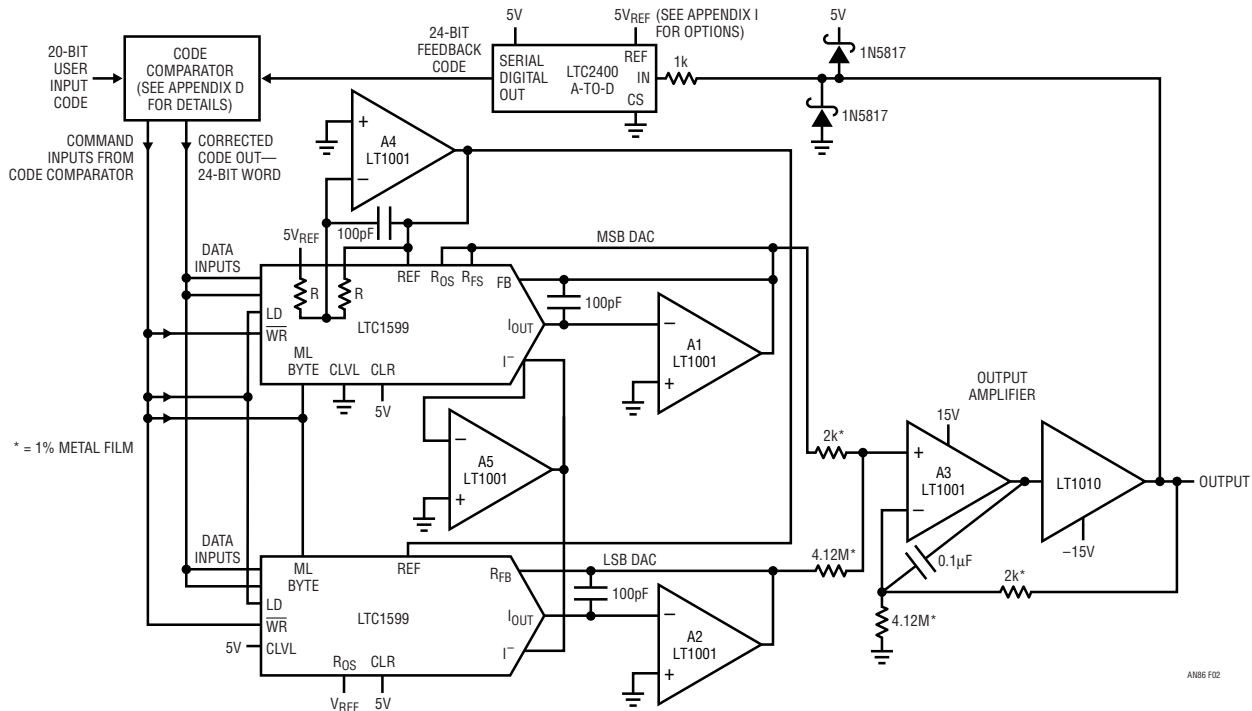


Figure 2. Detail of 1ppm DAC. Composite DAC is comprised of two DAC values summed at output amplifier. LTC2400 A-to-D and code comparator furnish stabilizing feedback

Note 5: One wonders what Lord Kelvin's response would be to the digitization of his progeny. Such uncertainties are the residue of progress.

Note 6: The code comparator is detailed in Appendix D, "A Processor Based Code Comparator."

Note 7: Voltage reference options are discussed in Appendix I, "Voltage References." For tutorial on the LTC2400, refer to Appendix B.

Linearity Considerations

A-to-D linearity determines overall DAC linearity. The A-to-D has about ± 2 ppm nonlinearity. In applications where this error is permissible, it may be ignored. If 1ppm linearity is required, it is obtainable by correcting the residual linearity error with software techniques. Details on LTC2400 linearity and this feature are presented in Appendices D and E.

DC Performance Characteristics

Figure 3 is a plot of linearity vs output code. The data shows linearity is within 1ppm over all codes.⁸ Output noise, measured in a 0.1Hz to 10Hz bandpass, is seen in Figure 4 to be about 0.2LSB.⁹ This measurement is somewhat corrupted by equipment limitations, which set a noise floor of about 0.2 μ V.

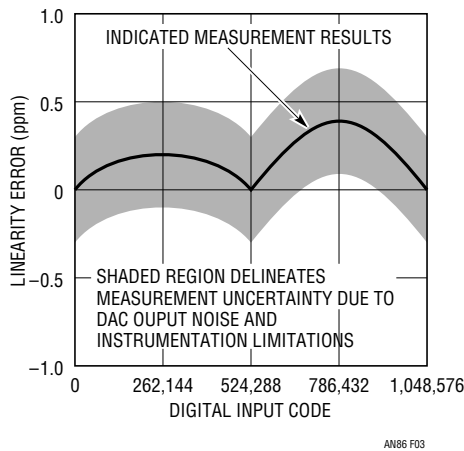


Figure 3. Linearity Plot Shows No Error Outside 1ppm for All Codes

Dynamic Performance

The A-to-D's conversion rate combines with the loop's sampled data characteristic and slow amplifiers to dictate relatively slow DAC response. Figure 5's slow response requires about 150 microseconds.

Figure 6 shows full-scale DAC settling time to within 1ppm ($\pm 5\mu$ V) requires about 1400 milliseconds. A smaller step (Figure 7) of 500 μ V needs only 100 milliseconds to settle within 1ppm.¹⁰

Conclusion

Summarized 1ppm DAC specifications appear in Figure 9. These specifications should be considered guidelines, as the options and variations noted will affect performance. Consult the appropriate appendices for design specifics and trade-offs.

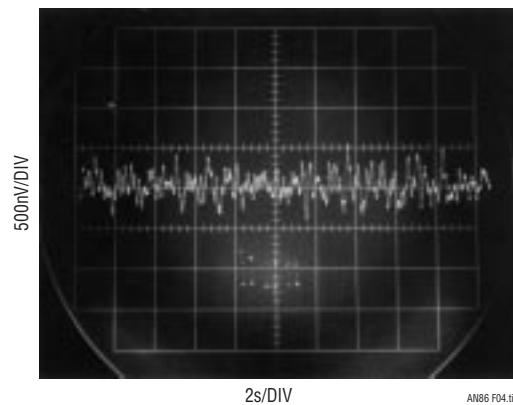


Figure 4. Output Noise Indicates Less Than 1 μ V, About 0.2LSB. Measurement Noise Floor, Due to Equipment Limitations, Is 0.2 μ V

Note 8: Establishing and maintaining confidence in a 1ppm linearity measurement is uncomfortably close to the state of the art. The technique used is shown in Appendix C, "Verifying Data Converter Linearity to 1ppm."

Note 9: Noise measurement considerations appear in Appendix H, "Microvolt Level Noise Measurement."

Note 10: Measuring DAC settling time to 1ppm is by no means straightforward, even at the relatively slow speed involved here. See Appendix G, "Measuring DAC Settling Time."

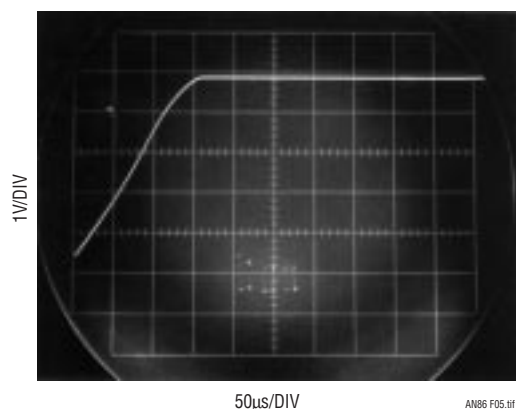


Figure 5. DAC Output Full-Scale Slew Characteristics

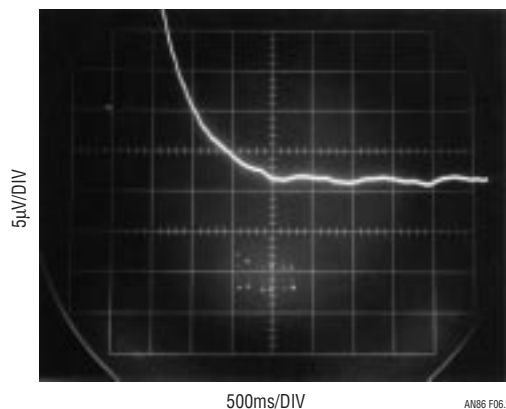


Figure 6. High Resolution Settling Detail After a Full-Scale Step. Settling Time Is 1400 Milliseconds to Within 1ppm ($\pm 5\mu\text{V}$)

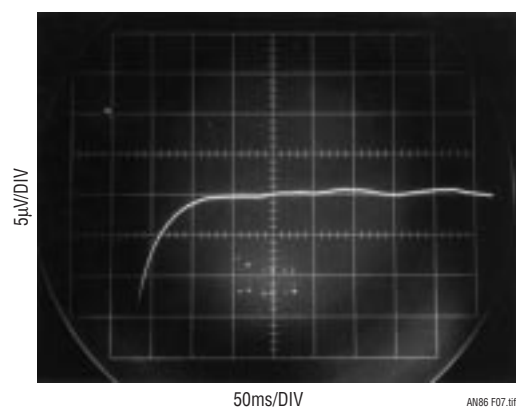


Figure 7. Small Step Settling Time Measures 100 Milliseconds to Within 1ppm ($\pm 5\mu\text{V}$) for a $500\mu\text{V}$ Transition

PARAMETER	SPECIFICATION
Resolution	1ppm
Full-Scale Error	4ppm of V_{REF} (Trimable to 1ppm by V_{REF} Adjustment)
Full-Scale Error Drift	0.04ppm/ $^{\circ}\text{C}$ Exclusive of Reference (0.1ppm/ $^{\circ}\text{C}$ with LTZ1000A Reference ¹)
Offset Error	0.5ppm
Offset Error Drift	0.01ppm/ $^{\circ}\text{C}$
Nonlinearity	$\pm 2\text{ppm}$, Trimmable to Less Than 1ppm^2
Output Noise	0.2ppm ($\approx 0.9\mu\text{V}$, 0.1Hz to 10Hz BW)
Slew Rate	0.033V/ μs
Settling Time—Full-Scale Step	1400 Milliseconds
Settling Time— $500\mu\text{V}$ Step	100 Milliseconds
Output Voltage Range	0V to 5V. For Other Ranges See Note 3

Note 1: See Appendix I

Note 2: See Appendix E

Note 3: See Appendices E and F

Figure 8. Summarized Specifications for the 20-Bit DAC

Note: This Application Note was derived from a manuscript originally prepared for publication in EDN magazine.

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20. Vishay Inc., "Vishay Foil Resistors," Vishay Inc., 1999.

Application Note 86

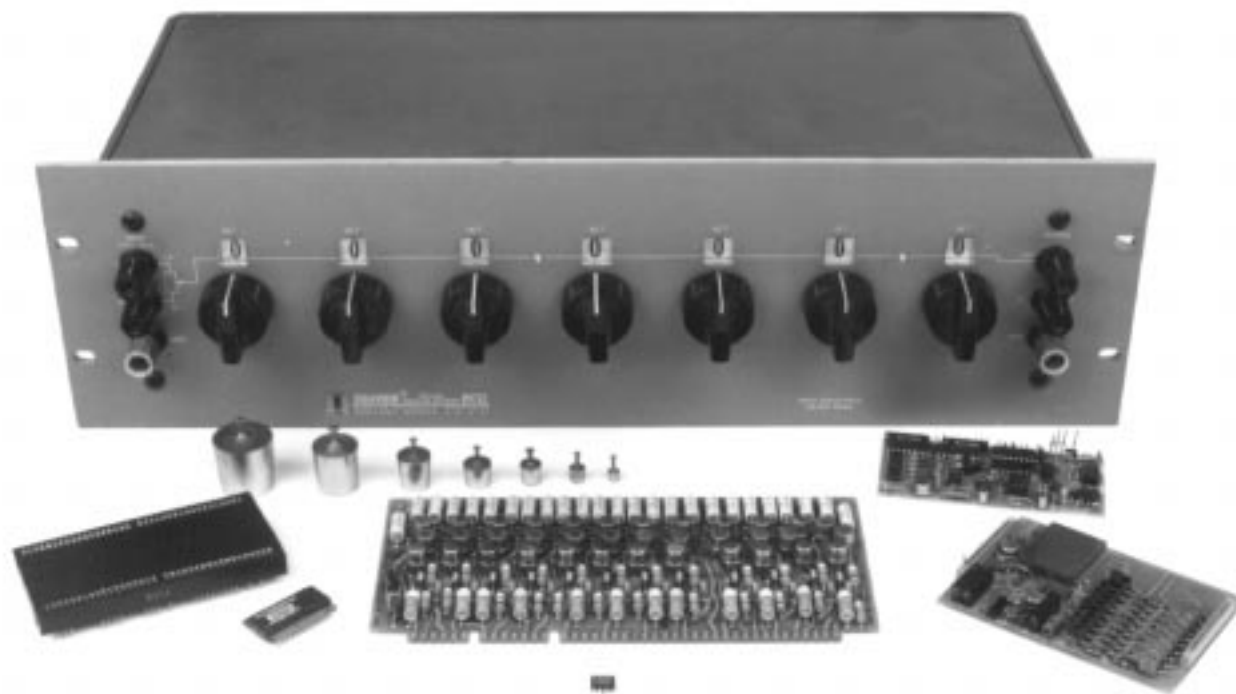
APPENDIX A

A HISTORY OF HIGH ACCURACY DIGITAL-TO-ANALOG CONVERSION

People have been converting digital-to-analog quantities for a long time. Probably among the earliest uses was the summing of calibrated weights (Figure A1, left center) in weighing applications. Early electrical digital-to-analog conversion inevitably involved switches and resistors of different values, usually arranged in decades. The application was often the calibrated balancing of a bridge or reading, via null detection, some unknown voltage. The most accurate resistor-based DAC of this type is Lord Kelvin's Kelvin-Varley divider (Figure, large box). Based on switched resistor ratios, it can achieve ratio accuracies of 0.1ppm (23+ bits) and is still widely employed in standards laboratories.¹ High speed digital-to-analog conversion resorts to electronically switching the resistor network. Early electronic DACs were built at the board level using discrete precision resistors and germanium transistors (Figure, center foreground, is a 12-bit DAC from a

Minuteman missile D-17B inertial navigation system, circa 1962). The first electronically switched DACs available as standard product were probably those produced by Pastoriza Electronics in the mid 1960s. Other manufacturers followed and discrete- and monolithically-based modular DACs (Figure, right and left) became popular by the 1970s. The units were often potted (Figure, left) for ruggedness, performance or to (hopefully) preserve proprietary knowledge. Hybrid technology produced smaller package size (Figure, left foreground). The development of Si-Chrome resistors permitted precision monolithic DACs such as the LTC1595 (Figure, immediate foreground). In keeping with all things monolithic, the cost-performance trade off of modern high resolution IC DACs is a bargain. Think of it! A 16-bit DAC in an 8-pin IC package. What Lord Kelvin would have given for a credit card and LTC's phone number.

Note 1: See Appendix C, "Verifying Data Converter Linearity to 1ppm," for details on Kelvin-Varley Dividers.



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Figure A1. Historically Significant Digital-to-Analog Converters Include: Weight Set (Center Left), 23+ Bit Kelvin-Varley Divider (Large Box), Hybrid, Board and Modular Types, and the LTC1595 IC (Foreground). Where Will It All End?

APPENDIX B

THE LTC2400—A MONOLITHIC 24-BIT ANALOG-TO-DIGITAL CONVERTER

The LTC2400 is a micropower 24-bit A-to-D converter with an integrated oscillator, 4ppm nonlinearity and 0.3ppm RMS noise. It uses delta-sigma technology to provide extremely high stability. The device can be configured for better than 110dB rejection at 50Hz or 60Hz $\pm 2\%$, or it can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 120Hz.

This ultraprecision A-to-D converter in an SO-8 pin package forms the heart of the 20-bit DAC described in the text. It is significant that the device is used here as a circuit *component* rather than in the traditional standalone role accorded precision A-to-D converters. This freedom, in keeping with the IC's economy and ease of use, is a noteworthy opportunity. Alert designers will recognize this development and capitalize on it. Key specifications for the A-to-D are given in Figure B1.

PARAMETER	CONDITIONS	
Resolution (No Missing Codes)	$0.1V \leq V_{REF} \leq V_{CC}$	24 Bits
Integral Nonlinearity	$V_{REF} = 2.5V$ $V_{REF} = 5V$	2ppm of V_{REF} 4ppm of V_{REF}
Offset Error	$2.5V \leq V_{REF} \leq V_{CC}$	0.5ppm of V_{REF}
Offset Error Drift	$2.5V \leq V_{REF} \leq V_{CC}$	0.01ppm of $V_{REF}/^{\circ}C$
Full-Scale Error	$2.5V \leq V_{REF} \leq V_{CC}$	4ppm of V_{REF}
Full-Scale Error Drift	$2.5V \leq V_{REF} \leq V_{CC}$	0.02ppm of $V_{REF}/^{\circ}C$
Total Unadjusted Error	$V_{REF} = 2.5V$ $V_{REF} = 5V$	5ppm of V_{REF} 1ppm of V_{REF}
Output Noise		1.5 μ V _{RMS}
Normal Mode Rejection 60Hz $\pm 2\%$		110dB (Min)
Normal Mode Rejection 50Hz ± 2		110dB (Min)
Input Voltage Range	$0.125V \cdot V_{REF}$ to $1.125V \cdot V_{REF}$	
Reference Voltage Range	$0.1V \leq V_{REF} \leq V_{CC}$	
Supply Voltage	$2.7V \leq V_{CC} \leq 5.5V$	
Supply Current		
Conversion Mode	$\overline{CS} = 0V$	200 μ A
Sleep Mode	$\overline{CS} = V_{CC}$	20 μ A

**Figure B1. Key Specifications for LTC2400 A-to-D Converter.
High Linearity and Extreme Stability Allow Realization of 1ppm DAC**

Application Note 86

APPENDIX C

VERIFYING DATA CONVERTER LINEARITY TO 1PPM

Help from the Nineteenth Century

INTRODUCTION

Verifying 1ppm linearity of the DAC and the analog-to-digital converter used to construct it requires special considerations. Testing necessitates some form of voltage source that produces equal amplitude output steps for incremental digital inputs. Additionally, for measurement confidence, it is desirable that the source be substantially more linear than the 1ppm requirement. This is, of course, a stringent demand and painfully close to the state of the art.

The most linear “D to A” converter is also one of the oldest. Lord Kelvin’s Kelvin-Varley divider (KVD), in its most developed form, is linear to 0.1ppm. This manually switched device features ten million individual dial settings arranged in seven decades. It may be thought of as a 3-terminal potentiometer with fixed “end-to-end” resistance and a 7-decade switched wiper position (Figure C1).

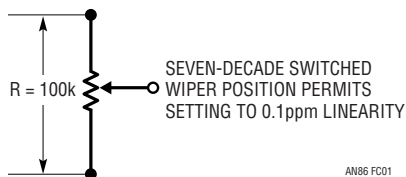


Figure C1. Conceptual Kelvin-Varley Divider

The actual construction of a 0.1ppm KVD is more artistry and witchcraft than science. The market is relatively small, the number of vendors few and resultant price high. If \$13,000 for a bunch of switches and resistors seems offensive, try building and certifying your own KVD. Figure C2 shows a detailed schematic.

The KVD shown has a 100kΩ input impedance. A consequence of this is that wiper output resistance is high and varies with setting. As such, a very low bias current follower is required to unload the KVD without introducing significant error. Now, our KVD looks like Figure C3. The LT1010 output buffer allows driving cables and loads and, more subtly, maintains the amplifier’s high open-loop gain.

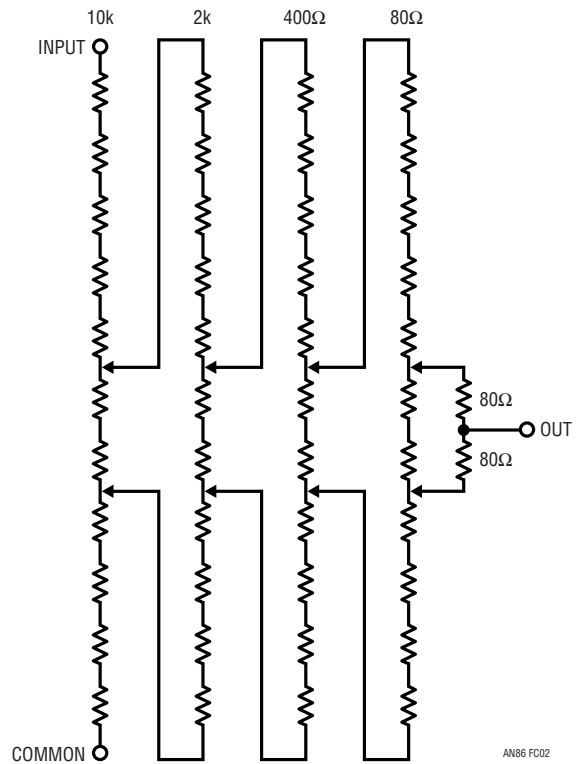


Figure C2. A 4-Decade Kelvin-Varley Divider. Additional Decades Are Implemented By Opening Last Switch, Deleting Two Associated 80Ω Values and Continuing ÷ 5 Resistor Chains

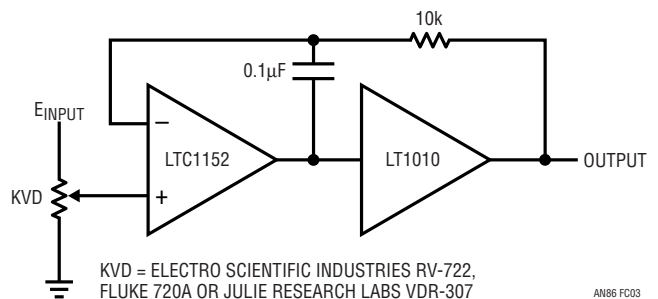
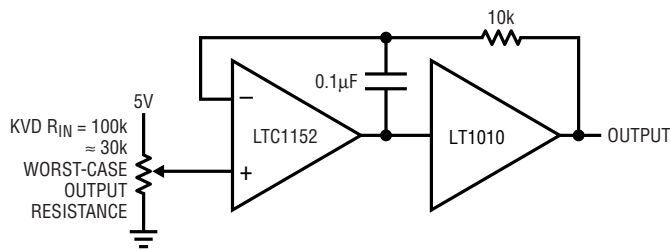


Figure C3. KVD with Buffer Gives Output Drive Capability

Approach and Error Considerations

This schematic is deceptively simple. In practice, construction details are crucial. Parasitic thermocouples (Seebeck effect), layout, grounding, shielding, guarding, cable choice and other issues affect achievable performance.¹ In fact, as good as the chopper-stabilized LTC1152 is with respect to drift, offset, bias current and CMRR, selection is required if we seek sub-ppm nonlinearity performance. Figure C4, an error budget analysis, details some of the selection criteria.



ERROR SOURCE	WORST-CASE SPEC	REALISTIC SELECTION TARGET	ERROR IN PPM
E_{OS}	5 μ V	0.5 μ V	0.1
$E_{OS\Delta T}$	0.05 μ V/ $^{\circ}$ C	0.05 μ V/ $^{\circ}$ C	0.01/ $^{\circ}$ C
I_B	50pA	10pA	0.1
CMRR	110dB	140dB	0.1
FINITE GAIN	140dB	140dB	0.1

AN86 FC04

Figure C4. Error Budget Analysis for the KVD Buffer. Selection Permits \approx 0.4ppm Predicted Linearity Error

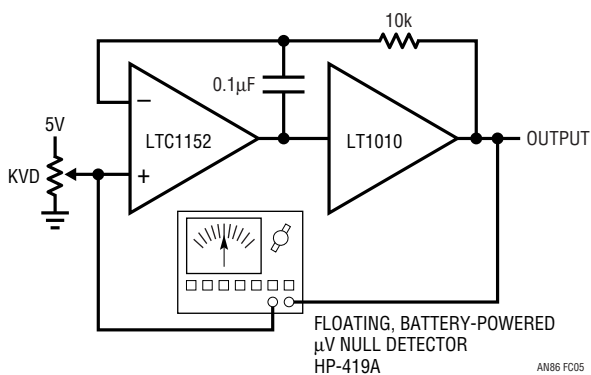


Figure C5. Determining Buffer Error By Measuring Input-Output Deviation with Floating Microvolt Null Detector. Technique Permits Evaluation of Fixed and Operating Point Induced Errors

The buffer is tested with Figure C5's circuit. As the KVD is run through its entire range, the floating null detector must remain well within 1ppm (5 μ V), preferably below 0.5ppm. This test ensures that all error sources, particularly I_B and CMRR, whose effects vary with operating point, are accounted for. Measured performance indicates the sum of all errors called out in Figure C4 is well within desired limits.

In Figure C6, we add offset trim, a stable voltage source and a second KVD to drive the main KVD. Additionally, an ensemble of three HP3458A voltmeters monitor the output.

The offset trim bleeds a small current into the main KVD ground return, producing a few microvolts of offset-trim range. This functionally trims out all sources of zero error (amplifier offsets, parasitic thermocouple mismatches and the like), permitting a true zero volt output when the main KVD is set to all zeros.

The voltmeters, specified for <0.1ppm nonlinearity on the 10V range, "vote" on the source's output.

Circuitry Details

Figure C7 is a more detailed schematic. It is similar to Figure C6 but highlights issues and concerns. The grounding scheme is single point, preventing mixing of return currents and the attendant errors. The shielded cables used for interconnections between the KVDs and voltmeters should be specified for low thermal activity. Keithley type SC-93 and Guildline #SCW are suitable. Crush type copper lugs (as opposed to soldered types) provide lower parasitic thermocouple activity at KVD and DVM connection points. However, they must be kept clean to prevent oxidation, thus avoiding excessive thermal voltages.² A copper deoxidant (Caig Labs "Deoxid" D100L) is quite effective for maintaining such cleanliness. Low thermal lugs and jacks, preterminated to cables, are also available (Hewlett-Packard 11053, 11174A) and convenient.

Thermal baffles enclosing KVD and DVM connections tend

Note 1: See Appendix J, "Cables, Connections, Solder, Layout, Component Choice, Error and Arcana," for relevant tutorial.

Note 2: See above Footnote.

Application Note 86

to thermally equilibrate their associated banana jack terminals, minimizing residual parasitic thermocouple activity. Additionally, restrict the number of connections in the signal path. Necessary connections should be matched in number and material so that differential cancellation occurs. Complying with this guideline may necessitate deliberate introduction of solder-copper junctions (marked “X” on Figure C7) to obtain optimum differential cancellation.³ This is normally facilitated by simply breaking the appropriate wire or PC trace and soldering it. Ensure that the introduced thermocouples temperature track the junctions they are supposed to cancel. This is usually accomplished by locating all junctions within close physical proximity.

The noise filtering capacitor at the main KVD is a low leakage type, with its metal case driven by the output buffer to guard out surface leakage.

When studying the approach used, it is essential to differentiate between linearity and absolute accuracy. This eliminates concerns with absolute standards, permitting certain freedoms in the measurement scheme. In particular, although single-point grounding was used, remote sensing was not. This is a deliberate choice, made to minimize the number of potential error-causing parasitic thermocouples in the signal path. Similarly, a ratiometric reference connection between the KVD LTZ1000A voltage source and the voltmeters was not utilized for the same reason. In theory, a ratiometric connection affords lower drift. In practice, the resultant introduced parasitic thermocouples obviate the desired advantage. Additionally, the aggregate stability of the LTZ1000A reference and the voltmeter references (also, incidentally, LTZ1000A based) is comfortably inside 0.1ppm for periods of 10 minutes.⁴ This is more than enough time for a 10-point linearity measurement.

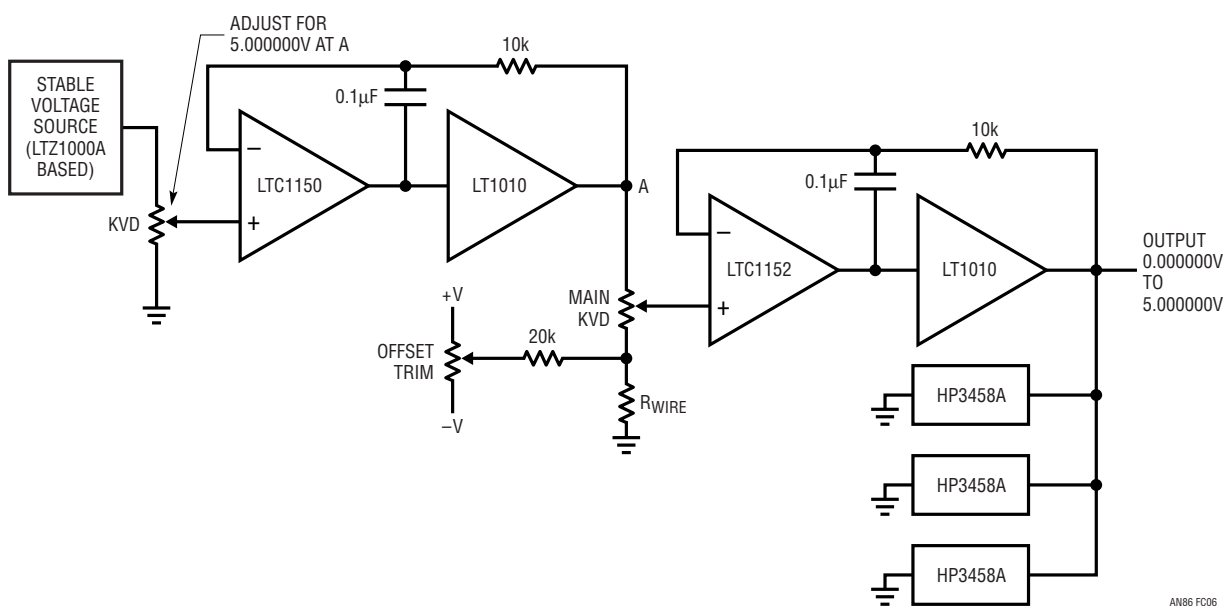


Figure C6. Simplified Sub-ppm Linearity Voltage Source

Note 3: See Appendix J, “Cables, Connections, Solder, Layout, Component Choice, Terror and Arcana,” for further discussion.

Note 4: The LTZ1000A reference is detailed in Appendix I, “Voltage References.”

Construction

Figures C8 and C9 are photographs of the voltage source and the reference-buffer box internal construction. The figure captions annotate some significant features.

Results

This KVD-based, high linearity voltage source has been in use in our lab for nearly two years. During this period, the total linearity uncertainty defined by the source and its monitoring voltmeters has been just 0.3ppm (see Figure

C10's measurement regime). This is more than 3 times better than the desired 1ppm performance, promoting confidence in our measurements.⁵

Acknowledgments

The author is indebted to Lord Kelvin and to Warren Little of the C. S. Draper Laboratory (née M. I. T. Instrumentation Laboratory) standards lab. Warren taught me, with great patience, the wonders of KVDs some thirty years ago and I am still trading on his efforts.

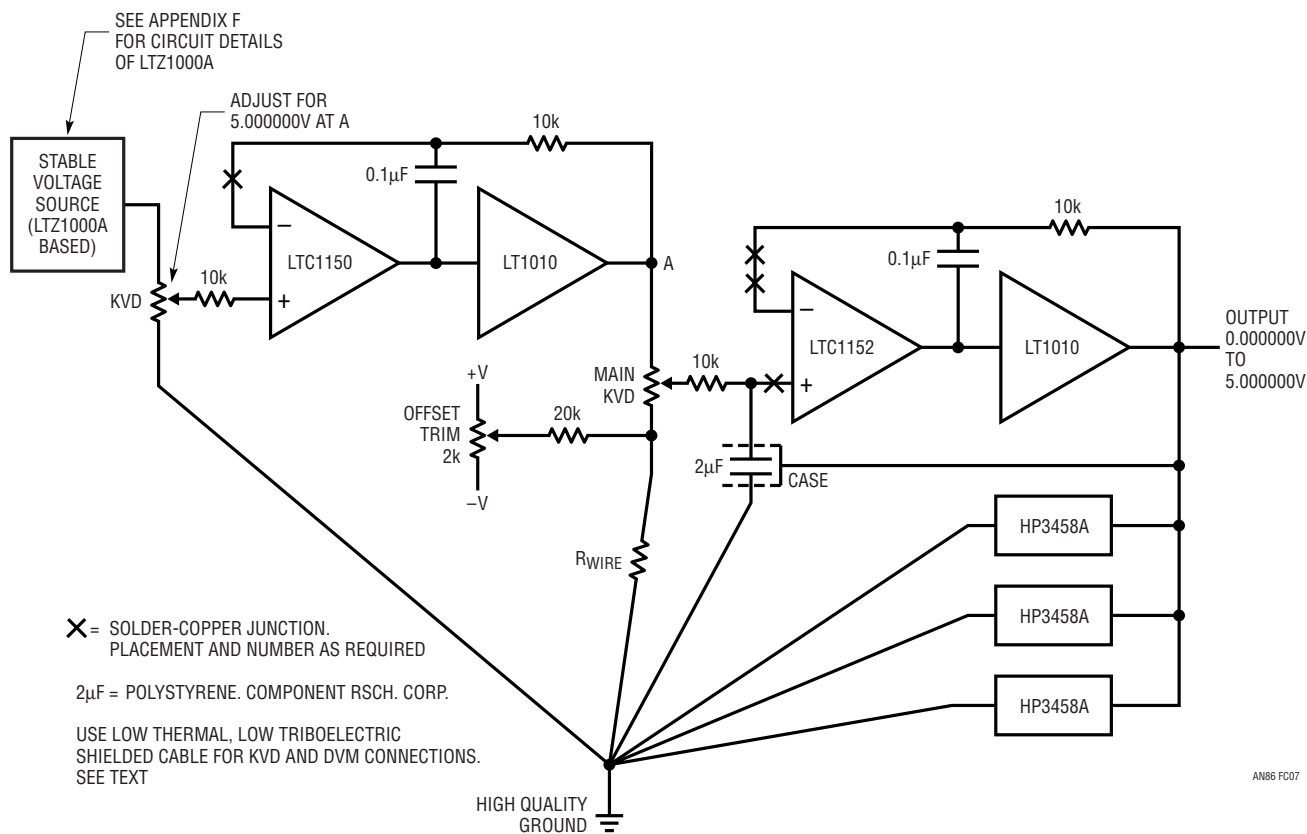
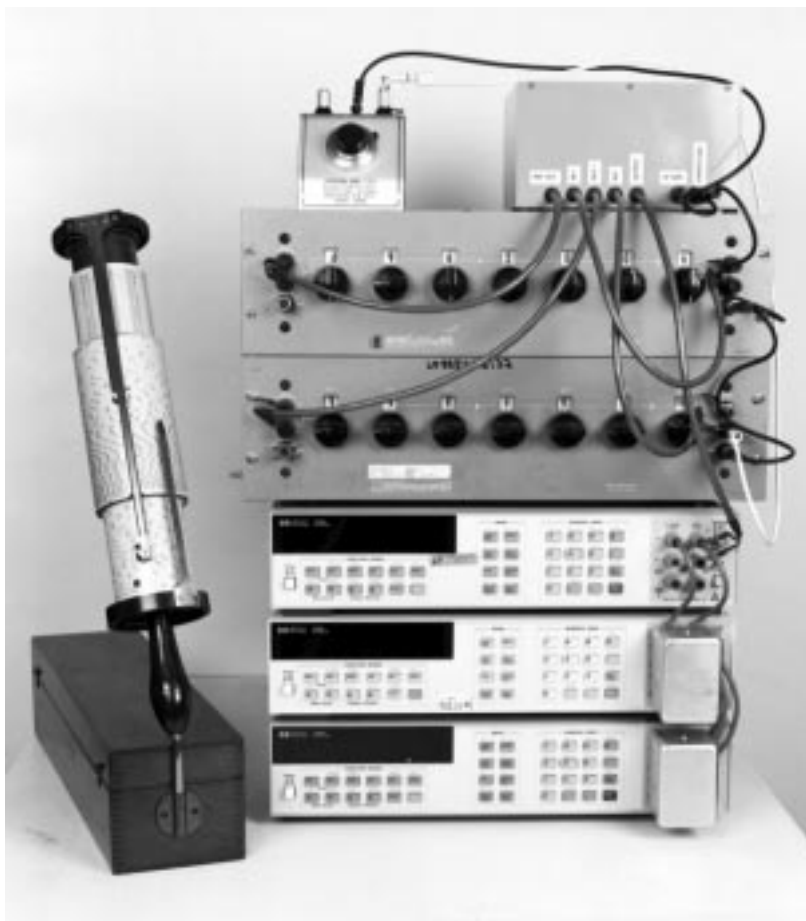


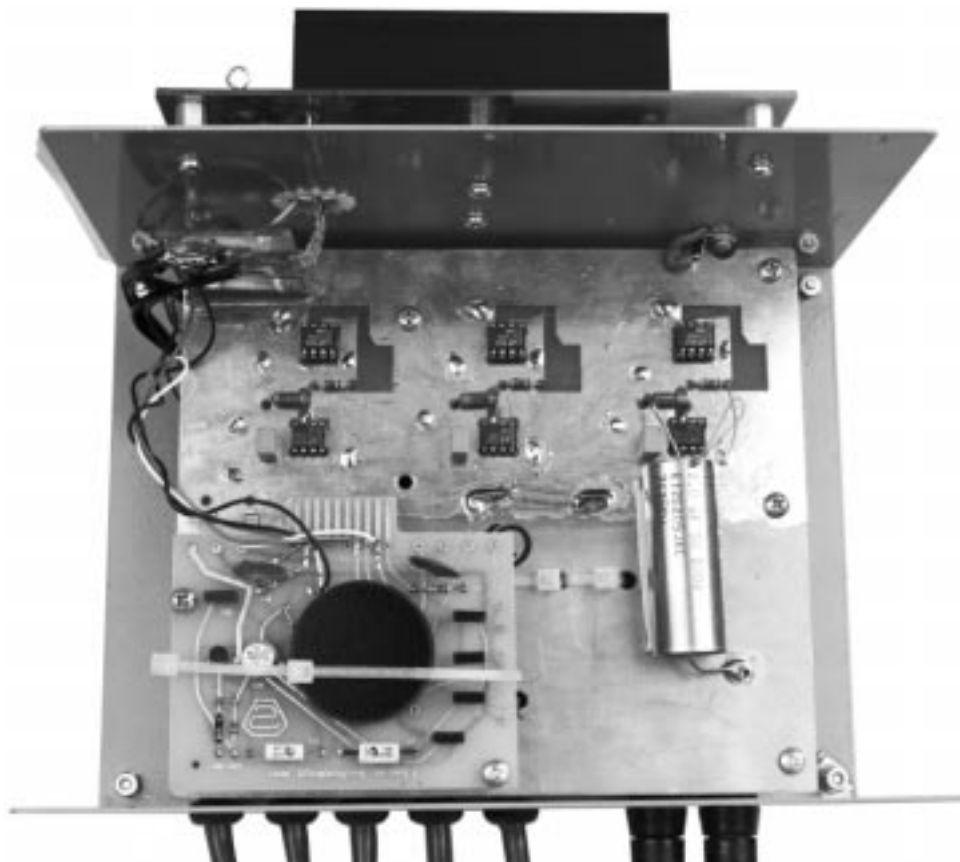
Figure C7. Complete Sub-ppm Linearity Voltage Source

Note 5: The author, wholly unenthralled by web surfing, has spent many delightful hours “surfing the Kelvin.” This activity consists of dialing various Kelvin-Varley divider settings and noting monitoring A-to-D agreement within 1ppm. This is astonishingly nerdy behavior, but thrills certain types.



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Figure C8. The Sub-ppm Linearity Voltage Source. Box Upper Right Is LTZ1000A Based Reference and Buffers. Upper Left Is Offset Trim. Reference and Main Kelvin-Varley Dividers Are Photo Center—Upper and Center-Middle, Respectively. Three HP3458 DVMs (Photo Lower) Monitor Output. Computer (Left Foreground) Aids Linearity Calculations



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Figure C9. Reference-Buffer Box Construction. LTZ1000A Reference Circuitry Is Photo Lower Left, Buffer Amplifiers Photo Center. Note Capacitor Case Bootstrap Connection (Photo Center—Right). Single Point Ground Mecca Appears Photo Upper Left. Power Supply (Photo Top) Mounts Outside Box, Minimizing Magnetic Field Disturbance

1. VERIFY KVD LINEARITY BY INTERCOMPARISON AND INDEPENDENT CAL. LAB.
2. TAKE WORST-CASE VOLTMETER ENSEMBLE DEVIATIONS OVER 0V TO 5V, EVERY 0.5V
3. 100 RUNS (10 PER DAY, ONCE PER HOUR)
4. INDICATED RESULT IS 0.3ppm NONLINEARITY

AN86 FC10

Figure C10. Testing Regime for the High Linearity Voltage Source

Application Note 86

APPENDIX D

A PROCESSOR-BASED CODE COMPARATOR

The code comparator enforces the loop by setting the slave DAC inputs to the code that equalizes the user input and the LTC2400 A-to-D output. This action is more fully described on page one of the text.

Figure D1 is the code comparator's digital hardware. It is composed of three input data latches and a PIC-16C5X processor. Inputs include user data (e.g., DAC inputs), linearity curvature correction (via DIP switches), convert command ("DA WR") and a selectable filter time constant. An output ("DAC RDY") indicates when the DAC output is settled to the user input value. Additional outputs and an

input control and monitor the analog section (text Figure 2) to effect loop closure. Note that although a total of 32 bits are presented to the two 16-bit slave DACs, there are 8 bits of overlap, allowing a total dynamic range of 24 bits. This provides 4 bits of indexing range below the 20th bit, ensuring a stable LSB of 1ppm of scale. The 8-bit overlap assures the loop will always be able to capture the correct output value.

The processor is driven by software code, authored by Florin Oprescu, which is described below.

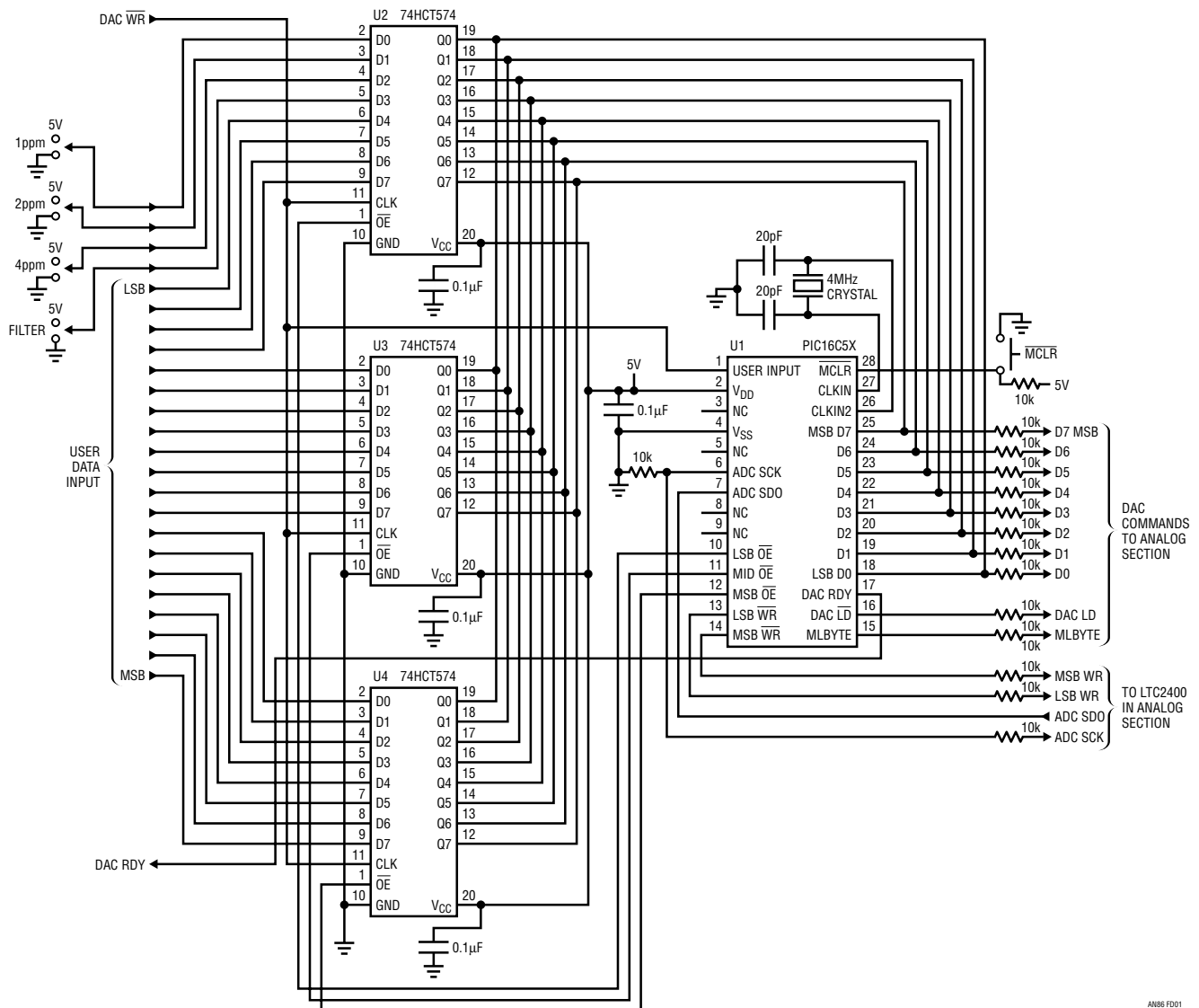


Figure D1. Code Comparator Hardware. User Control Lines Are at Left, Analog Section Connections Appear at Right Side

```
;20bit DAC code comparator
;
;*****
;
;      Filename:          dac20.asm          *
;      Date             12/4/2000         *
;      File Version:    1.1                *
;
;      Author:          Florin Oprescu     *
;      Company:        Linear Technology Corp.*
;
;*****
;
; Variables
;=====
; uses 17 bytes of RAM as follows:
;
; {UB2, UB1, UB0} user input word buffer
;-----
; 24 bits unsigned integer (3 bytes):
;
; The information is transferred from the external input register
; into {UB2, UB1, UB0} whenever a "user input update" event
; is detected by testing the timer0 content. Following the data
; transfer, the UIU ("user input update") flag is set and the DAC
; ready flags RDY and RDY2 are cleared. UB0 uses the same physical
; location as U0. The user input double buffering is necessary
; because the loop error corresponding to the current ADC reading
; must be calculated using the previous user input value.
; The old user input value can be replaced by the new user input
; value only after the loop error calculation.
; The worst case minimum response time to an UIU event must be
; calculated. The user shall not update the external input register
; at intervals shorter than this response time. For the moment the
; program can not block the user access to the external input
; register during a read operation. In such a situation the result
; of the read operation can be very wrong.
;
;      UB0 - least significant byte. Same physical location as U0
;
;      UB1 - second byte.
;
;      UB2 - most significant byte.
;
; {U2, U1, U0} user input word
;-----
; 24 bits unsigned integer (3 bytes):
;
; The information is transferred from {UB2, UB1, UB0[7:4], [0000]}
; into {U2, U1, U0} whenever the UIU flag is found set within the
; CComp ("code comparator") procedure. The UIU flag is reset
; following the data transfer.
```

Application Note 86

```
;
;   U0 - least significant byte of current DAC input
;       The 4 least significant bits U0[3:0] are set
;       to zero.
;
;   U1 - second byte of current DAC input
;
;   U2 - most significant byte of current DAC input
;
;
; {CON} control byte
;-----
; (1 byte):
;
; The 3 least significant bits CON[2:0] represent the ADC linearity
; correction factor transferred from UB[2:0] when the UIU flag
; is found set within the CComp procedure - at the same time as the
; {U2, U1, U0} variable is updated.
;
; The effect of CON[2:0] is additive and its weight is as follows:
;
;   CON[0] = 1 linearity correction effect is about 1ppm
;   CON[1] = 1 linearity correction effect is about 2ppm
;   CON[2] = 1 linearity correction effect is about 4ppm
;
; The LTC2400 has a typical 4ppm INL error therefore the default
; curvature correction value can be set at CON[2:0] = 100
;
; CON[3] is the control loop integration factor transferred from
; UB[3] when the UIU flag is found set within the CComp procedure.
; If CON[3]=0, after the control loop error becomes less than 4ppm
; the error correction gain is reduced from 1 to 1/4
; If CON[3]=1, after the control loop error becomes less than 4ppm
; the error correction gain is reduced from 1 to 1/16
;
; CON[7] is used as the UIU ("user input update") flag. It is set
; when {UB2, UB1, UB0} is updated and it is reset when {U2, U1, U0}
; and CON[3:0] are updated.
;
; CON[6] is used as the RDY ("DAC ready") flag. It is set when
; the DAC loop error becomes less than 4ppm and it is reset when
; the UIU flag is set.
;
; CON[5] is used as the RDY2 ("DAC ready twice") flag. It is set
; whenever the DAC loop error becomes less than 4ppm and the RDY
; flag has been previously set. It is reset when the UIU flag is set.
;
;
; The bit CON[4] is not used and is always set to 0.
;
;
```

```
; {ADC3, ADC2, ADC1, ADC0} formatted ADC conversion result
;-----
; 32 bits signed integer (4 bytes).
;
; The ADC reading is necessary only for the calculation of the control
; loop error and in order to save RAM space, it can share the same
; physical space as the loop error variable.
;
; The LTC2400 output format is offset binary. It must be converted
; to 2's complement before any arithmetic operation. A number of
; possible codes are not valid LTC2400 output codes. If such codes
; are detected it can be inferred that a serial transfer error has
; occurred, the data must be discarded and a new conversion must
; be started. For all LTC2400 devices B31=0 and B30=0 always. In
; addition, with the exception of some early samples of the device
; the sequence B[29:28]=00 should not occur in a valid transaction.
;
; ADC0 - least significant byte
;         contains ADC output bits B11(MSBIT) to B4 (LSBIT)
;
; ADC1 - second byte
;         contains ADC output bits B19(MSBIT) to B12 (LSBIT)
;
; ADC2 - third byte
;         contains ADC output bits B27(MSBIT) to B20 (LSBIT)
;
; ADC3 - most significant byte
;         contains ADC output bits ~B29(as 7 MSBITS for
;         2's complement sign extension) and B28 (LSBIT)
;
; {ADCC} ADC curvature correction
;-----
; 8 bits unsigned integer (1 byte)
;
; The LTC2400 transfer characteristic has a typical INL of about
; 4ppm and a parabolic shape symmetric with respect to mid-scale.
; This error can be corrected to a first and second order and
; ADDC contains the magnitude of this correction.
;
;
; {ER3, ER2, ER1, ER0} control loop error value
;-----
; signed integer (4 bytes)
;
; Contains the value of the current control loop error calculated
; as the difference between the previous user input and the last
; ADC reading. It is used to adjust the Low_DAC setting. Uses the
; same physical location as {ADC3, ADC2, ADC1, ADC0}:
;
; ER0 - least significant byte, same location as ADC0
;
; ER1 - second byte, same location as ADC1
```


Application Note 86

```
;
;   ER2 -   third byte, same location as ADC2
;
;   ER3 -   most significant byte, same location as ADC3
;
;
; {DL3, DL2, DL1, DL0} Low DAC control value
;-----
; signed integer (4 bytes):
;
; Contains the Low_DAC setting in a 2's complement, 32 bit
; format. Must be initialized to 0!
;
;   DL0 -   least significant byte - used for Low_DAC
;           control
;
;   DL1 -   second byte - used for Low_DAC control after
;           conversion to offset binary format {DL1, DL0}
;
;   DL2 -   third byte - may be only 00 or FF
;
;   DL3 -   most significant byte - may be only 00 or FF
;
;
; {INDX} Index variable for various program functions
;-----
; 1 byte.
;
;
; {TMPV} Temporary variable for various program functions
;-----
; 1 byte.
;
;
; Algorithm
;=====
;
; After each ADC conversion cycle the processor calculates the control
; loop error value as the difference between the desired output and
; the latest conversion result. Than it updates the DACs command
; such as to reduce the error magnitude. A new ADC conversion cycle
; is started following the DACs update operation.
;
; In order to maintain adequate control loop stability it is necessary
; for the DACs and the associated amplifiers to settle to better than
; 20 bits accuracy before the ADC starts sampling the system output. For
; an LTC2400 based system this settling time is 66ms.
;
; Initialization:
;   Initializes the PIC controller and the hardware interface
;   and starts the Scan procedure.
;
```

```

; 1. Load ADC control port with default values
;   SCKAD = 0
;   SDOAD = 1
; 2. Set ADC control port I and O pins
;   SCKAD = output
;   SDOAD = input
; 3. Load register control port with default values
;   NCSR[2:0] = 111
;   NCSD[1:0] = 11
;   ADDAC     = 1
;   NLDAC     = 1
;   DACRDY    = 0
; 4. Set register control port in output mode
; 5. Set data bus to default value DBUS[7:0]=0x00
; 6. Set data bus in output mode
; 7. Initialize internal registers and variables:
;   OPTION    = 0x2F
;   Timer0 used as counter is incremented by low-to-high edge
;   Prescaler works with watch dog timer in div128 mode
;   CON       = 0x80
;   Simulate a UIU "user interface update" event to force
;   the update of both Low_DAC and High_DAC
;   {DL3, DL2, DL1, DL0} = 0
;   {   U2, U1,  U0} = 0
; 8. Update hardware using the initialized variables
; 9. Start new ADC conversion by reading and discarding
;   32 serial bits.
; 10. Start the Scan procedure
;
; Scan:
; Continuously looks for "user input update" events. When
; a "user input update" event is detected updates the
; input buffer {UB2, UB1, UB0}, resets timer, sets UIU flag
; and resets RDY and RDY2 flags.
;
; The active low write signal for the external input register
; (which is the same as the user interface NWR input signal)
; is driven by the user and it is connected to the counter
; input of Timer0. The Timer0 is used in counter mode without a
; prescaler and it increments whenever a low-to-high transition
; is detected at its input. This is the same transition which
; latches in the input register a new user command.
; Because of the PIC controller timing constraints, this write
; signal must be maintained low for at least 2*Tosc + 20ns
; where Tosc is the maximum PIC clock period. When a 4 MHz
; clock is used for the PIC processor, the low time must be
; longer than about 520ns.
;
; 1. Test for "user input update" events by testing the Timer0
;   value.
;   If Timer0>0 an UIU event has occurred. Reset the timer
;   and answer Yes.
;   If Timer0=0 answer No.

```

Application Note 86

```
; 1.1 If Yes, read input latch into {UB2, UB1, UB0},
; reset DACRDY output line, set UIU flag and
; and reset RDY and RDY2 flags (CON[7:5]=100)
; Than continue
; 1.2 If No continue
;
; Continuously looks for the ADC end of conversion event. When
; the "end of conversion" is detected it reads the 28 most
; significant bits from the ADC and it constructs the ADC
; result {ADC3, ADC2, ADC1, ADC0} in 2's complement format
; If ADC3[1] == 0 => ADC3[7:1]=1111 111
; If ADC3[1] == 1 => ADC3[7:1]=0000 000
; For very early LTC2400 samples only, it is possible
; to obtain as a valid 0 conversion result ADC3[1:0]=00
; In this case:
; If ADC3[1:0] == 0 => ADC3=0
; It also calculates the first (x1) and second (x2) order ADC
; curvature correction ADCC as follows:
; x1 = {0x00, 0x80} -
; -abs({ADC3, ADC2, ADC1, ADC0}/(2^16)-{0x00, 0x80})
; x2 = {0x00, 0x40} -
; -abs({0x00, {0,ADC2[6:0]},ADC1,ADC0}/(2^16)-{0x00,0x40})
; ADCC = floor((x1 + x2/2) * {00000 CON[2:0]} / 4 )
; The actual implementation uses only the least significant
; byte of x without any substantial additional error.
; Thus the above relation can be modified as follows:
; ADCC = floor((abs(ADC2) + abs({ADC2[6],ADC2[6:0]}))/2) *
; * {00000 CON[2:0]} / 4 )
; The maximum correction range is about 7ppm INL at mid
; scale for CON[2:0] = 111.
;
; 2. Test for ADC "end of conversion" event by testing the
; value of the ADC_SDO signal.
; If ADC_SDO = LOW answer Yes.
; If ADC_SDO = HIGH answer No.
; 2.1 If Yes read 28 most significant bits from the ADC,
; update {ADC3, ADC2, ADC1, ADC0} and calculate the
; curvature correction byte ADCC. Than start the CComp
; procedure.
; It should be noticed that while reading the first 28
; most significant bits from the ADC the controller
; generates 27 serial clock pulses. An additional 5 serial
; clock pulses (for a total of 32) are necessary to restart
; the conversion.
; 2.2 If No restart the Scan procedure.
;
;
; CComp:
; Calculates the current control loop error as:
;
; error = current_user_input - ADC_reading +
; + new_user_input_LSB - current_user_input_LSB
;
```

```

; The curvature correction is included in the ADC
; conversion result and is always positive therefore:
;
; ADC_reading = {ADC3, ADC2, ADC1, ADC0} +
;               + { 0, 0, 0, ADCC}
;
; The term "new_user_input_LSB - current_user_input_LSB"
; represents the residue of the new user command which
; is added to the Low_DAC.
;
; {ER3, ER2, ER1, ER0} =
;   = {0, U2, U1, U0} - {ADC3, ADC2, ADC1, ADC0} -
;   - { 0, 0, 0, ADCC} +
;   + {0, 0, 0, UB0} - { 0, 0, 0, U0} =
;
;   = {0, U2, U1, UB0} - {ADC3, ADC2, ADC1, ADC0} -
;   - { 0, 0, 0, ADCC}.
;
; The loop error {ER3, ER2, ER1, ER0} is a 32 bit signed number
; and the weight of the least significant bit is 1/16ppm of
; the ADC reference voltage. A 4ppm error value is represented
; as {0, 0, 0, 0x40}.
;
; The ADC output noise is dominated by thermal noise and has a
; white distribution. The control loop noise can be reduced by
; the square root of N by averaging N successive ADC readings.
; The obvious penalty is a slow settling time. Due to the
; limited amount of RAM available a direct implementation
; of this noise reduction strategy is difficult. In an equivalent
; implementation, when the absolute value of the loop error
; {ER3, ER2, ER1, ER0} decreases below a certain threshold, the
; gain of the error correction loop can be decreased. The default
; threshold is set at a very conservative 4ppm. This value must
; always be larger than the peak noise level of the ADC. A very
; quiet implementation can probably operate with a threshold of
; 2ppm. If CON[3]=0 the gain of the error correction loop is
; decreased from 1 to 1/4. If CON[3]=1 the gain of the error
; correction loop is decreased from 1 to 1/16.
;
; The High_DAC is always controlled by the 16 most significant
; bits of the most recent user command {UB2, UB1}
;
; The Low_DAC is controlled by the {DL3, DL2, DL1, DL0}
; variable which integrates the control loop error. Under
; correct operating condition abs({DL3, DL2, DL1, DL0}) < 2^15.
; In order to avoid roll-overs during large transients the
; {DL3, DL2, DL1, DL0} must be clamped within the +/- 2^15 range.
; The 16 bit Low_DAC can then be controlled by {DL1, DL0}
; after conversion to offset binary format.
;

```

Application Note 86

```
; The DACRDY output line reflects the state of the
; internal RDY2 flag.
;
; After the updates are completed we must start a new ADC
; conversion by completing the serial transfer.
;
; 1. Test if UIU flag is set
;   1.1 If Yes, move UB[3:0] into CON[3:0]
;       and {UB0[7:4], 0000} into U0. The last ADC result
;       is curvature corrected using the previous CON[3:0] value!.
; 2. Calculate {ER3, ER2, ER1, ER0}.
; 3. Test if UIU flag is set
;   3.1 If Yes, move {UB2, UB1} into {U2, U1} and
;       clear UIU, RDY and RDY2 flags (CON[7:5]=000 )
;   3.2 If No, test if abs({ER3, ER2, ER1, ER0}) < 4ppm
;       3.2.1 If Yes, test if CON[6]=1 (RDY flag)
;           3.2.1.1 If Yes, set RDY2 flag (CON[5]=1 )
;           3.2.1.2 If No, set RDY flag (CON[6]=1 )
;           and test if CON[3]=0 (filter flag)
;           3.2.1.3 If Yes, {ER3, ER2, ER1, ER0} =
;                           = {ER3, ER2, ER1, ER0}/4
;           3.2.1.4 If No, {ER3, ER2, ER1, ER0} =
;                           = {ER3, ER2, ER1, ER0}/16
;       3.2.2 If No, clear UIU, RDY and RDY2
;           flags (CON[7:5]=000 )
; 4 {DL3, DL2, DL1, DL0} = {DL3, DL2, DL1, DL0} +
;   +{ER3, ER2, ER1, ER0}.
; 5. Update High_DAC, Low_DAC and DACRDY output line
; 6. Read the 4 least significant bits from ADC and start
;   a new conversion
; 7. Restart the Scan procedure
;
;
; Hardware resources
;=====
;
; Uses 8 input/output pins, 9 output pins, 1 input pin and 1
; counter input pin
;
; DBUS[7:0] data bus
;-----
; 8 bit bi-directional data bus is used to read the 20 bit input
; command IC[19:0], the one bit filter selection FS[0] and the 3 bit
; curvature correction selection CC[2:0]. It is also used to write
; the 16 bit Low_DAC command LDAC[15:0] and the 16 bit High_DAC
; command HDAC[15:0].
;
; assigned to PIC port C[7:0]
;
```

```
; The data format for the read and write operations is as follows:
;
; DBUS[ 7:0] = IC[19:12] when NCSR[2] = 0
; DBUS[ 7:0] = IC[11: 4] when NCSR[1] = 0
; DBUS[ 7:0] = {IC[3:0], FS[0], CC[2:0]} when NCSR[0] = 0
; LDAC[ 7:0] = DBUS[7:0] when NCSD[0] = 0 and ADDAC = 0
; LDAC[15:8] = DBUS[7:0] when NCSD[0] = 0 and ADDAC = 1
; HDAC[ 7:0] = DBUS[7:0] when NCSD[1] = 0 and ADDAC = 0
; HDAC[15:7] = DBUS[7:0] when NCSD[1] = 0 and ADDAC = 1
;
;
; NCSR[2:0] active low output enable controls for input registers
;-----
; 3 output lines used to selectively enable the three 8-bit input
; registers in order to read the user updated DAC command, the 3
; curvature correction bits and the one filter control bit.
;
; NCSR[0] enables the low input byte (LSB) and is assigned to port B[0]
;
; NCSR[1] enables the second input byte and is assigned to port B[1]
;
; NCSR[2] enables the high input byte (MSB) and is assigned to port B[2]
;
;
; NCSD[1:0] active low input enable controls for the DACs
;-----
; 2 output lines used to selectively enable the two DACs
;
; NCSD[0] enables the Low_DAC and is assigned to port B[3]
;
; NCSD[1] enables the High_DAC and is assigned to port B[4]
;
;
; ADDAC DAC address control
;-----
; output line. A low enables a write operation to the low byte of
; Low_DAC or High_DAC. A high enables a write operation to the high
; byte of Low_DAC or High_DAC.
;
; ADDAC is assigned to port B[5]
;
;
```

Application Note 86

```
; NLDAC active low DAC load control
;-----
; output line. A high to low transition on this line updates the
; Low_DAC and High_DAC output values
;
; NLDAC is assigned to port B[6]
;
;
; DACRDY active high ready output signal
;-----
; output line. Indicates that the control loop error has been
; within a +/- 4ppm range for at least 250 ms
;
; DACRDY is assigned to port B[7]
;
;
; SCKAD external serial clock line for the ADC
;-----
; output line. ADC external serial clock. An external 10Kohm
; pull-down resistor is necessary on this line for correct
; power-up configuration.
;
; SCKAD is assigned to port A[0]
;
;
; SDOAD serial data line from ADC
;-----
; input line. Used to read ADC serial data.
;
; SDOAD is assigned to port A[1]
;
;
;
; NWRUI active low user interface write control
;-----
; input line. The user must bring this line low in order to update
; the DAC input value. A minimum low and high time is required !
;
; NWRUI is assigned to TOCKI counter input pin
;
;
;
```



```

; The spare I/O pins A[3:2] are configured as outputs and maintained LOW.
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
list      p=16c55A      ; list directive to define processor
#include   <p16c5x.inc>  ; processor specific variable definitions

__CONFIG  _CP_OFF & _WDT_ON & _XT_OSC

;VARIABLE DEFINITIONS
;=====

UB0      EQU    H'0008'      ; user input word buffer LSB
UB1      EQU    H'0009'      ; user input word buffer second byte
UB2      EQU    H'000A'      ; user input word buffer MSB

U0       EQU    H'0008'      ; user input word LSB
U1       EQU    H'000B'      ; user input word second byte
U2       EQU    H'000C'      ; user input word MSB

CON      EQU    H'000D'      ; control byte

ADC0     EQU    H'000E'      ; ADC conversion result LSB
ADC1     EQU    H'000F'      ; ADC conversion result second byte
ADC2     EQU    H'0010'      ; ADC conversion result third byte
ADC3     EQU    H'0011'      ; ADC conversion result MSB

ADCC     EQU    H'0012'      ; ADC curvature correction byte

ER0      EQU    H'000E'      ; control loop error LSB
ER1      EQU    H'000F'      ; control loop error second byte
ER2      EQU    H'0010'      ; control loop error third byte
ER3      EQU    H'0011'      ; control loop error MSB

DL0      EQU    H'0013'      ; Low_DAC LSB
DL1      EQU    H'0014'      ; Low_DAC second byte
DL2      EQU    H'0015'      ; Low_DAC third byte
DL3      EQU    H'0016'      ; Low_DAC MSB

INDX     EQU    H'0017'      ; index variable

TMPV     EQU    H'0018'      ; temporary variable

#define   OPRDF  0x2F      ; OPTION register default value
#define   CONDF  0x80      ; CON register default value

```

Application Note 86

;HARDWARE ASSIGNMENT DEFINITIONS

;=====

```
#define DBUS    PORTC        ; 8bit I/O data bus

#define REGCN   PORTB        ; register control port
#define REGDF   0x7F         ; register control port default value
#define NCSR0   PORTB,0     ; LSB input register active low output enable
#define NCSR1   PORTB,1     ; second byte input register active low output enable
#define NCSR2   PORTB,2     ; MSB input register active low output enable

#define NCSD0   PORTB,3     ; Low_DAC active low write enable
#define NCSD1   PORTB,4     ; High_DAC active low write enable
#define ADDAC   PORTB,5     ; address bit for Low_DAC and High_DAC
#define NLDAC   PORTB,6     ; active low load control for Low_DAC and High_DAC

#define DACRDY  PORTB,7     ; 20bit_DAC ready indicator

#define ADCCN   PORTA        ; ADC control port
#define ADCTR   0x02         ; ADC control port configuration
                               ; SDOAD input, the rest outputs
#define ADCDF   0x02         ; ADC control port default value
#define SCKAD   PORTA,0     ; ADC external serial clock
#define SDOAD   PORTA,1     ; ADC serial data output
```

;THE CODE

;=====

```
RESET      ORG    0x1FF      ; processor reset vector
           goto   start

           ORG    0x000
                               ;Initialization procedure
                               ;-----

start      movlw  ADCDF      ;write ADC control port default value
           movwf  ADCCN      ;
           movlw  ADCTR      ;set the I and O pin states for the
           tris   ADCCN      ;ADC control port
           ;
           movlw  REGDF      ;write register control port default value
           movwf  REGCN      ;
           clrw   ;set register control port pins as
           tris   REGCN      ;output only
           ;
           movwf  DBUS       ;set DBUS default value of 0
           tris   DBUS       ;set DBUS as output
           ;
           movlw  OPRDF      ;set OPTION register default value
           option ;
           ;
```

```

        clrf    TMR0          ;
        btfs   STATUS,NOT_TO ;if this is not a power-on reset
        movwf  TMR0          ;load Timer0 with a nonzero value
                                ;to force an initial read of the
                                ;external input register
                                ;
        clrf    DL3          ;initialize {DL3, DL2, DL1, DL0}=0
        clrf    DL2          ;
        clrf    DL1          ;
        clrf    DL0          ;
        clrf    U2          ;initialize {U2, U1, U0}=0
        clrf    U1          ;
        clrf    U0          ;
                                ;
        movlw   CONDF        ;set CON variable default value
        movwf  CON          ;
                                ;prepare to trigger a new ADC conversion
                                ;after completing a hardware update
        movlw   0x20         ;read and discard 32 serial bits from
        movwf  INDX         ;the ADC
                                ;
        goto   iupdt        ;go to the hardware update function

                                ;ADC output buffer flush function
                                ;-----
fladc      movlw   0x20         ;reads and discards 32 serial bits from
        movwf  INDX         ;the ADC

                                ;ADC dummy serial read function
                                ;-----
                                ;reads and discards the number of serial
                                ;bits indicated by the INDX variable
rddmy      bsf    SCKAD        ;low-to-high ADC serial clock edge
        bcf    SCKAD        ;high-to-low ADC serial clock edge
        decfsz INDX,1        ;test if we read enough bits
        goto   rddmy        ;if No, read one more bit
        btfs   SDOAD        ;if Yes test that a new conversion has started
        goto   fladc        ;if No, there is an interface problem. Flush the
                                ;ADC output buffer and start a new conversion
        goto   scan        ;if Yes restart the scan procedure

                                ;external input register read function
                                ;-----
rduiu      movlw   0xFF        ;input register read routine
        tris   DBUS         ;set data bus in read mode (input)
        bcf    NCSR0        ;output enable for input reg. LSB
        nop                    ;wait for data bus to settle
        movf   DBUS,0        ;read input reg. LSB
        bsf    NCSR0        ;output disable for input reg. LSB

        bcf    NCSR1        ;output enable for input reg. second byte
        movwf  UB0          ;store input reg. LSB into input buffer
        movf   DBUS,0        ;read input reg. second byte
        bsf    NCSR1        ;output disable for input reg. second byte

```

Application Note 86

```
bcf    NCSR2           ;output enable for input reg. MSB
movwf  UB1             ;store input reg. second byte into input buffer
movf   DBUS,0         ;read input reg. MSB
movwf  UB2             ;store input reg. MSB into input buffer

clrw                   ;terminate input reg. read operation
bsf    NCSR2           ;output disable for input reg. MSB
tris   DBUS           ;return data bus to write mode

clrf   TMR0           ;clear Timer0 to continue wait for a UIU event
bcf    DACRDY         ;signal user that input data has been read

bsf    CON,7          ;set UIU flag
bcf    CON,6          ;clear RDY flag
bcf    CON,5          ;clear RDY2 flag

;scan procedure
;-----
;monitors UIU and end-of-conversion events
scan   movf   TMR0,1   ;test if Timer0 = 0
      btfss  STATUS,Z ;if Timer0=0 no UIU has occurred, skip next
      goto  rduiu     ;a user interface update has occurred
                        ;go and read the new DAC input data

      btfsc  SDOAD     ;test ADC end of conversion signal
      goto  scan      ;conversion not ready, rescan

;ADC serial read function
;-----
rdadc  movlw  0x1B     ;ADC conversion is done, read first 28 bits
      movwf  INDX     ;the first bit must be "0" to get here
                        ;so do not bother with it
rdbit  bsf    SCKAD    ;low-to-high ADC serial clock edge
      bcf    SCKAD    ;high-to-low ADC serial clock edge
      bcf    STATUS,C ;move ADC output bit to carry. First clear carry
      btfsc  SDOAD    ;read ADC output bit
      bsf    STATUS,C ;if ADC output is "1" set carry
      rlf   ADC0,1   ;load carry as msb of ADC result
      rlf   ADC1,1   ;and shift left all 4 bytes of the ADC result
      rlf   ADC2,1   ;
      rlf   ADC3,1   ;
      decfsz INDX,1  ;test if all 28 bits have been read
      goto  rdbit   ;if not, continue
                        ;
                        ;we have skipped the first ADC bit (ADC bit31=0)
                        ;which has been tested as =0 when we detected the
                        ;end of conversion.
                        ;we have read 27 additional bits and have generated
                        ;27 clock pulses. To restart the conversion we must
                        ;produce the 5 remaining clock pulses
```

```

;verify validity of ADC serial data and format it
;-----
btfsc ADC3,2 ;test if the ADC bit30 is "0"
goto fladc ;if not there is an interface problem. Flush the
;ADC output buffer and start a new conversion
;if yes, put the ADC result in 2's complement form

movlw 0x03 ;first clear the 6 most significant bits in ADC3
andwf ADC3,1 ;

btfsc STATUS,Z ;tests for the [ADC_B29,ADC_B28]=00 ADC output

goto rdend ;if Yes the formatting is completed.
;in very early LTC2400 samples the ADC output code
;[ADC_B29,ADC_B28]=00 is valid

;
goto fladc ;for current LTC2400 devices improved error
;detection capability is obtained if the
;previous line is replaced with this line.
;The replacement is not mandatory.
;For current LTC2400 parts the output code
;[ADC_B29,ADC_B28]=00 is not valid thus it may
;be assumed that an ADC interface error has
;occurred. Flush the ADC output buffer and start
;a new conversion

movlw 0x02 ;if No, convert ADC3 in 2's complement form
btfss ADC3,1 ;
movlw 0xFE ;
xorwf ADC3,1 ;

;curvature correction calculator
;-----
;first order curvature correction multiplier
;use ADC2[7:0] as a 2's complement number
rdend movf ADC2,0 ;calculate abs(ADC2)
btfsc ADC2,7 ;if ADC2[7]=0 w = ADC2
comf ADC2,0 ;else w = !ADC2
movwf ADCC ;ADCC=w=abs(ADC2)
;second order curvature correction multiplier
;use ADC2[6:0] as a 2's complement number
movf ADC2,0 ;calculate abs(ADC2[6:0])
btfsc ADC2,6 ;if ADC2[6]=0 w = ADC2
comf ADC2,0 ;else w = !ADC2
movwf TMPV ;TMPV=w=abs(ADC2[6:0])
rrf TMPV,0 ;w=TMPV/2 in order to scale the second order
;curvature correction
andlw 0x1f ;clear 3 MSB of w to complete calculation
addwf ADCC,0 ;w=abs(ADC2)+abs(ADC2[6:0])/2
movwf TMPV ;TMPV contains the curvature correction multiplier
;
clrf ADCC ;
bcf STATUS,C ;clear carry for div-by-2 operation
btfsc CON,2 ;if CON[2]=1

```

Application Note 86

```
movwf ADCC           ;ADCC=ADCC+abs(ADC2)
rrf  TMPV,1         ;TMPV=TMPV/2
movf  TMPV,0        ;
bcf  STATUS,C      ;clear carry for div-by-2 operation
btfsc CON,1        ;if CON[1]=1
addwf ADCC,1       ;ADCC=ADCC+abs(ADC2)/2
rrf  TMPV,1         ;TMPV=TMPV/2
movf  TMPV,0        ;
btfsc CON,0        ;if CON[0]=1
addwf ADCC,1       ;ADCC=ADCC+abs(ADC2)/4

                                ;code comparator procedure
                                ;-----
ccomp  btfss  CON,7   ;if the UIU flag is clear
      goto  ercalc  ;skip CON[3:0] and U0 update
      movlw 0xF0     ;else update CON[3:0]
      andwf CON,1    ;clear CON[3:0]
      movlw 0x0F     ;extract new CON[3:0]
      andwf UB0,0    ;from input buffer
      iorwf CON,1    ;and load it

      movlw 0xF0     ;move UB[7:4] to U0[7:4]
      andwf UB0,1    ;UB0 and U0 use the same
                        ;physical location

                                ;calculate control loop error
                                ;-----
ercalc  comf  ADCC,1  ;ADCC 1's complement
      comf  ADC0,1  ;ADC0 1's complement
      movlw 0x02    ;add carry-in for ADCC and for ADC0
                        ;2's complement conversion
      clrf  TMPV     ;prepare carry-out accumulator
      addwf UB0,0    ;w=carry-in + UB0
      btfsc STATUS,C ;if there is a carry-out
      incf  TMPV,1   ;accumulate it
      addwf ADCC,0   ;w=carry-in + UB0 - ADCC
      btfsc STATUS,C ;if there is a carry-out
      incf  TMPV,1   ;accumulate it
      addwf ADC0,1   ;ER0=UB0 - ADC0 - ADCC
                        ;has same location as ADC0
      btfsc STATUS,C ;if there is a carry-out
      incf  TMPV,1   ;accumulate it
```

```

comf   ADC1,1           ;ADC1 1's complement
movlw  0xff            ;w=0xff (1's complement of ADCC second byte)
addwf  TMPV,0         ;w=0xff + carry-in
clrf   TMPV           ;prepare carry-out accumulator
btfsc  STATUS,C       ;if there is a carry-out
incf   TMPV,1         ;accumulate it
addwf  U1,0           ;w=0xff + carry-in + UB1
btfsc  STATUS,C       ;if there is a carry-out
incf   TMPV,1         ;accumulate it
addwf  ADC1,1         ;ER1=U1 - ADC1 - 0 + carry-in
                        ;has same location as ADC1

btfsc  STATUS,C       ;if there is a carry-out
incf   TMPV,1         ;accumulate it

comf   ADC2,1           ;ADC2 1's complement
movlw  0xff            ;w=0xff (1's complement of ADCC third byte)
addwf  TMPV,0         ;w=0xff + carry-in
clrf   TMPV           ;prepare carry-out accumulator
btfsc  STATUS,C       ;if there is a carry-out
incf   TMPV,1         ;accumulate it
addwf  U2,0           ;w=0xff + carry-in + UB2
btfsc  STATUS,C       ;if there is a carry-out
incf   TMPV,1         ;accumulate it
addwf  ADC2,1         ;ER2=U2 - ADC2 - 0 + carry-in
                        ;has same location as ADC2

btfsc  STATUS,C       ;if there is a carry-out
incf   TMPV,1         ;accumulate it

comf   ADC3,1           ;ADC3 1's complement
decf   TMPV,1         ;ADCC 2's complement term. The next
                        ;carry-in is not useful - discard
movf   TMPV,0         ;w=carry-in
addwf  ADC3,1         ;ER3= 0 - ADC3 - 0 + carry-in
                        ;has same location as ADC3

btfsc  CON,7          ;test if the UIU flag is set
goto   lduiu         ;go to U1, U2 update

```


Application Note 86

```
                                ;error comparator
                                ;-----
                                ;calculate absolute value of loop error and
                                ;compare loop error magnitude with the 4ppm
                                ;threshold
movf    ER3,0                    ;W = ER3
btfsc  ER3,7                    ;test if {ER3, ER2, ER1, ER0} < 0
comf   ER3,0                    ;if yes W = -ER3
btfss  STATUS,Z                ;test if W=0
goto   nrdy                    ;if not absolute error >= 4ppm

movf    ER2,0                    ;W = ER2
btfsc  ER3,7                    ;test if {ER3, ER2, ER1, ER0} < 0
comf   ER2,0                    ;if yes W = -ER2
btfss  STATUS,Z                ;test if W=0
goto   nrdy                    ;if not absolute error >= 4ppm

movf    ER1,0                    ;W = ER1
btfsc  ER3,7                    ;test if {ER3, ER2, ER1, ER0} < 0
comf   ER1,0                    ;if yes W = -ER1
btfss  STATUS,Z                ;test if W=0
goto   nrdy                    ;if not absolute error >= 4ppm

movf    ER0,0                    ;W = ER0
btfsc  ER3,7                    ;test if {ER3, ER2, ER1, ER0} < 0
comf   ER0,0                    ;if yes W = -ER0
andlw  0xC0                    ;keep only W[7:6] which are bits >= 4ppm
btfss  STATUS,Z                ;test if W[7:6]=0
goto   nrdy                    ;if not absolute error >= 4ppm

                                ;if we are here the absolute loop error is
                                ;less than 4 ppm. Set the flags and
                                ;scale the loop error.
btfsc  CON,6                    ;test if RDY flag is already set
bsf    CON,5                    ;if Yes, set RDY2 flag
bsf    CON,6                    ;set RDY flag in any case
```

```

;error scaling
;-----
;reduce error correction value for loop
;damping and ADC noise reduction
btfsc CON,3 ;test if CON[3]=0
goto div4 ;if Yes ER0=ER0/4
;if No ER0=ER0/16
rrf ER0,1 ;*1/2
rrf ER0,0 ;*1/2
andlw 0x3F ;clear 2 most significant bits
btfsc ER3,7 ;if {ER3, ER2, ER1, ER0} < 0
iorlw 0xC0 ;set 2 most significant bits
movwf ER0 ;ER0=ER0/4
div4 rrf ER0,1 ;*1/2
rrf ER0,0 ;*1/2
andlw 0x3F ;clear 2 most significant bits
btfsc ER3,7 ;if {ER3, ER2, ER1, ER0} < 0
iorlw 0xC0 ;set 2 most significant bits
movwf ER0 ;ER0=ER0/4
goto eracc ;go to error accumulator

;load latest user input
;-----
lduiu movf UB1,0 ;
movwf U1 ;U1=UB1
movf UB2,0 ;
movwf U2 ;U2=UB2
nrldy movlw 0x1F ;
andwf CON,1 ;clear UIU, RDY and RDY2 flags

;error accumulator
;-----
;adds the current loop error to the
;previous Low_DAC control value
;{DL3, DL2, DL1, DL0}={DL3, DL2, DL1, DL0}+
; +{ER3, ER2, ER1, ER0}
eracc movf ER0,0 ;the carry-in is 0
clrf TMPV ;clear carry-in accumulator
addwf DL0,1 ;DL0=DL0+ER0
btfsc STATUS,C ;if there is a carryout
incf TMPV,1 ;accumulate in carry-in
movf TMPV,0 ;load carry-in
clrf TMPV ;clear carry-in accumulator
addwf ER1,0 ;W=ER1+carry-in
btfsc STATUS,C ;if there is a carryout
incf TMPV,1 ;accumulate in carry-in
addwf DL1,1 ;DL1=DL1+ER1
btfsc STATUS,C ;if there is a carryout
incf TMPV,1 ;accumulate in carry-in
movf TMPV,0 ;load carry-in
clrf TMPV ;clear carry-in accumulator
addwf ER2,0 ;W=ER2+carry-in

```

Application Note 86

```
    btfsc STATUS,C      ;if there is a carryout
    incf  TMPV,1        ;accumulate in carry-in
    addwf DL2,1         ;DL2=DL2+ER2
    btfsc STATUS,C      ;if there is a carryout
    incf  TMPV,1        ;accumulate in carry-in
    movf  TMPV,0        ;load carry-in
    addwf ER3,0         ;W=ER3+carry-in
    addwf DL3,1         ;DL3=DL3+ER3

                                ;Low_DAC control truncation
                                ;-----
                                ;limits the {DL3, DL2, DL1, DL0} range to
                                ; abs({DL3, DL2, DL1, DL0}) < 2^15 by
                                ;truncation
    btfss STATUS,Z      ;test if DL3=0
    goto  negpot        ;if No, DL may be negative
                                ;if Yes, DL is positive
                                ;test for overflow (>= 2^15)
    movf  DL2,1         ;
    btfss STATUS,Z      ;test if DL2=0
    goto  overflow      ;if No, DL >= 2^15, must truncate
                                ;if Yes continue testing for overflow
    btfsc DL1,7         ;test if DL1[7]=1
    goto  overflow      ;if No, DL >= 2^15, must truncate
    goto  updt          ;if Yes we are done with DL range control

overflow    clrf  DL3      ;if we arrive here DL >= 2^15. Must
    clrf  DL2      ;truncate to DL=2^15-1 => DL3=DL2=0
    movlw 0xFF     ;and DL1=0xEF, DL0=0xFF
    movwf DL0      ;
    movwf DL1      ;
    bcf   DL1,7    ;
    goto  updt     ;done with overflow correction
```

```

udflow    clrfl  DL1      ;if we arrive here DL < -2^15. Must
          bsf   DL1,7    ;truncate to DL=-2^15-1 => DL3=DL2=0xFF
          clrfl  DL0      ;and DL1=0x80, DL0=0
          movlw 0xFF      ;
          movwf DL3        ;
          movwf DL2        ;
          goto  updt       ;done with underflow correction

negpot    btfss  DL3,7    ;DL may be negative. Test if DL3[7]=1
          goto  ovflow    ;if No, DL > 2^15, must truncate
          incf  DL3,0     ;if Yes, DL <0.
          btfss STATUS,Z  ;test if DL3=FF
          goto  udflow    ;if No, DL < -2^15, must truncate
          incf  DL2,0     ;if Yes continue testing for underflow
          btfss STATUS,Z  ;test if DL2=FF
          goto  udflow    ;if No, DL < -2^15, must truncate
          ;if Yes continue testing for underflow
          btfss DL1,7     ;test if DL1[7]=0
          goto  udflow    ;if No, DL < -2^15, must truncate
          ;if Yes we are done with DL range control

          ;Hardware update function
          ;-----
          ;Low_DAC and High_DAC update
          ;
          ;This is the hardware update function
          ;entry point for normal operation.
          ;
          updt    movlw  0x05 ;prepare to generate the last 5 ADC external
          movwf  INDX      ;serial clock pulses
          ;when going to restart the scan procedure
          ;at the end of the hardware update function
          ;This will trigger a new ADC conversion.
          ;
          ;This is the hardware update function
          ;entry point for initial operation.
          ;The INDX variable has been initialized
          ;before to 0x2F which will generate
          ;32 serial clock pulses to the ADC thus
          ;starting a new conversion
          ;

```

Application Note 86

```
iupdt      clrw          ;set the data bus in write mode
           tris   DBUS    ;
           bcf   ADDAC    ;set DAC address for LSB
           movf  U1,0     ;load High_DAC LSB
           movwf DBUS     ;
           bcf   NCSD1    ;write to High_DAC
           bsf   NCSD1    ;
           movf  DL0,0    ;load Low_DAC LSB
           movwf DBUS     ;
           bcf   NCSD0    ;write to Low_DAC
           bsf   NCSD0    ;
           bsf   ADDAC    ;set DAC address for MSB
           movf  U2,0     ;load High_DAC MSB
           movwf DBUS     ;
           bcf   NCSD1    ;write to High_DAC
           bsf   NCSD1    ;
           movlw 0x80     ;change DL1 to offset binary
           xorwf DL1,0    ;load Low_DAC MSB
           movwf DBUS     ;
           bcf   NCSD0    ;write to Low_DAC
           bsf   NCSD0    ;
           bcf   NLDAC    ;load Low_DAC and High_DAC
           bsf   NLDAC    ;
           ;DACRDY output update
           btfsc CON,5    ;test if RDY2 flag is set
           bsf   DACRDY   ;if Yes, set DACRDY output
           btfss CON,5    ;if No
           bcf   DACRDY   ;and only if No, clear DACRDY output
           ;
           clrwdt        ;clear watch dog timer
           ;
           goto   rddmy   ;generate the necessary number
           ;of ADC serial clock pulses in order
           ;to start a new conversion

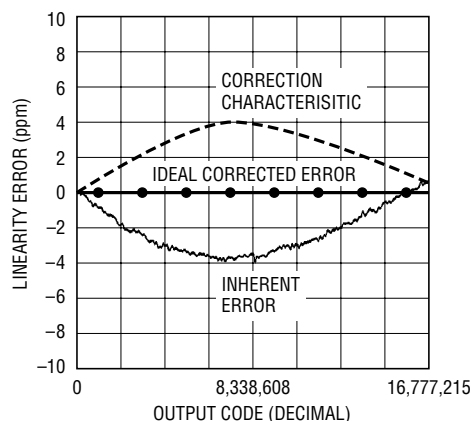
           END           ; directive 'end of program'
```

APPENDIX E

LINEARITY AND OUTPUT RANGE OPTIONS

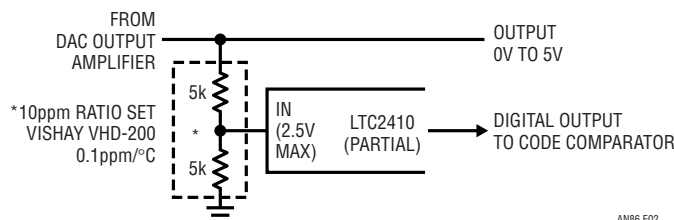
The LTC2400 used as the feedback A-to-D element in the DAC has a typical ± 2 ppm residual nonlinearity. Figure E1's lower curve shows this, along with the first order correction necessary (upper curve) to get nonlinearity inside 1ppm (center curve). If true 1ppm performance is necessary, the software based correction described in Appendix D can be utilized. The software generates the desired "inverted bowl" correction characteristic. The correction may be set to complement the residual nonlinearity characteristics of any individual LTC2400 via DIP switches at the code comparator.

The LTC2410 offers another approach to improved linearity. This LTC2400 variant has improved linearity but specifies a maximum 2.5V input range. Figure E2 divides the DAC output with a precision resistor ratio set, allowing LTC2410 use while maintaining the 5V full-scale output. The disadvantage of this approach is the ratio set's additional 0.1ppm/ $^{\circ}$ C and 5ppm/year error contribution.¹ Figure E3 is similar, although the ratio set's new value permits a 10V full-scale output.



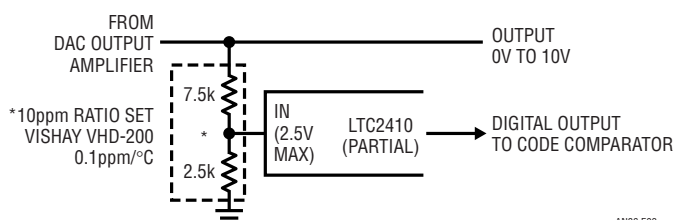
AN86 FE01

Figure E1. LTC2400 A-to-D Inherent Residual Linearity Error (Lower), Correction Characteristic (Upper) and Resultant Corrected Linearity (Center). Correction Ensures <1ppm Nonlinearity



AN86 E02

Figure E2. Precision Resistor Ratio Set Divides DAC Output, Permitting Higher Inherent Linearity LTC2410 Utilization. Disadvantage Is 5ppm/Yr and 0.1ppm/ $^{\circ}$ C Additional Drift Terms



AN86 E03

Figure E3. Similar to Figure E2, Except 3:1 Ratio Set Permits 10V Output While Accommodating LTC2410's 2.5V Input

Note 1: The strata is becoming rarified when "error contribution" is delineated in fractional parts-per-million and the yearly drift rate noted.

Application Note 86

APPENDIX F

OUTPUT STAGES

Some applications may require outputs other than the text circuit's 0V to 5V range. The simplest variation is a bipolar output, shown in Figure F1. The circuit, a summing inverter, subtracts the DAC output from a reference to obtain a bipolar output. Resistor and reference values may be varied to obtain different output excursions. The LT1010 output buffer provides drive capability and the chopper stabilized amplifier maintains $0.05\mu\text{V}/^\circ\text{C}$ stability. The resistors introduce a $0.3\text{ppm}/^\circ\text{C}$ error contribution¹

Figure F2 yields voltage gain by dividing the DAC output prior to its application to the feedback A-to-D. In this case, the 1:1 divider ratio sets a 10V output, assuming an A-to-D reference of 5V. As in Figure F1, the resistors add a slight temperature error, about $0.1\text{ppm}/^\circ\text{C}$ for the ratio set specified.²

Figure F3 uses active devices for voltage outputs as high as $\pm 100\text{V}$. The discrete high voltage stage is driven in closed-loop fashion by a chopper stabilized amplifier. Q1 and Q2 furnish voltage gain, and feed the Q3-Q4 emitter follower outputs. Q5 and Q6 set current limit at 25mA by diverting output drive when voltages across the 27 Ω shunts become too high. The local 1M-50k feedback pairs set stage gain at 20, allowing LTC1152 drives to cause full

$\pm 120\text{V}$ output swing. The local feedback reduces stage gain-bandwidth, making dynamic control easier. This stage is relatively simple to frequency compensate because only Q1 and Q2 contribute voltage gain. Additionally, the high voltage transistors have large junctions, resulting in low f_t s, and no special high frequency roll-off precautions are needed. Because the stage inverts, feedback is returned to the amplifier's positive input. Frequency compensation is achieved by rolling off the amplifier with the local $0.005\mu\text{F}$ -10k pair.

Heating and voltage coefficient errors are minimized in the feedback term by using four individual resistors. Trimming involves selecting the indicated resistor for exactly 100.0000V output with the DAC at full scale.

Figure F4 increases output current capability with a current gain stage inside the DAC output amplifier's feedback loop. This stage replaces the LT1010 150mA buffer shown in the text. The figure shows two options, differing in output capacity. It is worth noting that as output current rises, wiring resistance becomes a large potential error term. For example, at only 10mA output, 0.001Ω of wiring resistance introduces $10\mu\text{V}$ drop—a 2ppm error. Because of this, heavy loads should be supplied via short, highly conductive paths and remote sensing employed.

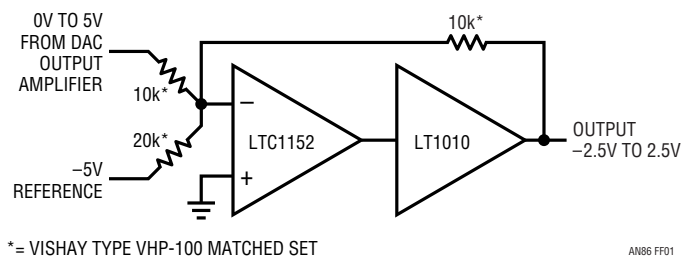


Figure F1. Precision Resistors and Chopper Stabilized Output Amplifier Allow Bipolar DAC Output. Trade-Off Is $\approx 0.3\text{ppm}/^\circ\text{C}$ Additional Resistor Based Error

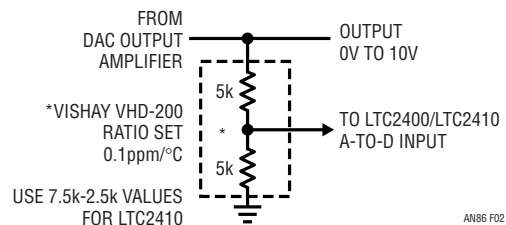


Figure F2. $\times 2$ Voltage Gain Obtained By Feedback Division at A-to-D. Slight Increase in Overall Temperature Coefficient Results

Note 1: See Note 1 in Appendix E.

Note 2: See above footnote.

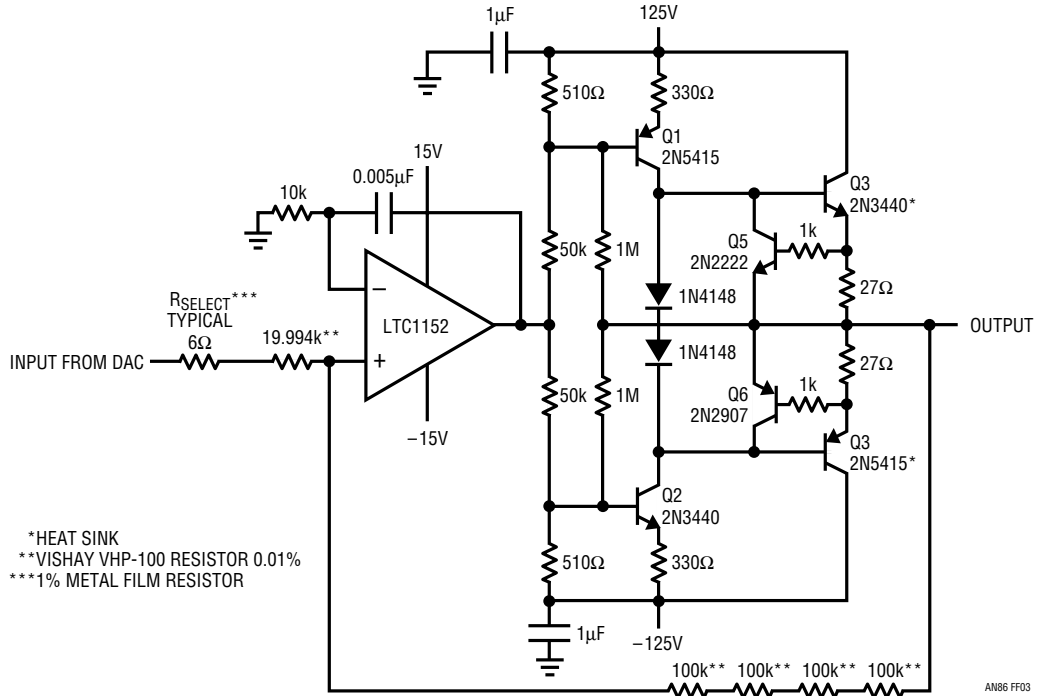


Figure F3. High Voltage Output Stage Delivers $\pm 100V$ at 25mA. Multiple Feedback Resistors Minimize Dissipation and Voltage Coefficient Effects

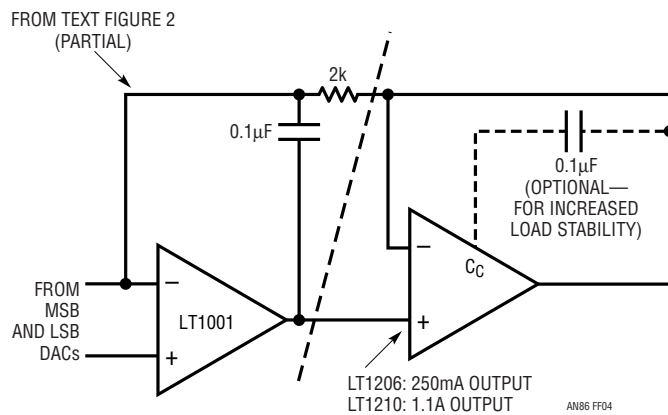


Figure F4. LT1206/LT1210 Output Stages Supply 250mA and 1.1A Loads, Respectively. Remote Sensing Is Usually Necessary to Compensate IR Drops

Application Note 86

APPENDIX G

MEASURING DAC SETTLING TIME

Measuring the 20-bit DAC's output settling time is a challenging task. Although the time scale involved is relatively slow, the $5\mu\text{V}$ LSB step size presents problems. The issue reduces to obtaining a great deal of gain without inducing overdrive in the monitoring oscilloscope. Such overdrive will corrupt the measurement, rendering displayed results meaningless.

Figure G1 is a solution. The DAC output is resistively balanced against a precision variable reference supply, adjustable in $0.5\mu\text{V}$ steps.¹ The circuit's remainder constitutes a clamped, distributed gain of 2000 amplifier. Diode clamping, placed at each gain stage input, prevents saturation from occurring even with large DAC-reference supply imbalances. The distributed gain allows 10kHz bandwidth while maintaining clamping effectiveness. The monitoring oscilloscope, operating at 5mV or $10\text{mV}/\text{DIV}$ ($5\mu\text{V}$ to $10\mu\text{V}$ at the DAC output), can readily discern $5\mu\text{V}$ settling without incurring deleterious overdrive.

Layout and construction of this circuit requires care. Figure G2 shows construction details. A linear layout minimizes parasitic feedback paths, preventing oscillation. The DAC input step is fully shielded, preventing feedthrough to various sensitive points within the amplifier. Finally, the entire circuit is built into a shielded enclosure to minimize effects of stray RF and pick up.

The circuit is tested by applying a test step that settles much faster than the DAC. Figure G3 uses a mercury wetted reed relay based pulse generator to supply the step. The unit noted is commercially produced, although similar results are obtainable with standard mercury based reed relays. When the relay opens the circuit's output settles essentially instantaneously (Figure G4) relative to DAC speed and settling time amplifier bandwidth.

Figure G1's response is tested by grounding one of its inputs and driving the other with the pulse generator. Figure G5 shows settling to within 1ppm ($\pm 5\mu\text{V}$) in 2ms. This is much faster than the DAC settles, lending confidence to text Figures 6 and 7 indicated results.

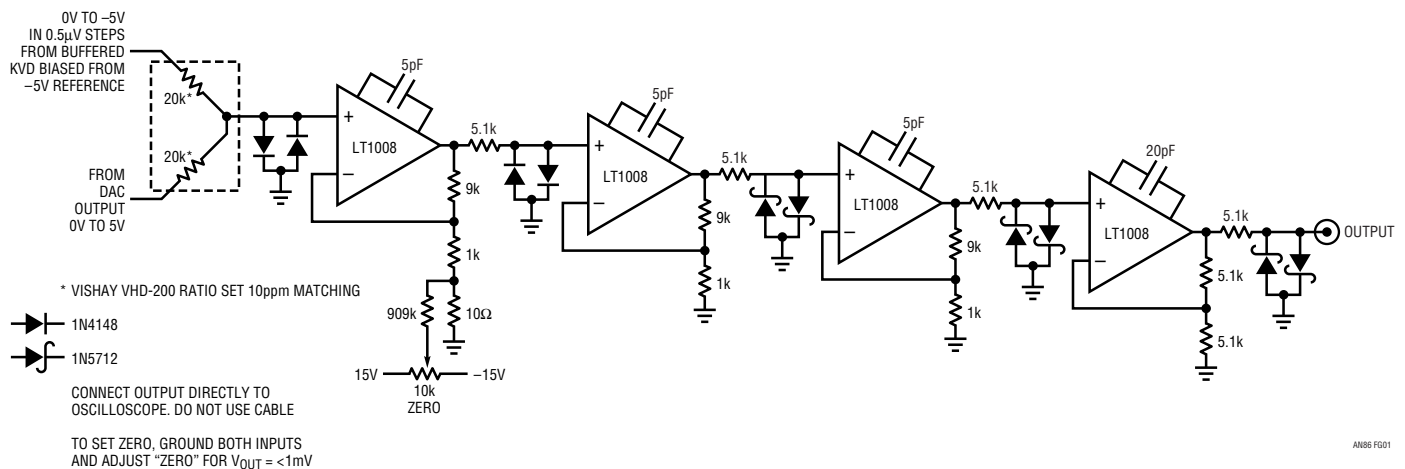


Figure G1. Clamped, Distributed Gain-of-2000 Amplifier Permits DAC Settling Time Measurement Without Saturation Effects

Note 1: See Appendix C for details on such a supply.



AN86 FG02.tif

Figure G2. Settling Time Amplifier Construction. Bandwidth Is Only 10kHz, Although Gain of 2000 Necessitates Layout Care to Avoid Parasitic Feedback Induced Oscillation. Input (Photo Lower Left) Is Fully Shielded, Preventing Radiative Feedthrough to Amplifier. Enclosure Shields Circuit from Stray RF and Pickup

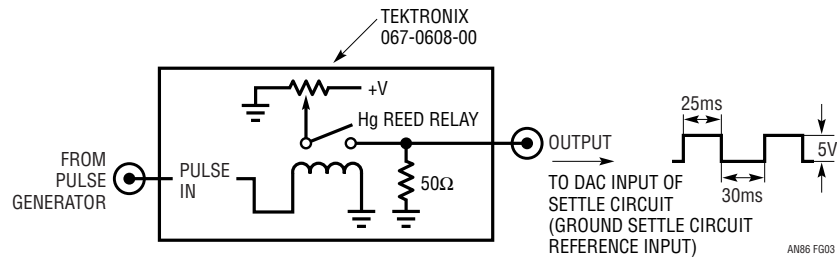
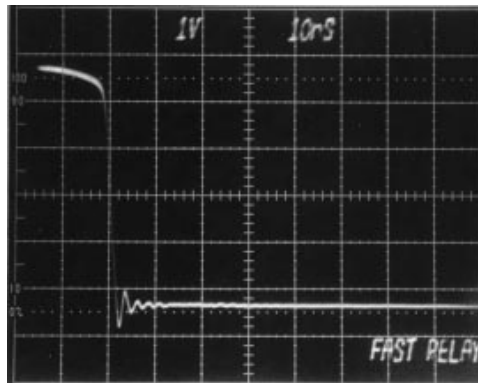
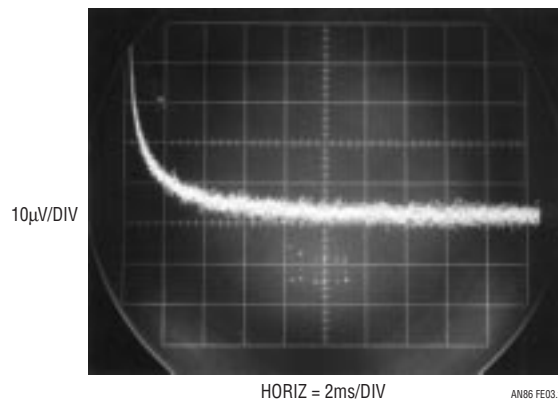


Figure G3. Reed Relay Based Pulser Supplies Clean Step to Test Settling Time Circuit



AN86 FG03.tif

Figure G4. Mercury Wetted Reed Relay Opens in 5 Nanoseconds, Settles Quickly to Zero. 500MHz Ring-Off Derives from Source-Termination Impedance Mismatch



AN86 FE03.tif

Figure G5. Settling Time Circuit Responds to Test Step with 2ms Settling to ±1ppm (±5μV)

APPENDIX H

MICROVOLT LEVEL NOISE MEASUREMENT

Verifying DAC output noise requires a quiet, high gain amplifier at the oscilloscope. Figure H1 shows one way to take the measurement. The input preamplifier, operating at a gain of 1000, supplies a high pass cutoff at 0.1Hz. It drives the oscilloscope via a 10Hz discrete low pass filter. The oscilloscope, set to 1mV/DIV, indicates 1 μ V/DIV referred to the preamplifier input. Figure H2 indicates DAC output noise well below an LSB, about 0.9 μ V. Equipment limitations set measurement noise floor at 0.2 μ V.

Figure H3 shows the noise measurement test setup. Note that the signal levels involved dictate a completely shielded, coaxial path from breadboard to oscilloscope.

Figure H4 lists some applicable high sensitivity amplifiers suitable for the noise measurement. Current generation oscilloscopes rarely have greater than 2mV/DIV sensitivity, although older instruments offer more capability. The figure lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These units

feature wideband, low noise performance. It is particularly significant that many of these instruments are no longer produced. This is in keeping with current instrumentation trends, which emphasize digital signal acquisition as opposed to analog measurement capability.

The monitoring oscilloscope should have exceptional trace clarity. In the latter regard high quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments is well-suited to low level noise measurement.¹ The digitizing uncertainties and raster scan limitations of DSOs impose display resolution penalties. Many DSO displays will not even register the fine structure of the noise waveform.

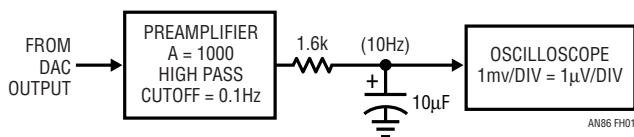


Figure H1. Microvolt Noise Measurement Necessitates High Gain Preamplifier for Oscilloscope. Preamplifier and Discrete Filter Set 0.1Hz to 10Hz Measurement Bandpass

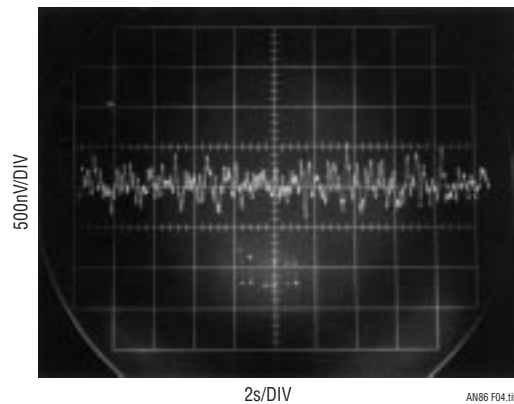


Figure H2. Indicated DAC Output Noise in a 0.1Hz to 10Hz Bandpass Is Below 1 μ V, About 0.2LSB. Equipment Limitations Set Measurement Noise Floor at 0.2 μ V

Note 1: In our work we have found Tektronix types 453, 453A, 454, 454A, 547 and 556 excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise floor limited background.



AN86 FH03.tif

Figure H3. Noise Measurement Test Setup Includes Shielded DAC Breadboard (Foreground), Preamplifier (Left) and Low Pass Filter Attached to Oscilloscope (Center). Measurement Path Is Fully Coaxial

INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	MAXIMUM BANDWIDTH	SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Differential Amplifier	Tektronix	1A7/1A7A	500kHz/1MHz	10 μ V/DIV	Secondary Market	Requires 500 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	7A22	1MHz	10 μ V/DIV	Secondary Market	Requires 7000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	5A22	1MHz	10 μ V/DIV	Secondary Market	Requires 5000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	ADA-400A	1MHz	10 μ V/DIV	Current Production	Standalone with Optional Power Supply, Settable Bandstops
Differential Amplifier	Tektronix	AM-502	1MHz	100,000	Secondary Market	Standalone with Optional Power Supply, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 1000	Current Production	Standalone, Settable Bandstops
Differential Amplifier	Stanford Research Systems	SR-560	1MHz	Gain = 50000	Current Production	Standalone, Settable Bandstops, Battery or Line Operation

Figure H4. Some Applicable High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Compatibility, Sensitivity and Availability

APPENDIX I

VOLTAGE REFERENCES

Figure I1 lists some voltage reference options for use with the DAC. The self-contained types are convenient and easily applied. The LM199A and the LTZ1000A require external circuitry but offer higher performance. All choices must be trimmed to establish absolute DAC accuracy. The LTZ1000A offers the highest stability and is discussed below.

Figure I2 shows the LTZ1000A and its support circuitry. A1 senses LTZ1000A die temperature and accordingly controls the IC heater via the 2N3904. A2 controls reference current. The Zener reference is sensed via Kelvin connections, minimizing voltage drop effects. A single point ground eliminates return current mixing and the attendant errors that would be produced.

Figure I3 offers choices for reference buffering. All employ a chopper stabilized amplifier augmented with a buffer output stage. Buffer error is extremely low, as noted in Appendix C's discussion. I3a, a simple unity-gain stage, transmits the input to the output with low error and minimal reference loading. I3b takes moderate gain, allowing a 7V reference input to produce (in this case) 10V at the output. I3c offers two ways to get 5V from the nominal 7V input. A precision divider lightly loads the reference in one case; the 5V output is taken at the LT1010. Reference loading is avoided by placing the divider at the output (optional case shown) and driving the A-to-D reference input from the divider output, which is permissible.

TYPE	VOLTAGE	INITIAL ACCURACY	TEMPERATURE DRIFT	LONG-TERM STABILITY	COMMENTS
LTZ1000A	7.2V	Minimum 7V Maximum 7.5V	0.05ppm/ $^{\circ}$ C	4ppm/Yr Typical	Highest Stability Zener Available. Requires External Heater Control and Reference Buffer Circuitry
LM199A	6.95V	2%	0.5ppm/ $^{\circ}$ C	10ppm/Yr Typical	Self-Contained, Including Heater Control Circuitry. Zener Output Is Unbuffered
LT1021	5V, 7V, 10V	0.05V (7V)	2ppm/ $^{\circ}$ C (7V)	20ppm/kHr Noncumulative	Fully Self-Contained. Trimmable
LT1027	5V	0.02%	2ppm/ $^{\circ}$ C	20ppm/kHr Noncumulative	Fully Self-Contained. Trimmable
LT1236	5V, 10V	0.05%	5ppm/ $^{\circ}$ C	20ppm/kHr Noncumulative	Fully Self-Contained. Trimmable

Figure I1. Reference Choices Compared for Output Voltage, Accuracy and Stability. Highest Stability Types Require External Circuitry

Application Note 86

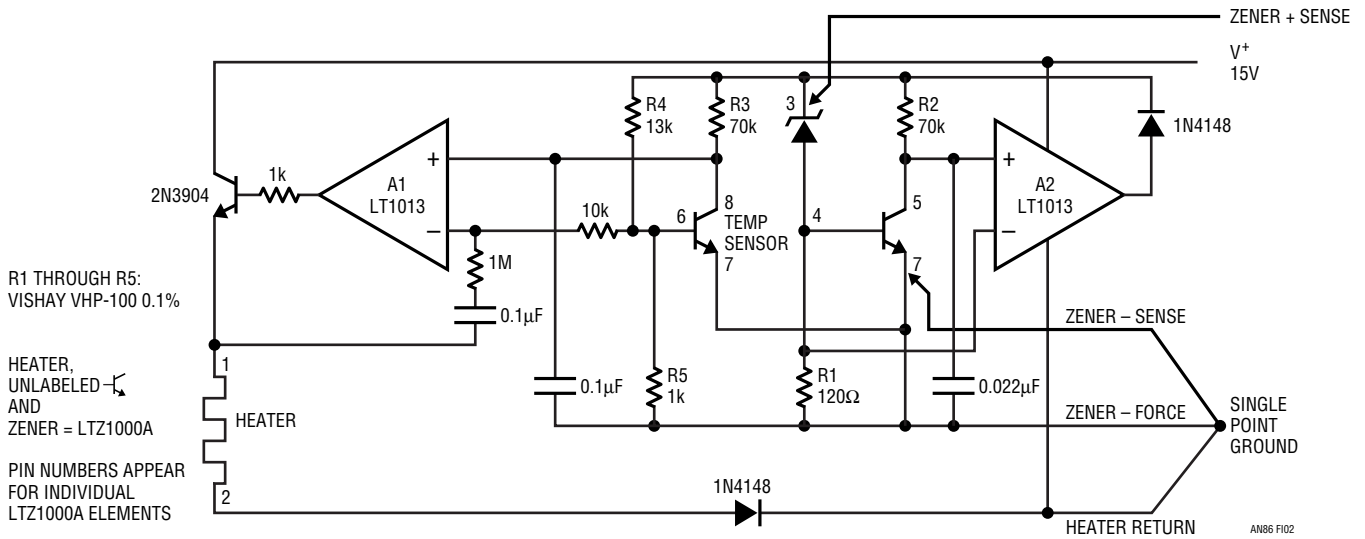


Figure 12. 7V Reference Includes A1 Heater Control Amplifier, A2 Zener Current Regulator and LTZ1000A Zener. Note Zener Kelvin Connections and Single Point Ground

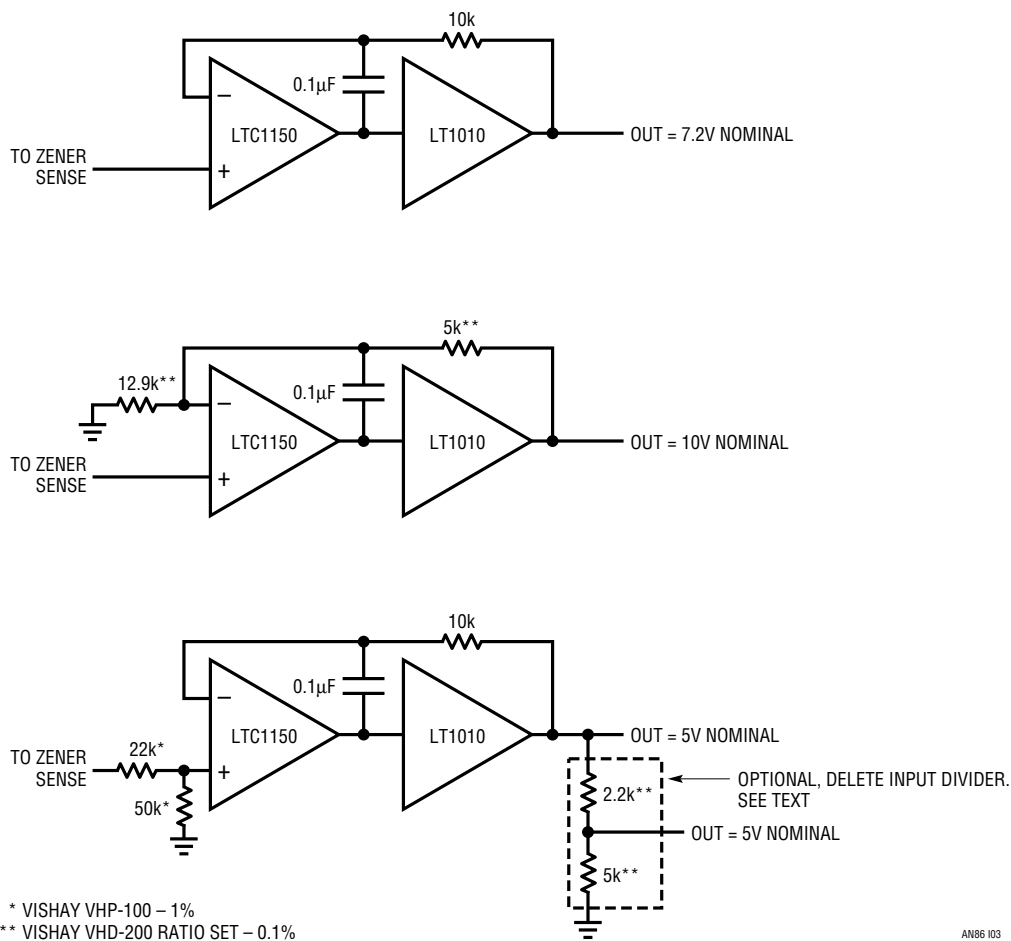


Figure 13. Chopper Stabilized Reference Buffer Options Include Unity Gain (a), 10V (b) and 5V (c) Output. Trimming Is Required for Absolute Accuracy

APPENDIX J

CABLES, CONNECTIONS, SOLDER, COMPONENT CHOICE, TERROR AND ARCANA

Subtle parasitic effects can have pronounced and seemingly inexplicable effects on low level circuit performance. Perhaps the most prevalent detractor to microvolt level circuitry is unintended thermocouples. Considerable discussion for dealing with thermocouples appeared in Appendix C and should be considered preliminary to this section's material.

In 1822, Thomas Seebeck, an Estonian physician, accidentally joined semicircular pieces of bismuth and copper (Figure J1) while studying thermal effects on galvanic arrangements. A nearby compass indicated a magnetic disturbance. Seebeck experimented repeatedly with different metal combinations at various temperatures, noting relative magnetic field strengths. Curiously, he did not believe that electric current was flowing and preferred to describe the effect as "thermomagnetism." He published his results in a paper, "Magnetische Polarisation der Metalle und Erze durch Temperatur-Differenz" (see References).

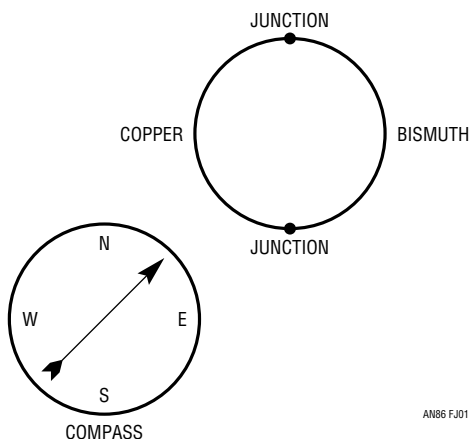


Figure J1. The Arrangement for Dr. Seebeck's Accidental Discovery of "Thermomagnetism"

Subsequent investigation has shown the "Seebeck Effect" to be fundamentally electrical in nature, repeatable and quite useful. Thermocouples, by far the most common transducer, are Seebeck's descendants. Unfortunately, unintended and unwanted thermocouples are also Seebeck's progeny.

In low drift circuits, unwanted thermocouples are probably the primary source of error. Connectors, switches, relay contacts, sockets, wire and even solder are all candidates for thermal EMF generation. It is relatively clear that connectors and sockets can form thermal junctions. However, it is not at all obvious that junctions of wire from different manufacturers can easily generate 200nV/°C—four times a precision amplifier's drift specification! Figure J2 shows a plot obtained for such a wire junction. Even solder can become an error term at low levels, creating a junction with copper or Kovar wires or PC traces (see Figure J3). Figure J4 lists thermocouple potentials for some common materials found in electronic assemblies.

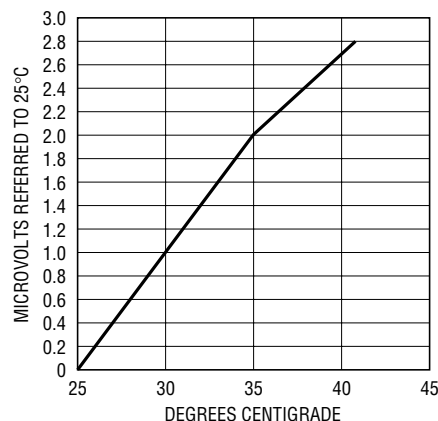


Figure J2. Thermal EMF Generated by Two "Identical" Copper Wires Due to Oxidation and Impurities

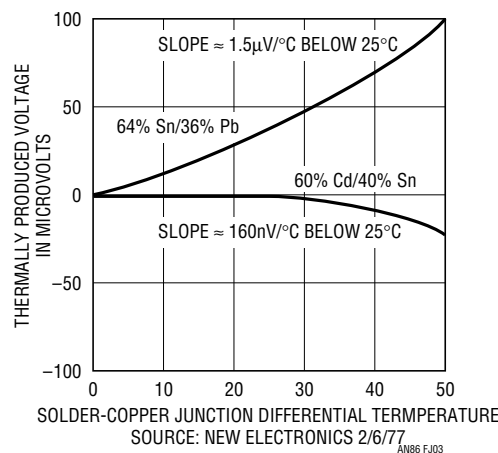


Figure J3. Solder-Copper Thermal EMFs. Cd/Sn Has Notably Lower Activity but Is Toxic, Not Available and Not Recommended

Application Note 86

The unusually energetic response of Cu-CuO necessitated the treatment described in Appendix C (Figure C7 and associated text) for cleaning DVM and Kelvin-Varley divider connections. Readers finding this figure's information seemingly academic should be awakened by Figure J5. This chart lists thermoelectric potentials for commonly employed laboratory connectors. Thermocouple activity of some types is more than 20 times greater than others. Be careful!

Minimizing thermal EMF induced errors is possible if judicious attention is given to circuit board layout. In general, it is good practice to limit the number of junctions in the signal path. Avoid connectors, sockets, switches and other potential error sources to the extent possible. In some cases this will not be possible. In these instances, attempt to balance the number and type of junctions in the signal path so that differential cancellation occurs. Doing this may involve deliberately creating and introducing junctions to offset unavoidable junctions. This can be a tricky procedure. Repeated deliberate temperature excursions may be necessary to determine the optimal number and placement of added junctions. Experimentation, tempered by a healthy reserve of patience and abundance of time, is required. This practice, borrowed from standards lab procedures, can be quite effective in reducing thermal

EMF originated drifts. Figure J6 shows a simple example where a nominally unnecessary resistor is included to promote such thermal balancing. For remote signal sources connectors may be unavoidable. In these cases, choose a connector specified for relatively low thermal EMF activity and ensure a similarly balanced approach in routing signals through the connector along the circuit board and to circuitry. If some imbalance is unavoidable, deliberately introduce an intentional counterbalancing junction. In all cases maintain the differencing junctions in close physical proximity, which will keep them at the same temperature. Avoid drafts and temperature gradients, which can introduce thermal imbalances and cause problems. Figure J7 shows the LTC1150 set up in a test circuit to measure its temperature stability. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity each input sees is also balanced because of the symmetrical connection of the resistors and their identical size. Thus, thermal EMF induced shifts are equal in phase and amplitude and cancellation occurs. Very slight air currents can still affect even this arrangement. Figure J8 shows a strip chart of output noise with the circuit covered by a small styrofoam cup (HANDI-KUP™ Company Model H8-S) and with no cover in "still" air. This data illustrates why it is often prudent to enclose low level circuitry inside some form of thermal baffle.

MATERIALS	POTENTIAL ($\mu\text{V}/^\circ\text{C}$)
Cu-Cu	< 0.2
Cu-Ag	0.3
Cu-Au	0.3
Cu-Cd/Sn	0.3
Cu-Pb/Sn	1 to 3
Cu-Kovar	40
Cu-Si	400
Cu-CuO	1000

Source: Low Level Measurements,
Keithley Instruments, 1984
(see References)

Figure J4. Thermoelectric Potentials for Various Materials Indicates Inadvisability of Mixing Materials in Signal Path. Cu-Cu Connections (Chart Top) Must Be Kept Clean or 5000:1 Degradation Occurs As They Oxidize (Chart Bottom)

HANDI-KUP is a trademark of WinCup.










CONNECTION TYPE	DESCRIPTION	THERMOELECTRIC POTENTIAL ($\mu\text{V}/^\circ\text{C}$)
BNC-BNC Mate		0.4
BNC-Banana Adapter		0.35
BNC-BNC "Barrel" Adapter		0.4
Male/Female Banana Mate Sample #1		0.35
Male/Female Banana Mate Sample #2		1.1
Male/Female Banana Mate (Type Specified for Low Thermal Activity) Sample #3		0.07
Copper Lug-Copper Banana Binding Post		0.08
Copper Lug-Standard Banana Binding Post		0.5
Plated Lug-Copper Banana Binding Post		1.7

Figure J5. Measured Thermoelectric Potentials for Some Common Laboratory Connectors. Pronounced Difference Between "Banana" Samples Is Due to Manufacturer's Materials Choice. Note That Copper Lug/Copper Banana Post Has 20× Lower Activity Than Plated Lug/Copper Banana Post

Application Note 86

Thermal EMFs are the most likely, but not the only, potential low level error source. Electrostatic and electromagnetic shielding may be required. Power supply transformer fields are notorious sources of errors often mistakenly attributed to amplifier DC drift and noise. A transformer's magnetic field impinging on a PC trace can easily generate microvolts across that conductor in accordance with well known magnetic theory. The circuit cannot distinguish between this spurious signal and the desired input. Attempts to eliminate the problem by rolling off circuit response may work, but often the filtered version of the undesired pickup masquerades as an unstable DC term. The most direct approach is to use shielded transformers but careful layout may be equally effective and less costly. A circuit that requires the transformer to be close by to achieve a good quality grounding scheme may be disturbed by the transformer's magnetic field. An RF

choke connected across a scope probe can determine the presence and relative intensity of transformer fields, aiding layout experimentation.

Another source of parasitic error is stray leakage current. Such leakage currents must be prevented from influencing circuit operation. The simplest way to do this is to connect leakage sensitive points via teflon standoffs. Because the points never contact the PC board, stray leakage currents do not affect them. Although this approach is effective, its implementation may not be acceptable in production. Guarding is another technique for minimizing board leakage effects. The guard is a PC trace completely encircling the leakage sensitive points. This trace is driven at a potential equal to that of the point, preventing leakage to the "guarded" point. On PC boards, the guard should enclose the node(s) to be protected. Guarding was used to eliminate the effects of capacitor surface leakage in Appendix C's Figure C7.

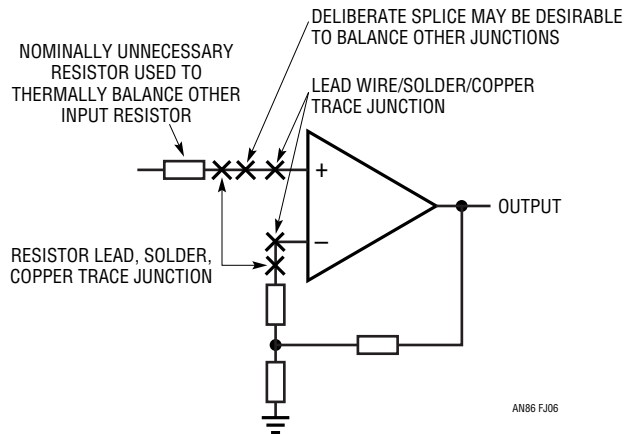


Figure J6. Typical Thermal Layout Considerations Emphasize Minimizing and Differencing Parasitic Thermocouples. Thermal Mass at Amplifier Inputs Should Be Equal, Allowing Differenced Parasitic Thermocouple Outputs to Arrive Matched In Phase and Amplitude

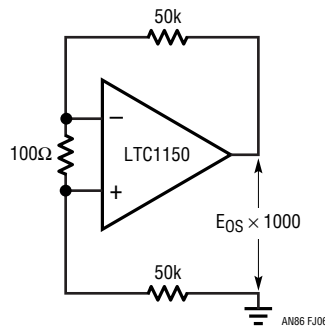


Figure J7. Amplifier Drift Test Circuit. Thermal EMFs and Thermal Capacity at Each Input Must Be Similar for Cancellation to Occur

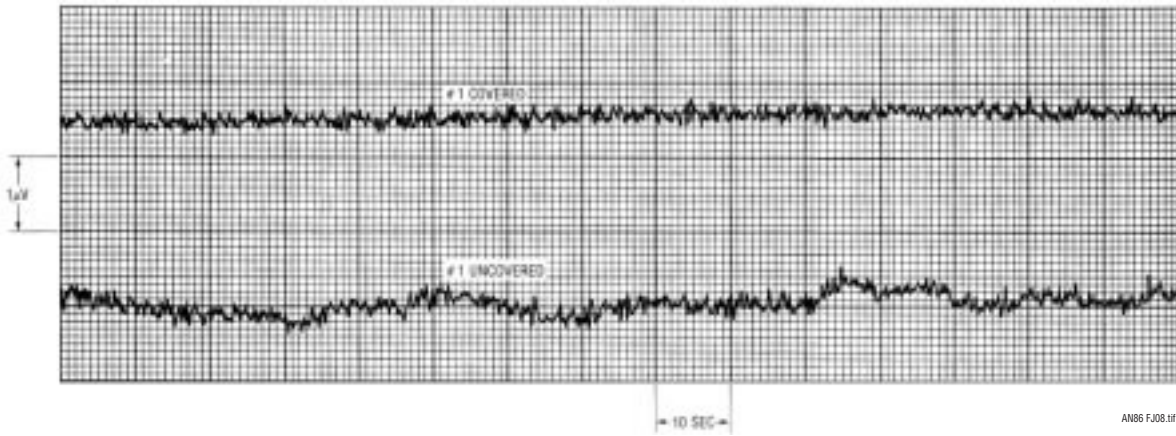
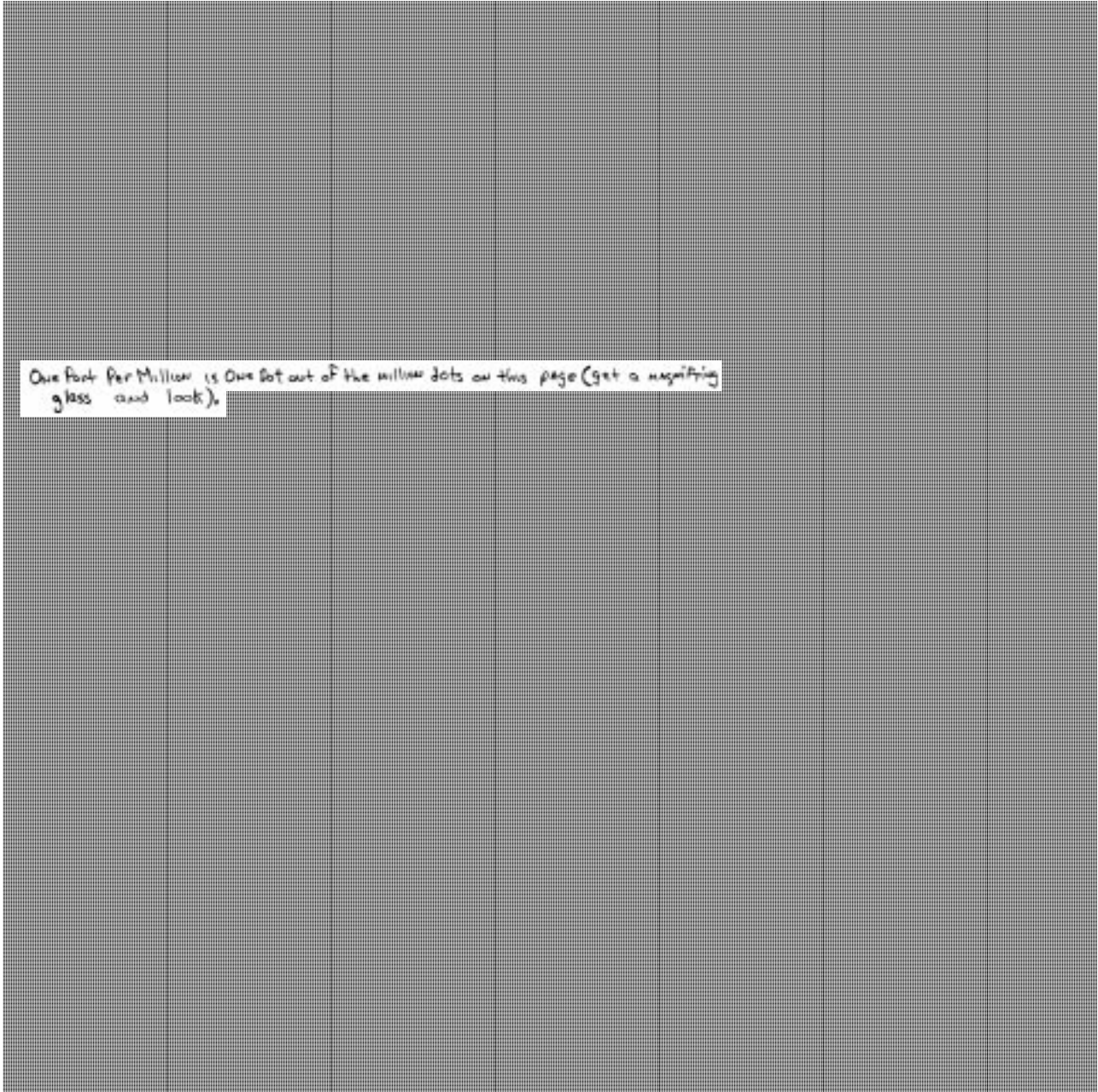


Figure J8. Effect of Thermal Baffle on Low Frequency Amplifier Noise in “Still” Air. Amplifier Is Covered By Small Cup in Upper Trace, Uncovered in Lower Trace. Instability Worsens If Air Movement Increases

Application Note 86



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A Thermoelectric Cooler Temperature Controller for Fiber Optic Lasers

Climatic Pampering for Temperamental Lasers

Jim Williams

INTRODUCTION

Continued demands for increased bandwidth have resulted in deployment of fiber optic-based networks. The fiber optic lines, driven by solid state lasers, are capable of very high information density. Highly packed data schemes such as DWDM (dense wavelength division multiplexing) utilize multiple lasers driving a fiber to obtain large multi-channel data streams. The narrow channel spacing relies on laser wavelength being controlled within 0.1nm (nanometer). Lasers are capable of this but temperature variation influences operation. Figure 1 shows that laser output peaks sharply vs wavelength, implying that laser wavelength must be controlled well within 0.1nm to maintain performance. Figure 2 plots typical laser wavelength vs temperature. The 0.1nm/°C slope means that although temperature facilitates tuning laser wavelength, it must not vary once the laser has been peaked. Typically, temperature control of 0.1°C is required to maintain laser operation well within 0.1nm.

Temperature Controller Requirements

The temperature controller must meet some unusual requirements. Most notably, because of ambient temperature variation and laser operation uncertainties, the controller must be capable of either sourcing or removing heat to maintain control. Peltier-based thermoelectric coolers (TEC) permit this but the controller must be truly bidirectional. Its heat flow control must not have dead zone or untoward dynamics in the “hot-to-cold” transition region. Additionally, the temperature controller must be a precision device capable of maintaining control well inside 0.1°C over time and temperature variations.

Laser based systems packaging is compact, necessitating small solution size with efficient operation to avoid excessive heat dissipation. Finally, the controller must operate from a single, low voltage source and its (presumably switched mode) operation must not corrupt the supply with noise.

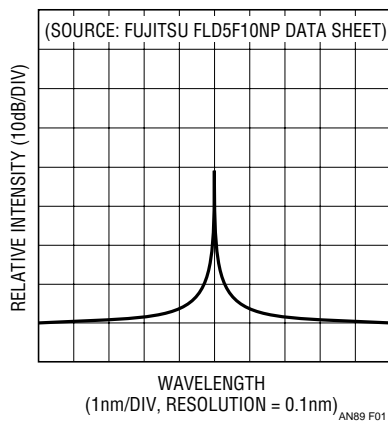


Figure 1. Laser Intensity Peak Approaches 40dB within a 1nm Window

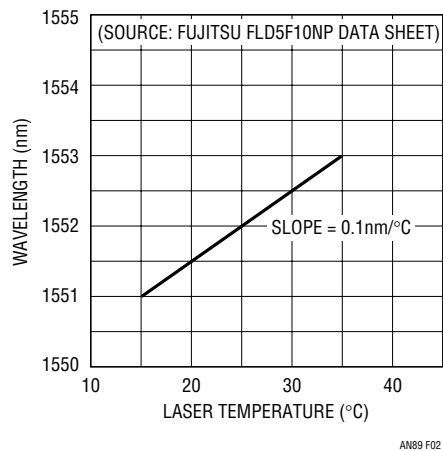


Figure 2. Laser Wavelength Varies $\approx 0.1\text{nm}/^\circ\text{C}$. Typical Application Requires Wavelength Stability within 0.1nm, Mandating Temperature Control

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Application Note 89

Temperature Controller Details

Figure 3, a schematic of the thermoelectric cooler (TEC) temperature controller, includes three basic sections. The DAC and the thermistor form a bridge, the output of which is amplified by A1. The LTC1923 controller is a pulse width modulator which provides appropriately modulated and phased drive to the power output stage. The laser is an electrically delicate and very expensive load. As such, the controller provides a variety of monitoring, limiting and overload protection capabilities. These include soft-start and overcurrent protection, TEC voltage and current sense and “out-of-bounds” temperature sensing. Aberrant operation results in circuit shutdown, preventing laser module damage. Two other features promote system level compatibility. A phase-locked loop based oscillator permits reliable clock synchronization of multiple LTC1923s in multilaser systems. Finally, the switched mode power delivery to the TEC is efficient but special considerations are required to ensure that switching related noise is not introduced (“reflected”) into the host power supply. The LTC1923 includes edge slew limiting which minimizes

switching related harmonics by slowing down the power stages’ transition times. This greatly reduces high frequency harmonic content, preventing excessive switching related noise from corrupting the power supply or the laser.¹ The switched mode power output stage, an “H-bridge” type, permits efficient bidirectional drive to the TEC, allowing either heating or cooling of the laser. The thermistor, TEC and laser, packaged at manufacture within the laser module, are tightly thermally coupled.

The DAC permits adjusting temperature setpoint to any individual laser’s optimum operating point, normally specified for each laser. Controller gain and bandwidth adjustments optimize thermal loop response for best temperature stability.

Thermal Loop Considerations

The key to high performance temperature control is matching the controller’s gain bandwidth to the thermal feedback path. Theoretically, it is a simple matter to do this using conventional servo-feedback techniques. Practi-

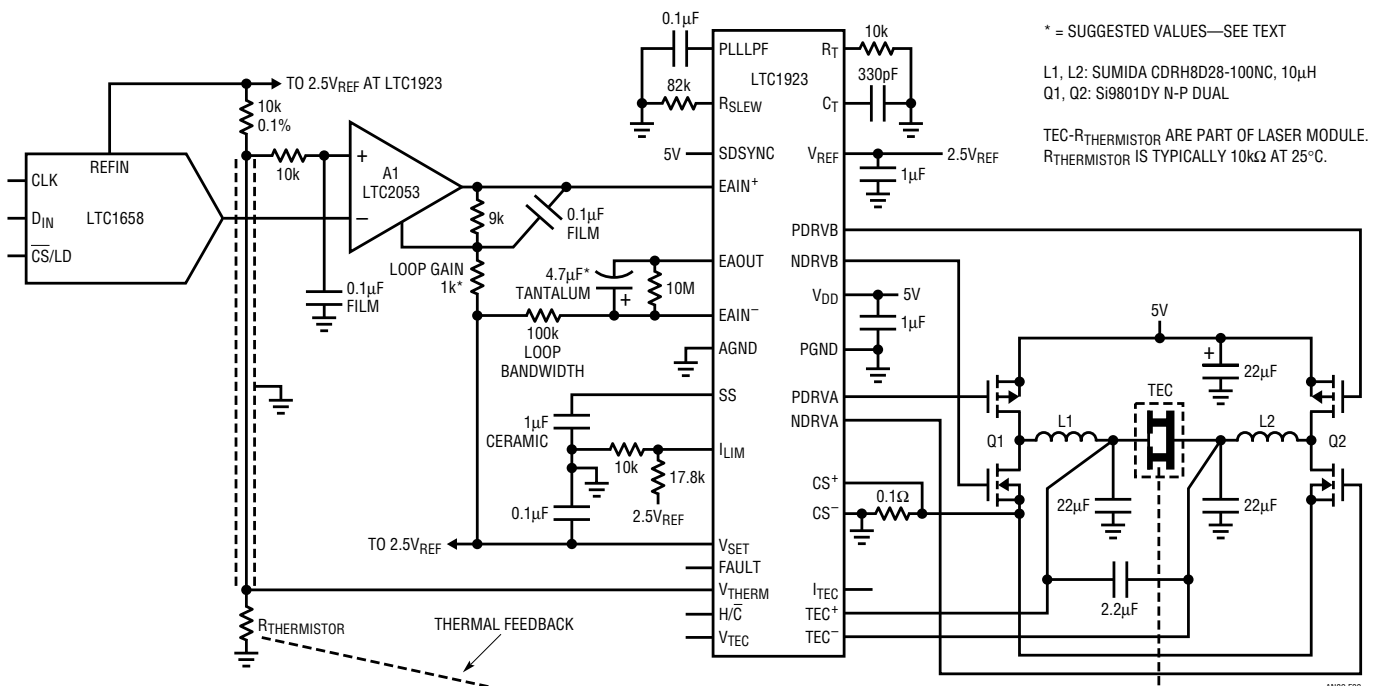


Figure 3. Detailed Schematic of TEC Temperature Controller Includes A1 Thermistor Bridge Amplifier, LTC1923 Switched Mode Controller and Power Output H-Bridge. DAC Establishes Temperature Setpoint. Gain Adjust and Compensation Capacitor Optimize Loop Gain Bandwidth. Various LTC1923 Outputs Permit Monitoring TEC Operating Conditions

Note 1: This technique derives from earlier efforts. See Reference 1 for detailed discussion and related topics.

cally, the long time constants and uncertain delays inherent in thermal systems present a challenge. The unfortunate relationship between servo systems and oscillators is very apparent in thermal control systems.

The thermal control loop can be very simply modeled as a network of resistors and capacitors. The resistors are equivalent to the thermal resistance and the capacitors to thermal capacity. In Figure 4 the TEC, TEC-sensor interface and sensor all have RC factors that contribute to a lumped delay in the system's ability to respond. To prevent oscillation, gain bandwidth must be limited to account for this delay. Since high gain bandwidth is desirable for good control, the delays should be minimized. This is presumably addressed by the laser module's purveyor at manufacture.

The model also includes insulation between the controlled environment and the uncontrolled ambient. The function of insulation is to keep the loss rate down so the temperature control device can keep up with the losses. For any given system, the higher the ratio between the TEC-sensor time constants and the insulation time constants, the better the performance of the control loop.²

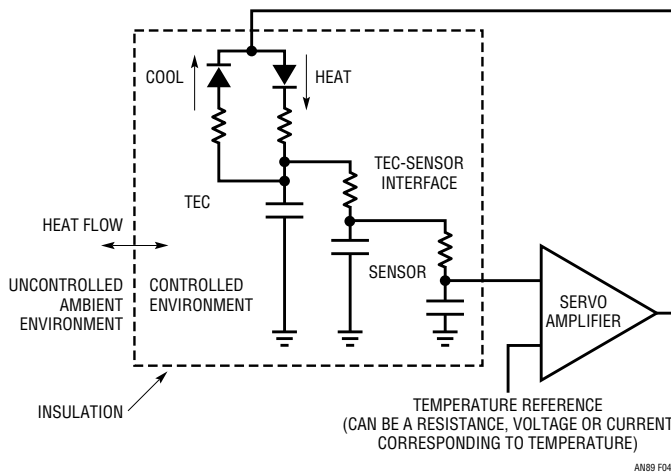


Figure 4. Simplified TEC Control Loop Model Showing Thermal Terms. Resistors and Capacitors Represent Thermal Resistance and Capacity, Respectively. Servo Amplifier Gain Bandwidth Must Accommodate Lumped Delay Presented by Thermal Terms to Avoid Instability

Temperature Control Loop Optimization

Temperature control loop optimization begins with thermal characterization of the laser module. The previous section emphasized the importance of the ratio between the TEC-sensor and insulation time constants. Determination of this information places realistic bounds on achievable controller gain bandwidth. Figure 5 shows results when a typical laser module is subjected to a 40°C step change in ambient temperature. The laser module's internal temperature, monitored by its thermistor, is plotted vs time with the TEC unpowered. An ambient-to-sensor lag measured in minutes shows a classic first order response.

The TEC-sensor lumped delay is characterized by operating the laser module in Figure 3's circuit with gain set at maximum and no compensation capacitor installed. Figure 6 shows large-signal oscillation due to thermal lag dominating the loop. A great deal of valuable information is contained in this presentation.³ The frequency, primarily determined by TEC-sensor lag, implies limits on how much loop bandwidth is achievable. The high ratio of this frequency to the laser module's thermal time constant (Figure 5) means a simple, dominant pole loop compen-

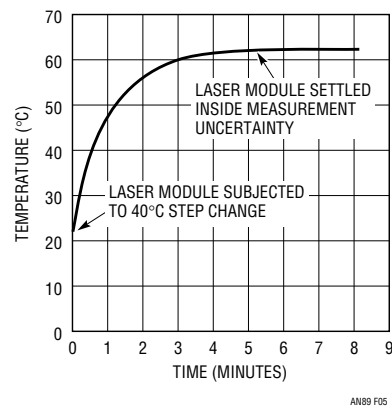


Figure 5. Ambient-to-Sensor Lag Characteristic for a Typical Laser Module Is Set by Package Thermal Resistance and Capacity

Note 2: For the sake of text flow, this somewhat academic discussion must suffer brevity. However, additional thermodynamic gossip appears in Appendix A, "Practical Considerations in Thermoelectric Cooler Based Control Loops."

Note 3: When a circuit "doesn't work" because "it oscillates," whether at millihertz or gigahertz, four burning questions should immediately dominate the pending investigation. What frequency does it oscillate at, what is the amplitude, duty cycle and waveshape? The solution invariably resides in the answers to these queries. Just stare thoughtfully at the waveform and the truth will bloom.

Application Note 89

sation will be effective. The saturation limited waveshape suggests excessive gain is driving the loop into full cooling and heating states. Finally, the asymmetric duty cycle reflects the TEC's differing thermal efficiency in the cooling and heating modes.

Controller gain bandwidth reduction from Figure 6's extremes produced Figure 7's display. The waveform results from a small step ($\approx 0.1^\circ\text{C}$) change in temperature setpoint. Gain bandwidth is still excessively high, producing a damped, ringing response over 2 minutes in duration! The loop is just marginally stable. Figure 8's test conditions are identical but gain bandwidth has been significantly reduced. Response is still not optimal but settling occurs in

≈ 4.5 seconds, about 25x faster than the previous case. Figure 9's response, taken at further reduced gain bandwidth settings, is nearly critically damped and settles cleanly in about 2 seconds. A laser module optimized in this fashion will easily attenuate external temperature shifts by a factor of thousands without overshoots or excessive lags. Further, although there are substantial thermal differences between various laser modules, some generalized guidelines on gain bandwidth values are possible.⁴ A DC gain of 1000 is sufficient for required temperature control, with bandwidth below 1 Hz providing adequate loop stability. Figure 3's suggested gain and bandwidth values reflect these conclusions, although stability testing for any specific case is mandatory.

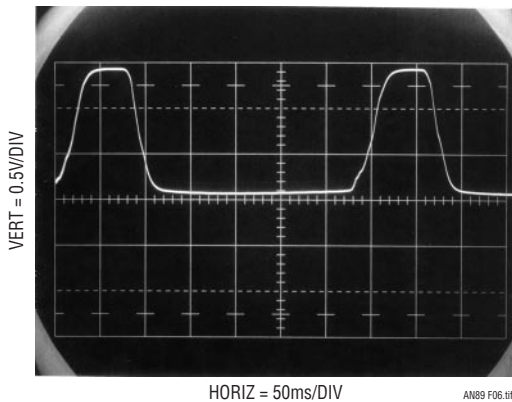


Figure 6. Deliberate Excess of Loop Gain Bandwidth Introduces Large-Signal Oscillation. Oscillation Frequency Provides Guidance for Achievable Closed-Loop Bandwidth. Duty Cycle Reveals Asymmetric Heating-Cooling Mode Gains

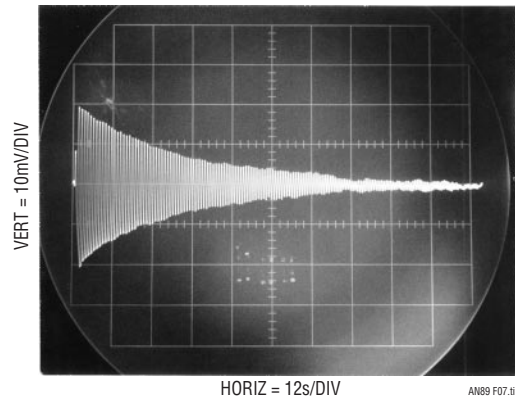


Figure 7. Loop Response to Small Step in Temperature Setpoint. Gain Bandwidth Is Excessively High, Resulting in Damped, Ringing Response Over 2 Minutes in Duration

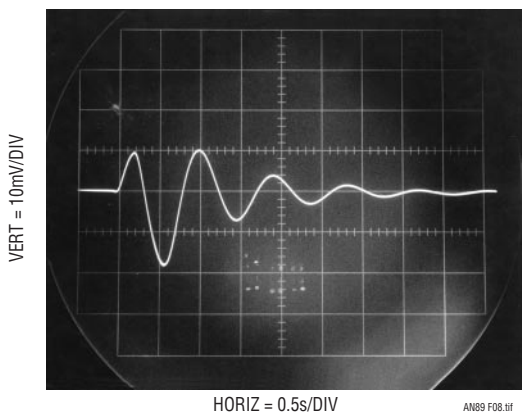


Figure 8. Same Test Conditions as Figure 7 but at Reduced Loop Gain Bandwidth. Loop Response Is Still Not Optimal but Settling Occurs in 4.5 Seconds—Over 25x Faster than Previous Case

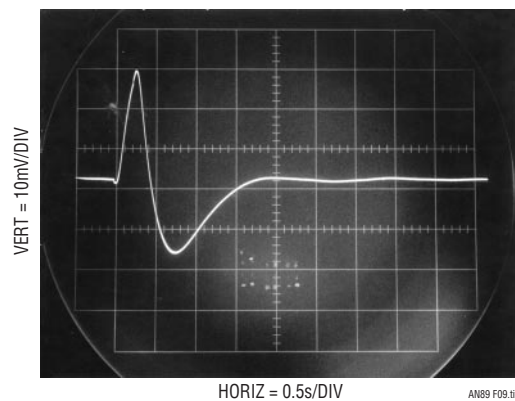


Figure 9. Gain Bandwidth Optimization Results in Nearly Critically Damped Response with Settling in 2 Seconds

Note 4: See Appendix A, "Practical Considerations in Thermoelectric Cooler Based Control Loops," for additional comment.

Temperature Stability Verification

Once the loop has been optimized, temperature stability can be measured. Stability is verified by monitoring thermistor bridge offset with a stable, calibrated differential amplifier.⁵ Figure 10 records ± 1 millidegree baseline stability over 50 seconds in the cooling mode. A more stringent test measures longer term stability with significant variations in ambient temperature. Figure 11's strip-chart recording measures cooling mode stability against an environment that steps 20°C above ambient every hour over 9 hours.⁶ The data shows 0.008°C resulting variation,

indicating a thermal gain of 2500.⁷ The 0.0025°C baseline tilt over the 9 hour plot length derives from varying ambient temperature. Figure 12 utilizes identical test conditions, except that the controller operates in the heating mode. The TEC's higher heating mode efficiency furnishes greater thermal gain, resulting in a 4x stability improvement to about 0.002°C variation. Baseline tilt, just detectable, shows a similar 4x improvement vs Figure 11.

This level of performance ensures the desired stable laser characteristics. Long-term (years) temperature stability is primarily determined by thermistor aging characteristics.⁸

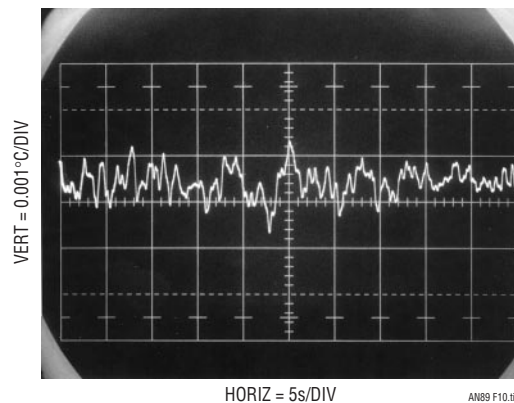


Figure 10. Short-Term Monitoring in Room Environment Indicates 0.001°C Cooling Mode Baseline Stability

Note 5: This measurement monitors thermistor stability. Laser temperature stability will be somewhat different due to slight thermal decoupling and variations in laser power dissipation. See Appendix A.

Note 6: That's right, a *strip-chart recording*. Stubborn, locally based aberrants persist in their use of such archaic devices, forsaking more modern alternatives. Technical advantage could account for this choice, although deeply seated cultural bias may be a factor.

Note 7: Thermal gain is temperature control aficionado jargon for the ratio of ambient-to-controlled temperature variation.

Note 8: See Appendix A for additional information.

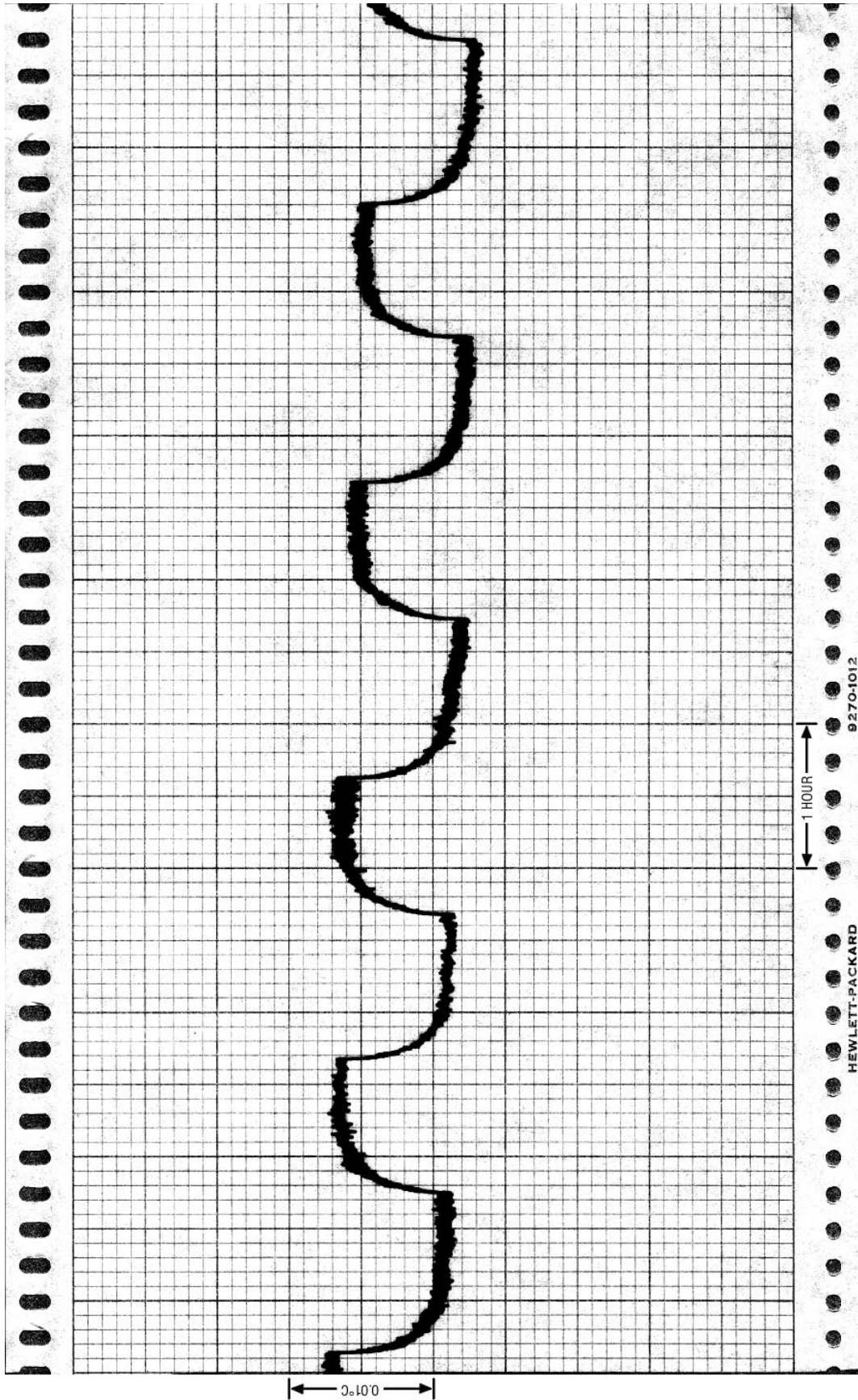


Figure 11. Long-Term Cooling Mode Stability Measured in Environment that Steps 20 Degrees Above Ambient Every Hour. Data Shows Resulting 0.008°C Peak-to-Peak Variation, Indicating Thermal Gain of 2500. 0.0025°C Baseline Tilt Over Plot Length Derives From Varying Ambient Temperature

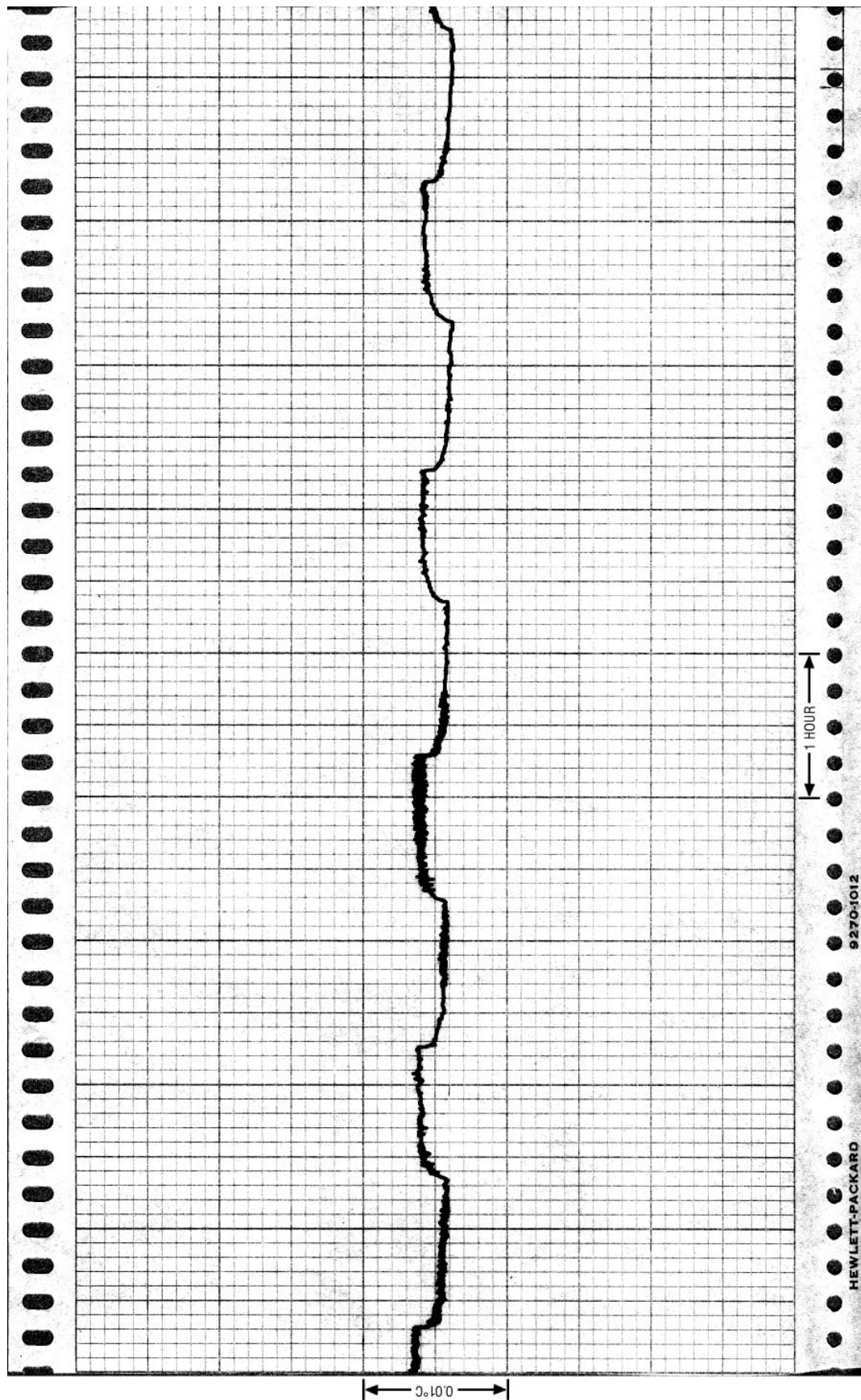


Figure 12. Identical Test Conditions as Figure 11, Except in Heating Mode. TEC's Higher Heating Mode Efficiency Results in Higher Thermal Gain. 0.002°C Peak-to-Peak Variation Is 4x Stability Improvement. Baseline Tilt, Just Detectable, Shows Similar 4x Improvement vs Figure 11

Application Note 89

Reflected Noise Performance

The switched mode power delivery to the TEC provides efficient operation but raises concerns about noise injected back into the host system via the power supply. In particular, the switching edge's high frequency harmonic content can corrupt the power supply, causing system level problems. Such "reflected" noise can be troublesome to deal with. The LTC1923 avoids these issues by controlling the slew of its switching edges, minimizing high frequency harmonic content.⁹ This slowing down of switching transients typically reduces efficiency by only 1% to 2%, a small penalty for the greatly improved noise performance. Figure 13 shows noise and ripple at the 5V supply with slew control in use. Low frequency ripple,

12mV in amplitude, is usually not a concern, as opposed to the high frequency transition related-components, which are much lower. Figure 14, a time and amplitude expansion of Figure 13, more clearly studies high frequency residue. High frequency amplitude, measured at center screen, is about 1mV. The slew limiting's effectiveness is measured in Figure 15 by disabling it. High frequency content jumps to nearly 10mV, almost 10x worse performance. Leave that slew limiting in there!

Most applications are well served by this level of noise reduction. Some special cases may require even lower reflected noise. Figure 16's simple LC filter may be employed in these cases. Combined with the LTC1923's slew limiting, it provides vanishingly small reflected ripple and

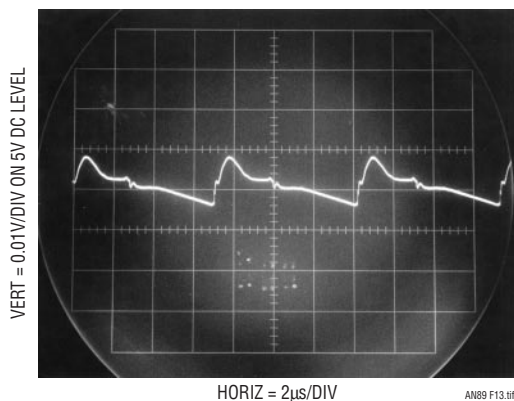


Figure 13. "Reflected" Noise at 5VDC Input Supply Due to Switching Regulator Operation with Edge Slew Rate Limiting in Use. Ripple Is 12mV_{P-P}, High Frequency Edge Related Harmonic Is Much Lower

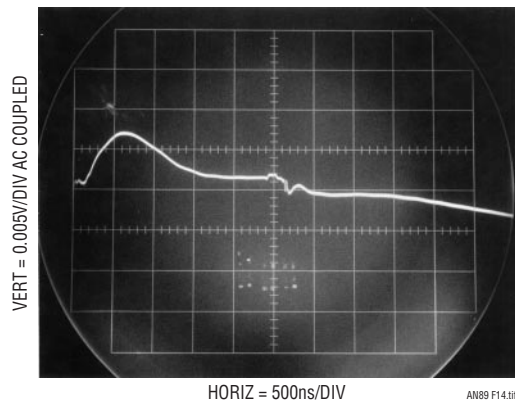


Figure 14. Time and Amplitude Expansion of Figure 13 More Clearly Shows Residual High Frequency Content with Slew Limiting Employed

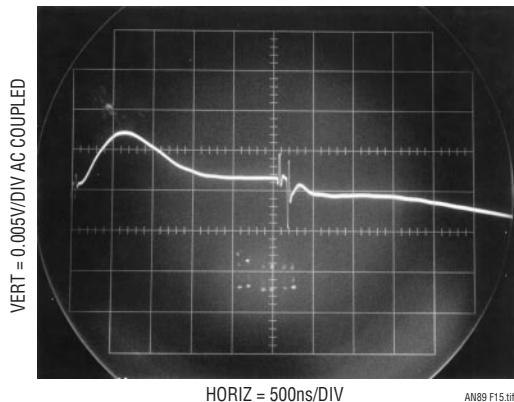


Figure 15. Same Test Conditions as Previous Figure, Except Slew Limiting Is Disabled. High Frequency Harmonic Content Rises \approx x10. Leave that Slew Limiting in There!

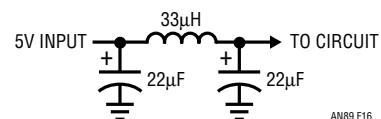


Figure 16. LC Filter Produces 1mV Reflected Ripple and 500µV High Frequency Harmonic Noise Residue

Note 9: This technique derives from previous work. See Reference 1.

high frequency harmonics. Figure 17, taken using this filter, shows only about 1mV of ripple, with submillivolt levels of high frequency content. Figure 18 expands the time scale to examine the high frequency remnants. Amplitude is 500 μ V, about 1/3 Figure 14's reading. As before,

slew limiting effectiveness is measurable by disabling it. This is done in Figure 19, with a resulting 4.4x increase in high frequency content to about 2.2mV. As in Figure 15, if lowest reflected noise is required, leave that slew limiting in there!

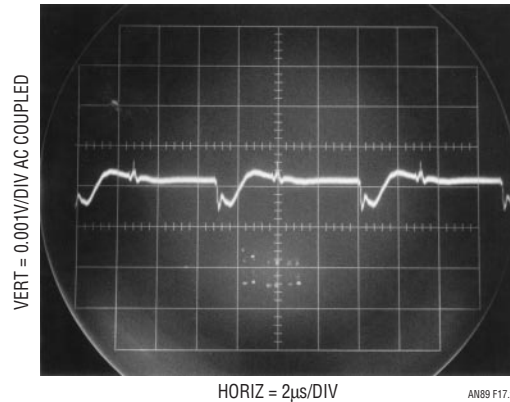


Figure 17. 5V Supply Reflected Ripple Measures 1mV with Figure 16's LC Filter in Use, a 10x Reduction Over Figure 13. Switching Edge Related Harmonic Content Is Small Due to Slew Limiting Action

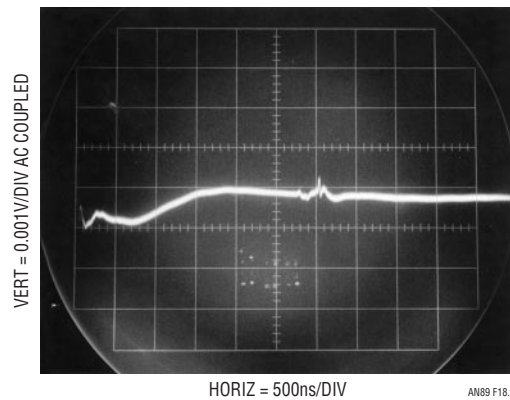


Figure 18. Horizontal Expansion Permits Study of High Frequency Harmonic with Slew Limiting Enabled. Amplitude Is 500 μ V, About 1/3 Figure 14's Reading

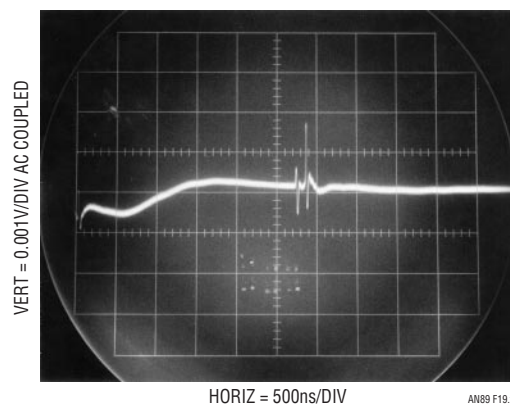


Figure 19. Same Conditions as Previous Figure, Except Slew Limiting Is Disabled. Harmonic Content Amplitude Rises to 2.2mV, a 4.4x Degradation. As in Figure 15, Leave that Slew Limiting in There!

Application Note 89

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Note: This Application Note was derived from a manuscript originally prepared for publication in EDN magazine.

APPENDIX A

PRACTICAL CONSIDERATIONS IN THERMOELECTRIC COOLER BASED CONTROL LOOPS

There are a number of practical issues involved in implementing thermoelectric cooler (TEC) based control loops. They fall within three loosely defined categories. These include temperature setpoint, loop compensation and loop gain. Brief commentary on each category is provided below.

Temperature Setpoint

It is important to differentiate between temperature accuracy and stability requirements. The exact temperature setpoint is not really important, so long as it is stable. Each individual laser's output maximizes at some temperature (see text Figures 1 and 2). Temperature setpoint is typically incremented until this peak is achieved. After this, only temperature setpoint stability is required. This is why thermistor tolerances on laser module data sheets are relatively loose (5%). Long-term (years) temperature setpoint stability is primarily determined by thermistor stability over time. Thermistor time stability is a function of operating temperatures, temperature cycling, moisture contamination and packaging. The laser modules' relatively mild operating conditions are very benign, promoting good long-term stability. Typically, assuming good grade thermistors are used at module fabrication, thermistor stability comfortably inside 0.1°C over years may be expected.

Also related to temperature setpoint is that the servo loop controls *sensor* temperature. The laser operates at a somewhat different temperature, although laser temperature stability depends upon the stable loop controlled environment. The assumption is that laser dissipation constant remains fixed, which is largely true.¹

Loop Compensation

Figure 3's "dominant pole" compensation scheme takes advantage of the long time constant from ambient into the laser module (see text Figure 5). Loop gain is rolled off at a frequency low enough to accommodate the TEC-thermistor lag (see text Figure 6) but high enough to smooth transients arriving from the outside ambient. The relatively high TEC-thermistor to module insulation time constant ratio (<1 second to minutes) makes this approach viable. Attempts at improving loop response with more sophisticated compensation schemes encounter difficulty due to laser module thermal term uncertainties. Thermal terms can vary significantly between laser module brands,

Note 1: Academics will be quick to note that this phenomenon also occurs in the sensor's operation. Strictly speaking, the sensor operates at a slightly elevated temperature from its nominally isothermal environment. The assumption is that its dissipation constant remains fixed, which is essentially the case. Because of this, its temperature is stable.

rendering tailored compensation schemes impractical or even deleterious. Note that this restriction still applies, although less severely, even for modules of “identical” manufacture. It is very difficult to maintain tight thermal term tolerances in production.

The simple dominant pole compensation scheme provides good loop response over a wide range of laser module types. It’s the way to go.

Loop Gain

Loop gain is set by both electrical and thermal gain terms. The most unusual aspect of this is different TEC gain in heating and cooling modes. Significantly more gain is available in heating mode, accounting for the higher stabilities noted in the text (Figures 11 and 12). This higher gain means that loop gain bandwidth limits should be

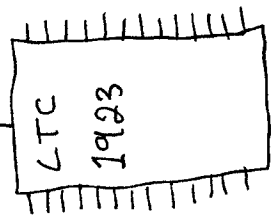
determined in heating mode to avoid unpleasant surprises. Figure 3’s suggested loop gain and compensation values reflect this. It is certainly possible to get cute by changing loop gain bandwidth with mode but performance improvement is probably not worth the ruckus.²

It is important to remember that the TEC is a heat pump, the efficiency of which depends on the temperature across it. Gain varies with efficiency, degrading temperature stability as efficiency decreases. The laser module should be well coupled to some form of heat sink.³ The small amount of power involved does not require large sink capability but adequate thermal flow must be maintained. Usually, coupling the module to the circuit’s copper ground plane is sufficient, assuming the plane is not already thermally biased.

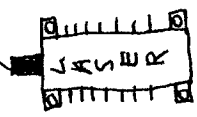
Note 2: The LTC1923’s “heat-cool” status pin beckons alluringly.

Note 3: Yes, this means you should use that messy white goop. A less obnoxious alternative is the thermally conductive gaskets, which are nearly as good.

Hey there,
Check me out.
I'll chill you out,
Stabilize your wavelength
& provide I, V & temperature
limiting. I've got edge slew
rate control for low noise,
switched mode, power delivery.
And, I'm fully synchronizable,
compact & have TEC
state monitoring outputs.
All on a single rail.



That kind of talk
makes me feel
so coherent.



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Current Sources for Fiber Optic Lasers

A Compendium of Pleasant Current Events

Jim Williams, Linear Technology Corporation

INTRODUCTION

A large group of fiber optic lasers are powered by DC current. Laser drive is supplied by a current source with modulation added further along the signal path. The current source, although conceptually simple, constitutes an extraordinarily tricky design problem. There are a number of practical requirements for a fiber optic current source and failure to consider them can cause laser and/or optical component destruction.

Design Criteria for Fiber Optic Laser Current Sources

Figure 1 shows a conceptual laser current source. Inputs include a current output programming port, an output current clamp and an enable command. Laser current is the sole output. This block diagram is deceptively simple. In practice, a laser current source must meet a number of practical requirements, some quite subtle. The key to a successful design is a thorough understanding of individual system requirements. Various approaches suit different sets of freedoms and constraints, although all must address some basic concerns.

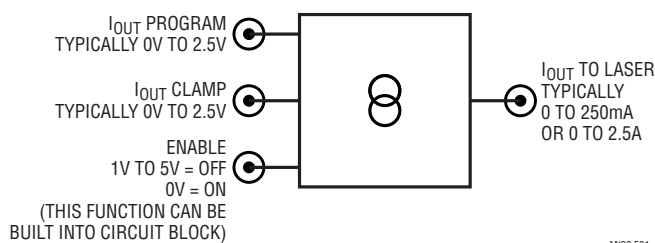


Figure 1. Conceptual Laser Current Source is Deceptively Simple. Practical System Issues and Laser Vulnerability Necessitate Careful Design

There are two basic sets of concerns for laser current sources: performance and protection. Performance issues include the current source's magnitude and stability under all conditions, output connection restrictions, voltage compliance, efficiency, programming interface and power requirements.

Protection features must be included to prevent laser and optical component damage. The laser, an expensive and delicate device, must be protected under all conditions, including supply ramp up and down, improper control input commands, open or intermittent load connections and "hot plugging."

Detailed Discussion of Performance Issues

It is useful to expand on the above cursory discussion to clarify design goals. As such, each previously called out issue is treated in greater detail below.

Required Power Supply

The available power supply should be defined. A single rail 5V supply is presently the most common and desirable. Supply tolerances, typically $\pm 5\%$, must be accounted for. System distribution voltage drops may result in surprisingly low rail voltages at the point of load. Occasionally, split rails are available, although this is relatively rare. Additionally, split rail operation can complicate laser protection, particularly during supply sequencing. See "Laser Protection Features" below for additional comment.

Output Current Capability

Low power lasers operate on less than 250mA. Higher power types can require up to 2.5A.

Output Voltage Compliance

Current source output voltage compliance must be able to accommodate the laser's forward junction drop and any additional drops in the drive path. Typically, voltage compliance of 2.5V is adequate.

Application Note 90

Efficiency

Heat build up in fiber optic systems is often a concern due to space limitations. Accordingly, current source efficiency can be an issue. At low current, linear regulation is often adequate. Switching regulator based approaches may be necessary at higher current.

Laser Connection

In some cases, the laser may float off ground; other applications require grounded anode or cathode operation. Grounding the anode seemingly mandates a negative supply but single rail operation can be retained if switching regulator techniques are employed.

Output Current Programming

Output current is set by a programming port voltage. The voltage may be derived from a potentiometer, DAC or filtered PWM. Typically, a range of 0V to 2.5V corresponds to 0A to 250mA or 0A to 2.5A. Set point accuracy is usually within 0.5%, although better tolerances are readily achievable. Output current stability, discussed below, is considerably tighter.

Stability

The current source should be well regulated against line, load and temperature changes. Line and load induced variations should be held well within 0.05%, with typical temperature drifts of 0.01%. Judicious component choice can considerably improve these figures.

Noise

Current source noise, which can modulate laser output, must be minimized. Typically, noise bandwidth to 100MHz is of interest. A linearly regulated current source has inherently low noise and usually presents no problems. Switching regulator based current sources require special techniques to maintain low noise.

Transient Response

The current source does not need fast transient response but it cannot overshoot the programmed current under any circumstances. Such overshoots can damage the laser or associated optical components.

Detailed Discussion of Laser Protection Issues

Overshoot

As noted above, outputs overshooting the nominal programmed current can be destructive. Any possible combination of improper control input or power supply turn on/off characteristics must be accounted for. Also, any spurious laser current under any condition is impermissible. Note that portions of the current source circuitry may have undesired and unpredictable responses during supply ramp up/down, complicating design.

Enable

An enable line allows shutting the current source output off. The enable line can also be used to hold current output off during supply ramp up, preventing undesired outputs. This can be tricky because the enable signal circuitry may be powered by the same supply that runs the laser. The enable signal must reliably operate independent of power supply turn-on profile. Optionally, the enable function can be self-contained within the current source, eliminating the necessity to generate this signal.

Output Current Clamp

The output current clamp sets maximum output current, overriding the output current programming command. This voltage controlled input can be set by a potentiometer, DAC or filtered PWM.

Open Laser Protection

An unprotected current source's output rises to maximum voltage if the load is disconnected. This circumstance can lead to "hot plugging" the laser, a potentially destructive event. Intermittent laser connections can produce similar undesirable results. The current source output should latch off if the load disconnects. Recycling power clears the latch but only if the load has been established.

The preceding discussion dictates considerable care when designing laser current sources. The delicate, expensive load, combined with the uncertainties noted, should promote an aura of thoughtful caution.¹ The following circuit examples (hopefully) maintain this outlook while simultaneously presenting practical, usable circuits. A variety of approaches are shown, in keeping with the broad area of

Note 1. "For Fools Rush in Where Angels Fear to Tread." An essay on criticism, A. Pope. 1711.

application. The designs can be directly utilized or serve as starting points for specific cases.

Basic Current Source

Figure 2, a basic laser current source, supplies up to 250mA via Q1. This circuit requires both laser terminals to float. The amplifier controls laser current by maintaining the 1Ω shunt voltage at a potential dictated by the programming input. Local compensation at the amplifier stabilizes the loop and the $0.1\mu\text{F}$ capacitor filters input commands, assuring the loop never slew limits. This precaution prevents overshoot due to programming input dynamics. The enable input turns off the current source by simultaneously grounding Q1's base and starving the amplifier's "+" input while biasing the "-" input high. This combination also insures the amplifier smoothly ramps to the desired output current when enable switches low. The enable input must be addressed by an external "watch-dog" which switches after the power supply has been verified to be within operating limits. Because the external circuitry may operate from the same supply as the current source, the enable threshold is set at 1V. The 1V threshold assures the enable input will dominate the current source output at low supply voltages during power turn on. This prevents spurious outputs due to unpredictable amplifier behavior below minimum supply voltage.

High Efficiency Basic Current Source

The preceding circuit uses Q1's linear regulation to close the feedback loop. This approach offers simplicity at the expense of efficiency. Q1's power dissipation can ap-

proach 1W under some conditions. Many applications permit this but some situations require heating minimization. Figure 3 minimizes heating by replacing Q1 with a step-down switching regulator. The switched mode power delivery eliminates almost all of the transistor's heat.

The figure shows similarities to Figure 2's linear approach, except for the LTC1504 switching regulator's addition. It is useful to liken the switching regulator's input (V_{CC}), feedback (FB) and output (V_{SW}) to the transistor's collector, base and emitter. This analogy reveals the two circuits to have very similar operating characteristics, with the switched mode version enhancing efficiency. The LTC1504's output LC filter introduces phase shift, necessitating attention to loop compensation. The amplifier's local rolloff is similar to Figure 2, although phase leading AC feedback elements ($0.01\mu\text{F}$ and $0.033\mu\text{F}$ capacitors) are required for good loop damping. In all other respects, including enable and programming input considerations, this circuit's operation is identical to Figure 2.

Grounded Cathode Current Source

Figure 4 allows the laser's cathode to be grounded, as is sometimes required, by sensing anode current. It utilizes A1, a device with 500mA output capability and programmable output current limit. A1 senses output current across the 1Ω shunt, with limiting controlled by the circuit's current programming input. A1 is set up as a unity-gain follower with respect to the laser, allowing its positive input to serve as a laser voltage clamp input. At laser voltages below the V_{CLAMP} input, A1 appears as a current source, controlled by the current programming

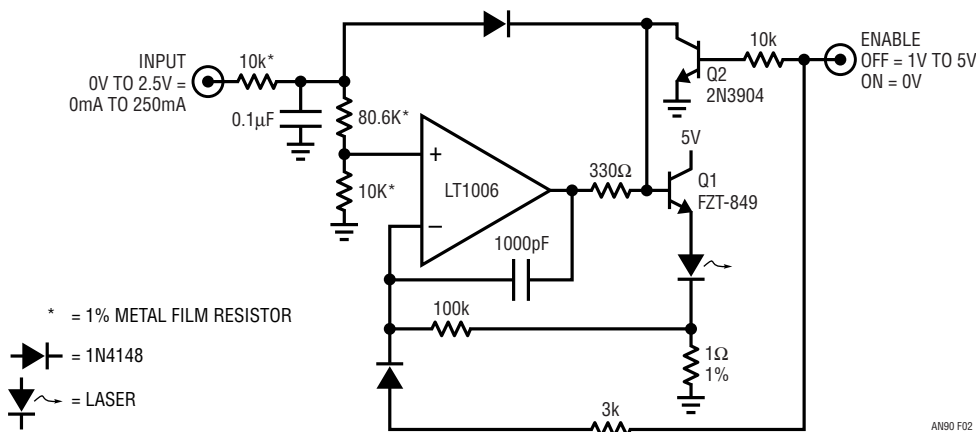


Figure 2. Basic Current Source Requires Off-Ground Operation of Laser Terminals. Amplifier Controls Current by Comparing 0.1Ω Shunt to Input. Biasing Enable Until Supply is Verified Prevents Spurious Outputs

Application Note 90

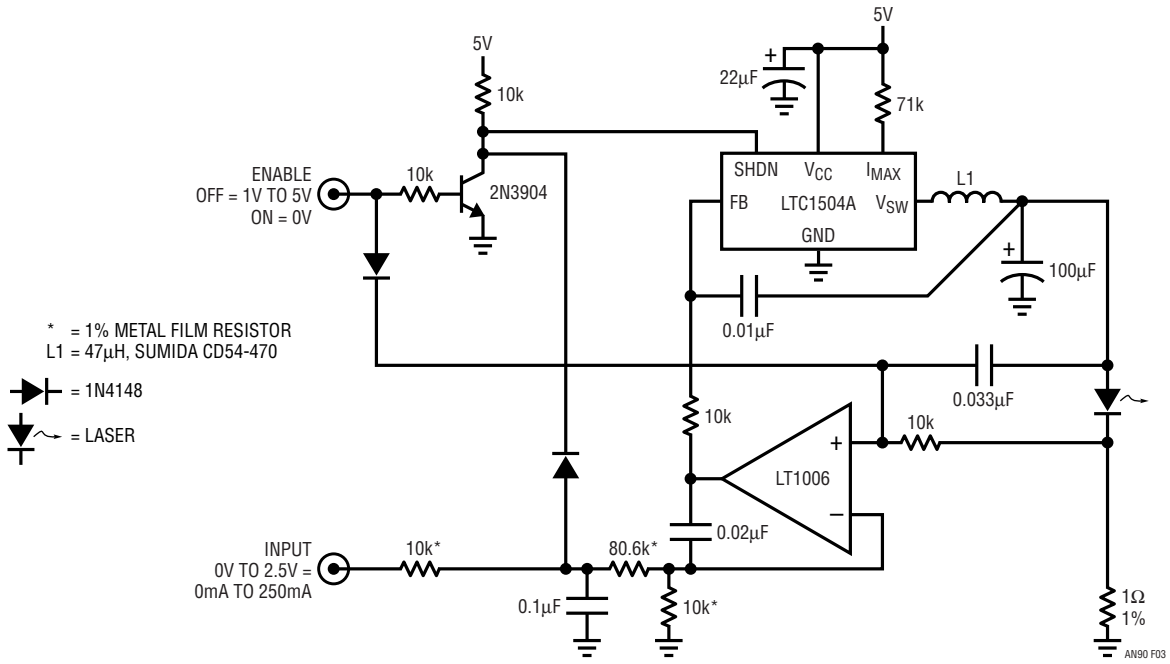


Figure 3. Switching Regulator Replaces Figure 2's Q1, Providing Higher Efficiency. Feedback Control and Enable Input Considerations are as Before

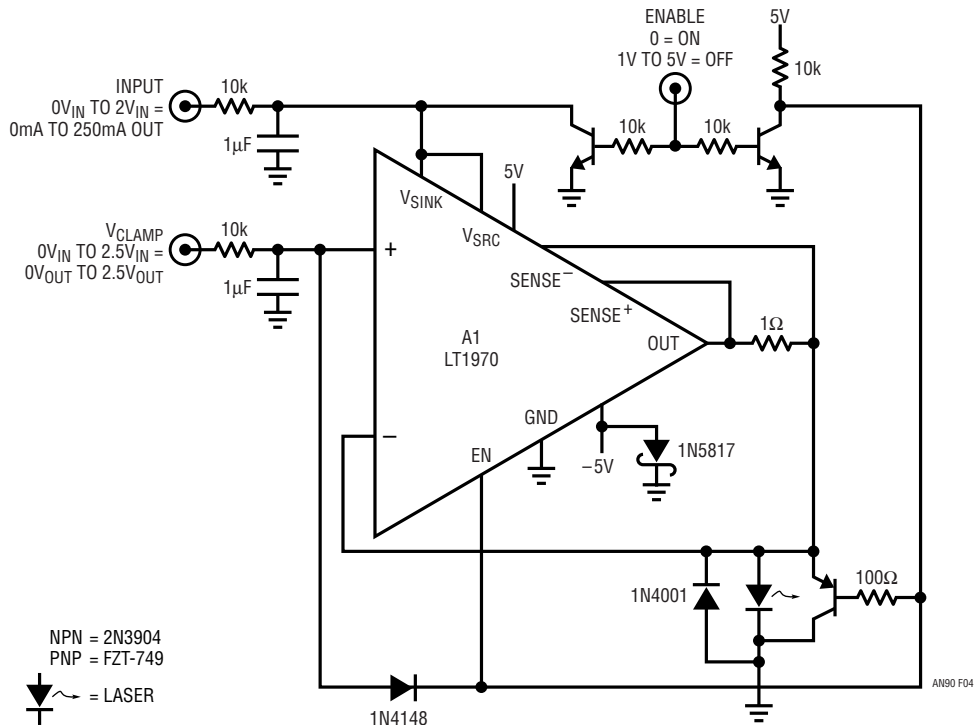


Figure 4. LT1970 Power Amplifier/Current Source Permits Grounding Laser Cathode, Although Requiring Split Rails. Appropriate Modifications would Allow Grounded Anode Operation. Enable Input Must be Biased Until Supplies are Verified

input's setting. At laser voltages equaling or above the V_{CLAMP} input, A1 is a voltage source, controlled by V_{CLAMP} 's value. This permits the V_{CLAMP} input to limit maximum voltage across the laser terminals.

The enable function operates similarly to previous descriptions and the $1\mu\text{F}$ capacitors restrict output movement to safe, well damped speeds. The diode shunting the laser prevents reverse bias during power supply sequencing. The 1N5817 protects against uncontrolled positive outputs if the negative supply drops out or sequences too slowly. This circuit's simplicity and laser connection versatility (appropriate modifications permit grounded anode operation) are attractive but A1's negative supply requirement may be detrimental. The negative supply complicates the external "watchdog" circuitry required for the enable input. In the worst case, it simply may not be available in the host system.

Single Supply, Grounded Cathode Current Source

Figure 5 preserves Figure 4's grounded cathode operation while operating from a single supply. This circuit is reminiscent of Figure 2, with a notable exception. Here, differential amplifier A2 senses across a shunt in the laser anode, permitting cathode grounding. A2's gain-scaled output feeds back to A1 for loop closure. Loop compensation and enable input considerations are related to previous examples and, as before, Q1 could be replaced with a switching regulator.

Fully Protected, Self-Enabled, Grounded Cathode Current Source

All of Figure 5's elements are repeated in Figure 6; no additional comment on them is necessary. However, three new features appear, allowing this circuit to operate in a fully protected and self-contained fashion. The circuit monitors its power supply and "self-enables" when the supply is within limits, eliminating the "enable" port and the external "watchdog" previously required. A settable current clamp and open laser protection prevent laser damage.

The self-enable is designed around an LT1431 shunt regulator. It has the highly desirable property of maintaining a predictable open collector output when operating below its minimum supply voltage. At initial turn on, supply voltage is very low (e.g., 1V), the LT1431's output does not switch and current flows to Q3's base. Q3 turns on, preventing Q1's base from receiving bias. Additionally, the circuit's current programming input is pulled down and A1's "-" input is driven. This arrangement ensures that the laser cannot receive current until Q3 turns off. Also, when Q3 does go off, A1's output will cleanly ramp up to the desired programmed current. The resistor values at the LT1431's "REF" input dictate the device will go low when V_{SUPPLY} passes through 4V. This potential ensures proper circuit operation. Supply start-up waveforms appear in Figure 7. Trace A, the nominal 5V rail, ramps for 3ms before arriving at 5V. During this interval, the LT1431

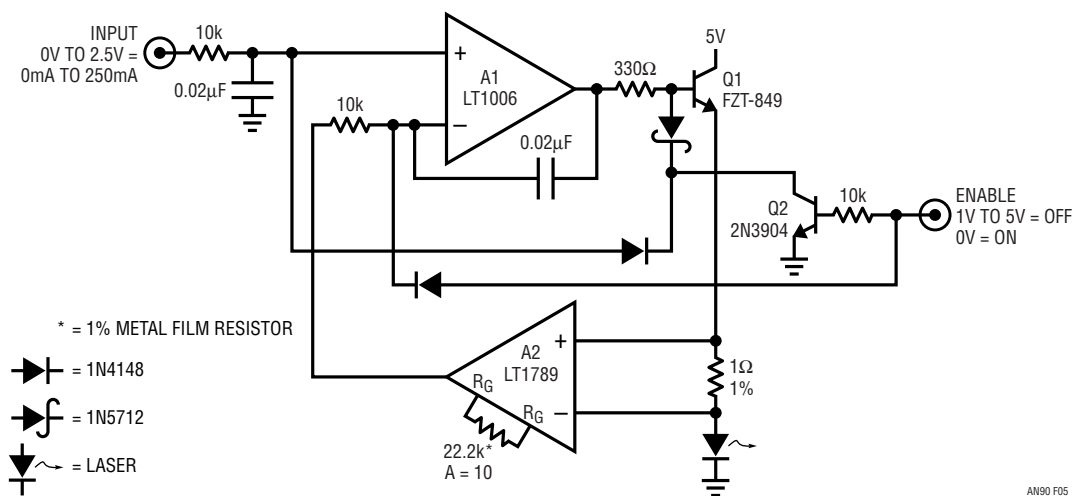


Figure 5. Differentially Sensed Shunt Voltage Allows Grounded Cathode Laser Drive with Single Supply. Loop and Enable Input Considerations Derive from Previous Figures

Application Note 90

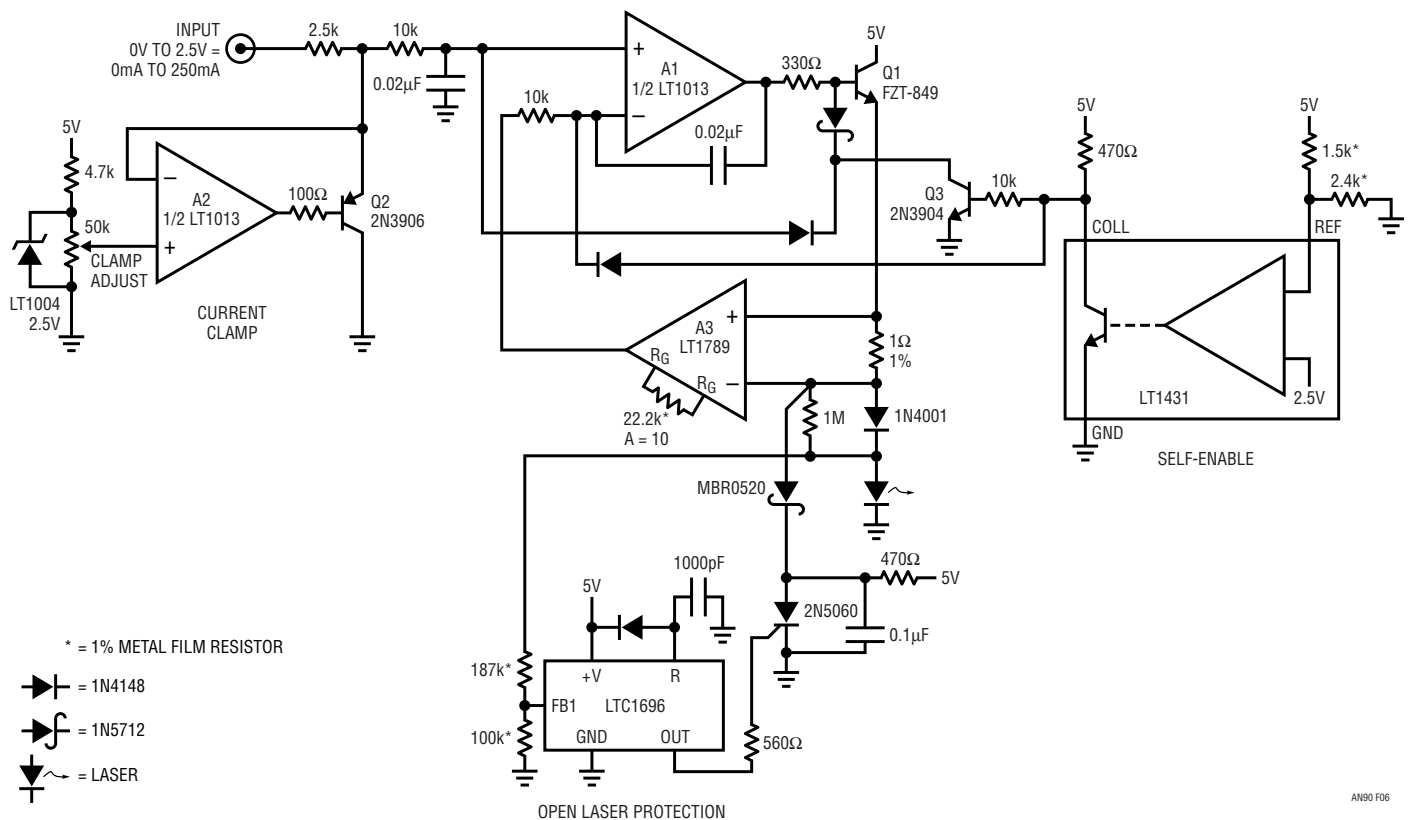


Figure 6. Figure 5's Circuit, Augmented with "Self-Enable," Monitors Power Supply, Operates when $V_{SUPPLY} = 4V$. Current and Open Laser Clamps Protect Laser

(trace B) follows the ramp, biasing Q3 on. A1's output (trace C) is uncontrolled during this period, Q1's emitter (trace D), however, is cut off due to Q3's conduction and cannot pass the disturbance. As a result, the laser conducts no current (trace E) during this time. When the supply (trace A) ramps beyond 4V (just before the photo's 4th vertical division), the LT1431 switches low (trace B), Q3 switches off and the circuit "self-enables." A1's output (trace C) ramps up, with Q1's emitter (trace D) and laser current (trace E) slaved to its movement. This action prevents any undesired current in the laser during supply turn on, regardless of unpredictable circuit behavior at low supply voltages.

Supply turn on is not the only time laser current must be controlled. Response to programming input changes must be similarly well behaved. Figure 8 shows laser current response (trace B) to a programming input step (trace A). Damping is clean, with no hint of overshoot.

The circuit also includes open laser protection. If the current source operates into an open load (no laser), it will

produce maximum voltage at the laser output terminals. This circumstance can lead to "hot plugging" the laser, a potentially destructive event. Intermittent laser connections can produce similar undesirable results. The LTC1696 overvoltage protection controller guards against open laser operation. This device's output latches high when its feedback input (FB) exceeds 0.88V. Here, the FB pin is biased so that laser output voltage exceeding 2.5V forces the LTC1696 high, triggering the SCR to shunt current away from the laser. The 470Ω resistor supplies SCR holding current and the diodes insure no current flows in the output.

Figure 9 details events with a properly connected laser at supply turn on. Trace A is the supply, trace B the laser voltage, trace C the LTC1696 output and trace D the laser current. The waveforms show laser voltage (trace B) rising to about 2V at supply turn on (trace A). Under these normal conditions, the LTC1696 output (trace C) stays low and laser current (trace D) rises to the programmed value.

Figure 10 shows what happens when the circuit is turned on into an open laser connection. Trace assignments are identical to the previous photo. At supply turn on (trace A), the laser voltage (trace B) transitions beyond the 2.5V open laser threshold. The LTC1696 output (trace C) goes high, the SCR latches and no current flows in the shunted laser line (trace D). Once this occurs, power must be recycled to reset the LTC1696-SCR latch. If the laser has not been properly connected, the circuit will repeat its protective action. Open laser protection is not restricted to turn on. It will also act if laser connection is lost at any time during normal circuit operation.

A final protection feature in Figure 6 is a current clamp. It prevents uncontrolled programming inputs from being transmitted by clamping them to a settable level. A2, Q2 and associated components form the clamp. Normally, A2's "+" input is above the circuit's programming input (Q2's emitter voltage), A2's output is high and Q2 is off. If the programming input exceeds A2's "+" input level, A2 swings low, Q2 comes on and the amplifier feedback controls Q2's emitter to the "clamp adjust" wiper potential. This clamps A1's input to the "clamp adjust" setting, preventing laser current overdrive. Clamp action need not

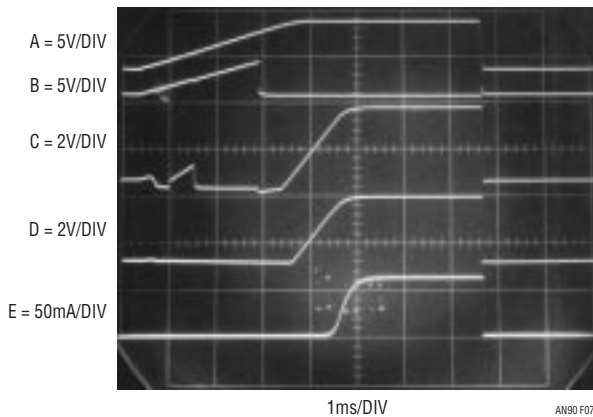


Figure 7. Figure 6's Waveforms During Power Supply Application (Trace A). Traces B and C are LT1431 and A1 Outputs, Respectively. Q1's Emitter (Trace D) Provides Power Gain. Feedback Sets Laser Current (Trace E). Self-Enable Circuit Prevents Spurious A1 Outputs (Trace C) During Supply Ramp Up from Corrupting Laser Current (Trace E)

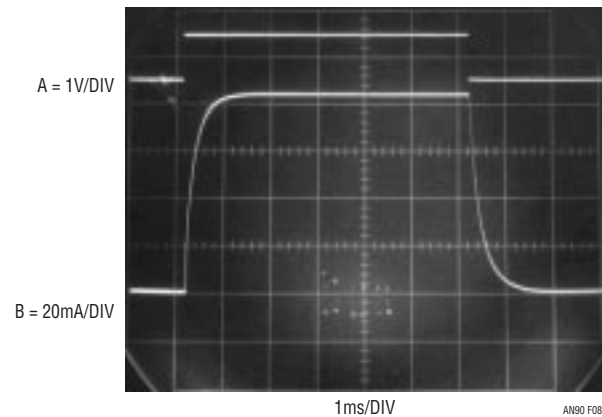


Figure 8. Figure 6's Output (Trace B) Responding to Trace A's Input Step. Trace B's Laser Current Has Controlled Damping, No Overshoot

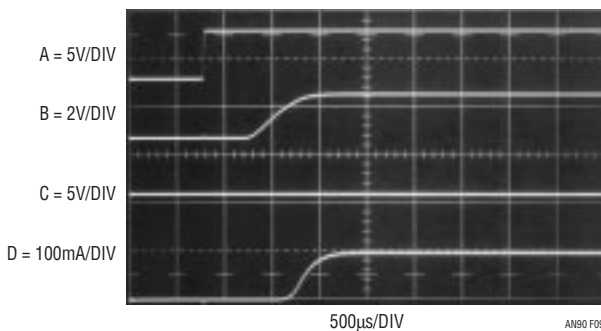


Figure 9. Figure 6's Open Laser Protection Does Not Act During Normal Turn On. Trace A is Supply, Trace B Laser Voltage, Trace C LTC1696 Output and Trace D Laser Current. LTC1696 Overvoltage Threshold is Not Exceeded, SCR is Unbiased (Trace C) and Laser Conducts Current (Trace D)

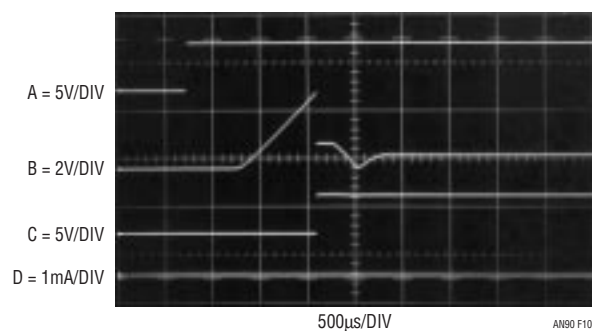


Figure 10. Open Laser Protection Circuit Responding to Open Laser Turn On. Trace Assignments Identical to Previous Figure. Laser Line (Trace B) Excursion Beyond Overvoltage Threshold Causes LTC1696 Output (Trace C), Biasing SCR to Clamp Open Laser Line. No Current Flows in Laser Line, Trace D (Note 100x Increase in Measurement Sensitivity vs Figure 9)

Application Note 90

be particularly fast to be effective, because of A1's 10k-0.02 μ F input filter. Figure 11's traces show clamp response to programming input overdrive. When the programming input (trace A) exceeds the clamp's preset level, Q2's emitter (trace B) does the same, causing A2's output (trace C) to swing down. A2 feedback controls Q2's emitter to the clamp level, arresting the voltage applied to the 10k-0.02 μ F filter. The filter band limits the abrupt clamp operation, resulting in a smooth corner at A1's positive input (trace D). A1's clamped input dictates a similarly shaped and clamped laser current (trace E). The clamp remains active until the programming input falls below the "clamp adjust" setting.

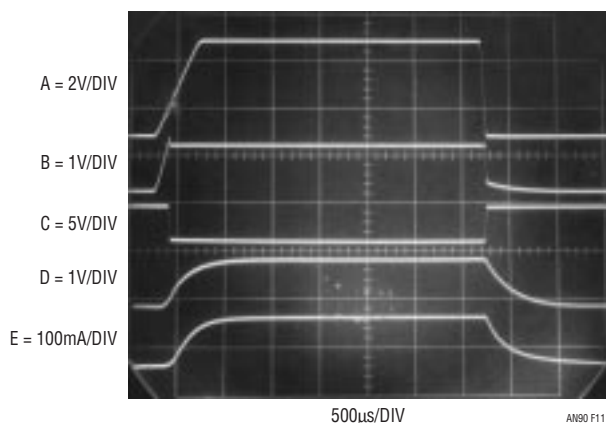


Figure 11. Figure 6's Current Clamp Reacting to Programming Input Overdrive. Waveforms Include Programming Input (Trace A), Q2 Emitter (Trace B), A2 Output (Trace C), A1 + Input (Trace D) and Laser Current (Trace E). When Programming Input Exceeds Clamp Threshold, A2 Swings Abruptly (Trace C), Causing Q2's Emitter (Trace B) to Clamp. A1's +Input (Trace D) Remains at Clamp Level, Maintaining Safe Laser Current (Trace E)

2.5A, Grounded Cathode Current Source

Figure 12, derived from Figures 3 and 6, provides up to 2.5A to a grounded cathode laser. A1 is the control amplifier, output current is efficiently delivered by the LT1506 switching regulator and A2 senses laser current via a 0.1 Ω shunt. Loop operation is similar to the descriptions given for Figures 3 and 6 with DC feedback to A1 coming from A2. Frequency compensation differs from the previous figures. Stable loop operation is achieved by local roll off at A1, augmented by two lead networks associated with L1. Midband lead is provided by feeding back a lightly filtered (1k-0.47 μ F) version of LT1506 V_{sw} output activity. High frequency lead, arriving via the 330 Ω -0.05 μ F pair, optimizes edge response. Figure 13's wave-

forms detail dynamic response. Trace A's input step arrives in filtered form at A1's positive input (trace B). The loop produces trace C's faithfully profiled laser current output.

As shown, the circuit has the externally controlled enable function, although Figure 6's "self-enable" feature may be used. Similarly, Figure 6's current clamp and open laser protection may be employed in this circuit.

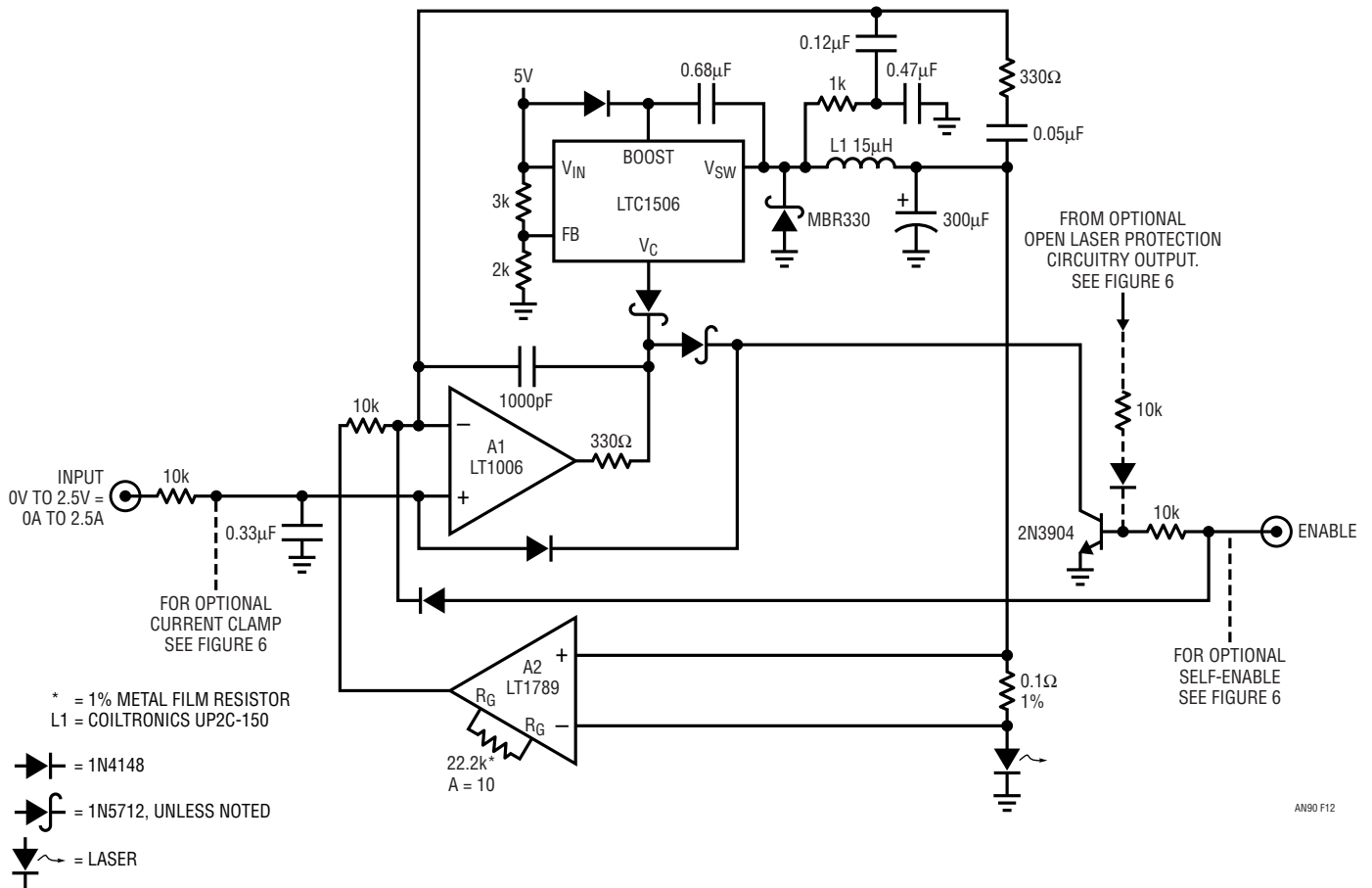
This circuit's switched mode energy delivery provides high efficiency at high power but output noise may be an issue. Residual harmonic content related to switching regulator operation appears in the laser current. The resultant low level modulation of laser output may be troublesome in some applications. Figure 14 shows about 800 μ A_{P-P} switching regulator related noise in the 2A laser current output.² This disturbance is composed of fundamental ripple and switching transition related harmonic. This 0.05% noise is below most optical system requirements, although the following circuit achieves substantially lower noise figures.

0.001% Noise, 2A, Grounded Cathode Current Source

The previous circuit's 0.05% noise content suits many optical system applications. More stringent requirements will benefit from Figure 15's extremely low noise content. This grounded cathode, 2A circuit has only 20 μ A_{P-P} noise, about 0.001%. Special switching regulator techniques are used to attain this performance. Substantial noise reduction is achieved by limiting edge switching speed in the regulator's power stage.³ Voltage and current rise times in switches Q1 and Q2 are controlled by the LT1683 pulse width modulator. The LT1683's output stage operates Q1 and Q2 in local loops which sense and control their edge times. Transistor voltage information is fed back via the 4.7pF capacitors; current status is derived from the 0.033 Ω shunt and also fed back. This arrangement permits the PWM control chip to fix transistor switching times, regardless of power supply or load changes. The transition rates are set by resistors (R_{VSL} and R_{CSL}) associated with

Note 2: Noise contains no regularly occurring or coherent components. As such, switching regulator output "noise" is a misnomer. Unfortunately, undesired switching related components in the regulated output are almost always referred to as "noise." Accordingly, although technically incorrect, this publication treats all undesired output signals as "noise." See Reference 7.

Note 3: See Reference 7 for details on this technique.



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Figure 12. Switched Mode Version of Figure 6 Has 2.5A Output. Feedback Loop Compensation Accommodates Switching Regulator Delay. Clamp, Protection and Self-Enable Circuits are Optional

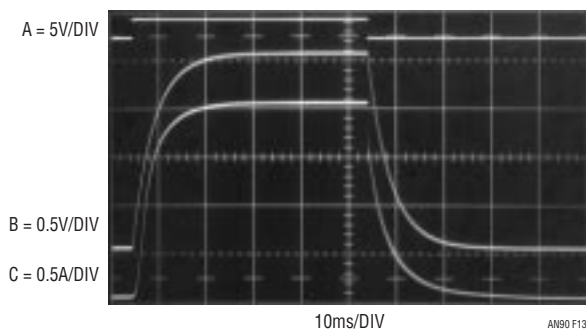


Figure 13. 2.5A Current Source Waveforms for an Input Step (Trace A). A1's Input Filter (Trace B) Smooths Step, Resulting in Trace C's Similarly Shaped Laser Current

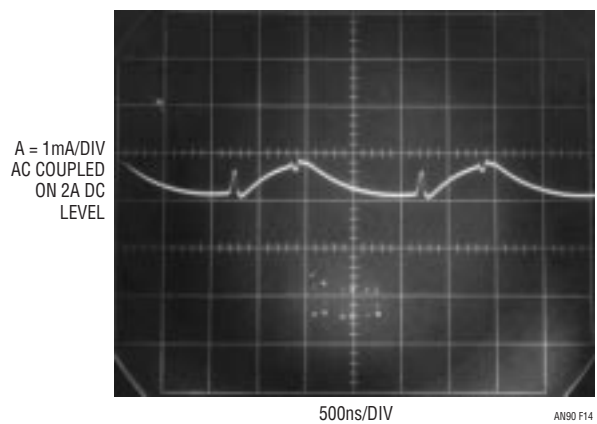


Figure 14. High Power Current Source Noise Includes Switching Regulator Fundamental Ripple and Harmonic Content. 800µAp-p Noise is About 0.05% of 2A DC Output

Application Note 90

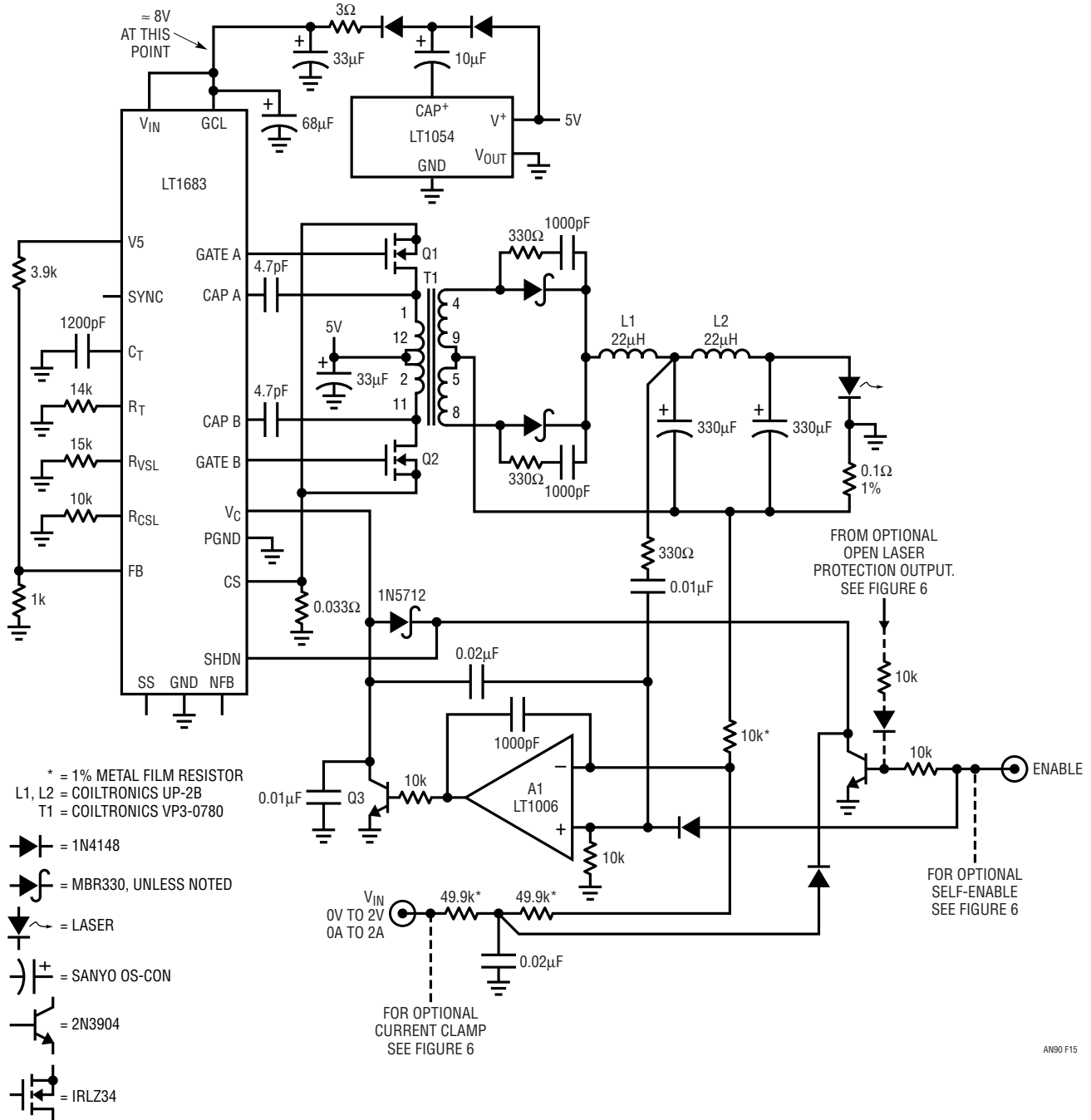


Figure 15. 0.001% Noise, 2A Laser Current Source Has Grounded Cathode Output. Clamp, Protection and Self-Enable Circuits May be Added

AN90 F15

the LT1683 controller. In practice, these resistor values are set by adjusting them to minimize output noise. The remainder of the circuit forms a grounded cathode laser current source.

Q1 and Q2 drive T1, whose rectified output is filtered by LC sections. Because T1's secondary floats, the laser cathode and the 0.1Ω shunt may be declared at circuit ground. The shunt is returned to T1's secondary center tap, completing a laser current flow path. This arrangement produces a negative voltage corresponding to laser current at the shunt's ungrounded end. This potential is resistively summed at A1 with the positive voltage current programming input information. A1's output feedback controls the LT1683's pulse width drives to Q1 and Q2 via Q3, closing a loop to set laser current. Loop compensation is set by band limiting at A1 and Q3's collector, aided by a single lead network arriving from the L1-L2 junction.

Some circuit details merit attention. The LT1683's supply input pins are fed from an LT1054 based voltage multiplier. This boosted voltage provides enough gate drive to ensure Q1-Q2 saturation. Damper networks across T1's rectifiers minimize diode switching related events in the output current. Finally, this circuit is compatible with the "self-enable" and laser protection features previously described. Appropriate connection points appear in the figure.

The speed controlled switching times result in a spectacular decrease in noise. Figure 16 shows just 20μA_{p-p} noise, about 0.001% of the 2A DC laser current. Fundamental

ripple residue and switching artifacts are visible against the measurement noise floor.⁴

0.0025% Noise, 250mA, Grounded Anode Current Source

This circuit, similar to the previous one, uses edge time control to achieve an exceptionally low noise output. It is intended for lower power lasers requiring grounded anode operation. The LT1533, a version of the previous circuit's LT1683, has internal power switches. These switches drive T1. T1's rectified and filtered secondary produces a negative output, biasing the laser. The laser's anode is grounded and its current path to T1's secondary completed via the 1Ω shunt. This configuration makes T1's center tap voltage positive and proportional to laser current. This voltage is compared by A1 to the current programming input. A1 biases Q2, closing a loop around the LT1533. Loop compensation is provided by local bandwidth limiting at A1 and Q2's collector damping and feedback capacitors.

This circuit's 2.5μA_{p-p} noise qualifies it for the most demanding applications. Figure 18 shows residual switching related noise approaching the measurement noise floor.

The enable function operates as previously described. Additionally, this circuit is compatible with Figure 6's "self-enable" and laser protection accessory circuits. Changes necessitated by the grounded anode operation appear on the schematic.

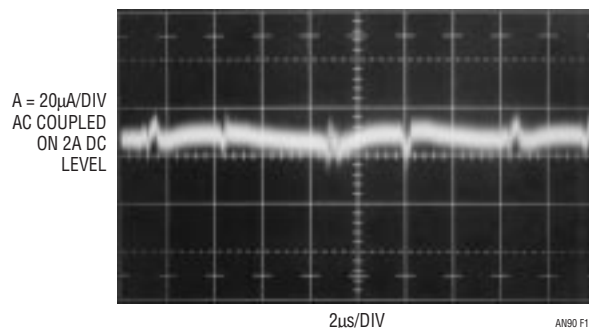


Figure 16. Figure 15's Output Noise Measures ≈20μA_{p-p}, About 0.001%. Coherent, Identifiable Components Include Fundamental Ripple Residue and Switching Artifacts

Note 4: Reliable wideband current noise measurement at these levels requires special techniques. See Appendix B, "Verifying Switching Regulator Related Noise" and Appendix C, "Notes on Current Probes and Noise Measurement," for details.

Application Note 90

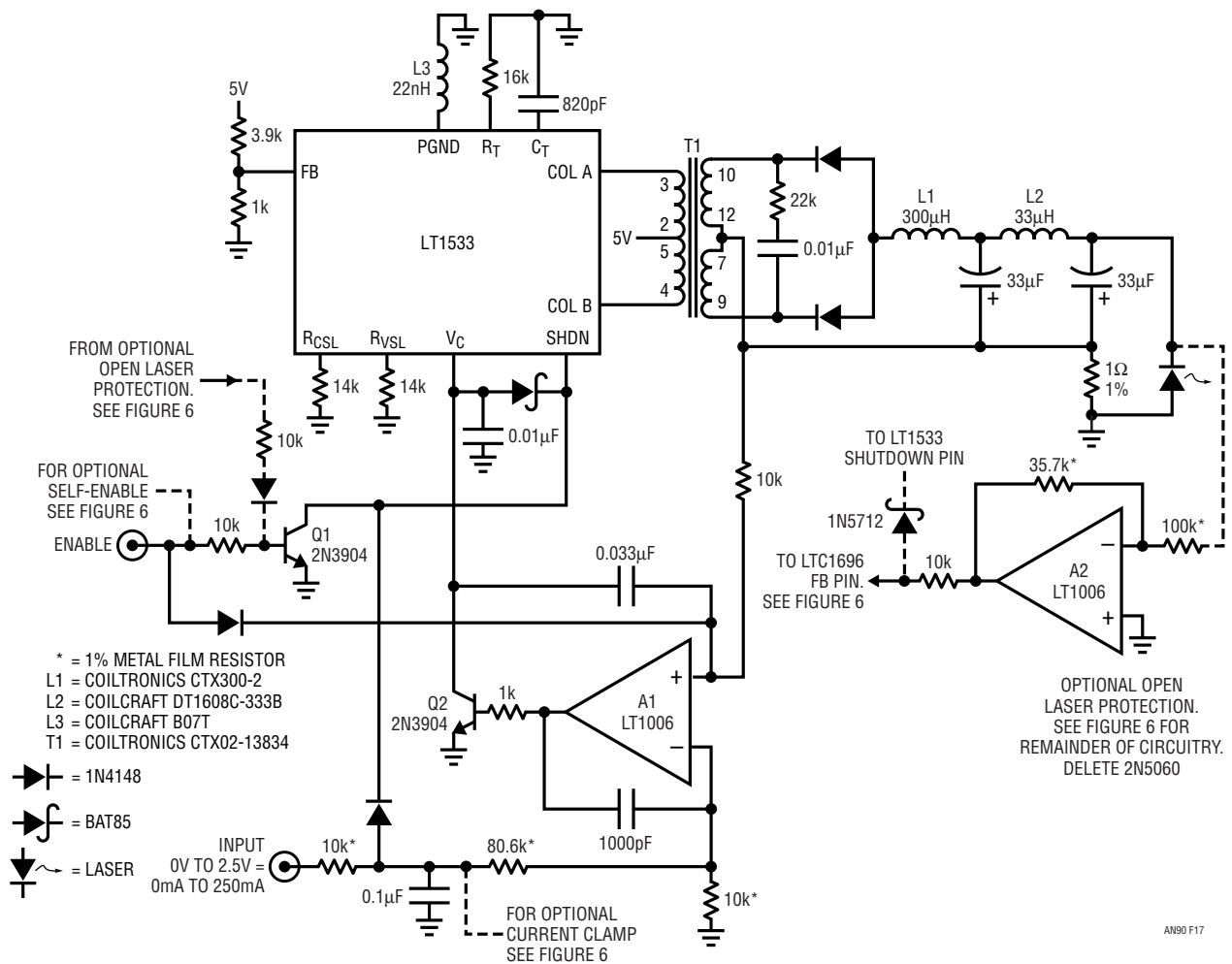


Figure 17. 0.0025% Noise, Grounded Anode Laser Current Source is 250mA Version of Figure 15

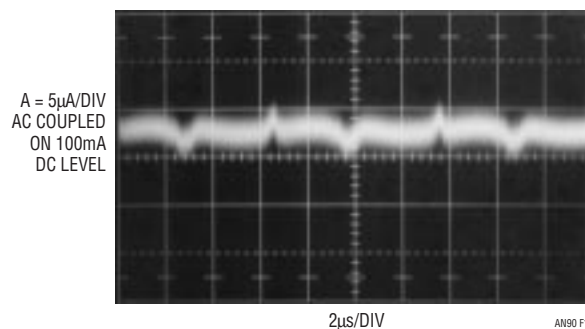


Figure 18. Figure 17's 2.5µA_{p-p} Switching Related Noise is Detectable in Measurement Noise Floor

Low Noise, Fully Floating Output Current Source

Figure 19 retains the preceding example's low noise but also has a fully floating output. Either laser terminal may be grounded without effecting circuit operation. This feature is realized by feedback controlling transformer primary current and relying on interwinding coupling to maintain regulation.⁵ This coupling varies slightly with operating point, limiting output current regulation to about 1%.

The schematic shows the LT1533 low noise switching regulator driving T1. The LT1533, while retaining its controlled edge time characteristics, is forced to run at 50% duty cycle by grounding its "duty" pin. Current flows through Q1 and the 0.1Ω shunt into T1's primary. The LT1533 open collector power outputs alternately chop primary current to ground. Primary current magnitude, and hence the 0.1Ω shunt voltage, is set by Q1's bias. Q1's bias, in turn, is set by A1's output, which represents the

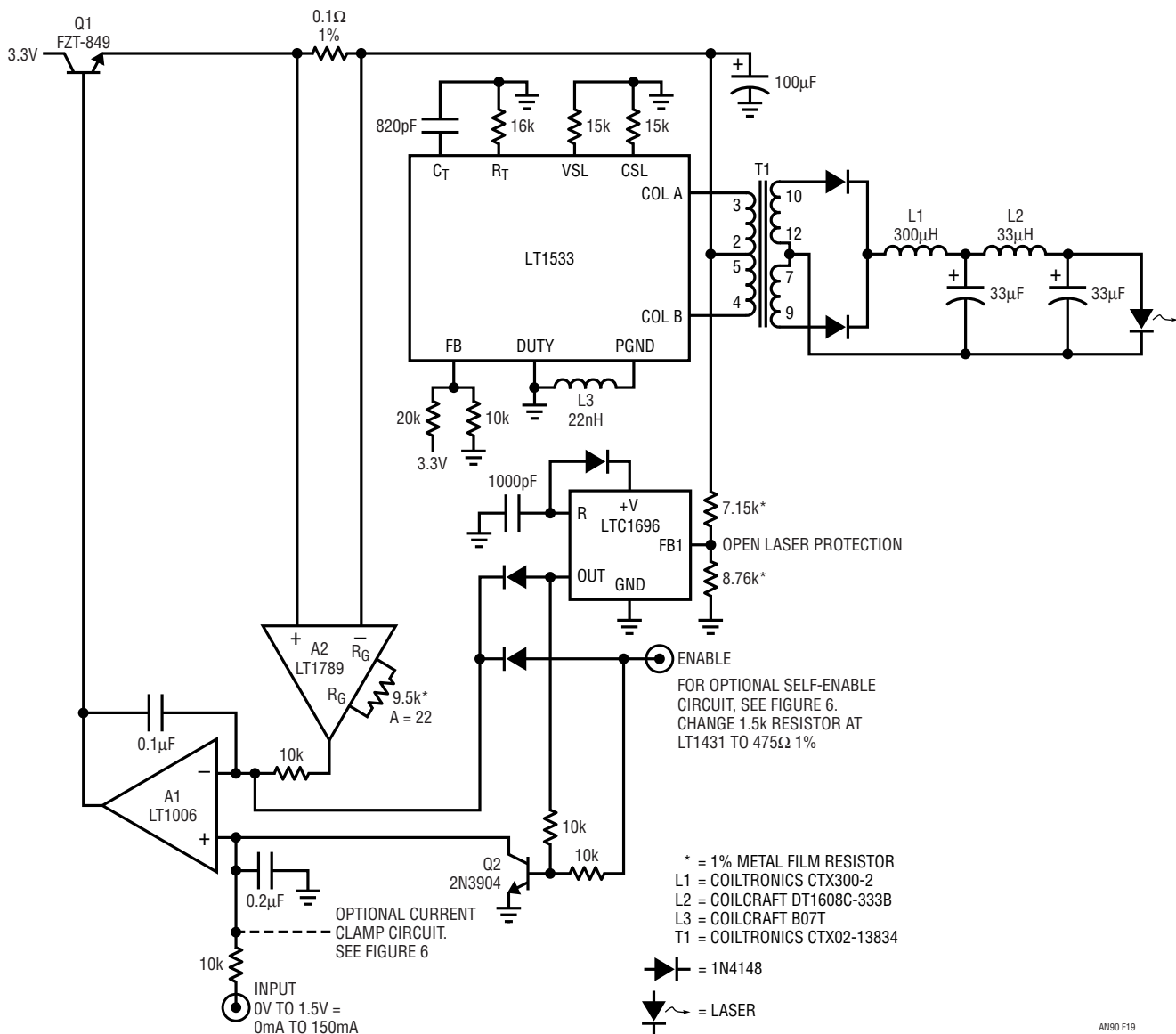


Figure 19. Switched Mode, Low Noise Current Source Has Floating Output, Permitting Grounding Laser Anode or Cathode. Open Laser Protection is Included; Circuit is Compatible with Current Clamp and Self-Enable Options

Note 5: We have engaged this stunt before to serve a variety of purposes. See References 2, 3 and 4.

Application Note 90

difference between the output current programming input and A2's amplified version of the shunt voltage. This loop enforces a shunt voltage proportionate to current programming input value. In this way, the current programming input sets T1 primary current, determining T2 secondary current through the laser. Current programming input scaling is calibrated by differential amplifier A2's gain setting resistor.

The primary side feedback's lack of global feedback mandates current regulation compromise. Figure 20's plot of laser current vs programming input voltage shows 1% conformance over nearly the entire range. The error below 10mA, due to nonideal transformer behavior, is normally insignificant because it is below typical laser threshold current. Line regulation, also degraded by the sensing scheme, still maintains about 0.05%/V. Similarly, load regulation, over a 1V to 1.8V compliance voltage, is typically 2%.

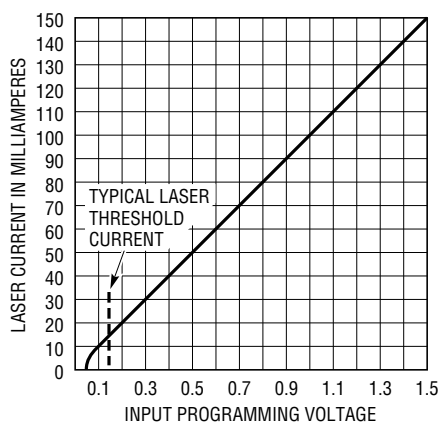
This circuit's floating output complicates inclusion of the laser protection and "self-enable" features described in Figure 6's text but they are accommodated. Open laser protection, shown in Figure 20, is accomplished by biasing the LTC1696 from T1's center tap. If the laser opens, the loop forces a marked rise at T1's center tap, latching the LTC1696's output high. This skews A1's inputs, sending its output low and shutting off Q1. All T1 drive ceases.

Because the LTC1696 output latches, power must be recycled to reset the circuit. If the laser has not been connected, the latch will act again, protecting the laser from "hot plugging" or intermittent connections. The "self-enable" and current clamp options may be added in accordance with the notations on the schematic.

Anode-at-Supply Current Source

Figure 21's current source is useful where the laser anode is committed to the power supply. A1, sensing Q1's emitter, closes a loop which forces constant current in the laser. Local compensation at A1 and input band limiting stabilize the loop.

This circuit also includes an inherent "self-enable" feature. The LT1635 operates at supply voltages down to 1.2V. Above 1.2V the LT1635's comparator configured section (C1) holds off circuit output until supply voltage reaches 2V. Below 1.2V supply, Q1's base biasing prevents unwanted outputs. Figure 22 details operation during supply turn on. At supply ramp up (trace A), output current (trace D) is disabled. When the supply reaches 2V, C1 (trace B) goes low, permitting A1's output (trace C) to rise. This biases Q1 and laser current flows (trace D). The LT1635 operates on supply voltages as low as 1.2V. Below this level, spurious outputs are prevented by junction stacking and band limiting at Q1's base. Q1's base compo-



AN90 F20

Figure 20. Laser Current vs Input Programming Voltage for Floating Current Source. Conformance is within 1% over Nearly Entire Range. Error Below 10mA, Due to Nonideal Transformer Behavior, is Below Typical Laser Threshold Current

nents also prevent unwanted outputs when the supply rises rapidly. Such rapid rise could cause uncontrolled A1 outputs before the amplifier and its feedback loop are established. Figure 23 shows circuit events during a rapid supply rise. Trace A shows the supply's quick ascent.

Trace B, C1's output, responds briefly but goes low some time after the supply moves past 2V. A1 (trace C) produces an uncontrolled output for about 100µs. The RC combination in Q1's base line filters this response to insignificant levels and no laser current (trace D) flows.

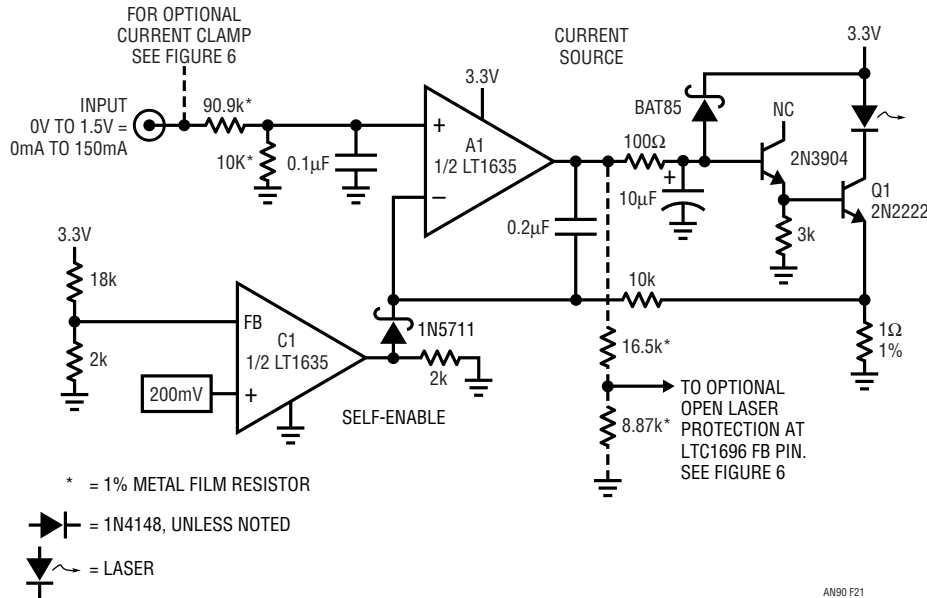


Figure 21. Circuit Has Laser Anode Committed to Supply, Inherent Self-Enabled Operation. LT1635 Functions at 1.2V, Although Self-Enable Feature Holds Off Output Until Power Supply Exceeds 2V. Current Clamp and Open Laser Protection are Optional

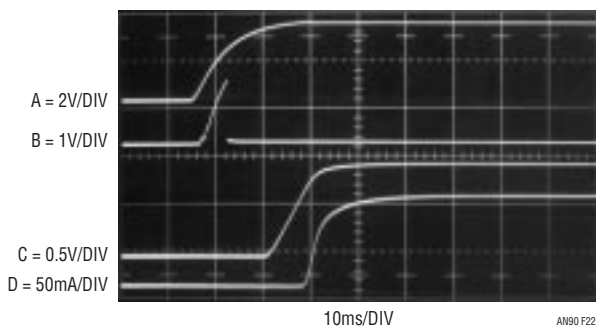


Figure 22. Output Current (Trace D) is Held Off Until Supply (Trace A) Ramps Past 2V. Self-Enable Comparator (Trace B) Operates Above 1.2V; Q1 Base (Trace C) Biasing Prevents Output Below 1.2V

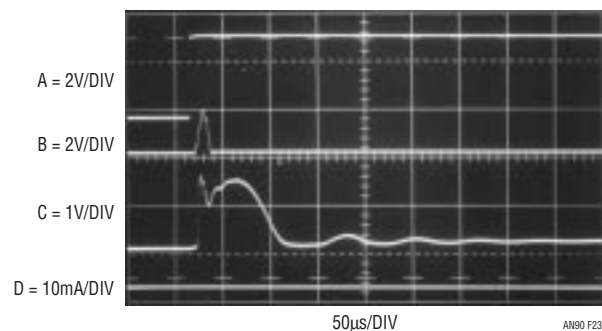


Figure 23. Rapidly Rising Supply (Trace A) Produces No Current Output (Trace D) Despite A1's Transient Uncontrolled Output (Trace C). C1 (Trace B) Reacts Properly but A1's Inactive Loop Cannot Respond. Q1's Base Line Components Preclude Spurious Current Output (Trace D)

Application Note 90

The slew retarded input and loop compensation yield clean dynamic response with no overshoot. Figure 24, trace A, is an input step. This step, filtered at A1's input (trace B), is represented as a well controlled laser current output in trace C.

Current clamping and open laser protection options are annotated in the schematic. Additionally, higher output current is possible at increased supply voltages, although Q1's dissipation limits must be respected.

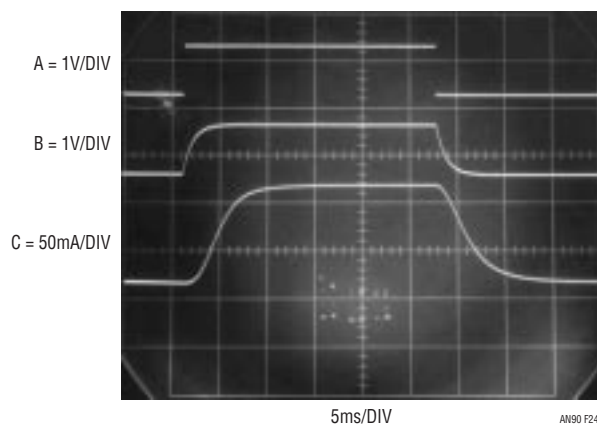


Figure 24. Output Current (Trace C) Responds Cleanly to Filtered Version (Trace B) of Trace A's Input Step

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

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APPENDIX A

SIMULATING THE LASER LOAD

Fiber optic lasers are a delicate, unforgiving and expensive load. This is a poisonous brew when breadboarding with high likelihood of catastrophe. A much wiser alternative is to simulate the laser load using either diodes or electronic equivalents. Lasers look like junctions with typical forward voltages ranging from 1.2V to 2.5V. The simplest way to simulate a laser is to stack appropriate numbers of diodes in series. Figure A1 lists typical junction voltages at various currents for two popular diode types. The MR750 is suitable for currents in the ampere range, while the 1N4148 serves well at lower currents. Typically, stacking two to three diodes allows simulating the laser in a given current range. Diode voltage tolerances and variations due to temperature and current changes limit accuracy, although results are generally satisfactory.

Electronic Laser Load Simulator

Figure A2 is a laser load simulator powered by a 9V battery. It eliminates diode load junction voltage drop uncertainty. Additionally, any desired “junction drop” voltage may be conveniently set with the indicated potentiometer. Electronic feedback enforces establishment and maintenance of calibrated junction drop equivalents.

The potentiometer sets a voltage at A1’s negative input. A1 responds by biasing Q1. Q1’s drain voltage controls Q2’s base and, hence, Q2’s emitter potential. Q2’s emitter is fed back to A1, closing a loop around the amplifier. This forces the voltage across Q2 to equal the potentiometer’s output voltage under all conditions. The capacitors at A1 and Q1 stabilize the loop and Q2’s base resistor and ferrite bead suppress parasitic oscillation. The 1N5400 prevents Q1-Q2 reverse biasing if the load terminals are reversed.

MR750 (25°C)	
TYPICAL JUNCTION CURRENT	TYPICAL JUNCTION VOLTAGE
0.5A	0.68V
1.0A	0.76V
1.5A	0.84V
2.0A	0.90V
2.5A	0.95V

1N4148 (25°C)	
TYPICAL JUNCTION CURRENT	TYPICAL JUNCTION VOLTAGE
0.1A	0.83V
0.2A	0.96V
0.3A	1.08V

Figure A1. Characteristics of Diodes Suitable for Simulating Lasers. Appropriate Series Connections Approximate Laser Forward Voltage

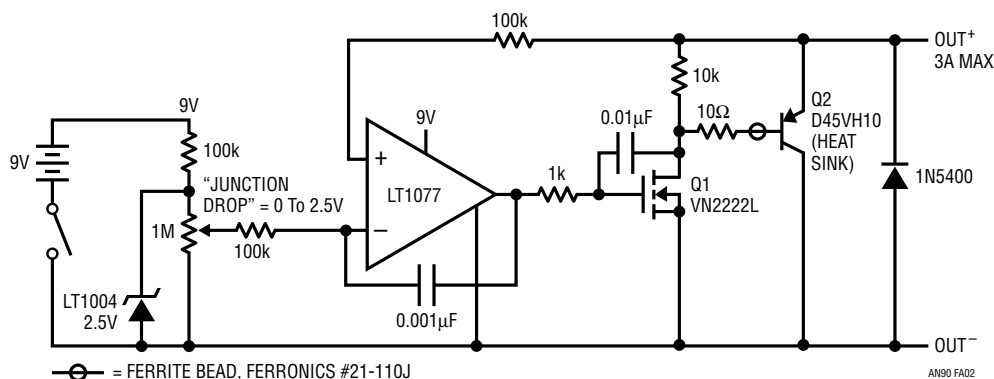


Figure A2. Floating, Battery-Powered Laser Simulator Sets Desired “Junction Drop” Across Output Terminals. Amplifier Feedback Controls Q2’s V_{CE} to Potentiometer Voltage

Application Note 90

APPENDIX B

VERIFYING SWITCHING REGULATOR RELATED NOISE

Measuring the switching regulator related current noise levels discussed in the text requires care. The microamp amplitudes and wide bandwidth of interest (100MHz) mandates strict attention to measurement technique. In theory, simply measuring voltage drop across a shunt resistor permits current to be determined. In practice, the resultant small voltages and required high frequency fidelity pose problems. Coaxial probing techniques are applicable but probe grounding requirements become severe. The slightest incidence of multiple ground paths (“ground loops”) will corrupt the measurement, rendering observed “results” meaningless. Differentially configured coaxial probes offer some relief from ground loop based difficulties but there is an inherently better approach.¹

Current transformers offer an attractive way to measure noise while eliminating probe grounding concerns. Two types of current probes are available: split core and closed core. The split core “clip on” types are convenient to use but have relatively low gain and a higher noise floor than closed core types.² The closed core transformer’s gain and noise floor advantages are particularly attractive for wideband, low current measurement.

Figure B1’s test setup allows investigation of the closed core transformer’s capabilities. The transformer specified has flat gain over a wide bandwidth, a well shielded enclosure and a coaxial 50Ω output connection. Its 5mV/mA output feeds a low noise x100, 50Ω input amplifier. The amplifier’s terminated output is monitored by an oscilloscope with a high sensitivity plug-in. A 1V pulse driving a known resistor value (“R”) provides a simple way to source calibrated current into the transformer.

If R = 10k, resultant pulsed current is 100μA. Figure B2’s oscilloscope photo shows test setup response. The waveform is crisp, essentially noise free and agrees with predicted amplitude. More sensitive measurement involves determining the test setup’s noise floor. Figure B3, taken with no current flowing in the transformer, indicates a noise limit of about 10μA_{p-p}. Most of this noise is due to the x100 amplifier.

The preceding exercise determines the test setup’s gain and noise performance. This information provides the confidence necessary to make a meaningful low level current measurement. Figure B4, taken with Figure B1’s R = 100k, sources only 10μA to the transformer. This is

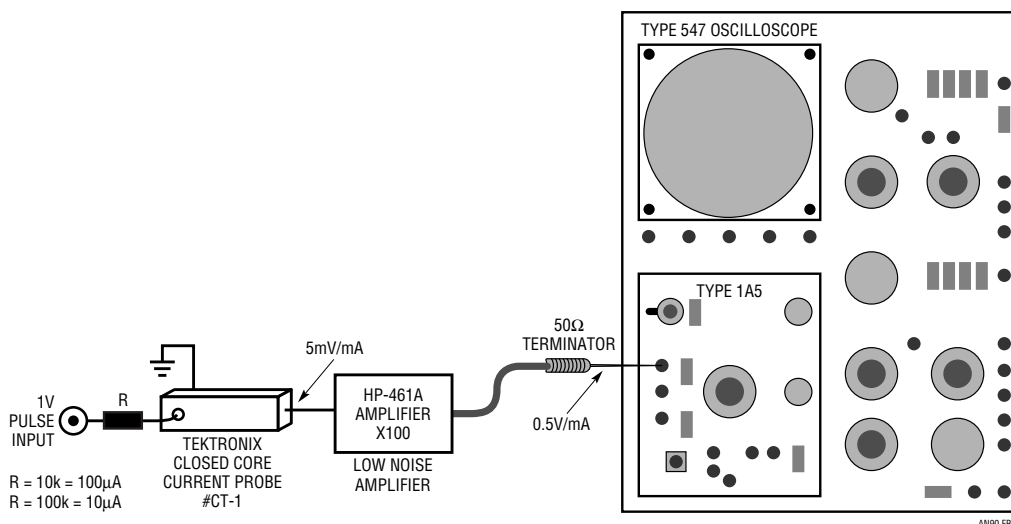


Figure B1. Noise Measurement Instrumentation Includes Resistors, Closed Core Current Probe, Low Noise Wideband Amplifier and Oscilloscope

Note 1: This is not to denigrate low level voltage probing methods. Their practice is well refined and directly applicable in appropriate circumstances. See Appendix C in Reference 7 for tutorial.

Note 2: See Appendix C, “Notes on Current Probes and Noise Measurement,” for a detailed comparison.

comparable to the previously determined noise floor but the trace, clearly delineated against the noise limit, indicates a $10\mu\text{A}$ amplitude. This level of agreement qualified this test method to obtain the text's quoted noise figures.

Isolated Trigger Probe

The performance limits noted above were determined with a well defined, pulsed input test signal. Residual switching regulator noise has a much less specific profile. The oscilloscope may encounter problems triggering on an ill-defined, noise laden waveform. Externally triggering the 'scope from the switching regulator's clocking solves this problem but introduces ground loops, corrupting the measurement.³ It is possible, however, to externally trigger the 'scope without making any galvanic connections to the circuit, eliminating ground loop concerns. This is

accomplished by coupling to the field produced by the switching regulator magnetics. A probe which does this is simply an RF choke terminated against ringing (Figure B5). The choke, appropriately positioned, picks up residual switching frequency related magnetic field, generating an isolated trigger signal.⁴ This arrangement furnishes a 'scope trigger signal with essentially no measurement corruption. The probe's physical form appears in Figure B6. For good results, the termination should be adjusted for minimum ringing while preserving the highest possible amplitude output. Light compensatory damping produces Figure B7's output, which will cause poor 'scope triggering. Proper adjustment results in a more favorable output (Figure B8), characterized by minimal ringing and well defined edges.

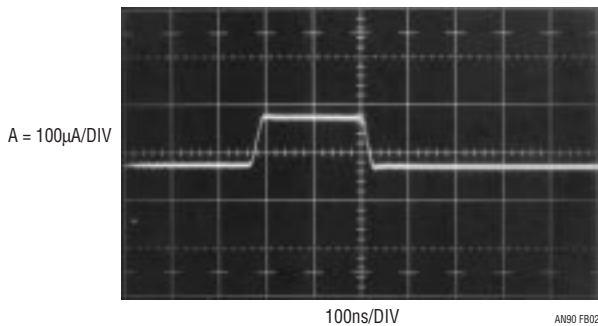


Figure B2. Response to a $100\mu\text{A}$ Input is Clean. Displayed Amplitude Agrees with Input Stimulus, Indicating Calibrated Measurement

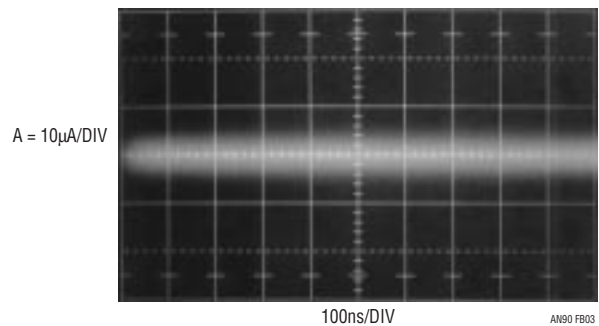


Figure B3. $10\mu\text{A}$ Noise Floor is Determined by Removing Current Loop from Transformer. Remaining Noise is Primarily Due to x100 Amplifier

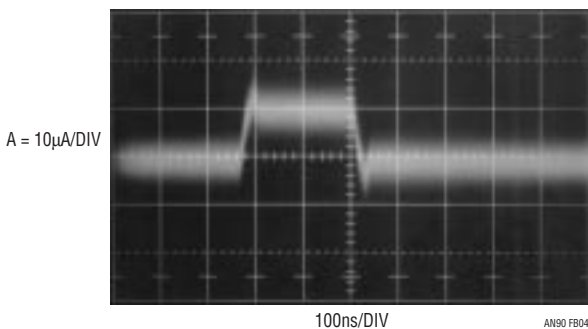


Figure B4. Verifying Gain Near Noise Floor. $10\mu\text{A}$ Input Pulse Produces Calibrated, Readily Discernable Output

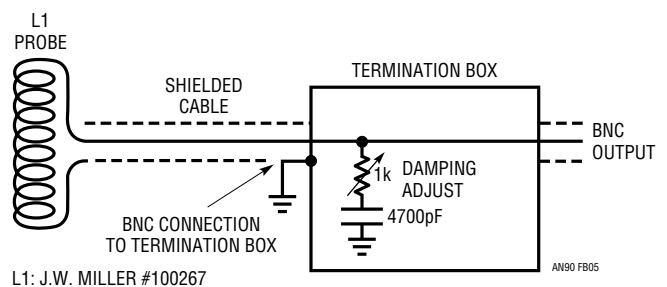


Figure B5. Simple Trigger Probe Eliminates Board Level Ground Loops. Termination Box Components Damp L1's Ringing Response

Note 3: See previous comments at the beginning of this appendix.

Note 4: Veterans of LTC application notes, a hardened crew, will recognize this probe's description from LTC Application Note 70 (Reference 7). It directly applies to this topic and is reproduced here for reader convenience.

Application Note 90

Trigger Probe Amplifier

The field around the switching magnetics is small and may not be adequate to reliably trigger some oscilloscopes. In such cases, Figure B9's trigger probe amplifier is useful. It uses an adaptive triggering scheme to compensate for variations in probe output amplitude. A stable 5V trigger output is maintained over a 50:1 probe output range. A1, operating at a gain of 100, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's

output signal appears at the junction of the 500pF capacitor and the 3M Ω units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394's positive input. The LT1394's negative input is biased directly from A1's output. The LT1394's output, the circuit's trigger output, is unaffected by >50:1 signal amplitude variations. An x100 analog output is available at A1.

Figure B10 shows the circuit's digital output (trace B) responding to the amplified probe signal at A1 (trace A).

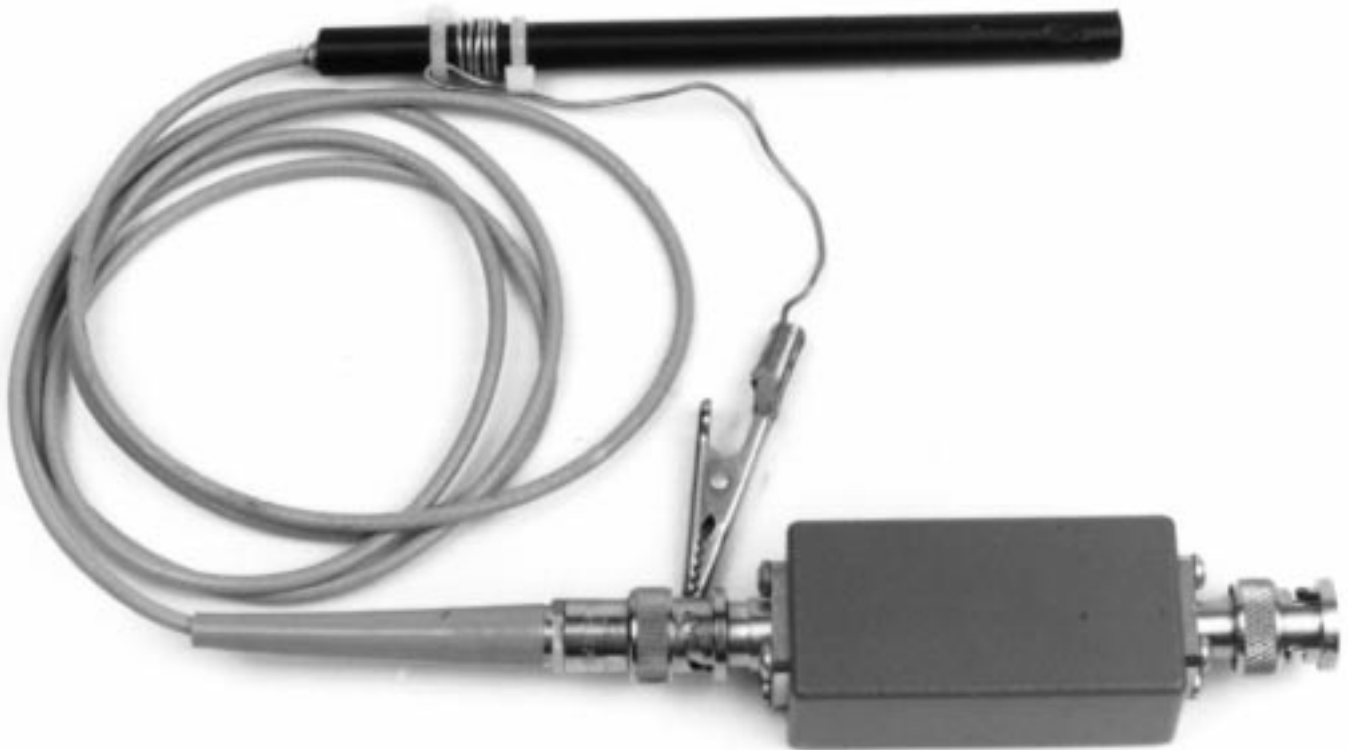


Figure B6. The Trigger Probe and Termination Box. Clip Lead Facilitates Positioning Probe, is Electrically Neutral

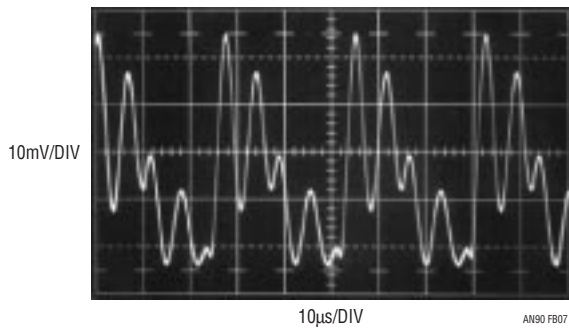


Figure B7. Misadjusted Termination Causes Inadequate Damping. Unstable Oscilloscope Triggering May Result

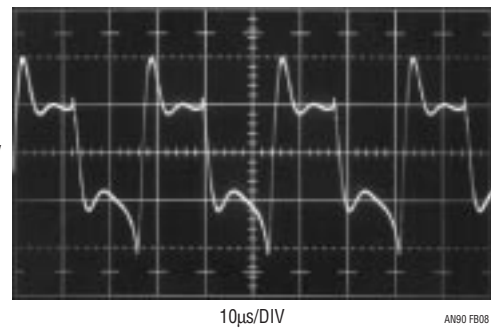


Figure B8. Properly Adjusted Termination Minimizes Ringing with Small Amplitude Penalty

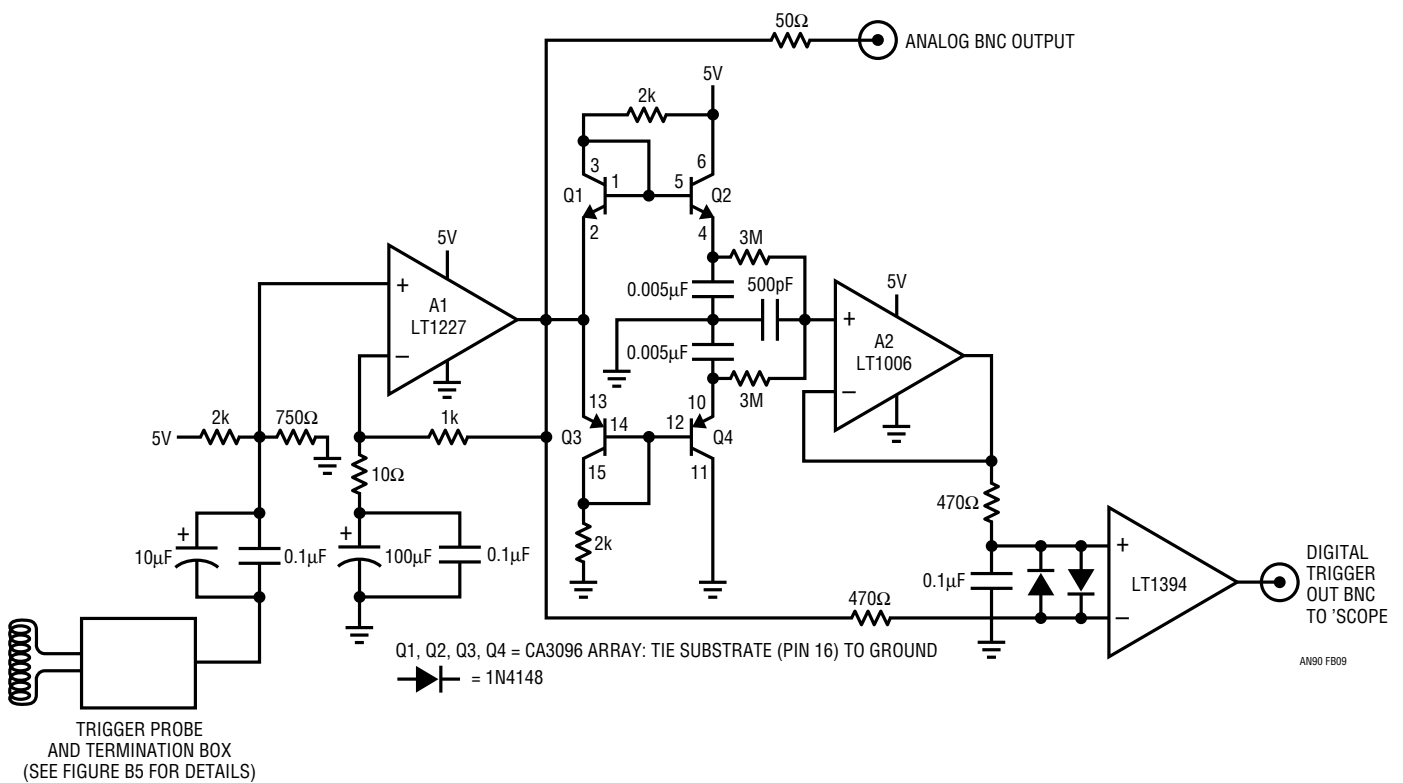


Figure B9. Trigger Probe Amplifier Has Analog and Digital Outputs. Adaptive Threshold Maintains Digital Output over 50:1 Probe Signal Variations

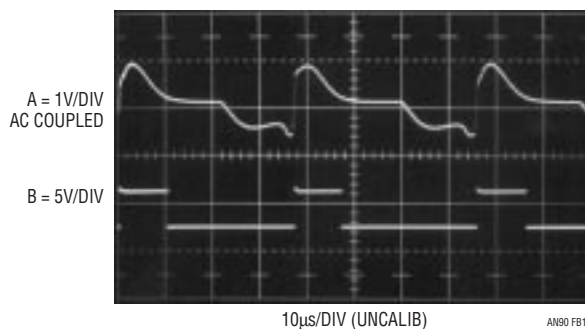


Figure B10. Trigger Probe Amplifier Analog (Trace A) and Digital (Trace B) Outputs

APPENDIX C

NOTES ON CURRENT PROBES AND NOISE MEASUREMENT

Appendix B explained current probes advantages in switching regulator related current noise measurement. Their minimally invasive nature eases connection parasitics, enhancing measurement fidelity. Different combinations of current probes and amplifiers provide varying degrees of performance and convenience. Figure C1 summarizes characteristics for two probes and applicable amplifiers. In general, the noise floor uncertainties of the convenient split core types are compromised by their construction. The closed core probes are less noisy and some types have inherently higher gain, a distinct advantage. A laboratory based comparison is revealing.

Figure C2 shows the CT-1 (closed core)-HP461A combination responding to a 100 μ A pulsed input. The waveform is clearly outlined, with pulse top and bottom trace thickening deriving from the noise floor.¹ Figure C3, taken with the same input, is degraded. The split core P6022-Preamble 1855 combination used has much greater noise. The decreased performance is almost entirely due to the split core probe's construction.

In closing, it is worthwhile noting that Hall element stabilized current probes (e.g., Tektronix AM503, P6042) are not suitable for low level measurement. The Hall device based flux nulling loop extends probe response to DC but introduces \approx 300 μ A of noise.

CURRENT PROBE	AMPLIFIER	NOISE FLOOR (100 MHz BW)	COMMENTS
Tektronix P6022 (1mV/mA)	Preamble 1855 (1M Ω)	100 μ A	Split Core is Convenient to Use but Sensitivity is Low, Resulting in Relatively High Overall Noise Floor
Tektronix CT-1 (5mV/mA)	Hewlett-Packard 461A (50 Ω)	15 μ A	Probe's Higher Gain Accounts for Most Noise Floor Reduction—50 Ω Input Amplifier Provides Some Additional Benefit. Closed Core Probe Requires Breaking Conductor to Make Measurement

Figure C1. Recommended Instrumentation for Current Noise Measurement. Split Core “Current Probe” is Convenient; Closed Core Provides Higher Gain and Lower Noise

Note 1: Diehard curmudgeons still using high quality analog oscilloscopes routinely discern noise presence due to trace thickening. Those stuck with modern instruments routinely view thick, noisy traces.

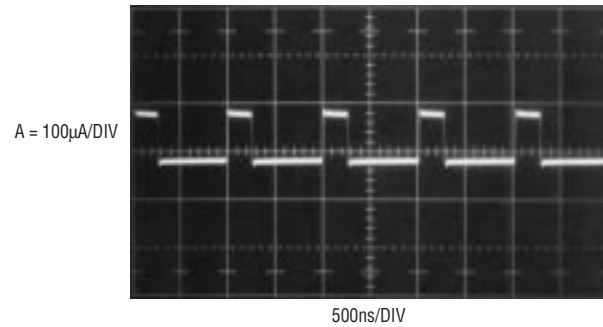


Figure C2. CT-1/HP-461A Combination Clearly Displays a 100µA Pulse Train. Noise Floor Causes Slight Pulse Top and Bottom Trace Thickening

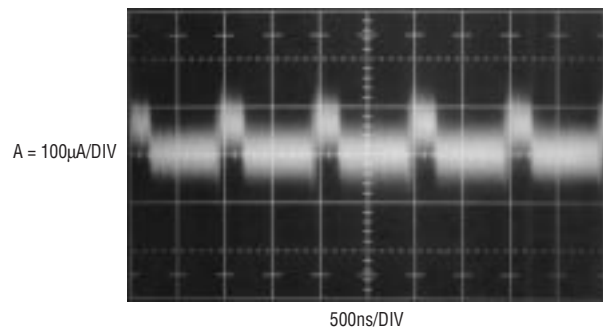
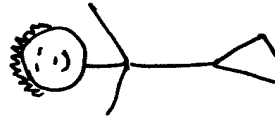


Figure C3. P6022/Preamble 1855 Presentation of Previous Figure's Waveform Has Degraded Signal-to-Noise Performance. Split Core "Current Probe" Convenience Necessitates Measurement Fidelity Compromise

Sacrebleu! Je n'aurais jamais cru que ma découverte ait pu amener du courant au laser.



Wu
Shu

Bonjour, M. André Ampère.
Je suis votre descendant et ma responsabilité est de fournir du courant au laser. Ma fonction doit être précise, fiable et elle doit protéger le laser. J'espère que vous êtes fier de moi.



Bias Voltage and Current Sense Circuits for Avalanche Photodiodes

Feeding and Reading the APD

Jim Williams, Linear Technology Corporation

INTRODUCTION

Avalanche photodiodes (APDs) are widely utilized in laser based fiberoptic systems to convert optical data into electrical form. The APD is usually packaged with a signal conditioning amplifier in a small module. An APD receiver module and attendant circuitry appears in Figure 1. The APD module (figure right) contains the APD and a transimpedance (e.g., current-to-voltage) amplifier. An optical port permits interfacing fiberoptic cable to the APD's photosensitive portion. The module's compact construction facilitates a direct, low loss connection between the APD and the amplifier, necessary because of the extremely high speed data rates involved.

The receiver module needs support circuitry. The APD requires a relatively high voltage bias (figure left) to operate, typically 20V to 90V. This voltage is set by the bias supply's programming port. This programming voltage may also include corrections for the APD's temperature dependent response. Additionally, it is desirable to monitor the APD's average current (figure center), which indi-

cates optical signal strength. This information can be combined with feedback techniques to maintain optical signal strength at an optimal level. The feedback loop's operating characteristics can also determine if deleterious degradation of optical components has occurred, permitting corrective measures to be taken. APD current is typically between 100nA and 1mA, a dynamic range of 10,000:1. This measurement, which should be taken with an accuracy inside 1%, normally must occur in the APD's "high side," complicating circuit design. This restriction applies because the APD's anode is committed to the receiver amplifier's summing point.

The APD module, an expensive and electrically delicate device, must be protected from damage under all conditions. The support circuitry must never produce spurious outputs which could destroy the APD module. Particular attention must be devoted to the bias supply's dynamic response under programming and power-up/down conditions. Finally, it is desirable to power the support circuitry from a single 5V rail.

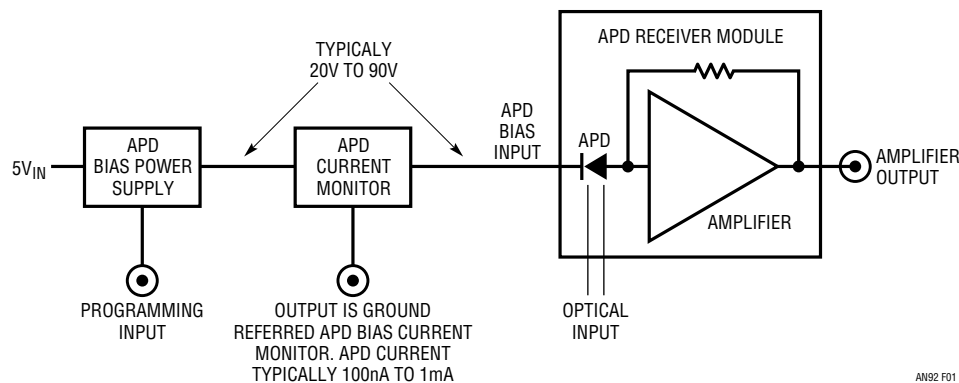


Figure 1. Avalanche Photodiode (APD) Module (Figure Right) Contains APD, Amplifier and Optical Port. Power Supply (Figure Left) Provides APD Bias Voltage. APD Current Monitor (Figure Center) Operates at High Common Mode Voltage, Complicating Signal Conditioning

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Application Note 92

The bias voltage and current measurement requirements described above constitute a significant design challenge and are addressed in the following text.

Simple Current Monitor Circuits (with Problems)

Figure 2's straightforward approaches attempt to address the current monitor problem. Figure 2a uses an instrumentation amplifier powered by a separate 35V rail to measure across the 1kΩ current shunt. Figure 2b is similar but derives its power supply from the APD bias line. Although both approaches function, they do not meet APD current sensing requirements. APD bias voltages can range to 90V, exceeding the amplifier's supply and common mode voltage limits. Additionally, the measurement's wide dynamic range requires the single rail powered amplifier to swing within 100μV of zero, which is impractical. Finally, it is desirable for the amplifiers to operate from a single, low voltage rail.

Figure 3's circuit divides down the high common mode voltage, theoretically permitting the 5V powered amplifier to extract the current measurement over a 20V to 90V APD bias range. In practice, this arrangement introduces prohibitive errors, primarily because the desired signal is also divided down. The current measurement information is buried in the divider resistor's tolerance, even with 0.01% components. The desired 1% accuracy over a 100mA to 1nA range cannot be achieved. Finally, although the amplifier operates from a single 5V supply, it cannot swing all the way to zero.

It is clear from the preceding circuits that common circuit approaches will not meet APD signal conditioning requirements. More sophisticated techniques are necessary.

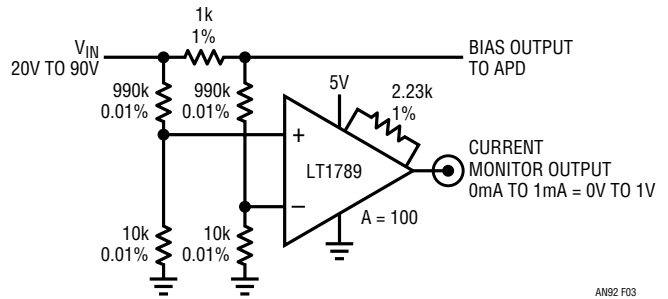
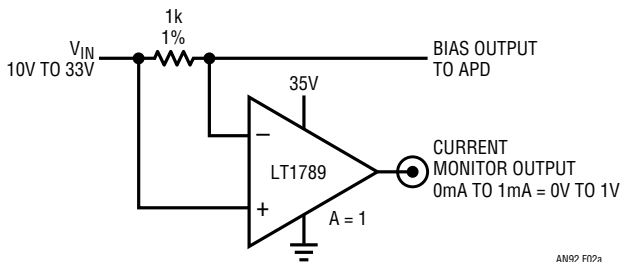


Figure 3. Dividing Down High Common Mode Voltage Introduces Huge Errors, Even with Precision Components. Desired 1% Accuracy Over 100nA to 1mA Current Monitor Range Is Buried by Resistor Mismatch, Even with 0.01% Resistors. Single Rail Powered Amplifier Cannot Swing Close Enough to Zero. Approach Is Impractical

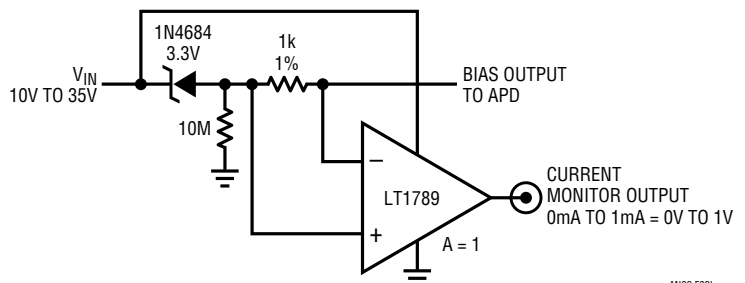
Carrier Based Current Monitor

Figure 4 utilizes AC carrier modulation techniques to meet APD current monitor requirements. It features 0.4% accuracy over the sensed current range, runs from a 5V supply and has the high noise rejection characteristics of carrier based "lock in" measurements.

The LTC1043 switch array is clocked by its internal oscillator. Oscillator frequency, set by the capacitor at Pin 16, is about 150Hz. S1 clocking biases Q1 via level shifter Q2. Q1 chops the DC voltage across the 1kΩ current shunt, modulating it into a differential square wave signal which



(2a)



(2b)

Figure 2. Instrumentation Amplifiers Extract Current Measurement from Modest Common Mode Voltages. Figure 2a Requires Separate Amplifier Power and Bias Supply Connections; Figure 2b Derives Both Connections from Single Point. Zener Level Shift Accommodates Amplifier Input Common Mode Range. Circuits Cannot Operate from Single, Low Voltage Rail, Swing Close to Zero or Accomodate High Bias Voltages

feeds A1 through 0.2μF AC coupling capacitors. A1's single-ended output biases demodulator S2, which presents a DC output to buffer amplifier A2. A2's output is the circuit output.

Switch S3 clocks a negative output charge pump which supplies the amplifier's V⁻ pins, permitting output swing to (and below) zero volts. The 100k resistors at Q1 minimize its on-resistance error contribution and prevent destructive potentials from reaching A1 (and the 5V rail) if either 0.2μF capacitor fails. A2's gain of 1.1 corrects for the slight attenuation introduced by A1's input resistors. In practice, it may be desirable to derive the APD bias voltage regulator's feedback signal from the indicated point, elimi-

nating the 1kΩ shunt resistor's voltage drop.¹ Verifying accuracy involves loading the APD bias line with 100nA to 1mA and noting output agreement.²

DC Coupled Current Monitor

Figure 5's DC coupled current monitor eliminates the previous circuit's trim but pulls more current from the APD bias supply. A1 floats, powered by the APD bias rail. The 15V zener diode and current source Q2 ensure A1 never is exposed to destructive voltages. The 1kΩ current shunt's voltage drop sets A1's positive input potential. A1 balances its inputs by feedback controlling its negative input via Q1. As such, Q1's source voltage equals A1's

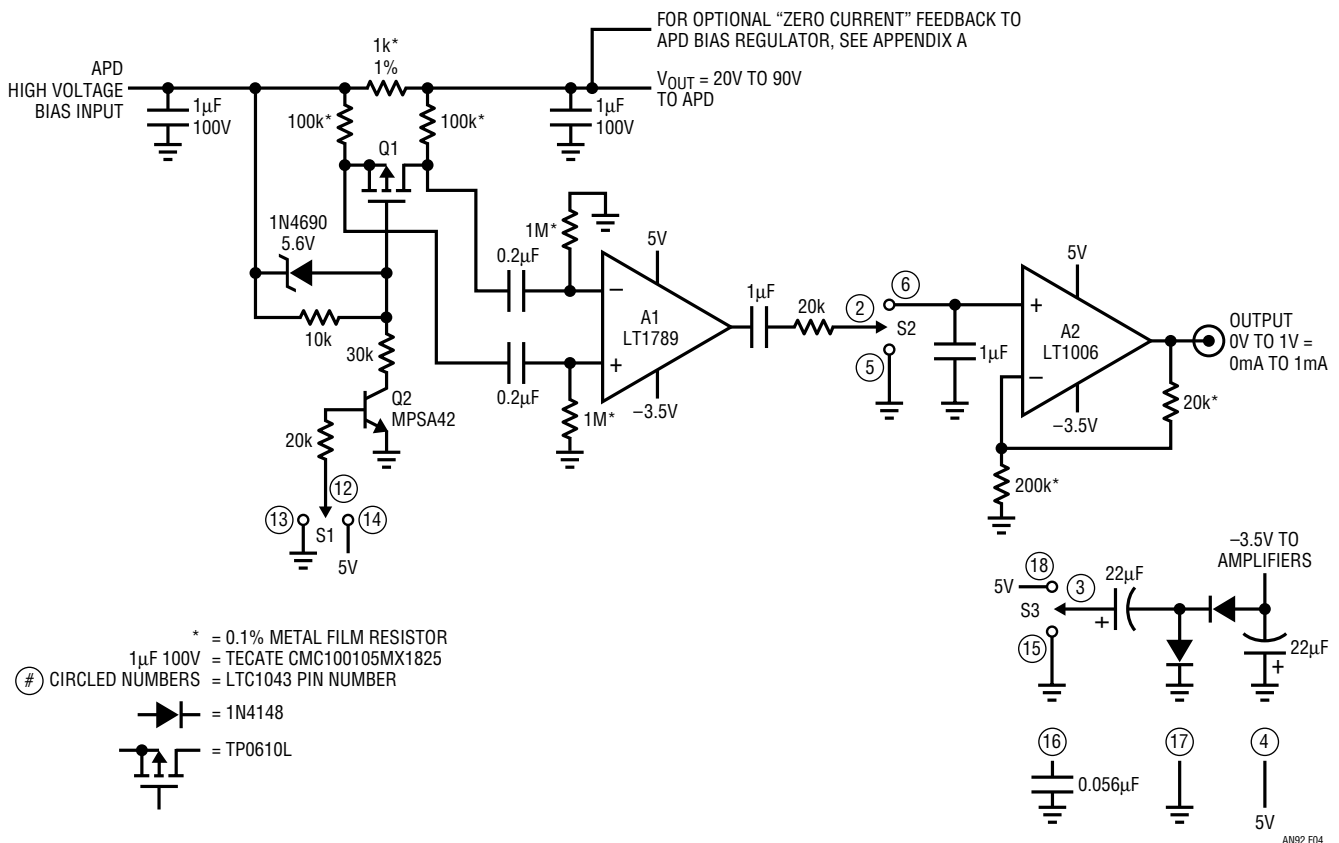


Figure 4. Lock-In Amplifier Technique Permits 1% Accurate APD Current Measurement Over 100nA to 1mA Range. APD Current Is AC Modulated by Q1, Single-Ended at A1 and Demodulated to DC by S2-A2

Note 1. See Appendix A, "Low Error Feedback Signal Derivation Techniques," for details.

Note 2. Appropriate high value load resistors, perhaps augmented with a monitoring current meter, are available from Victoreen and other suppliers. Tight resistor tolerance, while convenient, is not strictly required, as output target value is set by current meter indication.

Application Note 92

positive input voltage and its drain current sets the voltage across its source resistor. Q1's drain current produces a voltage drop across the ground referred 1k resistor identical to the drop across the 1kΩ current shunt and, hence, APD current. This relationship holds across the 20V to 90V APD bias voltage range. The 5.6V zener assures A1's inputs are always within their common mode operating range and the 10M resistor maintains adequate zener current when APD current is at very low levels.

Two output options are shown. A2, a chopper stabilized amplifier, provides an analog output. Its output is able to swing to (and below) zero because its V⁻ pin is supplied with a negative voltage. This potential is generated by using A2's internal clock to activate a charge pump which, in turn, biases A2's V⁻ pin.³

A second output option substitutes an A-to-D converter, providing a serial format digital output. No V⁻ supply is required, as the LTC2400 A-to-D will convert inputs to (and slightly below) zero volts.

Resistors at strategic locations prevent destructive failures. The 51kΩ unit protects A1 if the APD bias line shorts to ground. The 10k resistor limits current to a safe value if Q1 fails and the 100k resistor serves a similar purpose if Q2 malfunctions. As in the previous figure, APD voltage regulator feedback may be taken at the current shunt's output to maintain optimal regulation.⁴ As stated, this circuit does not require trimming and maintains 0.5% accuracy. It does, however, pull current approximately equaling the current delivered to the APD, in addition to Q2's collector current. This can be an issue if the APD bias supply has restricted current capability.

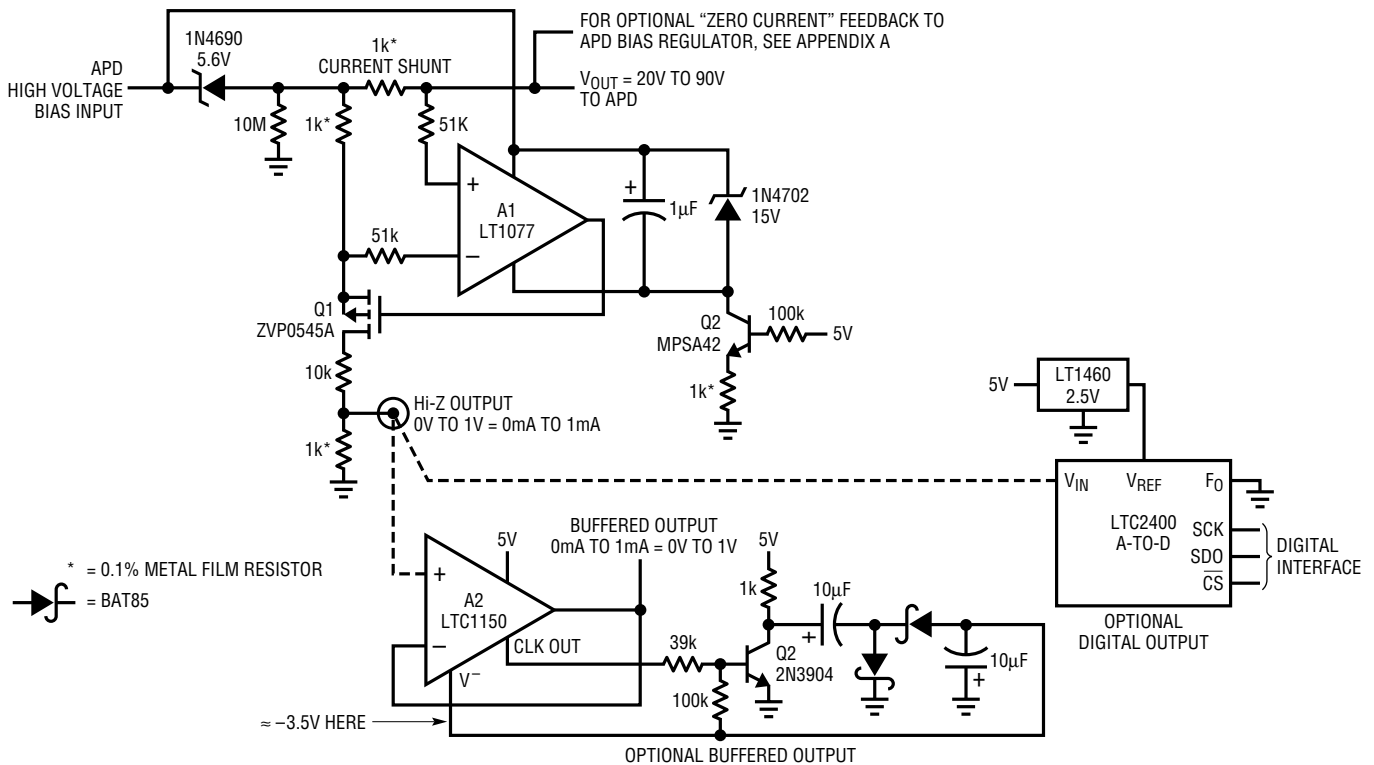


Figure 5. A1-Q1 Float at High Voltage Rail, Measuring APD Current Via 1kΩ Shunt. Q1's Ground Referred Drain Current Provides Hi-Z Output. Buffer Options Include Analog (Figure Bottom Left) and Digital (Figure Bottom Right)

Note 3. Circuit veterans will exercise extreme wariness when confronted with a bootstrapped biasing scheme such as this. Appendix D, "A Single Rail Amplifier with True Zero Volt Output Swing," should soothe anxieties.

Note 4: See Appendix A, "Low Error Feedback Signal Derivation Techniques."

APD Bias Supply

All previous examples have been current monitors. Figure 6, developed by Michael Negrete, is a high voltage APD bias supply.⁵ The LT1930A switching regulator and L1 form a flyback based boost stage. The flyback events pump a diode-capacitor network tripler, producing a high voltage DC output. Feedback from the output via the R1-R2 combination stabilizes the regulator's operating point. D6 and D7 protect the switch and feedback pins, respectively, from parasitic negative excursions and the 10Ω

resistors prevent excessive switch current. C8 and C9, series connected for high voltage capability, minimize output noise. A 0V to 4.5V programming voltage results in a corresponding 90V to 30V output (3% accuracy) with about 2mA of current capacity.

Circuit output noise is quite low. Figure 7, taken with 500μA loading at $V_{OUT} = 50V$, shows about 200μV ripple and harmonic residue in a 10MHz bandwidth. This is adequate for most APD receivers.⁶

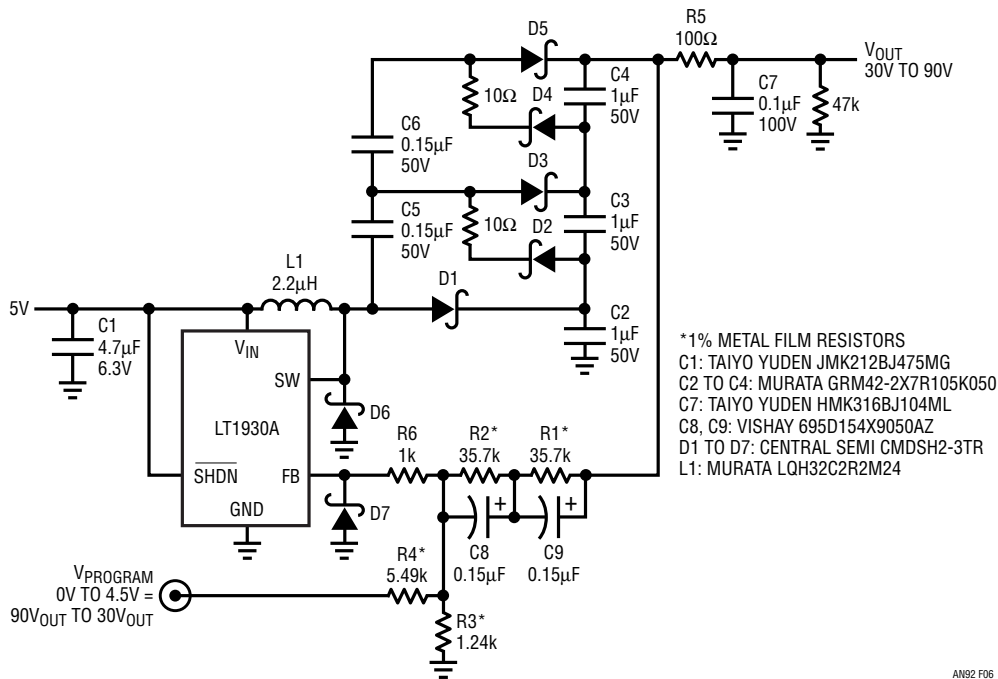


Figure 6. Boost Regulator/Charge Pump Supplies 30V to 90V APD Bias with Only 200μV_{p-p} Noise

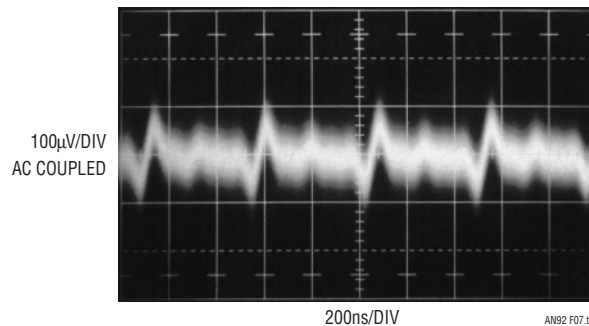


Figure 7. Figure 6's APD Bias Supply Shows 200μV_{p-p} Ripple and Harmonic Residue in 10MHz Bandwidth

Note 5: See Reference 7.

Note 6: Faithful noise measurements at these low levels requires considerable care. See Appendices B and C for practical details.

Application Note 92

APD Bias Supply and Current Monitor

Figure 8, the Martin Configuration, combines the previous circuit with Figure 5's current monitor, providing a complete APD signal conditioner.⁷ The programmable APD bias supply is as before, except that feedback comes via A2. A2, sensing after the 1k Ω current shunt, isolates the R1-R2 path loading, preventing it from influencing the shunt's voltage drop. A2's action also insures tight output regulation, despite the current shunt's presence.⁸

The current monitor, borrowing from Figure 5, measures across the 1k Ω current shunt, presenting its output in Q1's drain line. As shown, the output has about 1k Ω output impedance, although either of Figure 5's output options may be employed.

When considering circuit operation, note that both amplifiers are powered by the charge pump's high voltage output, with their V⁻ pin returned to the "2/3 V_{OUT}" point. This biasing permits the amplifiers to process high voltage signals, although the voltage across them never exceeds 30V.

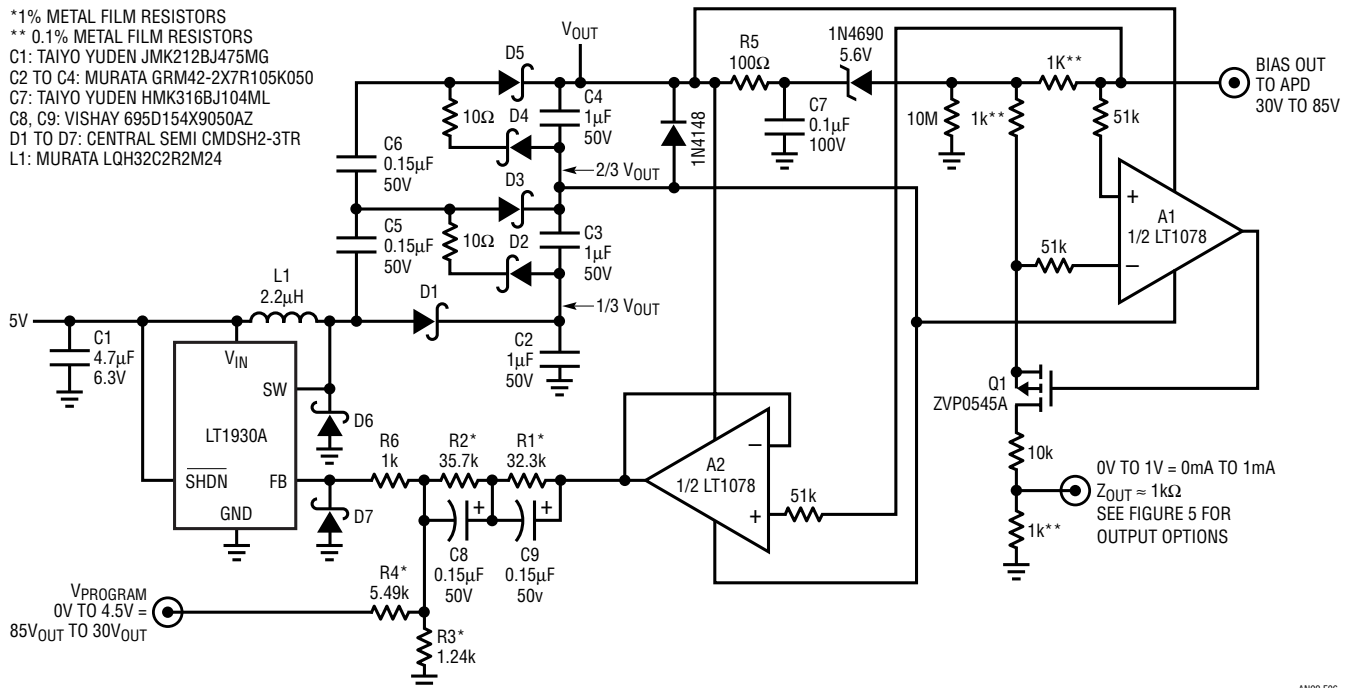


Figure 8. Figure 5's Current Monitor Combines with Figure 6's Bias Supply, Providing APD Bias and Current Measurement. A2 Buffers LT1930A's Feedback Path Loading from Bias Supply Output, Eliminating Current Error. Amplifiers Process 85V Signals, Although Voltage Across Them Never Exceeds 30V

Note 7: This circuit is based on work by Alan Martin.

Transformer Based APD Bias Supply and Current Monitor

Figure 9's circuit, another complete APD bias supply and current monitor, uses different techniques than the previous example. Advantages include 0.25% bias voltage and current monitoring accuracy, small size and fewer high voltage components for greater reliability. The LT1946 switching regulator and T1 form a flyback type boost configuration. T1's turn ratio provides voltage gain and the high voltage flyback events are rectified and smoothed to DC by the diode and capacitor in T1's secondary. This DC potential is divided down and fed back to A1. A1 compares this signal to the APD bias programming input and sets the LT1946's operating point, closing a control loop. Loop compensation is furnished by local rolloff at A1 and a lead network across the 10M feedback resistor. This loop establishes and maintains the APD bias output in accordance with the programming input's value. C1, active at V_{SUPPLY} = 1.2V, prevents output overshoot at power turn on by grounding the programming input command while

Note 8: See Appendix A, "Low Error Feedback Signal Derivation Techniques," for further discussion.

simultaneously forcing A1's output low. This shuts off the switching regulator and no high voltage is produced. When power at turn on reaches $\approx 4V$, C1 changes state and A1's positive input ramps to the programming voltage. The switching regulator's output follows this turn-on profile and no overshoot occurs. The LT1004 clamps spurious programming inputs beyond 2.5V, preventing excessive high voltage outputs.⁹

The circuit's current monitor portion takes full advantage of T1's floating secondary. Here, the $1k\Omega$ current shunt resides in T1's secondary return path (Pin 3), eliminating the high common mode voltages encountered in the previous "high side" sensed examples. Circuit ground is declared at the shunt's uncommitted terminal, meaning

T1's Pin 3 will undergo increasing negative excursion with greater APD current. Inverter A2 converts the shunt's negative voltage to a buffered positive output. Its gain, scaled 1% above unity, compensates its input resistor's shunt loading error. Swing to zero is facilitated by returning A2's V^- pin to a small negative potential derived from the LT1946's V_{SW} pin switching. The $10M-287k$ divider's current loading error is prevented from appearing in A2's output by a compensatory current from the APD bias programming input. This compensating current, arriving at A2 via the $100k-3.65k-1M$ network, is scaled to precisely balance out the shunt's output portion due to the $10M-287k$ path's loading error. See Appendix A for detailed discussion of this technique.

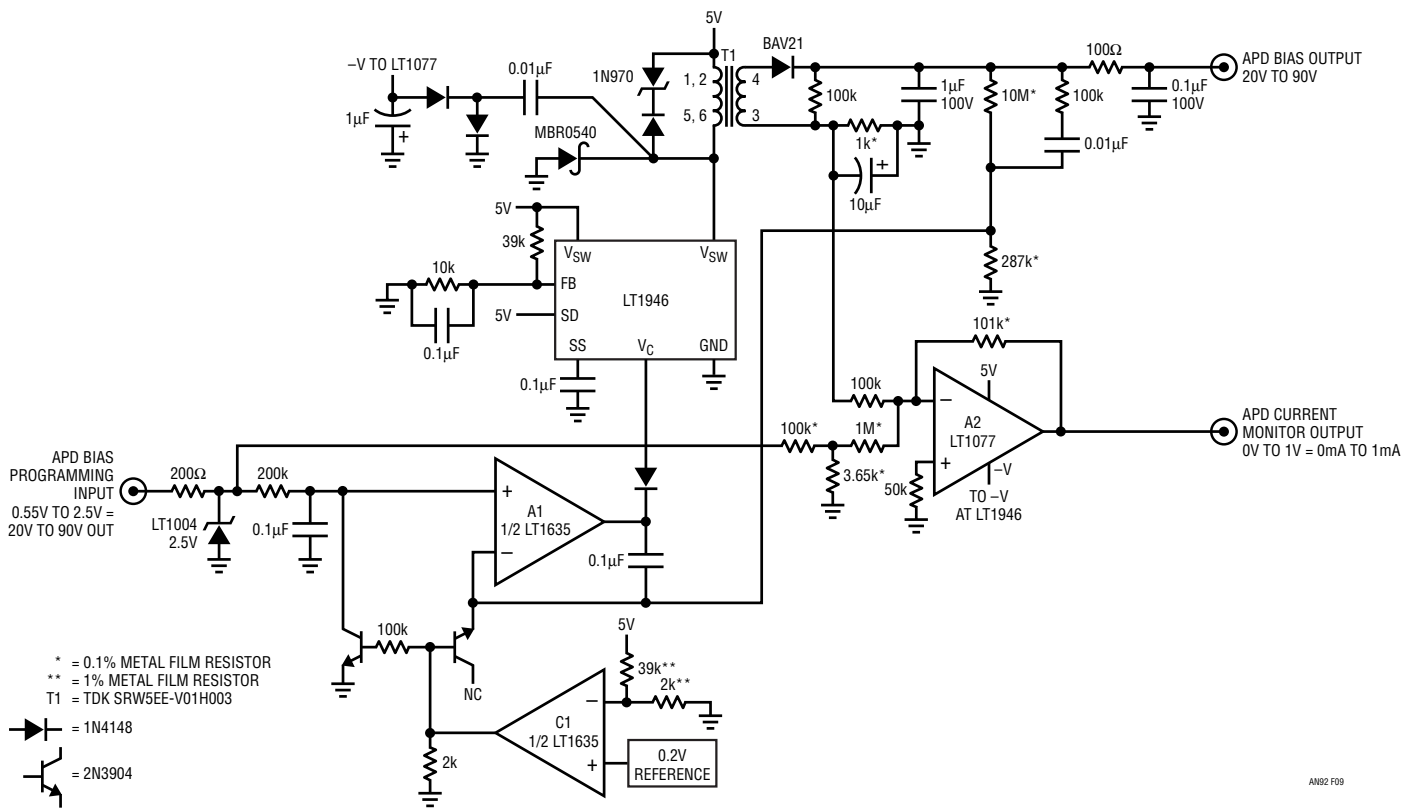


Figure 9. A1 Controls LT1946 Boost Regulator to Supply 20V to 90V Bias. C1 Prevents Output Overshoot at Power Turn-On. A2 Senses APD Current Across $1k\Omega$ Shunt in T1's Output Return. Programming Input Feedforward to A2 Cancels $10M-287k$ Feedback Divider's Loading Error, Preserving Current Monitor Accuracy

Note 9: Optional circuitry allows input clamping at any desired voltage. See Appendix E, "APD Protection Circuits."

Application Note 92

Output noise for this circuit, shown in Figure 10, is about $1\text{mV}_{\text{P-P}}$ in a 10MHz bandwidth. This is characteristic of flyback regulators and somewhat higher than Figure 8's charge pump based arrangement. It is still acceptable for most APD receivers, although special switching regulator techniques (read on!) can considerably reduce this figure.

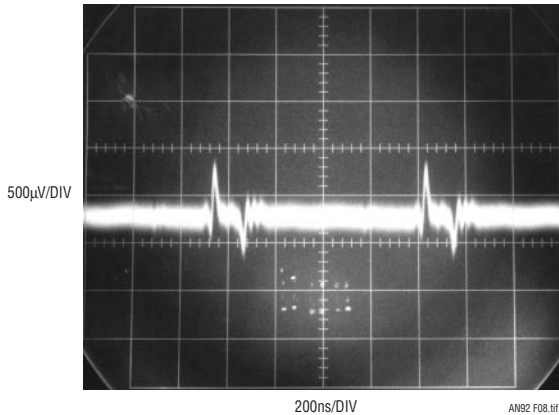


Figure 10. Figure 9's Output Noise Measures $1\text{mV}_{\text{P-P}}$ in 10MHz Bandwidth

Inductor Based APD Bias Supply

Figure 11 borrows from Figure 9's flyback technique to form a simple, small area APD bias supply. Figure 9's current monitor function has been deleted—this circuit provides only the bias supply. Additionally, Figure 9's transformer has been replaced with a 2-terminal inductor. The circuit is a basic inductor flyback boost regulator with a single important deviation. Q1, a high voltage device, has been interposed between the LT1946 switching regulator and the inductor. This permits the regulator to control Q1's high voltage switching without undergoing high voltage stress. Q1, operating as a "cascode" with the LT1946's internal switch, withstands L1's high voltage flyback events.¹⁰ Diodes associated with Q1's source terminal clamp L1 originated spikes arriving via Q1's junction capacitance. The high voltage is rectified and filtered to DC, forming the circuit's output. Feedback to the regulator

stabilizes the output, which may be varied by appropriate biasing at the V_{PROGRAM} input. Components at the LT1946 V_{C} pin compensate the loop. Over a 20V to 90V output range, the circuit remains within 2% of the V_{PROGRAM} input dictated output voltage. Figure 12 shows switching related output noise is about 1.3millivolts peak-to-peak in a 10MHz bandwidth.

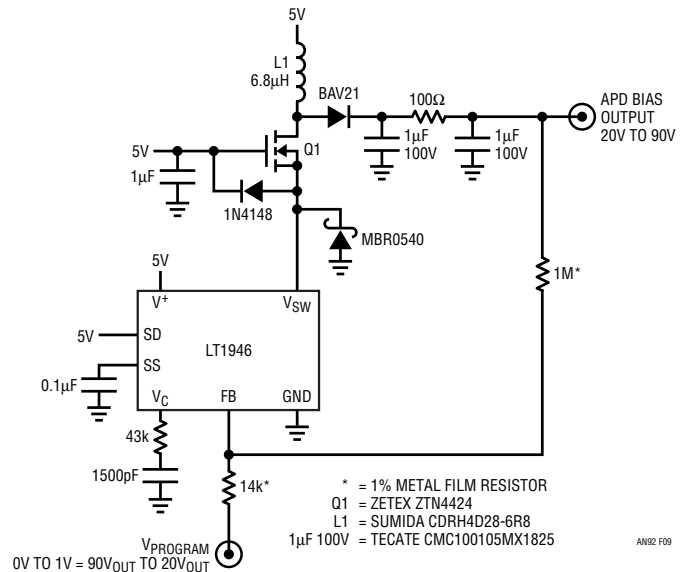


Figure 11. Q1 Cascode with LT1946 Switches L1, Providing 20V to 90V APD Bias Output. Q1's Source Diodes Clamp Parasitic Conducted Spikes to Safe Levels

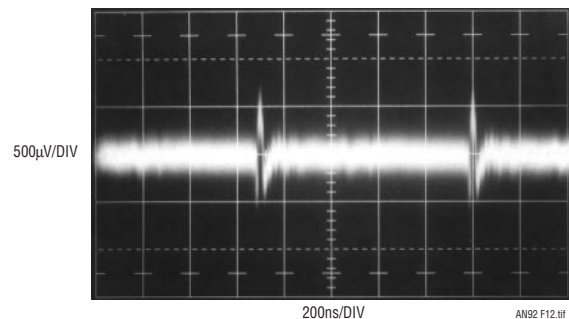


Figure 12. Cascode Based Bias Supply Noise in 10MHz Bandwidth Is About $1.3\text{mV}_{\text{P-P}}$

Note 10: See Reference 11.

200 μ V Output Noise APD Bias Supply

Some APD receiver applications require extremely low noise in an extended bandwidth. Figure 13's APD bias supply uses special switching regulator techniques to achieve 200 μ V noise in a 100MHz bandwidth. The LT1533 is a "push-pull" output switching regulator with controllable switch transition times. Output harmonic content ("noise") is notably reduced with slower switch transition times.¹¹ Switch current and voltage transition times are

controlled by resistors at the R_{CSL} and R_{VSL} pins, respectively. In all other respects, the circuit behaves as a classical push-pull, transformer based, step-up converter. The V_{PROGRAM} input biases a feedback loop, setting the output anywhere between 20V and 90V.

The controlled transition times result in a dramatic decrease in output noise. Figure 14 shows ripple and switching related residue of 200 μ V in a 100MHz bandwidth. This is far below conventional regulators, meeting the most stringent noise requirement.

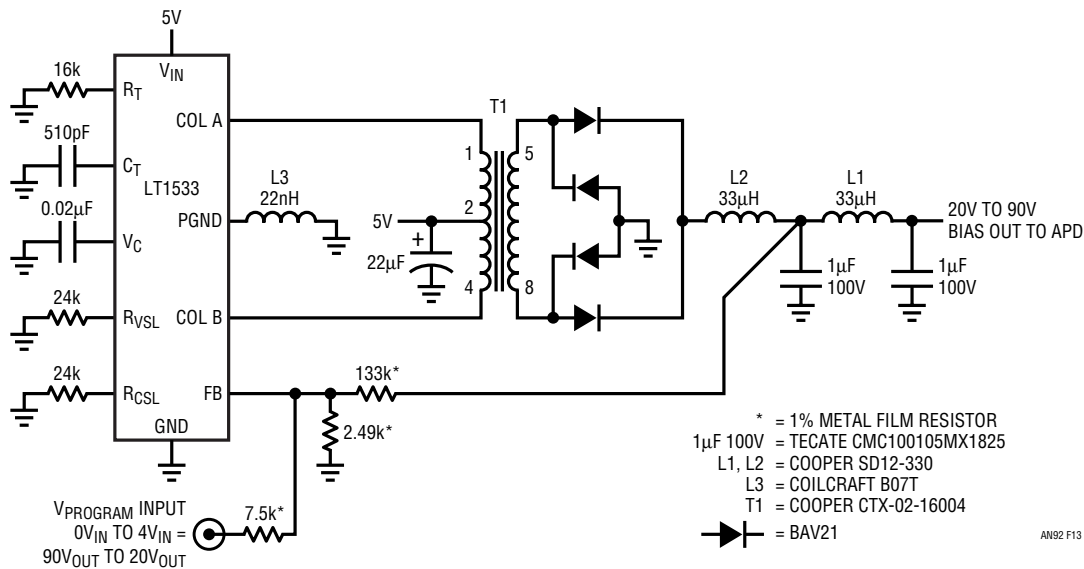


Figure 13. Transformer Coupled 20V to 90V APD Bias Supply Controls Switch Transition Time for Extremely Low Output Noise

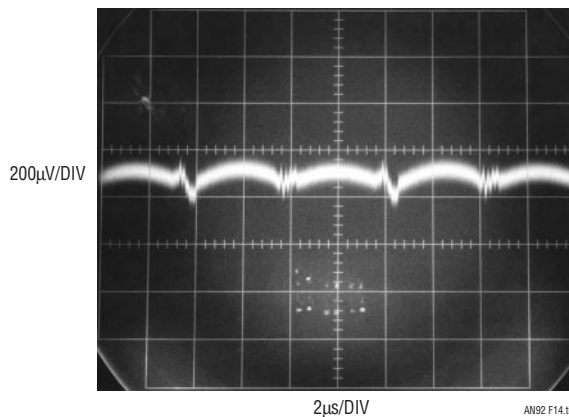


Figure 14. LT1533's Controlled Transition Times Achieve Spectacularly Low Output Harmonic Residue. Switching Related Noise Is Below 100 μ V, Fundamental Ripple About 200 μ V. Measurement Bandwidth is 100MHz

Note 11: Noise contains no regularly occurring or coherent components. As such, switching regulator output "noise" is a misnomer. Unfortunately, undesired switching related components in the regulated output are almost always referred to as "noise." Accordingly, although technically incorrect, this publication treats all undesired output signals as "noise." See Reference 2.

Application Note 92

Low Noise APD Bias Supply and Current Monitor

Figure 15 builds on the previous circuit's performance, forming a complete, high performance APD signal conditioner. The bias supply is identical to Figure 13's low noise example, with the addition of the A1 based feedback buffer. This stage, similar to the one in Figure 8, isolates the regulator's feedback path current from the 1kΩ shunt, preserving current monitor accuracy. A1's zener-current source power biasing scheme permits it to process high voltage signals even though it is a low voltage device.¹² The current monitor, shown in block form, may be selected from the choices indicated depending upon requirements.

0.02% Accuracy Current Monitor

Some APD current monitor applications call for high accuracy and stability. Figure 16's unusual optical switching based approach achieves 0.02% accuracy over a sensed 100nA to 1μA range. This scheme measures shunt current by switching (S1A, S1B) a capacitor across the shunt ("ACQUIRE"). After a time the capacitor charges to the voltage across the shunt. S1A and S1B open and S2A and S2B close ("READ"). This grounds one capacitor plate

and the capacitor discharges into the grounded 1μF unit at S2B. This switching cycle is continuously repeated, resulting in A1's ground referred positive input assuming the same voltage that is across the floating 1kΩ shunt. The LED driven MOSFET switches specified do not have junction potentials and the optical drive contributes no charge injection error. A nonoverlapping clock prevents simultaneous conduction in S1 and S2, which would result in charge loss, causing errors and possible circuit damage. The 5.1V zener prevents switched capacitor failure if the bias output is shorted to ground.

A1, a chopper stabilized amplifier, has a clock output. This clock, level shifted and buffered by Q3, drives a logic divider chain. The first flip-flop activates a charge pump, pulling A1's V⁻ pin negative, permitting amplifier swing to (and below) zero volts.¹³ The divider chain terminates into a logic network. This network provides phase opposed charging of the 0.02μF capacitors (Traces A and B, Figure 17). The gating associated with these capacitors is arranged so the logic provides nonoverlapping, complementary biasing to Q1 and Q2. These transistors supply this nonoverlapping drive to the S1 and S2 actuating LEDs (Traces C and D).

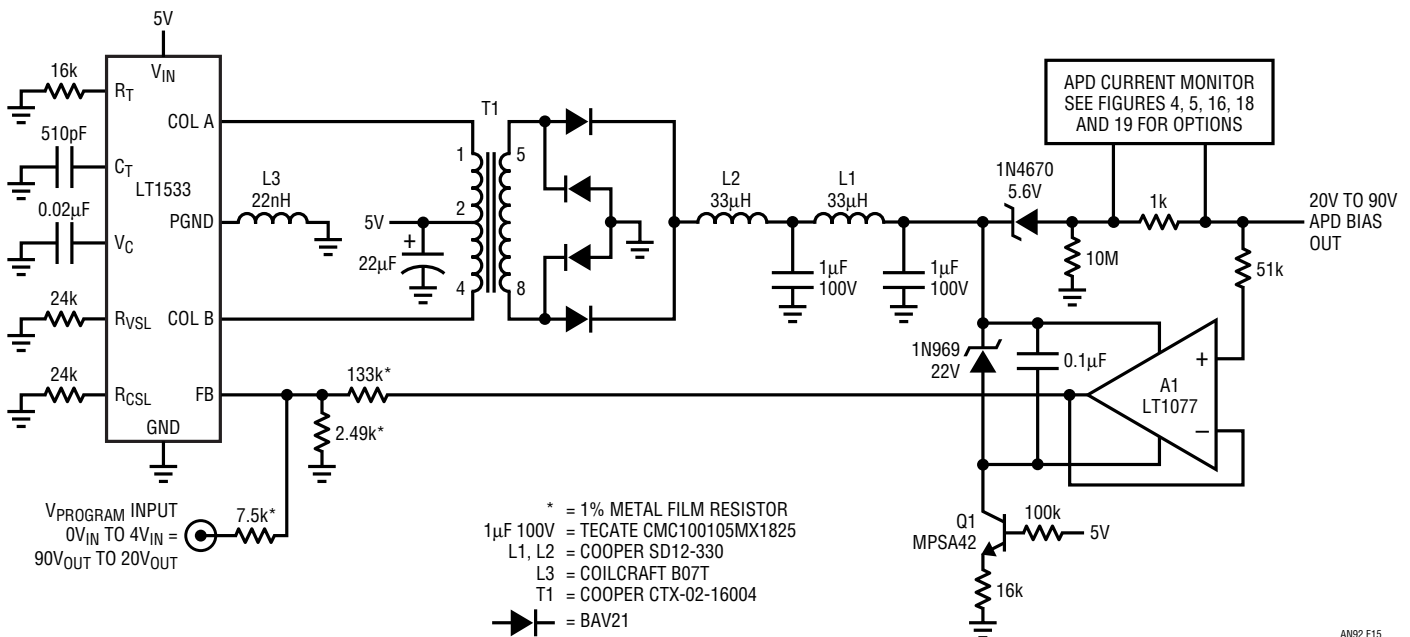


Figure 15. Figure 13 Augmented with Feedback Divider Buffer and Current Monitor Provides Complete 100μV Noise APD Signal Conditioner

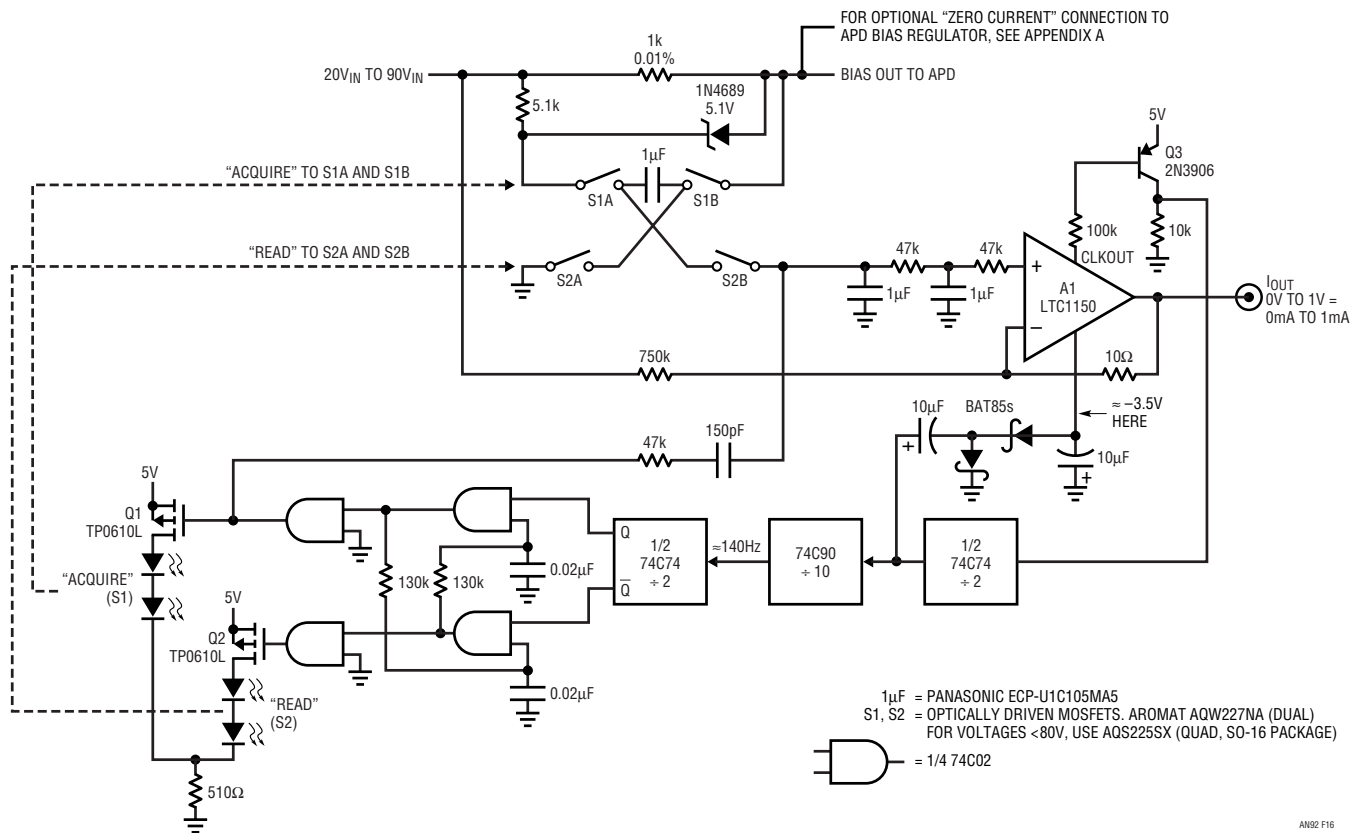
Note 12: The feedback buffer is considered in detail in Appendix A, "Low Error Feedback Signal Derivation Techniques."

Note 13: This scheme, a variant of the one described back in Figure 5, is detailed in Appendix D, "A Single Rail Amplifier with True Zero Volt Output Swing."

The extremely small parasitic error terms in the LED driven MOSFET switches results in nearly theoretical circuit performance. However, residual error ($\approx 0.1\%$) is caused by S1A's high voltage switching pumping S2B's 3pF to 4pF junction capacitance. This results in a slight quantity of unwanted charge being transferred to the $1\mu\text{F}$ capacitor at S2B. The amount of charge transferred varies with the APD bias voltage (20V to 90V) and, to a lesser extent, the varactor-like response of S2B's off-state capacitance.

These terms are partially cancelled by DC feedforward to A1's negative input and AC feedforward from Q1's gate to S2B. The corrections compensate error by a factor of five, resulting in 0.02% accuracy.

Optical switch failure could expose A1 to high voltage, destroying it and possibly presenting destructive voltages to the 5V rail. This most unwelcome state of affairs is prevented by the 47k resistors in A1's positive input.



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Figure 16. A 0.02% Accurate APD Current Monitor Utilizes Optically Driven FETs and Flying Capacitor. Logic Driven Q1-Q2 Provides Nonoverlapping Clocking to S1-S2 LEDs. Clock Derives from A1's Internal Oscillator

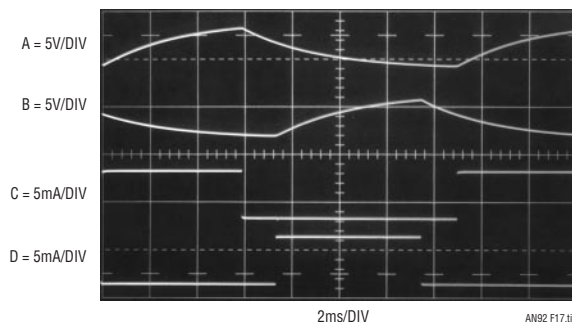


Figure 17. Clocked, Cross Coupled Capacitors (Traces A and B) in 74C02 Based Network Result in Nonoverlapping Drive (Traces C and D) to S1-S2 Actuating LEDs

Application Note 92

Digital Output 0.09% Accuracy Current Monitor

Figure 18 modifies the optically based current monitor to supply a digital output. The schematic is essentially identical to Figure 16's, with two significant differences. Here, a digital output is supplied via the LTC2431 A-to-D converter. The converter's differential inputs allow the same feedforward based error correction used in the previous example. The divider chain countdown ratio has changed to accommodate a higher speed clock, sourced by the LTC1799 oscillator. This higher speed clock, which times A-to-D operation, centers the A-to-D's internal notch filter at the optical switches commutation frequency, maximizing rejection.¹⁴

This circuit's 0.09% accuracy does not equal the previous analog output's version because of the LT1460 reference's 0.075% tolerance, which is not trimmable. The circuit can be adjusted to 0.02% accuracy by trimming the 1kΩ shunt so measured output current directly corresponds to A-to-D output.

Digital Output Current Monitor

Previous current monitor examples furnish digital output from ground referenced A-to-D converters fed from analog level shifting stages. Figure 19 directly digitizes shunt current by floating the A-to-D converter in the APD bias line. The A-to-D output is level shifted in the digital

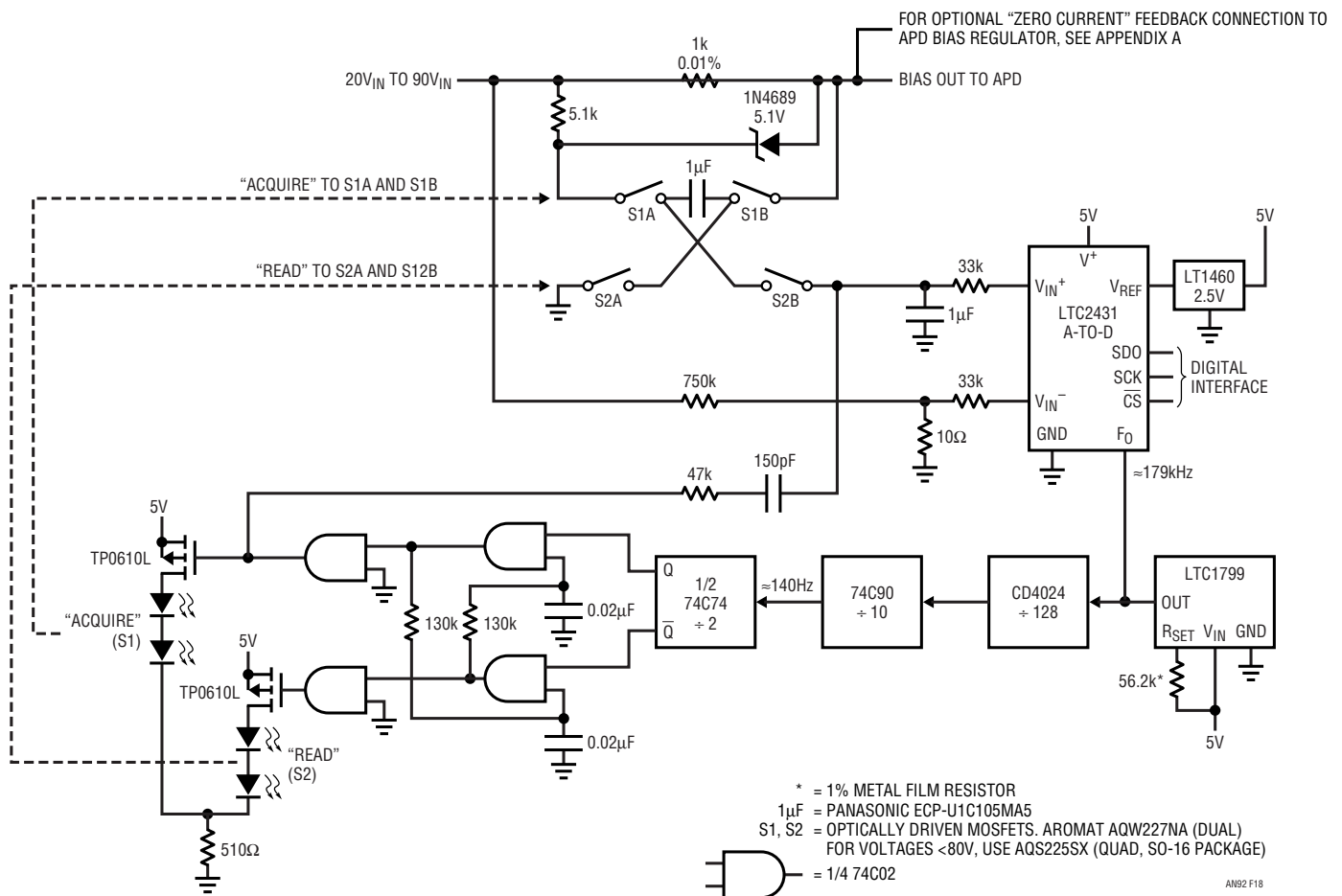


Figure 18. Figure 16's Optically Driven FET Based Current Monitor Modified for Digital Output. LTC1799 Clocks A-to-D and Optical Switch LEDs. 0.09% Accuracy, Trimmable to 0.02%

Note 14: The LTC2431's internal digital filter's first null occurs at 1/2560 of the frequency applied to its F₀ pin. For details, see the LTC2431 data sheet.

domain, presenting ground referred digital data. This simple approach is attractive, although the available APD bias supply must supply about 3mA to the A-to-D and its attendant circuitry.

The LTC2410 and its LT1029 reference are powered directly from the high voltage APD bias supply input. Current sink Q3 and the LT1029 bias the LTC2410 V^- pin, maintaining 5V across the A-to-D over the 20V to 90V bias rail range. The A-to-D's differential inputs measure across the 1k Ω current shunt. Resistors and a zener clamp protect the A-to-D from excessive voltages if the APD bias line is shorted to ground. The A-to-D's digital outputs, floating at high voltage, drive level shifts which provide

ground referred data. One of the identical stages is shown; the other indicated in conceptual form. The stage is designed for low quiescent and dynamic current consumption while maintaining data fidelity. This is necessary to minimize current drain from the APD bias supply and to avoid modulating it with transient loading artifacts. High voltage common emitter Q1 sources current to Q2, which provides a ground referred logic compatible output. Capacitive feedforwards maintain data edge speed while minimizing standing current requirements.

This circuit's 0.25% untrimmed accuracy is due to shunt and LT1029 tolerances. Trimming the LT1029 (see schematic note) permits 0.05% accuracy.

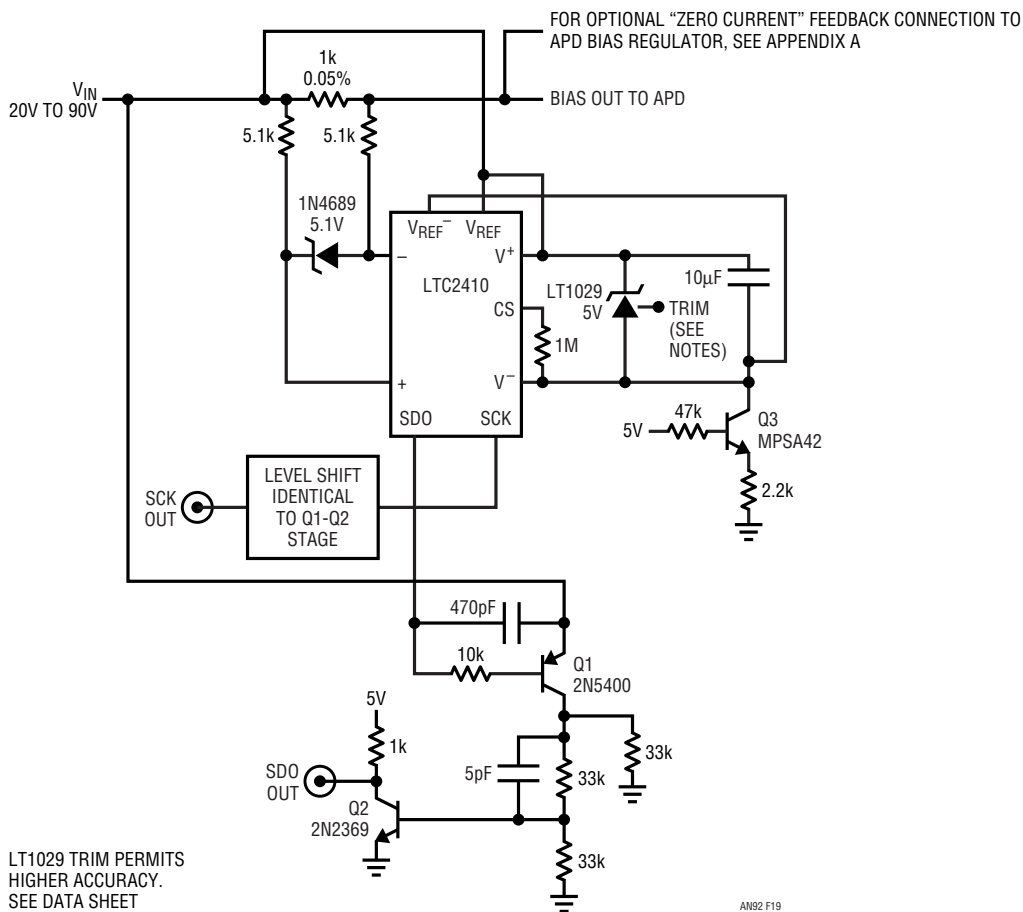


Figure 19. A-to-D Converter Floats at High Voltage, Forming Digital Output Current Monitor. Q1-Q2 Level Shift Provides Ground Referenced Digital Output. 0.25% Accuracy Is Trimmable to 0.05%

Application Note 92

Digital Output Current Monitor and APD Bias Supply

Figure 20 also floats an A-to-D converter across the shunt, while including an APD bias supply. The bias supply is derived from the LT1946 switching regulator and Q1, operating in nearly identical fashion to Figure 11's circuit. The primary difference is that Figure 11's inductor is replaced here with a transformer. The transformer's primary winding furnishes high voltage step-up, similar to Figure 11. The floating secondary drives an isolated LT1120 based 3.75V regulator. This floating regulator's output, stacked on top of the APD bias line, powers the LTC2400 A-to-D converter. The isolated 3.75V supply permits the A-to-D to measure across the 1kΩ shunt without pulling

operating power from the APD supply. Resistive current limiting and the 5.1V zener protect the A-to-D from high voltage if the APD bias output is shorted to ground. Low power optoisolators provide ground referred digital output while eliminating floating supply "starve out" due to cross regulation interaction with the APD regulation loop. Specifically, very low power APD bias outputs could result in insufficient transformer flux to furnish floating supply loading requirements. Common optoisolators require significant current, mandating the low power types specified. The previous circuit's discrete level shift stage would draw even less power but the optoisolators are simple and adequate.

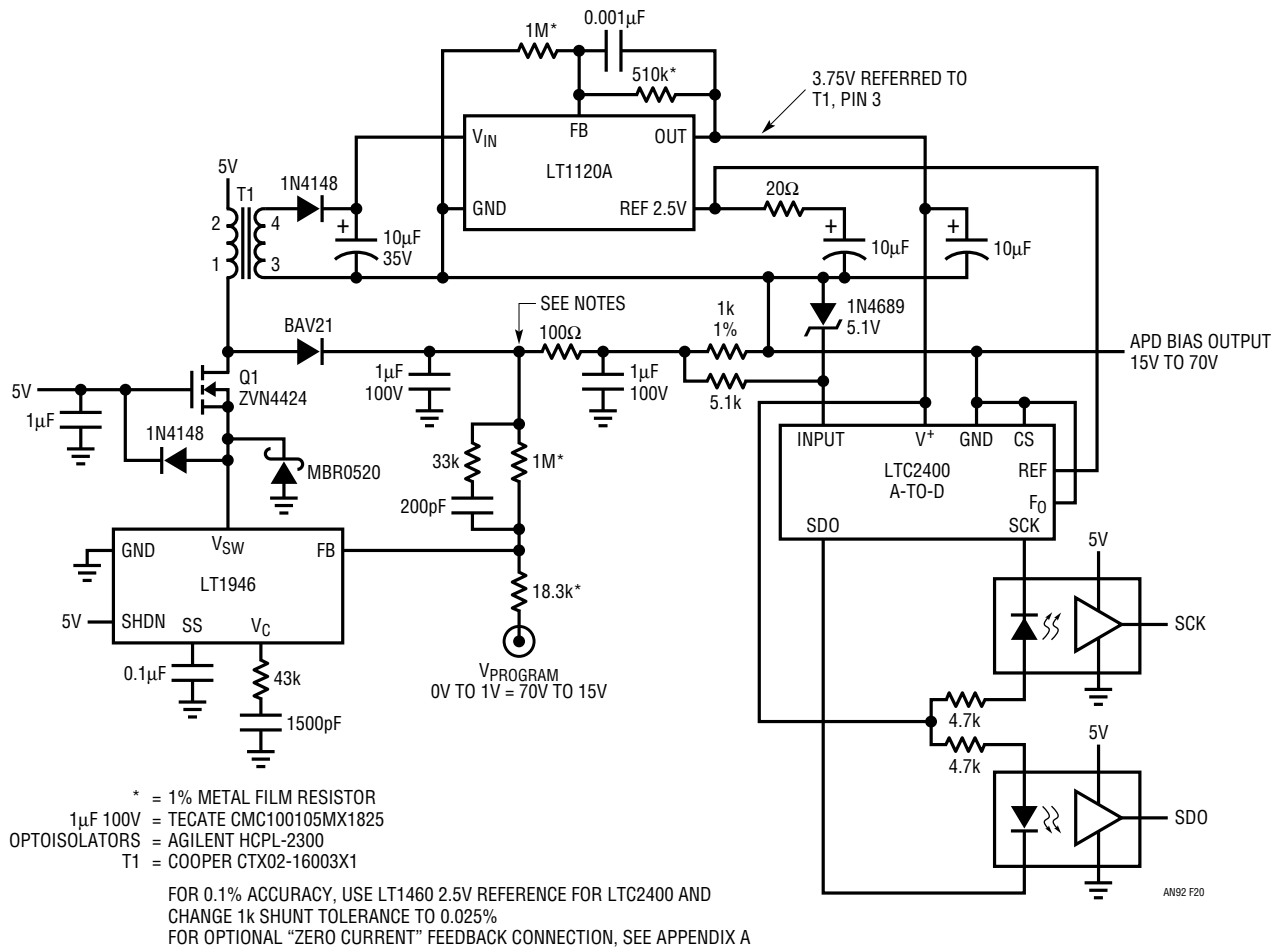


Figure 20. APD Bias Supply with Digital Output Current Monitor. T1's Primary Supplies APD High Voltage Source, Similar to Figure 11; Secondary Furnishes Power to Floating Circuitry. 1kΩ Shunt Voltage Drop Is Compensatable Using Optional Feedback Circuitry. Optoisolators Provide Ground Referred Digital Output. Current Monitor Accuracy is 2%, Trimmable to 0.1%

The LT1120 2.5V reference and 1kΩ shunt tolerances dictate 2% circuit accuracy. If the tighter tolerance components noted in the schematic are used, 0.1% accuracy is practical.

Summary

Figure 21's chart is an attempt to summarize the circuits presented, although such brevity breeds oversimplification. As such, although the chart reviews salient features, there is no substitute for a thorough investigation of any particular application's requirements.

FIGURE NUMBER	BIAS SUPPLY CAPABILITY	ANALOG OUTPUT CURRENT MONITOR (100nA to 1mA)	DIGITAL OUTPUT CURRENT MONITOR (100nA to 1mA)	COMMENTS
4	No	Yes	No	0.4% Accuracy. High Noise Rejection
5	No	Yes	Yes	0.5% Accuracy. Draws Current from APD Bias Supply Approximately Equalling Current Delivered to the APD in Addition to Housekeeping Current
6	Yes 30V to 90V	No	No	200μV Noise in 10MHz Bandwidth. 3% Accuracy
8	Yes 30V to 85V	Yes	No	3% Bias Voltage Accuracy. 0.5% Current Monitor Accuracy. Current Monitor Has 1kΩ Output Impedance
9	Yes 20V to 90V	Yes	No	0.25% Bias Voltage Accuracy. 1mV Output Noise in 10MHz Bandwidth. 0.25% Current Monitor Accuracy. Small Size. Few Large Value, High Voltage Capacitors Improves Reliability. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level
11	Yes 20V to 90V	No	No	2% Bias Voltage Accuracy. 1.5mV Output Noise in 10MHz Bandwidth. Small Size, Simple
13	Yes 20V to 90V	No	No	2% Bias Voltage Accuracy. 200μV Ripple and Noise in 100MHz Bandwidth. Relatively Large Solution Size Due to 250kHz Oscillator Frequency
15	Yes 20V to 90V	Yes	Yes	2% Bias Voltage Accuracy. 200μV Ripple and Noise in 100MHz Bandwidth. Current Monitor Accuracy Depends on Option Selected. Relatively Large Solution Size Due to 250kHz Oscillator Frequency
16	No	Yes	No	0.02% Accuracy. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level
18	No	No	Yes	0.09% Accuracy. 0.02% Achievable with Shunt Trimming. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level
19	No	No	Yes	0.25% Accuracy. Trimmable to 0.05% by Adjusting Reference
20	Yes 15V to 70V	No	Yes	2% Bias Voltage Accuracy. 2% Current Monitor Accuracy. 0.1% Accuracy Obtainable with Optional LT1460 Reference. Low Current Drain from APD Rail Permits Smaller High Voltage Capacitors for a Given Ripple Level

Figure 21. Summarized Characteristics of Techniques Presented. Applicable Circuit Depends on Application Specifics

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

Application Note 92

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APPENDIX A

LOW ERROR FEEDBACK SIGNAL DERIVATION TECHNIQUES

Various text circuits either detail or make reference to counteracting loading effects of the APD bias supply's output feedback divider. If the divider is located before the 1k Ω current shunt, its current drain is not included in the current monitor's output and no error is incurred. A potential difficulty with this approach is that the 1k Ω shunt appears in series with the bias supply output, degrading load regulation. The maximum 1mA shunt current produces a 1V output regulation drop. In some cases this is permissible and no further consideration is required. Circumstances dictating tighter load regulation require compensation techniques.

Divider Current Error Compensation—"Low Side" Shunt Case

When the shunt is in a transformer's return path ("low side shunt"), divider error is cancelled by introducing a compensatory term into the APD current monitor circuitry.

Figure A1 shows details. The output voltage divider's current loading error is prevented from appearing in A1's output by feeding forward a compensatory current from the APD bias programming input. This compensating current, arriving at A1 via R_{LARGE} , is scaled to precisely balance out the portion of shunt output contributed by the voltage divider's loading error.

Divider Current Error Compensation—"High Side" Shunt Case

Figure A2 addresses situations where the shunt resides in the "high side." Such arrangements involve high common mode voltages, seemingly mandating a high voltage buffer amplifier to isolate the divider's current loading. Figure A2 shows a way around this, using standard low voltage amplifiers to process high voltage signals. A1, sensing after the 1k Ω shunt, isolates the feedback divider's loading while permitting the APD bias regulator to include the shunt within its feedback loop. A1 is powered directly from the bias regulator's high voltage output but its V^- pin is

zener clamped with respect to its V^+ pin. Current sink Q1 maintains this bias over the wide range of possible APD regulator outputs. Although A1 processes high voltage signals, the voltage across it is held to safe levels. The 5.6V zener in the APD bias line ensures A1's inputs are always inside their common mode operating range. The 10M

resistor maintains adequate zener bias when APD currents are extremely low. A 51k resistor protects A1 from destructive high voltage if the APD bias output is shorted to ground. Similarly, the 100k resistor prevents high voltage from appearing on the 5V supply if Q1 fails.

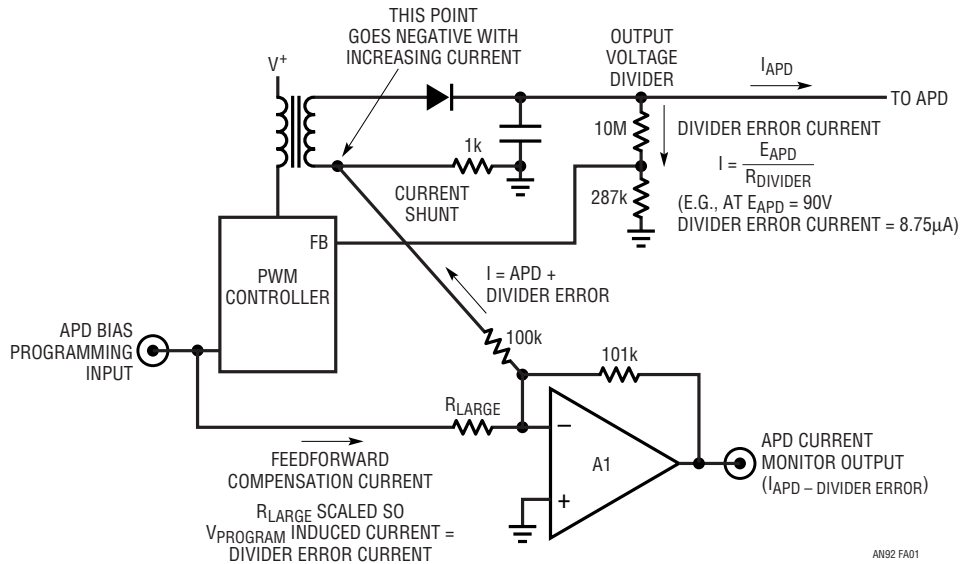


Figure A1. Output Voltage Divider Current Loading Error Is Compensated with Feedforward from Programming Input. A1 Algebraically Sums Feedforward Term and Current Shunt Information, Presents Corrected Output

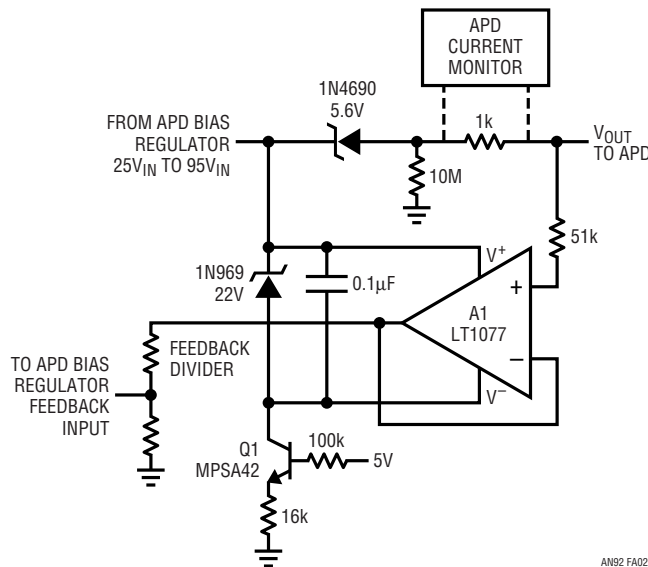


Figure A2. A1 Follower Floats from High Voltage Rail, Eliminates Feedback Divider Current Loading Error. Q1 Current Source and 22V Zener Maintain Low Voltage Across Amplifier; 5.6V Zener Accommodates A1's Input Range

APPENDIX B

PREAMPLIFIER AND OSCILLOSCOPE SELECTION

The low level measurements described require some form of preamplification for the oscilloscope. Current generation oscilloscopes rarely have greater than 2mV/DIV sensitivity, although older instruments offer more capability. Figure B1 lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These units feature wideband, low noise performance. It is particularly significant that many of these instruments are no longer produced. This is in keeping with current instrumentation trends, which emphasize digital signal acquisition as opposed to analog measurement capability.

The monitoring oscilloscope should have adequate bandwidth and exceptional trace clarity. In the latter regard high quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments is well-suited to low level noise measurement.¹ The digitizing uncertainties and raster scan limitations of DSOs impose display resolution penalties. Many DSO displays will not even register the small levels of switching-based noise.

INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	BANDWIDTH	MAXIMUM SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Amplifier	Hewlett-Packard	461A	150MHz	Gain = 100	Secondary Market	50Ω Input, Standalone
Differential Amplifier	Tektronix	1A5	50MHz	1mV/DIV	Secondary Market	Requires 500 Series Mainframe
Differential Amplifier	Tektronix	7A13	100MHz	1mV/DIV	Secondary Market	Requires 7000 Series Mainframe
Differential Amplifier	Tektronix	11A33	150MHz	1mV/DIV	Secondary Market	Requires 11000 Series Mainframe
Differential Amplifier	Tektronix	P6046	100MHz	1mV/DIV	Secondary Market	Standalone
Differential Amplifier	Preamble	1855	100MHz	Gain = 10	Current Production	Standalone, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 1000	Current Production	Standalone, Settable Bandstops

Figure B1. Some Applicable High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Bandwidth, Sensitivity and Availability

Note 1: In our work we have found Tektronix types 453, 453A, 454, 454A, 547 and 556 excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise floor limited background.

APPENDIX C

PROBING AND CONNECTION TECHNIQUES FOR LOW LEVEL, WIDEBAND SIGNAL INTEGRITY¹

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. The low level, wideband measurements demand care in routing signals to test instrumentation.

Ground Loops

Figure C1 shows the effects of a ground loop between pieces of line-powered test equipment. Small current flow between test equipment's nominally grounded chassis creates 60Hz modulation in the measured circuit output. *This problem can be avoided by grounding all line powered test equipment at the same outlet strip or otherwise ensuring that all chassis are at the same ground potential. Similarly, any test arrangement that permits circuit current flow in chassis interconnects must be avoided.*

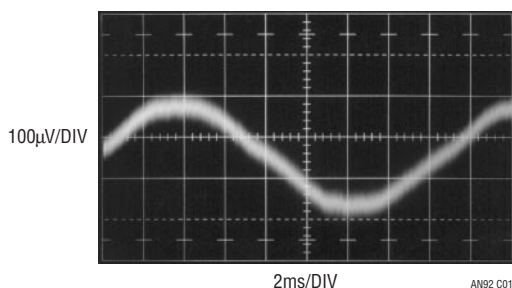


Figure C1. Ground Loop Between Pieces of Test Equipment Induces 60Hz Display Modulation

Pickup

Figure C2 also shows 60Hz modulation of the noise measurement. In this case, a 4-inch voltmeter probe at the feedback input is the culprit. *Minimize the number of test connections to the circuit and keep leads short.*

Poor Probing Technique

Figure C3's photograph shows a short ground strap affixed to a scope probe. The probe connects to a point which provides a trigger signal for the oscilloscope. Circuit output noise is monitored on the oscilloscope via the coaxial cable shown in the photo.

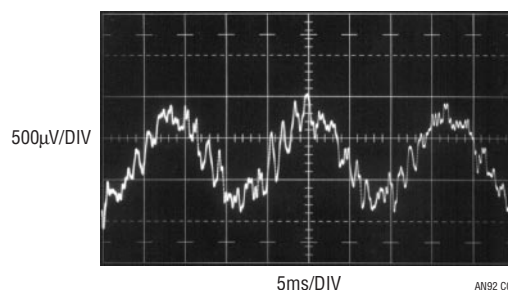


Figure C2. 60Hz Pickup Due to Excessive Probe Length at Feedback Node

Note 1: Veterans of LTC Application Notes, a hardened crew, will recognize this Appendix from AN70 (see Reference 2). Although that publication concerned considerably more wideband noise measurement, the material is directly applicable to this effort. As such, it is reproduced here for reader convenience.

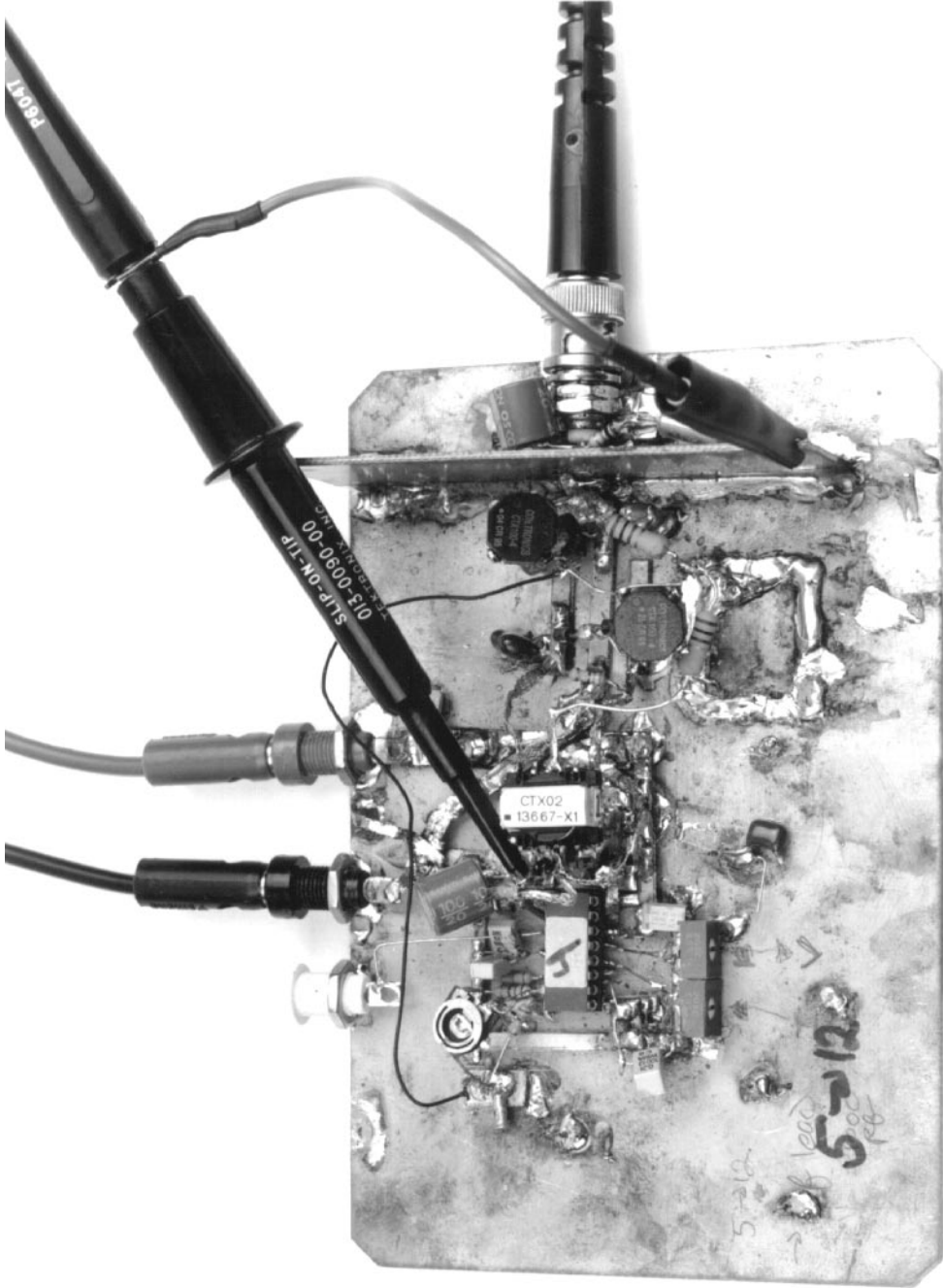


Figure C3. Poor Probing Technique. Trigger Probe Ground Lead Can Cause Ground Loop-Induced Artifacts to Appear in Display

Figure C4 shows results. A ground loop on the board between the probe ground strap and the ground referred cable shield causes apparent excessive ripple in the display. *Minimize the number of test connections to the circuit and avoid ground loops.*

Violating Coaxial Signal Transmission—Felony Case

In Figure C5, the coaxial cable used to transmit the circuit output noise to the amplifier-oscilloscope has been replaced with a probe. A short ground strap is employed as the probe's return. The error inducing trigger channel probe in the previous case has been eliminated; the 'scope is triggered by a noninvasive, isolated probe.² Figure C6 shows excessive display noise due to breakup of the coaxial signal environment. The probe's ground strap violates coaxial transmission and the signal is corrupted by RF. *Maintain coaxial connections in the noise signal monitoring path.*

Violating Coaxial Signal Transmission—Misdemeanor Case

Figure C7's probe connection also violates coaxial signal flow, but to a less offensive extent. The probe's ground strap is eliminated, replaced by a tip grounding attachment. Figure C8 shows better results over the preceding case, although signal corruption is still evident. *Maintain coaxial connections in the noise signal monitoring path.*

Proper Coaxial Connection Path

In Figure C9, a coaxial cable transmits the noise signal to the amplifier-oscilloscope combination. In theory, this affords the highest integrity cable signal transmission.

Figure C10's trace shows this to be true. The former example's aberrations and excessive noise have disappeared. The switching residuals are now faintly outlined in the amplifier noise floor. *Maintain coaxial connections in the noise signal monitoring path.*

Direct Connection Path

A good way to verify there are no cable-based errors is to eliminate the cable. Figure C11's approach eliminates all cable between breadboard, amplifier and oscilloscope. Figure C12's presentation is indistinguishable from Figure C10, indicating no cable-introduced infidelity. *When results seem optimal, design an experiment to test them. When results seem poor, design an experiment to test them. When results are as expected, design an experiment to test them. When results are unexpected, design an experiment to test them.*

Test Lead Connections

In theory, attaching a voltmeter lead to the regulator's output should not introduce noise. Figure C13's increased noise reading contradicts the theory. The regulator's output impedance, albeit low, is not zero, especially as frequency scales up. The RF noise injected by the test lead works against the finite output impedance, producing the 200 μ V of noise indicated in the figure. If a voltmeter lead must be connected to the output during testing, it should be done through a 10k Ω -10 μ F filter. Such a network eliminates Figure C13's problem while introducing minimal error in the monitoring DVM. *Minimize the number of test lead connections to the circuit while checking noise. Prevent test leads from injecting RF into the test circuit.*

Note 2: To be discussed. Read on.

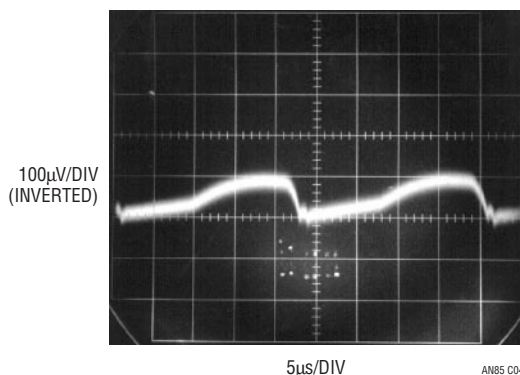


Figure C4. Apparent Excessive Ripple Results from Figure C3's Probe Misuse. Ground Loop on Board Introduces Serious Measurement Error

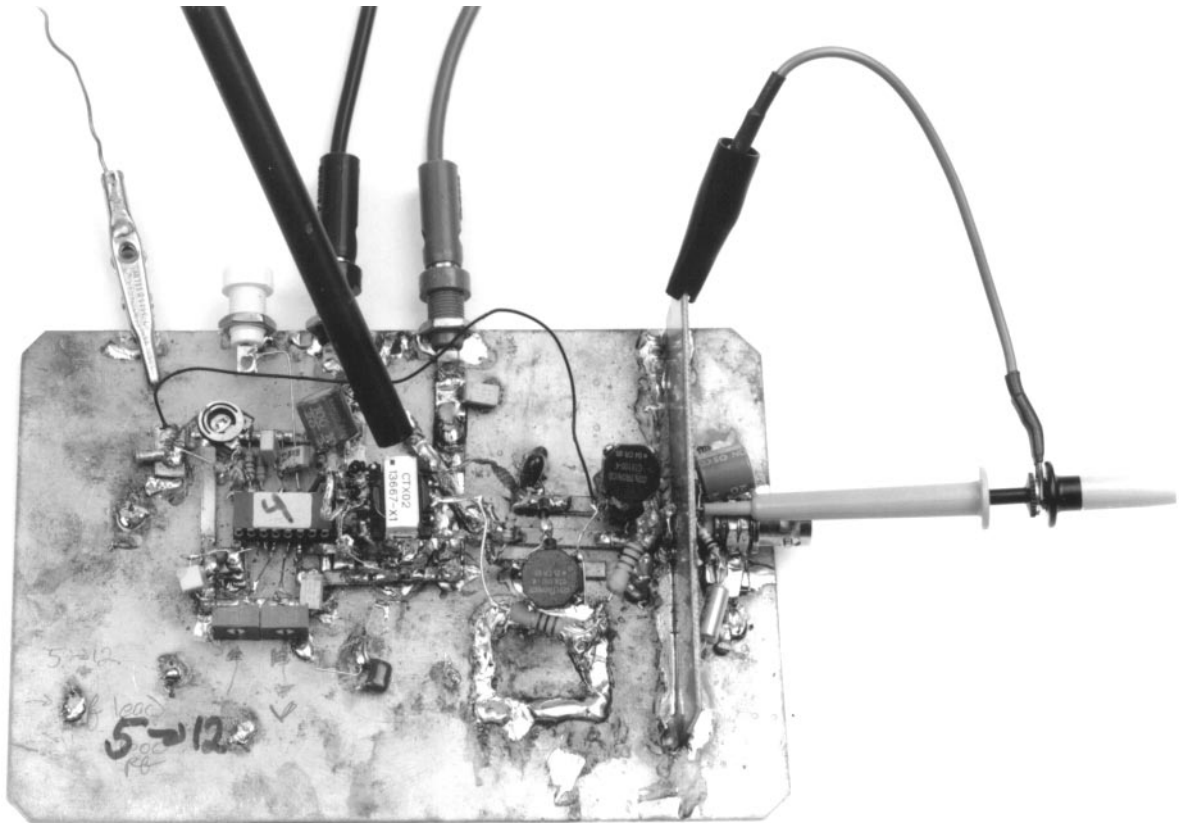


Figure C5. Floating Trigger Probe Eliminates Ground Loop, But Output Probe Ground Lead (Photo Upper Right) Violates Coaxial Signal Transmission

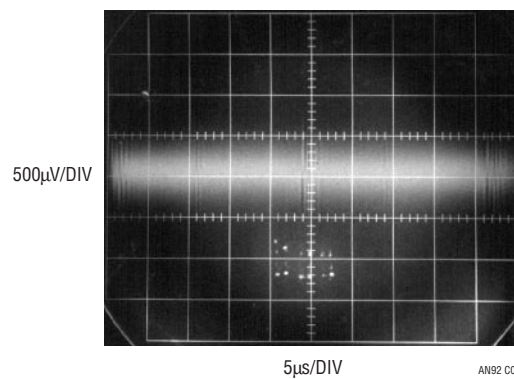


Figure C6. Signal Corruption Due to Figure C5's Noncoaxial Probe Connection

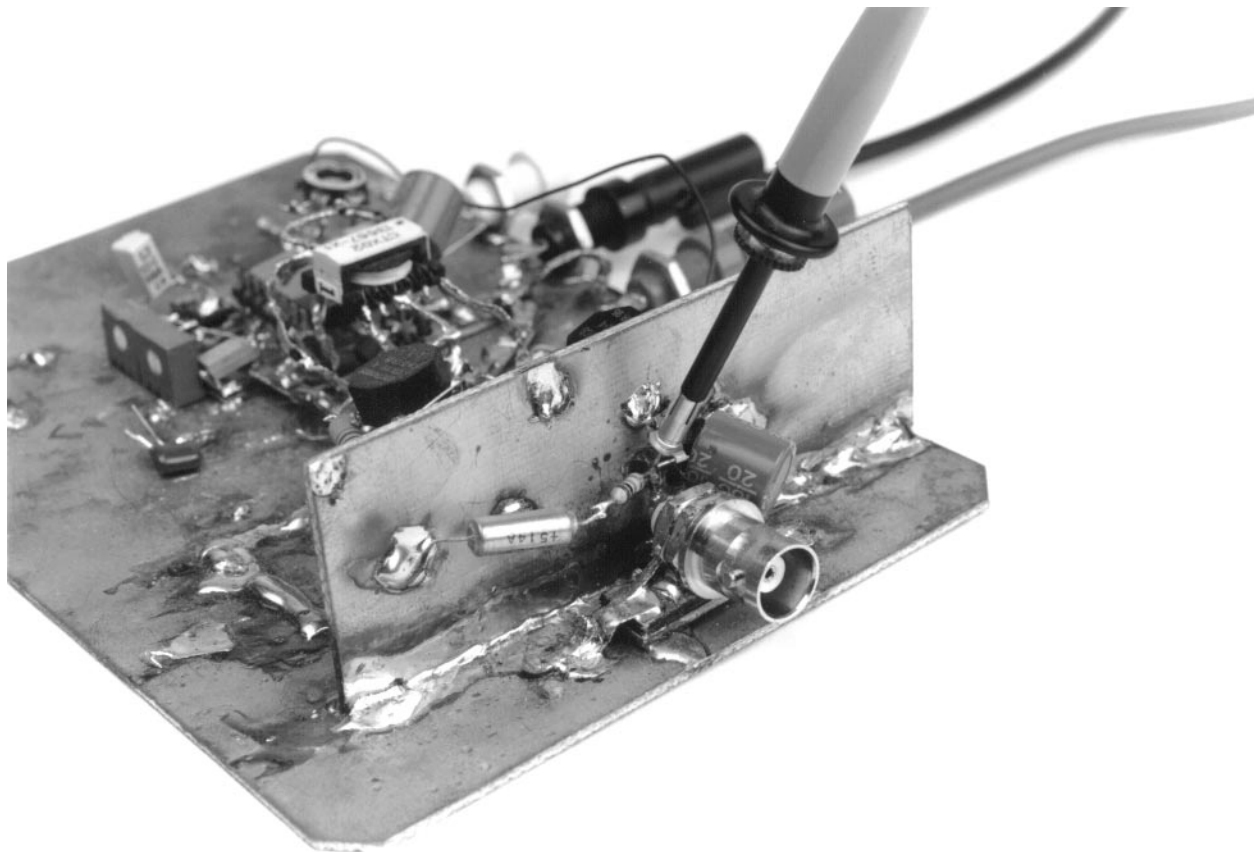


Figure C7. Probe with Tip Grounding Attachment Approximates Coaxial Connection

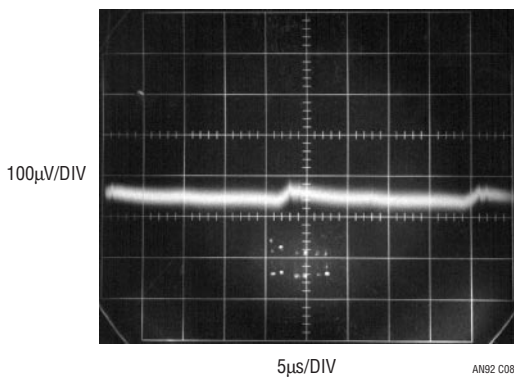


Figure C8. Probe with Tip Grounding Attachment Improves Results. Some Corruption Is Still Evident

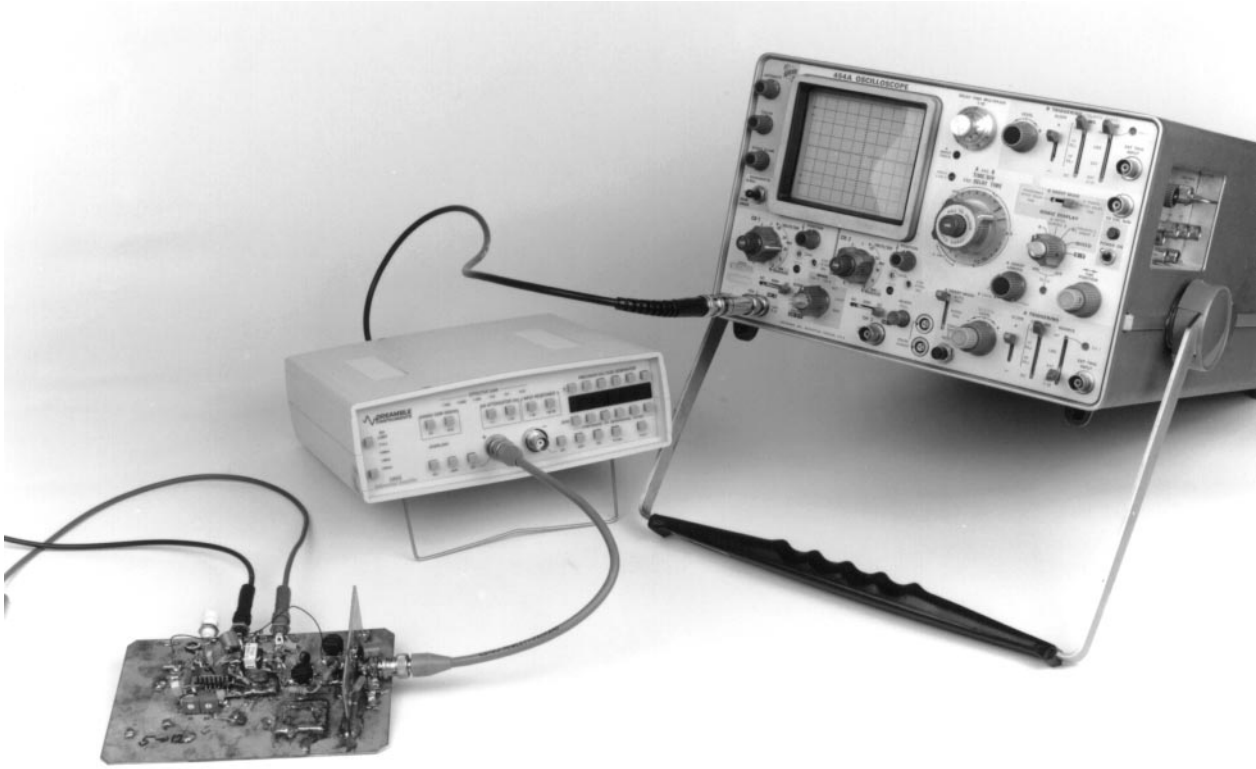


Figure C9. Coaxial Connection Theoretically Affords Highest Fidelity Signal Transmission

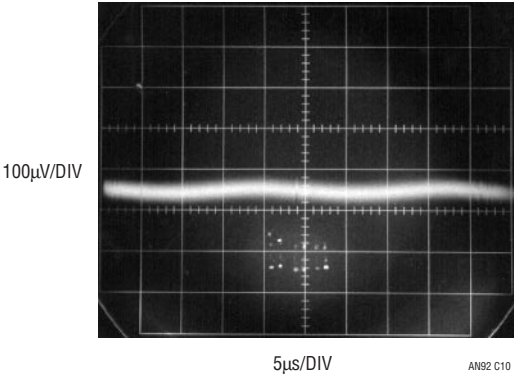


Figure C10. Life Agrees with Theory. Coaxial Signal Transmission Maintains Signal Integrity. Switching Residuals Are Faintly Outlined in Amplifier Noise

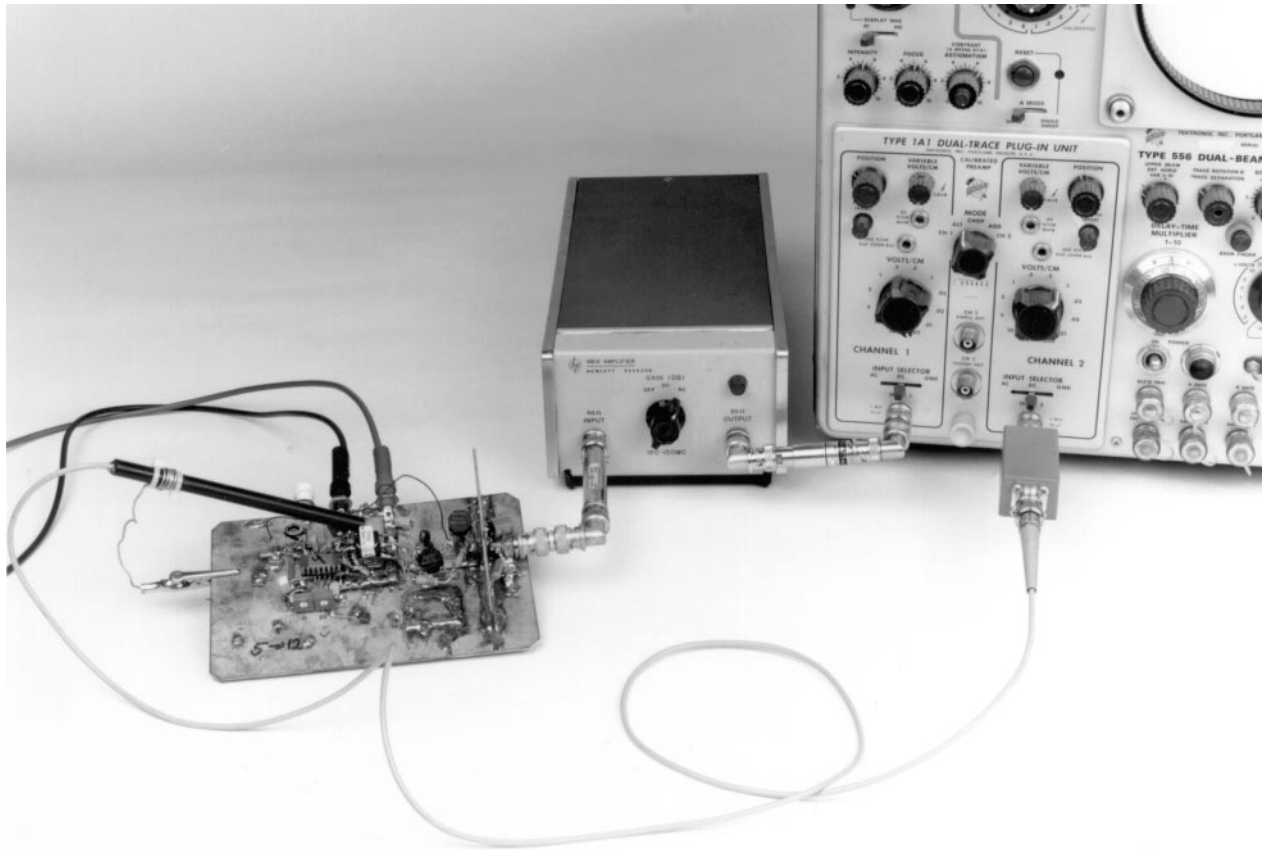


Figure C11. Direct Connection to Equipment Eliminates Possible Cable-Termination Parasitics, Providing Best Possible Signal Transmission

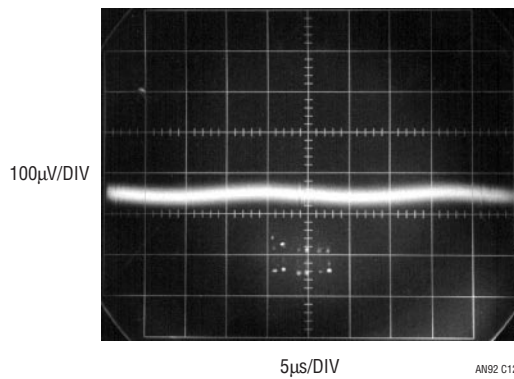


Figure C12. Direct Connection to Equipment Provides Identical Results to Cable-Termination Approach. Cable and Termination Are Therefore Acceptable

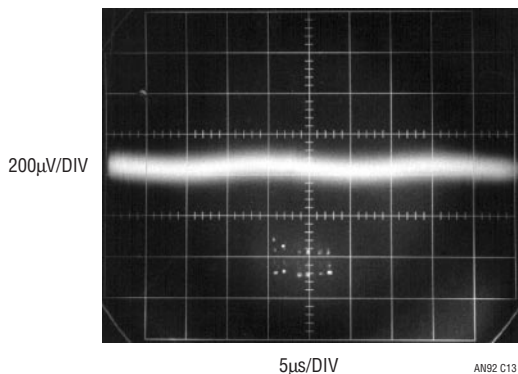


Figure C13. Voltmeter Lead Attached to Regulator Output Introduces RF Pickup, Multiplying Apparent Noise Floor

Isolated Trigger Probe

The text associated with Figure C5 somewhat cryptically alluded to an “isolated trigger probe.” Figure C14 reveals this to be simply an RF choke terminated against ringing. The choke picks up residual radiated field, generating an isolated trigger signal. This arrangement furnishes a scope trigger signal with essentially no measurement corruption. The probe’s physical form appears in Figure C15. For good results, the termination should be adjusted for minimum ringing while preserving the highest possible amplitude output. Light compensatory damping produces Figure C16’s output, which will cause poor scope triggering. Proper adjustment results in a more favorable output (Figure C17), characterized by minimal ringing and well-defined edges.

Trigger Probe Amplifier

The field around the switching magnetics is small and may not be adequate to reliably trigger some oscilloscopes. In such cases, Figure C18’s trigger probe amplifier is useful. It uses an adaptive triggering scheme to compensate for variations in probe output amplitude. A stable 5V trigger output is maintained over a 50:1 probe output range. A1, operating at a gain of 100, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2’s emitter capacitor, while the minimum excursion is retained in Q4’s

emitter capacitor. The DC value of the midpoint of A1’s output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal’s excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394’s positive input. The LT1394’s negative input is biased directly from A1’s output. The LT1394’s output, the circuit’s trigger output, is unaffected by >50:1 signal amplitude variations. An X100 analog output is available at A1.

Figure C19 shows the circuit’s digital output (Trace B) responding to the amplified probe signal at A1 (Trace A).

Figure C20 is a typical noise testing setup. It includes the breadboard, trigger probe, amplifier, oscilloscope and coaxial components.

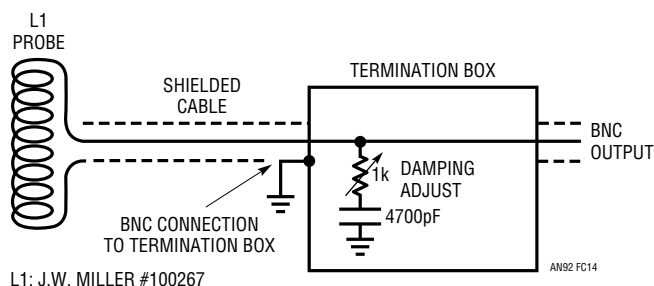


Figure C14. Simple Trigger Probe Eliminates Board Level Ground Loops. Termination Box Components Damp L1’s Ringing Response



Figure C15. The Trigger Probe and Termination Box. Clip Lead Facilitates Mounting Probe, Is Electrically Neutral

Application Note 92

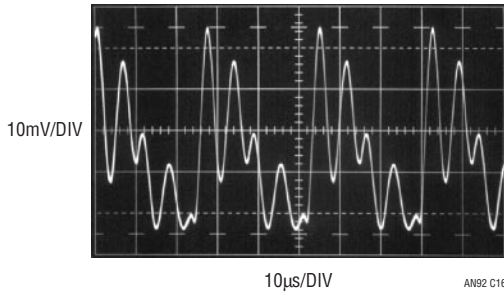


Figure C16. Misadjusted Termination Causes Inadequate Damping. Unstable Oscilloscope Triggering May Result

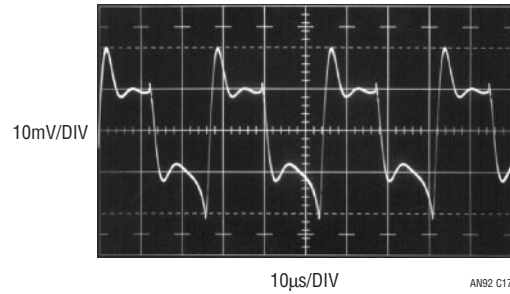


Figure C17. Properly Adjusted Termination Minimizes Ringing with Small Amplitude Penalty

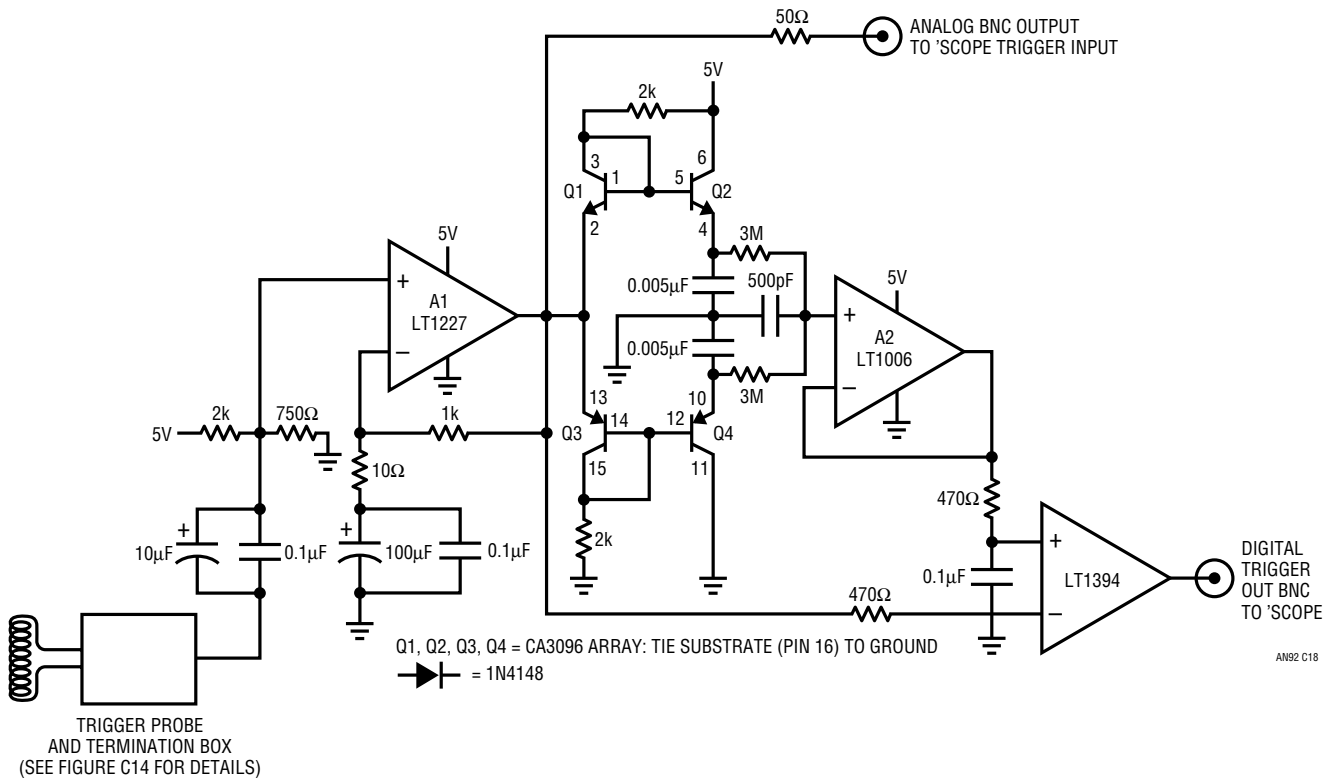


Figure C18. Trigger Probe Amplifier Has Analog and Digital Outputs. Adaptive Threshold Maintains Digital Output Over 50:1 Probe Signal Variations

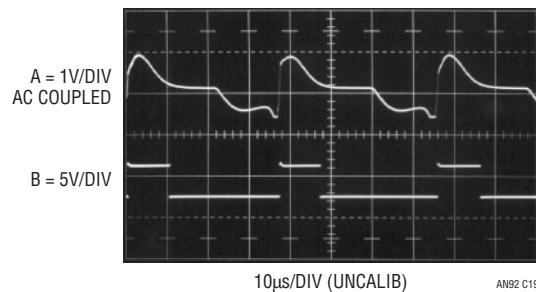


Figure C19. Trigger Probe Amplifier Analog (Trace A) and Digital (Trace B) Outputs

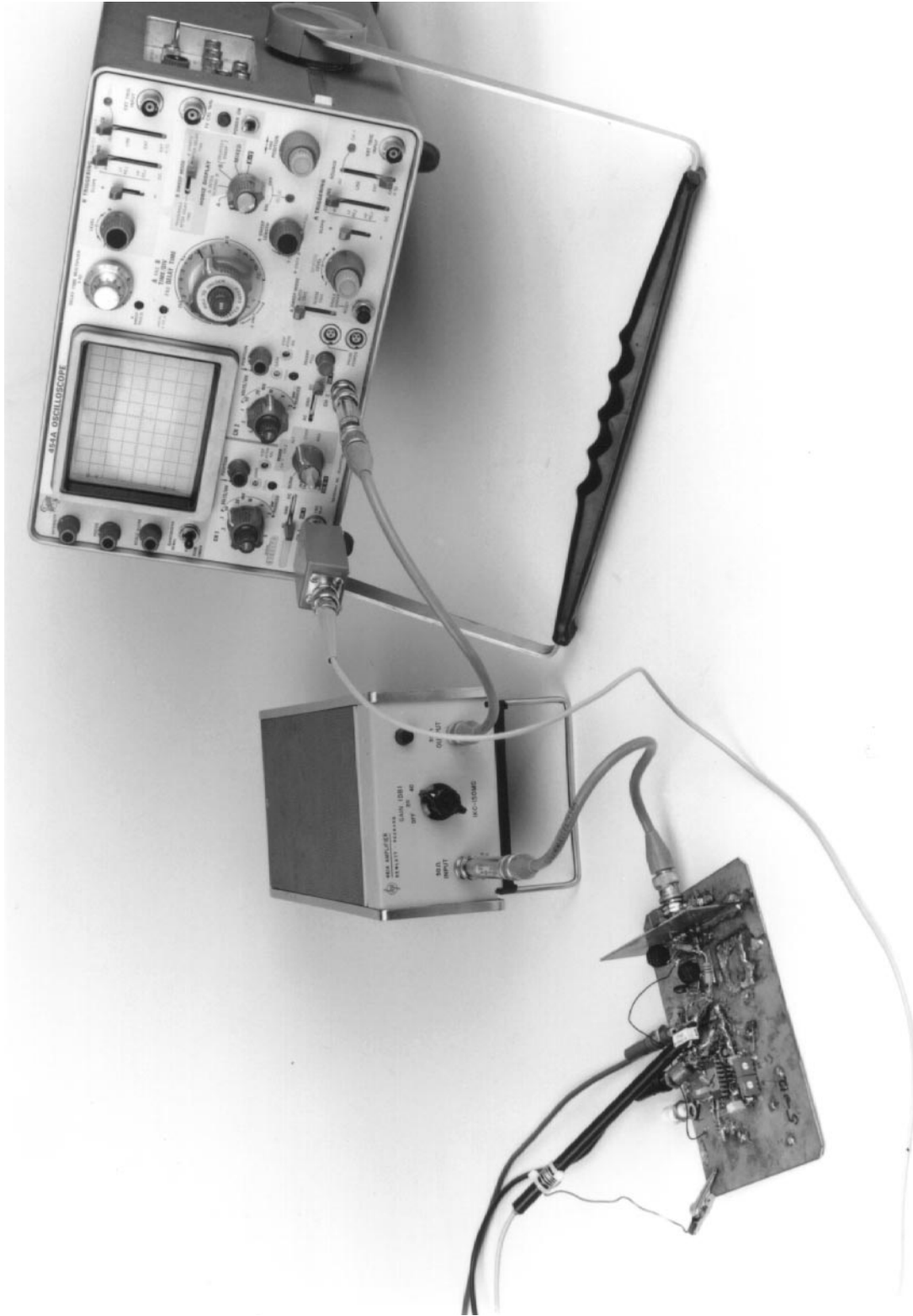


Figure C20. Typical Noise Test Setup Includes Trigger Probe, Amplifier, Oscilloscope and Coaxial Components

Application Note 92

APPENDIX D

A SINGLE RAIL AMPLIFIER WITH TRUE ZERO VOLT OUTPUT SWING

Performance requirements necessitate analog output current monitors to swing within $100\mu\text{V}$ of zero. This is difficult because the circuits run from a single, positive rail. No single rail amplifier can swing this close to zero while maintaining accurate outputs. Figure D1's power supply bootstrapping scheme achieves the desired characteristics with minimal component addition.

A1, a chopper stabilized amplifier, has a clock output. This output switches Q1, providing drive to the diode-capacitor charge pump. The charge pump output feeds A1's V^-

terminal, pulling it below zero, permitting output swing to (and below) ground. If desired, negative output excursion can be limited by either clamp option shown.

Reliable start-up of this bootstrapped power supply scheme is a valid concern, warranting investigation. In Figure D2, the amplifier's V^- pin (Trace C) initially rises at supply turn-on (Trace A) but heads negative when amplifier clocking (Trace B) commences at about midscreen.

The circuit provides a simple way to obtain output swing to zero volts, permitting a true "live at zero" output.

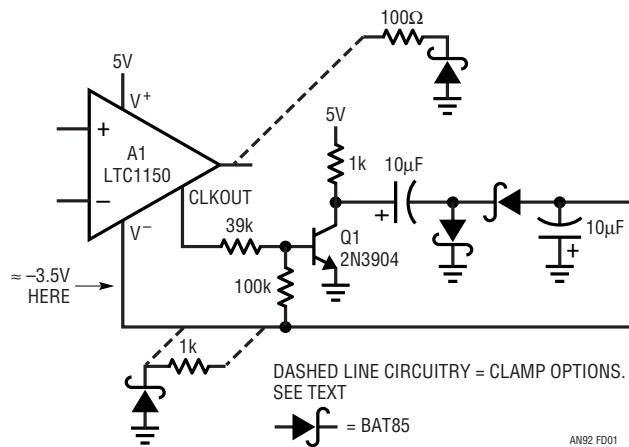


Figure D1. Single Rail Powered Amplifier Has True Zero Volt Output Swing. A1's Clock Output Switches Q1, Driving Diode-Capacitor Charge Pump. A1's V^- Pin Assumes Negative Voltage, Permitting Zero (and Below) Volt Output Swing

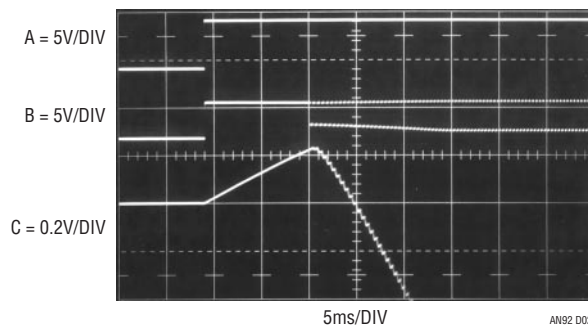


Figure D2. Amplifier Bootstrapped Supply Start-Up. Amplifier V^- Pin (Trace C) Initially Rises Positive at 5V Supply (Trace A) Turn-On. When Amplifier Internal Clock Starts (Trace B, 5th Vertical Division), Charge Pump Activates, Pulling V^- Pin Negative

APPENDIX E

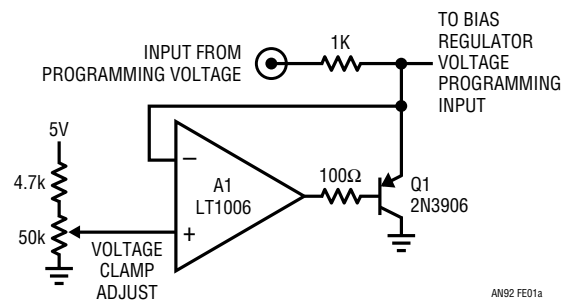
APD PROTECTION CIRCUITS

APD receiver modules are electrically delicate and expensive devices. Because of this, Figure E1's protection circuits may be of interest. They are designed to protect the APD module from bias programming overvoltage error (Figure E1a), excessive current (E1b) or destructive voltage (Figure E1c). In Figure E1a, Q1 is normally off and programming voltage passes to the bias regulator voltage programming input. Abnormally high inputs, defined by the potentiometer's setting, cause A1 to swing low, biasing Q1 and closing A1's feedback loop. This causes Q1's emitter to clamp at the potentiometer wiper's voltage, safely limiting the bias regulator's programming input.

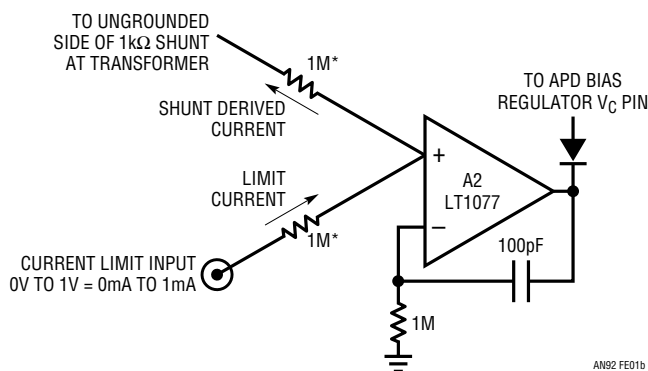
Figure E1b is an APD current limiter. This particular circuit is designed for use with "low side" shunts in transformer coupled APD supplies, such as text Figure 9, although the technique is generally applicable. As long as the shunt

current's absolute value is below the current limit point, A2 is saturated high and the associated APD bias regulator functions normally. Shunt overcurrent forces A2's output lower, pulling the regulator's control pin (V_C) lower and limiting current. The 100pF-1M Ω combination stabilizes A2 and the bias regulator assumes the characteristics of a current source.

Figure E1c is an overvoltage crowbar. It is intended as the last line of defense against uncontrolled APD bias supply high voltage outputs. Normally, the LTC1696 crowbar IC is below its 0.88V trigger threshold and the SCR is off. If the APD bias rises too high the LTC1696 triggers, firing the SCR. SCR turn-on "crowbars" the APD bias line, arresting the high voltage and maintaining a short across the line via its latch characteristic. If the APD bias supply has significant output impedance, prolonged SCR loading is not deleterious; if not, the bias supply should be fused.

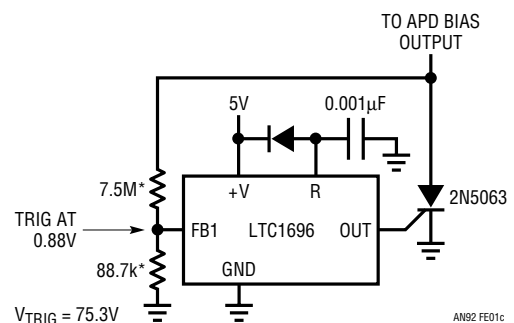


(E1a) Programming Voltage Clamp



(E1b) Current Limiter

* = 1% METAL FILM RESISTOR
 = 1N4148



(E1c) Bias Voltage Crowbar

Figure E1. Protection Circuits Prevent APD Destruction Due to Hardware or Software Failures. Options Include Programming Voltage Clamp (Figure E1a), Current Limiter (Figure E1b) and Bias Voltage Crowbar (Figure E1c)

Hey Jim, you've been working on APD circuits for an awfully long time.

But I need it NOW. We've got customers waiting.

Hi, Terry, I'm having trouble getting them to work.

Well, I don't have anything that works now. So, just go away & I'll call you when I'm ready.

Someday, when I don't have to make anything work, I'm gonna wear a tie too.

www.02

Instrumentation Applications for a Monolithic Oscillator

A Clock for All Reasons

Jim Williams

INTRODUCTION


Oscillators are fundamental circuit building blocks. A substantial percentage of electronic apparatus utilize oscillators, either as timekeeping references, clock sources, for excitation or other tasks. The most obvious oscillator application is a clock source in digital systems.¹ A second area is instrumentation. Transducer circuitry, carrier based amplifiers, sine wave formation, filters, interval generators and data converters all utilize different forms of oscillators. Although various techniques are common, a simply applied, broadly tunable oscillator with good accuracy has not been available.

Clock Types

Commonly employed oscillators are resonant element based or RC types.² Figure 1 shows two of each. Quartz crystals and ceramic resonators offer high initial accuracy and low drift (particularly quartz) but are essentially untunable over any significant range. Typical RC types have lower initial accuracy and increased drift but are easily tuned over broad ranges. A problem with conventional RC oscillators is that considerable design effort is required to achieve good specifications. A new device, the LTC1799, is also an RC type but fills the need for a simply applied, broadly tunable, accurate oscillator. Its accuracy and drift specifications fit between resonator based types and typical RC oscillators. Additionally, its board footprint, a 5-pin SOT-23 package and a single resistor, is notably small. Note that no external timing capacitor is required.

CLOCK TYPE	TYPICAL FREQUENCY ACCURACY	TYPICAL FREQUENCY RANGE	TUNABILITY	TEMPERATURE COEFFICIENT	POWER SUPPLY REJECTION RATIO	COMMENTS
Quartz	0.005%	10kHz to 200MHz	Poor	0.5ppm/°C Easily Achieved. See Comments	1ppm/V	High Stability and Initial Accuracy at Expense of Tunability. Essentially No Tunability. $1 \cdot 10^{-9}$ Stability Achievable with Compensation Techniques
Ceramic Resonator	0.5%	250kHz to 60MHz	Poor	30ppm/°C	20ppm/V	Lower Performance and cost than Quartz. Essentially Untunable
LTC1799	1.5%	1kHz to 33MHz	Good	40ppm/°C Plus Resistor Temperature Coefficient	500ppm/V	Add 10 to 50ppm/°C Temperature Coefficient, Depending on Resistor Type. Extremely Small Footprint— SOT-23 and 1 Resistor
Typical RC Based Clock	10%	1Hz to 25MHz	Good	200ppm/°C	2500ppm/V	Requires Careful Design and Component Selection for Best Results

Figure 1. LTC1799 Compared to Other Oscillators. Quartz and Ceramic Based Types Offer Higher Frequency Accuracy and Lower Drift but Lack Tunability. RC Designs are Tunable but Accuracy, Temperature Coefficient and PSRR are Poor

 LTC and LT are registered trademarks of Linear Technology Corporation.

Note 1: Strictly speaking, an oscillator (from the Latin verb, “*oscillo*,” to swing) produces sinusoids; a clock has rectangular or square wave output. The terms have come to be used interchangeably and this publication bends to that convention.

Note 2: This forum excludes such exotica as rubidium and cesium based atomic resonance devices, nor does it admit mundane but dated approaches such as tuning forks.

Application Note 93

A (Very) Simple, High Performance Oscillator

Figure 2 shows how simple to use the LTC1799 is. A single resistor (R_{SET}) programs the device's internal clock and pin-settable decade dividers scale output frequency. Various combinations of resistor value and divider choice permit outputs from 1kHz to 33MHz.³ Figure 3 shows R_{SET} vs output frequency for the three divider pin states and the governing equation. The inverse relationship between resistance and frequency means that LTC1799 *period* vs resistance is linear.

Figure 4 reveals that the LTC1799 has speciated into a family. At present, there are two additional devices. The LTC6900, quite similar, cuts supply current to 500 μ A but gives up some frequency range. The LTC6902, designed for noise smoothed, multiphase power applications, has multiphase outputs and spread spectrum capability. Spread spectrum clocking distributes power switching over a settable frequency range, preventing significant noise peaking at any given point. This greatly reduces EMI concerns.

The LTC1799's combination of simplicity, broad tunability and good accuracy invites use in instrumentation cir-

cuitry. The following text utilizes the device's attributes in a variety of such applications.

Platinum RTD Digitizer

A platinum RTD, used for R_{SET} in Figure 5, results in a highly predictable O1 output period vs temperature. O1's output, scaled via counters, is presented to a clocked, period determining logic network which delivers digital output data. Over a 0°C to 100°C sensed temperature, 1000 counts are delivered, with accuracy inside 1°C. Extended range (sensor limits are -50°C to 400°C) is possible by using a monitoring processor to implement linearity correction in accordance with sensor characteristics.⁴

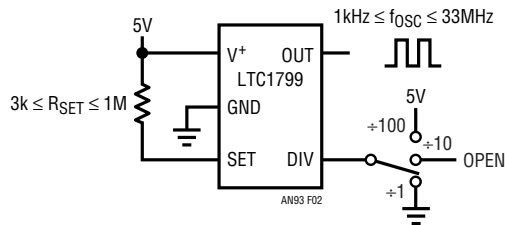


Figure 2. LTC1799 Oscillator Frequency Is Determined by R_{SET} and Divider Pin (DIV). Tunable Range Spans 1kHz to 33MHz

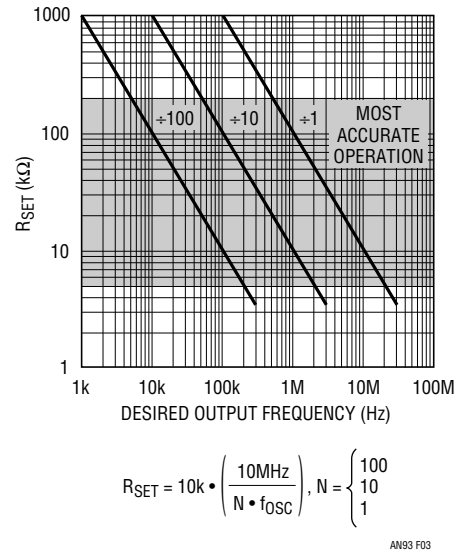


Figure 3. R_{SET} vs Output Frequency for the Three Divider Pin States and Governing Equation. Relationship between R_{SET} and Frequency Is Inverse; R_{SET} vs Period has Linear Characteristic

DEVICE TYPE	FREQUENCY RANGE	FREQUENCY ACCURACY	TEMPERATURE COEFFICIENT	PSRR	COMMENTS
LTC1799	1kHz to 33MHz	1.5%	40ppm/°C + Resistor Drift	0.05%/V	$I_{SUPPLY} = 1mA$
LTC6900	1kHz to 20MHz	1.5%	40ppm/°C + Resistor Drift	0.04%/V	Low Power ($I_{SUPPLY} = 500\mu A$) Version of LTC1799
LTC6902	5kHz to 20MHz	1.5%	40ppm/°C + Resistor Drift	0.04%/V	2-, 3- or 4-Phase Outputs. Programmable Width Spread Spectrum Frequency Modulation. Intended for Multiphase Power Supply Applications

Figure 4. Oscillator Family Details. LTC6900 Is Low Power Version of LTC1799. LTC6902, Intended for Noise Sensitive, High Power Switching Regulator Applications, Has Multiphase, Spread Spectrum Outputs. All Types Have Excellent Tunability, Good Frequency Accuracy, Low Temperature Coefficient and High PSRR

Note 3: This deceptively simple operation derives from noteworthy internal cleverness. See Appendix A, "LTC1799 Internal Operation" for a description.

Note 4: Linearity deviation over -50°C to 400°C is several degrees. See Reference 1.

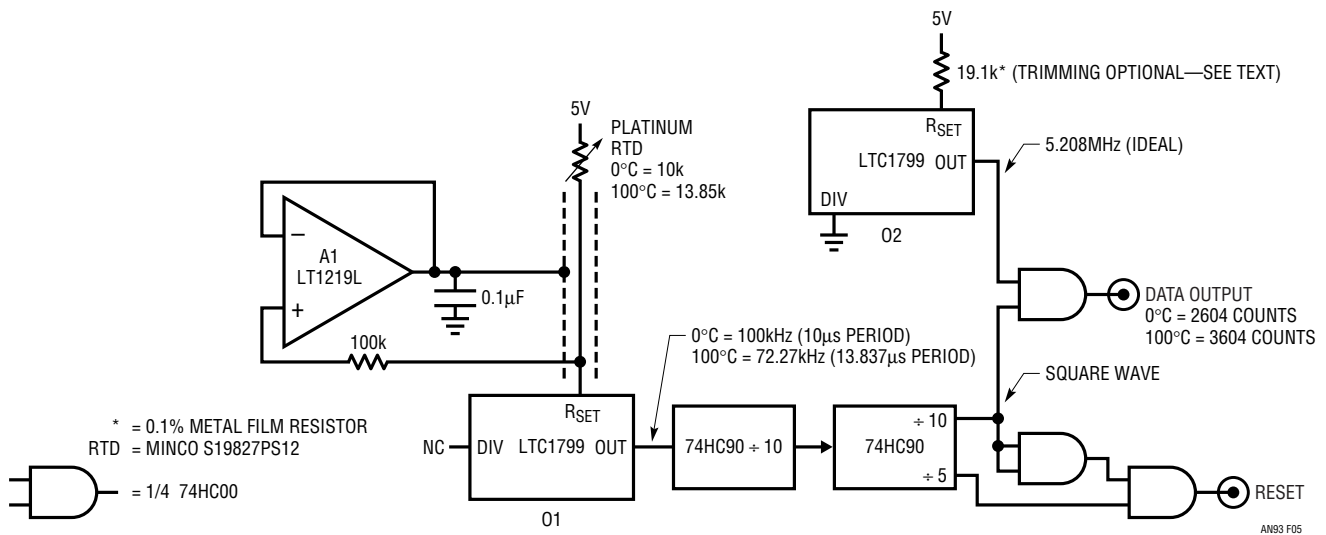


Figure 5. Platinum RTD Digitizer Accurate within 1° Over 0°C to 100°C. Platinum RTD Value Is Linearly Converted to Period by LTC1799. Logic and Second LTC1799 Clock Digitize Period into Output Data Bursts. A1 Drives RTD Shield at R_{SET} Potential, Bootstrapping Pin Capacitance to Permit Remotely Located Sensor

If the RTD is at the end of a cable, the cable shield should be driven by A1 as shown. This bootstraps the cable shield to the same potential as R_{SET}, eliminating jitter inducing capacitive loading effects at the R_{SET} node.⁵

Figure 6 shows operating waveforms. The RTD determines O1's output (Trace A), which is divided by 100 and assumes square wave form (Trace B). The logic network combines with O2's fixed frequency to digitize period measurement, which appears as output data bursts (Trace C). The logic also produces a reset output (Trace D), facilitating synchronization of monitoring logic.

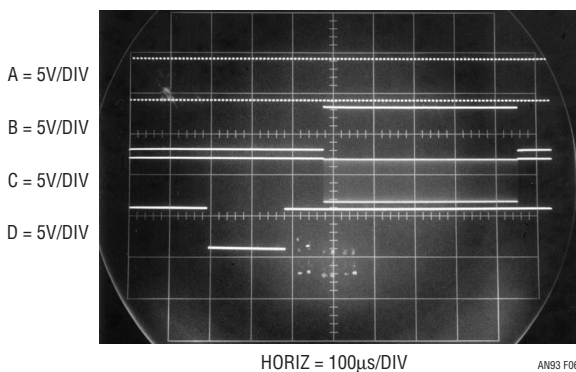


Figure 6. Platinum RTD Biased LTC1799 Produces Output (Trace A) which Is Divided by 100 (Trace B) and Gated with 5.2MHz Clock. Resultant Data Bursts (Trace C) Correspond to Temperature. Reset Pulse (Trace D), Preceding Each Data Burst, Permits Synchronization of Monitoring Logic

As shown, accuracy is about 1.5°C, primarily due to LTC1799 initial error. Obtaining accuracy inside 1°C involves simulating a 100°C temperature (13,850Ω) at the sensor terminals and trimming R_{SET} for appropriate output. A precision resistor decade box (e.g., ESI DB62) allows convenient calibration.

Thermistor-to-Frequency Converter

Figure 7's circuit also directly converts temperature to digital data. In this case, a thermistor sensor biases the R_{SET} pin. The LTC1799 frequency output is predictable, although nonlinear. The inverse R_{SET} vs frequency relationship combines with the thermistor's nonlinear characteristic to give Figure 8's data. The curve is nonlinear, although tightly controlled.

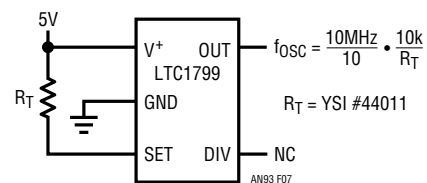


Figure 7. Simple Temperature-to-Frequency Converter Biases R_{SET} with Thermistor. Frequency Output Is Predictable, Although Nonlinear

Note 5: The R_{SET} node, while not unduly sensitive, requires management of stray capacitance. See Appendix B, "R_{SET} Node Considerations" for detail.

Application Note 93

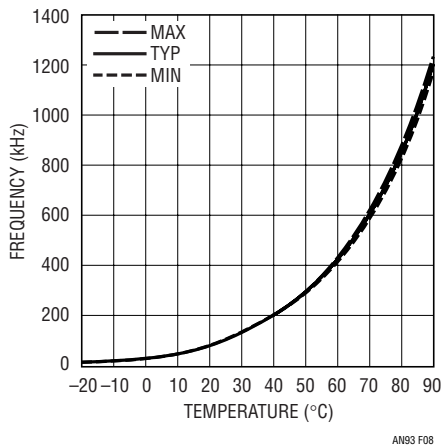


Figure 8. LTC1799 Inverse Resistance vs Frequency Relationship and Nonlinear Thermistor Characteristic Result in above Data. Curve Is Nonlinear, Although Tightly Controlled

Isolated, 3500V Breakdown, Thermistor-to-Frequency Converter

This circuit, building on the previous approach, galvanically isolates the thermistor from the circuit's power and data output ports. The 3500V breakdown barrier between the thermistor and power/data output ports permits operation at high common mode voltages. Such conditions are often encountered in industrial measurement situations.

Figure 9's pulse generator, C1, running around 10kHz, produces a 2.5 μ s wide output (Trace A, Figure 10). Q1-Q2 provide power gain, driving T1 (Trace B is Q2's collector). T1's secondary responds, charging the 100 μ F capacitor to a DC level via the 1N5817 rectifier. The capacitor powers O1, which oscillates at the sensor determined frequency. O1's output, differentiated to conserve power, switches Q4. Q4, in turn, drives T1's secondary, T1's primary receives Q4's signal and Q3 amplifies it, producing the circuit's data output (Trace C). Q3's collector also lightly

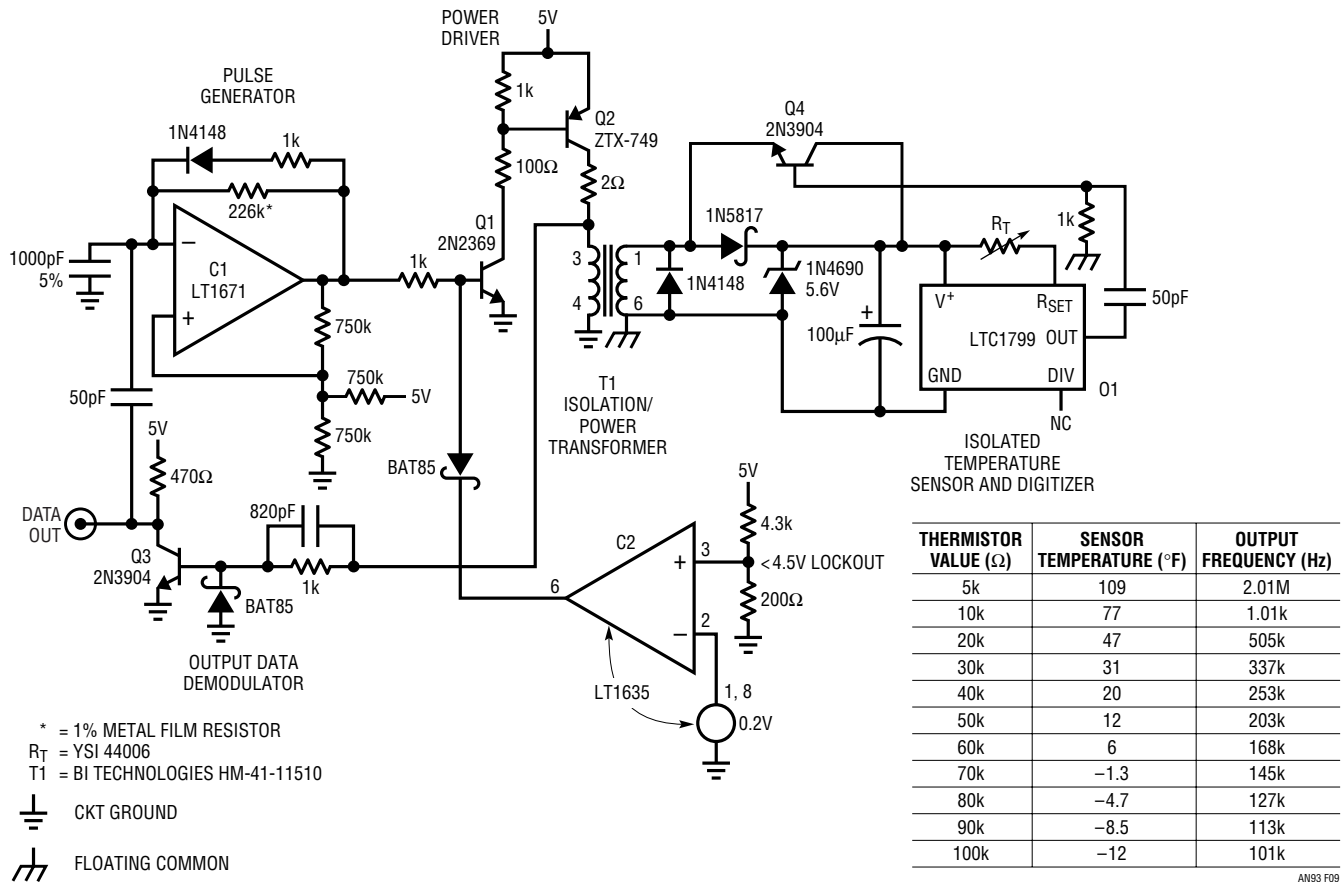


Figure 9. A Galvanically Isolated Thermistor Digitizer. C1 Sources Pulsed Power to Thermistor Biased LTC1799 via Q1, Q2 and T1. LTC1799 Output Modulates T1 through Q4. Q3 Extracts Data, Presents Ouput. T1's 3500V Breakdown Sets Isolation Limit

modulates C1's negative input (Trace D), synchronizing T1's primary drive to the data output. C2 prevents erratic circuit operation below 4.5V by removing Q1's drive.

C1's continuous clocking, while maintaining O1's isolated DC power supply, generates periodic cessations in the frequency coded output. These interruptions can be used as markers to control operation of monitoring logic. Output frequency vs thermistor characteristics are included in Figure 9.

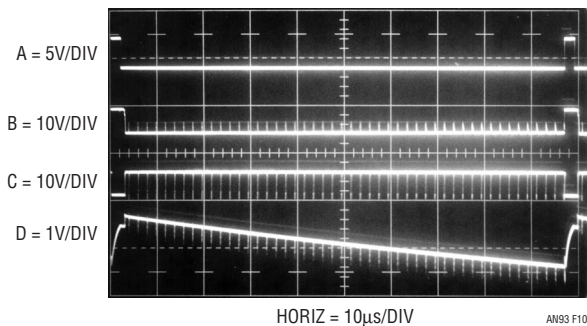


Figure 10. Isolated Thermistor Digitizer's Waveforms Include C1's Output (Trace A), Q2's Collector Drive to T1 (Trace B), Data Output (Trace C) and C1's Negative Input (Trace D). C1's Negative Input (Trace D) Is Lightly Modulated by Q3, Synchronizing Transformer Power Drive to Data Output

Relative Humidity Sensor Digitizer-Hetrodyne Based

Figure 11 converts the varying capacitance of a linearly responding relative humidity sensor to a frequency output. The 0Hz to 1kHz output corresponds to 0% to 100% sensed relative humidity (RH). Circuit accuracy is 2%, plus an additional tolerance dictated by the selected sensor grade. Circuit temperature coefficient is $\approx 400\text{ppm}/^\circ\text{C}$ and power supply rejection ratio is $<1\%$ over 4.5V to 5.5V. Additionally, one sensor terminal is grounded, often beneficial for noise rejection.

This is basically a hetrodyne circuit. Two oscillators, one variable, one fixed, are mixed, producing sum and difference frequencies. The variable oscillator is controlled by the capacitive humidity sensor. The demodulated difference frequency is the output.⁶ The hetrodyne frequency subtraction approach permits a sensed 0% RH to give a 0Hz output, even though sensor capacitance is not zero at RH = 0%.

C1, the sensor controlled variable oscillator, runs between the indicated output frequencies for the RH sensor excursion noted. The RH sensor is AC coupled, in accordance with its manufacturer's data sheet.⁷ Reference oscillator O1 is tuned to C1's nominal 25% RH dictated frequency.

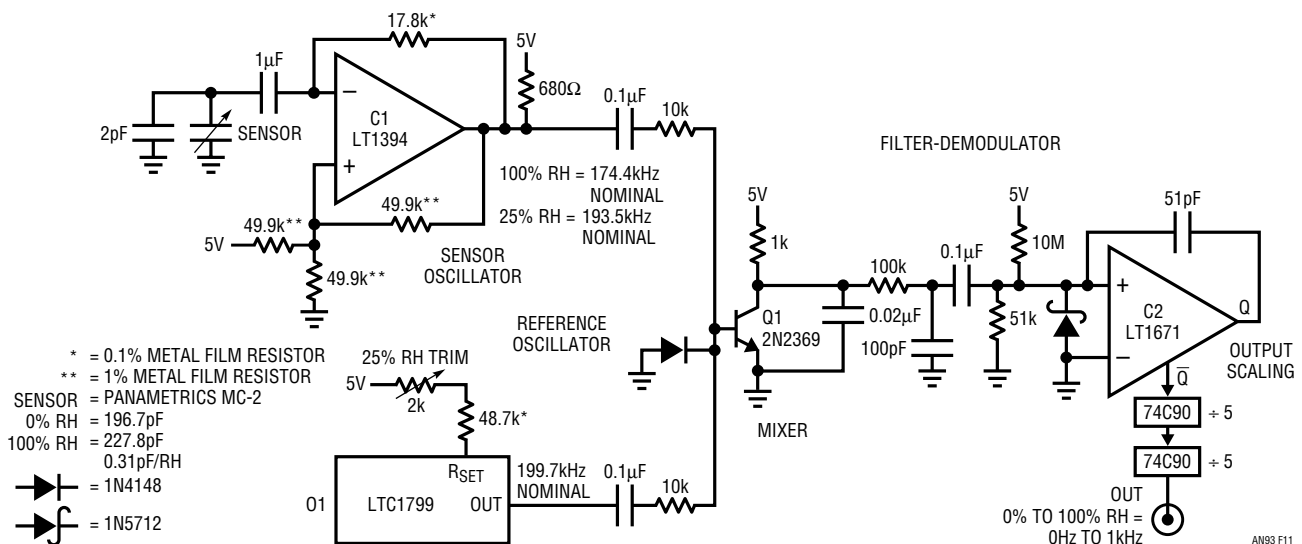


Figure 11. Hetrodyne Based Humidity Transducer Digitizer Has Grounded Sensor, 2% Accuracy. Capacitively Sensed Hygrometer Beats Humidity Dependent Oscillator (C1) Against Stable Oscillator O1. Difference Frequency Is Demodulated by Q1, Converted to Pulse Form at C2. Counters Scale Output for 0kHz to 1kHz = 0% to 100% Relative Humidity

Note 6: Hetrodyne techniques, usually associated with communications circuitry, have previously been applied to instrumentation. This circuit's operation was adapted from approaches described in References 2, 3 and 4.

Note 7: DC coupling introduces destructive electromigration effects. See Reference 6.

Application Note 93

The two oscillators are mixed at Q1's base (Figure 12, Trace A). Q1 amplifies the mixed frequency components, although collector filtering attenuates the sum frequency. The RH determined difference frequency, appearing as a sine wave at Q1's collector (Trace B), remains. This waveform is filtered and AC coupled to zero crossing detector C2. AC hysteretic feedback at C2's input (Trace C) produces clean C2 output (Trace D). Counter based scaling at C2's output combines with slight sensor padding (note 2pF value across the sensor) to provide numeric output frequency correspondence to RH. Calibration involves simulating the RH sensor's 25% value and trimming O1 for a 250Hz output. The simulated value may be built up from known discrete capacitors or simply dialed out on a precision variable air capacitor (General Radio 1422D).

When evaluating circuit operation, it is useful to consider that C1's frequency changes inversely with sensor capacitance; its *period* is linear vs sensor capacitance. This would normally corrupt the desired linear output relationship between frequency and RH. Practically, because the sensor's excursion range is small compared to its 0% RH value, the error is similarly small. This term almost entirely accounts for the circuit's stated 2% accuracy.

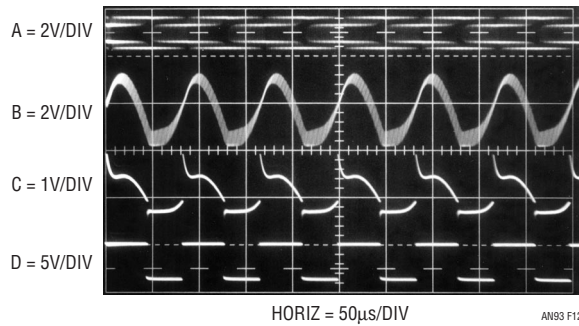


Figure 12. Sensor and Stable Oscillators are Mixed at Q1's Base (Trace A); Difference Frequency Appears at Q1's Collector (Trace B). Filtering and AC Hysteresis at C2's + Input (Trace C) Produce Clean Response at C2's Output (Trace D)

Relative Humidity Sensor Digitizer-Charge Pump Based

Figure 13 also digitizes the capacitive humidity sensor's output but has better specifications than the previous circuit. Circuit accuracy is 0.3%, plus the selected sensor grade's tolerance. Temperature coefficient is about 300ppm/°C and power supply rejection ratio is 0.25% for 5V ±0.5V. Compromises include a floating sensor and somewhat more complex circuitry.

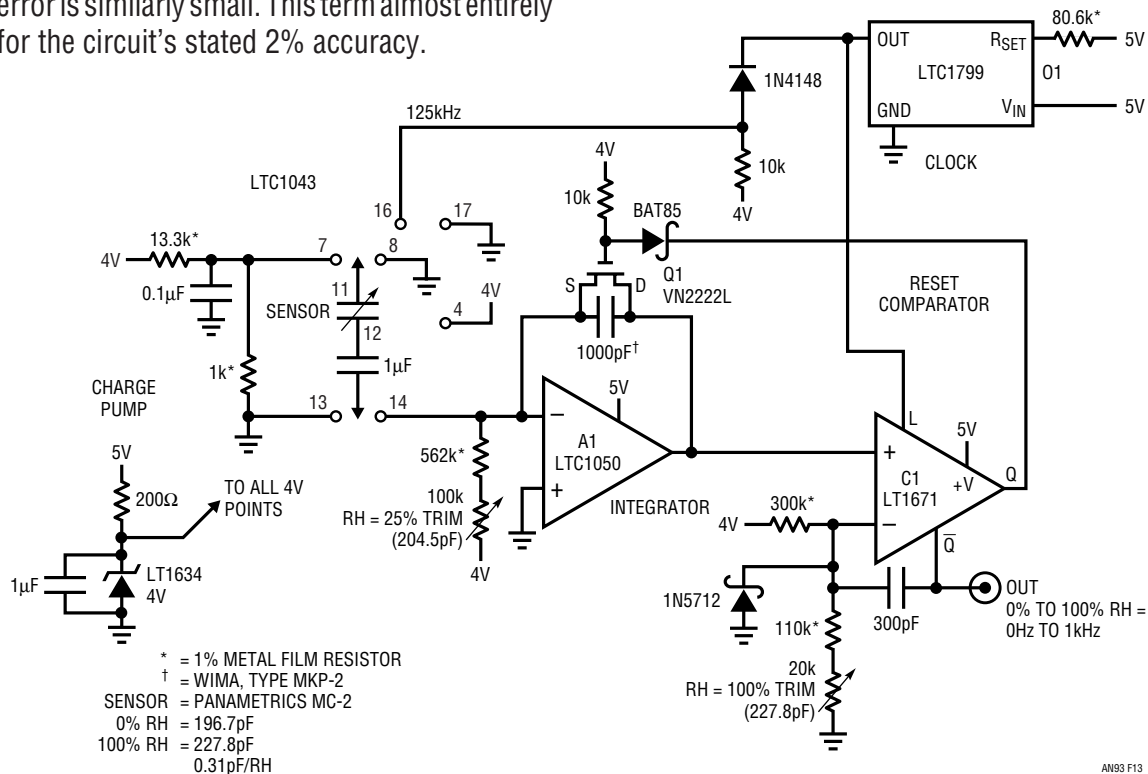


Figure 13. Hygrometer Digitizer Has 0.3% Accuracy, Although Sensor Must Float Off-Ground. Humidity Sensor Determines Charge Delivered to A1 Integrator During Each Charge Pump Cycle. Resultant A1 Output Ramp Is Reset by Level Triggered C1 via Q1. Output Frequency, Taken at C1, Varies with Humidity

O1 (Trace A, Figure 14) clocks an LTC1043 switch array based charge pump. This configuration alternately connects the AC coupled RH sensor to a 4V reference derived potential and then discharges it into A1's summing point. A1, an integrator, responds with a ramping output, Trace B of Figure 14. When A1's output exceeds C1's negative input voltage, C1's Q output (Trace C, Figure 14) goes high, triggering Q1 and resetting the ramp. AC feedback to C1's negative input (Trace D) ensures long enough Q1 on-time for complete ramp reset. This action's repetition rate depends on RH sensor value. The A1-C1 loop is synchronized to the charge pump's clocking by O1's output path to C1's latch input. In theory, if the charge pump, offset term (25% trim current) and ramp amplitude are tied to the same potential, this circuit does not require a voltage reference. In practice, the sensor's extremely small capacitance shifts magnify the effect of charge pump errors vs supply, necessitating powering the LTC1043 from the 4V reference. Once this is done, the mentioned points are tied to the 4V reference. Note that the 5V powered O1's output must be level shifted to drive the LTC1043.

A trimmed DC offset current (100k potentiometer) into A1's summing junction compensates the RH sensor's offset term (e.g., 0% RH \neq 0pF). Output frequency is scaled by the 20k Ω trim at C1 so 0% to 100% RH = 0Hz to 1kHz. Trimming involves substituting capacitance for the sensor's known 100% and 25% values and trimming the appropriate adjustments. The adjustments are somewhat interactive, necessitating repetition until convergence occurs. A precision variable capacitor (General

Radio type 1422D) is invaluable in this regard, although acceptable results are possible with built-up calibrated discrete capacitors.

Relative Humidity Sensor Digitizer-Time Domain Bridge Based

Figure 15, also a relative humidity (RH) digitizer, features 1% accuracy, PSRR of 1% over 4.5V to 5.5V, temperature coefficient of 350ppm/ $^{\circ}$ C and a ground referred sensor. Additionally, the circuit's trim scheme accommodates wide tolerance grade RH sensors. The circuit is basically a time domain bridge; it subtracts time intervals representing sensor and sensor offset values to determine sensor value extrapolated to RH = 0%. This measurement is digitized and scaled so zero to 100 counts equals 0% to 100% RH at the output.

O1's nominal 12.77MHz output, conditioned by a counter chain and an inverter configured gate, presents a 12.4kHz, 2.5 μ s pulse (Trace A, Figure 16) to Q1A and Q1B. The transistors' collectors fall (Trace B = Q1A collector – Trace C = Q1B collector) to zero volts. When the base drive ceases, both collectors ramp towards 5V. Trace B's ramp slope varies with the RH sensor's capacitance; Trace C's ramp slope represents the sensor's offset value (0% RH \neq 0pF). C1 and C2 switch when their associated ramp inputs cross the comparators' common DC input potential. The comparator outputs (Trace D = C2, Trace E = C1) define a "both high" time region proportional to the ramp slopes' difference and, hence, an offset corrected version of sensor value. This time interval is gated with O1's output, providing Trace F's data output.

Circuit operation is fairly straightforward, although some details bear mention. Q1, a dual transistor, promotes cancellation of the individual transistors' V_{CE} vs temperature terms, minimizing their error contribution. The unit specified, a 2-die type, minimizes crosstalk; monolithic types should not be substituted. Similarly, a dual comparator should not be substituted for the single types specified for C1 and C2. Also, the comparators operate at high source impedance relative to their input characteristics but symmetry provides adequate error cancellation. Finally, the 5.6k resistor combines with the output gates' input capacitance, forming a \approx 20ns lag. This delay prevents false output data transients when the ramps are resetting.

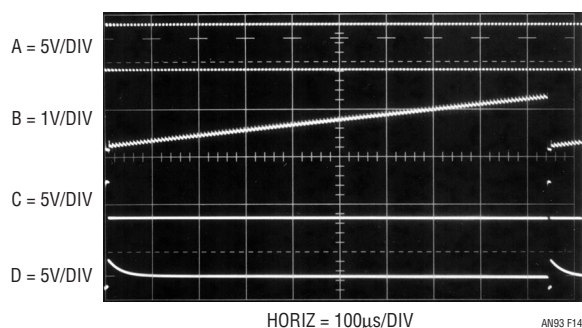


Figure 14. LTC1799 Clock (Trace A) Drives Humidity Sensor Based Charge Pump, Producing A1 Output Ramp (Trace B). C1 Q Output, Trace C, Biases Q1, Resetting Ramp. AC Feedback at C1 (Trace D) Permits Complete Ramp Reset, Sets Output Pulse Width

Application Note 93

Trimming procedure is similar to the previous RH circuit. It involves substituting capacitance for the sensor's known 100% and 25% values and trimming the indicated adjustments. The adjustments are somewhat interactive, neces-

sitating repetition until convergence occurs. A precision variable capacitor (General Radio type 1422D) is invaluable for this work, although acceptable results are possible with calibrated discrete capacitor assemblies.

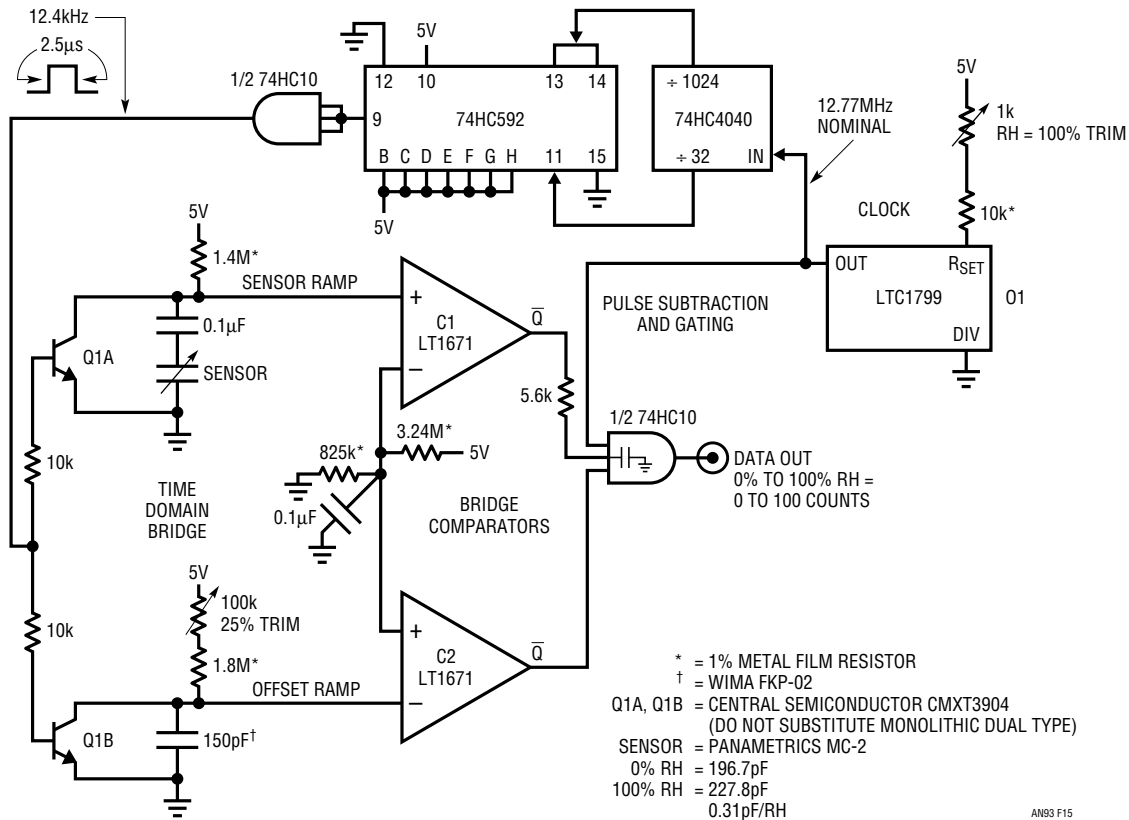


Figure 15. Humidity Transducer Digitizer Has Grounded Sensor, 1% Accuracy; Trim Scheme Allows Low Tolerance Sensors. Clocked Q1A-Q1B Configurations Produce Ramp Outputs. Q1A Ramp Slope Varies with Humidity Sensor Value, Q1B Ramp Represents Sensor's Offset (0% RH ≠ 0pF). C1, C2 Digitize Ramp Times. Gate Extracts Time Difference, Presents 0 to 100 Counts Out for 0% to 100% Relative Humidity

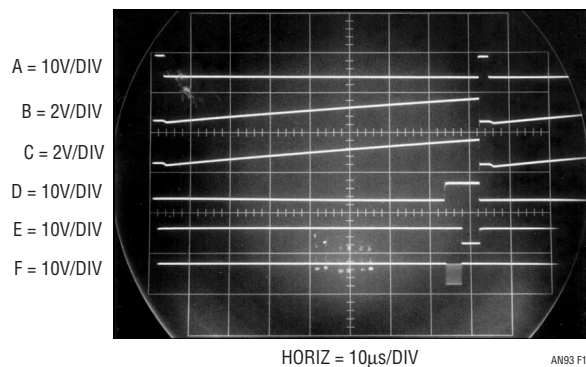
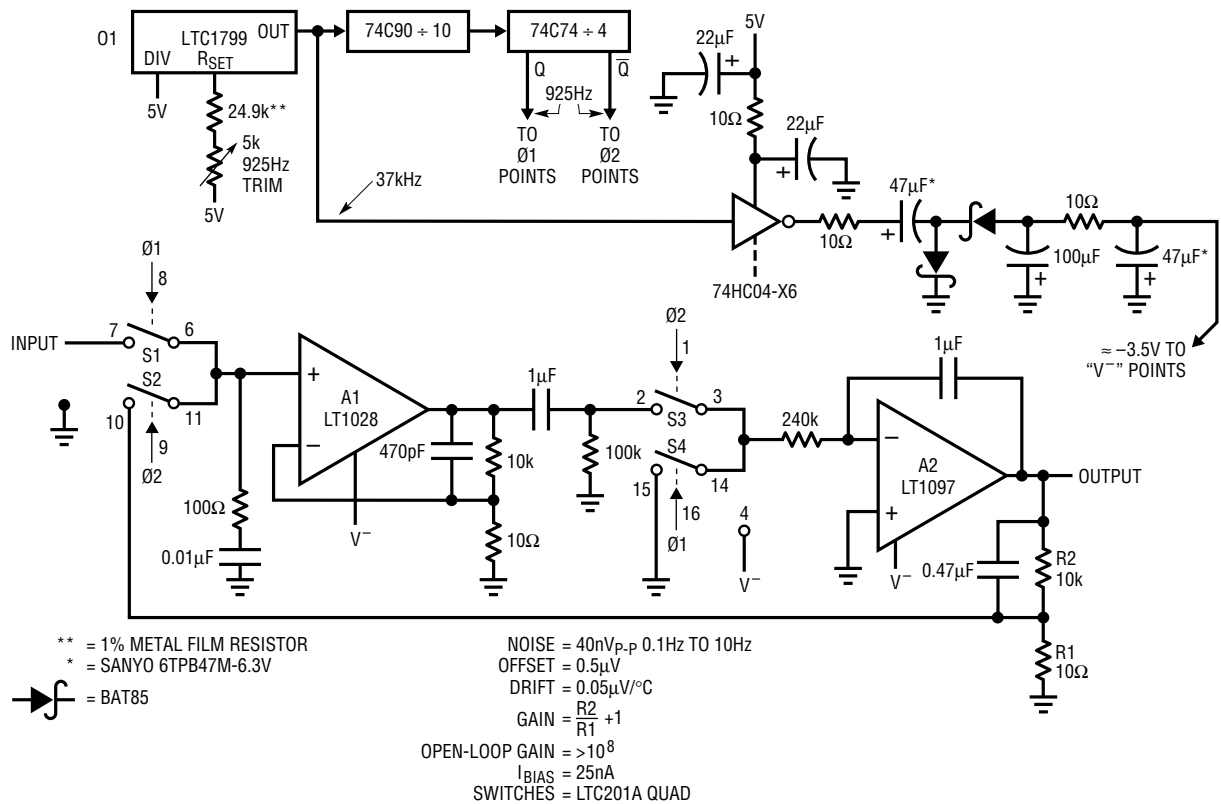


Figure 16. Humidity Sensor Time Domain Bridge Waveforms. Gate (Figure 15, Upper Left) Clocks (Trace A) Q1A and Q1B. Sensor and Offset Ramps Are Traces B and C. C1 and C2 Outputs are Traces D and E. Gate Extracts C1-C2 Time Difference, Presents Trace F's Digitized Output

40nV Noise, 0.05µV/°C Drift, Chopped Bipolar Amplifier

Figure 17's circuit, adapted from Reference 7, combines the low noise of an LT1028 with a chopper based carrier modulation scheme to achieve an extraordinarily low noise, low drift DC amplifier. DC drift and noise performance exceed any currently available monolithic amplifier. Offset is inside 1µV, with drift less than 0.05µV/°C. Noise in a 10Hz bandwidth is less than 40nV, far below monolithic chopper stabilized amplifiers. Bias current, set by the bipolar LT1028 input, is about 25nA. The circuit is powered by a single 5V supply, although its output will swing ±2.5V. Additionally, a carefully selected chopping frequency prevents deleterious interaction with 60Hz related components at the amplifier's input. These specifications suit demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

O1's 37kHz output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing A1 to see a chopped version of the input voltage. A1 amplifies this AC signal. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because A1 is AC coupled, its DC offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift noted. A1's input damper minimizes offset voltage contribution due to nonideal switch behavior.



AN93 F17

Figure 17. 5V Powered, Chopped Bipolar Amplifier. Noise $I_s \approx 40nV$ with $0.05\mu V/^\circ C$ Drift. DC Input Is Carrier Modulated, Amplified by A1, Demodulated to DC and Fed Back from A2. 925Hz Carrier Clock Prevents Interaction with 60Hz Line Originated Components. Negative Supply, Derived via Charge Pump, Allows Zero Volt Output Swing

Application Note 93

Normally, this single supply amplifier's output would be unable to swing to ground. This restriction is eliminated by powering the circuit's negative rail from a charge pump. O1's 37kHz output excites the charge pump, comprised of paralleled logic inverters and discrete components. Deliberate 10Ω loss terms combine with the specified $47\mu\text{F}$ capacitors to form a very low noise power source. These precautions eliminate charge pump noise which might otherwise degrade amplifier noise performance.

Figure 18, a noise plot of the amplifier in a 0.1Hz to 10Hz bandwidth, shows about 40nV of peak-to-peak noise. A1 and the 60Ω resistance of S1-S2 contribute about equally to form this noise. When using this amplifier, it is important to realize that A1's bias current flowing through the input source impedance causes additional noise. In general, to maintain low noise performance, source resistance should be kept below 500Ω . Fortunately, transducers such as strain gauge bridges, RTDs and magnetic detectors are well below this figure.

45nV Noise, $0.05\mu\text{V}/^\circ\text{C}$ Drift, Chopped FET Amplifier

Figure 19 replaces the previous circuit's input stage with a pair of extremely low noise J-FETs. In most other respects, circuit operation is similar. Noise increases very slightly, to $\approx 45\text{nV}$, but bias current decreases to only 500pA —50 times lower than the previous circuit. The noise performance is especially noteworthy—it is almost 17 times better than currently available monolithic chopper stabilized amplifiers and nearly equals the best bipolar designs. Other performance specifications, appearing in the figure, are similar to Figure 17.

The 925Hz clock is retained, although this $\pm 15\text{V}$ powered design uses zeners to derive internal $\pm 5\text{V}$ points. The clock and logic run from 5V and the LTC201 switches use $\pm 5\text{V}$. The switches low voltage rails reduce charge injection, minimizing its effect on offset voltage. RC damper networks further attenuate parasitic switch behavior effects, resulting in the $1\mu\text{V}$ offset specification.

Noise measured over Figure 20's 50 second interval is about 45nV in a 0.1Hz to 10Hz bandwidth. This is spectacularly low noise for a J-FET based design and is directly attributable to the input pairs' die size and current density.⁸

Clock Tunable, Filter Based Sine Wave Generator

A feedback loop enclosed resonator can be made to oscillate. Figure 21's sine wave generator takes advantage of this and eliminates the need for an amplitude control loop. This circuit, a mildly modified form of the Regan resonant bandpass loop, is clock tunable and produces sine and cosine outputs.⁹

The LTC1060 switched capacitor filter is set up as a clock tunable bandpass filter with a Q of 10. O1 clocks the filter at 100kHz, resulting in a 1kHz bandpass. C1, switched by the sine output, supplies square wave drive to the filter input in regenerative fashion. The loop is self-sustaining, resulting in continuous sine wave outputs at the indicated points. Zener bridge clamping of C1's output stabilizes square wave amplitude applied to the filter and, hence, the sine wave outputs. This form of amplitude control eliminates AGC loop settling times and potential instabilities. Changes in O1's clock frequency permit bandpass tuning, with no amplitude shifts during or after tuning.

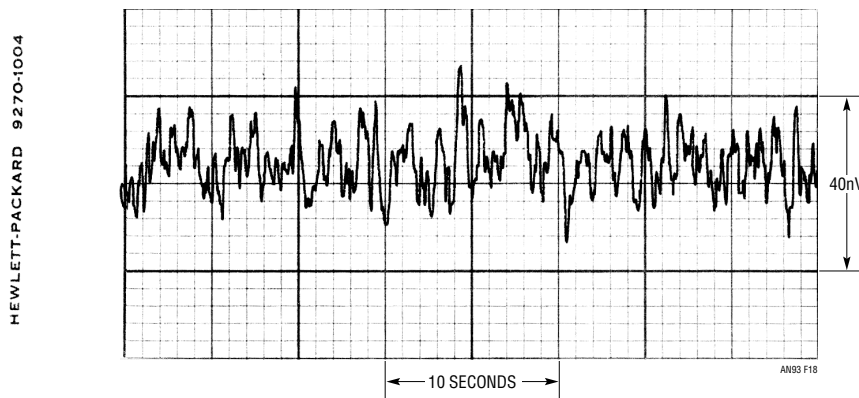
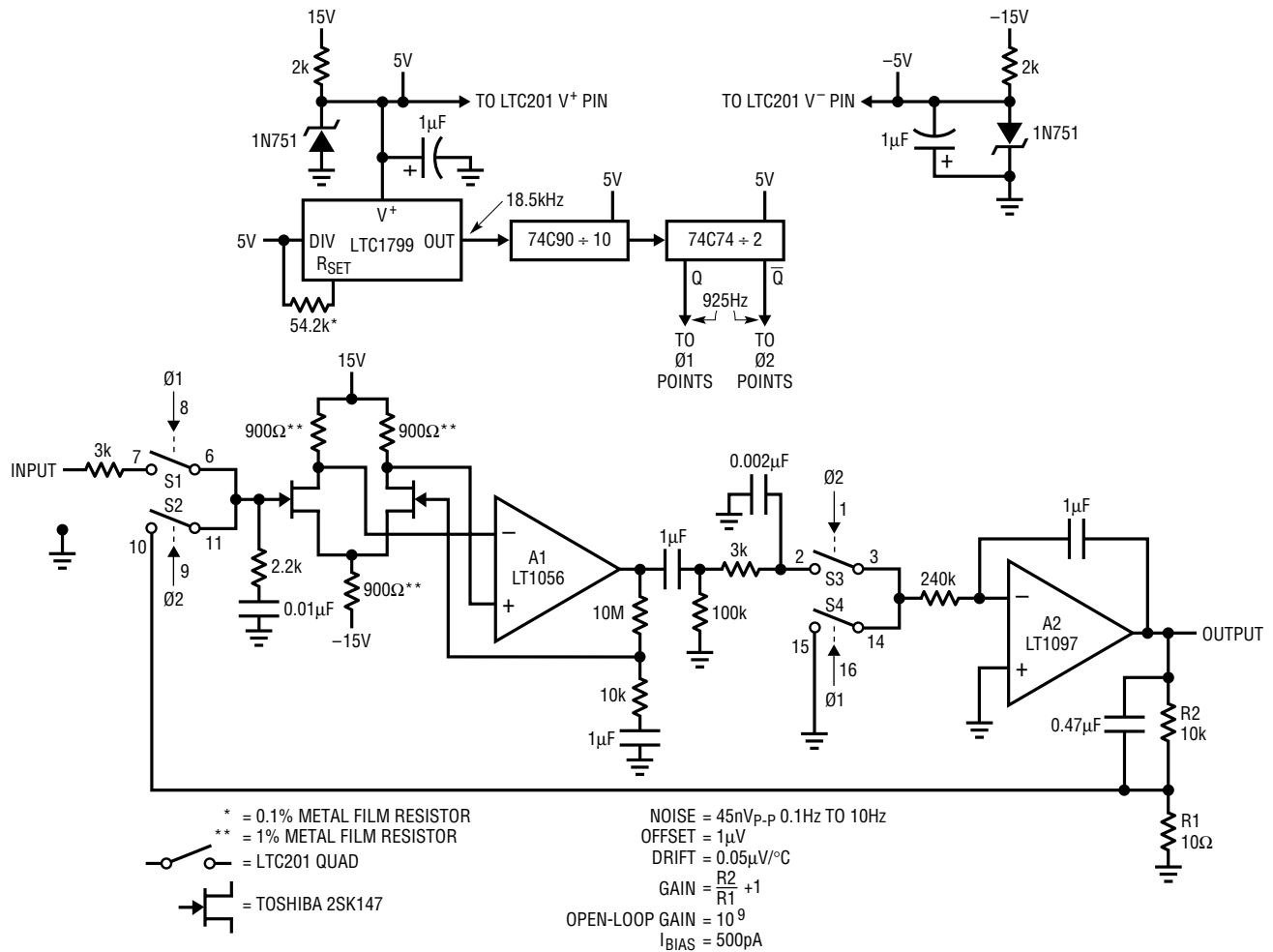


Figure 18. Noise in a 0.1Hz-10Hz Bandwidth Is about 40nV with $0.05\mu\text{V}/^\circ\text{C}$ Drift

Note 8: See References 8 and 9.

Note 9: This circuit draws heavily on a scheme originated by Tim Regan. See Reference 10.



AN93 F19

Figure 19. FET Input Version of Figure 17 Has 500pA Bias Current. 925Hz Clock Is Retained, Noise Increases Slightly to ≈45nV

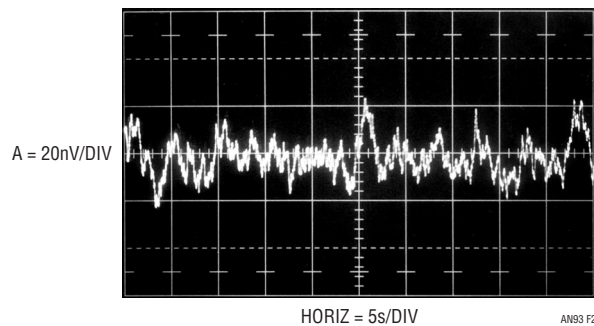


Figure 20. Chopped FET Input Amplifier Noise Is ≈45nV in 0.1Hz to 10Hz Bandwidth

Application Note 93

Figure 22 shows operating waveforms. The bandpass filter, responding to C1's clamped output (Trace A), produces sine (Trace C) and cosine (Trace B) outputs. Distortion, Trace D, dominated by filter clock residue, is 2%.

Clock Tunable, Memory Based Sine Wave Generator

This circuit generates a variable frequency sine wave by continuously clocking a sine coded lookup table memory. The memory's state is converted to an analog output by a

DAC. A strength of this technique is its rapid, high fidelity response to frequency and amplitude change commands.

O1, set to one of three output frequencies dictated by its digital control inputs, clocks the 74HC191 counters. These counters parallel load a 2716 EPROM programmed to produce an 8-bit (256 states) digitally coded sine wave. The program, developed by Sean Gold and Guy M. Hoover, appears in Figure 24.¹⁰ The 2716's parallel output is fed to a DAC, producing the analog output.

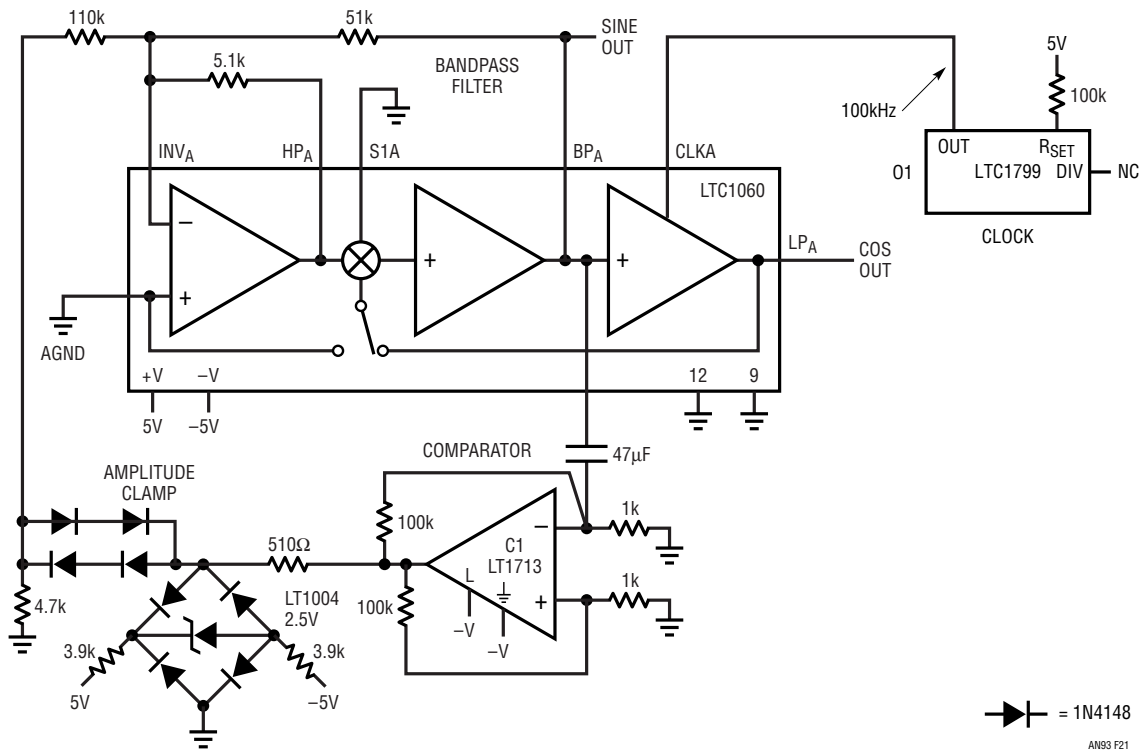


Figure 21. The Regan Resonant Bandpass Loop. A Bandpass Filter, Driven by C1's Oscillation Loop, Continuously Rings at Resonance. Clock Controls Output Frequency. Zener Bridge Clamp Sets Sine and Cosine Output Amplitude

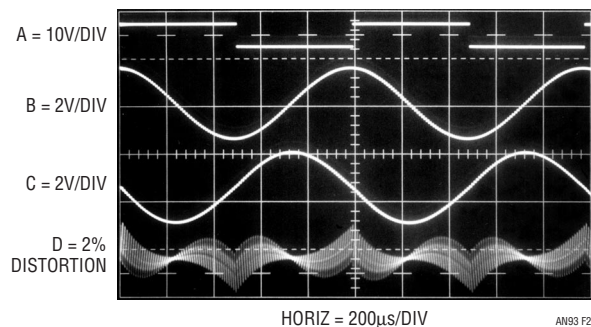


Figure 22. Bandpass Filter, Responding to C1's Loop Enforced Excitation (Zener Clamp Output, Trace A), Produces Sine (Trace C) and Cosine (Trace B) Outputs. Distortion (Trace D), Dominated by Switched Capacitor Filter Clock Residue, Is 2%

Note 10: See Reference 11.

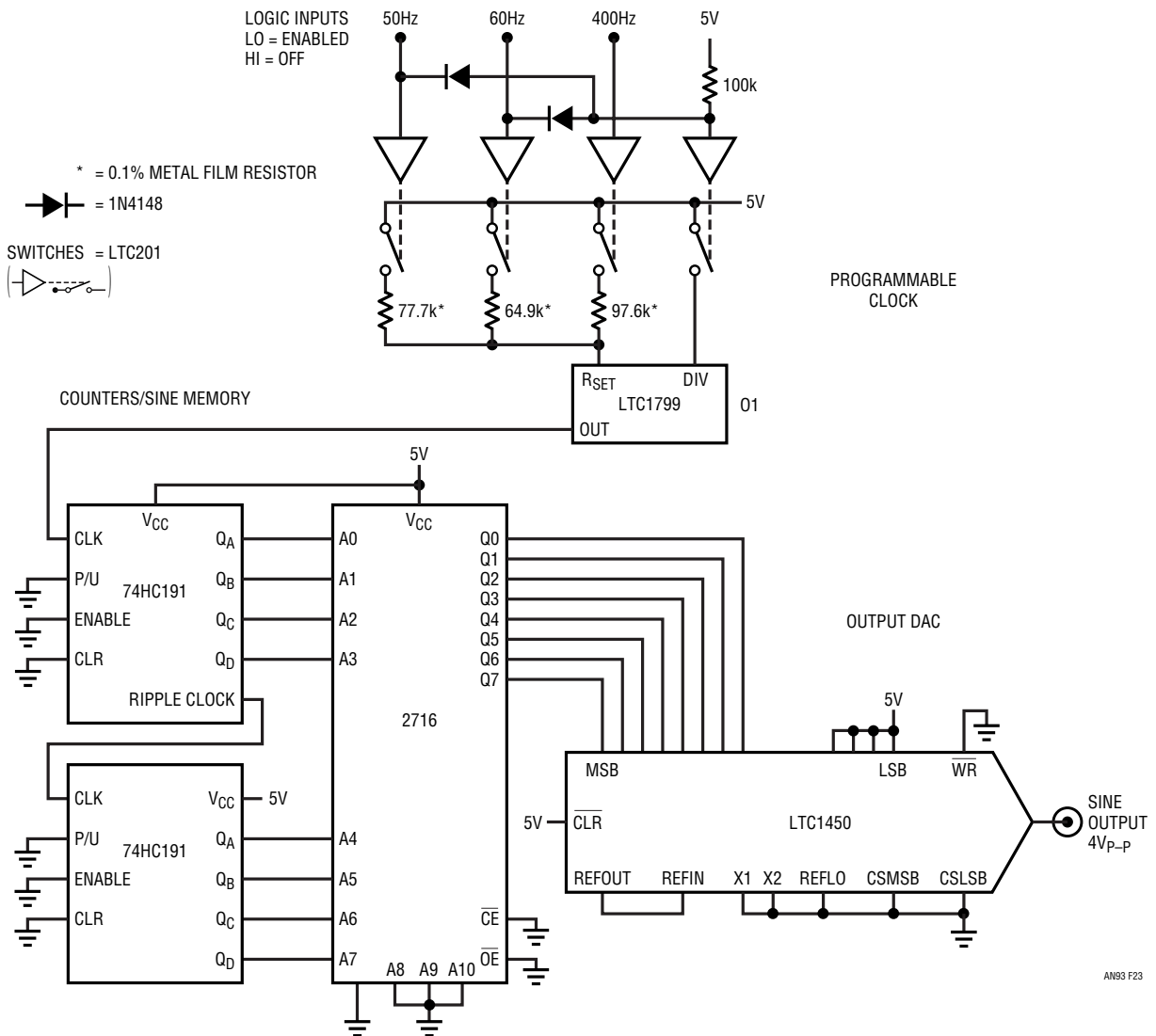


Figure 23. Counter Driven, Sine Encoded Memory Produces 0.75% Distortion Sinewave via D/A Converter. LTC1799 Oscillator Frequency, Controlled by Digital Inputs, Sets Output Frequency

Line	0736	Column	Wrap	APLZ/PC
				GENCODES
FF	FF	FF	FE	FE FE FD FD FC FB FA F9 F9 F7 F6
F5	F4	F3	F1	F0 EE ED EB E9 E8 E6 E4 E2 E0 DE DC
09	07	05	02	00 CE C8 C9 C6 C3 C1 BE B9 B8 B6 B3
80	AD	AA	A7	A4 A1 9E 9B 98 95 92 8E 8B 88 85 82
7F	7C	78	75	72 6F 6C 69 66 63 60 5D 5A 57 54 51
4E	4B	48	45	42 40 3D 3A 38 35 33 30 2E 2B 29 27
25	22	20	1E	1C 1A 18 17 15 13 11 10 0E 0D 0C 0A
09	08	07	06	05 04 03 03 02 02 01 01 00 00 00 00
00	00	00	00	01 01 02 02 03 03 04 05 06 07 08 09
0A	0C	0D	0E	10 11 13 15 17 18 1A 1C 1E 20 22 25
27	29	2B	2E	30 33 35 38 3A 3D 40 42 45 48 4B 4E
51	54	57	5A	5D 60 63 66 69 6C 6F 72 75 78 7C 7F
82	85	88	8B	8E 92 95 98 9B 9E A1 A4 A7 AA AD B0
83	B6	B8	B8	BE C1 C3 C6 C9 CB CE D0 D2 D5 D7 D9
DC	DE	E0	E2	E4 E6 E8 E9 EB ED EE F0 F1 F3 F4 F5
F6	F7	F9	F9	FA FB FC FD FE FE FE FF FF FF FF

Figure 24. Sinewave Generation Code for the Memory

Trace A in Figure 25 is the sine wave output, in this case tuned to 60Hz. Distortion, appearing as Trace B, is mostly composed of clock residue and measures about 0.75%. In Figure 26, the digital inputs abruptly change output frequency to 400Hz and then promptly return it to 60Hz. These frequency shifts occur crisply, with no alien components or untoward behavior. Amplitude shifts, accomplished by driving the DAC's reference input (see LTC1450 data sheet), are similarly well behaved. Figure 27 shows Trace B's amplitude faithfully responding to Trace A's DAC reference input step. As before, the lack of control loop time constants promotes uncorrupted response.

Application Note 93

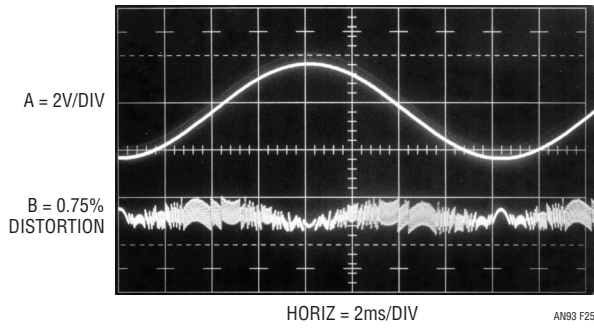


Figure 25. Sinewave Output (Trace A) and Its Distortion (Trace B). Clock Related Products Are Evident in Distortion Presentation

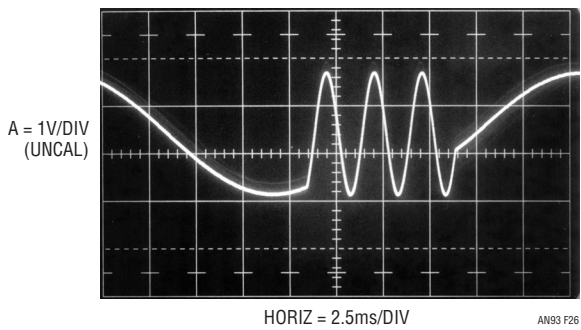


Figure 26. Fast Oscillator Frequency Shifting Permits Crisp Sinewave Output Frequency Change

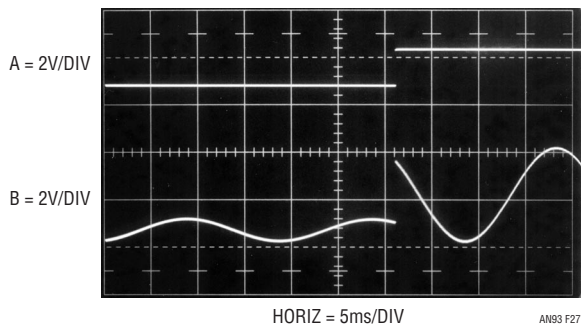


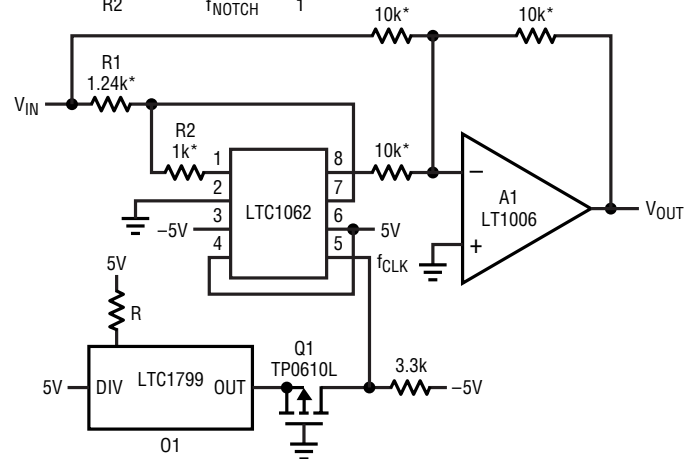
Figure 27. Trace B's Sinewave Amplitude Instantaneously and Faithfully Responds to DAC Reference Input Step, Trace A

Clock Tunable Notch Filter

Figure 28 shows a quick, clean way to tune a notch filter's center frequency by varying a single resistor, which could be switched. The LTC1062 switched capacitor filter and A1 form a clock tunable notch (see LTC1062 data sheet). O1, running from the 5V supply, furnishes the clock, which is level shifted by Q1 to drive the $\pm 5V$ powered LTC1062. In this case, three common notch frequencies are listed; others are selectable by tuning O1 in accordance with the equivalency listed.

R	CLOCK FREQUENCY	NOTCH CENTER FREQUENCY
210k	4.75kHz	60Hz
249k	3.96kHz	50Hz
31.5k	31.72kHz	400Hz

$$\frac{R1}{R2} = 1.234, \quad \frac{f_{\text{CLOCK}}}{f_{\text{NOTCH}}} = \frac{79.3}{1}$$



* = 1% METAL FILM RESISTOR

AN93 F28

Figure 28. A Clock Tuned, Highly Selective Notch Filter. LTC1799 Oscillator Sets Notch Center Frequency According to Table. R Value Could be Switched Under Digital Control

Figure 29 shows notch performance at a 60Hz center frequency. Response is down over 45dB at 60Hz, with steep slopes on either side of the notch. This characteristic is maintained as center frequency is clock-tuned over broad ranges.

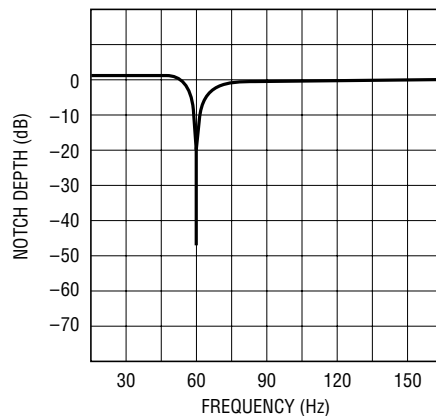


Figure 29. Notch Characteristic at 60Hz Center Frequency. Response Is Essentially Identical as Center Frequency Is Tuned over Broad Range

AN93 F29

Clock Tunable Interval Generator with $20 \times 10^6:1$ Dynamic Range

An accurate interval generator with large dynamic range appears in Figure 30.¹¹ The circuit is made up of a clock, a counter and a dual flip-flop. Clock frequency and counter modulo are programmable. A trigger input is passed to flip-flop 1's \bar{Q} output (Trace A, Figure 31) synchronously with O1's clock (Trace C). This output going low sets flip-flop 2's Q output, a circuit output, high (Trace B). Simultaneously, flip-flop 2's \bar{Q} output resets the 4060 counter, allowing it to accumulate clock pulses (again, Trace C). When enough clock pulses occur to set the selected 4060 output high, flip-flop 2's clear input (Trace D) is pulled low, ending the circuit's output width. The output width is settable by O1's frequency and the counter's modulo, both variable over many decades. As shown, the interval is

programmable over 800 nanoseconds to 16 seconds, although other counters can extend this range. Interval accuracy and stability is almost entirely dependent on O1's programming resistor.

8-Bit, 80µs, Passive Input, A/D Converter

In general, monolithic A/D converters have replaced discrete types. Occasionally, specific desirable circuit characteristics dictate a discrete design. Examples of such special cases include the need for a passive analog input, output data format, control protocol or economic constraints. Figure 32's 8-bit design has 90ppm/°C drift (<1LSB 0°C to 70°C) and converts in 80µs. The circuit consists of a current source, an integrating capacitor, a comparator, logic and a clock.¹²

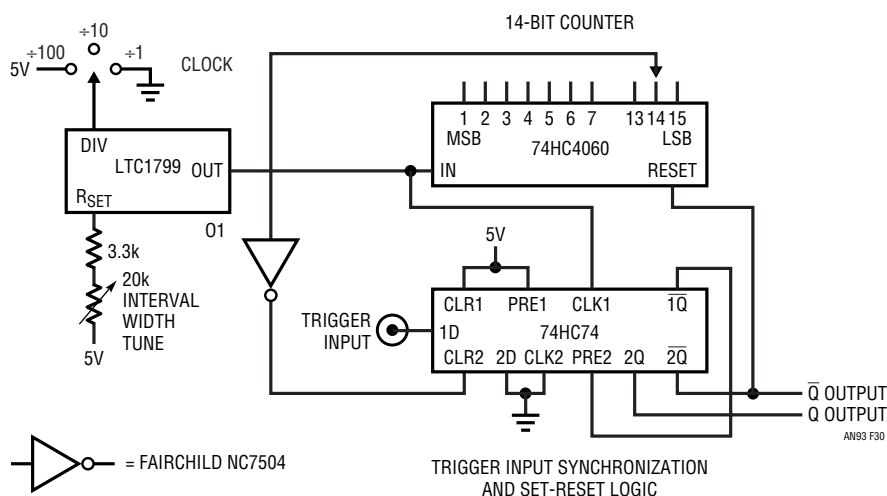


Figure 30. 1% Accurate Interval Generator with $20 \times 10^6:1$ Dynamic Range. Flip-Flop Output, Set by Trigger Input, Resets when Counter Times Out. LTC1799 Oscillator Controls Timing Sequence

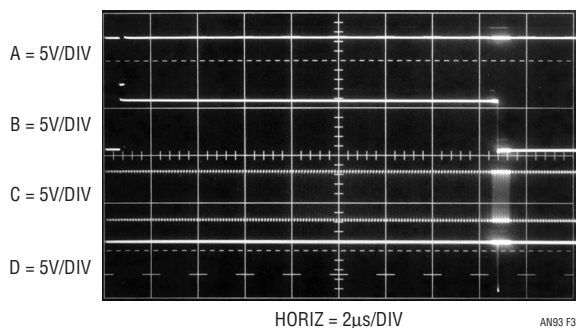


Figure 31. Trace A's Trigger Pulse Sets Circuit Output (Trace B) High. LTC1799 Oscillator (Trace C) Clocks Counter until Selected Counter Output Biases Inverter Low (Trace D), Resetting Circuit Output (Trace B). Reset Sequence Intensified for Photographic Clarity

Note 11: Pedestrian laboratory argot for interval generator is "one shot."

Note 12: This circuit is a modern incarnation of the earliest electronic A/D known to the author. See Reference 13.

Application Note 93

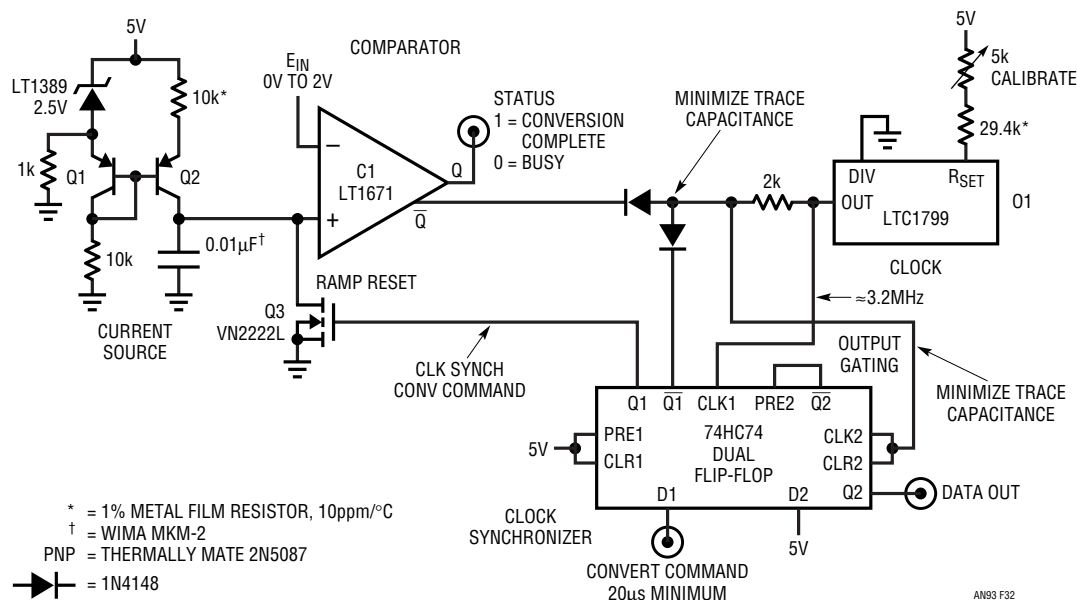


Figure 32. Simple 8-Bit A/D Converter Has Passive, High Impedance Input. Additional Features Include 80µs Conversion Time, Accurate 0°C to 70°C Operation

Applying a pulse to the convert command input causes flip-flop Q1 output to go high (Trace A, Figure 33) when the CLK1 input is clocked by O1. This turns on Q3, resetting the 0.01µF capacitor (Trace B). Simultaneously, Q1 goes low, pulling the CLK2-CLR2 input down. C1's Q output, the circuit's status output (Trace C), also goes low and C1's Q output rises high. This logic state prevents any of O1's clock pulses from being transmitted to the circuit's data output (Trace D). When the convert command falls, Q1 goes low, Q3 turns off and the 0.01µF capacitor begins to ramp. Concurrently, Q1 goes high, allowing clock pulses to appear at the data output. When the ramp crosses E_{IN}'s voltage, C1's outputs exchange state, pulling the CLK2-CLR2 line low and data output pulses cease. Thus, the O1 originated clock burst appearing at the data output is directly and solely proportional to E_{IN}. For the arrangement shown, 256 pulses appear for a 2V full-scale input. Conversion time decreases with the time required for the ramp to cross E_{IN}. A full-scale conversion requires 80µs, linearly descending to 8µs at 0.1 scale.

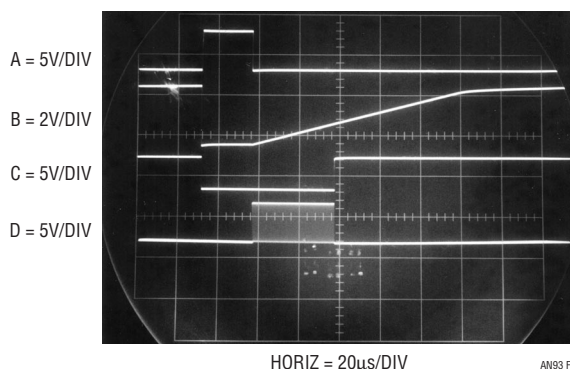


Figure 33. 8-Bit A/D Converter Waveforms (E_{IN} = 1V) Include Synchronized Convert Command (Trace A), Reference Ramp (Trace B), Status Output (Trace C) and Data Output (Trace D). Conversion, Initiable when Status Output Is High, Begins when Command Line Goes Low

Flip-flop 2, connected as a logic buffer, duplicates the high impedance diode-2kΩ node's logic state. As such, this node's trace capacitance should be minimized. This is facilitated by locating the diodes and 2k resistor adjacent to the CLK2-CLR2 inputs. Circuit trimming is accomplished by applying a 2V input and adjusting O1's frequency output ("calibrate") for 256 data output pulses per conversion.

Note: This Application Note was derived from a manuscript originally prepared for publication in EDN magazine.

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APPENDIX A

LTC1799 INTERNAL OPERATION

As shown in Figure A1, the LTC1799's master oscillator is controlled by the ratio of the voltage between the V^+ and SET pins and the current entering the SET pin (I_{RES}). The voltage on the SET pin is forced to approximately 1.13V below V^+ by the PMOS transistor and its gate bias voltage. This voltage is accurate to $\pm 7\%$ at a particular input current and supply voltage (see Figure A2). The effective input resistance is approximately 2k.

A resistor R_{SET} , connected between the V^+ and SET pins, "locks together" the voltage ($V^+ - V_{SET}$) and current, I_{RES} , variation. This provides the LTC1799's high precision. The master oscillation frequency reduces to:

$$f_{MO} = 10\text{MHz} \cdot \left(\frac{10\text{k}\Omega}{R_{SET}} \right)$$

The LTC1799 is optimized for use with resistors between 10k and 200k, corresponding to master oscillator frequencies between 0.5MHz and 10MHz. Accurate frequencies up to 20MHz ($R_{SET} = 5\text{k}$) are attainable if the supply voltage is greater than 4V.

To extend the output frequency range, the master oscillator signal may be divided by 1, 10 or 100 before driving OUT (Pin 5). The divide-by value is determined by the state of the DIV input (Pin 4). Tie DIV to GND or drive it below 0.5V to select $\div 1$. This is the highest frequency range, with the master output frequency passed directly to OUT. The DIV pin may be floated or driven to midsupply to select $\div 10$, the intermediate frequency range. The lowest frequency range, $\div 100$, is selected by tying DIV to V^+ or driving it to within 0.4V of V^+ . Figure A3 shows the

Application Note 93

relationship between R_{SET} , divider setting and output frequency, including the overlapping frequency ranges near 100kHz and 1MHz.

The CMOS output driver has an on resistance that is typically less than 100Ω. In the ÷1 (high frequency) mode, the rise and fall times are typically 7ns with a 5V supply and 11ns with a 3V supply. These times maintain a clean

square wave at 10MHz (20MHz at 5V supply). In the ÷10 and ÷100 modes, where the output frequency is much lower, slew rate control circuitry in the output driver increases the rise/fall times to typically 14ns for a 5V supply and 19ns for a 3V supply. The reduced slew rate lowers EMI (electromagnetic interference) and supply bounce.

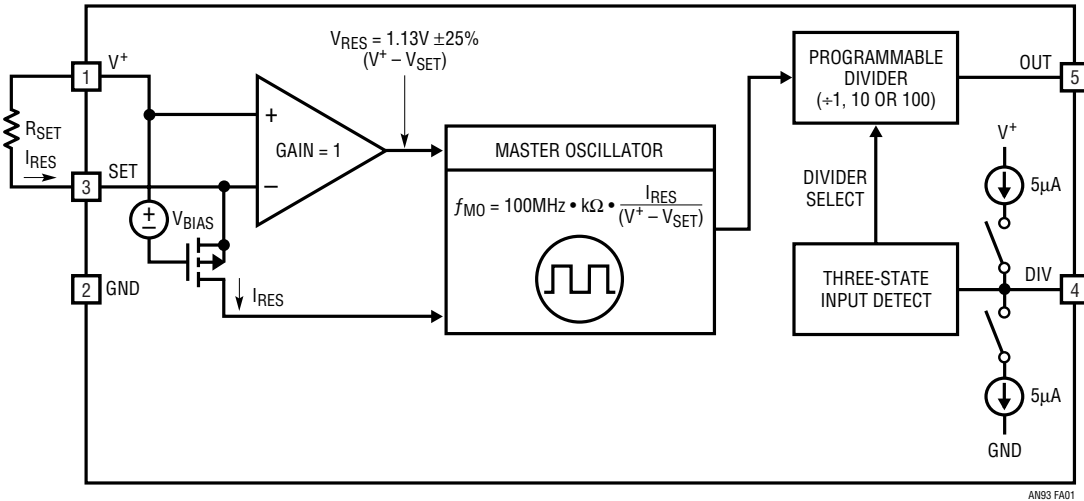


Figure A1. LTC1799 Master Oscillator Frequency Is Controlled by Ratio of Voltage Between V^+ and SET and Current Entering SET. Pin-Programmable Frequency Divider Permits Output Frequency Ranging

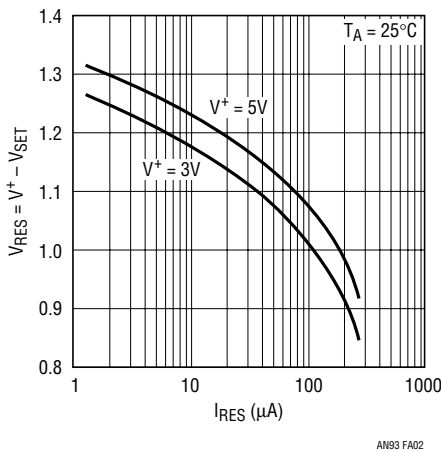


Figure A2. $V^+ - V_{SET}$ Variation with I_{RES}

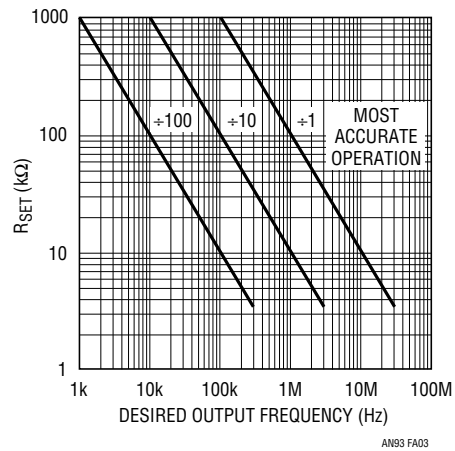


Figure A3. R_{SET} vs Desired Output Frequency for Three Output Divider Settings

APPENDIX B

R_{SET} NODE CONSIDERATIONS

The R_{SET} node is the LTC1799's sole analog input. Figure B1, a partial LTC1799 block diagram (see Appendix A for more detail) shows that the node is a MOSFET source and an amplifier input. Equivalent input resistance is about 2kΩ and the point sits approximately 1.13V below the LTC1799 V⁺ pin. Excessive stray capacitance or noise at R_{SET} will influence amplifier operation, causing master oscillator jitter. Stray capacitance at R_{SET} should be limited to <10pF and signal lines, particularly those operating at high speed, should be routed away from R_{SET}. A simple guideline is to place the programming resistor directly at

R_{SET}. In cases where R_{SET} is a transducer (e.g., a temperature sensor), it may be desirable to locate the transducer at the end of cable. Maintaining low effective capacitance at the R_{SET} node requires “bootstrap” driving the cable shield at the R_{SET} potential (Figure B2). This negates the effect of shield capacitance, because charge cannot transfer between it and R_{SET}. An amplifier capable of driving the shield is required but this is accomodatable. Text Figure 5 is a practical incarnation of this technique.

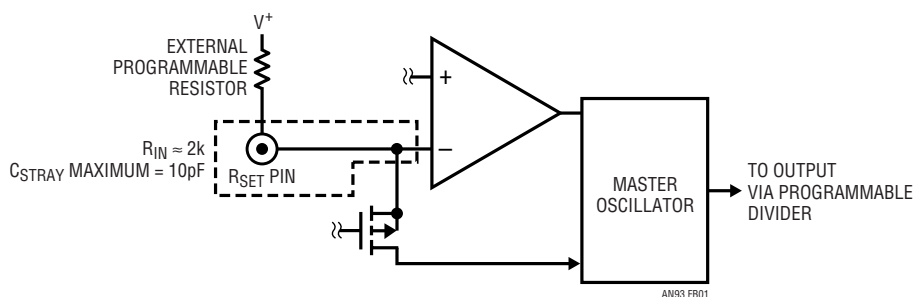


Figure B1. R_{SET} Pin Has Effective Input Resistance of ≈2k. Stray Pin Capacitance Must be <10pF to Avoid Output Frequency Jitter

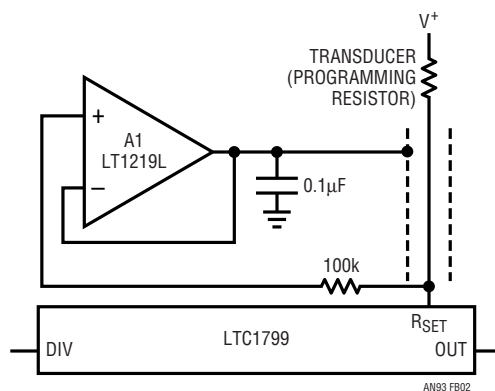
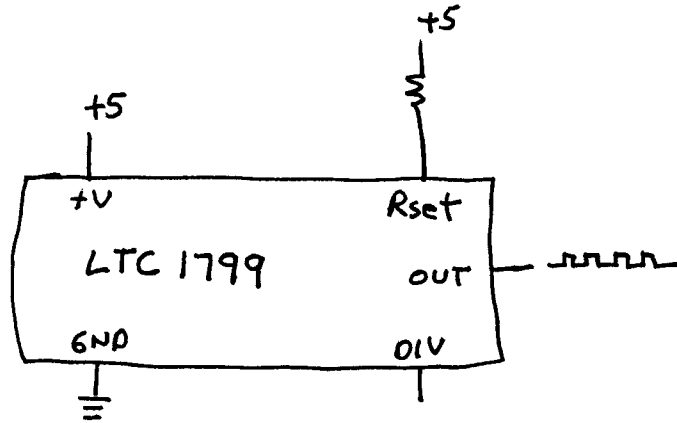


Figure B2. A1 Senses R_{SET} Voltage, Bootstraps Cable Drive Potential. Arrangement Prevents Cable Capacitance from Influencing R_{SET} Node Because Charge Cannot Transfer. 100k Resistor Isolates A1's Input and Trace Capacitance

Application Note 93



"Everything should be as simple as possible,
but not too simple."

— Einstein

William
'03

Slew Rate Verification for Wideband Amplifiers

The Taming of the Slew

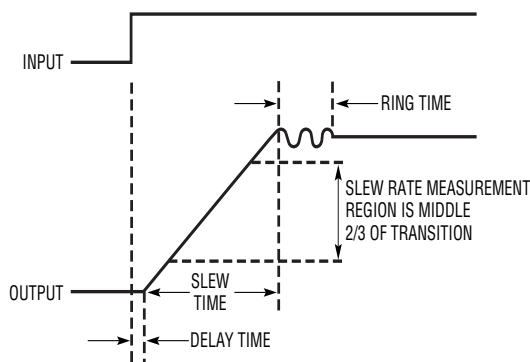
Jim Williams

INTRODUCTION

Slew rate defines an amplifier's maximum rate of output excursion. This specification sets limits on undistorted bandwidth, an important capability in A/D driver applications. Slew rate also influences achievable performance in D/A output stages, filters, video amplification and data acquisition. Because of its importance, amplifier slew rate must be verified by measurement. Deriving a measurement approach requires understanding slew rate's relationship to amplifier dynamics.

Amplifier Dynamic Response

Figure 1 shows that amplifier dynamic response components include delay, slew and ring times. The *delay time* is small and is almost entirely due to amplifier propagation delay. During this interval there is no output movement. During *slew time* the amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. The



AN94 F01

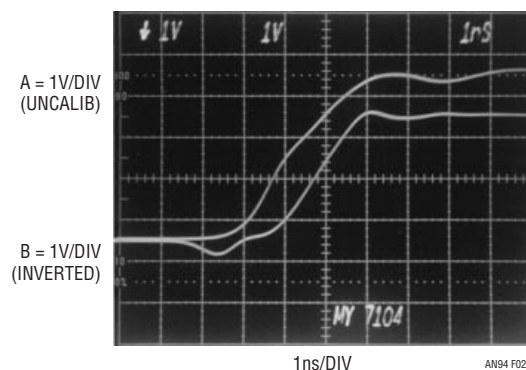
Figure 1. Amplifier Response Components Include Delay, Slew and Ring Times. Slew Rate is Typically Measured During Middle 2/3 of Slew Time

Note 1. Although not considered here, settling time determination is a high order measurement challenge. It is treated in considerable detail in References 2, 3, and 4.

total elapsed time from input application until the output arrives at and remains within a specified error band around the final value is the *settling time*.¹

Slew rate, normally measured during the middle 2/3 of output movement at $A = +1$, is expressed in volts/microsecond. Discounting the initial and final movement intervals ensures that amplifier gain-bandwidth limitations during partial input overdrive do not influence the measurement.

Historically, slew rate measurement has been relatively simple.² Early amplifiers had slew rates of typically $1\text{V}/\mu\text{s}$, with later versions sometimes reaching hundreds of volts/ μs . Standard laboratory pulse generators easily supplied rise times well beyond amplifier speeds. As slew rates have crossed $1000\text{V}/\mu\text{s}$, the pulse generator's finite rise time has become a concern. A recent device, the LT1818 (See Box Section, "A $2500\text{V}/\mu\text{s}$ Slew Rate Amplifier with



AN94 F02

Figure 2. LT1818 Slew Rate (Upper Trace) is Comparable to Schottky TTL Transition Time (Lower Trace)

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

Note 2. The term "slew rate" has a clouded origin. Although used for many years in amplifier literature, there is no mention of it on the Philbrick K2-W (the first standard product op amp, introduced in January 1953) data sheet, dated 1964. Rather, the somewhat more dignified "maximum rate of output swing" is specified.

A 2500V/ μ S SLEW RATE AMPLIFIER WITH -85 dBc DISTORTION AT 5MHz

A/D driving, D/A output stages, data acquisition, video amplification and high frequency filters require low distortion, wideband amplifiers. The LT1818 amplifier (LT1819 is a dual version), with 2500V/ μ s slew rate, 400MHz GBW and -85 dBc distortion, is designed for these applications. Additionally, only 9mA supply current is required. The table provides short form specifications.

LT1818 Short Form Specifications

CHARACTERISTIC	SPECIFICATION
Gain – Bandwidth Product	400MHz (Typ) 270MHz (Min)
Full Power Bandwidth	95MHz (Typ)
Slew Rate	2500V/ μ s (Typ), A = +1
Delay	1ns (Typ)
Settling Time	10ns to 0.1% (Typ)
Distortion	-85 dBc at 5MHz (Typ)
Input Noise Voltage	6nV/ $\sqrt{\text{Hz}}$ (Typ)
DC Gain	2500 (Typ) 1500 (Min)
Output Current	± 70 mA (Typ) ± 40 mA (Min)
Input Voltage Range	± 3.5 V at ± 5 V Supplies (Min)
Input Bias Current	8 μ A (Max)

-85 dBc Distortion at 5MHz”), has a 2500V/ μ s slew rate, or 2.5V/nanosecond. Figure 2 puts this transition rate in perspective. The LT1818’s slew rate (Trace A) is comparable to a Schottky TTL gate’s (Trace B) transition time. Such speed eliminates almost all pulse generators as candidates for putting the amplifier into slew rate limiting.

Pulse Generator Rise Time Effects on Measurement

Pulse generator rise time limitations are a significant concern when attempting to accurately determine slew rate. Figures 3 through 6 demonstrate this by recording amplifier (at A = +1) response to progressively faster pulse generator rise times. Figure 3’s apparent slew rate limit is ≈ 385 V/ μ s when driven by a 10ns rise time pulse generator. Figure 4 indicates 800V/ μ s using a 5ns rise time generator. A 3.5ns rise time generator prompts Figure 5’s 1400V/ μ s response and a 1ns rise time instrument results in Figure 6’s 2500v/ μ s observed slew rate. Figure 7’s plot summarizes results. The data shows a non-linear slew rate increase as pulse generator rise time

decreases. The continuous slew rate increase with decreasing generator rise time, although approaching a zero rise time enforced bound, hints that slew rate limit has not been reached. Determining if this is so requires a faster pulse generator than Figure 6’s 1ns rise time unit.

Subnanosecond Rise Time Pulse Generators

The majority of general purpose pulse generators have rise times in the 2.5ns to 10ns range. Instrument rise times below 2.5ns are relatively rare, with only a select few types getting down to 1ns.³ The ranks of subnanosecond rise time generators are even thinner. Subnanosecond rise time generation, particularly if relatively large swings (e.g. 5V to 10V) are desired, employs arcane technologies and exotic construction techniques (see references 5–16 and 20). Available instruments in this class work well, but can easily cost \$10,000 with prices rising towards \$30,000 depending on features. For slew rate testing in a laboratory or production environment there is a substantially less expensive alternative.

360ps Rise Time Pulse Generator

Figure 8 shows a circuit for producing subnanosecond rise time pulses. Rise time is 360ps, with adjustable pulse amplitude. Output pulse occurrence is settable from before-to-after a trigger output. This circuit uses an avalanche pulse generator to create extremely fast rise time pulses.⁴

Q1 and Q2 form a current source that charges the 1000pF capacitor. When the LTC1799 clock is high (trace A, Figure 9) both Q3 and Q4 are on. The current source is off and Q2’s collector (trace B) is at ground. C1’s latch input prevents it from responding and its output remains high. When the clock goes low, C1’s latch input is disabled and its output drops low. The Q3 and Q4 collectors lift and Q2 comes on, delivering constant current to the 1000pF capacitor (trace B). The resulting linear ramp is applied to C1 and C2’s positive inputs. C2, biased from a potential derived from the 5V supply, goes high 30 nanoseconds after the ramp begins, providing the “trigger output” (trace C)

Note 3: See Reference 3 for further discussion and recommendations.

Note 4: Additional examples of avalanche pulse generators and theoretical discussion appear in Reference 3 and References 5 through 16. The circuit detailed here produces positive going pulses referred to a zero volt baseline. Level shifting options are presented in Appendix B, “Pulse Generator Output Level Shifting.”

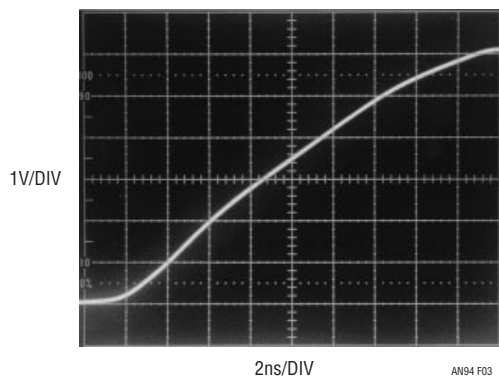


Figure 3. LT1818 Slew Rate Measures $\approx 385\text{V}/\mu\text{s}$ When Driven By Ten Nanosecond Rise Time Pulse Generator

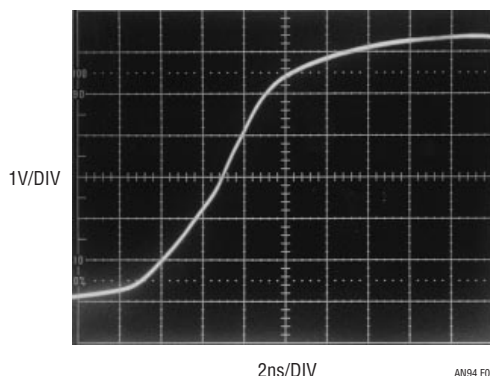


Figure 4. Five Nanosecond Rise Time Pulse Generator Indicates $800\text{V}/\mu\text{s}$ Slew Rate

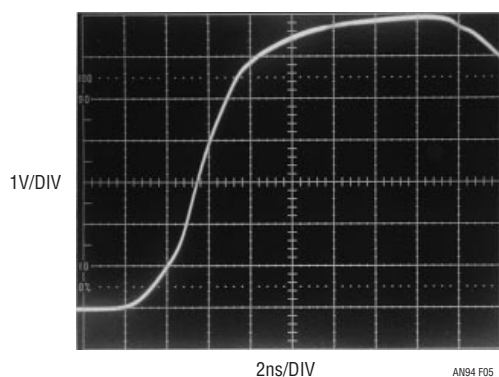


Figure 5. $1400\text{V}/\mu\text{s}$ Slew Rate is Observed with Faster ($t_{\text{RISE}} = 3.5\text{ns}$) Pulse Generator

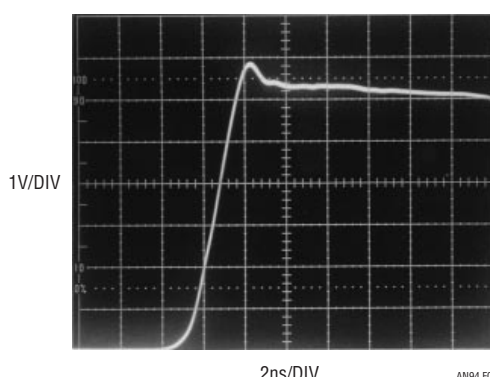


Figure 6. One Nanosecond Rise Time Pulse Generator Results in $2500\text{V}/\mu\text{s}$ Slew Rate. Verifying Slew Rate Limiting Occurrence Requires Repeating Measurement with Subnanosecond Rise Time Pulse Generator

via its output network. C1 goes high when the ramp crosses the potentiometer programmed delay at its negative input, in this case about 170ns. C1 going high triggers the avalanche-based output pulse (trace D), which will be described. This arrangement permits the delay programming control to vary output pulse occurrence from 30 nanoseconds before to 300 nanoseconds after the trigger output. Figure 10 shows the output pulse (trace D) occurring 25ns before the trigger output. All other waveforms are identical to Figure 9.

When C1's output pulse is applied to Q5's base, it avalanches. The result is a quickly rising pulse across Q5's emitter termination resistor. The 10pF collector capacitor and the charge line discharge, Q5's collector voltage falls and breakdown ceases. The 10pF collector capacitor and the charge line then recharge. At C1's next pulse, this action repeats. The 10pF capacitor supplies the initial pulse response, with the charge lines prolonged discharge contributing the pulse body. The 40" charge line length forms an output pulse width about 12ns in duration.

Avalanche operation requires high voltage bias. The LT1533 low noise switching regulator and associated components supply this high voltage. The LT1533 is a "push-pull" output switching regulator with controllable transition times.

Output harmonic content ("noise") is notably reduced with slower switch transition times.⁵ Switch current and voltage transition times are controlled by resistors at the R_{CSL} and R_{VSL} pins, respectively. In all other respects the circuit behaves as a classical push-pull, step-up converter.

Circuit Optimization

Circuit optimization begins by setting the "Output Amplitude Vernier" to maximum and grounding Q4's collector. Next, set the "Avalanche Voltage Adjust" so free running

Note 5: The LT1533's low noise performance and its measurement are discussed in Reference 17.

Application Note 94

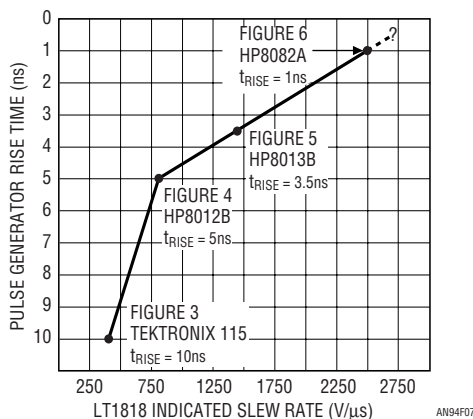


Figure 7. Summarized Data for the Pulse Generators. Decreasing Rise Time Promotes Higher Observed Slew Rate. Verifying Slew Rate Limiting Occurrence Requires Subnanosecond Rise Time Pulse Generator

pulses *just* appear at Q5's emitter, noting the bias test points voltage. Readjust the "Avalanche Voltage Adjust" five volts below this voltage and unground Q4's collector. Set the "30ns Trim" so the trigger output goes low 30ns after the clock goes low. Adjust the delay programming control to maximum and set the "300ns Calib." so C1 goes high 300ns after the clock goes low. Slight interaction between the 30ns and 300ns trims may require repeating their adjustments until both points are calibrated.

Q5 requires selection for optimal avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 30 2N2501s, spread over a 17-year date code span, yielded $\approx 90\%$. All "good" devices switched in less than 475ps with some below 300ps.⁶ In practice, Q5 should be selected for "in-circuit" rise time under 400 picoseconds. Once this is done, output pulse shape is optimized for slew rate testing by adjusting Q5's collector damping trim. The optimization procedure takes full advantage of the freedom that pulse purity is *not* required for slew rate testing. Normally, the pulse edge is carefully adjusted so that maximum transition speed is attained with minimal sacrifice of pulse purity. Slew rate testing does not require this, considerably simplifying optimization.⁷

Slew rate testing permits overshoot and post-transition aberrations if they do not influence amplifier response in the measurement region. Figures 11 through 13 detail the optimization procedure. In Figure 11, the damping trim is set for significant effect, resulting in a reasonably clean pulse but sacrificing rise time.⁸ Figure 12 represents the

opposite extreme. Minimal damping accentuates rise time, but pronounced post-transition ring may influence amplifier operation during slew testing. Figure 13's compromise damping is more realistic. Edge rate is only slightly reduced, but post-transition ring is significantly attenuated. The damping photographs were taken with a 1GHz real time oscilloscope (Tektronix 7104/7A29/7B15) with a 350ps rise time limit. Accurately determining Figure 13's rise time requires more bandwidth.⁹ Figure 14, taken with a 3.9GHz ($t_{RISE} = 90ps$) bandwidth oscilloscope (Tektronix 556 with 1S2 sampling plug-in) indicates 360 picosecond output rise time.¹⁰ Figure 15 aids measurement confidence by verifying 360 picosecond rise time in a 6GHz ($t_{RISE} = 60$ picoseconds) oscilloscope bandwidth (Tektronix TDS 6604). The 360 picosecond rise time is almost three times faster than Figure 6's 1 nanosecond rise time pulse generator, which promoted a 2500V/ μ s slew rate. Figure 16 puts this kind of speed into perspective. Trace A's 360ps rise time has completed its transition before trace B's 400MHz LT1818 amplifier begins to move! Trace A's rise time is actually faster than depicted, as the 1GHz real time measurement bandwidth limits observed response. Applying this faster rise time pulse should add useful information to Figure 7's data.

Refining Slew Rate Measurement

Figure 17 shows amplifier (A = +1) response to the 360 picosecond rise time pulse in a 1GHz real time bandpass. The middle 2/3 of the positive transaction, the slew rate measurement region, appears faster than Figure 6. Figure 18 increases sweep speed to 500 picoseconds/division. The photograph shows a measurement region

Note 6: 2N2501s are available from Semelab plc. Sales@semelab.co.uk; Tel. 44-0-1455-556565
A more common transistor, the 2N2369, may also be used but switching times are rarely less than 450ps. See also Footnotes 10 and 11.

Note 7: Optimization procedures for obtaining high degrees of pulse purity while preserving rise time appear in References 3, 5 and 6.

Note 8: The strata is becoming rarefied when a subnanosecond rise time is described as "sacrificed."

Note 9: Accurate rise time determination at these speeds mandates verifying measurement signal path (cables, attenuators, probes, oscilloscope) integrity. See Appendix A, "Verifying Rise Time Measurement Integrity" and Appendix C, "Connections, Cables, Adapters, Attenuators, Probes and Picoseconds."

Note 10: Experimental adjustment, iterated towards favorable results, of Q5's lead lengths, impedances and layout may be required for fastest rise time.

slew rate of $\approx 2800\text{V}/\mu\text{s}$, revealing an 11% error in Figure 6's determination. Applying these findings to Figure 7's plot produces Figure 19. The new data suggests that, while slew rate "hard" limiting may not be occurring, little practical improvement is possible because rise time is approaching zero. A faster rise time pulse generator could confirm this, but any slew rate improvement would likely

be academic.¹¹ Realistically, the large signal, 360 picosecond rise time input required to promote $2800\text{V}/\mu\text{s}$ slew rate is rarely encountered in practical circuitry.

Note 11: Faster rise times are possible, although considerable finesse is required in Q5's selection, layout, mounting, terminal impedance choice and triggering. The 360ps rise time quoted in the text represents readily reproducible results. Rise times below 300ps have been achieved, but require considerable and tedious effort. See Reference 5 and 6.

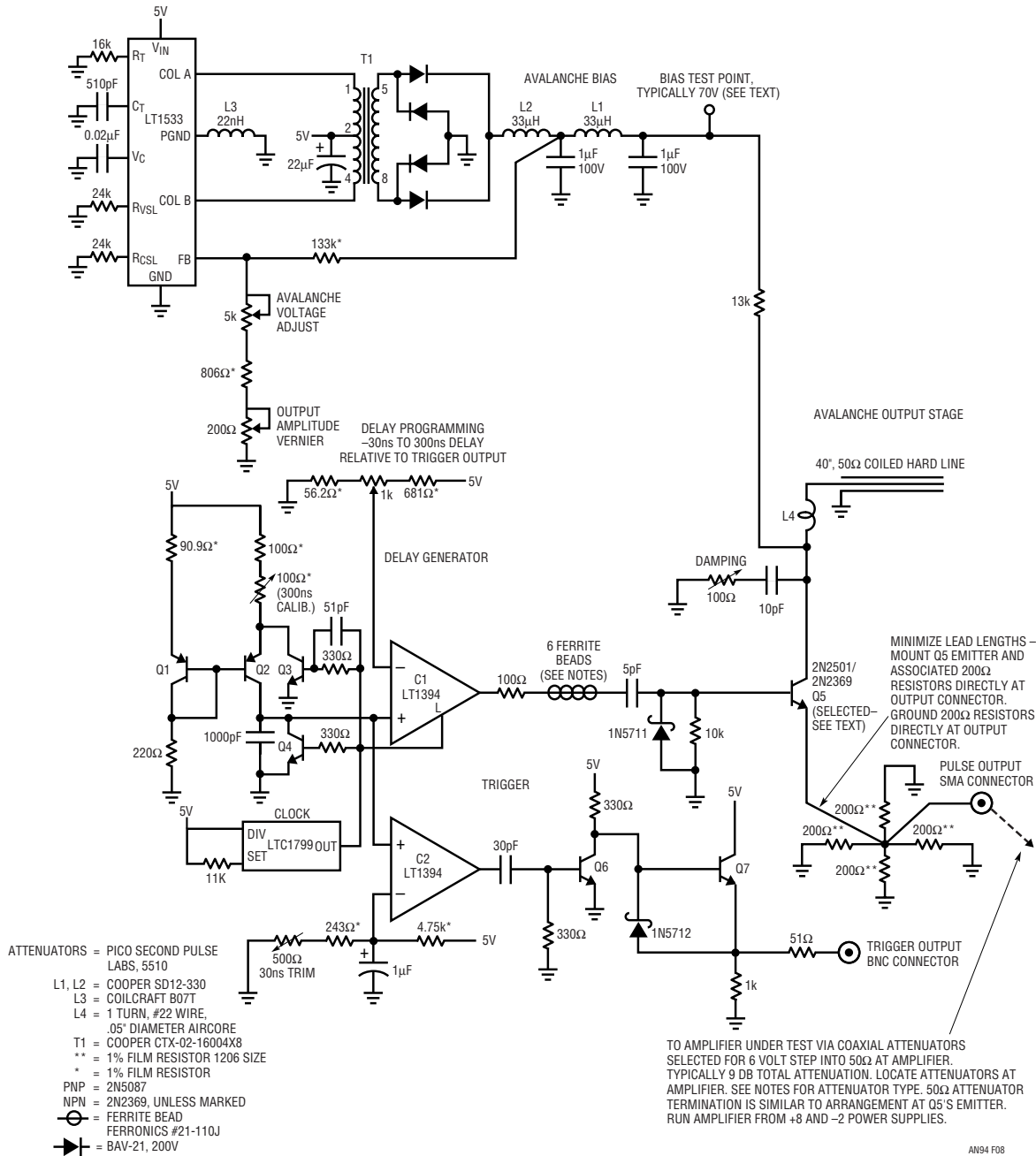


Figure 8. Variable Delay Triggers a Subnanosecond Rise Time Pulse Generator. Charge Line at Q5's Collector Determines ≈ 10 Nanosecond Output Width. Output Pulse Occurance is Settable from Before-to-After Trigger Output

Application Note 94

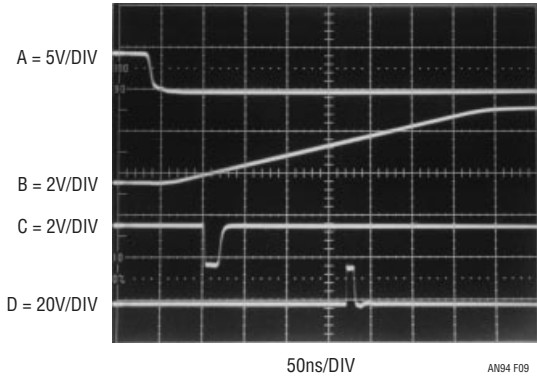


Figure 9. Pulse Generator's Waveforms Include Clock (Trace A), Q2's Collector Ramp (Trace B), Trigger Output (Trace C) and Pulse Output (Trace D). Delay Sets Output Pulse ≈ 170 ns After Trigger Output

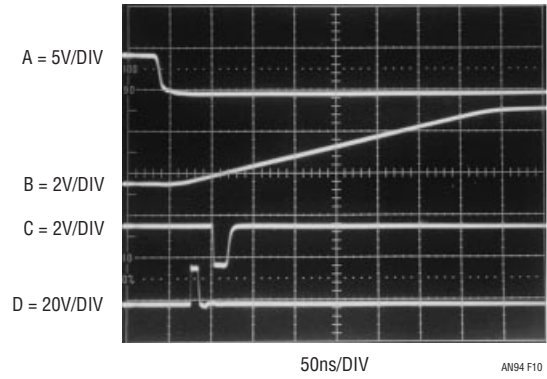


Figure 10. Pulse Generator's Waveforms with Delay Adjusted for Output Pulse Occurrence (Trace D) 25ns Before Trigger Output (Trace C). All Other Activity is Identical to Previous Figure

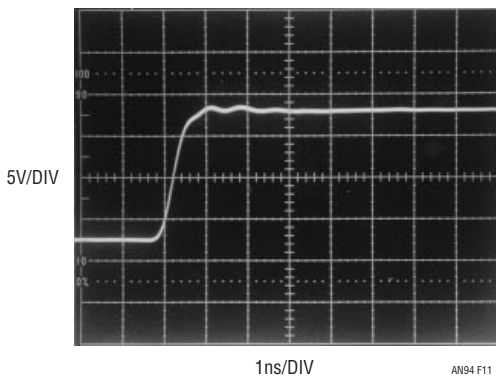


Figure 11. Excessive Damping is Characterized by Front Corner Rounding and Minimal Pulse-Top Aberrations. Trade Off is Relatively Slow Rise Time

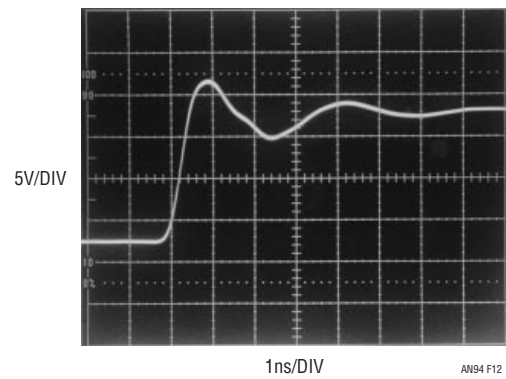


Figure 12. Minimal Damping Accentuates Rise Time, Although Pulse-Top Ringing is Excessive

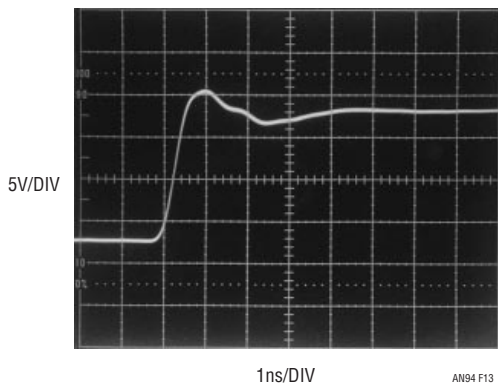


Figure 13. Optimal Damping Retards Pulse-Top Ringing; Preserves Rise Time in Slew Rate Measurement Region

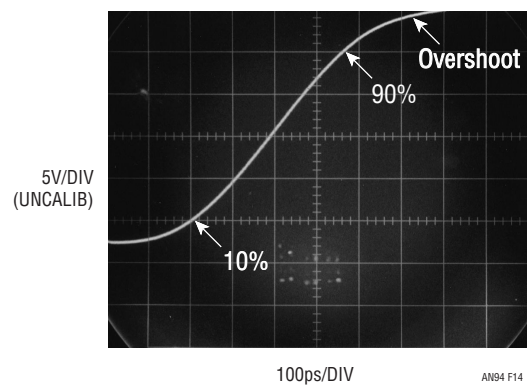


Figure 14. Figure 13's Rise Time Measures 360 Picoseconds in 3.9GHz Sampled Bandpass

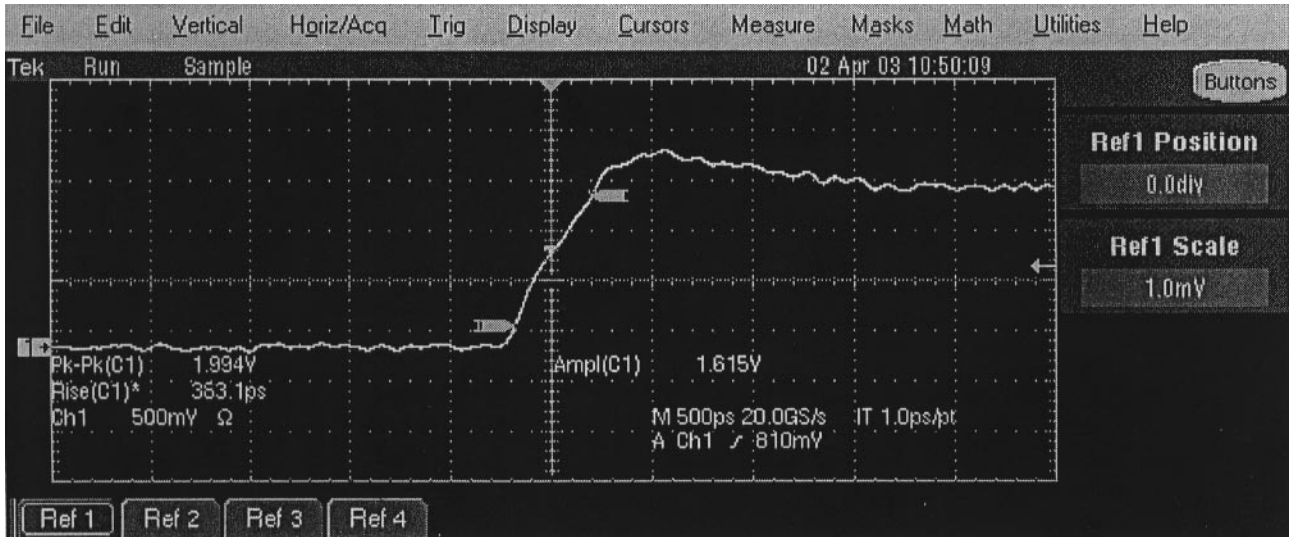


Figure 15. 360 Picosecond Rise Time Monitored in 6GHz Sampled Bandwidth Assures Measurement Integrity

(Courtesy of Michael J. Martin, Tektronix, Inc.)

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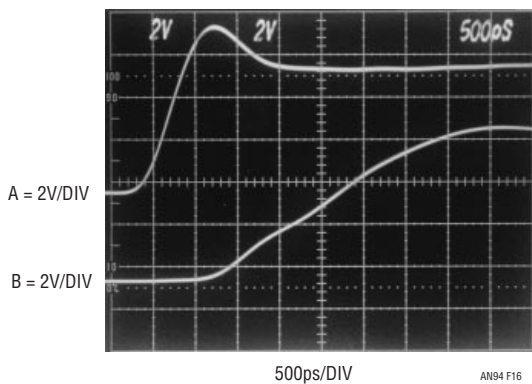


Figure 16. Trace A's 360 Picosecond Rise Time Pulse Completes Transition Before Amplifier Output (Trace B) Begins Movement. Trace A's Rise Time is Actually ≈ 150 ps Faster than Depiction, as 1GHz Measurement Bandwidth Limits Observed Response

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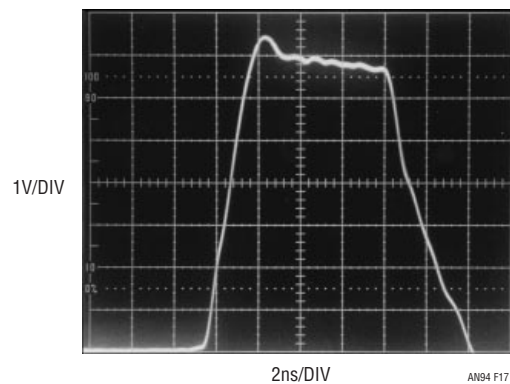


Figure 17. LT1818 Slew Response When Driven from Avalanche Pulse Generator Appears Faster Than Figure 6's 2500V/ μ s

AN94 F17

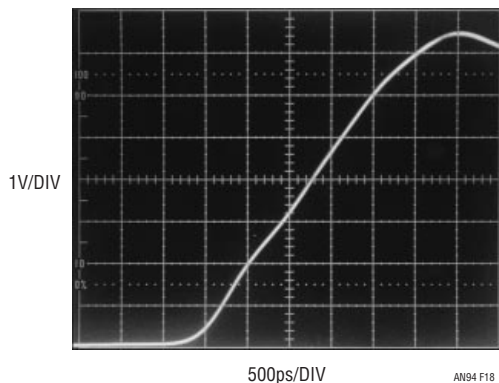


Figure 18. Time Expansion of Figure 17 Shows ≈ 2800 V/ μ s Slew Rate, Revealing 11% Error in Figure 6's 1 Nanosecond Rise Time Driven 2500V/ μ s Response

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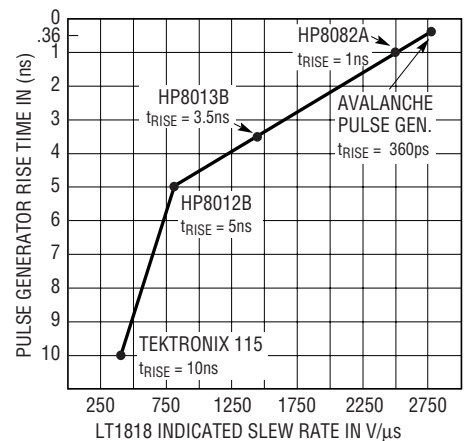


Figure 19. Figure 7's Data Restated to Include Avalanche Pulse Generator Results. Significant Slew Rate Increase is Unlikely Because Required Input Step Rise Time Approaches Zero.

AN94 F19

Application Note 94

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Note: This Application Note was derived from a manuscript originally prepared for publication in EDN magazine.

APPENDIX A

Verifying Rise Time Measurement Integrity

Any measurement requires the experimenter to insure measurement confidence. Some form of calibration check is always in order. High speed time domain measurement is particularly prone to error, and various techniques can promote measurement integrity.

Figure A1's battery-powered 200MHz crystal oscillator produces 5ns markers, useful for verifying oscilloscope time base accuracy. A single 1.5V AA cell supplies the LTC3400 boost regulator, which produces 5 volts to run the oscillator. Oscillator output is delivered to the 50Ω load via a peaked attenuation network. This provides well defined 5ns markers (Figure A2) and prevents overdriving low level sampling oscilloscope inputs.

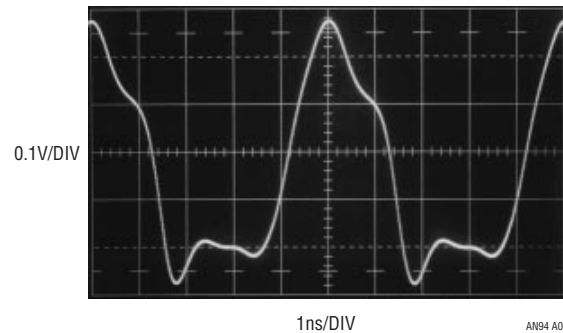


Figure A2. Time Mark Generator Output Terminated into 50Ω. Peaked Waveform is Optimal for Verifying Time Base Calibration

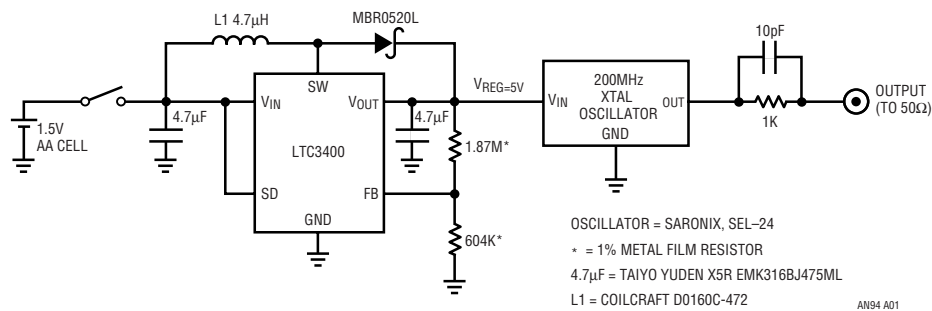


Figure A1. 1.5V Powered, 200MHz Crystal Oscillator Provides 5 Nanosecond Time Markers. Switching Regulator Converts 1.5V to 5V to Power Oscillator

MANUFACTURER	MODEL NUMBER	RISE TIME	AMPLITUDE	AVAILABILITY	COMMENTS
Avtech	AVP2S	40ps	0V to 2V	Current Production	Free Running or Triggered Operation, 0MHz to 1MHz
Hewlett-Packard	213B	100ps	≈175mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Hewlett-Packard	1105A/1108A	60ps	≈200mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Hewlett-Packard	1105A/1106A	20ps	≈200mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Picosecond Pulse Labs	TD1110C/TD1107C	20ps	≈230mV	Current Production	Similar to Discontinued HP1105/1106/8A. See above.
Stanford Research Systems	DG535 OPT 04A	100ps	0.5V to 2V	Current Production	Must be Driven with Stand-alone Pulse Generator
Tektronix	284	70ps	≈200mV	Secondary Market	50kHz Repetition Rate. Pre-trigger 75ns to 150ns Before Main Output. Calibrated 100MHz and 1GHz Sine Wave Auxiliary Outputs
Tektronix	111	500ps	≈±10V	Secondary Market	10kHz to 100kHz Repetition Rate. Positive or Negative Outputs. 30ns to 250ns Pre-trigger Output. External Trigger Input. Pulse Width Set with Charge Lines
Tektronix	067-0513-00	30ps	≈400mV	Secondary Market	60ns Pre-trigger Output. 100kHz Repetition Rate
Tektronix	109	250ps	0V to ±55V	Secondary Market	≈600Hz Repetition Rate (High Pressure Hg Reed Relay Based). Positive or Negative Outputs. Pulse Width Set by Charge Lines

Figure A3. Picosecond Edge Generators Suitable for Rise Time Verification. Considerations Include Speed, Features and Availability

Application Note 94

Once time base accuracy is confirmed it is necessary to check rise time. The lumped signal path rise time, including attenuators, connections, cables, oscilloscope and anything else, should be included in this measurement. Such “end-to-end” rise time checking is an effective way to promote meaningful results. A guideline for insuring accuracy is to have 4x faster measurement path rise time than the rise time of interest. Thus, text Figure 14’s 360 picosecond rise time measurement requires a verified 90 picosecond measurement path rise time to support it. Verifying the 90 picosecond measurement path rise time, in turn, necessitates a ≤ 22.5 picosecond rise time test step. Figure A3 lists some very fast edge generators for rise time checking.¹

The Hewlett-Packard 1105A/1106A, specified at 20 picoseconds rise time, was used to verify text Figure 14’s measurement signal path. Figure A4 indicates a 90 picosecond rise time, promoting measurement confidence.

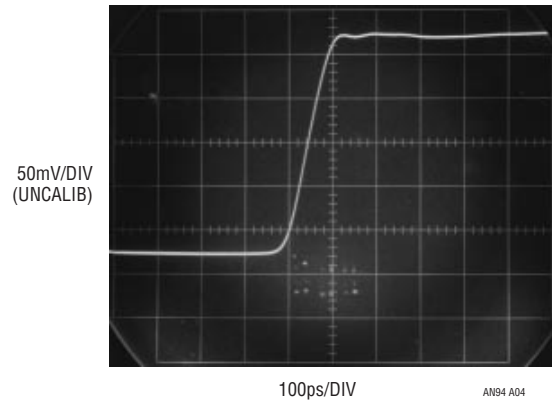


Figure A4. 20 Picosecond Step Produces ≈ 90 Picosecond Oscilloscope Rise Time, Verifying Text Figure 14’s Measurement Path Fidelity

Note 1: This is a fairly exotic group, but equipment of this caliber really is necessary for rise time verification.

APPENDIX B

Pulse Generator Output Level Shifting

The text’s avalanche pulse generator produces a positive 15V to 20V output. This is not suitable for most amplifiers. Various amplifier configurations require different forms of level shifting. A difficulty is that whatever level shift mechanism is employed must not degrade pulse rise time.

The simplest level shift is pure attenuation, facilitated by the coaxial attenuators listed in text Figure 8’s notes. These devices, well specified in the time domain, have 8 picosecond rise time. Combining these attenuators with amplifier power supplies of 8V and -2 V permitted a 6V pulse to bias the unity gain follower used in the text’s test.

In some cases the pulse must be negatively biased or inverted. Figure B1 shows ways to do this. The “bias tee” network capacitively strips the input’s DC component, re-establishing it with the potential present at the DC bias input. The inverting network, an autotransformer, magnetically accomplishes pulse inversion at unity gain. These conceptually straightforward networks are deceptively simple in appearance. Maintaining pulse fidelity and rise time at picosecond speeds involves numerous construction subtleties. The commercially available units noted in the figure are recommended.

Figure B2 shows bias tee response (trace B) to a fast input step (trace A). The output, in this case biased from -3 V, faithfully reproduces the input with only 300 picoseconds skew, primarily due to uncompensated measurement fixture delays.

Figure B3 records inverting transformer response (trace B) to trace A’s input. Rise time and fidelity are uncompromised, with about 600 picoseconds propagation delay.

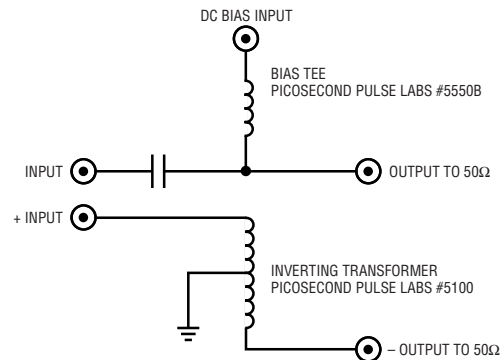


Figure B1. Output Level Shifters Include Bias Tee for DC Offsetting and Inverting Transformer for Negative Outputs. Practical Realization of Conceptually Simple Networks Requires Care to Maintain Picosecond Speed Fidelity

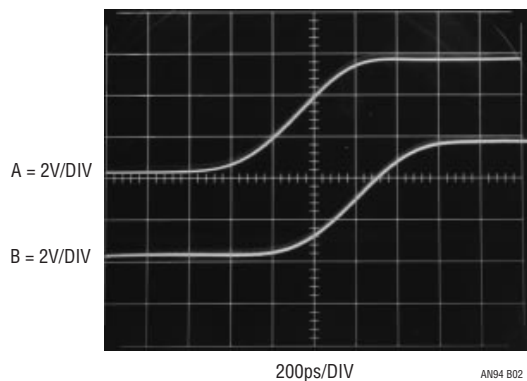


Figure B2. Bias Tee's Level Shifted Output (Trace B) Faithfully Reproduces Input (Trace A) in 3.9GHz Sampled Bandpass. 300 Picosecond Timing Skew Derives from Bias Tee and Measurement Fixture Delays

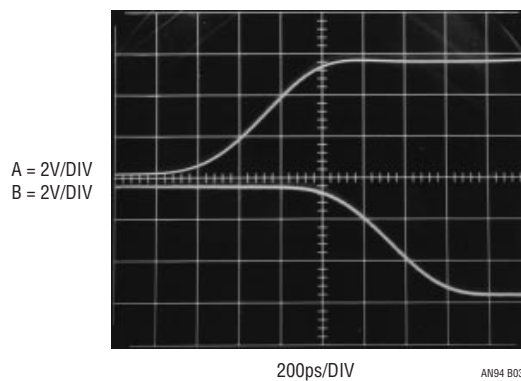


Figure B3. Wideband Pulse Transformers Output (Trace B) Inverts Input (Trace A) with Uncompromised Fidelity and 600 Picosecond Delay

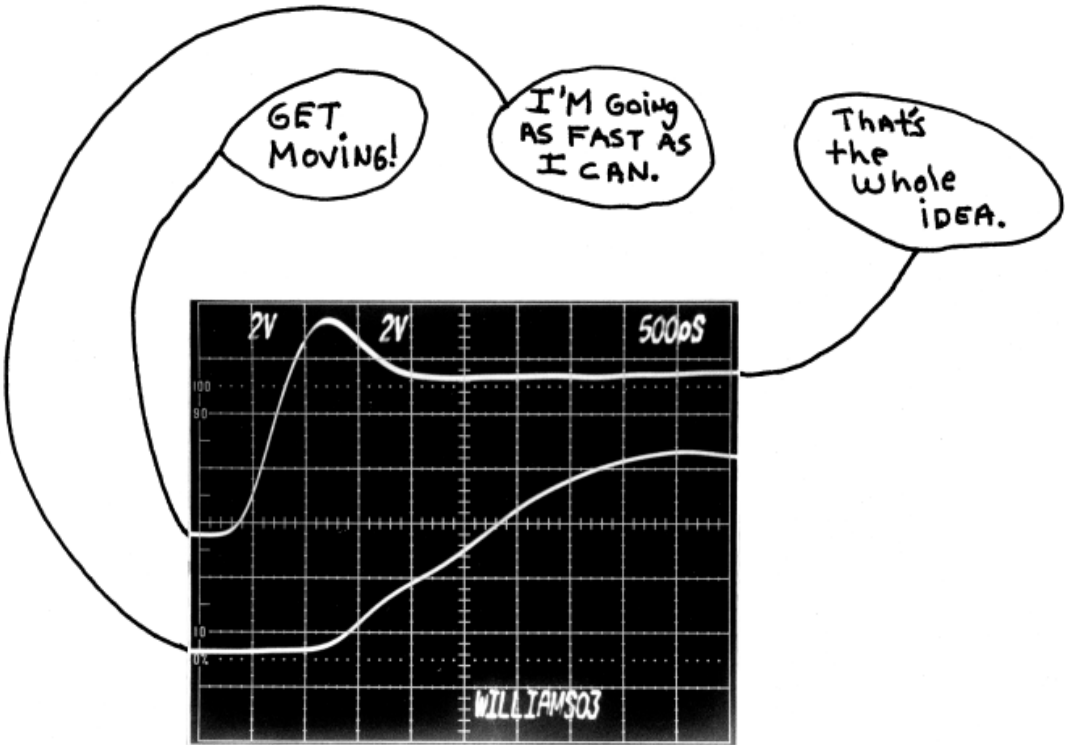
APPENDIX C

Connections, Cables, Adapters, Attenuators, Probes and Picoseconds

Subnanosecond rise time signal paths must be considered as transmission lines. Connections, cables, adapters, attenuators and probes represent discontinuities in this transmission line, deleteriously effecting its ability to faithfully transmit desired signal. The degree of signal corruption contributed by a given element varies with its deviation from the transmission lines nominal impedance. The practical result of such introduced aberrations is degradation of pulse rise time, fidelity, or both. Accordingly, introduction of elements or connections to the signal path should be minimized and necessary connections and elements must be high grade components. Any form of connector, cable, attenuator or probe must be fully specified for high frequency use. Familiar BNC hardware becomes lossy at rise times much faster than 350ps. SMA components are preferred for the rise times described in the text. Additionally, the avalanche pulse generator output cable should be 50Ω “hard line” or, at least, teflon-based coaxial cable fully specified for high frequency operation. Optimal connection practice eliminates any cable by coupling the generator output (via the necessary coaxial attenuators—see Figure 8) *directly* to the amplifier under test input. For example, replacing 18” of output cable with a direct connection improved generator rise time from 380 picoseconds to 360 picoseconds.

Mixing signal path hardware types via adapters (e.g. BNC/SMA) should be avoided. Adapters introduce significant parasitics, resulting in reflections, rise time degradation, resonances and other degrading behavior. Similarly, oscilloscope connections should be made directly to the instrument’s 50Ω inputs, avoiding probes. If probes must be used, their introduction to the signal path mandates attention to their connection mechanism and high frequency compensation. Passive “Z₀” types, commercially available in 500Ω (10x) and 5kΩ(100x) impedances, have input capacitance below 1pf. Any such probe must be carefully frequency compensated before use or misrepresented measurement will result. Inserting the probe into the signal path necessitates some form of signal pick-off which nominally does not influence signal transmission. In practice, some amount of disturbance must be tolerated and its effect on measurement results evaluated. High quality signal pick-offs always specify insertion loss, corruption factors and probe output scale factor.

The preceding emphasizes vigilance in designing and maintaining a signal path. Skepticism, tempered by enlightenment, is a useful tool when constructing a signal path and no amount of hope is as effective as preparation and directed experimentation.



Simple Circuitry for Cellular Telephone/Camera Flash Illumination

A Practical Guide for Successfully Implementing Flashlamps

Jim Williams and Albert Wu

INTRODUCTION

Next generation cellular telephones will include high quality photographic capability. Improved image sensors and optics are readily utilized, but high quality “Flash” illumination requires special attention. Flash lighting is crucial for obtaining good photographic performance and must be quite carefully considered.

Their line source light output is hundreds of times greater than point source LEDs, resulting in dense, easily diffused light over a wide area. Additionally, the flashlamp color temperature of 5500°K to 6000°K, quite close to natural light, eliminates the color correction necessitated by a white LED’s blue peaked output.

FLASH ILLUMINATION ALTERNATIVES

Two practical choices exist for flash illumination—LEDs (Light Emitting Diode) and flashlamps. Figure 1 compares various performance categories for LED and flashlamp approaches. LEDs feature continuous operating capability and low density support circuitry among other advantages. Flashlamps, however, have some particularly important characteristics for high quality photography.

FLASHLAMP BASICS

Figure 2 shows a conceptual flashlamp. The cylindrical glass envelope is filled with Xenon gas. Anode and cathode electrodes directly contact the gas; the trigger electrode, distributed along the lamp’s outer surface, does not. Gas breakdown potential is in the multikilovolt range; once breakdown occurs, lamp impedance drops to $\leq 1\Omega$. High

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PERFORMANCE CATEGORY	FLASHLAMP	LED
Light Output	High—Typically 10 to 400× Higher Than LEDs. Line Source Output Makes Even Light Distribution Relatively Simple	Low. Point Source Output Makes Even Light Distribution Somewhat Difficult
Illumination vs Time	Pulsed—Good for Sharp, Still Picture	Continuous—Good for Video
Color Temperature	5500°K to 6000°K—Very Close to Natural Light. No Color Correction Necessary	8500°K—Blue Light Requires Color Correction
Solution Size	Typically 3.5mm × 8mm × 4mm for Optical Assembly. 27mm × 6mm × 5mm for Circuitry—Dominated by Flash Capacitor (≈6.6mm Diameter; May be Remotely Mounted)	Typically 7mm × 7mm × 2.4mm for Optical Assembly, 7mm × 7mm × 5mm for Circuitry
Support Circuit Complexity	Moderate	Low
Charge Time	1 to 5 Seconds, Dependant Upon Flash Energy	None—Light Always Available
Operating Voltage and Currents	Kilovolts to Trigger, 300V to Flash. I _{SUPPLY} to Charge ≈ 100mA to 300mA, Dependant Upon Flash Energy. Essentially Zero Standby Current	Typically 3.4V to 4.2V at 30mA per LED Continuous—100mA Peak. Essentially Zero Standby Current
Battery Power Consumption	200 to 800 Flashes per Battery Recharge, Dependent Upon Flash Energy	≈120mW per LED (Continuous Light) ≈400mW per LED (Pulsed Light)

Partial Source: Perkin Elmer Optoelectronics

Figure 1. Performance Characteristics for LED and Flashlamp-Based Illumination. LEDs Feature Small Size, No Charge Time and Continuous Operating Capability; Flashlamps are Much Brighter with Better Color Temperature

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Application Note 95

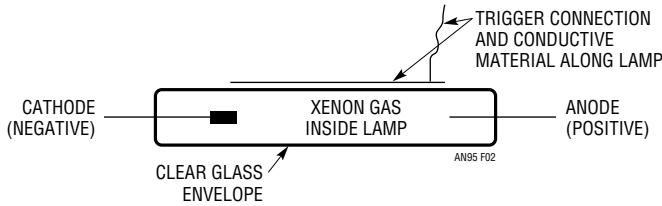


Figure 2. Flashlamp Consists of Xenon Gas-Filled Glass Cylinder with Anode, Cathode and Trigger Electrodes. High Voltage Trigger Ionizes Gas, Lowering Breakdown Potential to Permit Light Producing Current Flow Between Anode and Cathode. Distributed Trigger Connection Along Lamp Length Ensures Complete Lamp Breakdown, Resulting in Optimal Illumination

current flow in the broken down gas produces intense visible light. Practically, the large current necessary requires that the lamp be put into its low impedance state before emitting light. The trigger electrode serves this function. It transmits a high voltage pulse through the glass envelope, ionizing the Xenon gas along the lamp length. This ionization breaks down the gas, placing it into a low impedance state. The low impedance permits large current to flow between anode and cathode, producing intense light. The energy involved is so high that current flow and light output are limited to pulsed operation. Continuous operation would quickly produce extreme temperatures, damaging the lamp. When the current pulse decays, lamp voltage drops to a low point and the lamp reverts to its high impedance state, necessitating another trigger event to initiate conduction.

SUPPORT CIRCUITRY

Figure 3 diagrams conceptual support circuitry for flashlamp operation. The flashlamp is serviced by a trigger circuit and a storage capacitor that generates the high

transient current. In operation, the flash capacitor is typically charged to 300V. Initially, the capacitor cannot discharge because the lamp is in its high impedance state. A command applied to the trigger circuit results in a multikilovolt trigger pulse at the lamp. The lamp breaks down, allowing the capacitor to discharge¹. Capacitor, wiring and lamp impedances typically total a few ohms, resulting in transient current flow in the 100A range. This heavy current pulse produces the intense flash of light. The ultimate limitation on flash repetition rate is the lamp's ability to safely dissipate heat. A secondary limitation is the time required for the charging circuit to fully charge the flash capacitor. The large capacitor charging towards a high voltage combines with the charge circuit's finite output impedance, limiting how quickly charging can occur. Charge times of 1 to 5 seconds are realizable, depending upon available input power, capacitor value and charge circuit characteristics.

The scheme shown discharges the capacitor in response to a trigger command. It is sometimes desirable to effect partial discharge, resulting in less intense light flashes. Such operation permits "red-eye" reduction, where the main flash is immediately preceded by one or more reduced intensity flashes². Figure 4's modifications provide this operation. A driver and a high current switch have been added to Figure 3. These components permit

Note 1. Strictly speaking, the capacitor does not fully discharge because the lamp reverts to its high impedance state when the potential across it decays to some low value, typically 50V.

Note 2. "Red-eye" in a photograph is caused by the human retina reflecting the light flash with a distinct red color. It is eliminated by causing the eye's iris to constrict in response to a low intensity flash immediately preceding the main flash.

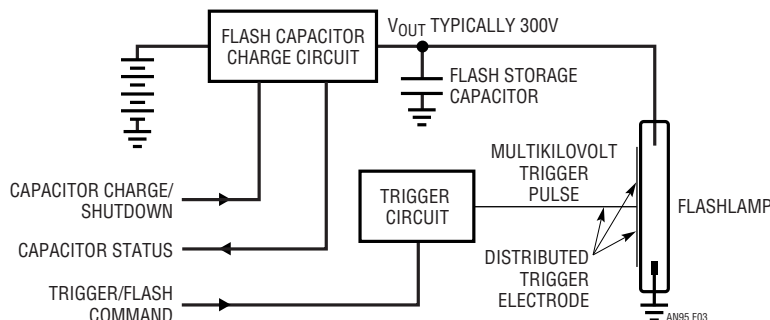


Figure 3. Conceptual Flashlamp Circuitry Includes Charge Circuit, Storage Capacitor, Trigger and Lamp. Trigger Command Ionizes Lamp Gas, Allowing Capacitor Discharge Through Flashlamp. Capacitor Must be Recharged Before Next Trigger Induced Lamp Flash Can Occur

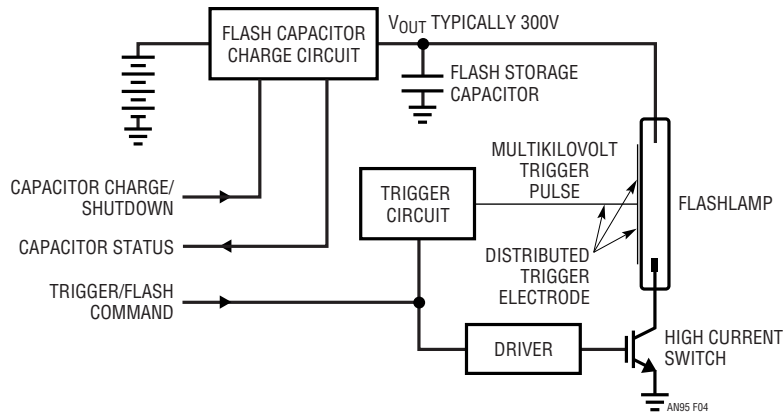


Figure 4. Driver/Power Switch Added to Figure 3 Permits Partial Capacitor Discharge, Resulting in Controllable Light Emission. Capability Allows Pulsed Low Level Light Before Main Flash, Minimizing “Red-Eye” Phenomena

stopping flash capacitor discharge by opening the lamp’s conductive path. This arrangement allows the “trigger/flash command” control line pulse width to set current flow duration, and hence, flash energy. The low energy, partial capacitor discharge allows rapid recharge, permitting several low intensity flashes in rapid succession immediately preceding the main flash without lamp damage.

FLASH CAPACITOR CHARGER CIRCUIT CONSIDERATIONS

The flash capacitor charger (Figure 5) is basically a transformer coupled step-up converter with some special capabilities³. When the “charge” control line goes high, the regulator clocks the power switch, allowing step-up transformer T1 to produce high voltage pulses. These pulses are rectified and filtered, producing the 300V DC output. Conversion efficiency is about 80%. The circuit regulates by stopping drive to the power switch when the desired output is reached. It also pulls the “DONE” line low, indicating that the capacitor is fully charged. Any capacitor leakage-induced loss is compensated by intermittent power switch cycling. Normally, feedback would be provided by resistively dividing down the output voltage. This approach is not acceptable because it would require excessive switch cycling to offset the feedback resistor’s constant power drain. While this action would maintain regulation, it would also drain excessive power from the primary source, presumably a battery. Regula-

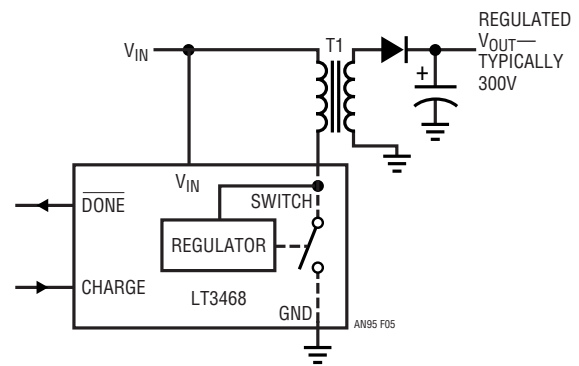


Figure 5. Flash Capacitor Charger Circuit Includes IC Regulator, Step-Up Transformer, Rectifier and Capacitor. Regulator Controls Capacitor Voltage by Monitoring T1’s Flyback Pulse, Eliminating Conventional Feedback Resistor’s Loss Path. Control Pins Include Charge Command and Charging Complete (“DONE”) Indication

tion is instead obtained by monitoring T1’s flyback pulse characteristic, which reflects T1’s secondary amplitude. The output voltage is set by T1’s turns ratio⁴. This feature permits tight capacitor voltage regulation, necessary to ensure consistent flash intensity without exceeding lamp energy or capacitor voltage ratings. Also, flashlamp energy is conveniently determined by the capacitor value without any other circuit alterations.

Note 3. Details on this device’s operation appear in Appendix A, “A Monolithic Flash Capacitor Charger.”

Note 4. See Appendix A for recommended transformers.

Application Note 95

DETAILED CIRCUIT DISCUSSION

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 6 is a complete flashlamp circuit based on the previous text discussion. The capacitor charging circuit, similar to Figure 5, appears at the upper left. D2 has been added to safely clamp T1-originated reverse transient voltage events. Q1 and Q2 drive high current switch Q3. The high voltage trigger pulse is formed by step-up transformer T2. Assuming C1 is fully charged, when Q1-Q2 turns Q3 on, C2 deposits current into T2's

primary. T2's secondary delivers a high voltage trigger pulse to the lamp, ionizing it to permit conduction. C1 discharges through the lamp, producing light.

Figure 7 details the capacitor charging sequence. Trace A, the "charge" input, goes high. This initiates T1 switching, causing C1 to ramp up (trace B). When C1 arrives at the regulation point, switching ceases and the resistively pulled-up "DONE" line drops low (trace C), indicating C1's charged state. The "TRIGGER" command (trace D), resulting in C1's discharge via the lamp-Q3 path, may occur any time (in this case $\approx 600\text{ms}$) after "DONE" goes low. Note that this figure's trigger command is lengthened for photographic clarity; it normally is $500\mu\text{s}$ to $1000\mu\text{s}$ in duration for a complete C1 discharge. Low level flash events, such as for "red-eye" reduction, are facilitated by short duration trigger input commands.

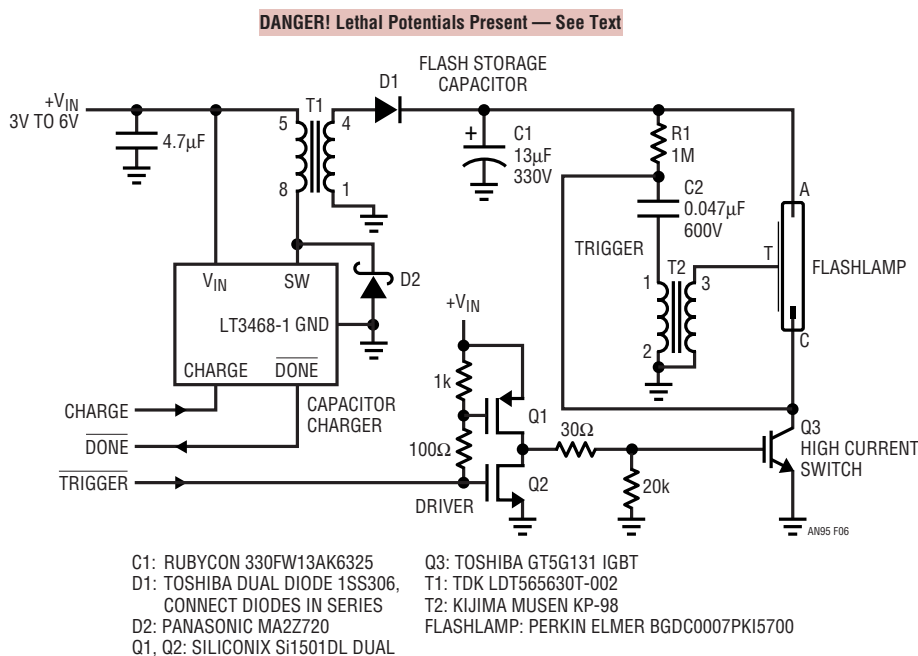


Figure 6. Complete Flashlamp Circuit Includes Capacitor Charging Components (Figure Left), Flash Capacitor C1, Trigger (R1, C2, T2), Q1-Q2 Driver, Q3 Power Switch and Flashlamp. TRIGGER Command Simultaneously Biases Q3 and Ionizes Lamp via T2. Resultant C1 Discharge Through Lamp Produces Light

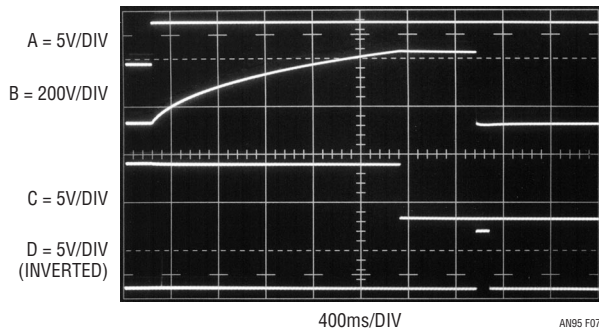


Figure 7. Capacitor Charging Waveforms Include Charge Input (Trace A), C1 (Trace B), DONE Output (Trace C) and TRIGGER Input (Trace D). C1's Charge Time Depends Upon Its Value and Charge Circuit Output Impedance. TRIGGER Input, Widened for Figure Clarity, May Occur any Time After DONE Goes Low

Figure 8 shows high speed detail of the high voltage trigger pulse (trace A) and resultant flashlamp current (trace B). Some amount of time is required for the lamp to ionize and begin conduction after triggering. Here, 10 μ s after the 8kV_{p-p} trigger pulse, flashlamp current begins its ascent to nearly 100A. The current rises smoothly in 5 μ s to a well defined peak before beginning its descent. The resultant light produced (Figure 9) rises more slowly, peaking in about 25 μ s before decaying. Slowing the oscilloscope sweep permits capturing the entire current and light events. Figure 10 shows that light output (trace B) follows lamp current (trace A) profile, although current peaking is more abrupt. Total event duration is \approx 500 μ s with most energy expended in the first 200 μ s. The leading edge's discontinuous presentation is due to oscilloscope chopped display mode operation.

LAMP, LAYOUT, RFI AND RELATED ISSUES

Lamp Considerations

Several lamp related issues require attention. Lamp triggering requirements must be thoroughly understood and adhered to. If this is not done, incomplete or no lamp flash may occur. Most trigger related problems involve trigger transformer selection, drive and physical location with respect to the lamp. Some lamp manufacturers supply the trigger transformer, lamp and light diffuser as a single, integrated assembly⁵. This obviously implies trigger transformer approval by the lamp vendor, assuming it is driven properly. In cases where the lamp is

Note 5. See Reference 1.

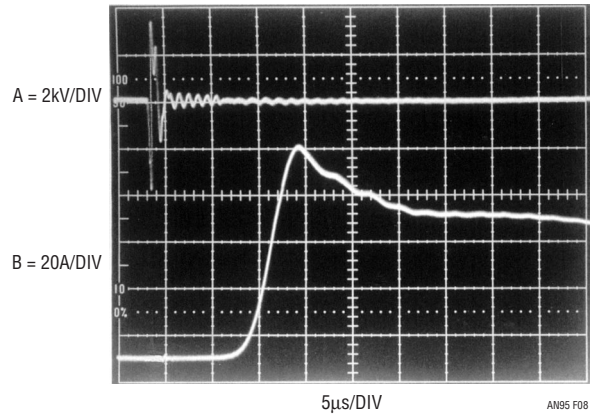


Figure 8. High Speed Detail of Trigger Pulse (Trace A) and Resultant Flashlamp Current (Trace B). Current Approaches 100A After Trigger Pulse Ionizes Lamp

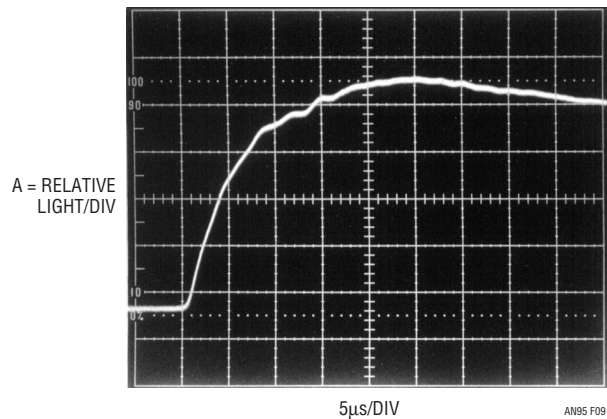


Figure 9. Smoothly Ascending Flashlamp Light Output Peaks in 25 μ s

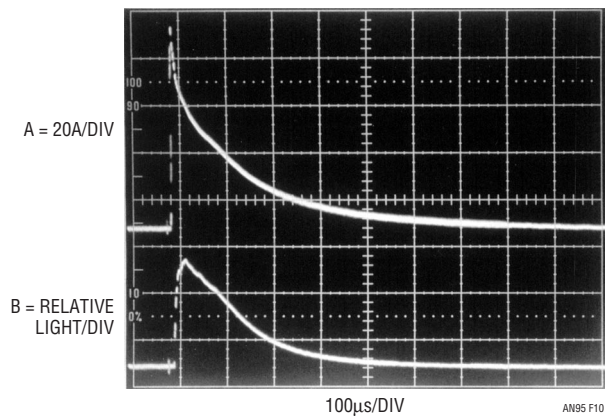


Figure 10. Photograph Captures Entire Current (Trace A) and Light (Trace B) Events. Light Output Follows Current Profile Although Peaking is Less Defined. Leading Edges Dashed Presentation Derives from Oscilloscope's Chopped Display Operation

Application Note 95

triggered with a user-selected transformer and drive scheme, it is essential to obtain lamp vendor approval before going to production.

The lamp's anode and cathode access the lamp's main discharge path. Electrode polarity must be respected or severe lifetime degradation will occur. Similarly, lamp energy dissipation restrictions must be respected or lifetime will suffer. Severe lamp energy overdrive can result in lamp cracking or disintegration. Energy is easily and reliably controlled by selecting capacitor value and charge voltage and restricting flash repetition rate. As with triggering, lamp flash conditions promoted by the user's circuit require lamp manufacturer approval before production.

Assuming proper triggering and flash energy, lamp lifetimes of ≈ 5000 flashes may be expected. Lifetime for various lamp types differs from this figure, although all are vendor specified. Lifetime is typically defined as the point where lamp luminosity drops to 80% of its original value.

Layout

The high voltages and currents mandate layout planning. Referring back to Figure 6, C1's discharge path is through the lamp, Q3 and back to ground. The $\approx 100\text{A}$ peak current means this discharge path must be maintained at low impedance. Conduction paths between C1, the lamp and Q3 should be short and well below 1Ω . Additionally, Q3's emitter and C1's negative terminal should be directly connected, the goal being a tight, highly conductive loop between C1's positive terminal, the lamp and Q3's return back to C1. Abrupt trace discontinuities and vias should be avoided as the high current flow can cause conductor erosion in local high resistivity regions. If vias must be employed they should be filled, verified for low resistance or used in multiples. Unavoidable capacitor ESR, lamp and Q3 resistances typically total 1Ω to 2.5Ω , so total trace resistance of 0.5Ω or less is adequate. Similarly, the high

current's relatively slow risetime (see Figure 8) means trace inductance does not have to be tightly controlled.

C1 is the largest component in the circuit; space considerations may make remotely mounting it desirable. This can be facilitated with long traces or wires so long as interconnect resistance is maintained within the limits stated above.

Capacitor charger IC layout is similar to conventional switching regulator practice. The electrical path formed by the IC's V_{IN} pin, its bypass capacitor, the transformer primary and the switch pin must be short and highly conductive. The IC's ground pin should directly return to a low impedance, planar ground connection. The transformer's 300V output requires larger than minimum spacing for all high voltage nodes to meet circuit board breakdown requirements. Verify board material breakdown specifications and ensure that board washing procedures do not introduce conductive contaminants. T2's multikilovolt trigger winding must connect *directly* to the lamp's trigger electrode, preferably with less than $1/4$ " of conductor. Adequate high voltage spacing must be employed. In general, what little conductor there is should not contact the circuit board. Excessive T2 output length can cause trigger pulse degradation or radio frequency interference (RFI). Modular flashlamp-trigger transformer assemblies are excellent choices in this regard.

A demonstration layout for Figure 6 appears in Figure 11. The topside component layer is shown. Power and ground are distributed on internal layers. LT3468 layout is typical of switching regulator practice previously described, although wide trace spacing accommodates T1's 300V output. The $\approx 100\text{A}$ pulsed current flows in a tight, low resistance loop from C1's positive terminal, through the lamp, into Q3 and back to C1. In this case lamp connections are made with wires, although modular flashlamp-trigger transformers allow trace-based connections⁶.

Note 6. See Reference 1.

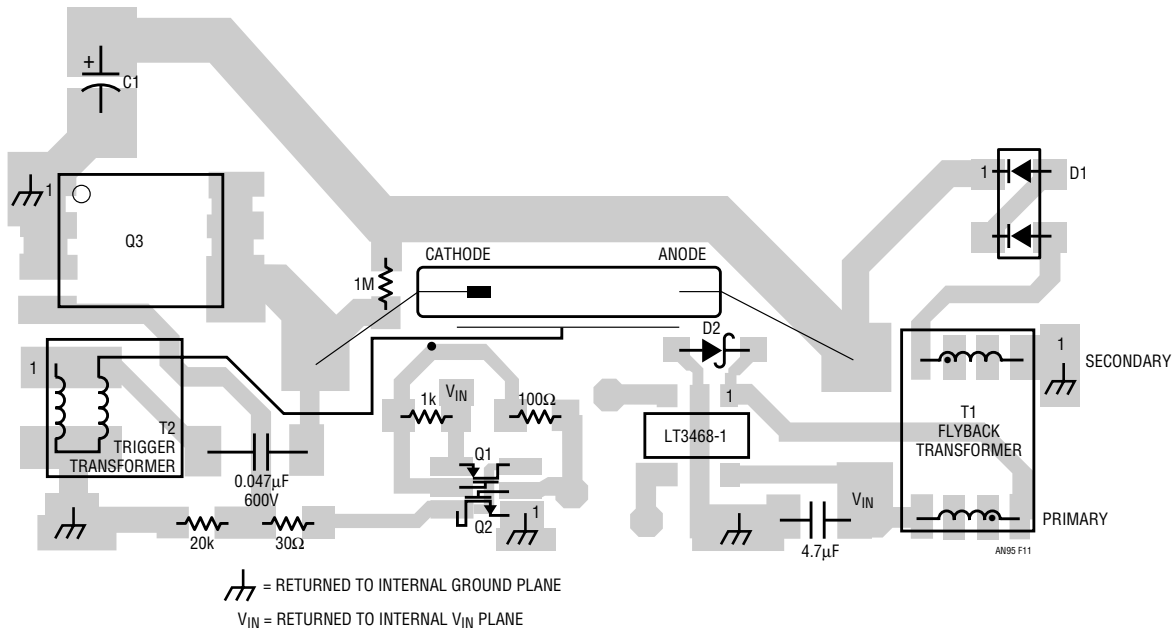


Figure 11. Magnified Demonstration Layout for Figure 6. High Current Flows in Tight Loop from C1 Positive Terminal, Through Lamp, Into Q3 and Back to C1. Lamp Connections are Wires, Not Traces. Wide T1 Secondary Spacing Accommodates 300V Output

Radio Frequency Interference

The flash circuit's pulsed high voltages and currents make RFI a concern. The capacitor's high energy discharge is actually far less offensive than might be supposed. Figure 12 shows the discharge's 90A current peak confined to a 70kHz bandwidth by its 5 μ s risetime. This means there is little harmonic energy at radio frequencies, easing this concern. Conversely, Figure 13's T2 high voltage output has a 250ns risetime ($BW \approx 1.5\text{MHz}$), qualifying it as a potential RFI source. Fortunately, the energy involved and

the exposed path length (see layout comments) are small, making interference management possible.

The simplest interference management involves placing radiating components away from sensitive circuit nodes or employing shielding. Another option takes advantage of the predictable time when the flash circuit operates. Sensitive circuitry within the telephone can be blanked during flash events, which typically last well under 1ms.

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

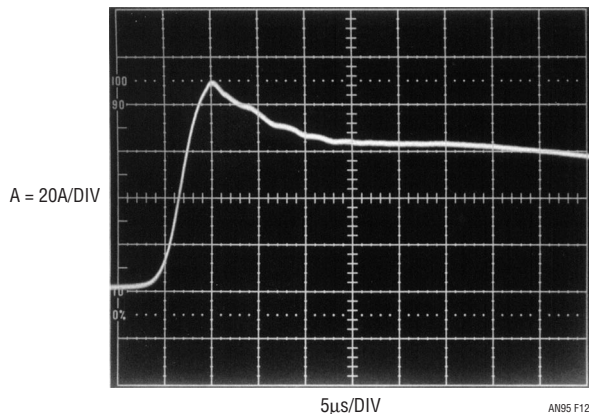


Figure 12. 90A Current Peak is Confined Within 70kHz Bandwidth by 5 μ s Risetime, Minimizing Noise Concerns

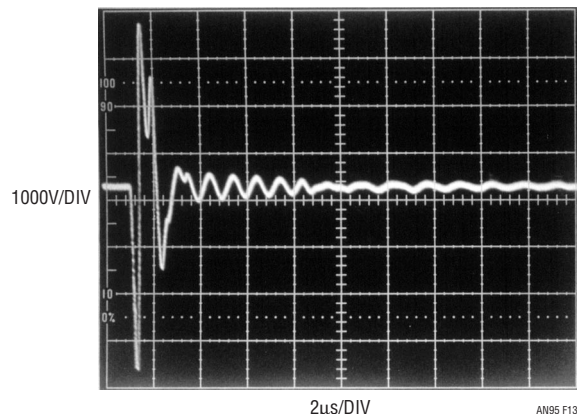


Figure 13. Trigger Pulses High Amplitude and Fast Risetime Promote RFI, but Energy and Path Exposure are Small, Simplifying Radiation Management

an95f

Application Note 95

REFERENCES

1. Perkin Elmer, "Flashtubes."
2. Perkin Elmer, "Everything You Always Wanted to Know About Flashtubes."
3. Linear Technology Corporation, "LT[®]3468/LT3468-1/LT3468-2 Data Sheet."
4. Wu, Albert, "Photoflash Capacitor Chargers Fit Into Tight Spots," Linear Technology, Vol. XIII, No. 4, December, 2003.
5. Rubycon Corporation. Catalog 2004, "Type FW Photoflash Capacitor," Page 187.

APPENDIX A

A MONOLITHIC FLASH CAPACITOR CHARGER

The LT3468/LT3468-1/LT3468-2 charge photoflash capacitors quickly and efficiently. Operation is understood by referring to Figure A1. When the CHARGE pin is driven high, a one shot sets both SR latches in the correct state. Power NPN, Q1, turns on and current begins ramping up in T1's primary. Comparator A1 monitors switch current and when peak current reaches 1.4A (LT3468), 1A (LT3468-2) or 0.7A (LT3468-1), Q1 is turned off. Since T1 is utilized as a flyback transformer, the flyback pulse on the SW pin causes A3's output to be high. SW pin voltage must be at least 36mV above V_{IN} for this to happen.

During this phase, current is delivered to the photoflash capacitor via T1's secondary and D1. As the secondary current decreases to zero, the SW pin voltage begins to collapse. When the SW pin voltage drops to 36mV above V_{IN} or lower, A3's output goes low. This fires a one shot which turns Q1 back on. This cycle continues, delivering power to the output.

Output voltage detection is accomplished via R2, R1, Q2 and comparator A2. Resistors R1 and R2 are sized so that when the SW voltage is 31.5V above V_{IN} , A2's output goes high, resetting the master latch. This disables Q1, halting

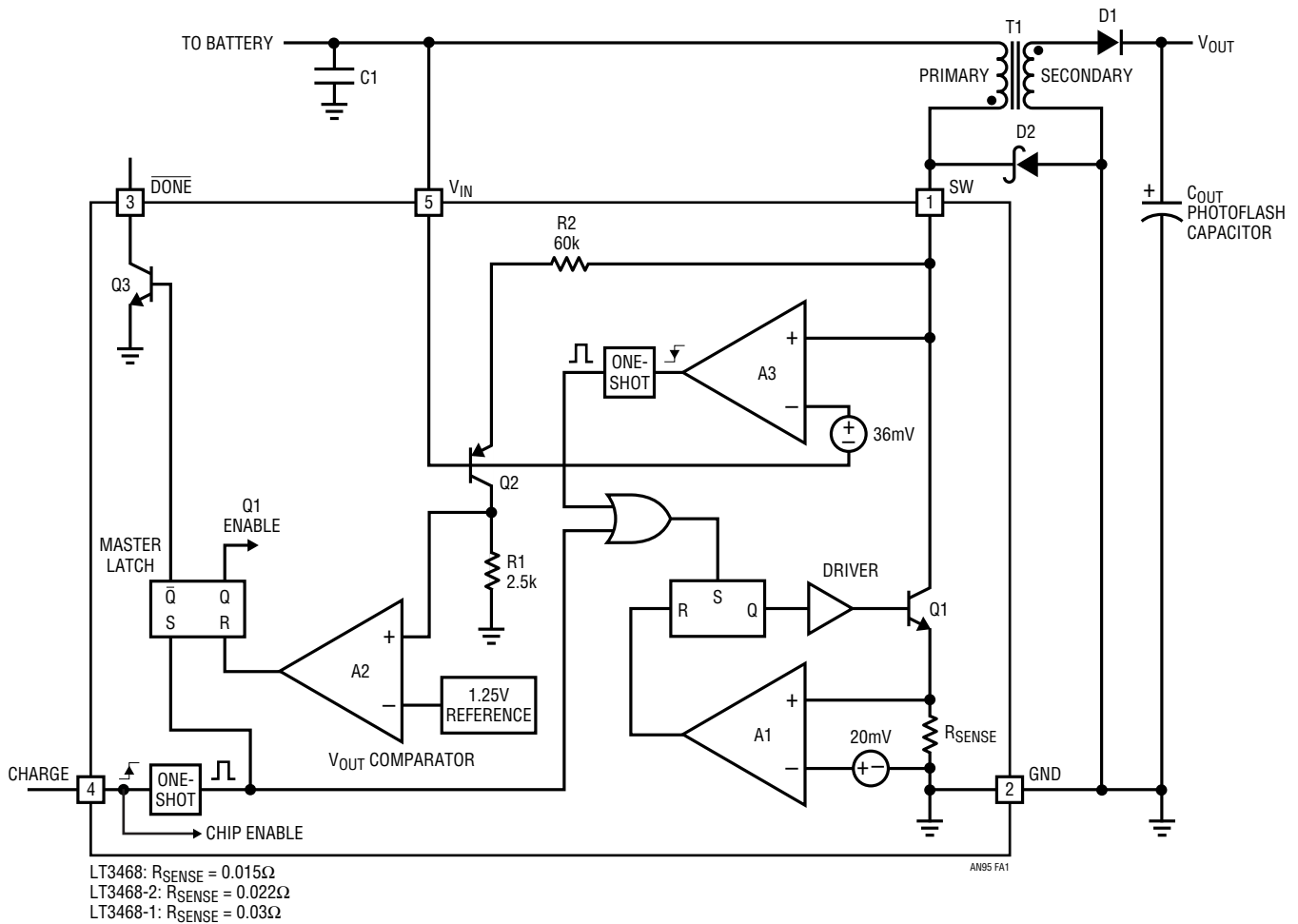


Figure A1. LT3468 Block Diagram. Charge Pin Controls Power Switching to T1. Photoflash Capacitor Voltage is Regulated by Monitoring T1's Flyback Pulse, Eliminating Conventional Feedback Resistors Loss Path

Application Note 95

power delivery. Q3 is turned on, pulling the $\overline{\text{DONE}}$ pin low, indicating the part has finished charging. Power delivery can only be restarted by toggling the CHARGE pin.

The CHARGE pin gives the user full control of the part. Charging can be halted at any time by bringing the CHARGE pin low. Only when the final output voltage is reached will the $\overline{\text{DONE}}$ pin go low. Figure A2 shows these various modes in action. When CHARGE is first brought high, charging commences. When CHARGE is brought

low during charging, the part shuts down and V_{OUT} no longer rises. When CHARGE is brought high again, charging resumes. When the target V_{OUT} voltage is reached, the $\overline{\text{DONE}}$ pin goes low and charging stops. Finally, the CHARGE pin is brought low again, the part enters shutdown and the $\overline{\text{DONE}}$ pin goes high.

The only difference between the three LT3468 versions is the peak current level. The LT3468 offers the fastest charge time. The LT3468-1 has the lowest peak current capability, and is designed for applications requiring limited battery drain. Due to the lower peak current, the LT3468-1 can use a physically smaller transformer. The LT3468-2 has a current limit between the LT3468 and the LT3468-1. Comparative plots of the three versions charge time, efficiency and output voltage tolerance appear in Figures A3, A4 and A5.

Standard off-the-shelf transformers, available for all LT3468 versions, are available and detailed in Figure A6. For transformer design considerations, as well as other supplemental information, see the LT3468 data sheet.

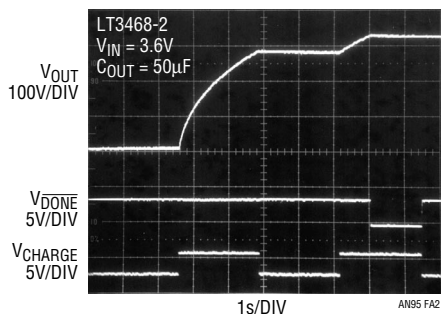


Figure A2. Halting the Charging Cycle with the CHARGE Pin

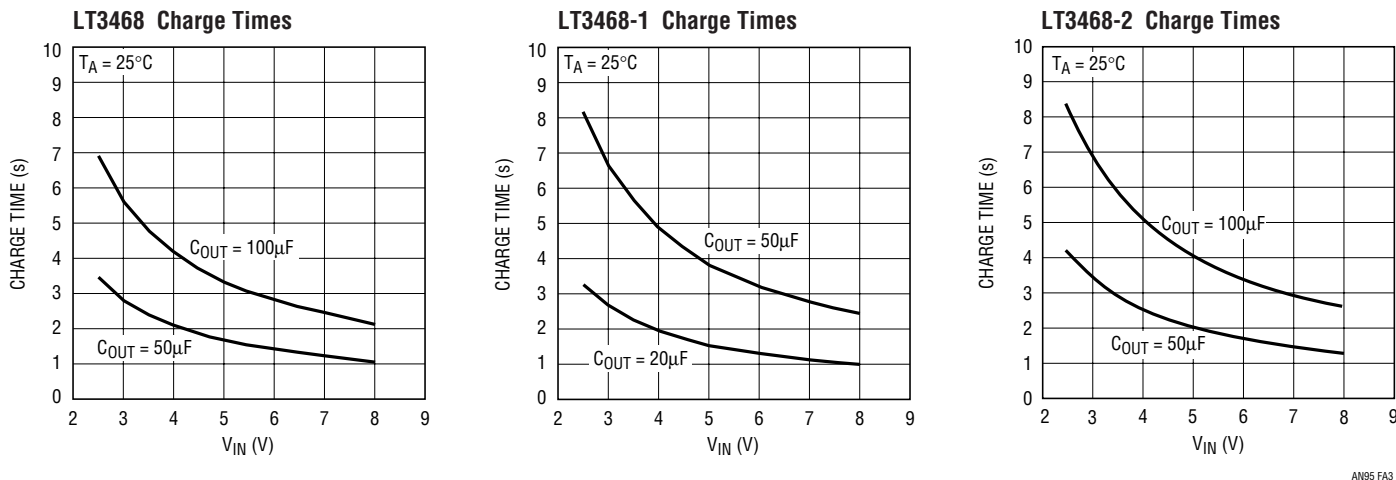
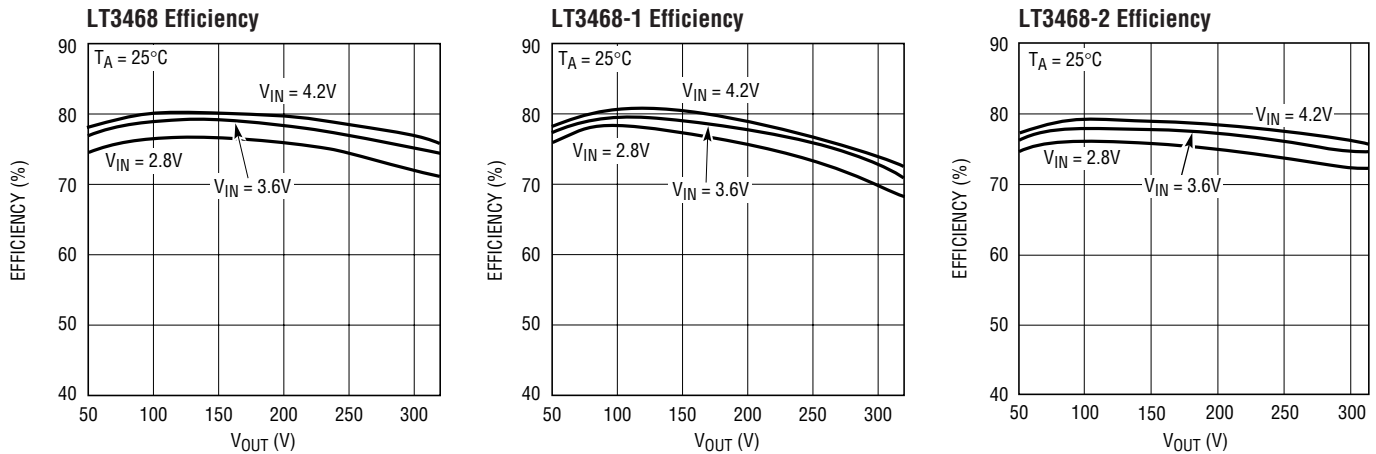
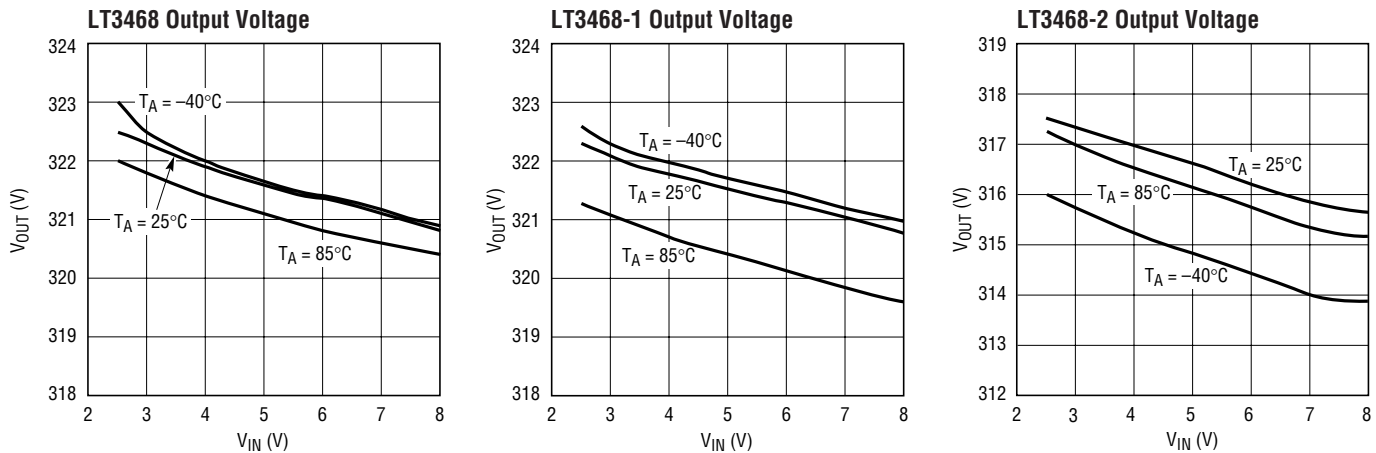


Figure A3. Typical LT3468 Charge Times. Charge Time Varies with IC Version, Capacitor Size and Input Voltage



AN95 FA4

Figure A4. Efficiency for the Three LT3468 Versions Varies with Input and Output Voltages



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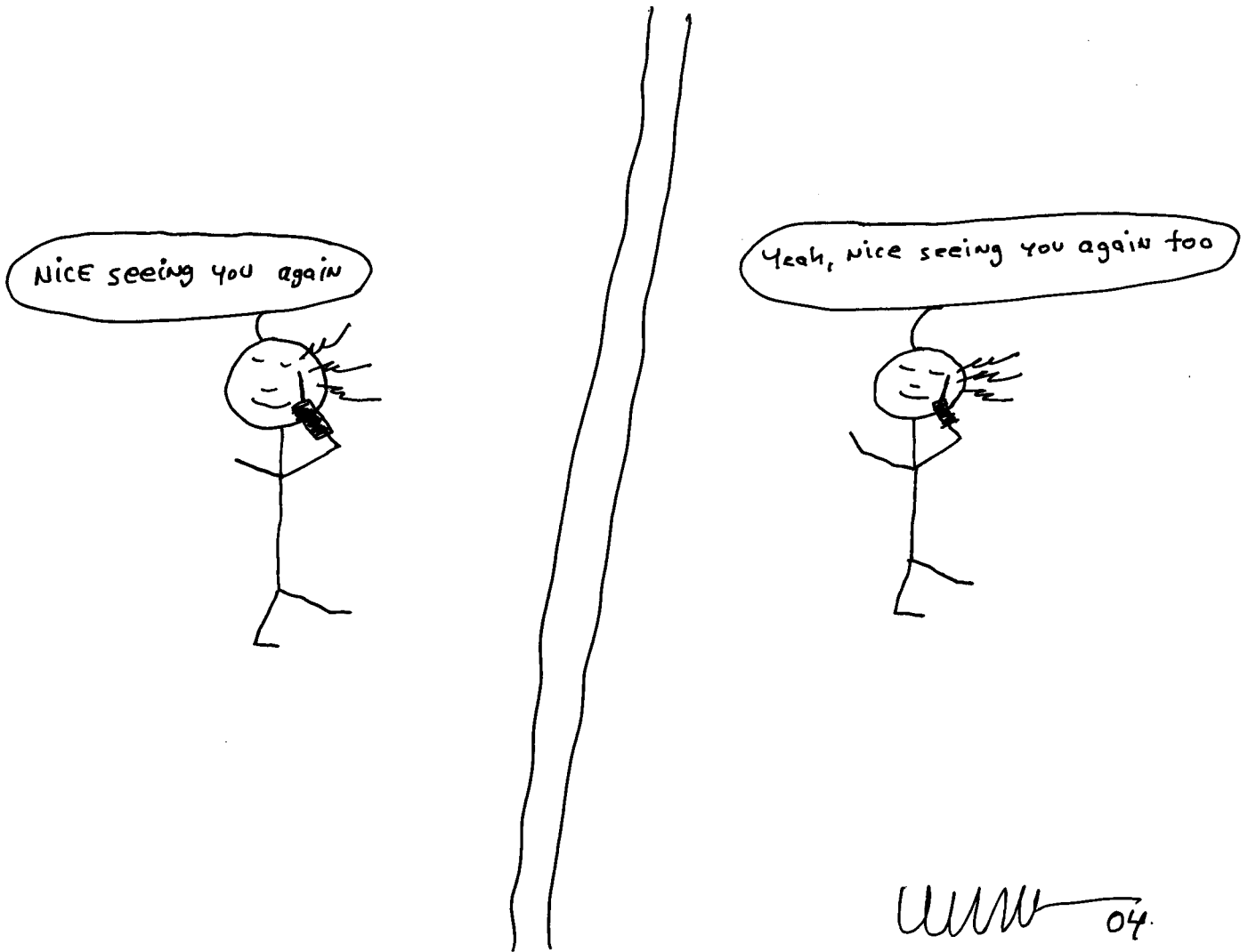
Figure A5. Typical Output Voltage Tolerance for the Three LT3468 Versions. Tight Voltage Tolerance Prevents Overcharging Capacitor, Controls Flash Energy

FOR USE WITH	TRANSFORMER NAME	SIZE (W × L × H) mm	LPRI (μH)	LPRI-LEAKAGE (nH)	N	RPRI (mΩ)	RSEC (Ω)	VENDOR
LT3468/LT3468-2 LT3468-1	SBL-5.6-1 SBL-5.6S-1	5.6 × 8.5 × 4.0 5.6 × 8.5 × 3.0	10 24	200 Max 400 Max	10.2 10.2	103 305	26 55	Kijima Musen Hong Kong Office 852-2489-8266 (ph) kijimahk@netvigator.com (email)
LT3468 LT3468-1 LT3468-2	LDT565630T-001 LDT565630T-002 LDT565630T-003	5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0	6 14.5 10.5	200 Max 500 Max 550 Max	10.4 10.2 10.2	100 Max 240 Max 210 Max	10 Max 16.5 Max 14 Max	TDK Chicago Sales Office (847) 803-6100 (ph) www.components.tdk.com
LT3468/LT3468-1 LT3468-1	T-15-089 T-15-083	6.4 × 7.7 × 4.0 8.0 × 8.9 × 2.0	12 20	400 Max 500 Max	10.2 10.2	211 Max 675 Max	27 Max 35 Max	Tokyo Coil Engineering Japan Office 0426-56-6336 (ph) www.tokyo-coil.co.jp

Figure A6. Standard Transformers Available for LT3468 Circuits. Note Small Size Despite High Output Voltage

an95f

Application Note 95



Signal Sources, Conditioners and Power Circuitry

Circuits of the Fall, 2004

Jim Williams

Introduction

Occasionally, we are tasked with designing circuitry for a specific purpose. The request may have customer origins or it may be an in-house requirement. Alternately, a circuit may be developed because its possibility is simply too attractive to ignore¹. Over time, these circuits accumulate, encompassing a wide and useful body of proven capabilities. They also represent substantial effort. These considerations make publication an almost obligatory proposition and, as such, a group of circuits is presented here. This is not the first time we have displayed such wares and, given the encouraging reader response, it will not be the last². Eighteen circuits are included in this latest effort, roughly arranged in the categories given in this publication's title. They appear at the next paragraph.

Voltage Controlled Current Source—Ground Referred Input and Output

A voltage controlled current source with ground referred input and output is difficult to achieve. Executions exist, but are often cumbersome, involving numerous components. Figure 1's conceptual design utilizes a differential amplifier featuring differential, uncommitted feedback inputs. The independent feedback inputs permit the differential signal inputs to operate anywhere inside their common mode range, unencumbered by feedback interaction. Similarly, the differential feedback ports may sense referred to any point within their common mode range. In both cases, common mode range extends from V^- to within 2V of the positive rail. Output swing extends to both rails.

The freedoms described above invite Figure 1's configuration. The amplifier is biased by a control voltage input, which feedback action impresses across the resistor. Scaling is set by the equation given, which will be recognized as a dressed version of Ohm's Law. Note that this

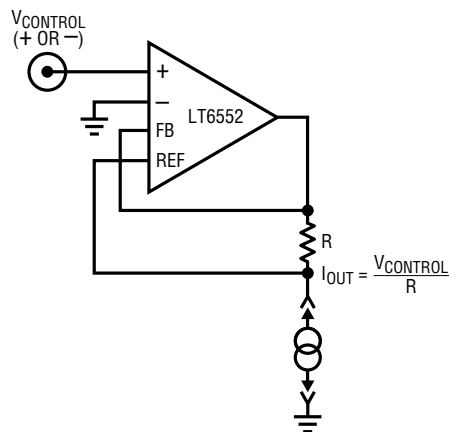


Figure 1. Conceptual Ground Referred Voltage Controlled Bipolar Current Source Utilizes Differential Amplifier's Separate Feedback Inputs. Compliance Limits are Imposed by Supply Voltage, Output Current Capacity and Input Common Mode Range

circuit will produce current outputs of either polarity, as dictated by the control input. Compliance limits are imposed by power supply voltage, output current capacity and input common mode range.

Figure 2 puts Figure 1's thesis to work. The test circuit (figure left) produces control signals to exercise the current source (figure right), which drives a capacitive load. Figure 3's waveforms describe circuit activity. Trace A is the clock, trace B A1's control input and trace C is capacitor voltage. The test circuit presents alternating polarity control inputs (trace B) after each Q1 directed capacitor reset to zero (trace C). The result, alternating, equal amplitude, opposed polarity linear capacitor ramps, clearly demonstrates the current sources capabilities.

LT, LTC and LT are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

Note 1. "When you see something technically sweet, you do it" (Robert J. Oppenheimer).

Note 2. Previous efforts of this ilk include AN45, AN52, AN61, AN66, AN67 and AN75. See References 14 to 19.

Application Note 98

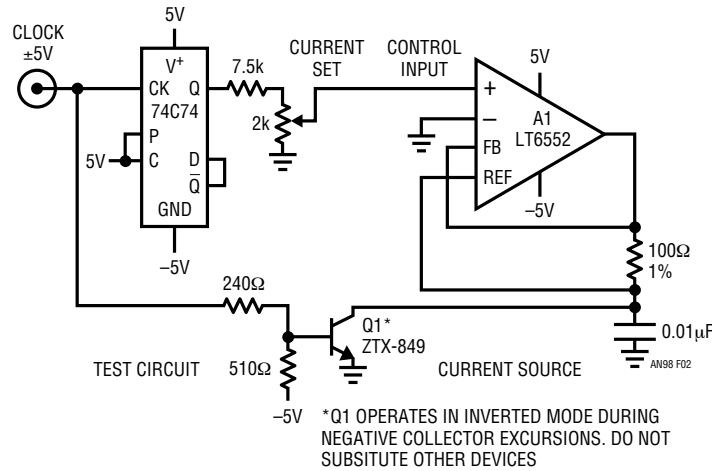


Figure 2. Practical Version of Figure 1 Sources Bipolar Current to Capacitive Load. Test Circuit Provides Bipolar Control Input and Resets Capacitor. Result is Alternating, Opposed Polarity Ramps Across Capacitor

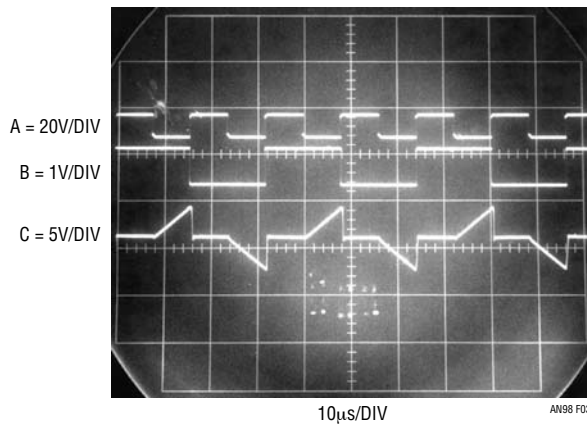


Figure 3. Voltage Controlled Current Source Test Circuit Waveforms Include Clock (Trace A), Control Input (Trace B) and Capacitor Voltage (Trace C). Bipolar Control Input Voltage Results in Complementary Capacitor Ramps

Stabilized Oscillator for Network Telephone Identification

Some telephone networks require an amplitude and frequency stabilized 100Hz carrier to indicate the status of any phone in the network. Figure 4, operating from a single 5V supply, provides this function using only two dual op amps and attendant discrete components. A1, a conventional multivibrator, operates at 100Hz. Its square and triangle outputs appear in Figure 5, traces A and B, respectively. The 100Hz triangle, heavily filtered by A2's 16Hz RC input pair, appears as a sine wave at A2's

amplified output (trace C). A2's output, in turn, is applied to A3, configured as a half wave rectifier. A3's input attenuation keeps the sine wave's negative excursions within the amplifier's input range ($V_{CM(LIMIT)} = -0.3V$). Single rail powered A3's output can't track the sine wave's negative portion; it simply saturates within millivolts of ground, producing trace D's half-wave rectified output. This output, representing A2's amplitude, is compared to a DC reference by band-limited A4-Q1. Q1's collector biases A1's power pin, closing an amplitude stabilization loop which regulates the circuit's sine wave output. Sine wave distortion, appearing in trace E, is only 4% despite

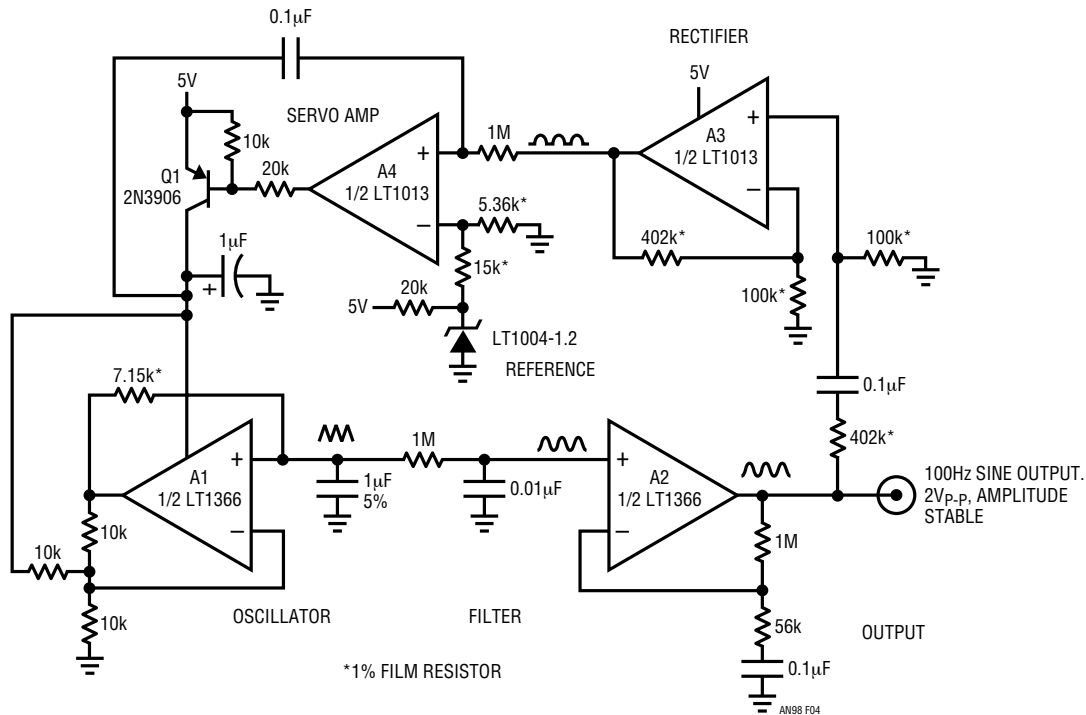


Figure 4. Amplitude/Frequency Stabilized Sine Wave Oscillator, Developed for Network Telephone Identification, Suits General Purpose Use. A1's Filtered Triangle Output Produces a 2V_{P-P} Sinewave at A2. A3's Rectified Output is Balanced Against Reference at A4. Q1 Closes Regulation Loop by Modulating A1's Power Pin

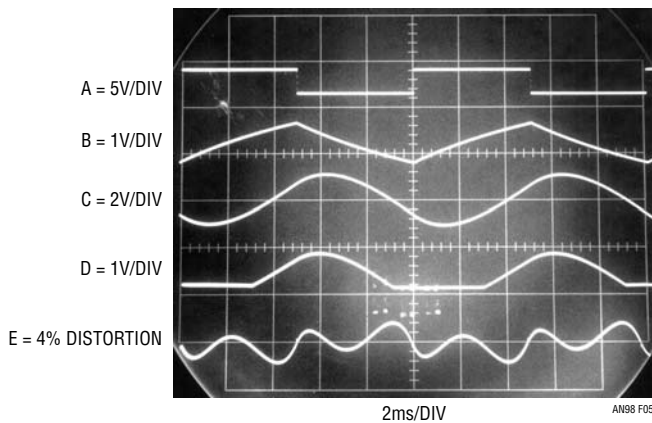


Figure 5. Figure 4's Waveforms Include A1's Square (Trace A) and Triangle (Trace B) Outputs, A2's Sinewave (Trace C), A3's Rectified Output (Trace D) and Distortion Residue (Trace E). 1M-0.01μF Filter at A2 Permits 4% Distortion, Despite Triangle Wave Infidelity

the originating triangle waves infidelity. Other specifications include less than 0.15% amplitude variation for supply shifts of 3.4V to 36V, frequency stability inside 0.01% over the same supply range and initial frequency accuracy of 6%.

Micro-Mirror Display Pulse Generator

Some "micro-mirror" displays require high voltage pulses for biasing. Pulse amplitude must be adjustable anywhere within a 0V to -50V window, with pulse top and bottom amplitude independently settable. Additionally, rise and fall times must be within 150ns into the 1500pF micro-mirror load, with absolutely no overshoot permissible. The input pulse is supplied from 5V powered positive going logic. These requirements dictate a very carefully considered level shifter.

Figure 6's circuit meets display requirements. The input pulse is applied to both sections of an LTC[®]1693 noninverting driver. The LTC1693 output reproduces the input pulse at a much lower source impedance. The LTC1693 output, referenced to the negative rail by the RC-diode combination, drives level shifter Q1. Q1, utilizing Baker clamping and base speed-up capacitance, provides wideband voltage gain with pulse amplitude set by collector and emitter supply potentials. Q1's collector capacitance is isolated by Q2-Q3. These transistors, in turn, drive output stage Q4-Q5 via a resistor. This resistor combines with Q4-Q5 input capacitance to control edge

Application Note 98

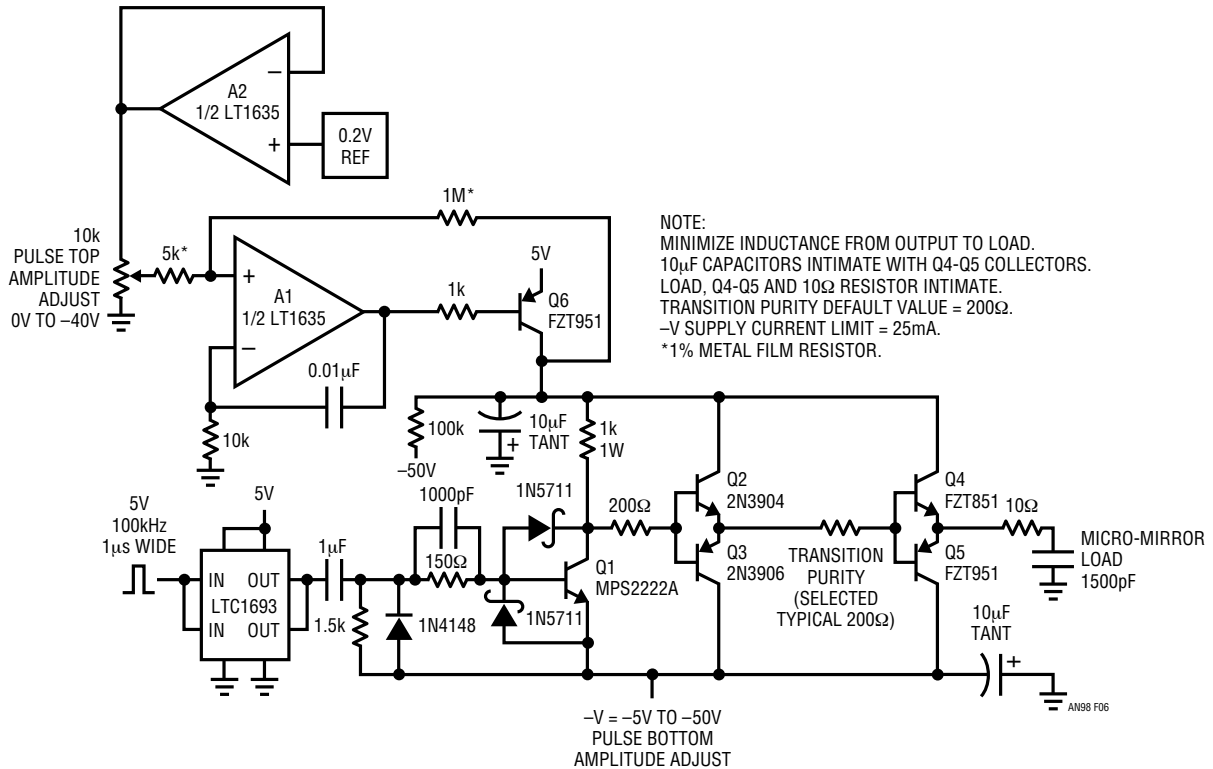


Figure 6. High Voltage, Wideband Level Shift for Micro-Mirror Biasing Precludes Overshoot. 5V Input Pulse Switches Q1 Voltage Gain Stage via LTC1693 Driver. Q2-Q3 Isolate Q1's Collector, Bias Q4-Q5 Output. A1-Q6 Regulate Pulse Top Amplitude; -V Potential Sets Pulse Bottom Voltage. Output Pulse Amplitude, Settable Anywhere Within These Limits, Has No Overshoot

times and overshoot. Its value, nominally 200Ω, will vary somewhat with layout and should be selected for best output waveform purity. Q4 and Q5, high current types, drive the capacitive load.

The 5-transistor stage swings to potentials established by Q1's emitter and collector rails³. Emitter rail voltage, hence "pulse bottom" amplitude, is set by the DC potential of its power supply, variable between -5V and -50V. The collector rail is controlled by A1, operating in the Wu configuration⁴. A1, containing an amplifier and a 0.2V reference, drives Q6 to regulate the collector rail anywhere between zero and -40V in accordance with the 10k potentiometer's setting. The settability of both power rails, combined with the transistor stages wide operating region, permits pulse amplitude control over the desired range.

Figure 7 shows the level shift output (trace B) responding to an input pulse (trace A) with amplitude limits adjusted for zero and -50V. The high voltage output transitions, occurring within 100ns, are exceptionally pure.

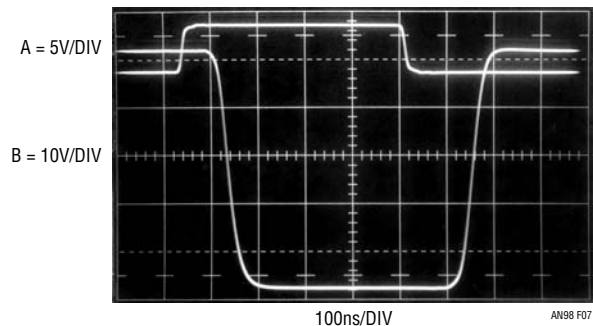


Figure 7. Level Shift Responds (Trace B) to Input Pulse (Trace A) with Amplitude Limits Adjusted for Zero and -50V. Fast, High Voltage Transitions are Exceptionally Pure

Note 3. Transistor data sheet aficionados may notice that the -50V potential exceeds Q1, Q2, Q3 V_{CE0} specifications. The transistors operate under V_{CER} conditions, where breakdown is considerably higher.

Note 4. The collector rail regulation scheme was suggested by Albert Wu of Linear Technology Corporation.

Simple Rise Time and Frequency Reference

A frequent requirement in wideband circuit work is a rise time/frequency reference. The LTC6905 oscillator provides a simple way to realize this. This device, programmable by pin strapping and a single resistor, achieves outputs over a continuous 17MHz to 170MHz range with accuracy inside 1%. Additionally, output stage transitions are typically within 500ps.

Figure 8's circuit is delightfully simple. The LTC6905 is set for 100MHz output by the pin strapping and resistor value shown. The 953Ω resistor isolates the IC's output from the

50Ω oscilloscope input and any parasitic capacitance, promoting the fastest possible transitions. Figure 9 shows circuit output in a 1GHz real-time bandwidth ($t_{RISE} = 350ps$). The 100MHz square wave displays sub-nanosecond transitions. Determining transition rise and fall times requires a faster oscilloscope⁵. Figures 10 and 11, measured in a 3.9GHz sampled bandpass, record a 400ps rise time (Figure 10) and a 320ps fall time (Figure 11).

Note 5. See Appendix A, "How Much Bandwidth is Enough?" and Appendix B, "Connections, Cables, Adapters, Attenuators, Probes and Picoseconds."

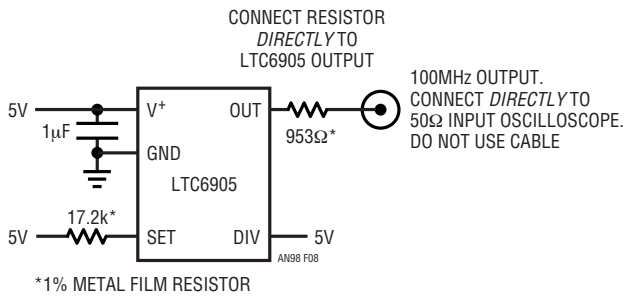


Figure 8. LTC6905 Oscillator Configured for Sub-Nanosecond Transitions and 100MHz Output is Rise Time/Frequency Reference

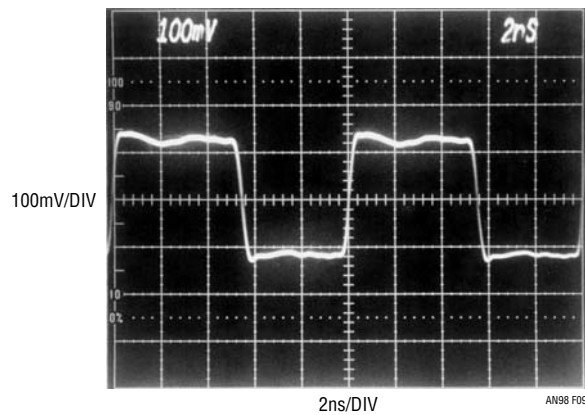


Figure 9. 100MHz Output Viewed in 1GHz Real-Time Bandwidth Displays Sub-Nanosecond Transitions

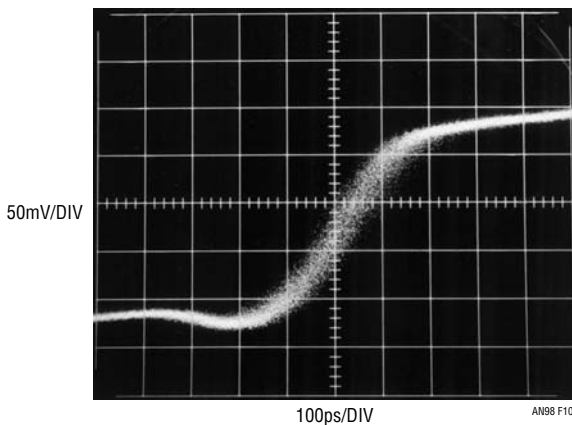


Figure 10. Transition Rise Time Measures 400ps in 3.9GHz ($t_{RISE} = 90ps$) Sampled Bandpass. Trace Granularity Derives from Sampling Oscilloscope Operation

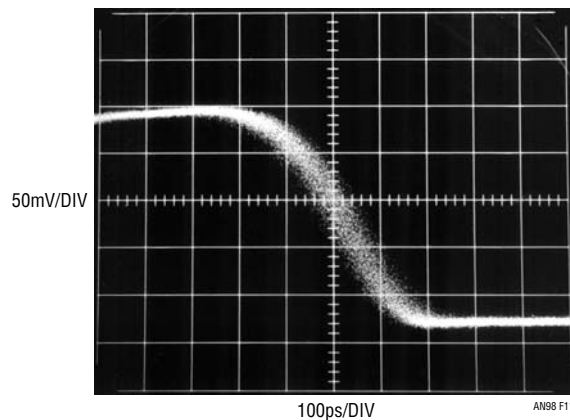


Figure 11. Transition Fall Time Measures 320ps in 3.9GHz ($t_{RISE} = 90ps$) Sampled Bandpass. Trace Granularity Derives from Sampling Oscilloscope Operation

Application Note 98

850 Picosecond Rise Time Pulse Generator with <1% Pulse Top Aberrations

Impulse response and rise time testing often require a fast rise time source with a high degree of pulse purity. These parameters are difficult to simultaneously achieve, particularly at sub-nanosecond speeds. Figure 12's circuit, derived from oscilloscope calibrators, meets these criteria, delivering an 850ps output with less than 1% pulse top aberrations.

Oscillator 01 delivers a 10MHz square wave to current mode switch Q2-Q3. Note that 01 is powered between ground and -5V to meet transistor biasing requirements. Q1 provides current drive to Q2-Q3. When 01 biases Q2, Q3 goes off. Q3's collector rises rapidly to a potential determined by Q1's collector current, D1, the resistors at the circuit's output and the 50Ω termination. When 01 goes low, Q2 turns off, Q3 comes on and the output settles to zero. D2 prevents Q3 from saturating.

The circuit's positive output transition is extremely fast and singularly clean. Figure 13, viewed in a 1GHz real-time bandwidth, shows 850ps rise time with exceptionally pure pre- and post-transition characteristics⁶. Figure 14 details pulse top settling. The photo shows the pulse-top region immediately following the positive 500mV transition.

Note 6. The measured 850ps rise time, influenced by the monitoring 1GHz oscilloscopes 350ps rise time, is almost certainly pessimistic. A root-sum-square correction applied to the measurement indicates a 775ps rise time. See Appendix A for detailed discussion.

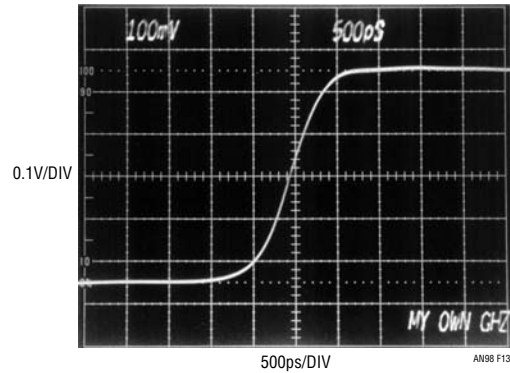


Figure 13. Figure 12's Displayed 850ps Transition Time is Free of Discontinuities when Viewed in a Real-Time 1GHz (t_{RISE} = 350ps) Bandwidth. Root-Sum-Square Correction Applied to Measurement Indicates 775ps Rise Time

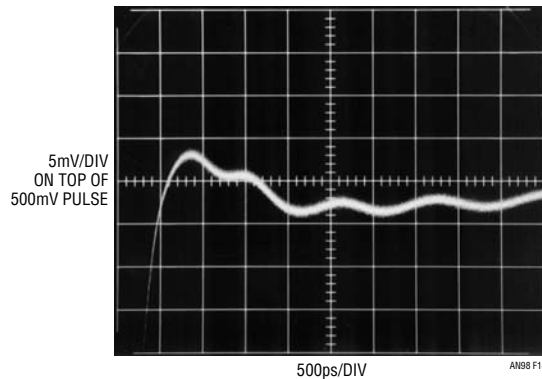


Figure 14. Pulse Top Aberrations Remain Inside 4mV Within 400ps of Transition Completion. 1GHz Ring-Off is Probably Due to Breadboard Limitations. Trace Granularity Derives from Sampling Oscilloscope Operation

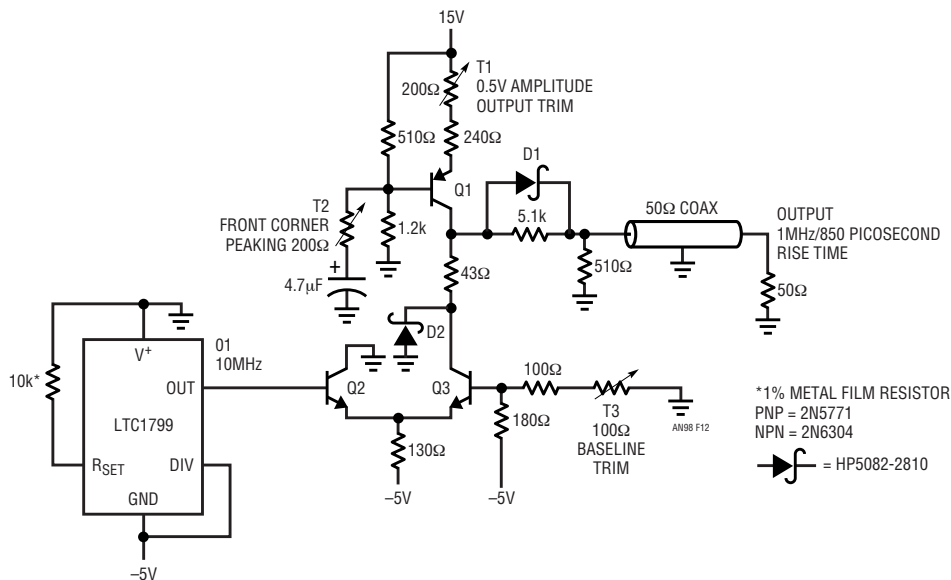


Figure 12. Oscillator 01 Drives Q2-Q3 Current Mode Switch, Producing 850ps Rise Time Output. Trims Facilitate Clean Transition with <1% Pulse Top Aberrations

Settling occurs within 400ps of the edge's completion, with all undesired activity within $\pm 4\text{mV}$. The 1mV, 1GHz ring-off is probably due to breadboard construction limitations, and could be eliminated with stripline layout techniques.

This level of performance requires trimming. The oscilloscope used should have at least 1GHz of bandwidth. T2 and T3 are adjusted for best pulse presentation while T1 sets 500mV output amplitude across the 50Ω termination. The trims are somewhat interactive, although not unduly so, converging quickly to give the results noted.

20 Picosecond Rise Time Pulse Generator

Figure 15, another fast rise time pulse generator, switches a high grade, commercially produced tunnel diode mount to produce a 20ps rise time pulse. O1's clocking (trace A, Figure 16) causes Q1's collector (trace B) to switch the capacitively loaded Q2-Q3 current source. The resultant repetitive ramp at Q3's collector (trace C), buffered by Q4, biases the tunnel diode mount via the output resistors. The tunnel diode driven output (trace D) follows the ramp until abruptly rising (trace D, just prior to 4th vertical division). This departure is caused by tunnel diode triggering. The edge associated with this triggering is extremely steep, with a specified rise time of 20ps and clean settling. Figure 17 examines this edge within the limitations of a 3.9GHz ($t_{\text{RISE}} = 90\text{ps}$) sampling oscilloscope. The trace shows the tunnel diode's switching, driving the oscilloscope to its

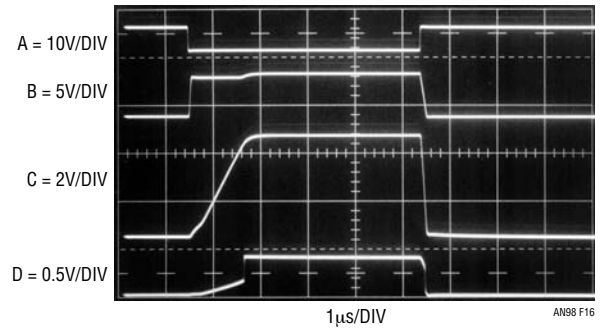


Figure 16. O1 (Trace A) Clocks Q1's Collector (Trace B), Switching Capacitively Loaded Q2-Q3 Current Source. Resultant Repetitive Ramp at Q3's Collector (Trace C), Buffered by Q4, Biases Tunnel Diode via Output Resistors. Tunnel Diode Output (Trace D) Follows Ramp Until Abruptly Triggering

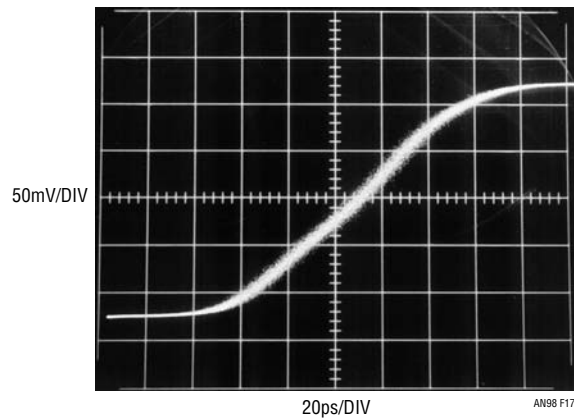


Figure 17. Figure 15's 20ps Edge Drives a 3.9GHz Sampling 'Scope to its 90ps Rise Time Limit. Trace Granularity is Characteristic of Sampling Oscilloscope Display

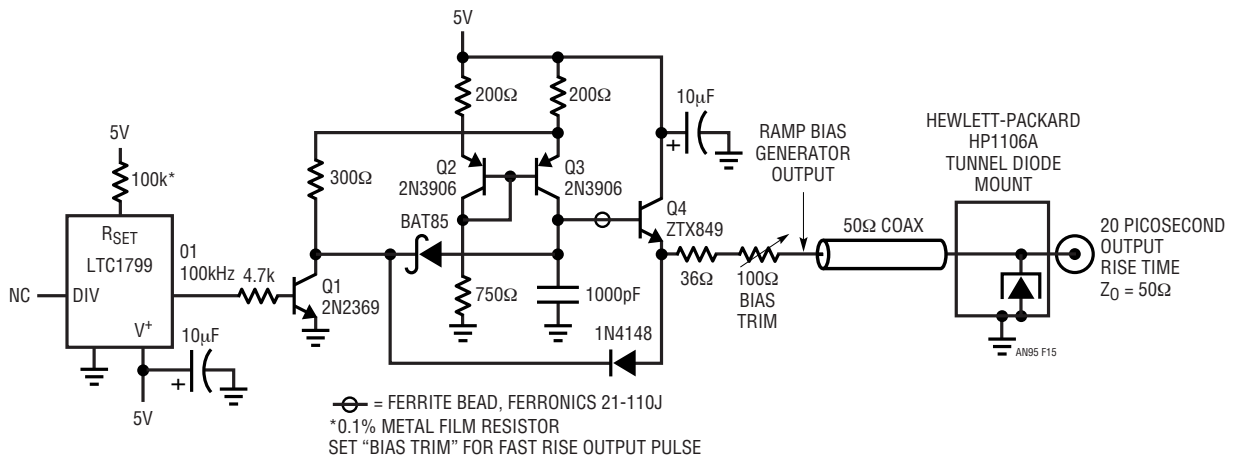


Figure 15. Current Ramps Into Tunnel Diode Until Switching Occurs, Producing a 20ps Edge. Q1, Squarewave Clocked from O1, Switches Q2-Q3 Capacitively Loaded Current Source, Producing Repetitive Ramps at Q4. Ascending Current Through Output Resistors Triggers Tunnel Diode

Application Note 98

90ps rise time limit⁷. Figure 18, slowing sweep speed to 100ps/division, shows pulse top settling (in a 3.9GHz bandwidth) within 4% inside 100ps⁸.

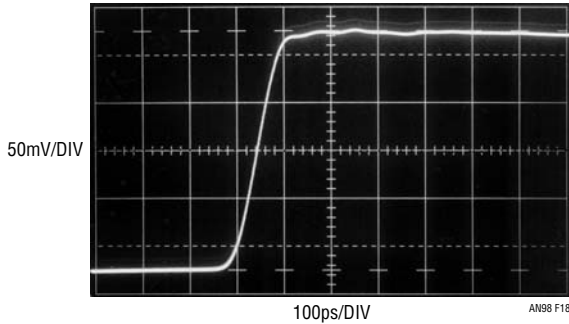


Figure 18. Reducing Sweep Speed Shows 4% Pulse Top Flatness Within Oscilloscope's 3.9GHz ($t_{RISE} = 90ps$) Bandwidth

Nanosecond Pulse Width Generator

The previous three circuits were optimized for fast rise time. It is sometimes desirable to produce extremely short width pulses in response to an input trigger. Such a predictable, programmable short time interval generator has broad use in fast pulse circuitry, particularly in sampling applications⁹. Figure 19, built around a quad high speed comparator and a fast gate, has a settable 0ns to 10ns output width with 520ps, 5V transitions. Pulse width varies less than 100ps with 5V supply variations of $\pm 5\%$. Minimum input trigger width is 30ns and input-output delay is 18ns¹⁰.

The input pulse (Figure 20, trace A) is inverted by C1, which also isolates the 50 Ω termination. C1's output drives

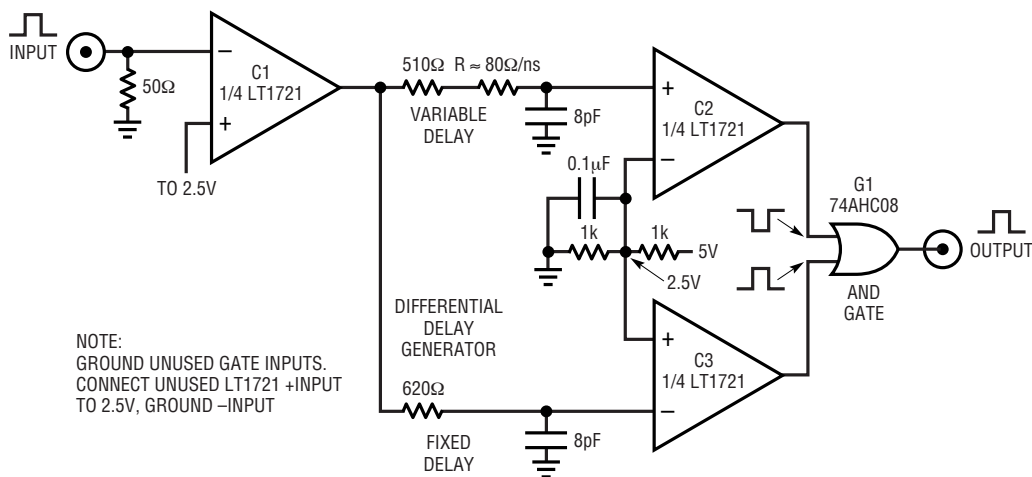


Figure 19. Pulse Generator Has 0ns to 10ns Width, 520ps Transitions. C1 Unloads Termination, Drives Differential Delay Network. C2-C3 Complementary Outputs Represent Delay Difference as Edge Timing Skew. G1, High During C2-C3 Positive Overlap, Presents Circuit Output

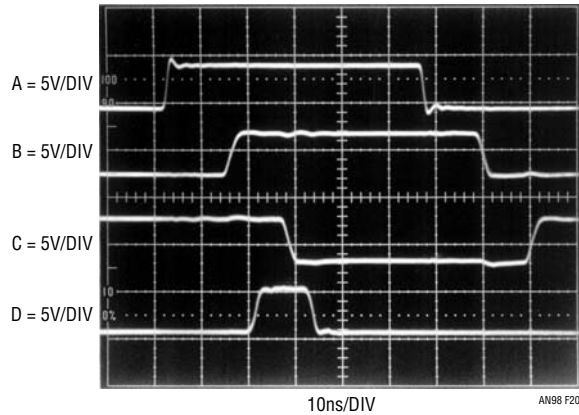


Figure 20. Pulse Generator Waveforms, Viewed in 400MHz Real-Time Bandwidth, Include Input (Trace A), C3 (Trace B) Fixed and C2 (Trace C) Variable Outputs. Circuit Output Pulse is Trace D. RC Network's Differential Delay Manifests as C2-C3 Positive Overlap. G1 Extracts This Interval, Presents Output

fixed and variable RC networks. The networks charge time difference, and hence delay, is primarily determined by programming resistor R, at a scale factor $\approx 80\Omega/ns$. C2 and C3, arranged as complementary output level detec-

Note 7. Sorry, but 3.9GHz is the fastest 'scope in my house. See Appendix A for relevant comment.

Note 8. The HP1106 is no longer produced, although available on the secondary market. The TD1107, currently manufactured by Picosecond Pulse Labs, is an equivalent unit, although we have no experience with it.

Note 9. Pedestrian laboratory argot for interval generator is "one-shot."

Note 10. This circuit is a considerably improved extension of earlier work. See References 4 and 5.

tors, represent the network's delay difference as edge time skew. Trace B is C3's ("fixed") output and trace C is C2's ("variable") output. Gate G1's output (trace D), high during C2-C3 positive overlap, presents the circuit's output pulse. Figure 21 shows a 5V, 5ns width (measured at 50% amplitude) output pulse with $R = 390\Omega$. The pulse is clean, with well defined transitions. Post-transition aberrations, within 8%, derive from G1's bond wire inductance and an imperfect coaxial probing path. Figure 22 shows the narrowest full amplitude (5V) pulse obtainable. Width measures 1ns at the 50% amplitude point and 1.7ns at the base in a 3.9GHz bandwidth. Shorter widths are obtainable if partial amplitude pulses are acceptable. Figure 23 shows a 3.3V, 700ps width (50%) with a 1.25ns base. G1's rise time limits minimum achievable pulse width. Figure 24, taken in a 3.9GHz sampled bandpass, measures 520ps rise time. Fall time is similar. Fall time is similar.

Single Rail Powered Amplifier with True Zero Volt Output Swing

Many single supply powered applications require amplifier output swings within millivolt or even sub-millivolt levels of ground. Amplifier output saturation limitations normally preclude such operation. Figure 25's power supply bootstrapping scheme achieves the desired characteristics with minimal component addition¹¹.

A1, a chopper stabilized amplifier, has a clock output. This output switches Q1, providing drive to the diode-capacitor charge pump. The charge pump output feeds A1's V^- terminal, pulling it below zero, permitting output swing to (and below) ground. If desired, the negative output excursion can be limited by either clamp option shown.

Note 11. See Reference 8, Appendix D.

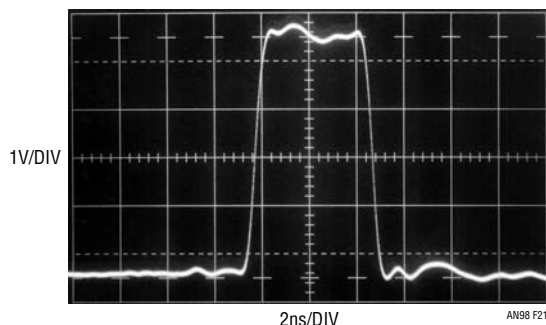


Figure 21. 5ns Wide Output with $R = 390\Omega$ is Clean, with Well Defined Transitions. Post-Transition Aberrations, Within 8%, Derive from G1 Bond Wire Inductance and Imperfect Coaxial Probe

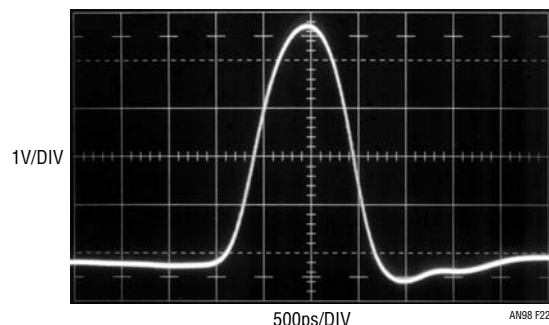


Figure 22. Narrowest Full Amplitude Pulse Width is 1ns; Base Width Measures 1.7ns. Measurement Bandwidth is 3.9GHz

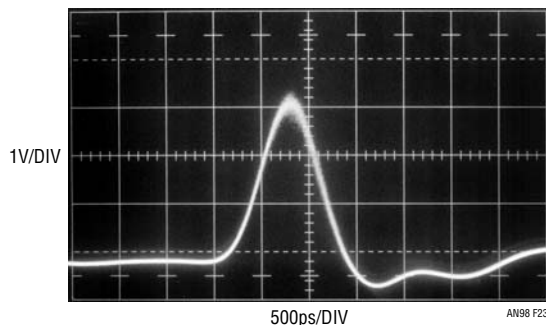


Figure 23. Partial Amplitude Pulse, 3.3V High, Measures 700ps Width with 1.25ns Base. Trace Granularity is Artifact of 3.9GHz Sampling Oscilloscope Operation

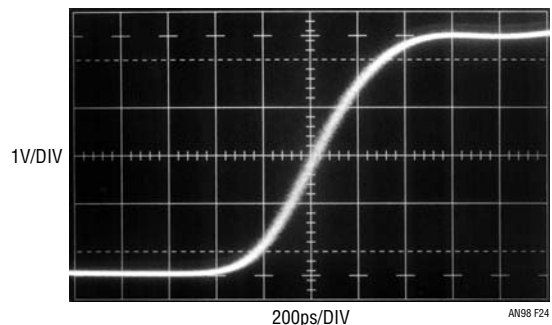


Figure 24. Transition Detail in 3.9GHz Bandpass ($t_{RISE} = 90ps$) Shows 520ps Rise Time. Fall Time is Similar. Trace Granularity Derives from Sampling Oscilloscope Operation

Application Note 98

Reliable start-up of this bootstrapped power supply scheme is a valid concern, warranting investigation. In Figure 26, the amplifier's V^- pin (trace C) initially rises at supply turn-on (trace A) but heads negative when amplifier clocking (trace B) commences at about midscreen.

The circuit provides a simple way to obtain output swing to zero volts, permitting a true “live at zero” output.

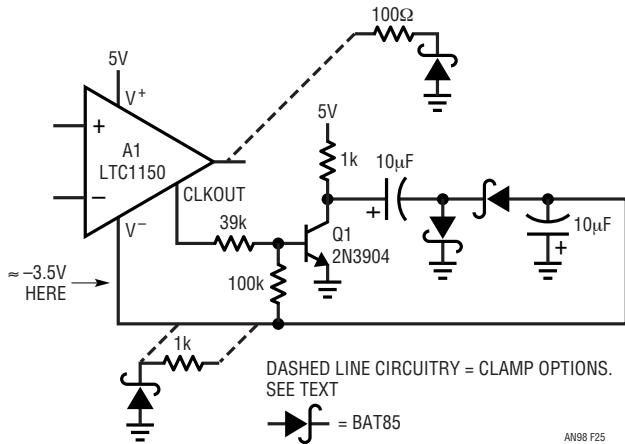


Figure 25. Single Rail Powered Amplifier Has True Zero Volt Output Swing. A1's Clock Output Switches Q1, Driving Diode-Capacitor Charge Pump. A1's V^- Pin Assumes Negative Voltage, Permitting Zero (and Below) Volt Output Swing

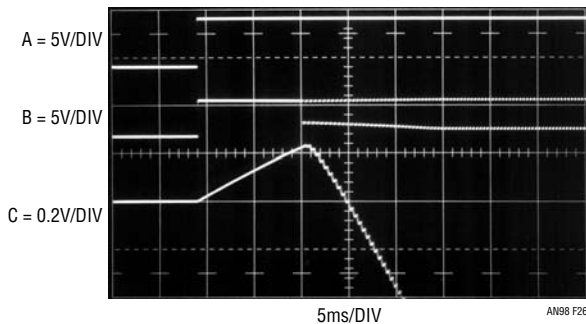


Figure 26. Amplifier Bootstrapped Supply Start-Up. Amplifier V^- Pin (Trace C) Initially Rises Positive at 5V Supply (Trace A) Turn-On. When Amplifier Internal Clock Starts (Trace B, 5th Vertical Division), Charge Pump Activates, Pulling V^- Pin Negative

Milliohmmeter

Resistance measurement of contacts, PC traces and vias requires a low resistance ohmmeter. Figure 27's 9V battery-powered design has a 1Ω full-scale range, with

resolution down to $1\text{m}\Omega$. It produces a 0V to 1V output for a 0Ω to 1Ω resistance at its 4-terminal Kelvin sensed input with 0.1% accuracy over a 5.25V to 9.5V power supply range. An AC carrier modulation scheme is employed to reject noise and error inducing DC offsets due to parasitic thermocouples (Seebeck effect)¹².

A1 and associated components form a 10mA current source that is alternately steered between Rx, the unknown resistance, and ground by LTC6943 switch pins 10, 11 and 12. The LTC6943's control pin (Pin 14) is clocked at $\approx 45\text{Hz}$ from the CD4024 divider output. This action causes a carrier modulated 10mA current flow through Rx. Rx's value determines the resultant AC voltage across it. This AC signal is capacitively coupled to LTC6943 switch pins 1, 4 and 5, driven synchronously with the current source modulation. These pins switching forms a synchronous rectifier, demodulating the AC signal back to DC across A2's input capacitor. A2 amplifies this DC potential at a gain of 1mV per milliohm, or 1V full scale. Note that single-rail powered A2's output can swing to true “zero” because it utilizes a variant of the supply bootstrapping scheme presented back in Figure 25. A2's clock output drives Q2, which pulses the CD4024 divider. One divider output switches the LTC6943 modulator-demodulator while another output drives the bootstrapped charge pump to supply A2's V^- pin with about -7V .

Diode clamps prevent accidental overvoltage at the probe inputs without introducing loading error to the 10mV maximum Rx carrier waveform. Circuit calibration involves placing a 1Ω , 0.1% resistor at Rx and adjusting the 200Ω trimmer for $1.000\text{V}_{\text{OUT}}$. The synchronously demodulated AC carrier technique displays the inherent narrow band noise rejection characteristics of “lock-in” type measurements. Figure 28 shows a normal waveform across Rx for $R_x = 1\Omega$. The 10mV signal is clean, and circuit output reads 1.000V. In Figure 29 noise is deliberately injected into the Rx probes, burying the carrier in a $6\times$ noise-to-signal ratio. Despite this, circuit output remains at 1.000V.

Note 12. This circuit's operation is derived from the Hewlett-Packard HP-4328A. See Reference 7.

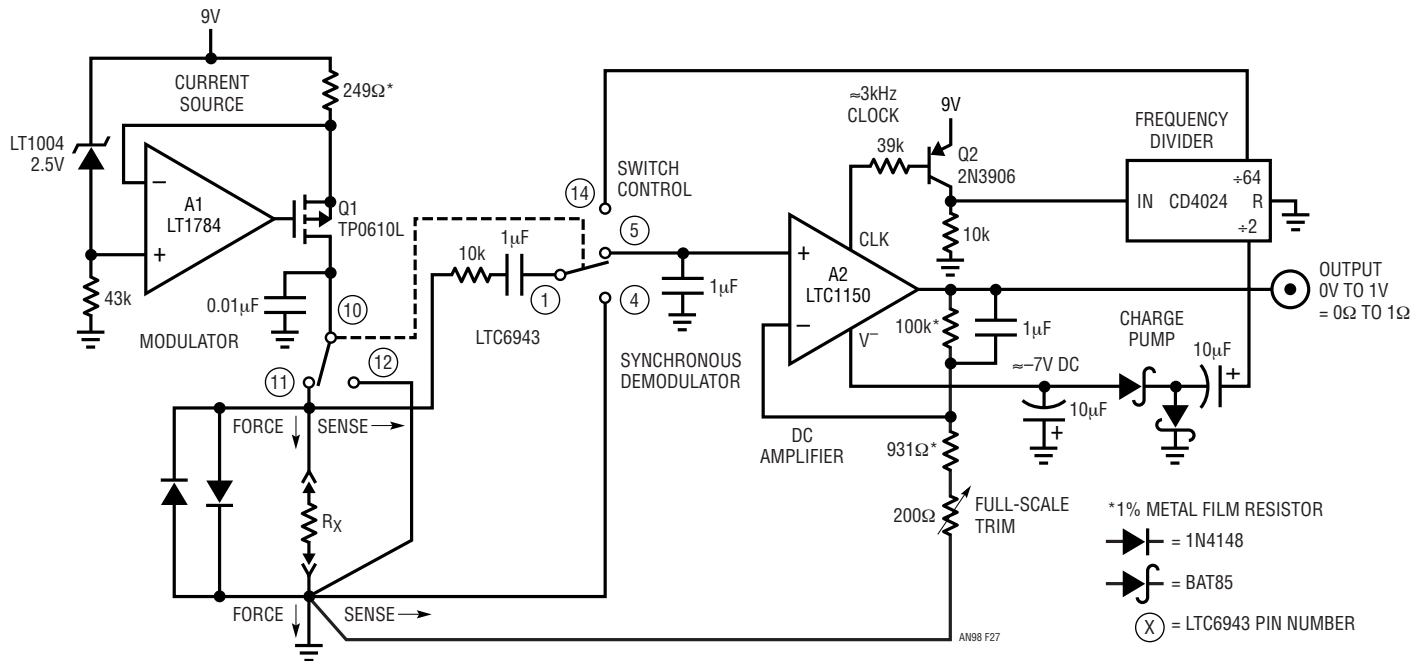


Figure 27. 1Ω Full-Scale Ohmmeter Accurately Resolves 0.001Ω for PC Board Trace/Via Resistance Measurement. Carrier Modulation of Unknown Resistance Permits Narrowband Synchronous Demodulation, Rejecting Noise and Parasitic DC Offsets. Kelvin Sensing at Rx Prevents Test Lead Induced Errors

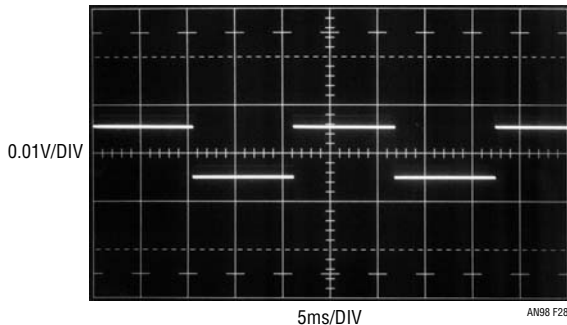


Figure 28. Normal Waveform at Rx with Rx = 1.000Ω. Circuit Output Correctly Reads 1.000V

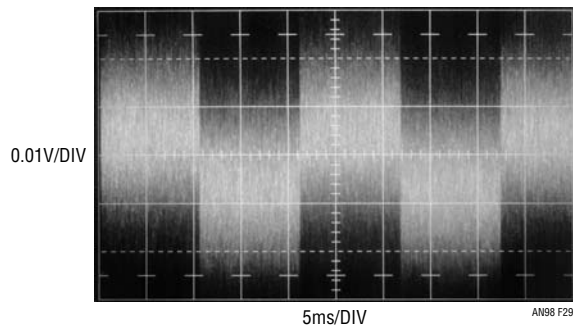


Figure 29. Rx Waveform with Rx = 1.000Ω and Noise Added. Circuit Output Remains 1.000V Despite 6× Noise-to-Signal Ratio

0.02% Accurate Instrumentation Amplifier with 125V_{CM} and 120dB CMRR

Figure 30's circuit may be used when high accuracy differential input measurement is required¹³. It is particularly suited to transducer signal conditioning where high common mode voltage may occur. The circuit has the low offset and drift of chopper stabilized A1, but also incorporates a novel optically coupled, switched capacitor input stage to achieve specifications unavailable in conventional designs. DC common mode rejection exceeds 120dB over a ±125V input range and gain accuracy and stability

are set by A1. Error from all sources is inside 0.02%. The design's high common mode voltage capability allows it to reliably extract small signals while withstanding transient and fault conditions often encountered in industrial environments.

This scheme measures input difference voltage by switching (S1A, S1B) a capacitor across the input ("ACQUIRE"). After a time the capacitor charges to the voltage across the

Note 13. Sharp-eyed devotees of LTC publications will recognize this as a mildly modified variant of Reference 8 (pp. 10-11) and Reference 13 (pp. 1-2).

Application Note 98

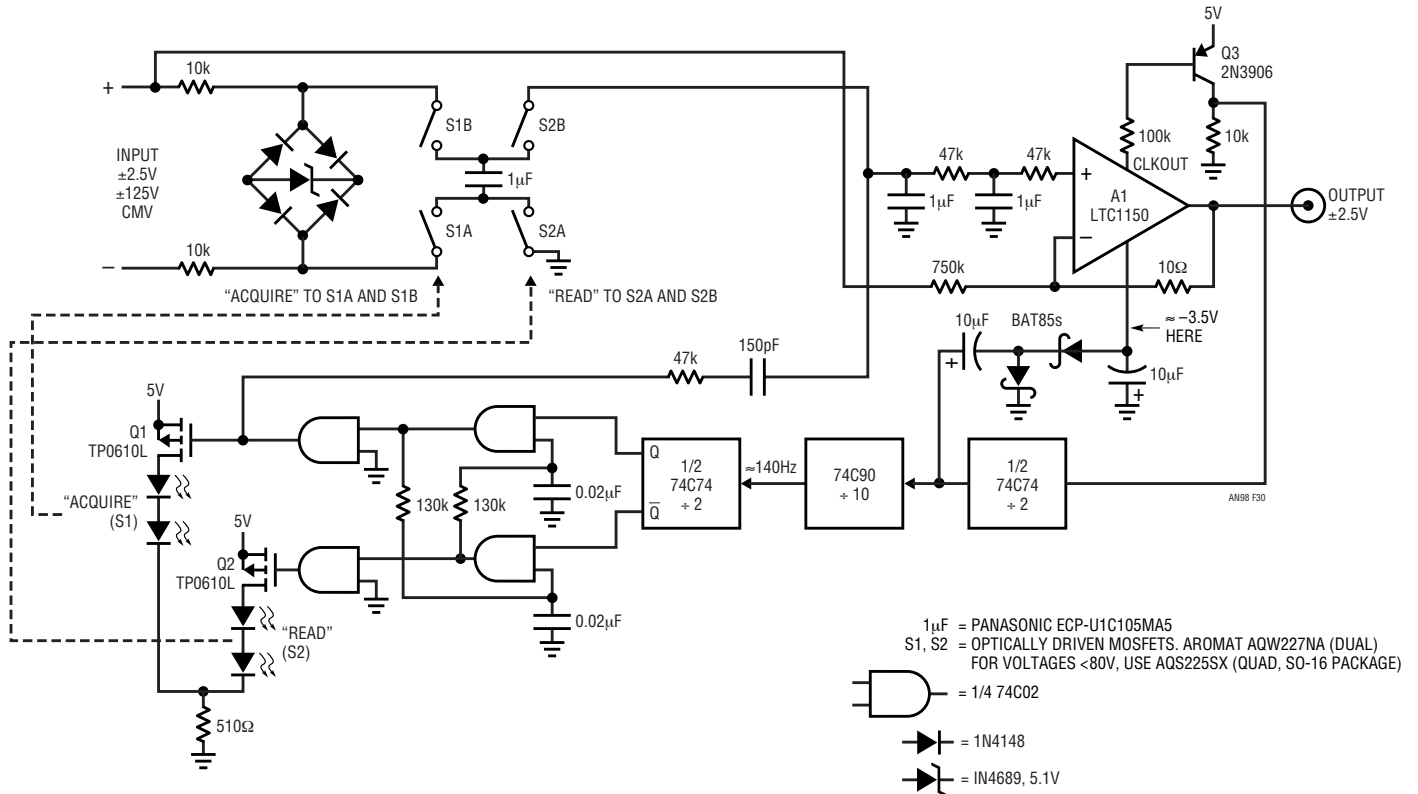


Figure 30. 0.02% Accurate, 125V Common Mode Range Instrumentation Amplifier Utilizes Optically Driven FETs and Flying Capacitor. Logic Driven Q1-Q2 Provides Nonoverlapping Clocking to S1-S2 LEDs. Clock Derives from A1's Internal Oscillator

input. S1A and S1B open and S2A and S2B close (“READ”). This grounds one capacitor plate and the capacitor discharges into the grounded 1µF unit at S2B. This switching cycle is continuously repeated, resulting in A1’s ground referred positive input assuming the input difference voltage. The common mode voltage is rejected by the optical switching of the ungrounded 1µF capacitor. The LED driven MOSFET switches specified do not have junction potentials and the optical drive contributes no charge injection error. A nonoverlapping clock prevents simultaneous conduction in S1 and S2, which would result in charge loss, causing errors and possible circuit damage. The 5.1V zener prevents switched capacitor failure if the inputs are subjected to differential overvoltage.

A1, a chopper stabilized amplifier, has a clock output. This clock, level shifted and buffered by Q3, drives a logic divider chain. The first flip-flop activates a charge pump, pulling A1’s V⁻ pin negative, permitting amplifier swing to (and below) zero volts¹⁴. The divider chain terminates into a logic network. This network provides phase opposed

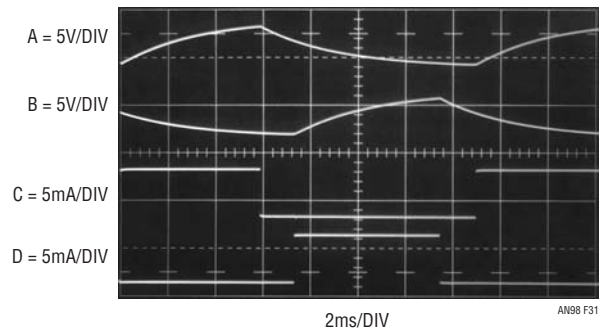


Figure 31. Clocked, Cross Coupled Capacitors (Traces A and B) in 74C02 Based Network Result in Nonoverlapping Drive (Traces C and D) to S1-S2 Actuation LEDs

charging of the 0.02µF capacitors (Traces A and B, Figure 31). The gating associated with these capacitors is arranged so the logic provides nonoverlapping, complementary biasing to Q1 and Q2. These transistors supply this nonoverlapping drive to the S1 and S2 actuating LEDs (Traces C and D).

Note 14. This arrangement will be recognized from Figures 25 and 27. See also Reference 8, Appendix D.

The extremely small parasitic error terms in the LED driven MOSFET switches results in nearly theoretical circuit performance. However, residual error ($\approx 0.1\%$) is caused by S1A's high voltage switching pumping S2B's 3pF to 4pF junction capacitance. This results in a slight quantity of unwanted charge being transferred to the $1\mu\text{F}$ capacitor at S2B. The amount of charge transferred varies with the input common mode voltage and, to a lesser extent, the varactor-like response of S2B's off-state capacitance. These terms are partially cancelled by DC feedforward to A1's negative input and AC feedforward from Q1's gate to S2B. The corrections compensate error by a factor of five, resulting in 0.02% accuracy.

Optical switch failure could expose A1 to high voltage, destroying it and possibly presenting destructive voltages to the 5V rail. This most unwelcome state of affairs is prevented by the 47k resistors in A1's positive input.

Wideband, Low Feedthrough, Low Level Switch

Rapid switching of wideband, low level signals is complicated by switch control artifacts corrupting the signal channel. FET-based designs suffer large charge injection-based errors, often orders of magnitude larger than the signal of interest. The classic diode bridge switch has much lower error, but requires substantial support circuitry and careful trimming¹⁵. Figure 32's circuit takes a different approach to synthesize a switch with minimal control channel feedthrough. This design switches signals over a $\pm 30\text{mV}$ range with peak control channel feedthrough

of millivolts and settling times inside 40ns. This capability, developed for amplifier and data converter settling time measurement, has broad implication in instrumentation and sampling circuitry.

The circuit approximates switch action by varying the transconductance of an amplifier, the maximum gain of which is unity. At low transconductance, amplifier gain is nearly zero, and essentially no signal is passed. At maximum transconductance, signal passes at unity gain. The amplifier and its transconductance control channel are very wideband, permitting them to faithfully track rapid variations in transconductance setting. This characteristic means the amplifier is never out of control, affording clean response and rapid settling to the "switched" input's value.

A1A, one section of an LT[®]1228, is the wideband transconductance amplifier. Its voltage gain is determined by its output resistor load and the current magnitude into its "I_{SET}" terminal. A1B, the second LT1228 section, unloads A1A's output. As shown it provides a gain of two, but when driving a back-terminated 50Ω cable, its effective gain is unity at the cable's receiving end. Current source Q1, controlled by the "switch control input," sets A1A's transconductance, and hence gain. With Q1 gated off (control input at zero), the 10MΩ resistor supplies about 1.5μA into A1A's I_{SET} pin, resulting in a voltage gain of nearly zero, blocking the input signal. When the switch control input goes high, Q1 turns

Note 15. See References 20 and 21 for practical examples of diode bridge switches.

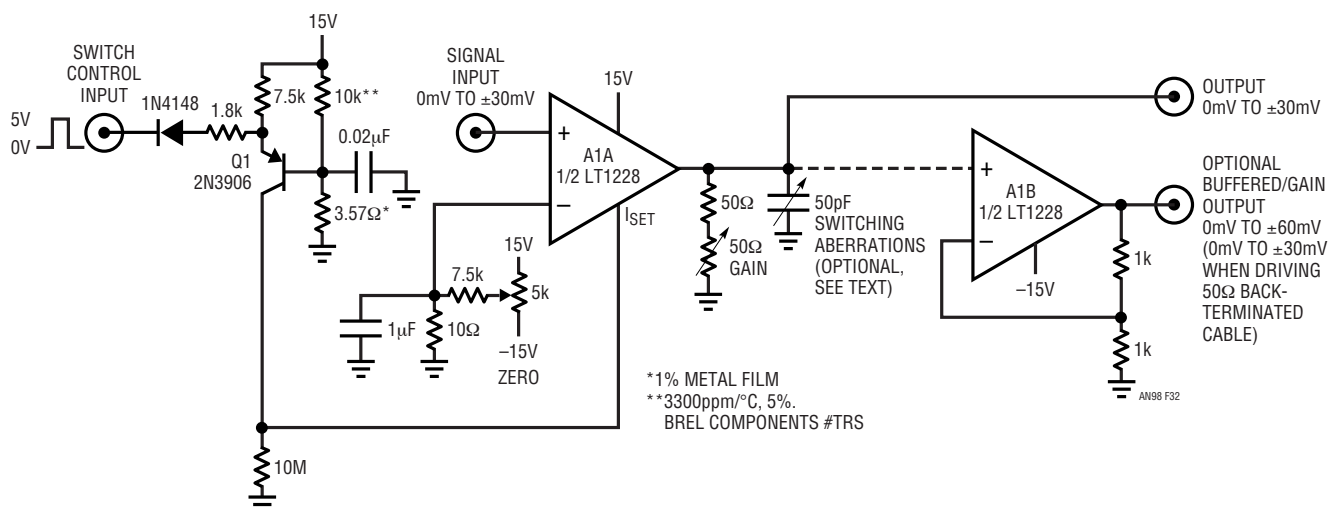


Figure 32. Transconductance Amplifier Based 100MHz Low Level Switch has Minimal Control Channel Feedthrough. A1A's Unity-Gain Output is Cleanly Switched by Logic Controlled Q1's Transconductance Bias. Optional A1B Provides Buffering and Signal Path Gain

an98f

Application Note 98

on, sourcing $\approx 1.5\text{mA}$ into the I_{SET} pin. This 1000:1 set current change forces maximum transconductance, causing the amplifier to assume unity gain and pass the input signal. Trims for zero and gain ensure accurate input signal replication at the circuit's output. The optional 50pF variable capacitor can be used to damp residual settling transients. The specified 10k resistor at Q1 has a 3300ppm/ $^{\circ}\text{C}$ temperature coefficient, compensating A1A's complementary transconductance tempco to minimize gain drift.

Figure 33 shows circuit response for a switched 10mV DC input and $C_{ABERRATION} = 35\text{pF}$. When the control input (trace A) is low, no output (trace B) occurs. When the

control input goes high, the output reproduces the input with "switch" feedthrough settling in about 20ns. Note that turn-off feedthrough is undetectable, due to the 1000 \times transconductance reduction and attendant 25 \times bandwidth drop. Figure 34 speeds the sweep up to 10ns/division to examine settling detail. The output (trace B) settles inside 1mV 40ns after the switch control (trace A) goes high. Peak feedthrough excursion, damped by $C_{ABERRATION}$, is only 5mV. Figure 35 was taken under identical conditions, except that $C_{ABERRATION} = 0\text{pF}$. Feedthrough increases to $\approx 20\text{mV}$, although settling time to 1mV remains at 40ns. Figure 36, using double exposure technique, compares signal channel rise times for

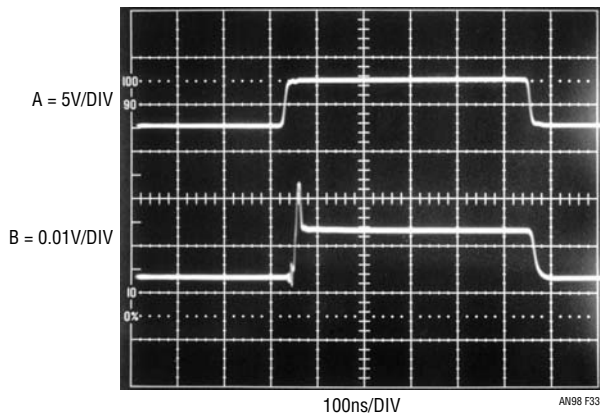


Figure 33. Control Input (Trace A) Dictates Switch Output's (Trace B) Representation of 0.01V DC Input. Control Channel Feedthrough, Evident at Switch Turn-On, Settles in 20ns. Turn-Off Feedthrough is Undetectable Due to Decreased Signal Channel Transconductance and Bandwidth. $C_{ABERRATION} \approx 35\text{pF}$ for This Test

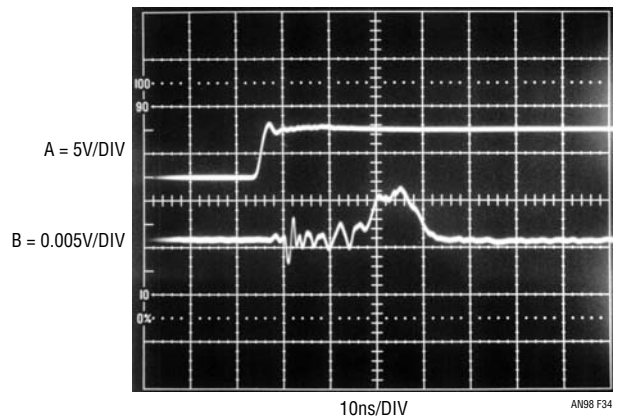


Figure 34. High Speed Delay and Feedthrough for 0V Signal Input. Output (Trace B) Peaks Only 0.005V Before Settling Inside 0.001V 40ns After Switch Control Command (Trace A). $C_{ABERRATION} \approx 35\text{pF}$ for This Test

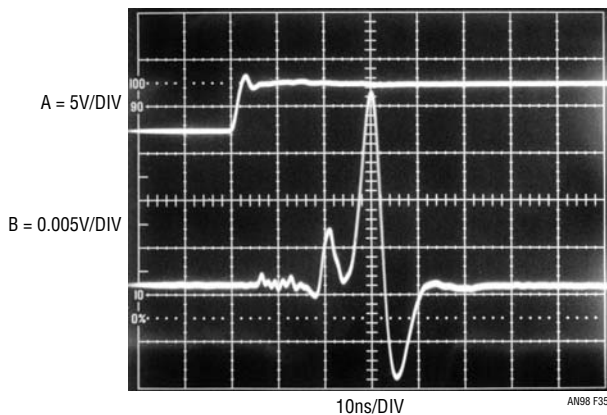


Figure 35. Identical Conditions as Figure 34 Except $C_{ABERRATION} = 0\text{pF}$. Feedthrough Related Peaking Increases to $\approx 0.02\text{V}$; 0.001V Settling Time Remains at 40ns

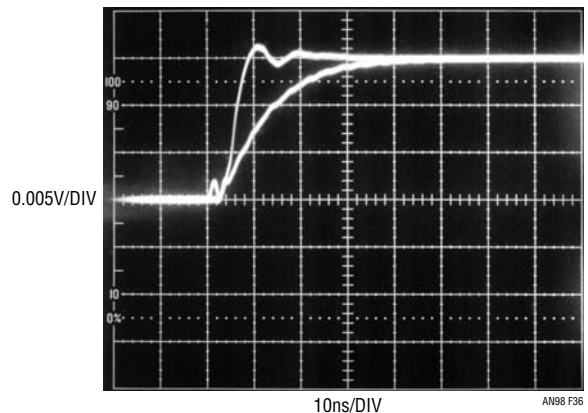


Figure 36. Signal Channel Rise Time for $C_{ABERRATION} = 0\text{pF}$ (Leftmost Trace) and $\approx 35\text{pF}$ (Rightmost Trace) Record 3.5ns and 25ns, Respectively. Switch Control Input High for this Measurement. Photograph Utilizes Double Exposure Technique

$C_{ABERRATION} = 0\text{pF}$ (leftmost trace) and $\approx 35\text{pF}$ (rightmost trace) with the control channel tied high. The larger $C_{ABERRATION}$ value, while minimizing feedthrough amplitude (see Figure 34), increases rise time by $7\times$ versus $C_{ABERRATION} = 0\text{pF}$.

To calibrate this circuit, ground the signal input and tie the control input to 5V. Set the “zero” trim for a zero volt output within $500\mu\text{V}$. Next, put 30mV into the signal input and adjust the gain trim for exactly 60mV at A1B’s unterminated output. Finally, if $C_{ABERRATION}$ is used, adjust it for minimum feedthrough amplitude with the signal input grounded and the control input fed with a 1MHz square wave.

5V Powered, 0.0015% Linearity, Quartz-Stabilized V→F Converter

Almost all precision voltage-to-frequency converters ($V\rightarrow F$) utilize charge pump based feedback for stability. These schemes rely on a capacitor for stability. A great deal of effort towards this approach has resulted in high performance $V\rightarrow F$ converters (see Reference 31). Obtaining temperature coefficients below $100\text{ppm}/^\circ\text{C}$ requires

careful attention to compensating the capacitor’s drift with temperature. Although this can be done, it complicates the design. Similarly, capacitor dielectric absorption causes errors, limiting linearity to typically 0.01% .

Figure 37’s 5V powered design, derived from Reference 31’s $\pm 15\text{V}$ fed circuit, reduces gain TC to $8\text{ppm}/^\circ\text{C}$ and achieves 15ppm linearity by replacing the capacitor with a quartz-stabilized clock.

In charge pump feedback-based circuits, the feedback is based on $Q = CV$. In a quartz-stabilized circuit, the feedback is based on $Q = IT$, where I is a stable current source and T is an interval of time derived from a clock. No capacitor is involved.

Figure 38 details Figure 37’s waveforms of operation. A positive input voltage causes A1 to integrate in the negative direction (trace A, Figure 38). The flip-flop’s Q1 output (trace B) changes state at the first positive-going clock edge (trace C) after A1’s output has crossed the D input’s switching threshold. C1 provides the quartz-stabilized clock. The flip-flop’s Q1 output controls the gating of

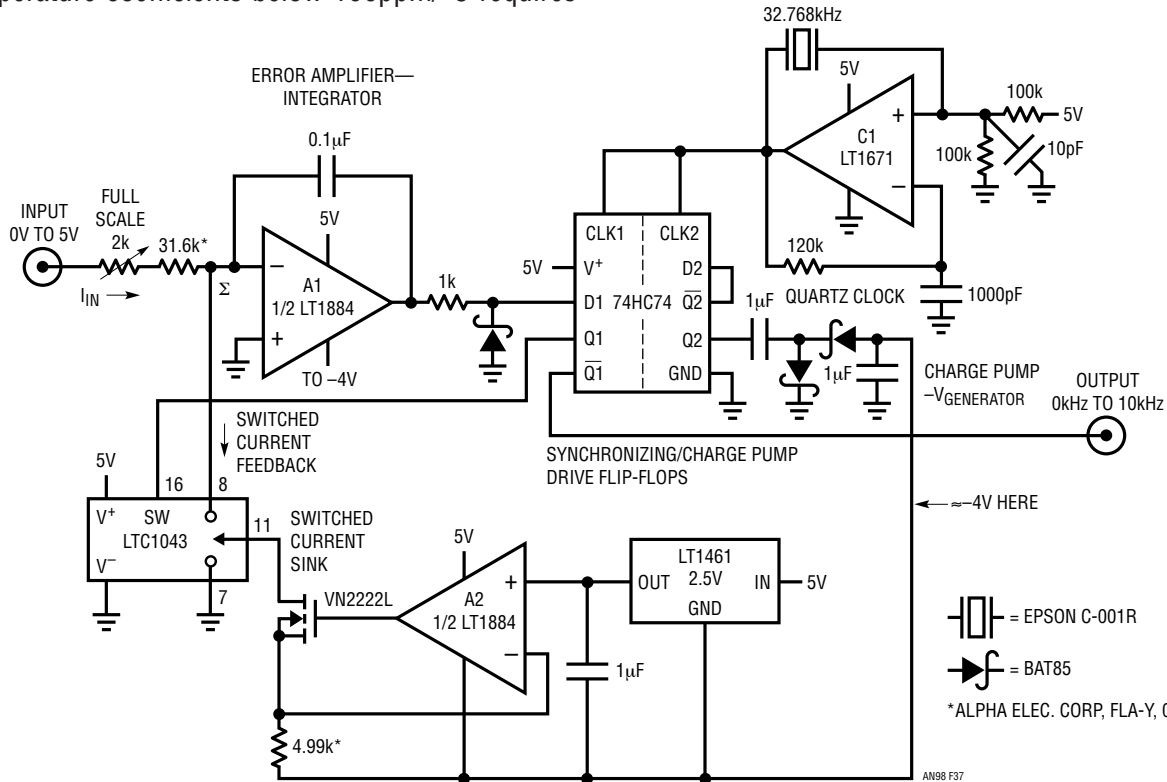


Figure 37. 5V Powered, Quartz-Stabilized 10kHz V→F Converter has 0.0015% Linearity and 8ppm/°C Temperature Coefficient. A1 Servo Controls A2 FET Switched Current Sink Via Clock Synchronized Flip-Flop to Maintain Zero Volt Summing Junction (Σ). Loop Repetition Frequency Directly Conforms to Input Voltage

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Application Note 98

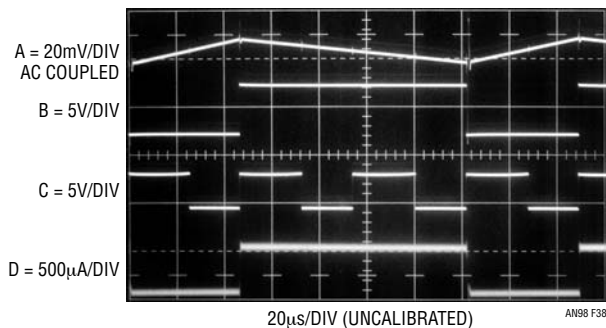


Figure 38. Quartz-Stabilized V→F Converter Waveforms Include A1 Output (Trace A), Flip-Flop Q1 Output (Trace B), Clock (Trace C) and Switched Current Feedback (Trace D). Current Removal (Trace D) from Summing Junction Commences When Clock Goes High with Q1 Low

a precision current sink composed of A2, the LT1461 voltage reference, a FET and the LTC1043 switch. A negative bias supply, derived from the flip-flop's Q2 output driving a charge pump, furnishes the sink current. When A1 is integrating negatively, Q1's output is high and the LTC1043 directs the current sink's output to ground via Pins 11 and 7. When A1's output crosses the D input's switching threshold, Q1 goes low at the first positive clock edge. LTC1043 Pins 11 and 8 close and a precise, quickly rising current flows out of A1's summing point (trace D).

This current, scaled to be greater than the maximum signal-derived input current, causes A1's output to reverse direction. At the first positive clock pulse after A1's output crosses the D input's trip point, switching again occurs and the entire process repeats. The repetition frequency depends on the input-derived current, hence the frequency of oscillation is directly related to the input voltage. The circuit's output is taken from the flip-flop's Q1 output. Because this circuit replaces a capacitor with a quartz-locked clock, temperature drift is low, typically inside 8ppm/°C. The quartz crystal contributes about 0.5ppm/°C, with most drift contributed by the current source components, the input resistor and switching time variations.

Short term frequency jitter occurs because of the uncertain timing relationship between loop frequency and clock phase. This is normally not a problem because the circuit's output is usually read over many cycles, e.g., 0.1 to 1 second. Figure 39 shows the effects of the timing

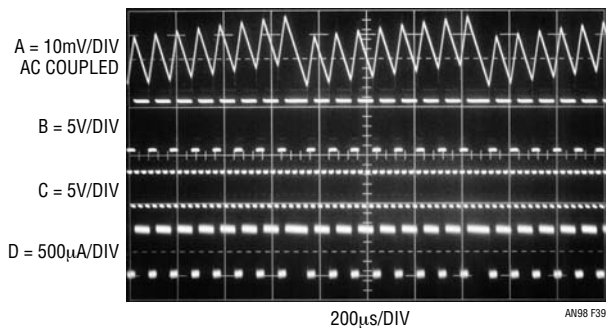


Figure 39. Same Trace Assignments as Figure 38. Reduced Oscilloscope Sweep Speed Shows Effect of Timing Uncertainty Between Loop and Clock. Loop Pulse Position is Occasionally Irregular, But Frequency is Constant Over Practical Measurement Intervals

uncertainty. Reduced sweep speed allows viewing of phase uncertainty induced modulation of A1's output ramp (trace A). Note pulse position (traces B and D) irregularity during A1's major excursions. This behavior causes short term pulse displacement, but output frequency is constant over practical measurement intervals.

Circuit linearity is inside 0.0015% (0.15Hz), gain temperature coefficient is 8ppm/°C (0.08Hz/°C) and power supply rejection better than 100ppm (1Hz) over a 4V to 6V range. The LT1884's low input bias and drift reduce zero point originated errors to insignificant levels. To trim this circuit, apply 5.0000V in and adjust the 2kΩ potentiometer for 10.000kHz output.

Basic Flashlamp Illumination Circuit for Cellular Telephones/Cameras

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Next generation cellular telephones will include high quality photographic capability. Flashlamp-based lighting is crucial for good photographic performance. A previous full-length Linear Technology publication detailed flash illumination issues and presented flash circuitry equipped

with “red-eye” reduction capability.^{16,17} Some applications do not require this feature; deleting it results in an extremely simple and compact flashlamp solution.

Figure 40’s circuit consists of a power converter, flashlamp, storage capacitor and an SCR-based trigger. In operation the LT3468-1 charges C1 to a regulated 300V at about 80% efficiency. A “trigger” input turns the SCR on, depositing C2’s charge into T2, producing a high voltage trigger event at the flashlamp. This causes the lamp to conduct high current from C1, resulting in an intense flash of light. LT3468-1 associated waveforms, appearing in Figure 41, include trace A, the “charge input,” going high. This initiates T1 switching, causing C1 to ramp up (trace B). When C1 arrives at the regulation point, switching ceases and the resistively pulled-up “DONE” line drops low (trace C), indicating C1’s charged state. The “TRIGGER” command (trace D), resulting in C1’s discharge via the lamp, may occur any time (in this case ≈600ms) after “DONE” goes low. Normally, regulation feedback would be provided by resistively dividing down the output voltage. This approach is not acceptable because it would require excessive switch cycling to offset the feedback resistor’s constant power drain. While this action would maintain regulation, it would also drain excessive power from the

primary source, presumably a battery. Regulation is instead obtained by monitoring T1’s flyback pulse characteristic, which reflects T1’s secondary amplitude. The output voltage is set by T1’s turns ratio. This feature permits tight capacitor voltage regulation, necessary to ensure consistent flash intensity without exceeding lamp energy or capacitor voltage ratings. Also, flashlamp energy is conveniently determined by the capacitor value without any other circuit dependencies.

Figure 42 shows high speed detail of the high voltage trigger pulse (trace A), the flashlamp current (trace B) and the light output (trace C). Some amount of time is required for the lamp to ionize and begin conduction after triggering. Here, 3μs after the 4kV_{p-p} trigger pulse, flashlamp

Note 16. See References 9 and 10.

Note 17. “Red-eye” in a photograph is caused by the human retina reflecting the light flash with a distinct red color. It is eliminated by causing the eye’s iris to constrict in response to a low intensity flash immediately preceding the main flash.

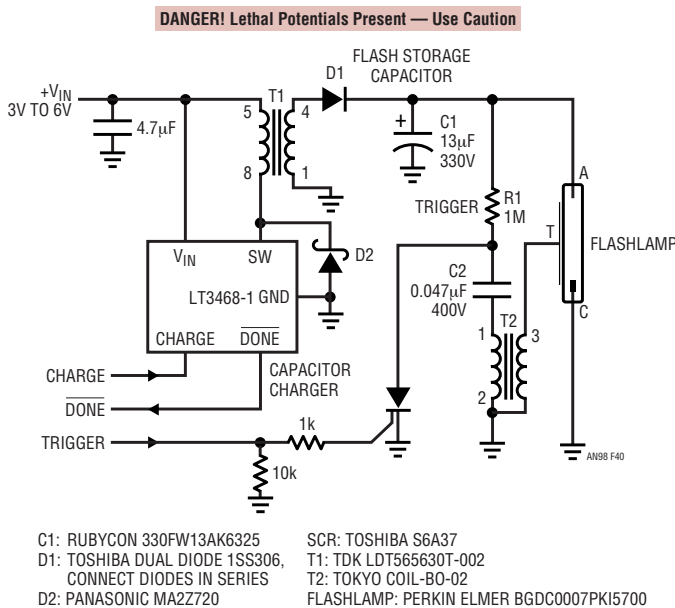


Figure 40. Complete Flashlamp Circuit Includes Capacitor Charging Components, Flash Capacitor C1, Trigger (R1, C2, T2, SCR) and Flashlamp. TRIGGER Command Biases SCR, Ionizing Lamp via T2. Resultant C1 Discharge Through Lamp Produces Light

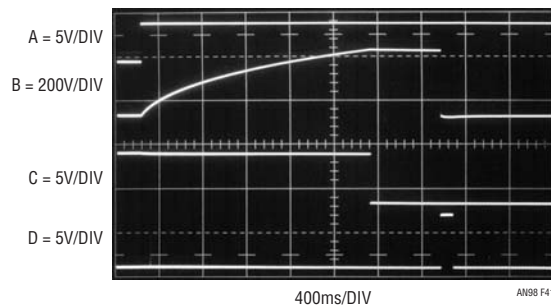


Figure 41. Capacitor Charging Waveforms Include Charge Input (Trace A), C1 (Trace B), DONE Output (Trace C) and TRIGGER Input (Trace D). C1’s Charge Time depends Upon Its Value and Charge Circuit Output Impedance. TRIGGER Input, Widened for Figure Clarity, May Occur any Time After DONE Goes Low

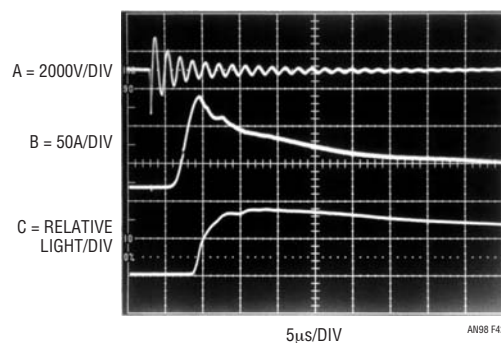


Figure 42. High Speed Detail of Trigger Pulse (Trace A), Resultant Flashlamp Current (Trace B) and Relative Light Output (Trace C). Current Exceeds 100A After Trigger Pulse Ionizes Lamp

Application Note 98

current begins its ascent to over 100A. The current rises smoothly in 3.5 μ s to a well defined peak before beginning its descent. The resultant light produced rises more slowly, peaking in about 7 μ s before decaying. Slowing the oscilloscope sweep permits capturing the entire current and light events. Figure 43 shows that light output (trace B) follows lamp current (trace A) profile, although current peaking is more abrupt. Total event duration is \approx 200 μ s with most energy expended in the first 100 μ s.

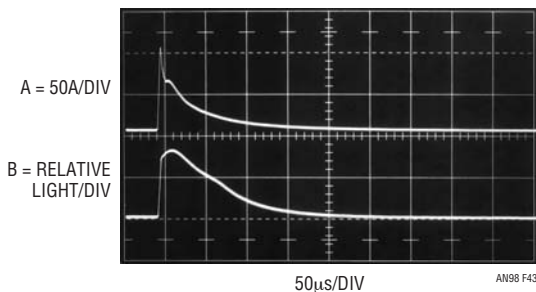
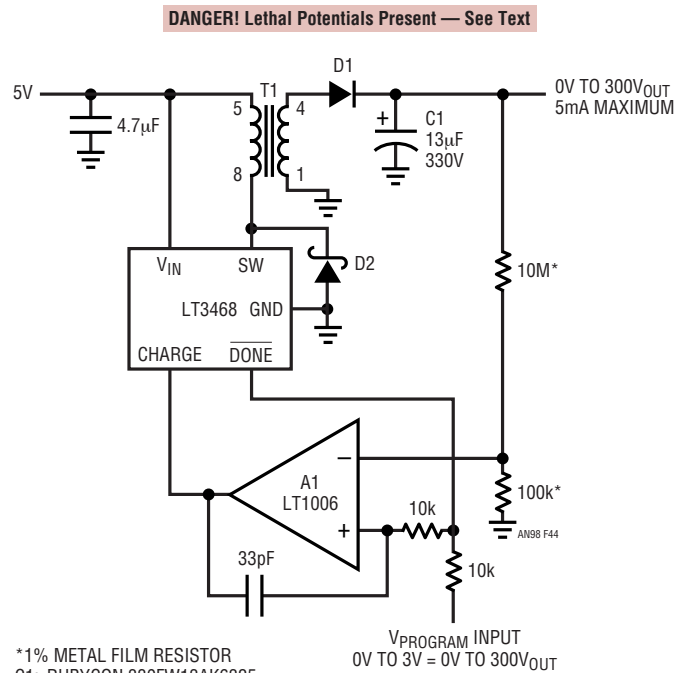


Figure 43. Photograph Captures Entire Current (Trace A) and Light (Trace B) Events. Light Output Follows Current Profile Although Peaking is Less Defined. Waveform Leading Edges Enhanced for Figure Clarity

0V to 300V Output DC/DC Converter

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 44 shows the LT3468 photoflash capacitor charger, described in the previous application, used as a general purpose, high voltage DC/DC converter. Normally, the LT3468 regulates its output at 300V by sensing T1's flyback pulse characteristic. This circuit forces the LT3468 to regulate at lower voltages by truncating its charge cycle before the output reaches 300V. A1 compares a resistively divided down portion of the output with the program input voltage. When the program input voltage (A1 + input) is exceeded by the output derived potential (A1 - input) A1's output goes low, shutting down the LT3468. The feedback capacitor provides AC hysteresis, sharpening A1's output to prevent chattering at the trip point. The LT3468 remains shut down until the output voltage drops low enough to



* 1% METAL FILM RESISTOR
 C1: RUBYCON 330FW13AK6325
 D1: TOSHIBA DUAL DIODE 1SS306,
 CONNECT DIODES IN SERIES
 D2: PANASONIC MA2Z720
 T1: TDK LDT565630T-002

Figure 44. A Voltage Programmable 0V to 300V Output Regulator. A1 Controls Regulator Output by Duty Cycle Modulating LT3468/T1 DC/DC Converter Power Delivery

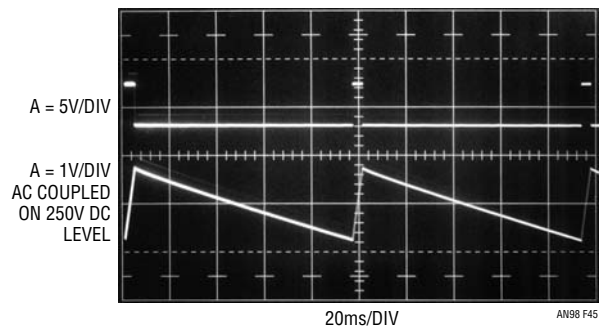


Figure 45. Details of Figure 44's Duty Cycle Modulated Operation. High Voltage Output (Trace B) Ramps Down Until A1 (Trace A) Goes High, Enabling LT3468/T1 to Restore Output. Loop Repetition Rate Varies with Input Voltage, Output Set Point and Load

trip A1's output high, turning it back on. In this way, A1 duty cycle modulates the LT3468, causing the output voltage to stabilize at a point determined by the program input. Figure 45 shows a 250V DC output (trace B) decaying down about 2V until A1 (trace A) goes high, enabling the LT3468 and restoring the loop. This simple circuit works well, regulating over a programmable 0V to

300V range, although its inherent hysteretic operation mandates the 2V output ripple noted. Loop repetition rate varies with input voltage, output set point and load but the ripple is always present. The next circuit essentially eliminates the ripple at the cost of increased complexity.

Low Ripple and Noise 0V to 300V Output DC/DC Converter

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 46 uses a post-regulator to reduce Figure 44's output ripple and noise to only 2mV. A1 and the LT3468

are identical to the previous circuit, except for the 15V zener diode in series with the 10M-100k feedback divider. This component causes C1's voltage, and hence Q1's collector, to regulate 15V above the $V_{PROGRAM}$ inputs dictated point. The $V_{PROGRAM}$ input is also routed to the A2-Q2-Q1 linear post-regulator. A2's 10M-100k feedback divider does not include a zener, so the post-regulator follows the $V_{PROGRAM}$ input with no offset. This arrangement forces 15V across Q1 at all output voltages. This figure is high enough to eliminate undesirable ripple and noise from the output while keeping Q1 dissipation low.

Q3 and Q4 form a current limit, protecting Q1 from overload. Excessive current through the 50Ω shunt turns Q3 on. Q3 drives Q4, shutting down the LT3468. Simultaneously a portion of Q3's collector current turns Q2 on hard, shutting off Q1. This loop dominates the normal regulation feedback, protecting the circuit until the overload is removed.

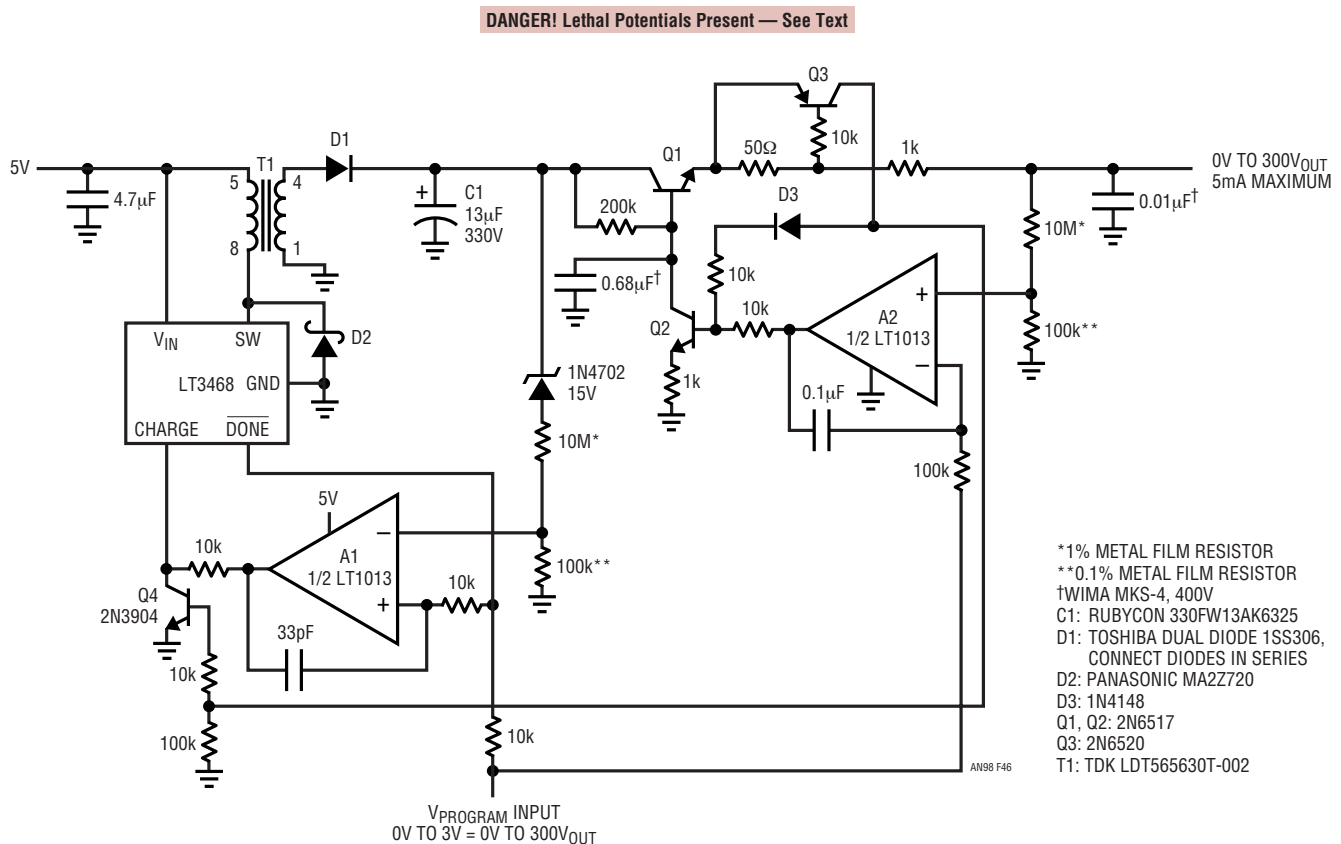


Figure 46. Post-Regulation Reduces Figure 44's 2V Output Ripple to 2mV. LT3468-Based DC/DC Converter, Similar to Figure 44, Delivers High Voltage to Q1 Collector. A2, Q1, Q2 Form Tracking, High Voltage Linear Regulator. Zener Sets Q1 $V_{CE} = 15V$, Ensuring Tracking with Minimal Dissipation. Q3-Q4 Limit Short-Circuit Output Current

Application Note 98

Figure 47 shows just how effective the post regulator is. When A1 (trace A) goes high, Q1's collector (trace B) ramps up in response (note LT3468 switching artifacts on ramps upward slope). When the A1-LT3468 loop is satisfied, A1 goes low and Q1's collector ramps down. The circuit's output post-regulator (trace C), however, rejects the ripple, showing only 2mV of noise. Slight trace blurring, right of photo center, derives from A1-LT3468 loop jitter.

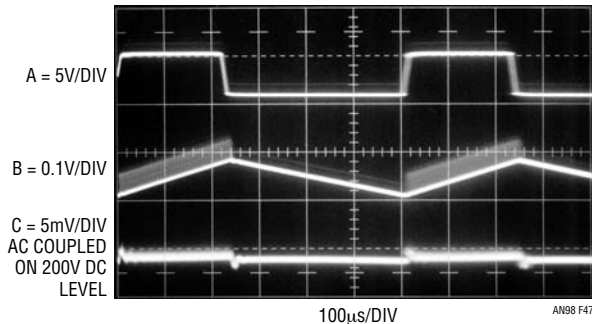


Figure 47. Low Ripple Output (Trace C) is Apparent in Post-Regulator's Operation. Traces A and B are A1 Output and Q1's Collector, Respectively. Trace Blurring, Right of Photo Center, Derives from Loop Jitter

5V to 200V Converter for APD Bias

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Avalanche photodiodes (APD) require high voltage bias. Figure 48's design provides 200V from a 5V input. The circuit is a basic inductor flyback boost regulator with a major important deviation. Q1, a high voltage device, has been interposed between the LT1172 switching regulator and the inductor. This permits the regulator to control Q1's high voltage switching without undergoing high voltage stress. Q1, operating as a "cascode" with the LT1172's internal switch, withstands L1's high voltage flyback events¹⁸. Diodes associated with Q1's source terminal

Note 18. See References 8 (page 8), 11 (Appendix D) and 22.

DANGER! Lethal Potentials Present — See Text

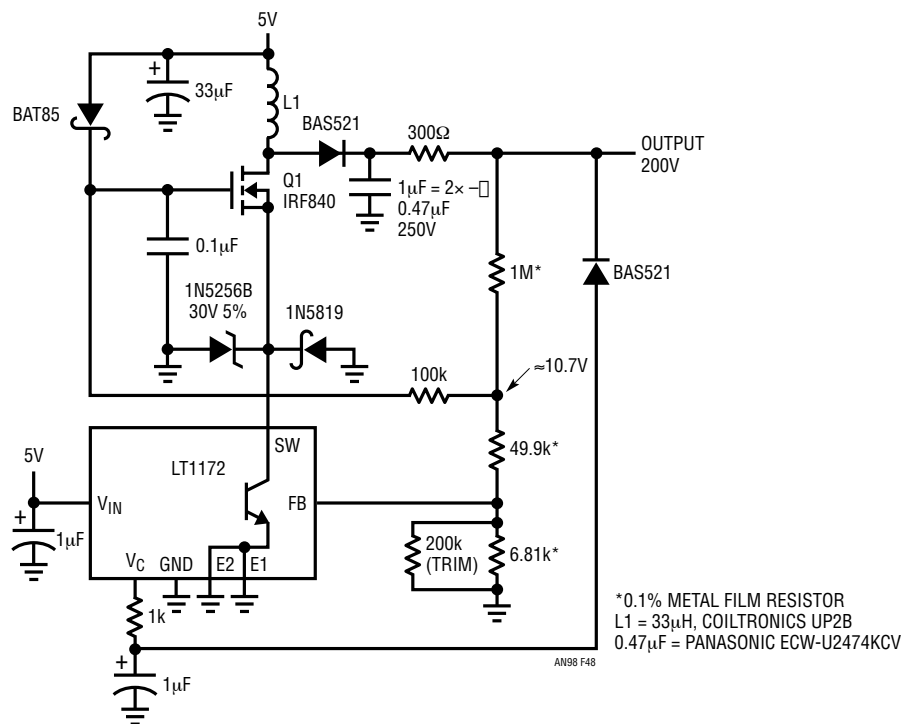


Figure 48. 5V to 200V Output Converter for APD Bias. Cascoded Q1 Switches High Voltage, Allowing Low Voltage Regulator to Control Output. Diode Clamps Protect Regulator from Transient Events; 100k Path Bootstraps Q1's Gate Drive from Output. Output Connected 300Ω-Diode Combination Provides Short-Circuit Protection

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clamp L1 originated spikes arriving via Q1's junction capacitance. The high voltage is rectified and filtered, forming the circuit's output. Feedback to the regulator stabilizes the loop and the RC at the V_C pin provides frequency compensation. The 100k path from the output divider bootstraps Q1's gate drive to about 10V, ensuring saturation. The output connected 300 Ω -diode combination provides short-circuit protection by shutting down the LT1172 if the output is accidentally grounded. The 200k trim resistor sets the 200V output $\pm 2\%$ while using standard values in the feedback divider.

Figure 49 shows operating waveforms. Traces A and C are LT1172 switch current and voltage, respectively. Q1's drain is trace B. Current ramp termination results in a high voltage flyback event at Q1's drain. A safety attenuated version of the flyback appears at the LT1172 switch. The sinusoidal signature, due to inductor ring-off between conduction cycles, is harmless.

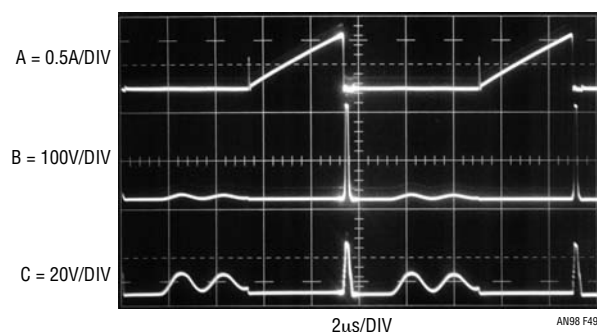


Figure 49. Waveforms for 5V to 200V Converter Include LT1172 Switch Current and Voltage (Traces A and C, Respectively) and Q1's Drain Voltage (Trace B). Current Ramp Termination Results in High Voltage Flyback Event at Q1 Drain. Safely Attenuated Version Appears at LT1172 Switch. Sinusoidal Signature, Due to Inductor Ring-Off Between Current Conduction Cycles, is Harmless. All Traces Intensified Near Center Screen for Photographic Clarity

Wide Range, High Power, High Voltage Regulator

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 50 is an example of a monolithic switching regulator making a complex function practical. This regulator provides outputs from millivolts to 500V at 100W with 80% efficiency¹⁹. A1 compares a variable reference voltage with a resistively scaled version of the circuit's output and biases the LT1074 switching regulator configuration. The switcher's DC output drives a DC/DC converter comprised of L1, Q1 and Q2. Q1 and Q2 receive out-of-phase square wave drive from the 74C74 $\div 4$ flip-flop stage and the LTC1693 FET drivers. The flip-flop is clocked from the LT1074 V_{SW} output via the Q3 level shifter. The LT3010 provides 12V power for A1, the 74C74 and the LTC1693. A1 biases the LT1074 regulator to produce the DC input at the DC/DC converter required to balance the loop. The converter has a voltage gain of about 20, resulting in high voltage output. This output is resistively divided down, closing the loop at A1's negative input. Frequency compensation for this loop must accommodate the significant phase errors generated by the LT1074 configuration, the DC/DC converter and the output LC filter. The 0.47 μ F roll-off term at A1 and the 100 Ω -0.15 μ F RC lead network provide the compensation, which is stable for all loads.

Note 19. This circuit is an updated version of Reference 12.

Application Note 98

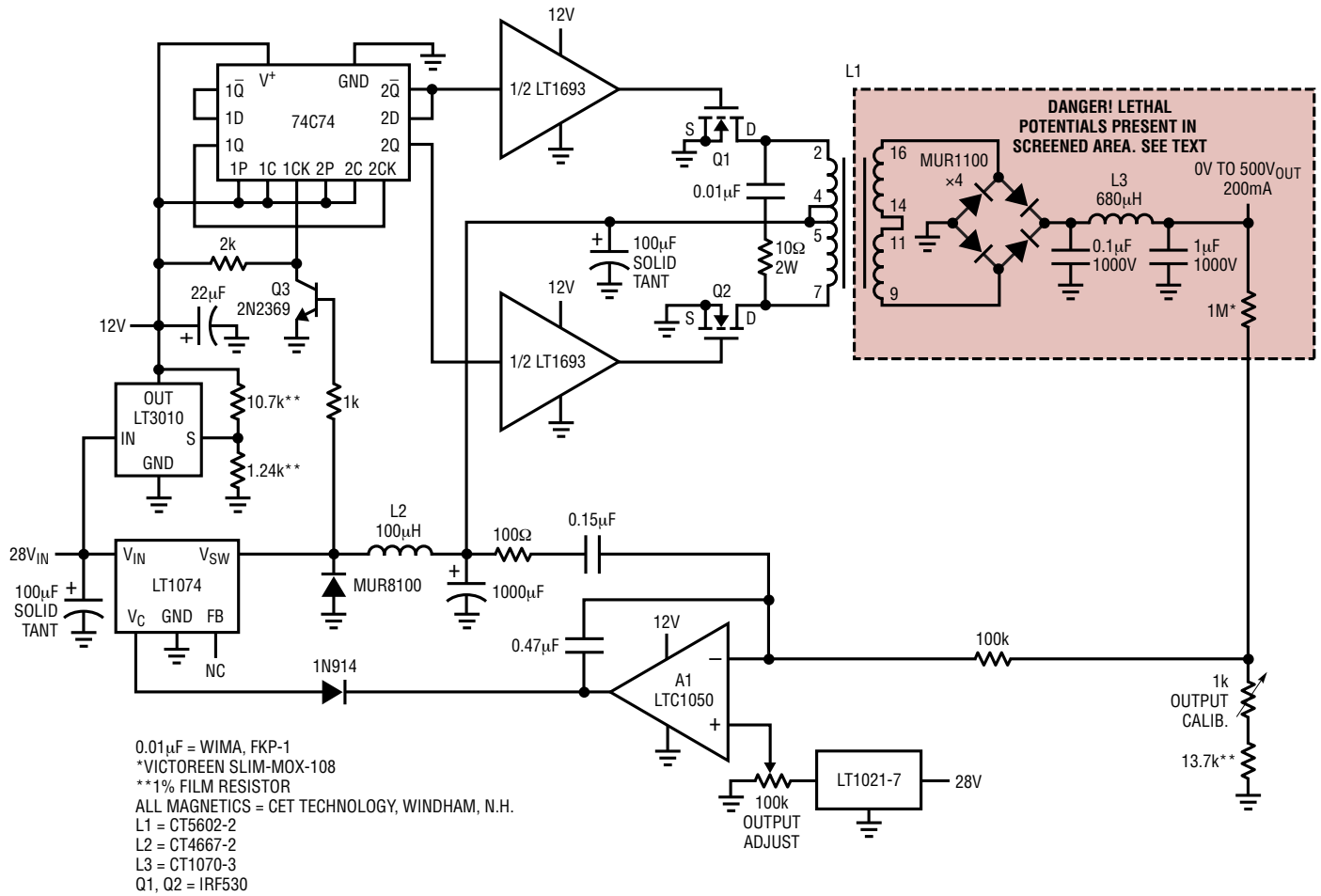


Figure 50. LT1074 Permits High Voltage Output Over 100dB Range with Power and Efficiency.
DANGER! Lethal Potentials Present—See Text

Figure 51 gives circuit waveforms at 500V output into a 100W load. Trace A is the LT1074 V_{SW} pin while trace B is its current. Traces C and D are Q1 and Q2's drain waveforms. The disturbance at the leading edges is due to cross-current conduction, which lasts about 300ns—a small percentage of the cycle. Transistor currents during this interval remain within reasonable values, and no overstress or dissipation problems occur. This effect could be eliminated with non-overlapping drive to Q1 and Q2²⁰, although there would be no reliability or significant efficiency gain.

All waveforms are synchronous because the flip-flop drive stage is clocked from the LT1074 V_{SW} output. The LT1074's maximum 95% duty cycle means that the Q1-Q2 switches can never see destructive DC drive. The only condition

allowing DC drive occurs when the LT1074 is at zero duty cycle. This case is clearly nondestructive, because L1 receives no power.

Figure 52 shows the same circuit points as Figure 51 but at only 5mV output. Here, the loop restricts drive to the DC/DC converter to small levels. Q1 and Q2 chop just 60mV into L1. At this level L1's output diode drops look large, but loop action forces the desired 0.005V output.

The LT1074's switched mode drive to L1 maintains high efficiency at high power, despite the circuit's wide output range²¹.

Note 20. See Reference 24 for an example of this technique.

Note 21. A circuit related to the one presented here appears in Reference 13. Its linear drive to the step-up DC/DC converter forces dissipation, limiting output power to about 10W.

Figure 53 shows output noise at 500V into a 100W load. Q1-Q2 chopping artifacts are clearly visible, although limited to about 50mV. The coherent noise characteristic is traceable to the synchronous clocking of Q1 and Q2 by the LT1074.

A 50V to 500V step command into a 100W load produces the response of Figure 54. Loop response on both edges is clean, with the falling edge slightly underdamped. This

slew asymmetry is typical of switching configurations, because the load and output capacitor determine negative slew rate. The wide range of possible loads mandates a compromise when setting frequency compensation. The falling edge could be made critically or even over damped, but the response time for other conditions would suffer. The compensation used seems a reasonable compromise.

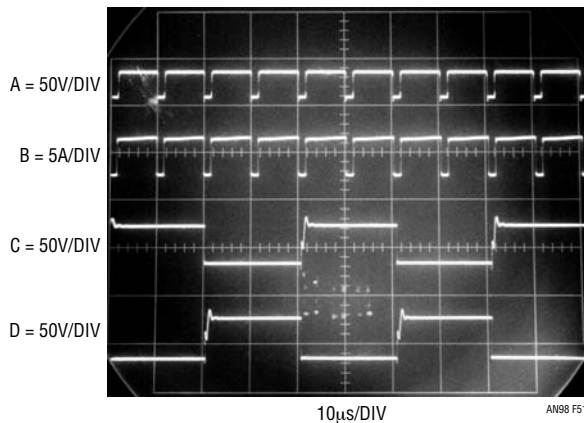


Figure 51. Figure 50's Operating Waveforms at 500V Output Into a 100W Load

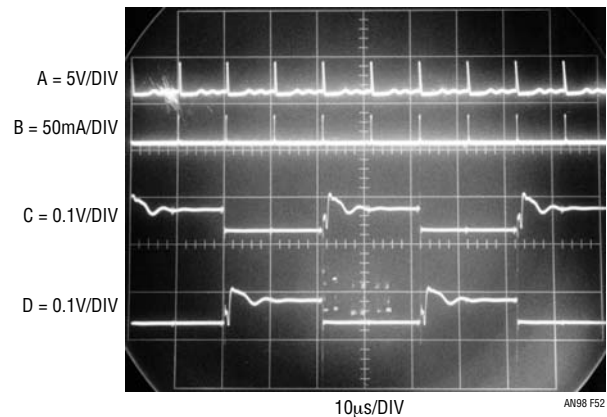


Figure 52. Operating Waveforms at 0.005V Output

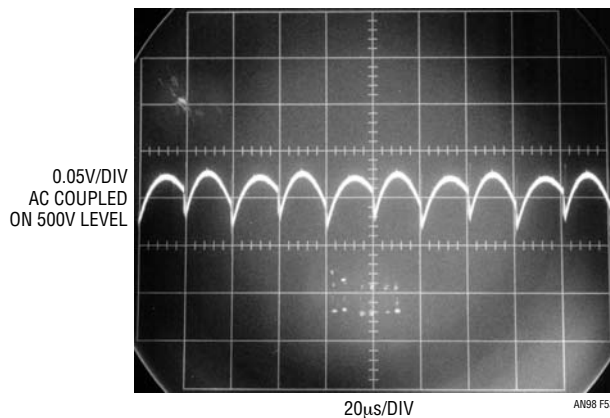


Figure 53. Output Noise at 500V into a 100W Load. Residue is Composed of Q1-Q2 Chopping Artifacts. **DANGER! Lethal Potentials Present—See Text**

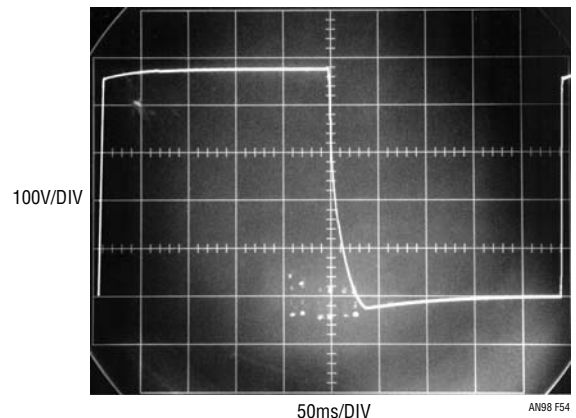


Figure 54. 500V Step Response with 100W Load (Photo Retouched for Clarity). **DANGER! Lethal Potentials Present—See Text**

Application Note 98

5V to 3.3V, 15A Paralleled Linear Regulator

Figure 55 is another high power supply; unlike the previous example, it is a linear regulator. Two 7.5A regulators are paralleled in a “master-slave” arrangement. The “master” regulator is wired to produce a 3.3V output in the conventional manner. The 124Ω feedback resistor senses at the 0.001Ω shunt located directly before the circuit

output. The “slave” regulator, also wired for a nominal 3.3V output, sources the circuit output in identical fashion. A1, sensing the regulators difference voltage, adjusts the “slave” regulator to equal the master’s output voltage. This allows the regulators to equally share the load current. The 0.001Ω shunts cause negligible regulation loss, but provide adequate signal for A1.

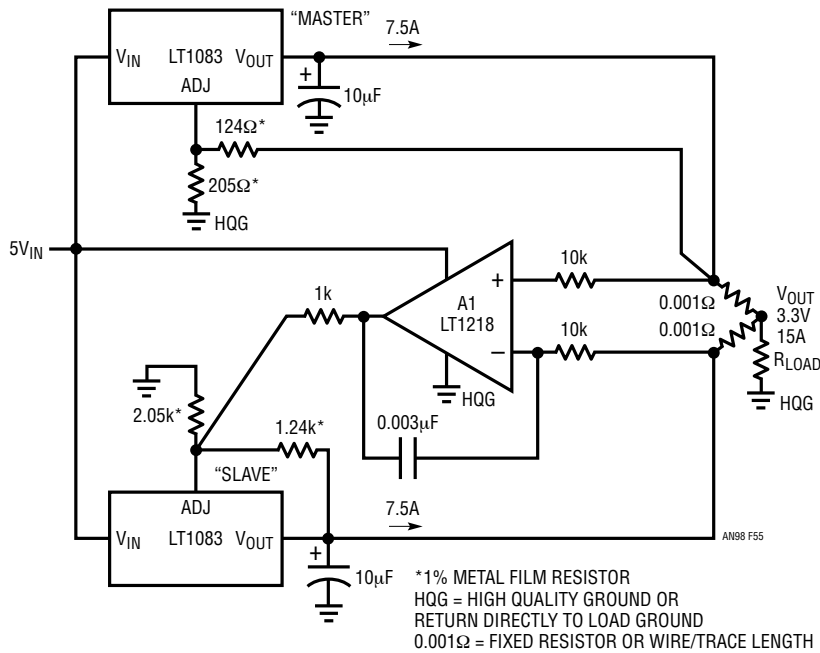


Figure 55. Paralleled Regulators Share Load Current. Amplifier Senses Differential Regulator Voltage; Biases “Slave” to Equalize Output Currents. Remote Sensing Negates Lead Wire Voltage Drops

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Application Note 98

APPENDIX A

How Much Bandwidth is Enough?

Accurate wideband oscilloscope measurements require bandwidth. A good question is just how much is needed. A classic guideline is that “end-to-end” measurement system rise time is equal to the root-sum-square of the system’s individual component’s rise times. The simplest case is two components; a signal source and an oscilloscope. Figure A1’s plot of $\sqrt{\text{signal}^2 + \text{oscilloscope}^2}$ rise time versus error is illuminating. The figure plots signal-to-oscilloscope rise time ratio versus observed rise time (rise time is bandwidth restated in the time domain, where:

$$\text{Rise Time (nanoseconds)} = \frac{350}{\text{Bandwidth (MHz)}}$$

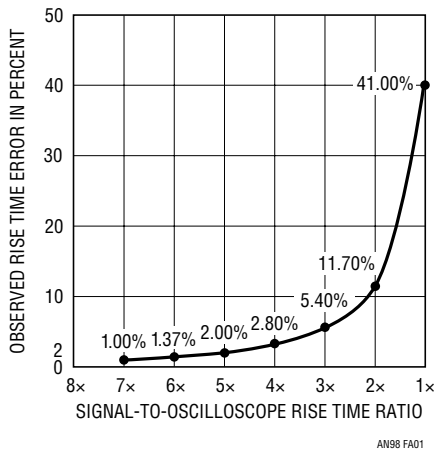


Figure A1. Oscilloscope Rise Time Effect on Rise Time Measurement Accuracy. Measurement Error Rises Rapidly as Signal-to-Oscilloscope Rise Time Ratio Approaches Unity. Data, Based on Root-Sum-Square Relationship, Does Not Include Probe, Which Does Not Follow Root-Sum-Square Law

The curve shows that an oscilloscope 3 to 4 times faster than the input signal rise time is required for measurement accuracy inside about 5%. This is why trying to measure a 1ns rise time pulse with a 350MHz oscilloscope ($t_{\text{RISE}} = 1\text{ns}$) leads to erroneous conclusions. The curve indicates a monstrous 41% error. Note that this curve does not include the effects of passive probes or cables connecting the signal to the oscilloscope. Probes do not necessarily follow root-sum-square law and must be carefully chosen and applied for a given measurement. For details, See Appendix B. Figure A2, included for reference, gives 10 cardinal points of rise time/bandwidth equivalency between 1MHz and 5GHz.

RISE TIME	BANDWIDTH
70ps	5GHz
350ps	1GHz
700ps	500MHz
1ns	350MHz
2.33ns	150MHz
3.5ns	100MHz
7ns	50MHz
35ns	10MHz
70ns	5MHz
350ns	1MHz

Figure A2. Some Cardinal Points of Rise Time/Bandwidth Equivalency. Data is Based on Rise Time/Bandwidth Formula in Text

APPENDIX B

Connections, Cables, Adapters, Attenuators, Probes and Picoseconds

Subnanosecond rise time signal paths must be considered as transmission lines. Connections, cables, adapters, attenuators and probes represent discontinuities in this transmission line, deleteriously effecting its ability to faithfully transmit desired signal. The degree of signal corruption contributed by a given element varies with its deviation from the transmission lines nominal impedance. The practical result of such introduced aberrations is degradation of pulse rise time, fidelity, or both. Accordingly, introduction of elements or connections to the signal path should be minimized and necessary connections and elements must be high grade components. Any form of connector, cable, attenuator or probe must be fully specified for high frequency use. Familiar BNC hardware becomes lossy at rise times much faster than 350ps. SMA components are preferred for the rise times described in the text. Additionally, cable should be 50Ω “hard line” or, at least, teflon-based coaxial cable fully specified for high frequency operation. Optimal connection practice eliminates any cable by coupling the signal output *directly* to the measurement input.

Mixing signal path hardware types via adapters (e.g. BNC/SMA) should be avoided. Adapters introduce significant

parasitics, resulting in reflections, rise time degradation, resonances and other degrading behavior. Similarly, oscilloscope connections should be made directly to the instrument’s 50Ω inputs, avoiding probes. If probes must be used, their introduction to the signal path mandates attention to their connection mechanism and high frequency compensation. Passive “Z₀” types, commercially available in 500Ω (10x) and 5kΩ(100x) impedances, have input capacitance below 1pf. Any such probe must be carefully frequency compensated before use or misrepresented measurement will result. Inserting the probe into the signal path necessitates some form of signal pick-off which nominally does not influence signal transmission. In practice, some amount of disturbance must be tolerated and its effect on measurement results evaluated. High quality signal pick-offs always specify insertion loss, corruption factors and probe output scale factor.

The preceding emphasizes vigilance in designing and maintaining a signal path. Skepticism, tempered by enlightenment, is a useful tool when constructing a signal path and no amount of hope is as effective as preparation and directed experimentation.

Hey Jim, don't you ever do anything else but work on circuits?

NO. NOTHING.

WHAT ABOUT SKIING, GOLF, TENNIS, COOKING, GARDENING, RESTAURANTS, TRAVEL, ENTERTAINING, MUSIC, ARTS, MOVIES?

NO. NOT INTERESTED, BUT MOVIES ARE OK.

WHY MOVIES?

IT'S DARK IN THERE. YOU CAN THINK ABOUT CIRCUITS

Minimizing Switching Regulator Residue in Linear Regulator Outputs

Banishing Those Accursed Spikes

Jim Williams

INTRODUCTION

Linear regulators are commonly employed to post-regulate switching regulator outputs. Benefits include improved stability, accuracy, transient response and lowered output impedance. Ideally, these performance gains would be accompanied by markedly reduced switching regulator generated ripple and spikes. In practice, all linear regulators encounter some difficulty with ripple and spikes, particularly as frequency rises. This effect is magnified at small regulator V_{IN} to V_{OUT} differential voltages; unfortunate, because such small differentials are desirable to maintain efficiency. Figure 1 shows a conceptual linear regulator and associated components driven from a switching regulator output.

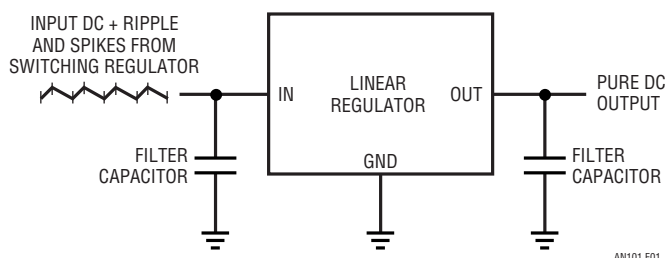
The input filter capacitor is intended to smooth the ripple and spikes before they reach the regulator. The output capacitor maintains low output impedance at higher frequencies, improves load transient response and supplies frequency compensation for some regulators. Ancillary purposes

include noise reduction and minimization of residual input-derived artifacts appearing at the regulators output. It is this last category—residual input-derived artifacts—that is of concern. These high frequency components, even though small amplitude, can cause problems in noise-sensitive video, communication and other types of circuitry. Large numbers of capacitors and aspirin have been expended in attempts to eliminate these undesired signals and their resultant effects. Although they are stubborn and sometimes seemingly immune to any treatment, understanding their origin and nature is the key to containing them.

Switching Regulator AC Output Content

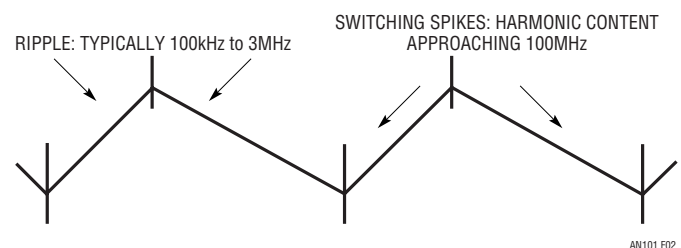
Figure 2 details switching regulator dynamic (AC) output content. It consists of relatively low frequency ripple at the switching regulator's clock frequency, typically 100kHz to 3MHz, and very high frequency content "spikes" associated with power switch transition times. The switching regulator's pulsed energy delivery creates the ripple. Filter capacitors smooth the output, but not completely. The

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AN101 F01

Figure 1. Conceptual Linear Regulator and Its Filter Capacitors Theoretically Reject Switching Regulator Ripple and Spikes



AN101 F02

Figure 2. Switching Regulator Output Contains Relatively Low Frequency Ripple and High Frequency "Spikes" Derived From Regulators Pulsed Energy Delivery and Fast Transition Times

Application Note 101

spikes, which often have harmonic content approaching 100MHz, result from high energy, rapidly switching power elements within the switching regulator. The filter capacitor is intended to reduce these spikes but in practice cannot entirely eliminate them. Slowing the regulator's repetition rate and transition times can greatly reduce ripple and spike amplitude, but magnetics size increases and efficiency falls¹. The same rapid clocking and fast switching that allows small magnetics size and high efficiency results in high frequency ripple and spikes presented to the linear regulator.

Ripple and Spike Rejection

The regulator is better at rejecting the ripple than the very wideband spikes. Figure 3 shows rejection performance for an LT1763 low dropout linear regulator. There is 40db attenuation at 100kHz, rolling off to about 25db at 1MHz. The much more wideband spikes pass directly through the regulator. The output filter capacitor, intended to absorb the spikes, also has high frequency performance limitations. The regulator and filter capacitors imperfect response, due to high frequency parasitics, reveals Figure 1 to be overly simplistic. Figure 4 restates Figure 1 and includes the parasitic terms as well as some new components.

The figure considers the regulation path with emphasis on high frequency parasitics. It is important to identify these parasitic terms because they allow ripple and spikes to propagate into the nominally regulated output. Additionally, understanding the parasitic elements permits a measurement strategy, facilitating reduction of high frequency output content. The regulator includes high frequency parasitic paths, primarily capacitive, across its pass transistor and into its reference and regulation amplifier. These terms combine with finite regulator gain-bandwidth to limit high frequency rejection. The input and output filter capacitors include parasitic inductance and resistance, degrading their effectiveness as frequency rises. Stray layout capacitance provides additional unwanted feedthrough paths. Ground potential differences, promoted by ground path resistance and inductance, add additional error and also complicate measurement. Some new components, not normally associated with linear regulators, also appear. These additions include ferrite beads or inductors in the regulator input and output lines. These components have their own high frequency parasitic paths but can considerably improve overall regulator high frequency rejection and will be addressed in following text.

Note 1: Circuitry employing this approach has achieved significant harmonic content reduction at some sacrifice in magnetics size and efficiency. See Reference 1.

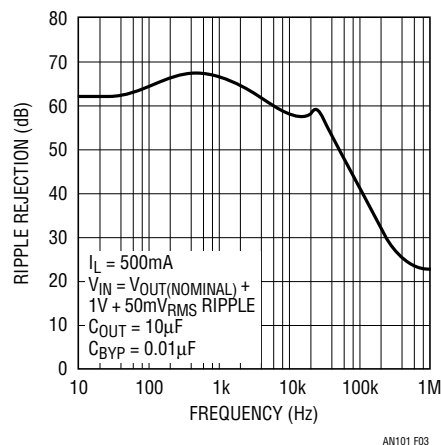
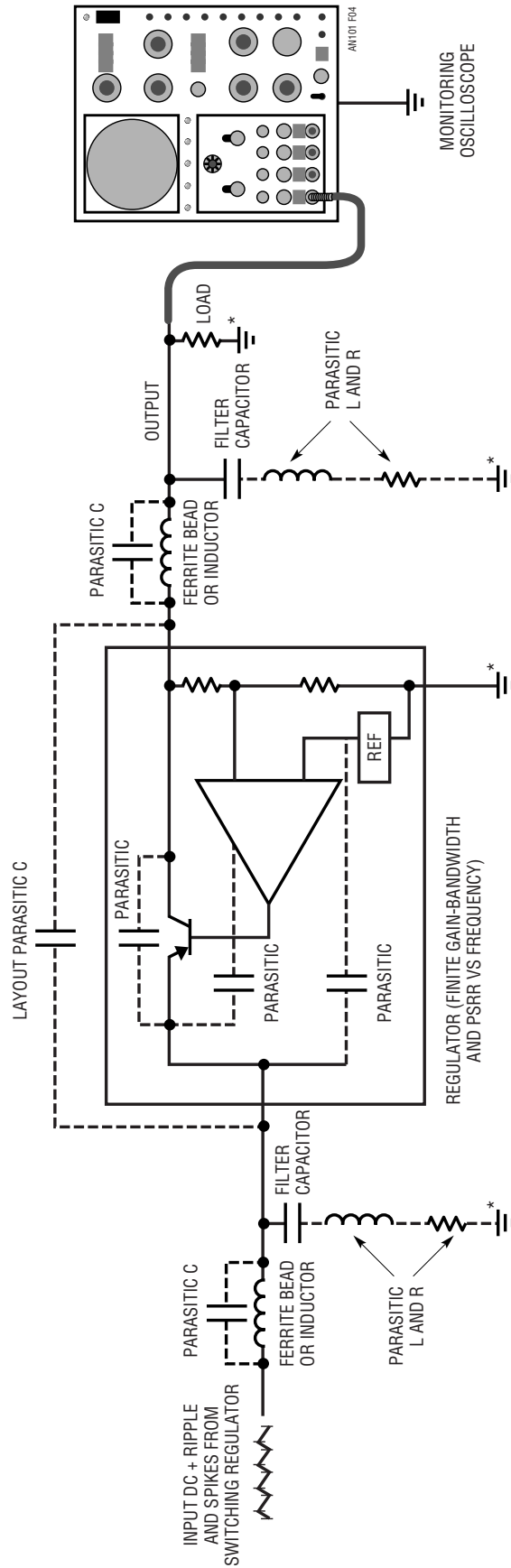


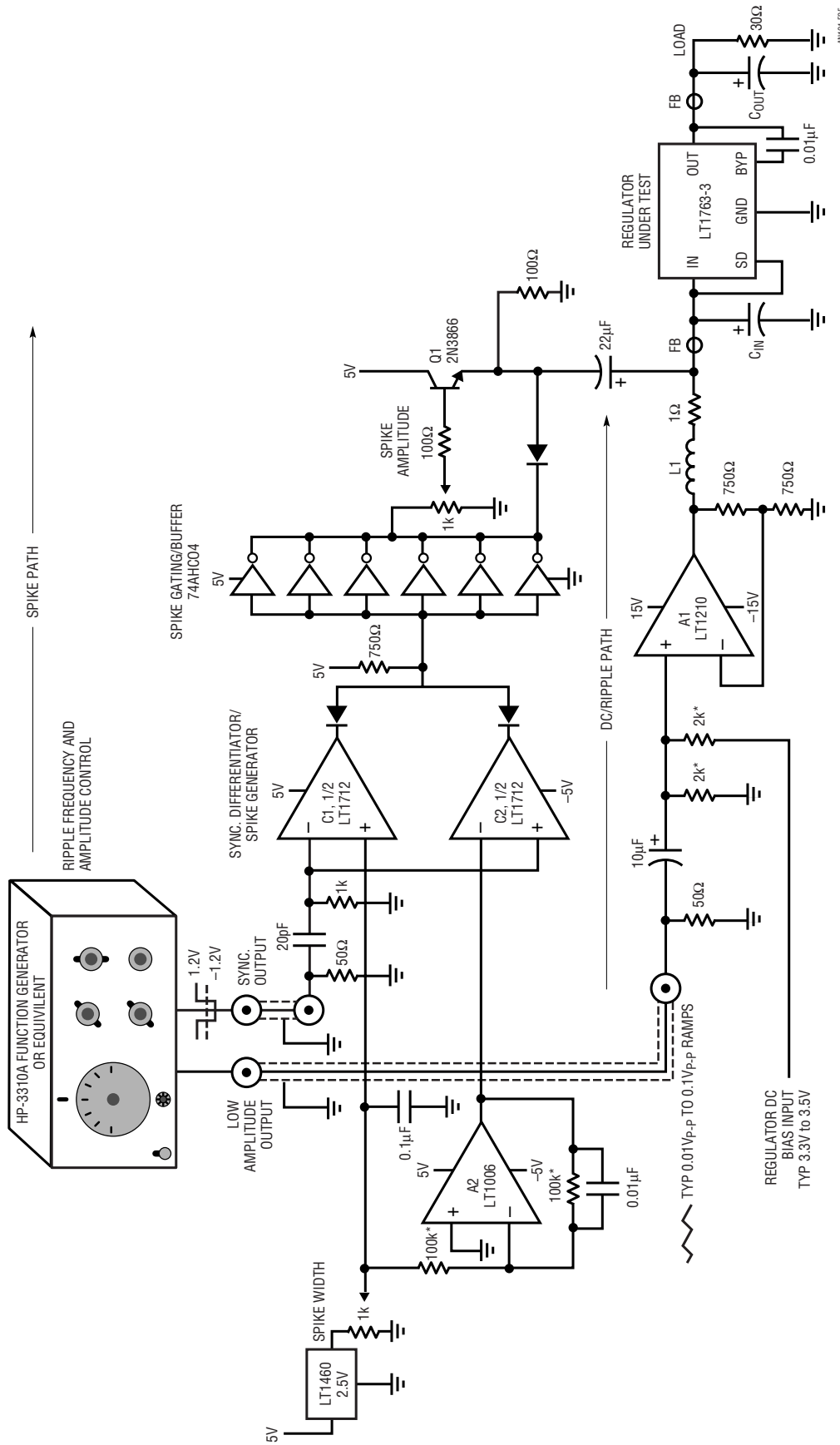
Figure 3. Ripple Rejection Characteristics for an LT1763 Low Dropout Linear Regulator Show 40dB Attenuation at 100kHz, Rolling Off Towards 1MHz. Switching Spike Harmonic Content Approaches 100MHz; Passes Directly From Input to Output



* = GROUND POTENTIAL DIFFERENCES PROMOTE OUTPUT HIGH FREQUENCY CONTENT AND CORRUPT MEASUREMENT.

Figure 4. Conceptual Linear Regulator Showing High Frequency Rejection Parasitics. Finite GBW and PSRR vs Frequency Limit Regulator's High Frequency Rejection. Passive Components Attenuate Ripple and Spikes, But Parasitics Degrade Effectiveness. Layout Capacitance and Ground Potential Differences Add Errors, Complicate Measurement

Application Note 101



* = 1% METAL FILM RESISTOR
 L1 = 4 TURNS #26, 1/4" DIAMETER
 FB = FERRITE BEAD, FAIR-RITE 2743002122. INDUCTORS OPTIONAL. SEE TEXT
 C_{IN} = SEE TEXT
 C_{OUT} = SEE TEXT

Figure 5. Circuit Simulates Switching Regulator Output. DC, Ripple Amplitude, Frequency and Spike Duration/Height are Independently Settable. Split Path Scheme Sums Wideband Spikes with DC and Ripple, Presenting Linear Regulator with Simulated Switching Regulator Output. Function Generator Sources Waveforms to Both Paths

Ripple/Spike Simulator

Gaining understanding of the problem requires observing regulator response to ripple and spikes under a variety of conditions. It is desirable to be able to independently vary ripple and spike parameters, including frequency, harmonic content, amplitude, duration and DC level. This is a very versatile capability, permitting real time optimization and sensitivity analysis to various circuit variations. Although there is no substitute for observing linear regulator performance under actual switching regulator driven conditions, a hardware simulator makes surprises less likely. Figure 5 provides this capability. It simulates a switching regulator's output with independently settable DC, ripple and spike parameters.

A commercially available function generator combines with two parallel signal paths to form the circuit. DC and ripple are transmitted on a relatively slow path while wideband spike information is processed via a fast path. The two

paths are combined at the linear regulator input. The function generator's settable ramp output (trace A, Figure 6) feeds the DC/ripple path made up of power amplifier A1 and associated components. A1 receives the ramp input and DC bias information and drives the regulator under test. L1 and the 1Ω resistor allow A1 to drive the regulator at ripple frequencies without instability. The wideband spike path is sourced from the function generator's pulsed "sync" output (trace B). This output's edges are differentiated (trace C) and fed to bipolar comparator C1-C2. The comparator outputs (traces D and E) are spikes synchronized to the ramps inflection points. Spike width is controlled by complementary DC threshold potentials applied to C1 and C2 with the 1k potentiometer and A2. Diode gating and the paralleled logic inverters present trace F to the spike amplitude control. Follower Q1 sums the spikes with A1's DC/ripple path, forming the linear regulator's input (trace G).

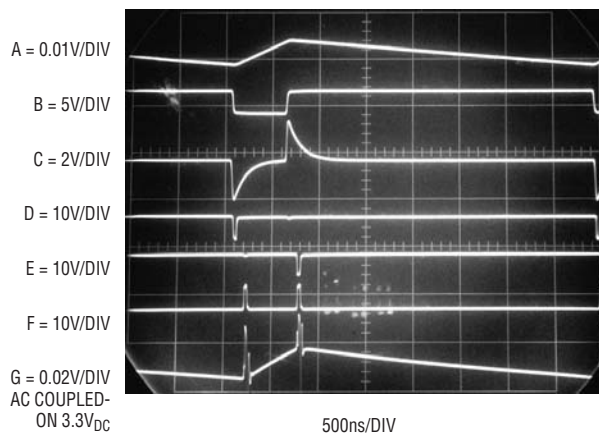


Figure 6. Switching Regulator Output Simulator Waveforms. Function Generator Supplies Ripple (Trace A) and Spike (Trace B) Path Information. Differentiated Spike Information's Bipolar Excursion (Trace C) is Compared by C1-C2, Resulting in Trace D and E Synchronized Spikes. Diode Gating/Inverters Present Trace F to Spike Amplitude Control. Q1 Sums Spikes with DC-Ripple Path From Power Amplifier A1, Forming Linear Regulator Input (Trace G). Spike Width Set Abnormally Wide for Photographic Clarity

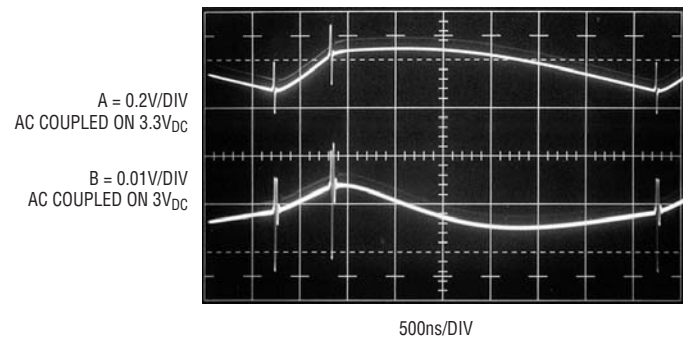


Figure 7. Linear Regulator Input (Trace A) and Output (Trace B) Ripple and Switching Spike Content for $C_{IN} = 1\mu F$, $C_{OUT} = 10\mu F$. Output Spikes, Driving $10\mu F$, Have Lower Amplitude, But Risetime Remains Fast

Application Note 101

Linear Regulator High Frequency Rejection Evaluation/Optimization

The circuit described above facilitates evaluation and optimization of linear regulator high frequency rejection. The following photographs show results for one typical set of conditions, but DC bias, ripple and spike characteristics may be varied to suit desired test parameters. Figure 7 shows Figure 5's LT1763 3V regulator response to a 3.3V DC input with trace A's ripple/spike contents, $C_{IN} = 1\mu\text{F}$ and $C_{OUT} = 10\mu\text{F}$. Regulator output (trace B) shows ripple attenuated by a factor of ≈ 20 . Output spikes see somewhat less reduction and their harmonic content remains high. The regulator offers no rejection at the spike rise time. The capacitors must do the job. Unfortunately, the capacitors are limited by inherent high frequency loss terms from completely filtering the wideband spikes; trace B's remaining spike shows no risetime reduction. Increasing capacitor value has no benefit at these rise times. Figure 8 (same trace assignments as Figure 7) taken with $C_{OUT} = 33\mu\text{F}$, shows 5 \times ripple reduction but little spike amplitude attenuation.

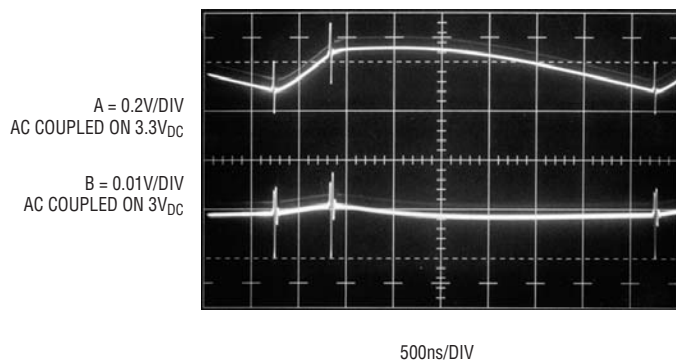


Figure 8. Same Trace Assignments as Figure 7 with C_{OUT} Increased to $33\mu\text{F}$. Output Ripple Decreases By 5 \times , But Spikes Remain. Spike Risetime Appears Unchanged

Figure 9's time and amplitude expansion of Figure 8's trace B permits high resolution study of spike characteristics, allowing the following evaluation and optimization. Figure 10 shows dramatic results when a ferrite bead immediately precedes C_{IN} ². Spike amplitude drops about 5 \times . The bead presents loss at high frequency, severely limiting spike passage³. DC and low frequency pass unattenuated to the regulator. Placing a second ferrite bead at the regulator output before C_{OUT} produces Figure 11's trace. The bead's high frequency loss characteristic further reduces spike amplitude below 1mV without introducing DC resistance into the regulator's output path⁴.

Figure 12, a higher gain version of the previous figure, measures 900 μV spike amplitude – almost 20 \times lower than without the ferrite beads. The measurement is completed by verifying that indicated results are not corrupted by common mode components or ground loops. This is done by grounding the oscilloscope input near the measurement point. Ideally, no signal should appear. Figure 13 shows this to be nearly so, indicating that Figure 12's display is realistic⁵.

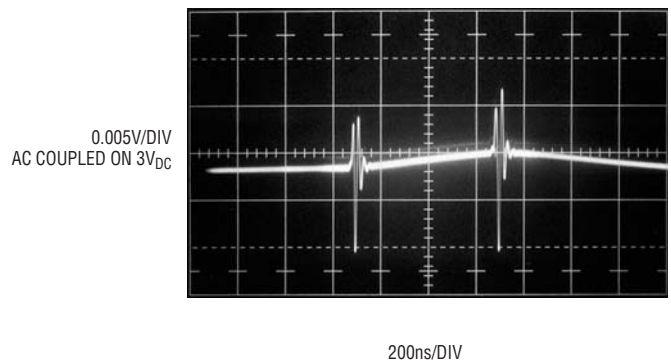


Figure 9. Time and Amplitude Expansion of Figure 8's Output Trace Permits Higher Resolution Study of Spike Characteristics. Trace Center-Screen Area Intensified for Photographic Clarity in This and Succeeding Figures

Note 2: "Dramatic" is perhaps a theatrical descriptive, but certain types find drama in these things.

Note 3: See Appendix A for information on ferrite beads

Note 4: Inductors can sometimes be used in place of beads but their limitations should be understood. See Appendix B.

Note 5: Faithful wideband measurement at sub-millivolt levels requires special considerations. See Appendix C.

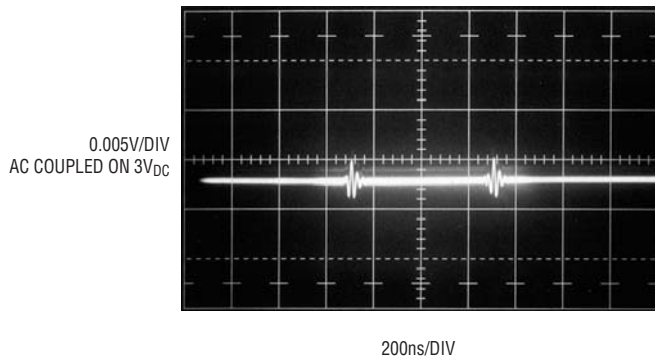


Figure 10. Adding Ferrite Bead to Regulator Input Increases High Frequency Losses, Dramatically Attenuating Spikes

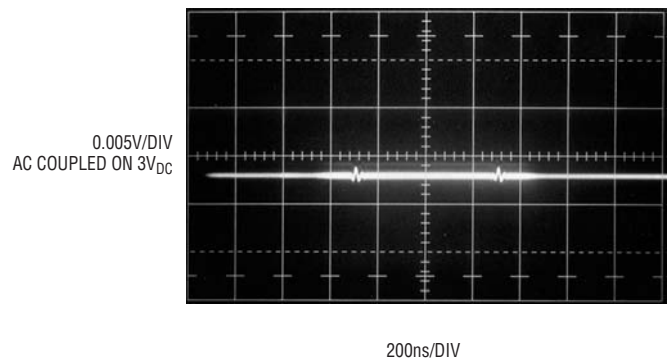


Figure 11. Ferrite Bead in Regulator Output Further Reduces Spike Amplitude

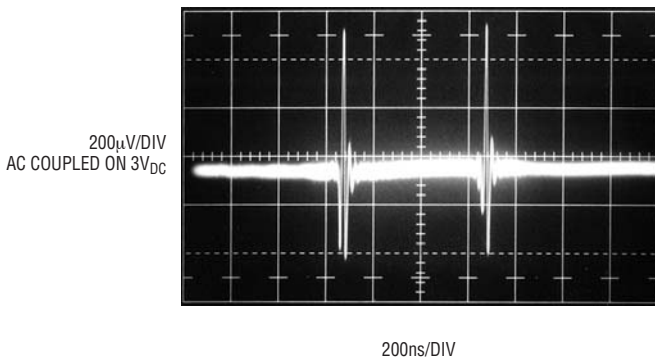


Figure 12. Higher Gain Version of Previous Figure Measures 900µV Spike Amplitude—Almost 20× Lower Than Without Ferrite Beads. Instrumentation Noise Floor Causes Trace Baseline Thickening

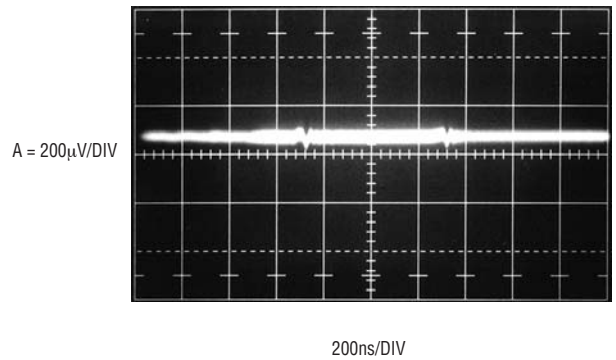


Figure 13. Grounding Oscilloscope Input Near Measurement Point Verifies Figure 12's Results Are Nearly Free of Common Mode Corruption

Application Note 101

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APPENDIX A

About Ferrite Beads

A ferrite bead enclosed conductor provides the highly desirable property of increasing impedance as frequency rises. This effect is ideally suited to high frequency noise filtering of DC and low frequency signal carrying conductors. The bead is essentially lossless within a linear regulator's passband. At higher frequencies the bead's ferrite material interacts with the conductors magnetic field, creating the loss characteristic. Various ferrite materials and geometries result in different loss factors versus frequency and power level. Figure A1's plot shows this. Impedance rises from 0.01Ω at DC to 50Ω at 100MHz . As DC current, and hence constant magnetic field bias, rises, the ferrite becomes less effective in offering loss. Note that beads can be "stacked" in series along a conductor, proportionally increasing their loss contribution. A wide variety of bead materials and physical configurations are available to suit requirements in standard and custom products.

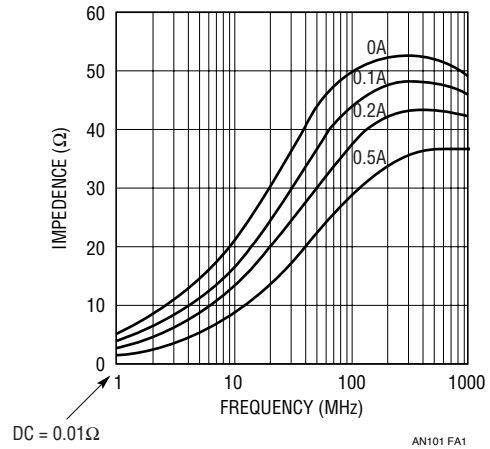


Figure A1. Impedance vs. Frequency at Various DC Bias Currents for a Surface Mounted Ferrite Bead (Fair-Rite 2518065007Y6). Impedance is Essentially Zero at DC and Low Frequency, Rising Above 50Ω Depending on Frequency and DC Current. Source: Fair-Rite 2518065007Y6 Datasheet.

APPENDIX B

Inductors as High Frequency Filters

Inductors can sometimes be used for high frequency filtering instead of beads. Typically, values of $2\mu\text{H}$ to $10\mu\text{H}$ are appropriate. Advantages include wide availability and better effectiveness at lower frequencies, e.g., $\leq 100\text{kHz}$. Figure B1 shows disadvantages are increased DC resistance in the regulator path due to copper losses, parasitic shunt capacitance and potential susceptibility to stray switching regulator radiation. The copper loss appears at DC, reducing efficiency; parasitic shunt capacitance allows

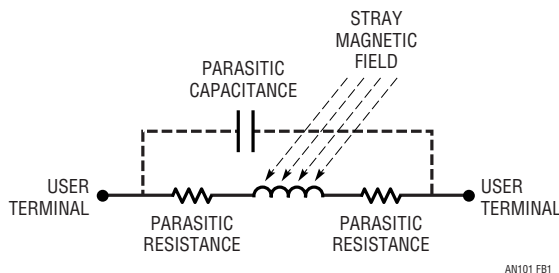


Figure B1. Some Parasitic Terms of an Inductor. Parasitic Resistance Drops Voltage, Degrading Efficiency. Unwanted Capacitance Permits High Frequency Feedthrough. Stray Magnetic Field Induces Erroneous Inductor Current

unwanted high frequency feedthrough. The inductors circuit board position may allow stray magnetic fields to impinge its winding, effectively turning it into a transformer secondary. The resulting observed spike and ripple related artifacts masquerade as conducted components, degrading performance.

Figure B2 shows a form of inductance based filter constructed from PC board trace. Such extended length traces, formed in spiral or serpentine patterns, look inductive at high frequency. They can be surprisingly effective in some circumstances, although introducing much less loss per unit area than ferrite beads.

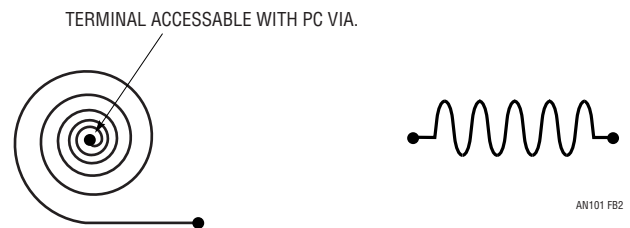


Figure B2. Spiral and Serpentine PC Patterns are Sometimes Used as High Frequency Filters, Although Less Effective Than Ferrite Beads

Application Note 101

APPENDIX C

Probing Technique for Sub-Millivolt, Wideband Signal Integrity

Obtaining reliable, wideband, sub-millivolt measurements requires attention to critical issues before measuring anything. A circuit board layout designed for low noise is essential. Consider current flow and interactions in power distribution, ground lines and planes. Examine the effects of component choice and placement. Plan radiation management and disposition of load return currents. If the circuit is sound, the board layout proper and appropriate components used, then, and only then, may meaningful measurement proceed.

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. Low level, wideband measurements demand care in routing signals to test instrumentation. Issues to consider include ground loops between pieces of test equipment (including the power supply) connected to the breadboard and noise pickup due to excessive test lead or trace length. Minimize the number of connections to the circuit board and keep leads short. Wideband signals to or from the breadboard must be routed in a coaxial environment with attention to where the coaxial shields tie into the ground system. A strictly maintained coaxial environment is particularly critical for reliable measurements and is treated here¹.

Figure C1 shows a believable presentation of a typical

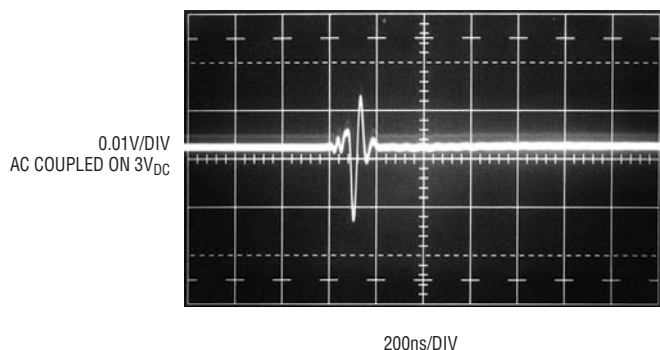


Figure C1. Spike Measured Within Continuous Coaxial Signal Path Displays Moderate Disturbance and Ringing After Main Event

switching regulator spike measured within a continuous coaxial signal path. The spike's main body is reasonably well defined and disturbances after it are contained. Figure C2 depicts the same event with a 3 inch ground lead connecting the coaxial shield to the circuit board ground plane. Pronounced signal distortion and ringing occur. The photographs were taken at 0.01V/division sensitivity. More sensitive measurement requires proportionately more care.

Figure C3 details use of a wideband 40dB gain pre-amplifier permitting text Figure 12's 200 μ V/division measurement. Note the purely coaxial path, including the AC coupling capacitor, from the regulator, through the pre-amplifier and to the oscilloscope. The coaxial coupling capacitor's shield is directly connected to the regulator board's ground plane with the capacitor center conductor going to the regulator output. There are no non-coaxial measurement connections. Figure C4, repeating text Figure 12, shows a cleanly detailed rendition of the 900 μ V output spikes. In Figure C5 two inches of ground lead has been deliberately introduced at the measurement site, violating the coaxial regime. The result is complete corruption of the waveform presentation. As a final test to verify measurement integrity, it is useful to repeat Figure C4's measurement with the signal path input (e.g., the coaxial coupling capacitor's center conductor) grounded near the measurement point as in text Figure 13. Ideally, no signal should appear. Practically, some *small* residue, primarily due to common mode effects, is permissible.

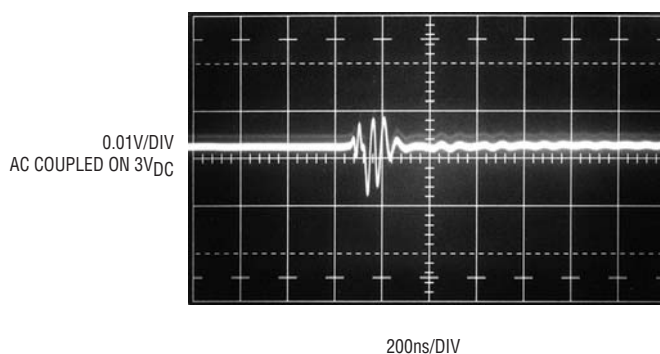


Figure C2. Introducing 3" Non-Coaxial Ground Connection Causes Pronounced Signal Distortion and Post-Event Ringing

Note 1: More extensive treatment of these and related issues appears in the appended sections of References 1 and 2. Board layout considerations for low level, wideband signal integrity appear in Appendix G of Reference 3.

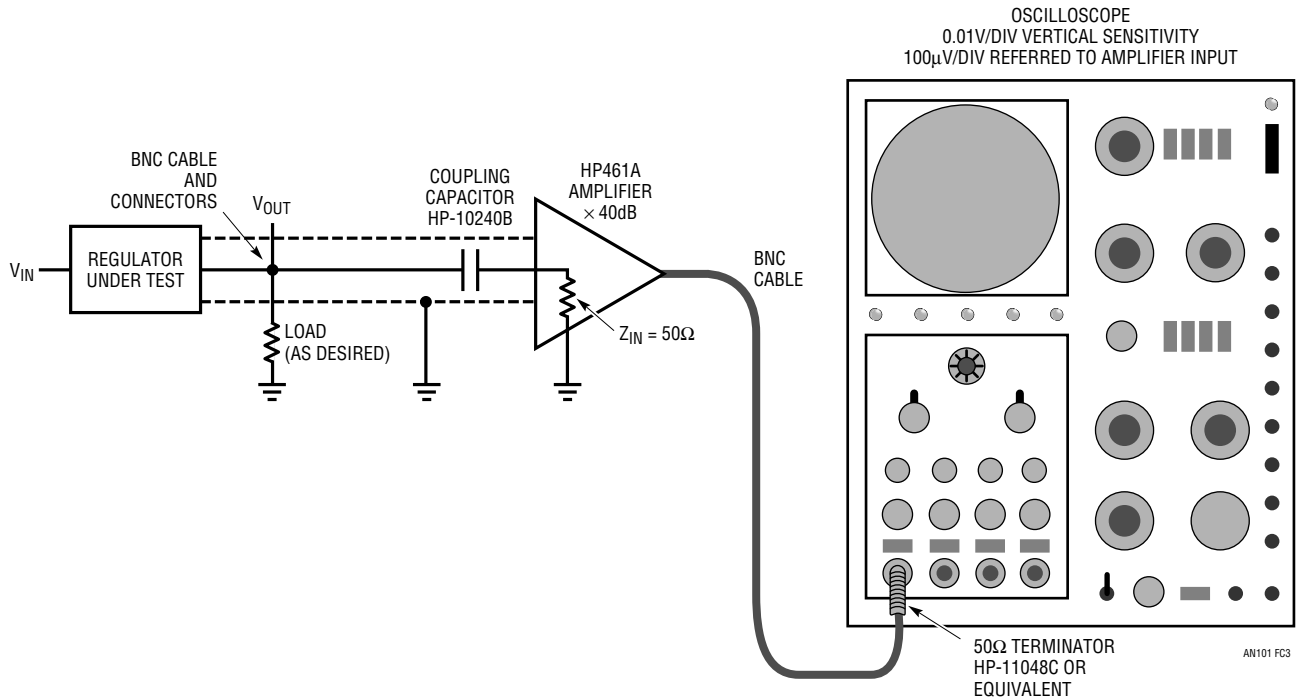


Figure C3. Wideband, Low Noise Pre-Amplifier Permits Sub-Millivolt Spike Observation. Coaxial Connections Must be Maintained to Preserve Measurement Integrity

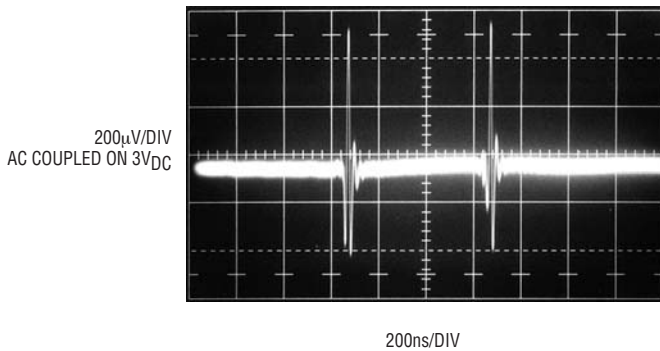


Figure C4. Low Noise Pre-Amplifier and Strictly Enforced Coaxial Signal Path Yield Text Figure 12's 900mV_{P-P} Presentation. Trace Baseline Thickening Represents Pre-Amplifier Noise Floor

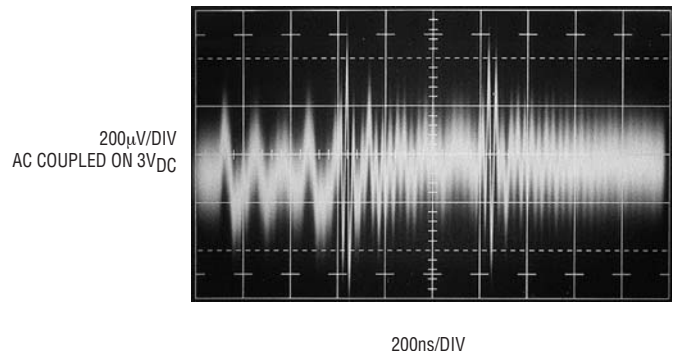


Figure C5. 2 Inch Non-Coaxial Ground Connection at Measurement Site Completely Corrupts Waveform Presentation

Application Note 101



Megahertz to Minihertz Converter

— Willw₀₅ —

Load Transient Response Testing for Voltage Regulators

Practical Considerations for Testing and Evaluating Results

Jim Williams

INTRODUCTION

Semiconductor memory, card readers, microprocessors, disc drives, piezoelectric devices and digitally based systems furnish transient loads that a voltage regulator must service. Ideally, regulator output is invariant during a load transient. In practice, some variation is encountered and becomes problematic if allowable operating voltage tolerances are exceeded. This mandates testing the regulator and its associated support components to verify desired performance under transient loading conditions. Various methods are employable to generate transient loads, allowing observation of regulator response.

Basic Load Transient Generator

Figure 1 diagrams a conceptual load transient generator. The regulator under test drives DC and switched resistive loads, which may be variable. The switched current and

output voltage are monitored, permitting comparison of the nominally stable output voltage versus load current under static and dynamic conditions. The switched current is either on or off; there is no controllable linear region.

Figure 2 is a practical implementation of the load transient generator. The voltage regulator under test is augmented by capacitors which provide an energy reservoir, similar to a mechanical flywheel, to aid transient response. The size, composition and location of these capacitors, particularly C_{OUT} , has a pronounced effect on transient response and overall regulator stability.¹ Circuit operation is straightforward. The input pulse triggers the LTC1693 FET driver to switch Q1, generating a transient load current out of the

Note 1. See Appendix A, "Capacitor Parasitic Effects on Load Transient Response" and Appendix B, "Output Capacitors and Stability" for extended discussion.

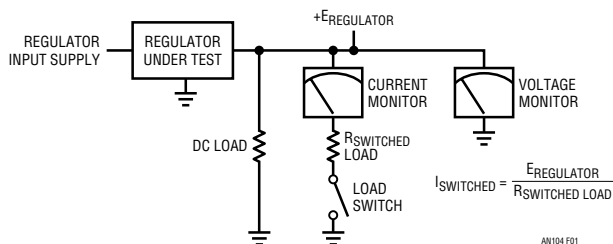


Figure 1. Conceptual Regulator Load Tester Includes Switched and DC Loads and Voltage/Current Monitors. Resistor Values Set DC and Switched Load Currents. Switched Current is Either On or Off; There is No Controllable Linear Region

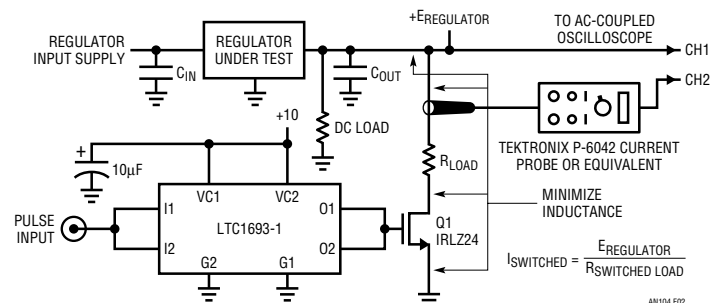


Figure 2. A Practical Regulator Load Tester. FET Driver and Q1 Switch R_{LOAD} . Oscilloscope Monitors Current Probe Output and Regulator Response

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Application Note 104

regulator. An oscilloscope monitors the instantaneous load voltage and, via a “clip-on” wideband probe, current. The circuit’s load transient generating capabilities are evaluated in Figure 3 by substituting an extraordinarily low impedance power source for the regulator. The combination of a high capacity power supply, low impedance connections and generous bypassing maintains low impedance across frequency. Figure 4 shows Figure 3 responding to the LTC1693-1 FET driver (Trace A) by cleanly switching 1A in 15ns (Trace B). Such speed is useful for simulating many loads but has restricted versatility. Although fast, the circuit cannot emulate loads between the minimum and maximum currents.

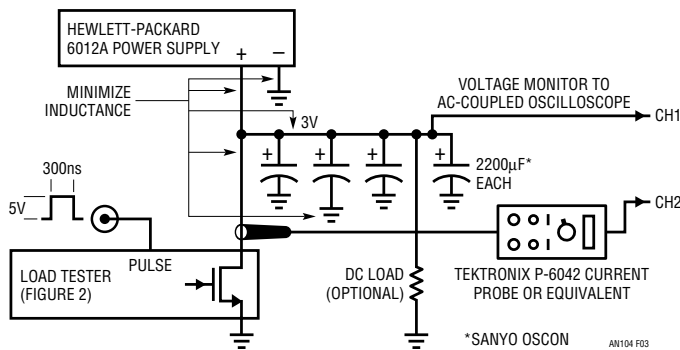


Figure 3. Substituting Well Bypassed, Low Impedance Power Supply for Regulator Allows Determining Load Tester’s Response Time

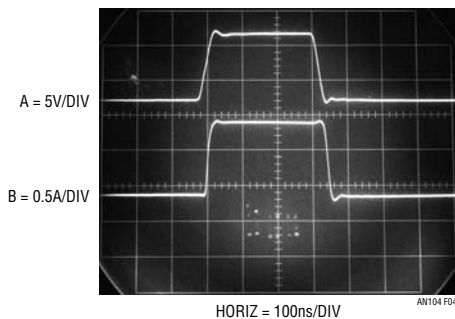


Figure 4. Figure 2’s Circuit Responds to FET Driver Output (Trace A), Switching a 1A Load (Trace B) in 15ns

Closed Loop Load Transient Generators

Figure 5’s conceptual closed loop load transient generator linearly controls Q1’s gate voltage to set instantaneous transient current at any desired point, allowing simulation of nearly any load profile. Feedback from Q1’s source to the A1 control amplifier closes a loop around Q1, stabilizing its

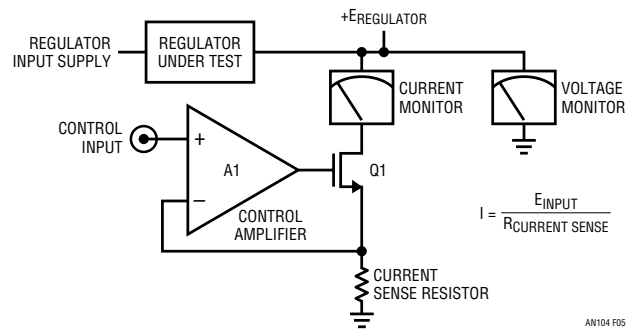


Figure 5. Conceptual Closed Loop Load Tester. A1 Controls Q1’s Source Voltage, Setting Regulator Output Current. Q1’s Drain Current Waveshape is Identical to A1 Input, Allowing Linear Control of Load Current. Voltage and Current Monitors are as in Figure 1

operating point. Q1’s current assumes a value dependant on the control input voltage and the current sense resistor over a very wide bandwidth. Note that once A1 biases to Q1’s conductance threshold, small variations in A1’s output result in large current changes in Q1’s channel. As such, large output excursions are not required from A1; its small signal bandwidth is the fundamental speed limitation. Within this restriction, Q1’s current waveform is identically shaped to A1’s control input voltage, allowing linear control of load current. This versatile capability permits a wide variety of simulated loads.

FET Based Circuit

Figure 6, a practical incarnation of a FET based closed loop load transient generator, includes DC bias and waveform inputs. A1 must drive Q1’s high capacitance gate at high frequency, necessitating high peak A1 output currents and attention to feedback loop compensation. A1, a 60MHz current feedback amplifier, has an output current capacity exceeding 1A. Maintaining stability and waveform fidelity at high frequency while driving Q1’s gate capacitance necessitates settable gate drive peaking components, a damper network, feedback trimming and loop peaking adjustments. A DC trim, also required, is made first. With no input applied, trim the “1mV adjust” for 1mV DC at Q1’s source. The AC trims are made utilizing Figure 7’s arrangement. Similar to Figure 3, this “brick wall” regulated source provides minimal ripple and sag when step loaded by the load transient generator. Apply the inputs shown and trim the gate drive, feedback and loop peaking adjustments for the cleanest, square cornered response on the oscilloscope’s current probe equipped channel.

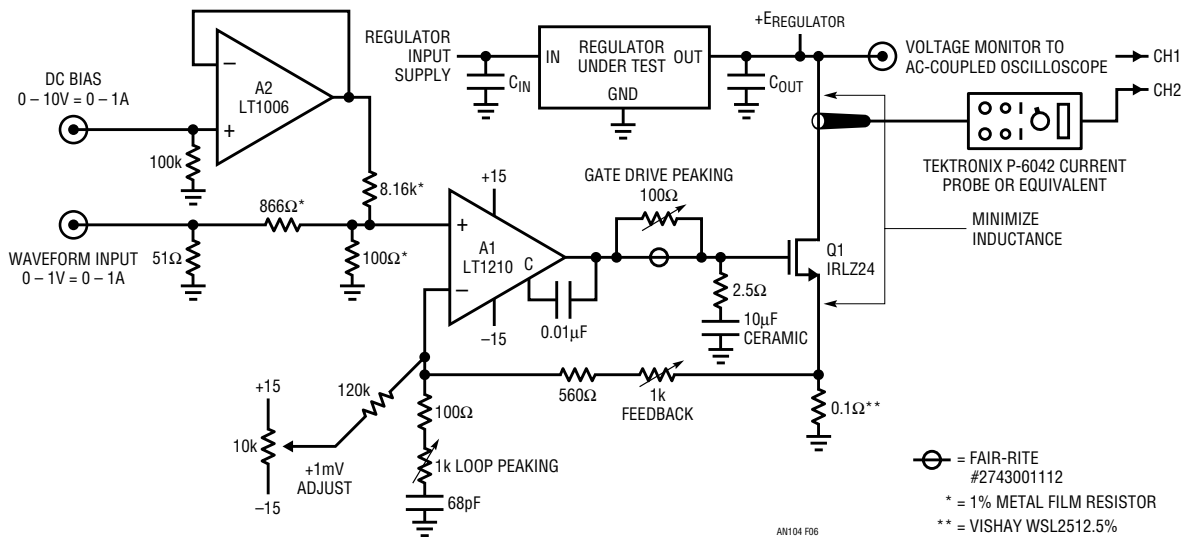


Figure 6. Detailed Closed Loop Load Tester. DC Level and Pulse Inputs Feed A1 to Q1 Current Sinking Regulator Load. Q1's Gain Allows Small A1 Output Swing, Permitting Wide Bandwidth. Damper Network, Feedback and Peaking Trims Optimize Edge Response

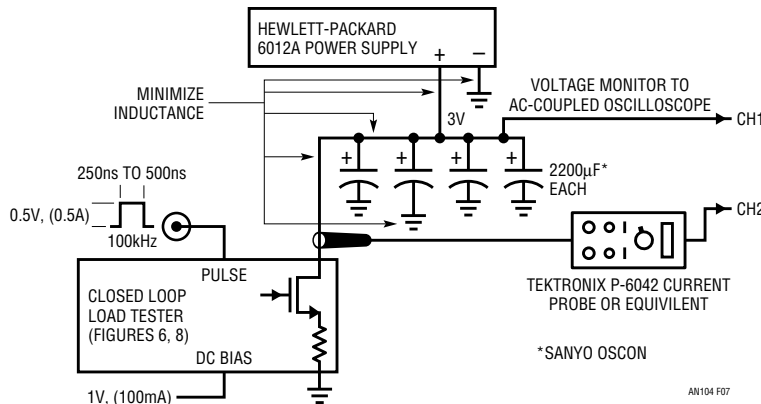


Figure 7. Closed Loop Load Tester Response Time is Determined as in Figure 3. "Brick Wall" Input Provides Low Impedance Source

Bipolar Transistor Based Circuit

Figure 8 considerably simplifies the previous circuit's loop dynamics and eliminates all AC trims. The major trade-off is a 2x speed reduction. The circuit is similar to Figure 6, except that Q1 is a bipolar transistor. The bipolar's greatly reduced input capacitance allows A1 to drive a more benign load. This permits a lower output current amplifier and eliminates the dynamic trims required to accommodate Figure 6's FET gate capacitance. The sole trim is the "1mV adjust" which is accomplished as described before². Aside from the 2x speed reduction the bipolar transistor also introduces a 1% output current error due to its base current.

Note 2. This trim may be eliminated at some sacrifice in circuit complexity. See Appendix D, "A Trimless Closed Loop Transient Load Tester".

Q2 is added to prevent excessive Q1 base current when the regulator supply is not present. The diode prevents reverse base bias under any circumstances.

Closed Loop Circuit Performance

Figures 9 and 10 show the two wideband circuits' operation. The FET based circuit (Figure 9) only requires a 50mV A1 swing (Trace A) to enforce Trace B's flat-topped current pulse with 50ns edges through Q1. Figure 10 details the bipolar transistor based circuit's performance. Trace A, taken at Q1's base, rises less than 100mV causing Trace B's clean 1A current conduction through Q1. This circuit's 100ns edges, about 2x slower than the more complex FET based version, are still fast enough for most practical transient load testing.

Application Note 104

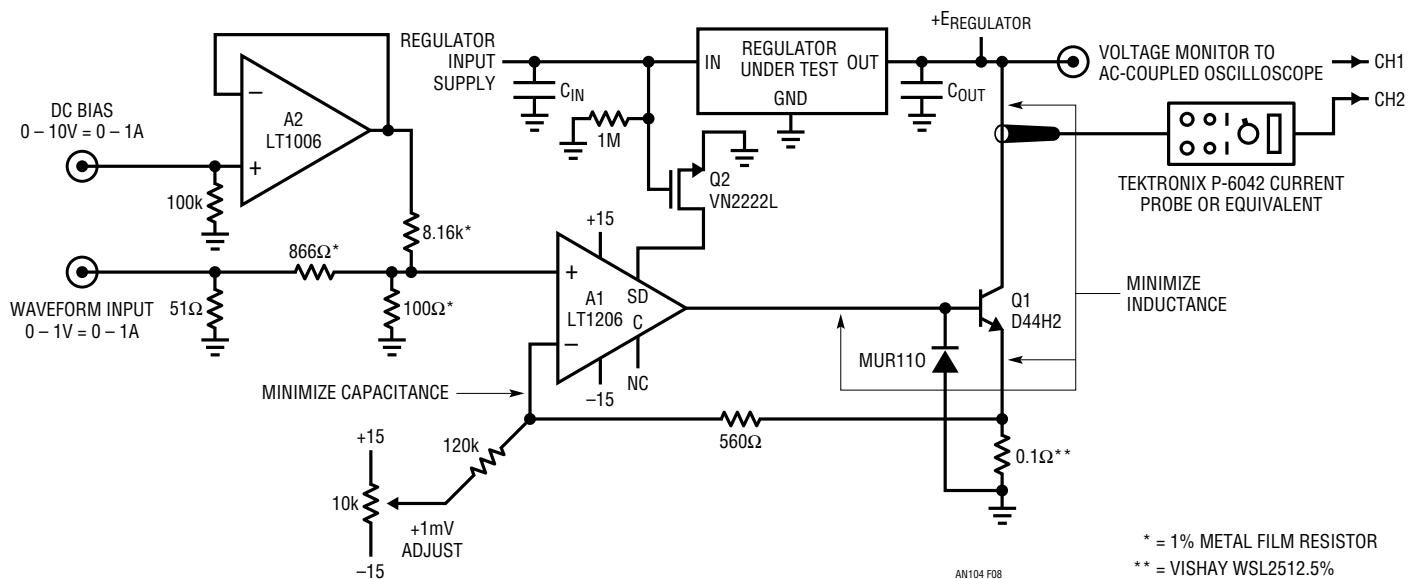


Figure 8. Figure 6 Implemented with Bipolar Transistor. Q1's Reduced Input Capacitance Simplifies Loop Dynamics, Eliminating Compensation Components and Trims. Trade Off is 2x Speed Reduction and Base Current Induced 1% Error

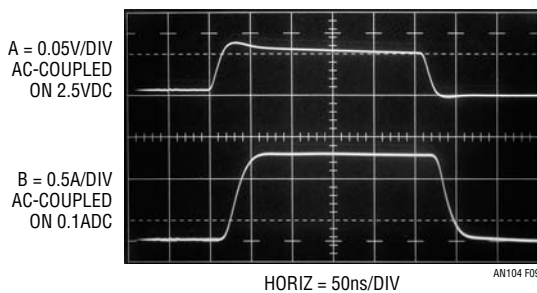


Figure 9. Figure 6's Closed Loop Load Tester Step Response (Q1 Current is Trace B) is Quick and Clean, Showing 50ns Edges and Flat Top. A1's Output (Trace A) Swings Only 50mV, Allowing Wideband Operation. Trace B's Presentation is Slightly Delayed Due to Voltage and Current Probe Time Skew

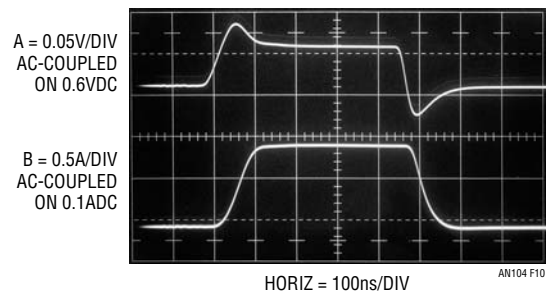


Figure 10. Figure 8's Bipolar Output Load Tester Response is 2x Slower than FET Version, but Circuit is Less Complex and Eliminates Compensation Trims. Trace A is A1's Output, Trace B is Q1's Collector Current

Load Transient Testing

The previously discussed circuits permit rapid and thorough voltage regulator load transient testing. Figure 11 uses Figure 6's circuit to evaluate an LT1963A linear regulator. Figure 12 shows regulator response (Trace B) to Trace A's asymmetrically edged input pulse. The ramped leading edge, within the LT1963A's bandwidth, results in Trace B's smooth 10mV_{P-P} excursion. The fast trailing edge, well outside LT1963A passband, causes Trace B's abrupt disruption. C_{OUT} cannot supply enough current to maintain output level and a 75mV_{P-P} spike results before the regulator resumes control. In Figure 13, a 500mA peak-to-peak 500kHz noise load, emulating a multitude of incoherent

loads, feeds the regulator in Trace A. This is within regulator bandwidth and only 6mV_{P-P} of disturbance appears in Trace B, the regulator output. Figure 14 maintains the same conditions, except that noise bandwidth is increased to 5MHz. Regulator bandwidth is exceeded, resulting in over 50mV_{P-P} error, an 8x increase.

Figure 15 shows what happens when a 0.2A DC biased, swept DC-5MHz, 0.35A load is presented to the regulator. The regulator's rising output impedance versus frequency results in ascending error as frequency scales. This information allows determination of regulator output impedance versus frequency.

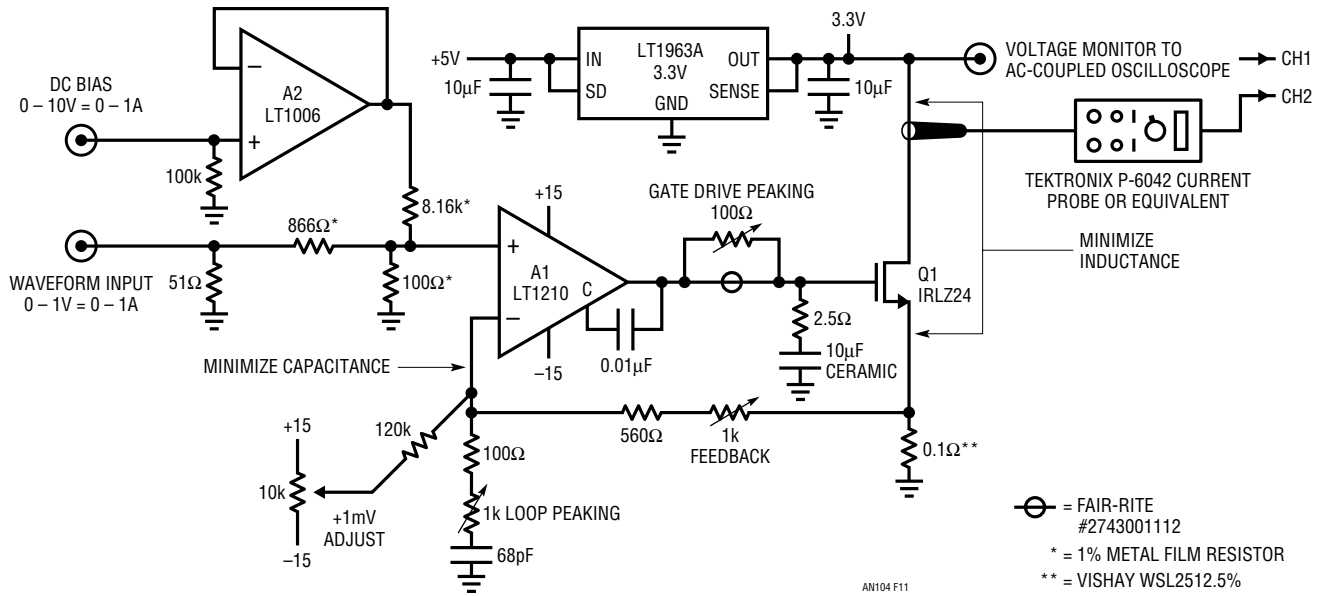


Figure 11. Closed Loop Load Tester Shown with LT1963A Regulator. Load Testing for a Variety of Current Load Waveshapes is Possible

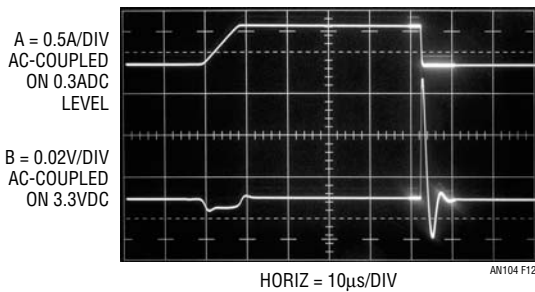


Figure 12. Figure 11 Responds (Trace B) to Asymmetrically Edged Pulse Input (Trace A). Ramped Leading Edge, Within LT1963A Bandwidth, Results in Trace B's Smooth 10mV_{p-p} Excursion. Fast Trailing Edge, Outside LT1963A Bandwidth, Causes Trace B's Abrupt 75mV_{p-p} Disruption. Traces Latter Portion Intensified for Photographic Clarity

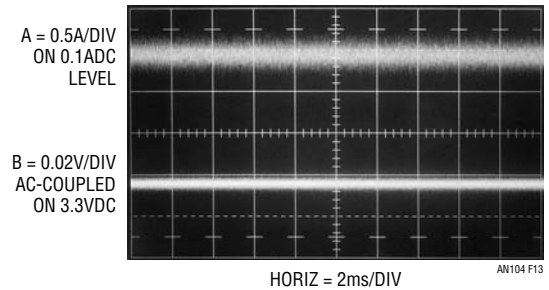


Figure 13. 500mA_{p-p}, 500kHz Noise Load (Trace A), Within Regulator Bandpass, Produces Only 6mV Artifacts at Trace B's Regulator Output

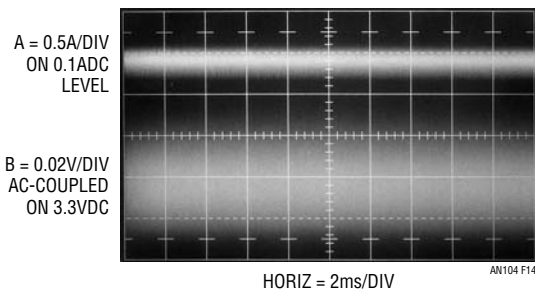


Figure 14. Same Conditions as Figure 13, Except Noise Bandwidth Increased to 5MHz. Regulator Bandwidth is Exceeded, Resulting in 50mV_{p-p} Output Error

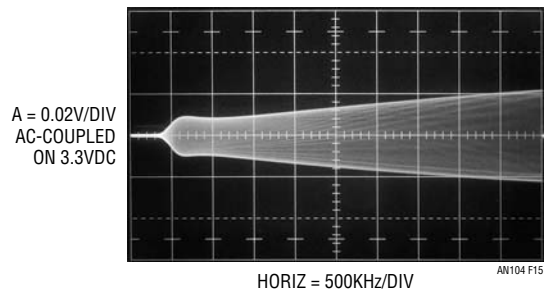


Figure 15. Swept DC - 5MHz, 0.35A Load (On 0.2ADC) Results in Above Regulator Response. Regulator Output Impedance Rises with Frequency, Causing Corresponding Ascending Output Error

Application Note 104

Capacitor's Role in Regulator Response

The regulator employs capacitors at its input (C_{IN}) and output (C_{OUT}) to augment its high frequency response. The capacitor's dielectric, value and location greatly influence regulator characteristics and must be quite carefully considered.³ C_{OUT} dominates the regulator's dynamic response; C_{IN} is much less critical, so long as it does not discharge below the regulator's dropout point. Figure 16 shows a typical regulator circuit and emphasizes C_{OUT} and its parasitics. Parasitic inductance and resistance limit capacitor effectiveness at frequency. The capacitor's dielectric and value significantly influence load step response. A "hidden" parasitic, impedance build-up in regulator output trace runs, also influences regulation characteristics, although its effects can be minimized by remote sensing (shown) and distributed capacitive bypassing.

Figure 17 shows Figure 16's circuit responding (Trace B) to a 0.5A load step biased on 0.1A DC (Trace A) with

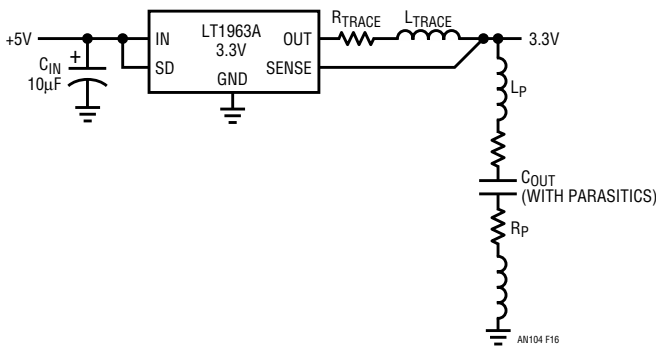


Figure 16. C_{OUT} Dominates Regulator's Dynamic Response; C_{IN} is Much Less Critical. Parasitic Inductance and Resistance Limit Capacitor Effectiveness at Frequency. Capacitor Value and Dielectric Significantly Influence Load Step Response. Excessive Trace Impedance is Also a Factor

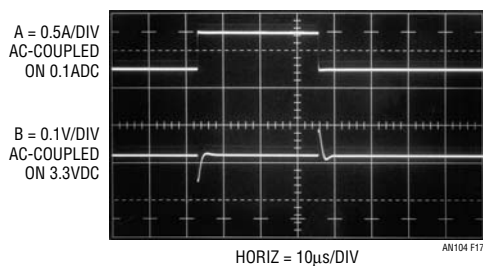


Figure 17. Stepped 0.5A Load to Figure 16's Circuit (Trace A) with $C_{IN} = C_{OUT} = 10\mu\text{F}$ Results in Trace B's Regulator Output. Low Loss Capacitors Promote Controlled Output Excursions

Note 3. See Appendices A and B for extended discussion of these concerns.

$C_{IN} = C_{OUT} = 10\mu\text{F}$. The low loss capacitors employed result in Trace B's well controlled output. Figure 18 greatly expands the horizontal time scale to investigate high frequency behavior. Regulator output deviation (Trace B) is smooth, with no abrupt discontinuities. Figure 19 runs the same test as Figure 17 using an output capacitor claimed as "equivalent" to the one employed in Figure 17. At $10\mu\text{s}/\text{division}$ things seem very similar, but Figure 20 indicates problems. This photo, taken at the same higher sweep speed as Figure 18, reveals the "equivalent" capacitor to have a 2x amplitude error versus Figure 18, higher frequency content and

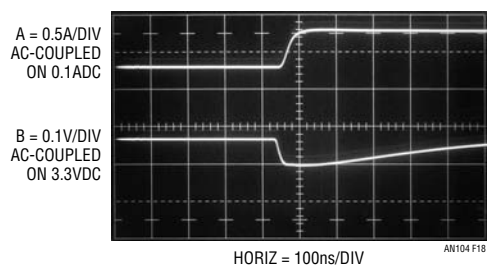


Figure 18. Expanding Horizontal Scale Shows Trace B's Smooth Regulator Output Response. Mismatched Current and Voltage Probe Delays Account for Slight Time Skewing

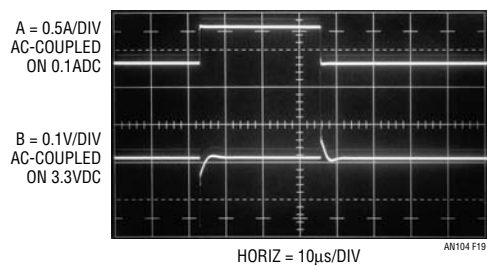


Figure 19. "Equivalent" $10\mu\text{F}$ C_{OUT} Capacitor's Performance Appears Similar to Figure 17's Type at $10\mu\text{s}/\text{DIV}$

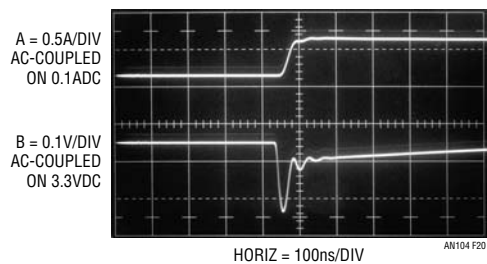


Figure 20. Horizontal Scale Expansion Reveals "Equivalent" Capacitor Produces 2x Amplitude Error vs Figure 18. Mismatched Probe Delays Cause Time Skewing Between Traces

resonances.⁴ Figure 21 substitutes a very lossy 10 μ F unit for C_{OUT} . This capacitor allows a 400mV excursion (note Trace B's vertical scale change), >4x Figure 18's amount. Conversely, Figure 22 increases C_{OUT} to a low loss 33 μ F type, decreasing Trace B's output response transient by 40% versus Figure 18. Figure 23's further increase, to a low loss 330 μ F capacitor, keeps transients inside 20mV; 4x lower than Figure 18's 10 μ F value.

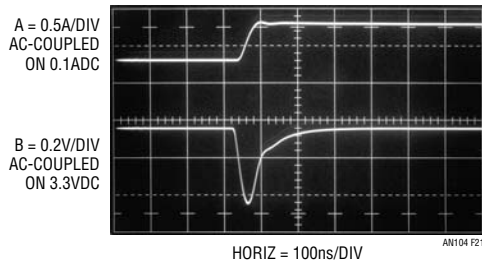


Figure 21. Excessively Lossy 10 μ F C_{OUT} Allows 400mV Excursion – 4x Figure 18's Amount. Time Skewing Between Traces Derives from Probe Mismatch

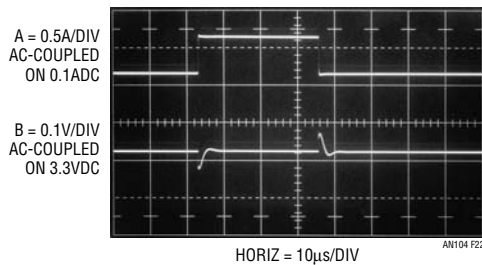


Figure 22. Increasing C_{OUT} with Low Loss 33 μ F Unit Reduces Output Response Transient by 40% Over Figure 17

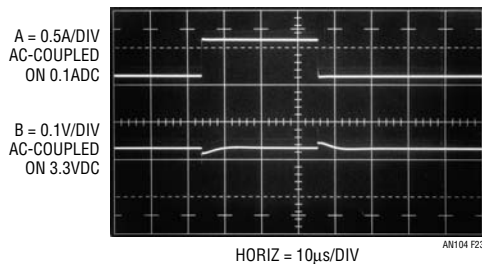


Figure 23. Low Loss 330 μ F Capacitor Keeps Output Response Transients Inside 20mV – 4x Lower than Figure 17's 10 μ F

The lesson from the preceding study is clear. Capacitor value and dielectric quality have a pronounced effect on transient load response. Try before specifying!

Load Transient Risettime versus Regulator Response

The closed loop load transient generator also allows investigating load transient risetime on regulation at high speed. Figure 24 shows Figure 16's circuit ($C_{IN} = C_{OUT} = 10\mu$ F) responding to a 0.5A, 100ns risetime step on a 0.1A DC load (Trace A). Response decay (Trace B) peaks at 75mV with some following aberrations. Decreasing Trace A's load step risetime (Figure 25) almost doubles Trace B's response error, with attendant enlarged following aberrations. This indicates increased regulator error at higher frequency.

All regulators present increasing error with frequency, some more so than others. A slow load transient can unfairly make a poor regulator look good. Transient load testing that does not indicate some response outside regulator bandwidth is suspect.

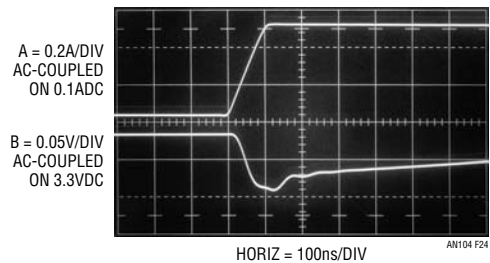


Figure 24. Regulator Output Response (Trace B) to 100ns. Risettime Current Step (Trace A) for $C_{OUT} = 10\mu$ F. Response Decay Peaks at 75mV

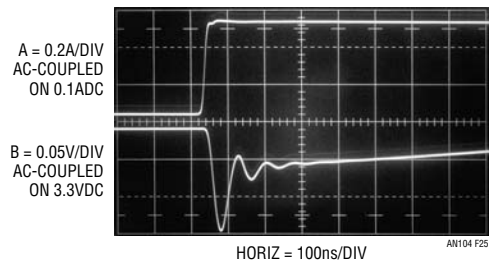


Figure 25. Faster Risettime Current Step (Trace A) Increases Response Decay Peak (Trace B) to 140mV, Indicating Increased Regulation Loss vs Frequency

Note 4. Always specify components according to observed performance, never to salesman's claims.

Application Note 104

A Practical Example – Intel P30 Embedded Memory Voltage Regulator

A good example of the importance of voltage regulator load step performance is furnished by the Intel P30 embedded memory. This memory requires a 1.8V supply, typically regulated down from +3V. Although current requirements are relatively modest, supply tolerances are tight. Figure 26's error budget shows only 0.1V allowable excursion from 1.8V, including all DC and dynamic errors. The LTC1844-1.8 regulator has a 1.75% initial tolerance (31.5mV), leaving only a 68.5mV dynamic error allowance. Figure 27 is the test circuit. Memory control line movement causes 50mA load transients, necessitating attention to capacitor selection.⁵ If the regulator is close to the power source C_{IN} is optional. If not, use a good grade 1 μ F capacitor for C_{IN} . C_{OUT} is a low loss 1 μ F type. In all other respects the circuit appears deceptively routine. A load transient generator provides Figure 28's output load test step

Intel P30 Embedded Memory Voltage Regulator Error Budget

PARAMETER	LIMITS
Intel Specified Supply Limits	1.8V \pm 0.1V
LTC1844 Regulator Initial Accuracy	\pm 1.75% (\pm 31.5mV)
Dynamic Error Allowance	\pm 68.5mV

Figure 26. Error Budget for Intel P30 Embedded Memory Voltage Regulator. 1.8V Supply Must Remain Within \pm 0.1V Tolerance, Including All Static and Dynamic Errors

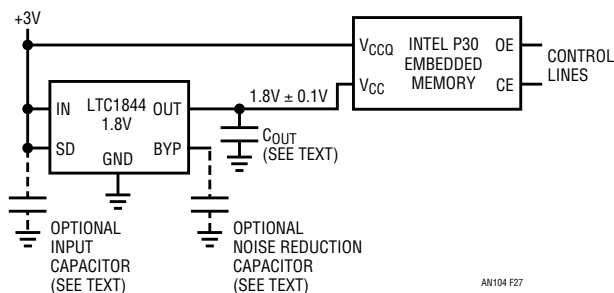


Figure 27. P30 Embedded Memory V_{CC} Regulator Must Maintain \pm 0.1V Error Band. Control Line Movement Causes 50mA Load Steps, Necessitating Attention to C_{OUT} Selection

Note 5. The LTC1844-1.8's noise bypass pin ("BYP") is used with an optional external capacitor to achieve extremely low output noise. It is not required for this application and is left unconnected.

(Trace A).⁶ Trace B's regulator response shows just 30mV peaks, $>2x$ better than required. Increasing C_{OUT} to 10 μ F, in Figure 29, reduces peak output error to 12mV, almost 6x better than specification. However, a poor grade 10 μ F (or 1 μ F, for that matter) capacitor produces Figure 30's unwelcome surprise. Severe peaking error on both edges occurs (Trace B's latter portion has been intensified to aid photograph clarity) with 100mV observable on the negative going edge. This is well outside the error budget and would cause unreliable memory operation.

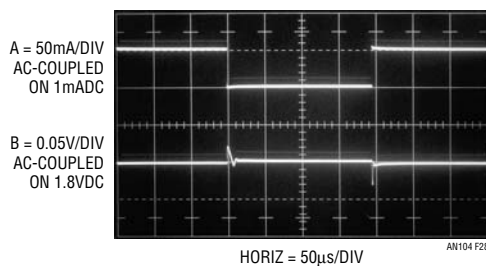


Figure 28. 50mA Load Step (Trace A) Results in 30mV Regulator Response Peaks, 2x Better than Error Budget Requirements. C_{OUT} = Low Loss 1 μ F

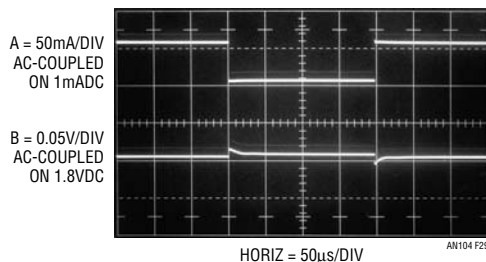


Figure 29. Increasing C_{OUT} to 10 μ F Decreases Regulator Output Peaks to 12mV, Almost 6x Better than Required

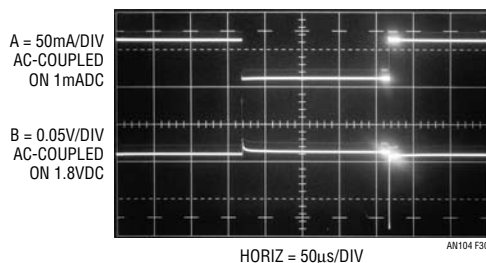


Figure 30. Poor Grade 10 μ F C_{OUT} Causes 100mV Regulator Output Peaks (Trace B), Violating P30 Memory Limits. Traces Latter Portion Intensified for Photographic Clarity

Note 6. Figure 8's circuit was used for this test, with Q1's emitter current shunt changed to 1 Ω .

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1. LT1584/LT1585/LT1587 Fast Response Regulators Datasheet. Linear Technology Corporation.
2. LT1963A Regulator Datasheet. Linear Technology Corporation.
3. Williams, Jim, "Minimizing Switching Residue in Linear Regulator Outputs". Linear Technology Corporation, Application Note 101, July 2005
4. Shakespeare, William, "The Taming of the Shrew," 1593–94.

Note. This application note was derived from a manuscript originally prepared for publication in EDN magazine.

APPENDIX A

Capacitor Parasitic Effects on Load Transient Response

Tony Bonte

Large load current changes are typical of digital systems. The load current step contains higher order frequency components that the output decoupling network must handle until the regulator throttles to the load current level. Capacitors are not ideal elements and contain parasitic resistance and inductance. These parasitic elements dominate the change in output voltage at the beginning of a transient load step change. The ESR (equivalent series resistance) of the output capacitors produces an instantaneous step in output voltage. ($\Delta V = \Delta I \cdot \text{ESR}$). The ESL (equivalent series inductance) of the output capacitors produces a droop proportional to the rate of change of output current ($V = L \cdot \Delta I / \Delta t$). The output capacitance produces a change in output voltage proportional to the

time until the regulator can respond ($\Delta V = \Delta t \cdot \Delta I / C$). These transient effects are illustrated in Figure A1.

The use of capacitors with low ESR, low ESL, and good high frequency characteristics is critical in meeting the output load voltage tolerances. These requirements dictate high quality, surface mount tantalum, ceramic or organic electrolyte capacitors. The capacitor's location is critical to transient response performance. Place the capacitor as close as possible to the regulator pins and keep supply line traces and planes at low impedance, bypassing individual loads as necessary. If the regulator has remote sensing capability, consider sensing at the heaviest load point.

Strictly speaking, the above are not the only time related terms that can influence regulator settling. Figure A2 lists 7 different terms, occurring over 9 decades of time, that can potentially influence regulation. The regulator IC must be carefully designed to minimize regulator loop and thermal error contributions.

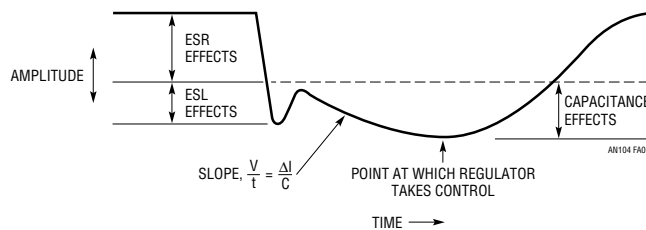


Figure A1. Parasitic Resistance, Inductance and Finite Capacitance Combine with Regulator Gain-Bandwidth Limitations to Form Load Step Response. Capacitors Equivalent Series Resistance (ESR) and Inductance (ESL) Dominate Initial Response; Capacitor Value and Regulator Gain-Bandwidth Determine Responses Latter Profile

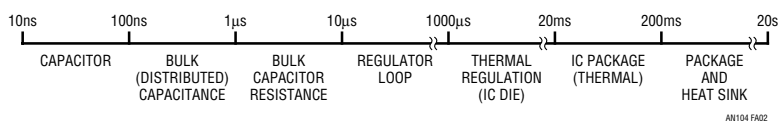


Figure A2. Time Constants Potentially Influencing Regulator Settling Time After a Load Step are Electrical and Thermal. Effects Span Over 9 Decades

APPENDIX B

Output Capacitors and Loop Stability

Dennis O'Neill

Editorial Note: The following text, excerpted from the LT1963A datasheet, concerns the output capacitor's relationship to transient response. Although originally prepared for LT1963A application, it is generalizable to most regulators and is presented here for reader convenience.

A voltage regulator is a feedback circuit. Like any feedback circuit, frequency compensation is needed to make it stable. For the LT1963A, the frequency compensation is both internal and external – the output capacitor. The size of the output capacitor, the type of the output capacitor, and the ESR of the particular output capacitor all affect the stability.

In addition to stability, the output capacitor also affects the high frequency transient response. The regulator loop has finite bandwidth. For high frequency transient loads recovery from a transient is a combination of the output capacitor and the bandwidth of the regulator. The LT1963A was designed to be easy to use and accept a wide variety of output capacitors. However, the frequency compensation is affected by the output capacitor and optimum frequency stability may require some ESR, especially with ceramic capacitors.

For ease of use, low ESR polytantalum capacitors (POSCAP) are a good choice for both the transient response and stability of the regulator. These capacitors have intrinsic ESR that improves the stability. Ceramic capacitors have extremely low ESR, and while they are a good choice in many cases, placing a small series resistance element will sometimes achieve optimum stability and minimize ringing. In all cases, a minimum of 10 μ F is required while the maximum ESR allowable is 3 Ω .

The place where ESR is most helpful with ceramics is low output voltage. At low output voltages, below 2.5V, some ESR helps the stability when ceramic output capacitors are used. Also, some ESR allows a smaller capacitor value to be used. When small signal ringing occurs with ceramics due to insufficient ESR, adding ESR or increasing the capacitor value improves the stability and reduces the ringing. Figure B1 gives some recommended values

V _{OUT}	10 μ F	22 μ F	47 μ F	100 μ F
1.2V	20m Ω	15m Ω	10m Ω	5m Ω
1.5V	20m Ω	15m Ω	10m Ω	5m Ω
1.8V	15m Ω	10m Ω	10m Ω	5m Ω
2.5V	5m Ω	5m Ω	5m Ω	5m Ω
3.3V	0m Ω	0m Ω	0m Ω	5m Ω
\geq 5V	0m Ω	0m Ω	0m Ω	0m Ω

Figure B1. Capacitor Minimum ESR

of ESR to minimize ringing caused by fast, hard current transitions.

Figures B2 through B7 show the effect of ESR on the transient response of the regulator. These scope photos show the transient response for the LT1963A at three different output voltages with various capacitors and various values of ESR. The output load conditions are the same for all traces. In all cases there is a DC load of 500mA. The load steps up to 1A at the first transition and steps back to 500mA at the second transition.

At the worst case point of 1.2V_{OUT} with 10 μ F C_{OUT} (Figure B2), a minimum amount of ESR is required. While 20m Ω is enough to eliminate most of the ringing, a value closer to 50m Ω provides a more optimum response. At 2.5V output with 10 μ F C_{OUT} (Figure B3) the output rings at the transitions with 0 Ω ESR but still settles to within 10mV in 20 μ s after the 0.5A load step. Once again a small value of ESR will provide a more optimum response.

At 5V_{OUT} with 10 μ F C_{OUT} (Figure B4) the response is well damped with 0 Ω ESR.

With a C_{OUT} of 100 μ F at 0 Ω ESR and an output of 1.2V (Figure B5), the output rings although the amplitude is only 20mV_{P-P}. With C_{OUT} of 100 μ F it takes only 5m Ω to 20m Ω of ESR to provide good damping at 1.2V output. Performance at 2.5V and 5V output with 100 μ F C_{OUT} shows similar characteristics to the 10 μ F case (see Figures B6 to B7). At 2.5V_{OUT} 5m Ω to 20m Ω can improve transient response. At 5V_{OUT} the response is well damped with 0 Ω ESR.

Capacitor types with inherently higher ESR can be combined with 0m Ω ESR ceramic capacitors to achieve both good high frequency bypassing and fast settling time. Figure B8 illustrates the improvement in transient response that can be seen when a parallel combination of ceramic and

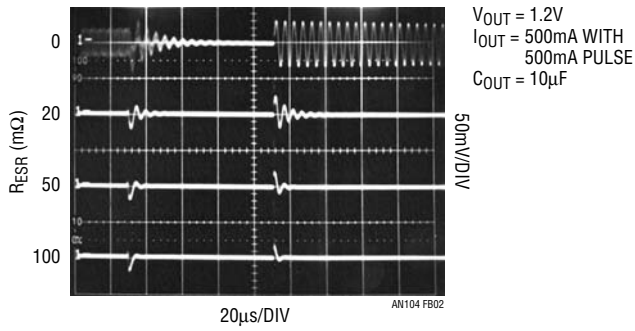


Figure B2

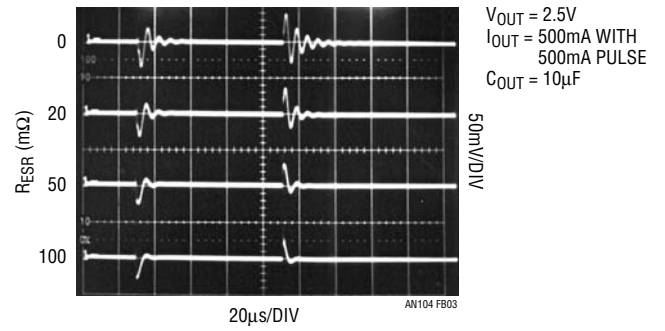


Figure B3

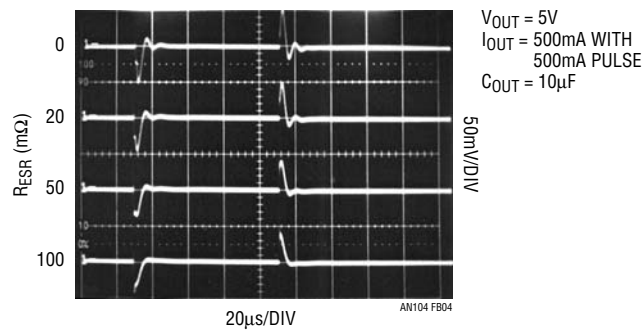


Figure B4

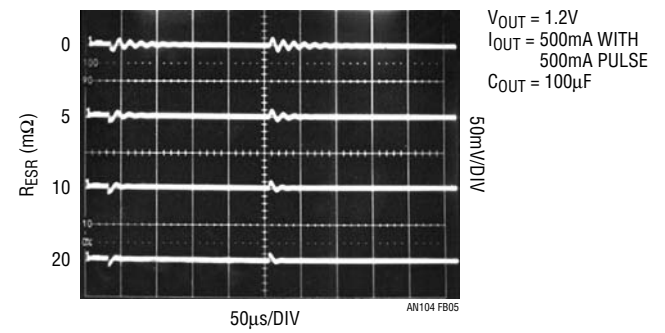


Figure B5

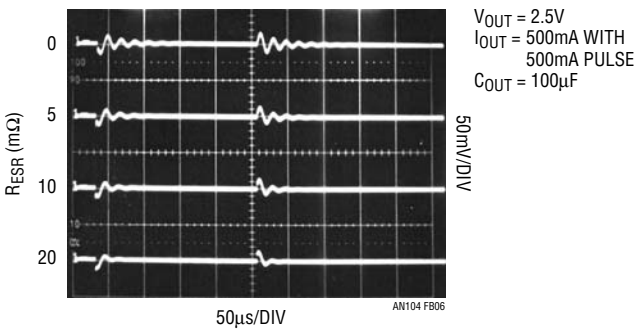


Figure B6

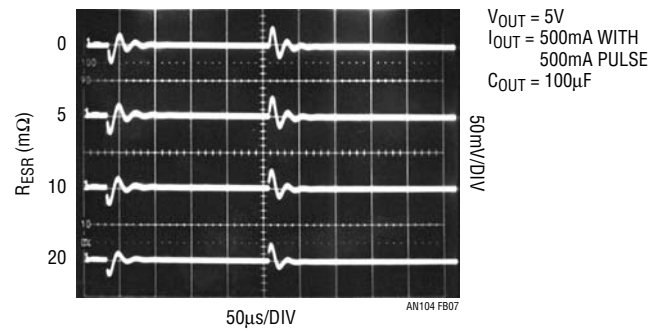


Figure B7

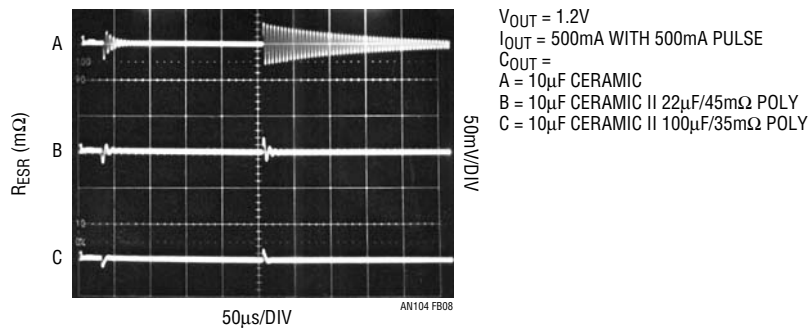


Figure B8

Application Note 104

POSCAP capacitors are used. The output voltage is at the worst case value of 1.2V. Trace A with a 10 μ F ceramic output capacitor, shows significant ringing with a peak amplitude of 25mV. For Trace B, a 22 μ F/45m Ω POSCAP is added in parallel with the 10 μ F ceramic. The output is well damped and settles to within 10mV in less than 20 μ s.

For Trace C, a 100 μ F/35m Ω POSCAP is connected in parallel with the 10 μ F ceramic capacitor. In this case the peak output deviation is less than 20mV and the output settles in about 10 μ s. For improved transient response the value of the bulk capacitor (tantalum or aluminum electrolytic) should be greater than twice the value of the ceramic capacitor.

Tantalum and Poly tantalum Capacitors

There is a variety of tantalum capacitor types available, with a wide range of ESR specifications. Older types have ESR specifications in the hundreds of m Ω to several Ohms. Some newer types of polytantalum with multi-electrodes have maximum ESR specifications as low as 5m Ω . In general the lower the ESR specification, the larger the size and the higher the price. Polytantalum capacitors have better surge capability than older types and generally lower ESR. Some types such as the Sanyo TPE and TPB series have ESR specifications in the 20m Ω to 50m Ω range, which provide near optimum transient response.

Aluminum Electrolytic Capacitors

Aluminum electrolytic capacitors can also be used with the LT1963A. These capacitors can also be used in conjunction with ceramic capacitors. These tend to be the cheapest and lowest performance type of capacitors. Care must be used in selecting these capacitors as some types can have ESR which can easily exceed the 3 Ω maximum value.

Ceramic Capacitors

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V

dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures B9 and B10. When used with a 5V regulator, a 10 μ F Y5V capacitor can exhibit an effective value as low as 1 μ F to 2 μ F over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

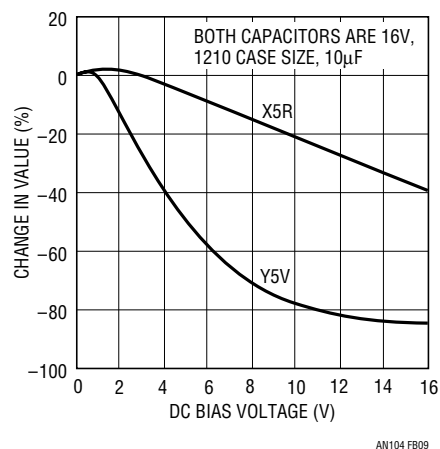


Figure B9. Ceramic Capacitor DC Bias Characteristics

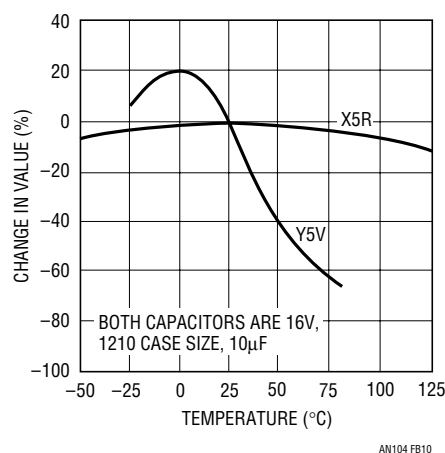


Figure B10. Ceramic Capacitor Temperature Characteristics

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

“FREE” Resistance with PC Traces

The resistance values shown in Figure B11 can easily be made using a small section of PC trace in series with the output capacitor. The wide range of non-critical ESR makes it easy to use PC trace. The trace width should be sized to handle the RMS ripple current associated with the load. The output capacitor only sources or sinks current for a few microseconds during fast output current transitions. There

is no DC current in the output capacitor. Worst case ripple current will occur if the output load is a high frequency (>100kHz) square wave with a high peak value and fast edges (<1μs). Measured RMS value for this case is 0.5 times the peak-to-peak current change. Slower edges or lower frequency will significantly reduce the RMS ripple current in the capacitor.

This resistor should be made using one of the inner layers of the PC board which are well defined. The resistivity is determined primarily by the sheet resistance of the copper laminate with no additional plating steps. Figure B11 gives some sizes for 0.75A RMS current for various copper thicknesses. More detailed information regarding resistors made from PC traces can be found in Application Note 69, Appendix A.

		10mΩ	20mΩ	30mΩ
0.5oz C _U	Width	0.011" (0.28mm)	0.011" (0.28mm)	0.011" (0.28mm)
	Length	0.102" (2.6mm)	0.204" (5.2mm)	0.307" (7.8mm)
1.0oz C _U	Width	0.006" (0.15mm)	0.006" (0.15mm)	0.006" (0.15mm)
	Length	0.110" (2.8mm)	0.220" (5.6mm)	0.330" (8.4mm)
2.0oz C _U	Width	0.006" (0.15mm)	0.006" (0.15mm)	0.006" (0.15mm)
	Length	0.224" (5.7mm)	0.450" (11.4mm)	0.670" (17mm)

Figure B11. PC Trace Resistors

APPENDIX C

Probing Considerations for Load Transient Response Measurements

Signals of interest in load transient response studies occur within a bandwidth of about 25MHz ($t_{RISE} = 14ns$) This is a modest speed range but probing technique requires some care for high fidelity measurement. Load current is measured with a DC stabilized (Hall Effect based) “clip on” current probe such as the Tektronix P-6042 or AM503. The conductor loop placed in the probe jaws should encompass the smallest possible area to minimize introduced parasitic inductance, which can degrade measurement. At higher speeds, grounding the probe case may slightly decrease measurement aberrations, but this is usually a small effect.

Voltage measurement, typically AC-coupled and in the 10mV to 250mV range, is best accomplished with Figure C1’s arrangement. The measured voltage is fed to a BNC fixtured 50Ω back terminated cable, which drives the oscilloscope via a DC blocking capacitor and a 50Ω termination.

The back termination is strict practice, enforcing a true 50Ω signal path. Practically, if its $\div 2$ attenuation presents problems, it can usually be eliminated with only minor signal degradation in the 25MHz measurement passband. The termination at the oscilloscope end is not negotiable. Figure C2 shows a typical observed load transient with no back termination but 50Ω at the oscilloscope. The presentation is clean and well defined. In C3, the cable’s 50Ω termination is removed, causing a distorted leading edge, ill-defined peaking and pronounced post-event ringing. Even at relatively modest frequencies the cable displays unterminated transmission line characteristics, resulting in signal distortion.

In theory, a 1x scope probe using a probe-tip coaxial connection could replace the above but such probes usually have bandwidth limitations of 10MHz to 20MHz. Conversely, a 10x probe is wideband, but oscilloscope vertical sensitivity must accommodate the introduced attenuation.

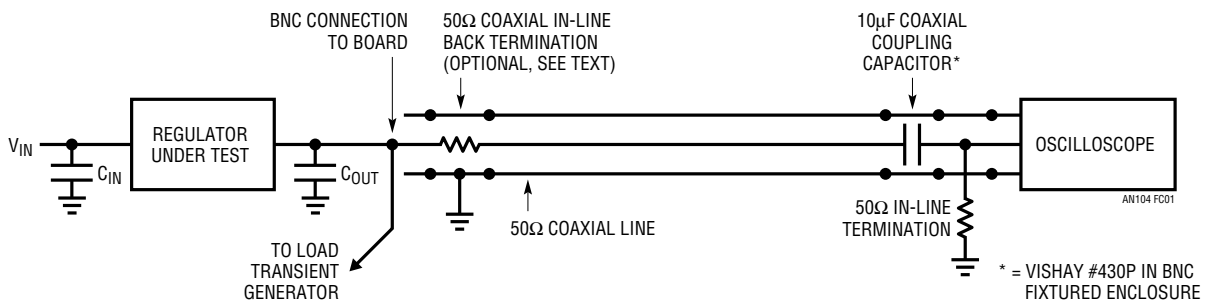


Figure C1. Coaxial Load Transient Voltage Measurement Path Promotes Observed Signal Fidelity. 50Ω Back Termination May Be Removed with Minimal Impact on 25MHz Signal Path Integrity. 50Ω Termination at Oscilloscope Cannot Be Deleted

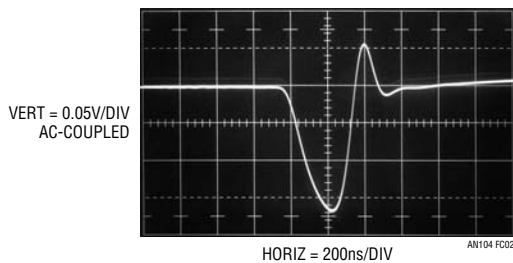


Figure C2. Typical High Speed Transient Observed Through Figure C1’s Measurement Path. Presentation is Clean and Well Defined

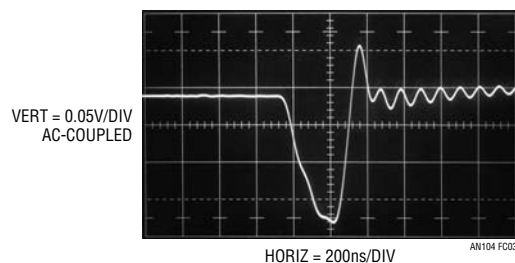
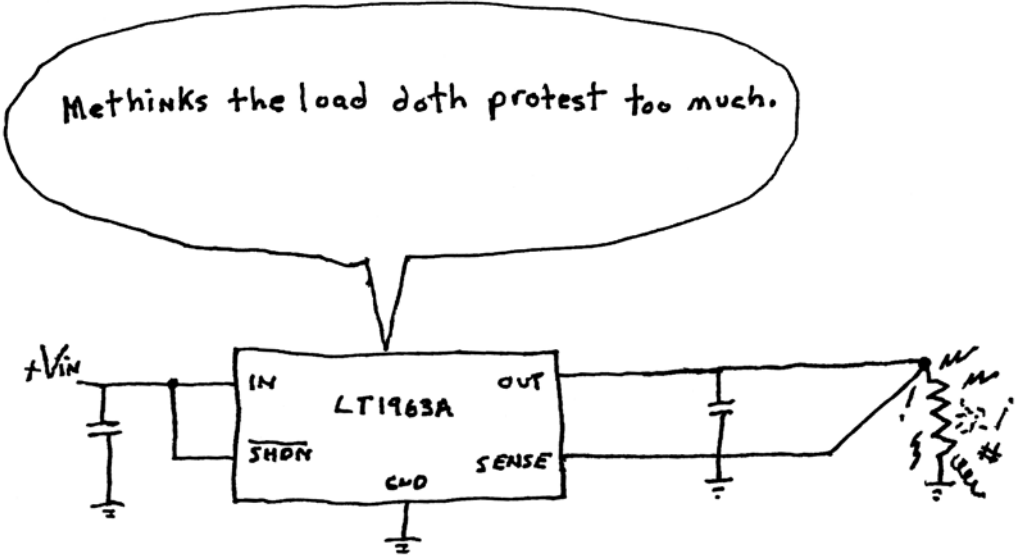


Figure C3. Figure C2’s Transient Measured with 50Ω Oscilloscope Termination Removed. Waveform Distortion and Post-Event Ringing Result

Application Note 104



— Willw₋₀₆ —

(with apologies to Wm. Shakespeare)

Instrumentation Circuitry Using RMS-to-DC Converters

RMS Converters Rectify Average Results

Jim Williams

INTRODUCTION

It is widely acknowledged that RMS (Root of the Mean of the Square) measurement of waveforms furnishes the most accurate amplitude information.¹ Rectify-and-average schemes, usually calibrated to a sine wave, are only accurate for one waveshape. Departures from this waveshape result in pronounced errors. Although accurate, RMS conversion often entails limited bandwidth, restricted range, complexity and difficult to characterize dynamic and static errors. Recent developments address these issues while simultaneously improving accuracy. Figure 1 shows the LTC®1966/LTC1967/LTC1968 device family. Low frequency accuracy, including linearity and gain error, is inside 0.5% with 1% error at bandwidths extending to 500kHz. These converters employ a sigma-delta based computational scheme to achieve their performance.²

Figure 2's pinout descriptions and basic circuits reveal an easily applied device. An output filter capacitor is all that is required to form a functional RMS-to-DC converter. Split and single supply powered variants are shown. Such ease of implementation invites a broad range of application; examples begin with Figure 3.

Isolated Power Line Monitor

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 3's AC power line monitor has 0.5% accuracy over a sensed 90VAC to 130VAC input and provides a safe, fully isolated output. RMS conversion provides accurate reporting of AC line voltage regardless of waveform distortion, which is common.

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¹See Appendix A, "RMS-to-DC Conversion" for complete discussion of RMS measurement.

²Appendix A details sigma-delta based RMS-to-DC converter operation.

PART NUMBER	LINEARITY ERROR TYP/MAX (%)	CONVERSION GAIN ERROR TYP/MAX (%)	1% ERROR BANDWIDTH (kHz)	3dB ERROR BANDWIDTH (kHz)	SUPPLY VOLTAGE		I _{SUPPLY} MAX (μA)
					MIN(V)	MAX(V)	
LTC1966	0.02/0.15	0.1/0.3	6	800	2.7	±5	170
LTC1967	0.02/0.15	0.1/0.3	200	4MHz	4.5	5.5	390
LTC1968	0.02/0.15	0.1/0.3	500	15MHz	4.5	5.5	2.3mA

Figure 1. Primary Differences in RMS to DC Converter Family are Bandwidth and Supply Requirements. All Devices Have Rail-to-Rail Differential Inputs and Output

Application Note 106

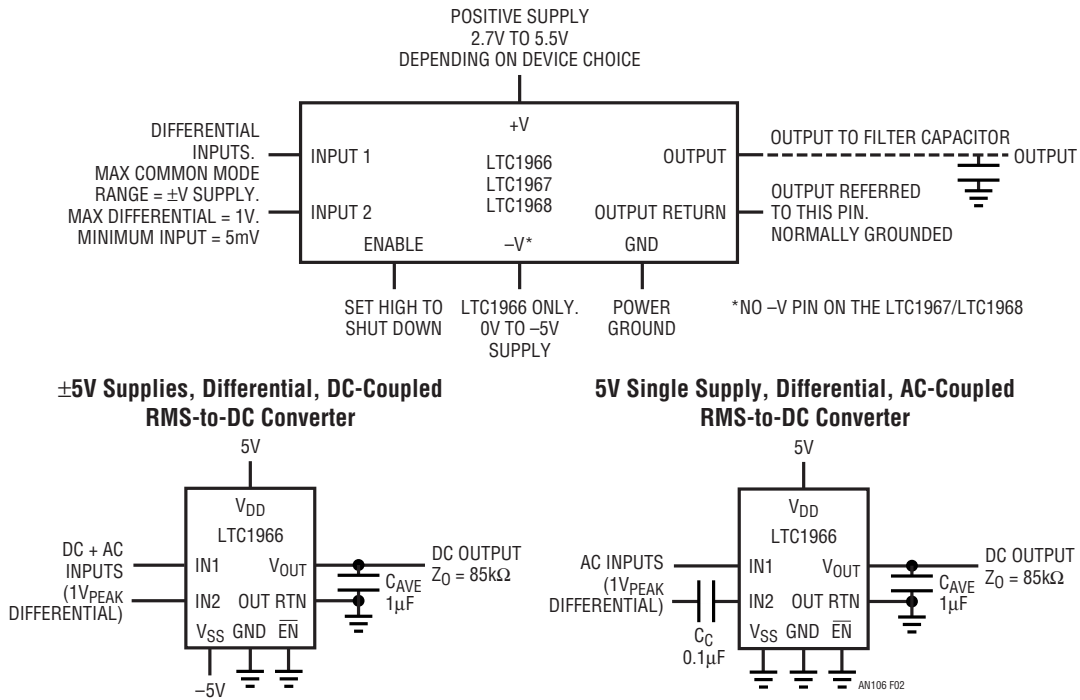


Figure 2. RMS Converter Pin Functions (Top) and Basic Circuits (Bottom). Pin Descriptions are Common to All Devices, with Minor Differences

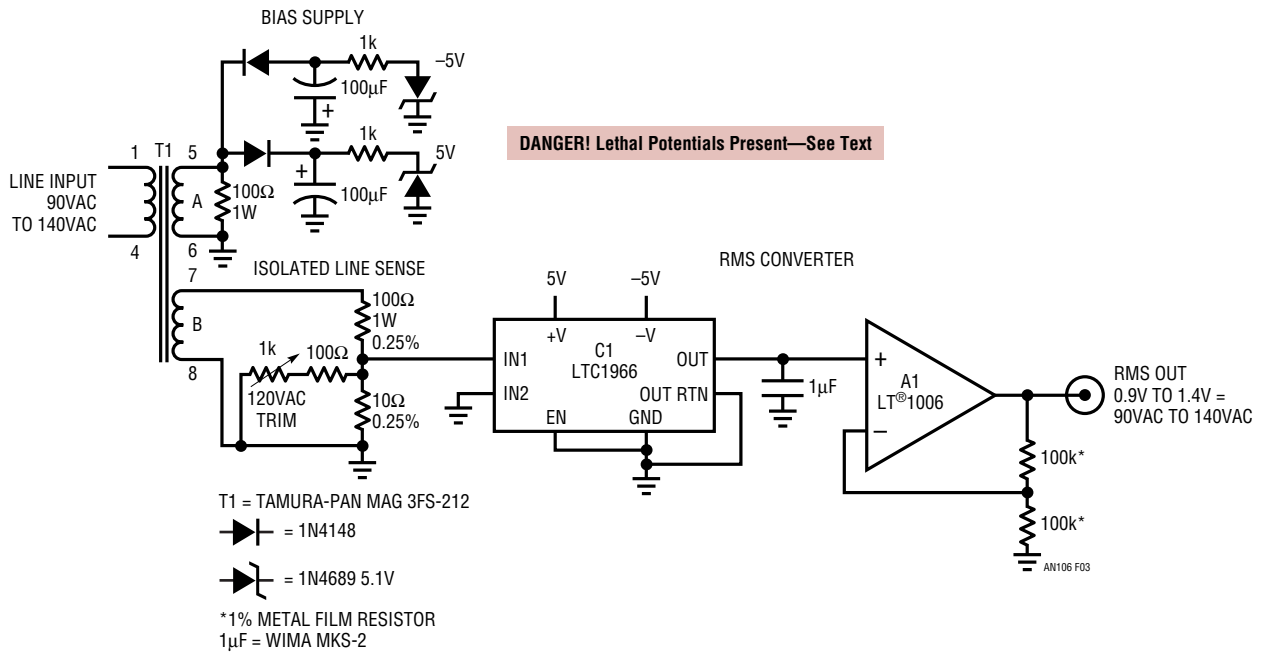


Figure 3. Isolated Power Line Monitor Senses Via Transformer with 0.5% Accuracy Over 90VAC to 130VAC Input. Secondary Loading Optimizes Transformer Voltage Conversion Linearity

The AC line voltage is divided down by T1's ratio. An isolated and reduced potential appears across T1's secondary B, where it is resistively scaled and presented to C1's input. Power for C1 comes from T1's secondary A, which is rectified, filtered and zener regulated to DC. A1 takes gain and provides a numerically convenient output. Accuracy is increased by biasing T1 to an optimal loading point, facilitated by the relatively low resistance divider values. Similarly, although C1 and A1 are capable of single supply operation, split supplies maintain symmetrical T1 loading. The circuit is calibrated by adjusting the 1k trim for 1.20V output with the AC line set at 120VAC. This adjustment is made using a variable AC line transformer and a well floated (use a line isolation transformer) RMS voltmeter.³

Figure 4's error plot shows 0.5% accuracy from 90VAC to 130VAC, degrading to 1.4% at 140VAC. The beneficial effect of trimming at 120VAC is clearly evident; trimming at full scale would result in larger overall error, primarily due to non-ideal transformer behavior. Note that the data is specific to the transformer specified. Substitution for T1 necessitates circuit value changes and recharacterization.

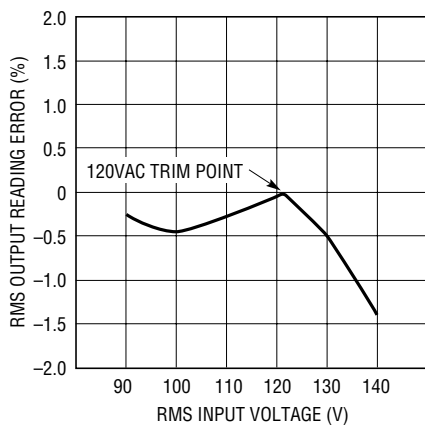


Figure 4. Error Plot for Isolated Line Monitor Shows 0.5% Accuracy from 90VAC to 130VAC, Degrading to 1.4% at 140VAC. Transformer Parasitics Account for Almost All Error

Fully Isolated 2500V Breakdown, Wideband RMS-to-DC Converter

NOTE: BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Accurate RMS amplitude measurement of SCR chopped AC line related waveforms is a common requirement. This measurement is complicated by the SCR's fast switching of a sine wave, introducing odd waveshapes with high frequency harmonic content. Figure 5's conceptual SCR-based AC/DC converter is typical. The SCRs alternately chop the 220VAC line, responding to a loop enforced, phase modulated trigger to maintain a DC output. Figure 6's waveforms are representative of operation. Trace A is one AC line phase, trace B the SCR cathodes. The SCR's irregularly shaped waveform contains DC and high frequency harmonic, requiring wideband RMS conversion for measurement. Additionally, for safety and system interface considerations, the measurement must be fully isolated.

³See Appendix B, "AC Measurement and Signal Handling Practice," for recommendations on RMS voltmeters and other AC measurement related gossip.

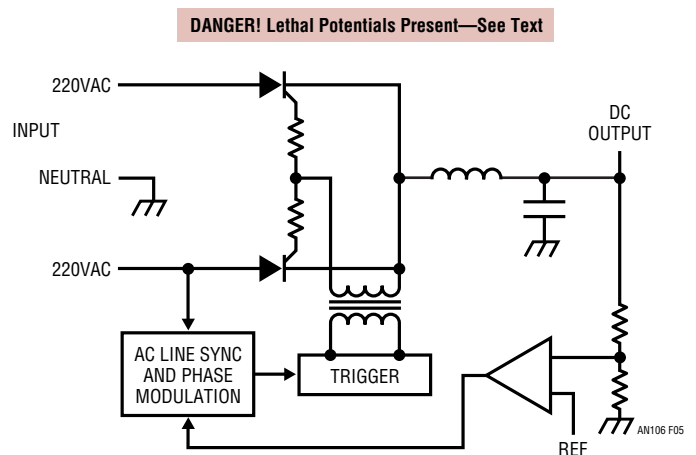


Figure 5. Conceptual AC/DC Converter is Typical of SCR-Based Configurations. Feedback Directed, AC Line Synchronized Trigger Phase Modulates SCR Turn-On, Controlling DC Output

Application Note 106

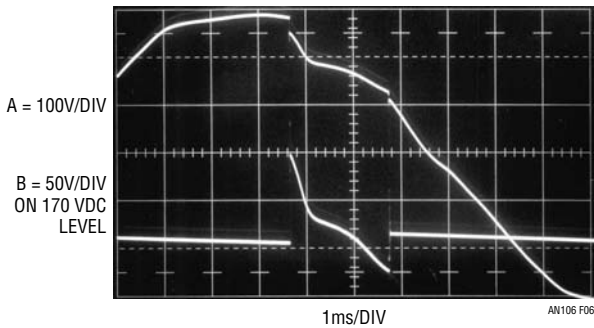


Figure 6. Typical SCR-Based Converter Waveforms Taken at AC Line (Trace A) and SCR Cathodes (Trace B). SCR's Irregularly Shaped Waveform Contains DC and High Frequency Harmonic, Requiring Wideband RMS Converter for Measurement

Figure 7 provides isolated power and data output paths to an RMS-to-DC converter, permitting safe, wideband, digital output RMS measurement. A pulse generator configured comparator combines with Q1 and Q2 to drive T1, resulting in isolated 5V power at T1's rectified, filtered and zener regulated output. The RMS-to-DC converter senses either 135VAC or 270VAC full-scale inputs via a resistive divider. The converter's DC output feeds a self-clocked, serially interfaced A/D converter; optocouplers convey output data across the isolation barrier. The LTC6650 provides a 1V reference to the A/D and biases the RMS-to-DC converter's inputs to accommodate the voltage divider's AC swing. Calibration is accomplished by adjusting the 20k trim while noting output data agreement with the input AC voltage. Circuit accuracy is within 1% in a 200kHz bandwidth.

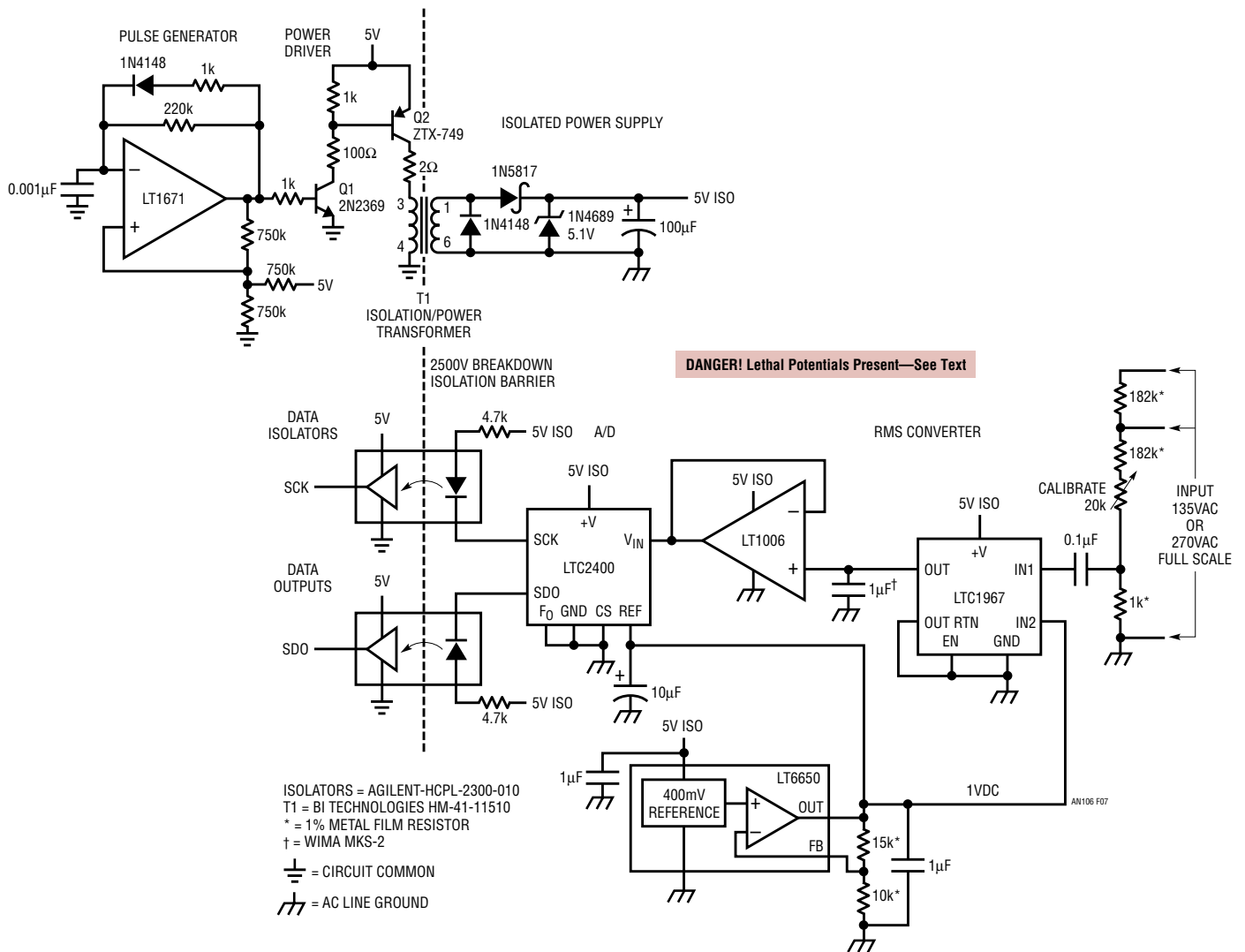


Figure 7. Isolated RMS Converter Permits Safe, Digital Output, Wideband RMS Measurement. T1-Based Circuitry Supplies Isolated Power. RMS-to-DC Converter Senses High Voltage Input via Resistive Divider. A/D Converter Provides Digital Output Through Optoisolators. Accuracy is 1% in 200kHz Bandwidth

an106f

Low Distortion AC Line RMS Voltage Regulator

NOTE: BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Almost all AC line voltage regulators rely on some form of waveform chopping, clipping or interruption to function. This is efficient, but introduces waveform distortion, which is unacceptable in some applications. Figure 8 regulates the AC line's RMS value within 0.25% over wide input swings and does not introduce distortion. It does this by continuously controlling the conductivity of a series pass MOSFET in the AC lines path. Enclosing the MOSFET in a diode bridge permits it to operate during both AC line polarities.

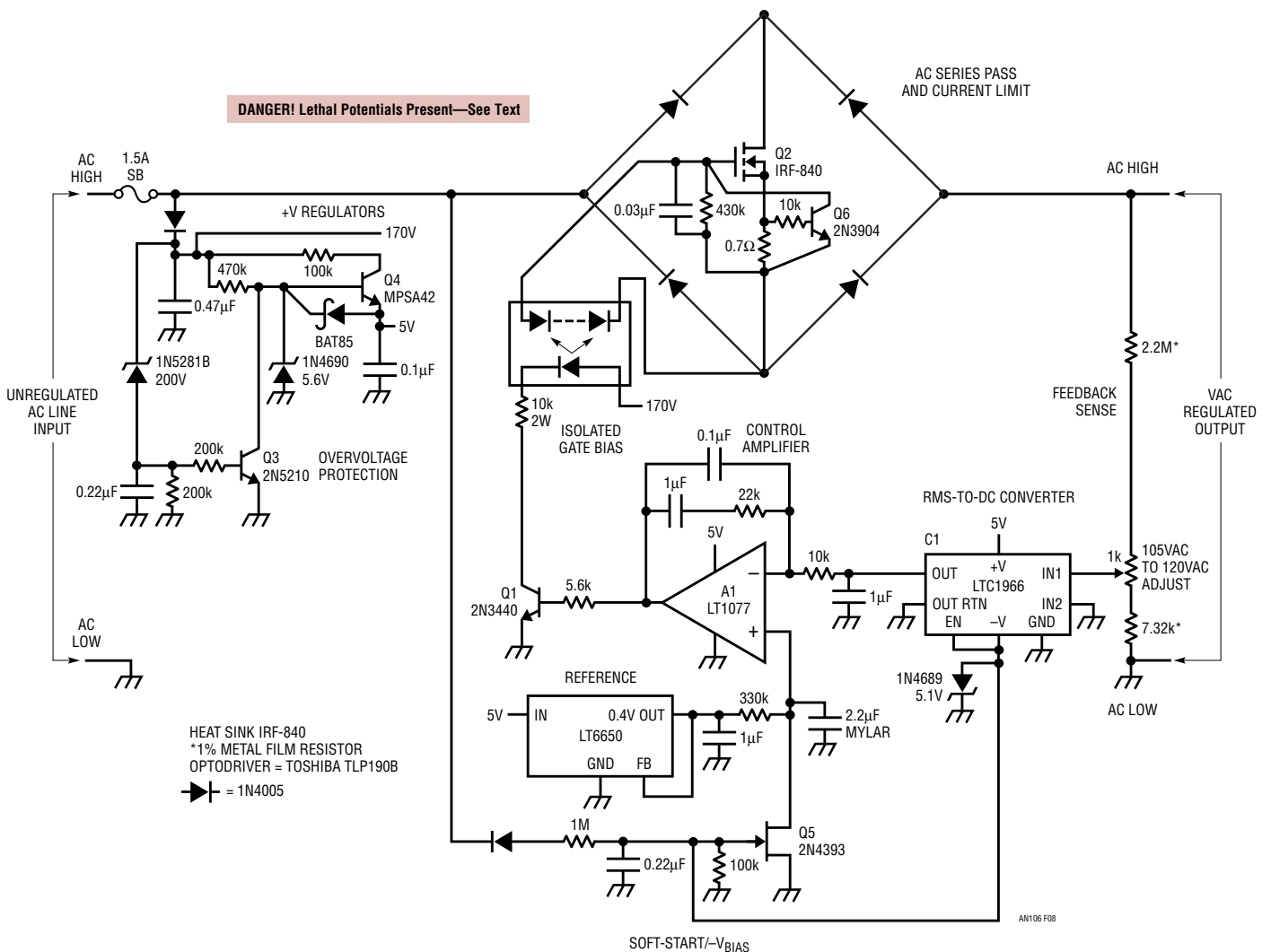


Figure 8. Adjustable AC Line Voltage Regulator Introduces No Waveform Distortion. Line Voltage RMS Value is Sensed and Compared to a Reference by A1. A1 Biases Photovoltaic Optocoupler via Q1, Setting Q2-Diode Bridge Conductivity and Closing a Control Loop. V_{IN} Must be $\geq 2V$ Above V_{OUT} to Maintain Regulation

Application Note 106

The AC line voltage is applied to the Q2-diode bridge. The Q2-diode bridge output is sensed by a calibrated variable voltage divider which feeds C1. C1's output, representing the regulated lines RMS value, is routed to control amplifier A1 and compared to a reference. A1's output biases Q1, controlling drive to a photovoltaic optoisolator. The optoisolator's output voltage provides level-shifted bias to diode bridge enclosed Q2, closing a control loop which regulates the output's RMS voltage against AC line and load shifts. RC components in A1's local feedback path stabilize the control loop. The loop operates Q2 in its linear region, much like a common low voltage DC linear regulator. The result is absence of introduced distortion at the expense of lost power. Available output power is constrained by heat dissipation. For example, with the output adjustment set to regulate 10V below the normal input, Q2 dissipates about 10W at 100W output. This figure can be improved upon. The circuit regulates for $V_{IN} \geq 2V$ above V_{OUT} , but operation in this region risks regulation dropout as V_{IN} varies.

Circuit details include JFET Q5 and associated components. The passive components associated with Q5's gate form a slow turn-on negative supply for C1. They also provide gate bias for Q5. Q5, a soft-start, prevents abrupt AC power application to the output at start-up. When power is off, Q5 conducts, holding A1's "+" input low. When power is applied, A1 initially has a zero volt reference, causing the control loop to set the output at zero. As the 1M Ω 0.22 μ F combination charges, Q5's gate moves negative, causing its channel conductivity to gradually decay. Q5 ramps off, A1's positive input moves smoothly towards the LT6650's 400mV reference, and the AC output similarly ascends towards its regulation point. Current sensor Q6, measuring across the 0.7 Ω shunt, limits output current to about 1A. At normal line inputs (90VAC to 135VAC) Q4 supplies 5V operating bias to the circuit. If line voltage rises beyond this point, Q3 comes on, turning off Q4 and shutting down the circuit.

X1000 DC Stabilized Millivolt Preamplifier

The preceding circuits furnish high level inputs to the RMS converter. Many applications lack this advantage and some form of preamplifier is required. High gain pre-amplification for the RMS converter requires more attention than might be supposed. The preamplifier must have low offset error because the RMS converter (desirably) processes DC as

legitimate input. More subtly, the preamplifier must have far more bandwidth than is immediately apparent. The amplifiers -3db bandwidth is of interest, but its closed loop 1% amplitude error bandwidth must be high enough to maintain accuracy over the RMS converter's 1% error passband. This is not trivial, as very high open-loop gain at the maximum frequency of interest is required to avoid inaccurate closed-loop gain.

Figure 9 shows an x1000 preamplifier which preserves the LTC1966's DC-6kHz 1% accuracy. The amplifier may be either AC or DC coupled to the RMS converter. The 1mV full-scale input is split into high and low frequency paths. AC coupled A1 and A2 take a cascaded, high frequency gain of 1000. DC coupled, chopper stabilized A3 also has X1000 gain, but is restricted to DC and low frequency by its RC input filter. Assuming the switch is set to "DC + AC," high and low frequency path information recombine at the RMS converter. The high frequency paths 650kHz -3db response combines with the low frequency sections microvolt level offset to preserve the RMS converters DC-6kHz 1% error. If only AC response is desired, the switch is set to the appropriate position. The minimum processable input, set by the circuits noise floor, is 15 μ V.

Wideband Decade Ranged X1000 Preamplifier

The LTC1968, with a 500kHz, 1% error bandwidth, poses a significant challenge for an accurate preamplifier, but Figure 10 meets the requirement. This design features decade ranged gain to X1000 with a 1% error bandwidth beyond 500kHz, preserving the RMS converters 1% error bandwidth. Its 20 μ V noise floor maintains wideband performance at microvolt level inputs.

Q1A and Q1B form a low noise buffer, permitting high impedance inputs. A1 and A2, both gain switchable, take cascaded gain in accordance with the figure's table. The gains are settable via reed relays controlled by a 2-bit code. A2's output feeds the RMS converter and the converter's output is smoothed by a Sallen-Keys active filter. The circuit maintains 1% error over a 10Hz to 500kHz bandwidth at all gains due to the preamplifiers -3db, 10MHz bandwidth. The 10Hz low frequency restriction could be eliminated with a DC stabilization path similar to Figure 9's but its gain would have to be switched in concert with the A1-A2 path.

an106f

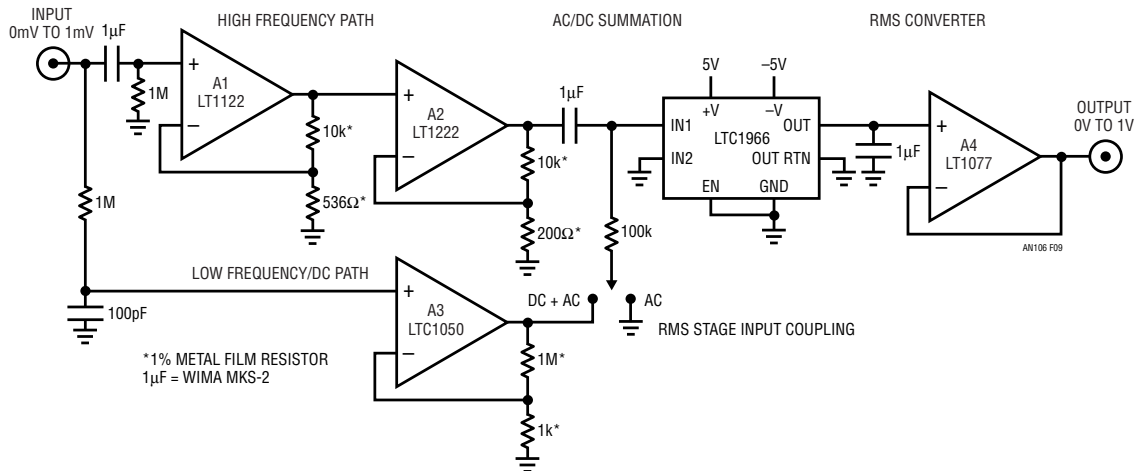


Figure 9. X1000 Preamplifier Allows 1mV Full-Scale Sensitivity RMS-to-DC Conversion. Input Splits Into High and Low Frequency Amplifier Paths, Recombining at RMS Converter. Amplifier's -3dB, 650kHz Bandwidth Preserves RMS-to-DC Converter's 6kHz, 1% Error Bandwidth. Noise Floor is 15µV

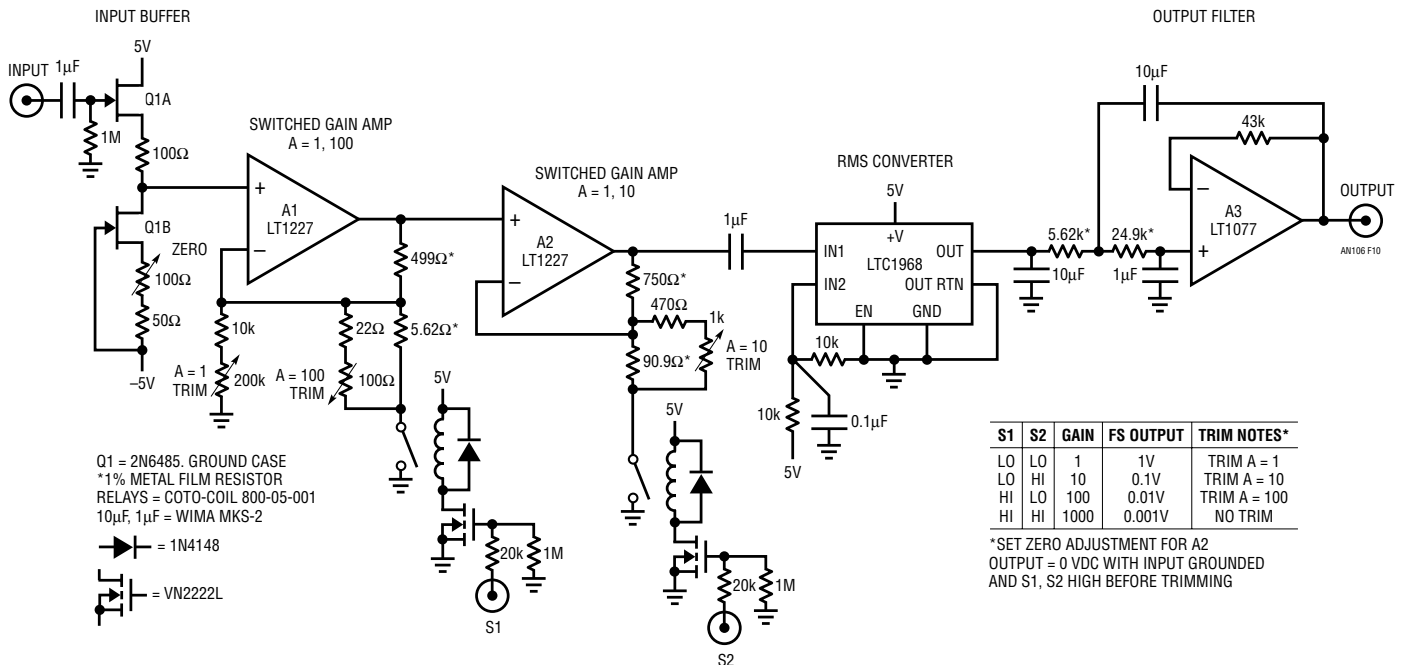


Figure 10. Switched Gain 10MHz (-3dB) Preamplifier Preserves LTC1968's 500kHz, 1% Error Bandwidth. Decade Ranged Gains (See Table) Allow 1mV Full Scale with 20µV Noise Floor. JFET Input Stage Presents High Input Impedance. AC Coupling, 3rd Order Sallen-Key Filter Maintains 1% Accuracy Down to 10Hz

Application Note 106

Figure 11 shows preamplifier response to a 1mV input step at a gain of X1000. A2's output is singularly clean, with trace thickening in the pulse flat portions due to the 20 μ V noise floor. The 35ns risetime indicates a 10MHz bandwidth.

To calibrate this circuit first set S1 and S2 high, ground the input and trim the "zero" adjustment for zero VDC at A2's output. Next, set S1 and S2 low, apply a 1V, 100kHz input, and trim "A = 1" for unity gain, measured at the

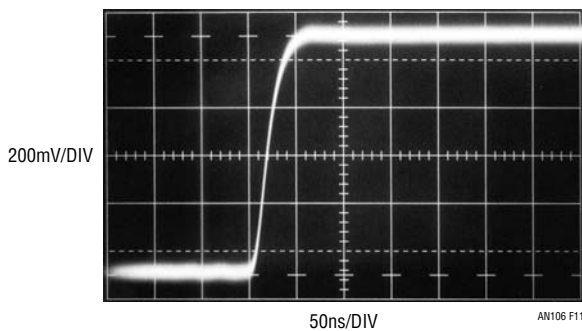


Figure 11. Figure 10's A2 Output Responds to a 1mV Input Step at X1000 Gain. 35ns Risetime Indicates 10MHz Bandwidth. Trace Thickening in Pulse Flat Portions Represents Noise Floor

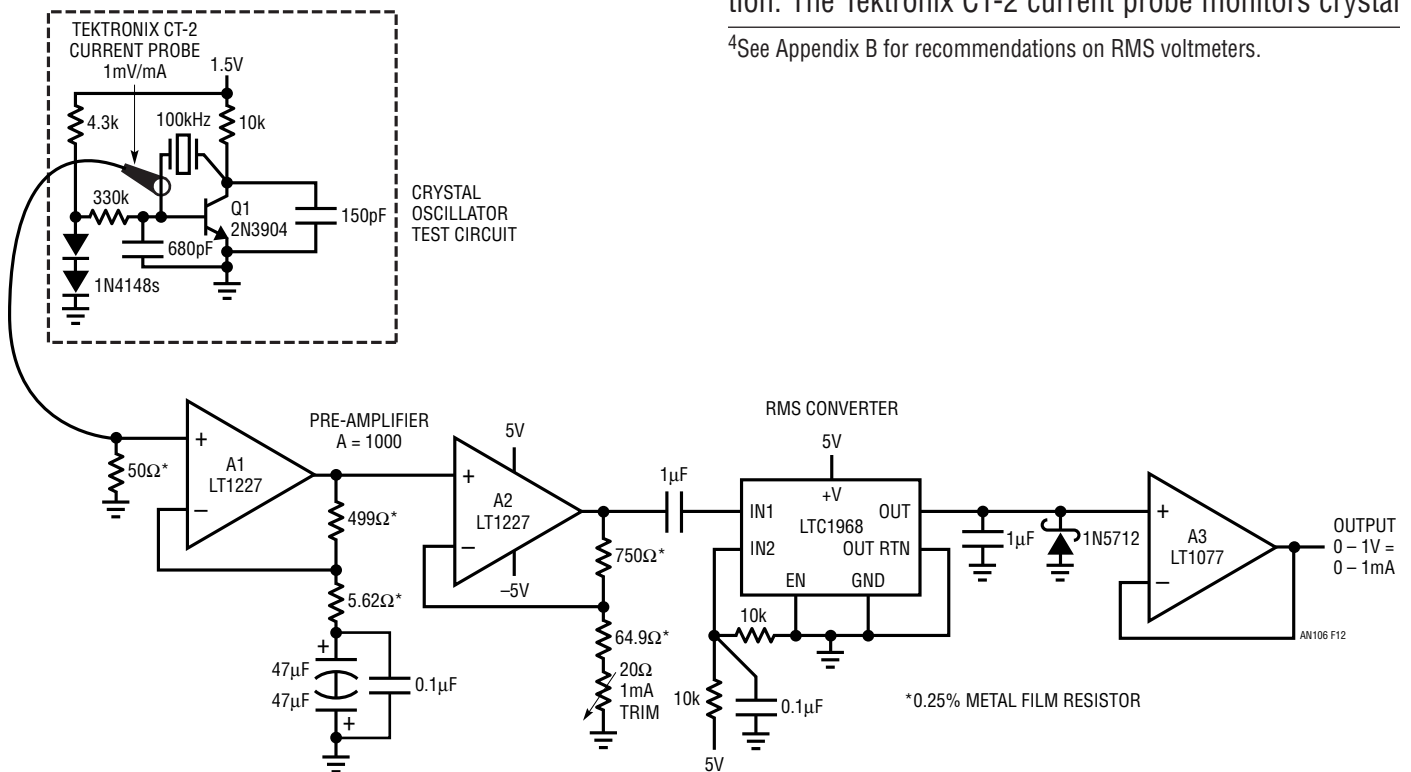


Figure 12. Figure 10's Wideband Amplifier Adapted for Isolated RMS Current Measurement of Quartz Crystal Current. FET Input Buffer is Deleted; Current Probe's 50 Ω Impedance Allows Direct Connection to A1. Current Probe Provides Minimal Crystal Loading in Oscillator Test Circuit

circuit output, in accordance with the table in the figure. Continue this procedure for the remaining three gains given in the table. A good way to generate the accurate low level inputs required is to set a 1.00VAC level and divide it down with a high grade 50 Ω attenuator such as the Hewlett Packard 350D or the Tektronix 2701. It is prudent to verify the attenuator's output with a precision RMS voltmeter.⁴

Wideband, Isolated, Quartz Crystal RMS Current Measurement

Quartz crystal RMS operating current is critical to long-term stability, temperature coefficient and reliability. Accurate determination of RMS crystal current, especially in low power types, is complicated by the necessity to minimize introduced parasitics, particularly capacitance, which corrupt crystal operation. Figure 12, a form of Figure 10's wideband amplifier, combines with a commercially available closed core current probe to permit the measurement. An RMS-to-DC converter supplies the RMS value. The quartz crystal test circuit shown in dashed lines exemplifies a typical measurement situation. The Tektronix CT-2 current probe monitors crystal

⁴See Appendix B for recommendations on RMS voltmeters.

current while introducing minimal parasitic loading (see Figure 14). The probe's 50Ω termination allows direct connection to A1—Figure 10's FET buffer is deleted. Additionally, because quartz crystals are not common below 4kHz, A1's gain does not extend to low frequency.

Figure 13 shows results. Crystal drive, taken at Q1's collector (trace A), causes a 25μA RMS crystal current which is represented at the RMS-to-DC converter input (trace B). The trace enlargement is due to the preamplifier's 5μA RMS equivalent noise contribution.

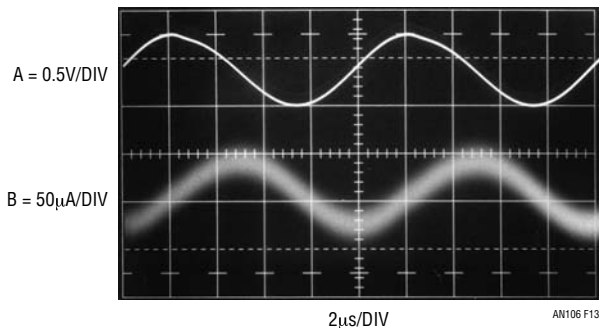


Figure 13. Crystal Voltage (Trace A) and Current (Trace B) for Figure 12's Test Circuit. 25μA RMS Crystal Current Measurement Includes Preamplifier 5μA RMS Noise Floor Contribution

PARAMETER	CT-1	CT-2
Sensitivity	5mV/mA	1mV/mA
Accuracy	3%	3%
Low Frequency Additional 1% Error BW*	98kHz	6.4kHz
-3dB Bandwidth	25kHz to 1GHz	1.2kHz to 200MHz
Noise Floor with Amplifier Shown*	1μA RMS	5μA RMS
Capacitive Loading	1.5pF	1.8pF
Insertion Impedance at 10MHz	1Ω	0.1Ω

*As measured. Not vendor specified

Figure 14. Relevant Specifications of Two Tektronix Current Probes. Primary Trade-Off is Low Frequency Error and Sensitivity. Noise Floor is Due to Amplifier Limitations

Figure 14 details characteristics of two Tektronix closed core current probes. The primary trade-off is low frequency error versus sensitivity. There is essentially no probe noise contribution and capacitive loading is notably low. Circuit calibration is achieved by putting 1mA RMS current through the probe and adjusting the indicated trim for a 1V circuit output. To generate the 1mA, drive a 1k, 0.1% resistor with 1V_{RMS}.⁵

AC Voltage Standard with Stable Frequency and Low Distortion

Figure 15 utilizes the RMS-to-DC converter's stability in an AC voltage standard. Initial circuit accuracy is 0.1% and long-term (6 months at 20°C to 30°C) drift remains within that figure. Additionally, the 4kHz operating frequency is within 0.01% and distortion inside 30ppm.

A1 and its power buffer A3 sense across a bridge composed of a 4kHz quartz crystal and an RC impedance in one arm; resistors and an LED driven photocell comprise the other arm. A1 sees positive feedback at the crystals 4kHz resonance, promoting oscillation. Negative feedback, stabilizing oscillation amplitude, occurs via a control path which includes an RMS-to-DC converter and amplitude control amplifier, A5. A5 acts on the difference between A3's RMS converted output and the LT1009 voltage reference. Its output controls the LED driven photocell to set A1's negative feedback. RC components in A5's feedback path stabilize the control loop. The 50k trim sets the optically driven resistor's value to the point where lowest A3 output distortion occurs while maintaining adequate loop stability.

Normally the bridge's "bottom" would be grounded. While this connection will work, it subjects A1 to common mode swings, increasing distortion due to A1's finite common mode rejection versus frequency. A2 eliminates this concern by forcing the bridges mid-points, and hence common mode voltage, to zero while not influencing desired circuit operation. It does this by driving the bridge "bottom" to force its input differential to zero. A2's output swing is 180° out of phase with A3's circuit output. This action eliminates common mode swing at A1, reducing circuit output distortion by more than an order of magnitude. Figure 16 shows the circuits 1.414V_{RMS} (2.000V_{PEAK}) output in trace A while trace B's distortion constituents include noise, fundamental related residue and 2F components.

The 4kHz crystal is a relatively large structure with very high Q factor. Normally, it would require more than 30 seconds to start and arrive at full regulated amplitude. This is avoided by inclusion of the Q1-LTC201 switch circuitry. At start-up A5's output goes high, biasing Q1. Q1's collector goes low, turning on the LTC201. This sets A1's gain abnormally high, increasing bridge drive and

⁵This measurement technique has been extended to monitor 32.768kHz "watch crystal" sub-microampere operating currents. Contact the author for details.

Application Note 106

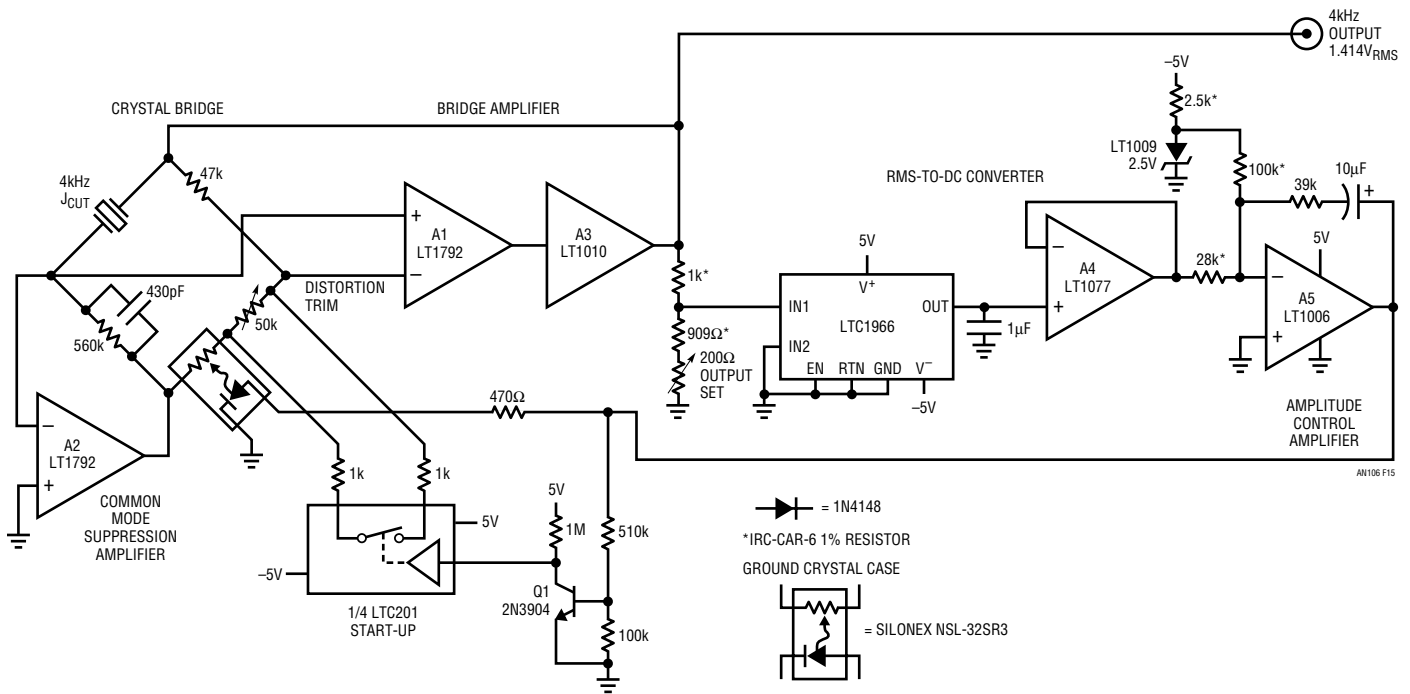


Figure 15. Quartz Stabilized Sine Wave Output AC Reference Has 0.1% Long-Term Amplitude Stability. Frequency Accuracy is 0.01% with <30ppm Distortion. Positive Feedback Around A1 Causes Oscillation at Crystal’s Resonance. A5, Acting on A3’s RMS Amplitude, Supplies Negative Feedback to A1 via Bridge Network, Stabilizing RMS Output Amplitude. Optocoupler Minimizes Feedback Induced Distortion. Q1 Closes Switch During Start-Up, Ensuring Rapid Oscillation Build-Up

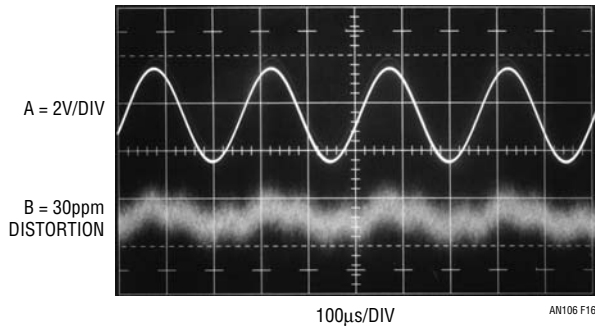


Figure 16. A3’s 1.414V_{RMS} (2.000V_{PEAK}), 4kHz Reference Output (Trace A) Shows 30ppm Distortion in Trace B. Distortion Constituents Include Noise, Fundamental Related Residue and 2F Components

accelerating crystal start-up. When the bridge arrives at its operating point A5’s output drops to a lower value, Q1 and the LTC201 switch go off, and the circuit transitions into normal operation. Start-up time is several seconds.

The circuit requires trimming for amplitude accuracy and lowest distortion. The distortion trim is made first. Adjust

the trim for minimal output distortion as measured on a distortion analyzer. Note that the absolute lowest level of distortion coincides with the point where control loop gain is just adequate to maintain oscillation. As such, find this point and retreat from it into the control loop’s active region. This necessitates giving up about 5ppm distortion, but 30ppm is achievable with good control loop stability. Output amplitude is trimmed with the indicated adjustment for exactly 1.414V_{RMS} (2.000V_{PEAK}) at the circuit output.

RMS Leveled Output Random Noise Generator

Figure 17 uses the RMS-to-DC converter in a leveled output random noise generator. Noise diode D1 AC biases A1, operating at a gain of 2.⁶ A1’s output feeds a 1kHz to 500kHz switch selectable lowpass filter. The filter output biases the variable gain amplifier, A2-A3, contained

⁶See Appendix C “Symmetrical White Gaussian Noise,” guest written by Ben Hessen-Schmidt of Noise Com, Inc. for tutorial on noise and noise diodes.

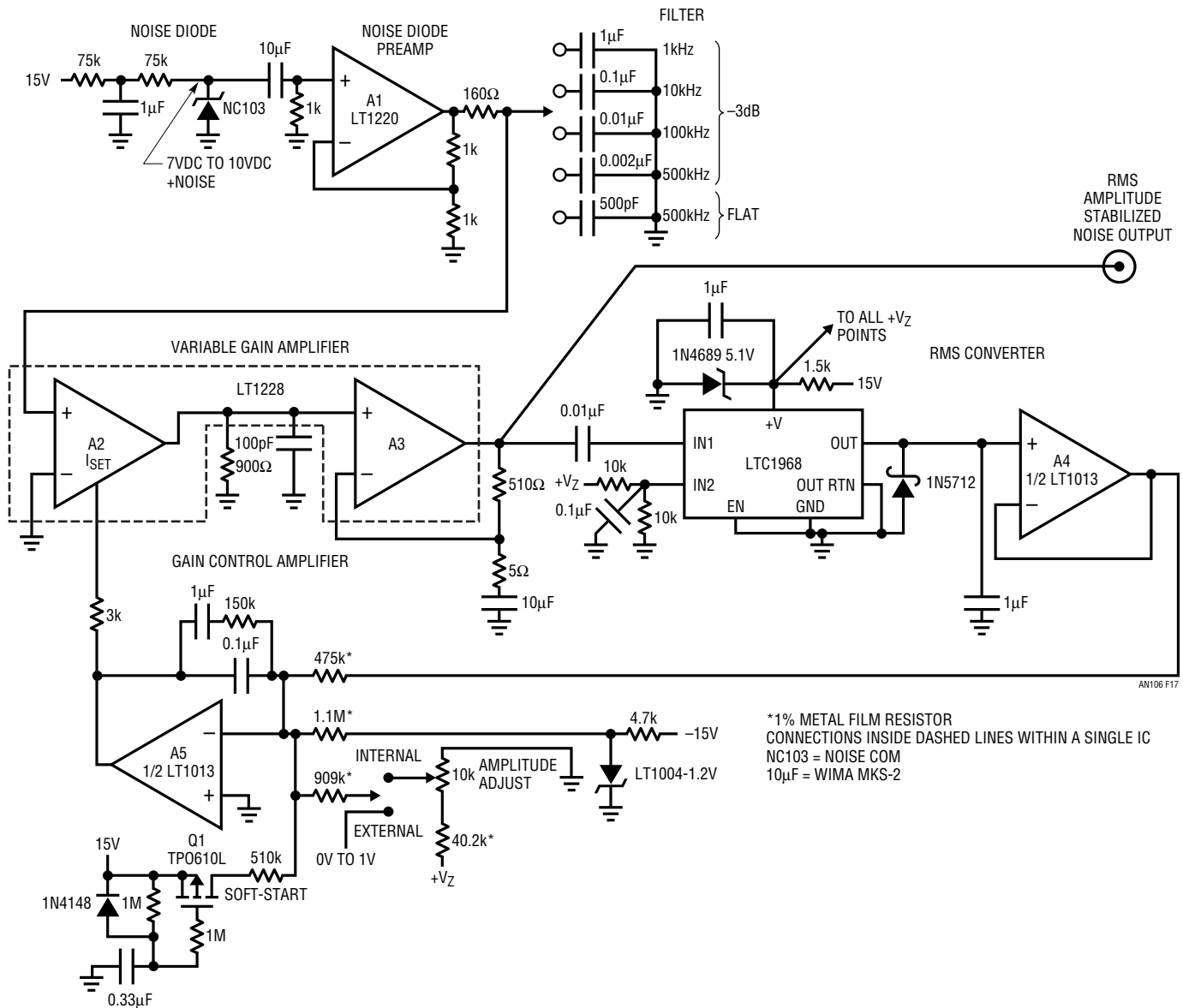


Figure 17. An RMS Levelled Output Random Noise Generator. Amplified (A1) Diode Noise Is Filtered, Variable Gain Amplified (A2-A3) and RMS Converted. Converter Output Feeds Back to A5 Gain Control Amplifier, Closing RMS Stabilized Loop. Output Amplitude, Taken at A3, is Settable

on one chip, include a current controlled transconductance amplifier (A2) and an output amplifier (A3). This stage takes AC gain, biases the LTC1968 RMS-to-DC converter and is the circuit's output. The RMS converter output at A4, feeds back to gain control amplifier A5, which compares the RMS value to a variable portion of the 5.1V zener potential. A5's output sets A2's gain via the 3k resistor, completing a control loop to stabilize noise RMS output amplitude. The RC components in A5's local feedback path

stabilize this loop. Output amplitude is variable by the 10k potentiometer; a switch permits external voltage control. Q1 and associated components, a soft-start circuit, prevent output overshoot at power turn-on.

Figure 18 shows circuit output noise in the 10kHz filter position; Figure 19's spectral plot reveals essentially flat RMS noise amplitude over a 500kHz bandwidth.

Application Note 106

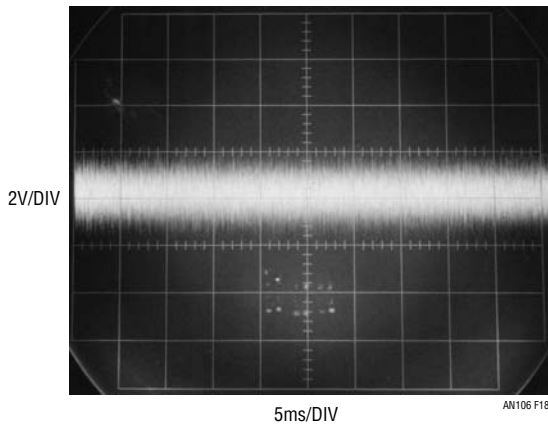


Figure 18. Figure 17's Output in the 10kHz Filter Position

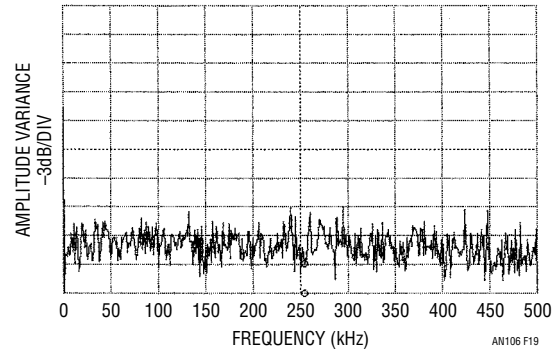


Figure 19. Amplitude vs Frequency for the Random Noise Generator is Essentially Flat to 500kHz. NC103 Diode Contributes Even Noise Spectrum Distribution; RMS Converter and Loop Stabilize Amplitude. Sweep Time is 2.8 Minutes, Resolution Bandwidth, 100Hz

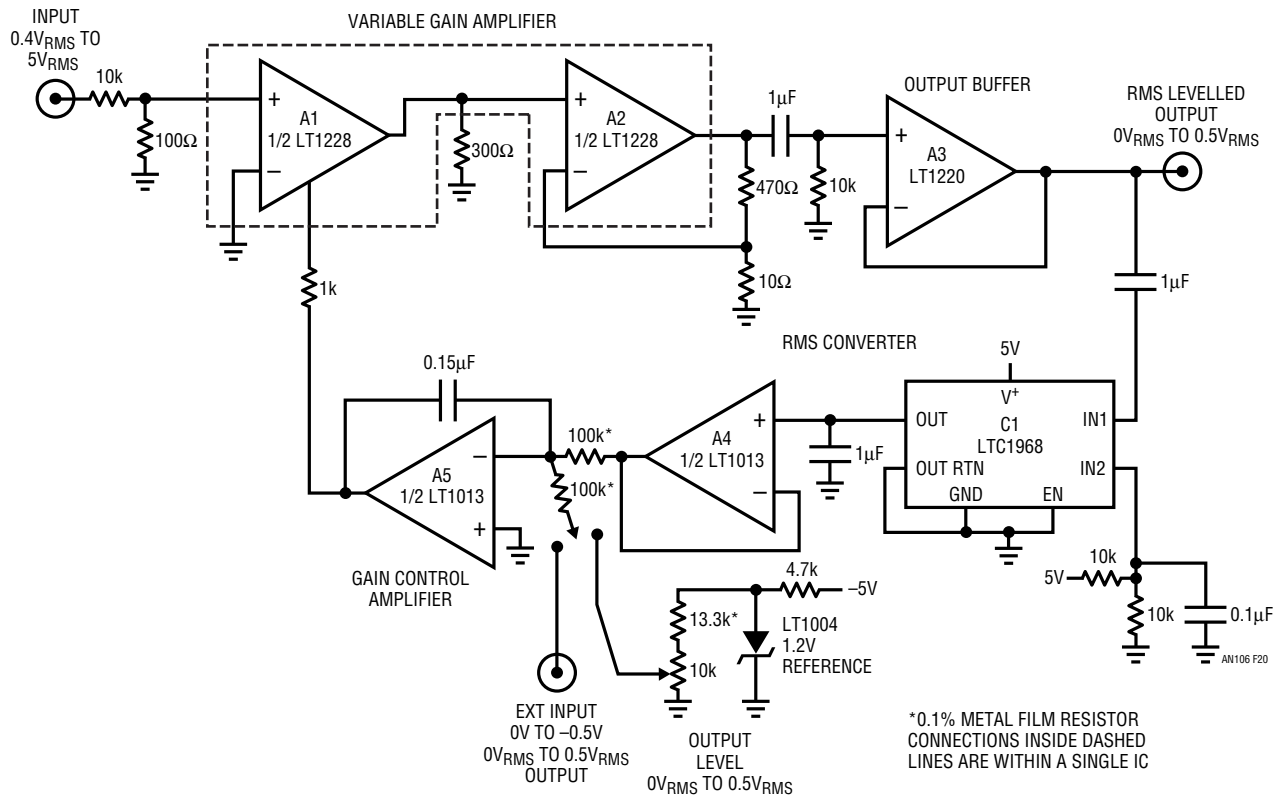


Figure 20. RMS Amplitude Level Control Uses Figure 17's Gain Control Loop. A1-A3 Provide Variable Gain to Input. RMS Converter Feeds Back to A5 Gain Control Amplifier, Closing Amplitude Stabilization Loop. Variable Reference Permits Settable, Calibrated RMS Output Amplitude Independent of Input Waveshape

RMS Amplitude Stabilized Level Controller

Figure 20 borrows the previous circuit's gain control loop to stabilize the RMS amplitude of an arbitrary input waveform. The unregulated input is applied to variable gain amplifier A1-A2 which feeds A3. DC coupling at A1-A2 permits passage of low frequency inputs. A3's output is

taken by RMS-to-DC converter C1-A4, which feeds the A5 gain control amplifier. A5 compares the RMS value to a variable reference and biases A1, closing a gain control loop. The 0.15 μ F feedback capacitor stabilizes this loop, even for waveforms below 100Hz. This feedback action stabilizes output RMS amplitude despite large variations

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in input amplitude while maintaining waveshape. Desired output level is settable with the indicated potentiometer or an external control voltage may be switched in.

Figure 21 shows output response (trace B) to abrupt reference level set point changes (trace A). The output settles within 60 milliseconds for ascending and descending transitions. Faster response is possible by decreasing A5's compensation capacitor, but low frequency waveforms

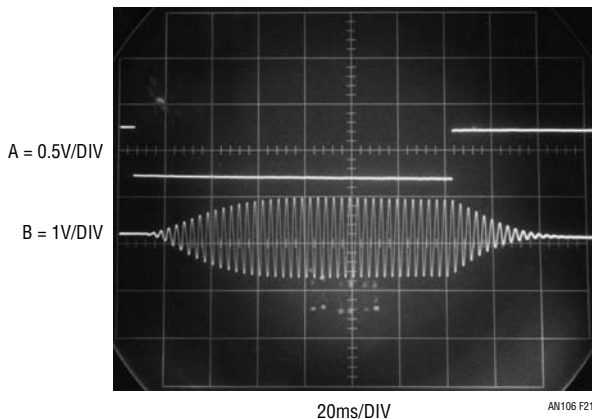


Figure 21. Amplitude Level Control Response (Trace B) to Abrupt Reference Changes (Trace A). Settling Time is Set by A5's Compensation Capacitor, Which Must be Large Enough to Stabilize Loop at Lowest Expected Input Frequency

would not be processable. Similar considerations apply to Figure 22's response to an input waveform step change. Trace A is the circuit's input and trace B its output. The output settles in 60 milliseconds due to A5's compensation. Reducing compensation value speeds response at the expense of low frequency waveform processing capability. Specifications include 0.1% output amplitude stability for inputs varying from 0.4V_{RMS} to 5V_{RMS}, 1% set point accuracy, 0.1kHz to 500kHz passband and 0.1% stability for 20% power supply deviation.

Note: This Application Note was derived from a manuscript originally prepared for publication In EDN magazine.

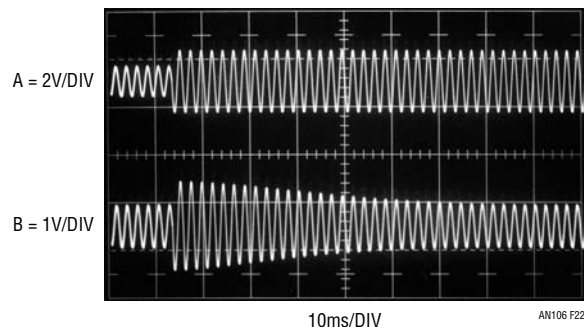


Figure 22. Amplitude Level Control Output Reacts (Trace B) to Input Step Change (Trace A). Slow Loop Compensation Allows Overshoot But Output Settles Cleanly

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Application Note 106

APPENDIX A

RMS-TO-DC CONVERSION

Joseph Petrofsky

Definition of RMS

RMS amplitude is the consistent, fair and standard way to measure and compare dynamic signals of all shapes and sizes. Simply stated, the RMS amplitude is the heating potential of a dynamic waveform. A $1V_{RMS}$ AC waveform will generate the same heat in a resistive load as will 1V DC. See Figure A1.

Mathematically, RMS is the “Root of the Mean of the Square”:

$$V_{RMS} = \sqrt{V^2}$$

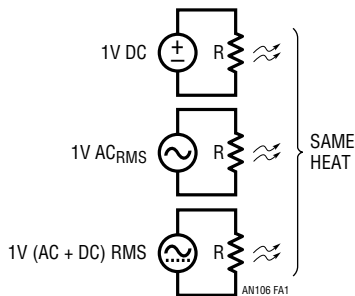


Figure A1

Alternatives to RMS

Other ways to quantify dynamic waveforms include peak detection and average rectification. In both cases, an average (DC) value results, but the value is only accurate at the one chosen waveform type for which it is calibrated, typically sine waves. The errors with average rectification are shown in Table A1. Peak detection is worse in all cases and is rarely used.

Table A1. Errors with Average Rectification vs True RMS

WAVEFORM	V_{RMS}	AVERAGE RECTIFIED (V)	ERROR*
Square Wave	1.000	1.000	11%
Sine Wave	1.000	0.900	*Calibrate for 0% Error
Triangle Wave	1.000	0.866	-3.8%
SCR at 1/2 Power, $\Theta = 90^\circ$	1.000	0.637	-29.3%
SCR at 1/4 Power, $\Theta = 114^\circ$	1.000	0.536	-40.4%

The last two entries of Table A1 are chopped sine waves as is commonly created with thyristors such as SCRs and Triacs. Figure A2a shows a typical circuit and Figure A2b shows the resulting load voltage, switch voltage and load currents. The power delivered to the load depends on the firing angle, as well as any parasitic losses such as switch “ON” voltage drop. Real circuit waveforms will also typically have significant ringing at the switching transition, dependent on exact circuit parasitics. Here, “SCR Waveforms” refers to the ideal chopped sine wave, though the LTC1966/LTC1967/LTC1968 will do faithful RMS-to-DC conversion with real SCR waveforms as well.

The case shown is for $\Theta = 90^\circ$, which corresponds to 50% of available power being delivered to the load. As noted in Table A1, when $\Theta = 114^\circ$, only 25% of the available power is being delivered to the load and the power drops quickly as Θ approaches 180° .

With an average rectification scheme and the typical calibration to compensate for errors with sine waves, the RMS level of an input sine wave is properly reported; it is only with a non-sinusoidal waveform that errors occur. Because of this calibration, and the output reading in V_{RMS} , the term True-RMS got coined to denote the use of an actual RMS-to-DC converter as opposed to a calibrated average rectifier.

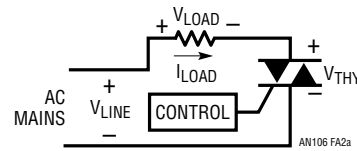


Figure A2a

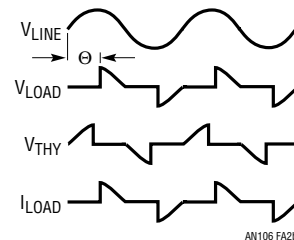


Figure A2b

How an RMS-to-DC Converter Works

Monolithic RMS-to-DC converters use an implicit computation to calculate the RMS value of an input signal. The fundamental building block is an analog multiply/divide used as shown in Figure A3. Analysis of this topology is easy and starts by identifying the inputs and the output of the lowpass filter. The input to the LPF is the calculation from the multiplier/divider; $(V_{IN})^2/V_{OUT}$. The lowpass filter will take the average of this to create the output, mathematically:

$$V_{OUT} = \left(\frac{(V_{IN})^2}{V_{OUT}} \right)$$

Because V_{OUT} is DC,

$$\left(\frac{(V_{IN})^2}{V_{OUT}} \right) = \frac{(V_{IN})^2}{V_{OUT}}, \text{ so}$$

$$V_{OUT} = \frac{(V_{IN})^2}{V_{OUT}}, \text{ and}$$

$$(V_{OUT})^2 = (V_{IN})^2, \text{ or}$$

$$V_{OUT} = \sqrt{(V_{IN})^2} = \text{RMS}(V_{IN})$$

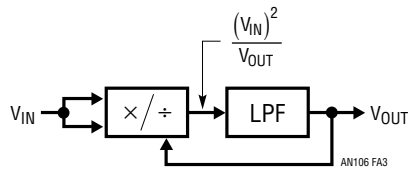


Figure A3 RMS-to-DC Converter with Implicit Computation

Unlike the prior generation RMS-to-DC converters, the LTC1966/LTC1967/LTC1968 computation does NOT use log/antilog circuits, which have all the same problems, and more, of log/antilog multipliers/dividers, i.e., linearity is poor, the bandwidth changes with the signal amplitude and the gain drifts with temperature.

How the LTC1966/LTC1967/LTC1968 RMS-to-DC Converters Work

The LTC1966/LTC1967/LTC1968 use a completely new topology for RMS-to-DC conversion, in which a $\Delta\Sigma$ modulator acts as the divider, and a simple polarity switch is used as the multiplier as shown in Figure A4.

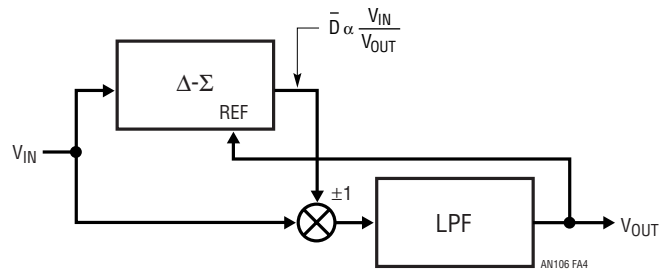


Figure A4. Topology of the LTC1966/LTC1967/LTC1968

The $\Delta\Sigma$ modulator has a single-bit output whose average duty cycle (\bar{D}) will be proportional to the ratio of the input signal divided by the output. The $\Delta\Sigma$ is a 2nd order modulator with excellent linearity. The single-bit output is used to selectively buffer or invert the input signal. Again, this is a circuit with excellent linearity, because it operates at only two points: ± 1 gain; the average effective multiplication over time will be on the straight line between these two points. The combination of these two elements again creates a lowpass filter input signal equal to $(V_{IN})^2/V_{OUT}$, which, as shown above, results in RMS-to-DC conversion.

The lowpass filter performs the averaging of the RMS function and must be a lower corner frequency than the lowest frequency of interest. For line frequency measurements, this filter is simply too large to implement on-chip, but the LTC1966/LTC1967/LTC1968 need only one capacitor on the output to implement the lowpass filter. The user can select this capacitor depending on frequency range and settling time requirements.

This topology is inherently more stable and linear than log/antilog implementations primarily because all of the signal processing occurs in circuits with high gain op amps operating closed loop.

Note that the internal scalings are such that the $\Delta\Sigma$ output duty cycle is limited to 0% or 100% only when V_{IN} exceeds $\pm 4 \cdot V_{OUT}$.

Application Note 106

Linearity of an RMS-to-DC Converter

Linearity may seem like an odd property for a device that implements a function that includes two very nonlinear processes: squaring and square rooting.

However, an RMS-to-DC converter has a transfer function, RMS volts in to DC volts out, that should ideally have a 1:1 transfer function. To the extent that the input to output transfer function does not lie on a straight line, the part is nonlinear.

A more complete look at linearity uses the simple model shown in Figure A5. Here an ideal RMS core is corrupted by both input circuitry and output circuitry that have imperfect transfer functions. As noted, input offset is introduced in the input circuitry, while output offset is introduced in the output circuitry.

Any nonlinearity that occurs in the output circuitry will corrupt the RMS in to DC out transfer function. A nonlinearity in the input circuitry will typically corrupt that transfer function far less simply because with an AC input, the RMS-to-DC conversion will average the nonlinearity from a whole range of input values together.

But the input nonlinearity will still cause problems in an RMS-to-DC converter because it will corrupt the accuracy as the input signal shape changes. Although an RMS-to-DC converter will convert any input waveform to a DC output, the accuracy is not necessarily as good for all waveforms as it is with sine waves. A common way to describe dynamic signal wave shapes is Crest Factor. The crest factor is the ratio of the peak value relative to the RMS value of a waveform. A signal with a crest factor of 4, for instance, has a peak that is four times its RMS value. Because this peak has energy (proportional to voltage squared) that is 16 times (4^2) the energy of the RMS value, the peak is necessarily present for at most 6.25% (1/16) of the time.

The LTC1966/LTC1967/LTC1968 perform very well with crest factors of 4 or less and will respond with reduced accuracy to signals with higher crest factors. The high performance with crest factors less than 4 is directly attributable to the high linearity throughout the LTC1966/LTC1967/LTC1968.

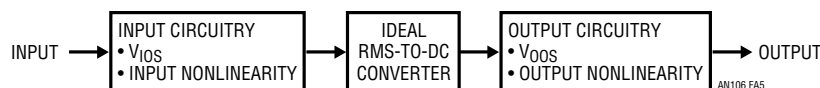


Figure A5. Linearity Model of an RMS-to-DC Converter

APPENDIX B

AC Measurement and Signal Handling Practice

Accurate AC measurement requires trustworthy instrumentation, proper signal routing technique, parasitic minimization, attention to layout and care in component selection. The text circuits DC-500kHz, 1% error bandwidth seems benign, but unpleasant surprises await the unwary.

An accurate RMS voltmeter is required for serious AC work. Figure B1 lists types used in our laboratory. These are high grade, specialized instruments specifically intended for precise RMS measurement. All are thermally based¹. The first three entries, general purpose instruments with many ranges and features, are easily used and meet almost all AC measurement needs. The last entry is more of a component than an instrument. The A55 series of “thermal converters” provide millivolt level outputs for various inputs. Typical input ranges are 0.5V_{RMS}, 1V_{RMS}, 2V_{RMS} and 5V_{RMS} and each converter is supplied with individual calibration data. They are somewhat cumbersome to use and easily destroyed but are highly accurate. Their primary use is as reference standards to check other instrument’s performance.

AC signal handling for high accuracy is a broad topic, involving a considerable degree of depth. This forum must suffer brevity, but some gossip is possible.

Layout is critical. The most prevalent parasitic in AC measurement is stray capacitance. Keep signal path connections short and small area. A few picofarrads of coupling into a high impedance node can upset a 500kHz, 1% accuracy signal path. To the extent possible, keep impedances low to minimize parasitic capacitive effects. Consider individual component parasitics and plan to accommodate them. Examine effects of component placement and orientation on the circuit board. If a ground plane is in use it may be necessary to relieve it in the vicinity of critical circuit nodes or even individual components.

Passive components have parasitics that must be kept in mind. Resistors suffer shunt capacitance whose effects vary with frequency and resistor value. It is worth noting that different brands of resistors, although nominally similar, may exhibit markedly different parasitic behavior. Capacitors in the signal path should be used so that their outer foil is connected to the less sensitive node, affording some relief from pick-up and stray capacitance induced effects. Some capacitors are marked to indicate the outer foil terminal, others require consulting the data sheet or vendor contact. Avoid ceramic capacitors in the signal path. Their piezoelectric responses make them unsuitable for precision AC circuitry. In general, any component in the signal path should be examined in terms of its potential parasitic contribution.

¹See references 1 and 2 for details on thermally based RMS-to-DC conversion.

MODEL	MANUFACTURER	1V RANGE	INPUT	BANDWIDTH	COMMENTS
3400A/3400B	Hewlett-Packard	1%	AC	10MHz/20MHz	Metered Instrument. Most Common RMS Voltmeter
3403C	Hewlett-Packard	0.2%	AC, AC + DC	100MHz	Digital Display, 1μV Sensitivity (2MHz BW), dB Ranges, Relative dB
8920/8921A	Fluke	0.7%	AC, AC + DC	20MHz	Digital Display, 10μV Sensitivity (2MHz BW), dB Ranges, Relative dB
A55	Fluke	0.05%	AC + DC	50MHz	Set of Individually Calibrated Thermal Converters. Reference Standards. Not for General Purpose Measurement

Figure B1. Precision Wideband RMS Voltmeters Useful for AC Measurement. All are Thermally Based, Permitting High Accuracy and Wide Bandwidth Independent of Input Waveshape. A55 Reference Standards, Although Unsuitable for General Purpose Measurement, Have Best Accuracy

Application Note 106

Active components, such as amplifiers, must be treated as potential error sources. In particular, as stated in the text, ensure that there is enough open loop gain at the frequency of interest to assure needed closed loop gain accuracy. Margins of 100:1 are not unreasonable. Keep feedback values as low as possible to minimize parasitic effects.

Route signals to and from the circuit board coaxially and at low impedance, preferably 50Ω, for best results. In 50Ω systems, remember that terminators and attenuators

have tolerances that can corrupt a 1% amplitude accuracy measurement. Verify such terminator and attenuator tolerances by measurement and account for them when interpreting measurement results. Similarly, verify the accuracy of any associated instruments 50Ω input or output impedance and account for deviations.

This all seems painful but is an essential part of achieving 1% accurate, 500kHz signal integrity. Failure to observe the precautions listed above risks degrading the RMS-to-DC converters system level performance.

APPENDIX C

Symmetrical White Gaussian Noise

by Ben Hessen-Schmidt,
NOISE COM, INC.

White noise provides instantaneous coverage of all frequencies within a band of interest with a very flat output spectrum. This makes it useful both as a broadband stimulus and as a power-level reference.

Symmetrical white Gaussian noise is naturally generated in resistors. The noise in resistors is due to vibrations of the conducting electrons and holes, as described by Johnson and Nyquist.¹ The distribution of the noise voltage is symmetrically Gaussian, and the average noise voltage is:

$$\bar{V}_n = 2\sqrt{kT \int R(f) p(f) df} \quad (1)$$

where:

- k = 1.38E-23 J/K (Boltzmann's constant)
- T = temperature of the resistor in Kelvin
- f = frequency in Hz
- h = 6.62E-34 Js (Planck's constant)
- R(f) = resistance in ohms as a function of frequency

$$p(f) = \frac{hf}{kT[\exp(hf/kT) - 1]} \quad (2)$$

p(f) is close to unity for frequencies below 40GHz when T is equal to 290°K. The resistance is often assumed to be independent of frequency, and $\int df$ is equal to the noise bandwidth (B). The available noise power is obtained when the load is a conjugate match to the resistor, and it is:

$$N = \frac{\bar{V}_n^2}{4R} = kTB \quad (3)$$

where the “4” results from the fact that only half of the noise voltage and hence only 1/4 of the noise power is delivered to a matched load.

Equation 3 shows that the available noise power is proportional to the temperature of the resistor; thus it is often called thermal noise power, Equation 3 also shows that white noise power is proportional to the bandwidth.

An important source of symmetrical white Gaussian noise is the noise diode. A good noise diode generates a high level of symmetrical white Gaussian noise. The level is often specified in terms of excess noise ratio (ENR).

$$\text{ENR (in dB)} = 10\text{Log} \frac{(T_e - 290)}{290} \quad (4)$$

T_e is the physical temperature that a load (with the same impedance as the noise diode) must be at to generate the same amount of noise.

¹See “Additional Reading” at the end of this section.

The ENR expresses how many times the effective noise power delivered to a non-emitting, nonreflecting load exceeds the noise power available from a load held at the reference temperature of 290°K (16.8°C or 62.3°F).

The importance of high ENR becomes obvious when the noise is amplified, because the noise contributions of the amplifier may be disregarded when the ENR is 17dB larger than the noise figure of the amplifier (the difference in total noise power is then less than 0.1dB). The ENR can easily be converted to noise spectral density in dBm/Hz or $\mu\text{V}/\sqrt{\text{Hz}}$ by use of the white noise conversion formulas in Table 1.

Table 1. Useful White Noise Conversion

dBm	=	dBm/Hz + 10log (BW)
dBm	=	20log ($\sqrt{V_n}$) - 10log(R) + 30dB
dBm	=	20log($\sqrt{V_n}$) + 13dB for R = 50 Ω
dBm/Hz	=	20log($\mu\sqrt{V_n}/\sqrt{\text{Hz}}$) - 10log(R) - 90dB
dBm/Hz	=	-174dBm/Hz + ENR for ENR > 17dB

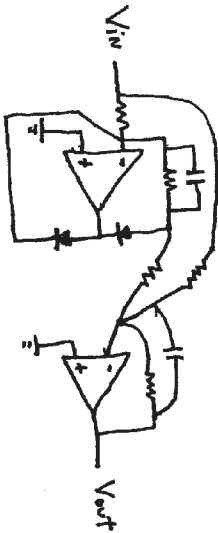
When amplifying noise it is important to remember that the noise voltage has a Gaussian distribution. The peak voltages of noise are therefore much larger than the average or RMS voltage. The ratio of peak voltage to RMS voltage is called crest factor, and a good crest factor for Gaussian noise is between 5:1 and 10:1 (14 to 20dB). An amplifier's 1dB gain-compression point should therefore be typically 20dB larger than the desired average noise-output power to avoid clipping of the noise.

For more information about noise diodes, please contact NOISE COM, INC. at (973) 386-9696.

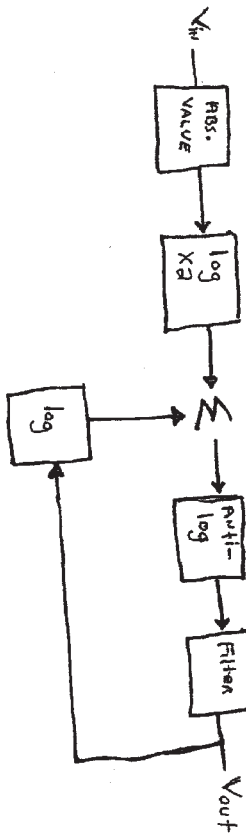
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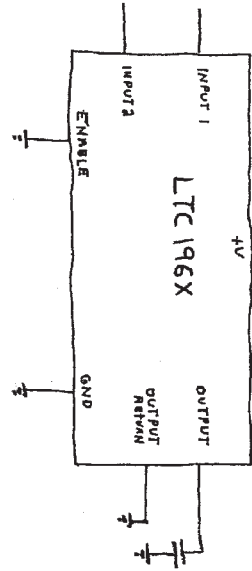
Application Note 106



The Ugly



The Bad



The Good

— 100Ω —

Developments in Battery Stack Voltage Measurement

A Simple Solution to a Not So Simple Problem

Jim Williams and Mark Thoren

Automobiles, aircraft, marine vehicles, uninterruptible power supplies and telecom hardware represent areas utilizing series connected battery stacks. These stacks of individual cells may contain many units, reaching potentials of hundreds of volts. In such systems it is often desirable to accurately determine each individual cell's voltage. Obtaining this information in the presence of the high "common mode" voltage generated by the battery stack is more difficult than might be supposed.

The Battery Stack Problem

The "battery stack problem" has been around for a long time. Its deceptively simple appearance masks a stubbornly resistant problem. Various approaches have been tried, with varying degrees of success.¹

Figure 1's voltmeter measures a single cell battery. Beyond the obvious, the arrangement works because there are no voltages in the measurement path other than the measured. The ground referred voltmeter only encounters the voltage to be measured.

Figure 2's "stack" of series connected cells is more complex and presents problems. The voltmeter must be switched between the cells to determine each individual cell's voltage. Additionally, the voltmeter, normally composed of relatively low voltage breakdown components, must withstand input voltage relative to its ground terminal. This "common mode" voltage may reach hundreds of

volts in a large series connected battery stack such as is used in an automobile. Such high voltage operation is beyond the voltage breakdown capabilities of most practical semiconductor components, particularly if accurate measurement is required. The switches present similar problems. Attempts at implementing semiconductor based switches encounter difficulty due to voltage breakdown

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¹See Appendix A, "A Lot of Cut Off Ears and No Van Goghs" for detail and commentary on some typical approaches.

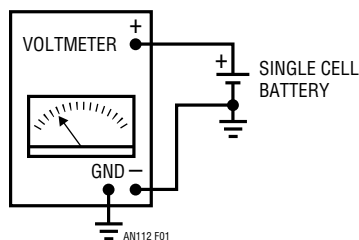


Figure 1. Voltmeter Measuring Ground Referred Single Cell is Not Subjected to Common Mode Voltage

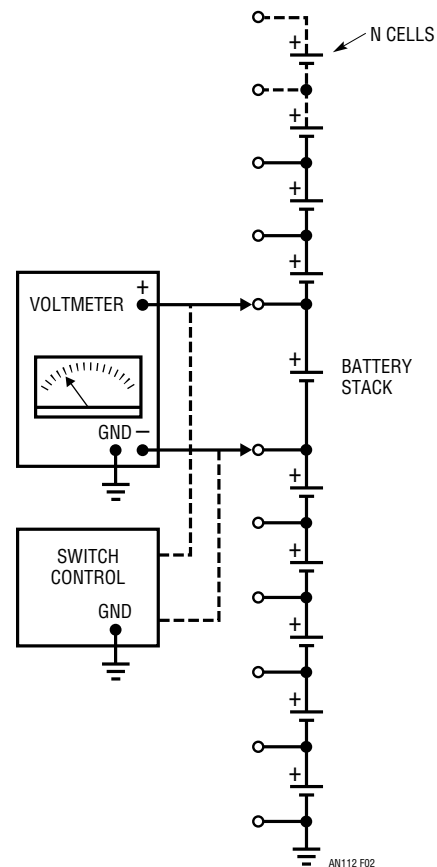


Figure 2. Voltmeter Measuring Cell in Stack Undergoes Increasing Common Mode Voltage as Measurement Proceeds Up Stack. Switches and Switch Control Also Encounter High Voltages

an112f

Application Note 112

and leakage limitations. What is really needed is a practical method that accurately extracts individual cell voltages while rejecting common mode voltages. This method cannot draw any battery current and should be simple and economically implemented.

Transformer Based Sampling Voltmeter

Figure 3's concept addresses these issues. Battery voltage (V_{BATTERY}) is determined by pulse exciting a transformer (T1) and recording transformer primary clamp voltage after settling occurs. This clamp voltage is predominately set by the diode and V_{BATTERY} shunting and similarly clamping T1's secondary. The diode and a small transformer term constitute predictable errors and are subtracted out, leaving V_{BATTERY} as the output.

Detailed Circuit Operation

Figure 4 is a detailed version of the transformer based sampling voltmeter. It closely follows Figure 3 with some minor differences which are described at this section's conclusion. The pulse generator produces a $10\mu\text{s}$ wide event (Trace A, Figure 5) at a 1kHz repetition rate. The pulse generator's low impedance output drives T1 via a 10k resistor and also triggers the delayed pulse generator.

T1's primary (Trace B) responds by rising to a value representing the sum of $V_{\text{DIODE}} + V_{\text{BATTERY}}$ along with a small fixed error contributed by the transformer. T1's primary clamps at this value. After a time (Trace C) dictated by the delayed pulse generator a pulse (Trace D) closes S1, allowing C1 to charge towards T1's clamped value. After a number of pulses C1 assumes a DC level identical to T1's primary clamp voltage. A1 buffers this potential and feeds differential amplifier A2. A2, operating at a gain near unity, subtracts the diode and transformer error terms, resulting in a direct reading V_{BATTERY} output.

Accuracy is critically dependent on transformer clamping fidelity over temperature and clamp voltage range. The carefully designed transformer specified yields Figure 6's waveforms. Primary (Trace A) and secondary (Trace B) clamping detail appear at highly expanded vertical scale. Clamping flatness is within millivolts; trace center aberrations derive from S1 gate feedthrough. Tight transformer clamp coupling promotes good performance. Circuit accuracy at 25°C is 0.05% over a 0V to 2V battery range with $120\text{ppm}/^\circ\text{C}$ drift, degrading to 0.25% at $V_{\text{BATTERY}} = 3\text{V}$.²

²Battery stack voltage monitor development is aided by the floating, variable potential battery simulator described in Appendix B.

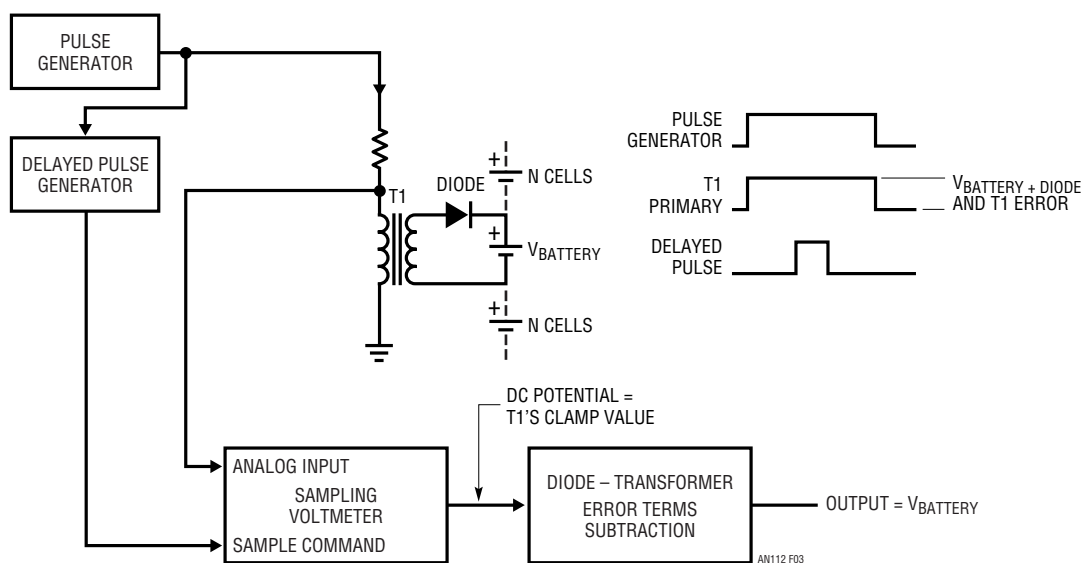


Figure 3. Transformer-Based Sampling Voltmeter Operates Independently of High Common Mode Voltages. Pulse Generator Periodically Activates T1. Delayed Pulse Triggers Sampling Voltmeter, Capturing T1's Clamped Value. Residual Error Terms are Corrected in Following Stage

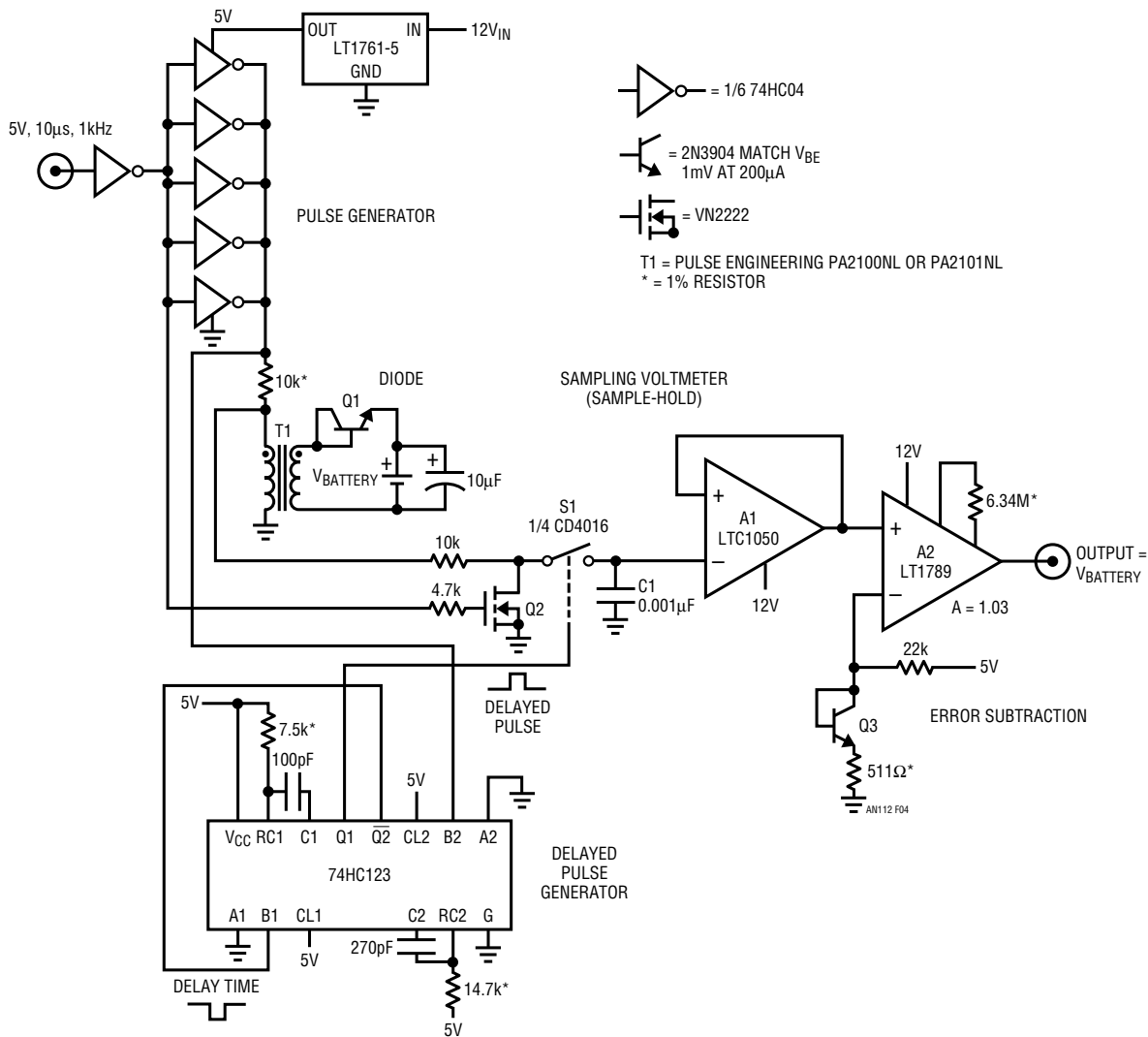


Figure 4. Transformer Fed Sampling Voltmeter Schematic Closely Follows Figure 3's Concept. Error Subtraction Terms Include Q3 Compensating Q1 and Resistor/Gain Corrections for Errors in T1's Clamping Action. Q1-Q3 Transistors Replace Diodes for More Consistent Matching. Q2 Prevents T1's Negative Recovery Excursion from Influencing S1

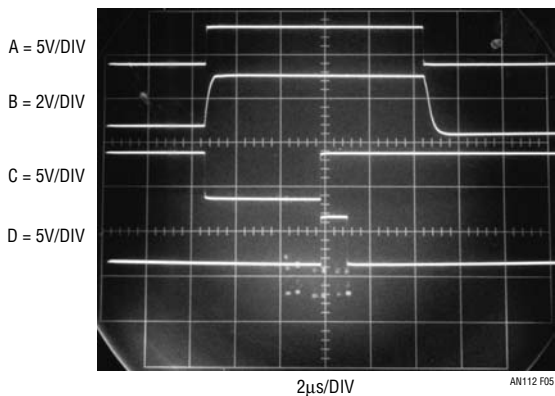


Figure 5. Figure 4's Waveforms Include Pulse Generator Input (Trace A), T1 Primary (Trace B), 74HC123 Q2 Delay Time Output (Trace C) and S1 Control Input (Trace D). Timing Ensures Sampling Occurs When T1 is Settled in Clamped State

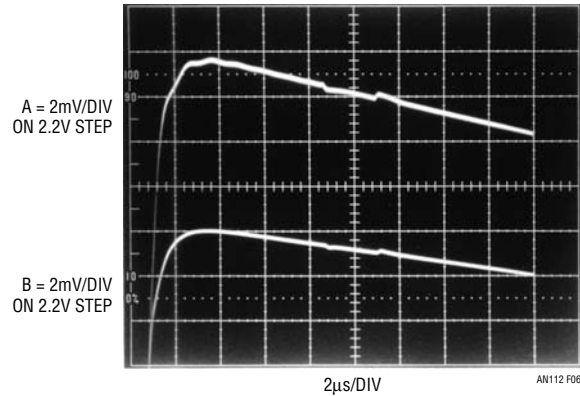


Figure 6. T1 Primary (Trace A) and Secondary (Trace B) Clamping Detail. Highly Expanded Vertical Scale Shows Primary and Secondary Clamping Flatness Within Millivolts. Trace Center Aberrations Derive from S1 Gate Feedthrough

an112f

Application Note 112

Several details aid circuit operation. Transistor V_{BE} 's, substituted for diodes, provide more consistent initial matching and temperature tracking. The $10\mu\text{F}$ capacitor at Q1 maintains low impedance at frequency, minimizing cell voltage movement during the sampling interval. Finally, synchronously switched Q2 prevents T1's negative recovery excursion from deleteriously influencing S1's operation.

This approach's advantage is that its circuitry does not encounter high common mode voltages—T1 galvanically isolates the circuit from common mode potentials associated with $V_{BATTERY}$. Thus, conventional low voltage techniques and semiconductors may be employed.

Multi-Cell Version

The transformer-based method is inherently adaptable to the multi-cell battery stack measurement problem previously described. Figure 7's conceptual schematic shows a multi-cell monitoring version. Each channel monitors one cell. Any individual channel may be read by biasing its appropriate enable line to turn on a FET switch, enabling that particular channel's transformer. The hardware required for each channel is typically limited to a transformer, a diode connected transistor and a FET switch.

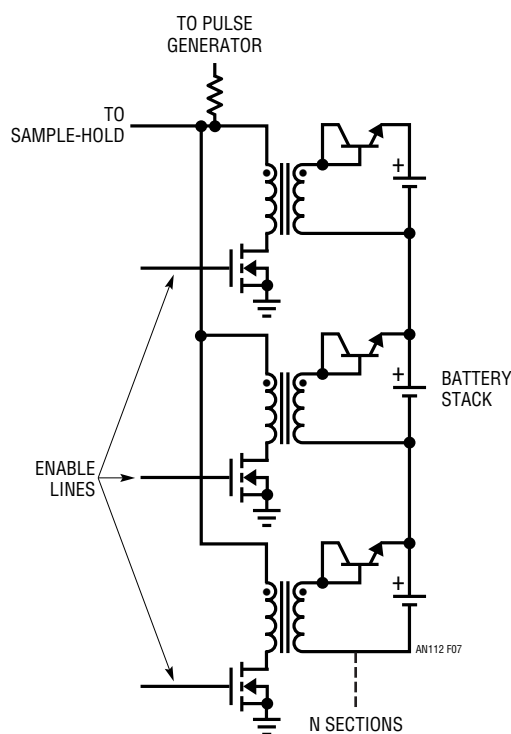


Figure 7. Multiple Channels are Facilitated by Adding Enable Lines and Transistor Switches

Automatic Control and Calibration

This scheme is suited to digitally based techniques for automatic calibration. Figure 8 uses a PIC16F876A microcontroller, fed from an LTC1867 analog to digital converter, to control the pulse generators and channel selection. As before, even though the cell stack may reach hundreds of volts, the transformer galvanic isolation allows the signal path components to operate at low voltage.

A further benefit of processor driven operation is elimination of Figure 4's V_{BE} diode matching requirement. In practice, a processor-based board is tested at room temperature with known voltages applied to all input terminals. The channels are then read, furnishing the information necessary for the processor to determine each channel's initial V_{BE} and gain. These parameters are then stored in nonvolatile memory, permitting a one-time calibration that eliminates both V_{BE} mismatch and gain mismatch induced errors.

Channels 6 and 7 provide zero and 1.25V reference voltages representing cell voltage extremes. The room-temperature values are stored to nonvolatile memory. As temperature changes occur, readings from channel 6 and 7 are used to calculate a change in offset and a change in gain that are applied to the six measurement channels. The calibration is maintained as temperature varies because each channel's $-2\text{mV}/^\circ\text{C}$ V_{BE} drift slopes are nearly identical. Similarly, gain errors from channel to channel are nearly identical.

Since the gain and offset are continuously calibrated, the gain and offset of the LTC1867 drop out of the equation. The only points that must be accurate are the 0V measurement (easy, just short the channel 6 inputs together) and the 1.25V reference voltage, provided by an LT[®]1790-1.25. The LTC[®]1867 internally amplifies its internal 2.5V reference to 4.096V at the REFCOMP pin, which sets the full scale of the ADC (4.096V when it is configured for unipolar mode, $\pm 2.048\text{V}$ in bipolar mode). Thus the absolute maximum cell voltage that can be measured is 3.396V. And since the offset measurement is nominally 0.7V at the ADC input it is never in danger of clamping at zero. (A zero reading will result if a given LTC1867 has a negative offset and the input voltage is any positive voltage less than or equal to the offset.)

Accuracy of the processor-driven circuit is 1mV over a 0V to 2V input range at 25°C. Drift drops to less than 50ppm/°C—almost 3x lower than Figure 4.

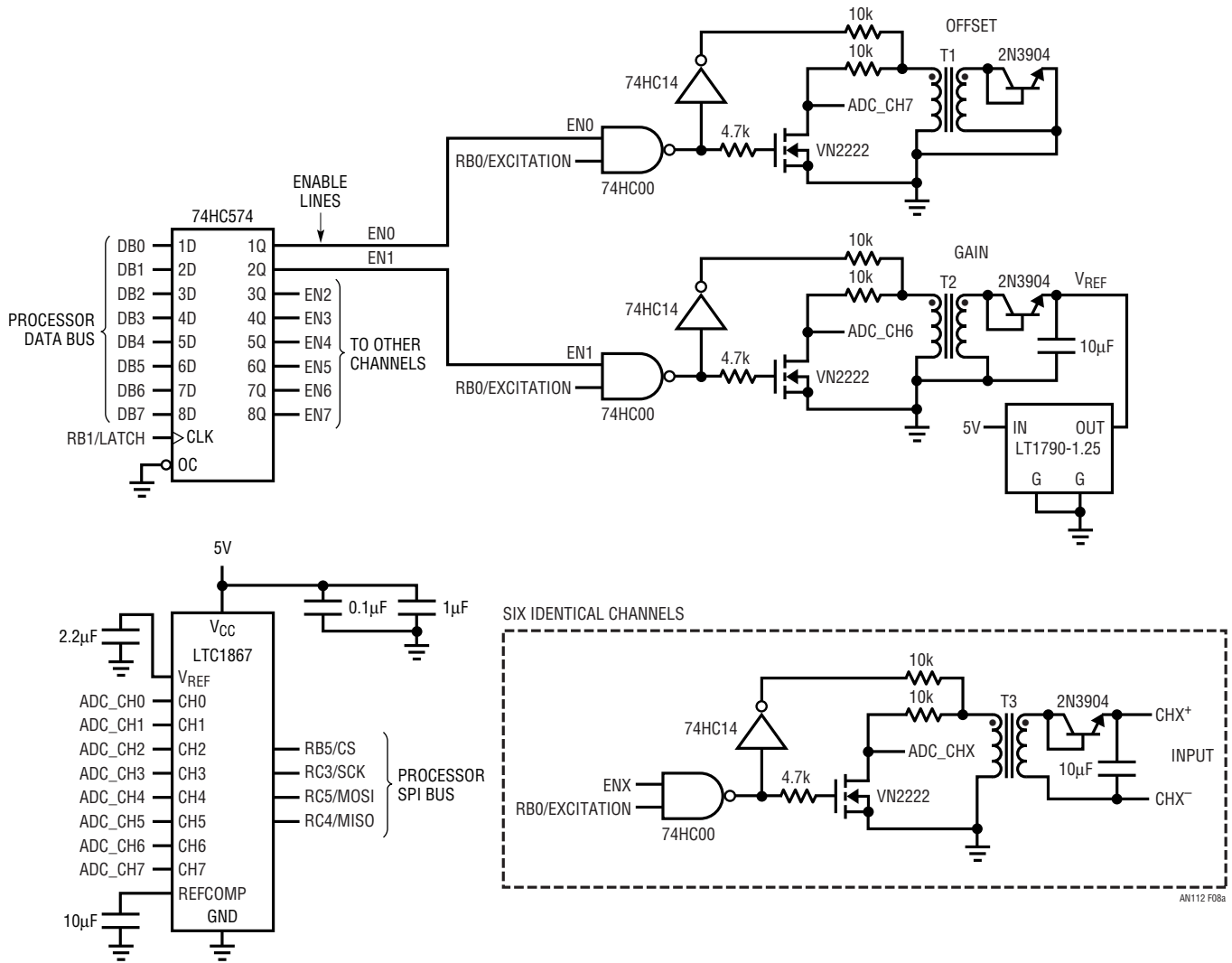


Figure 8a. Pulse Generators, Calibration Channels, Measurement Channels. ADC Calibration Channels Eliminate V_{BE} Matching Requirement and Compensate for Temperature Dependent Errors

Application Note 112

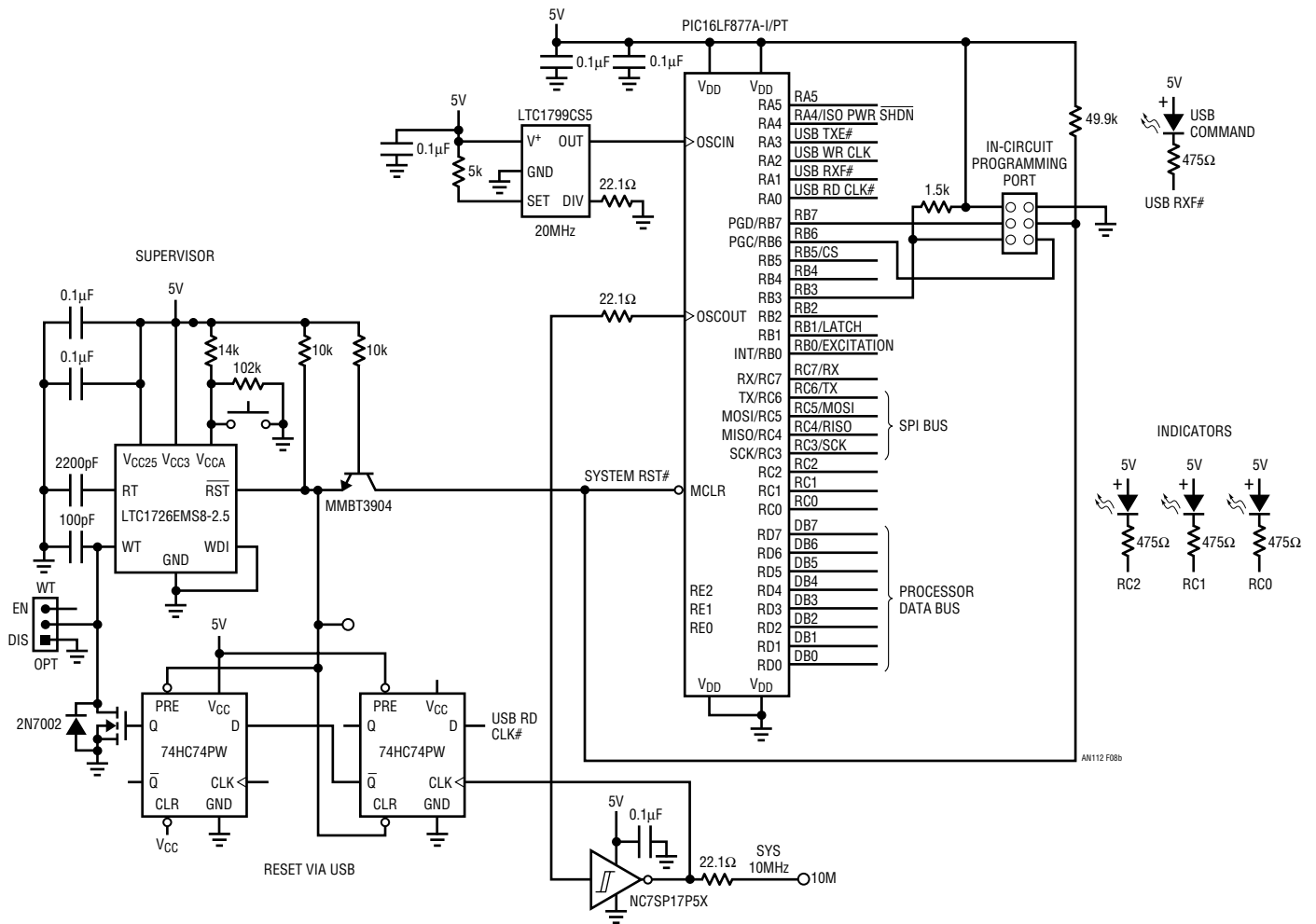


Figure 8b. Microcontroller and Reset

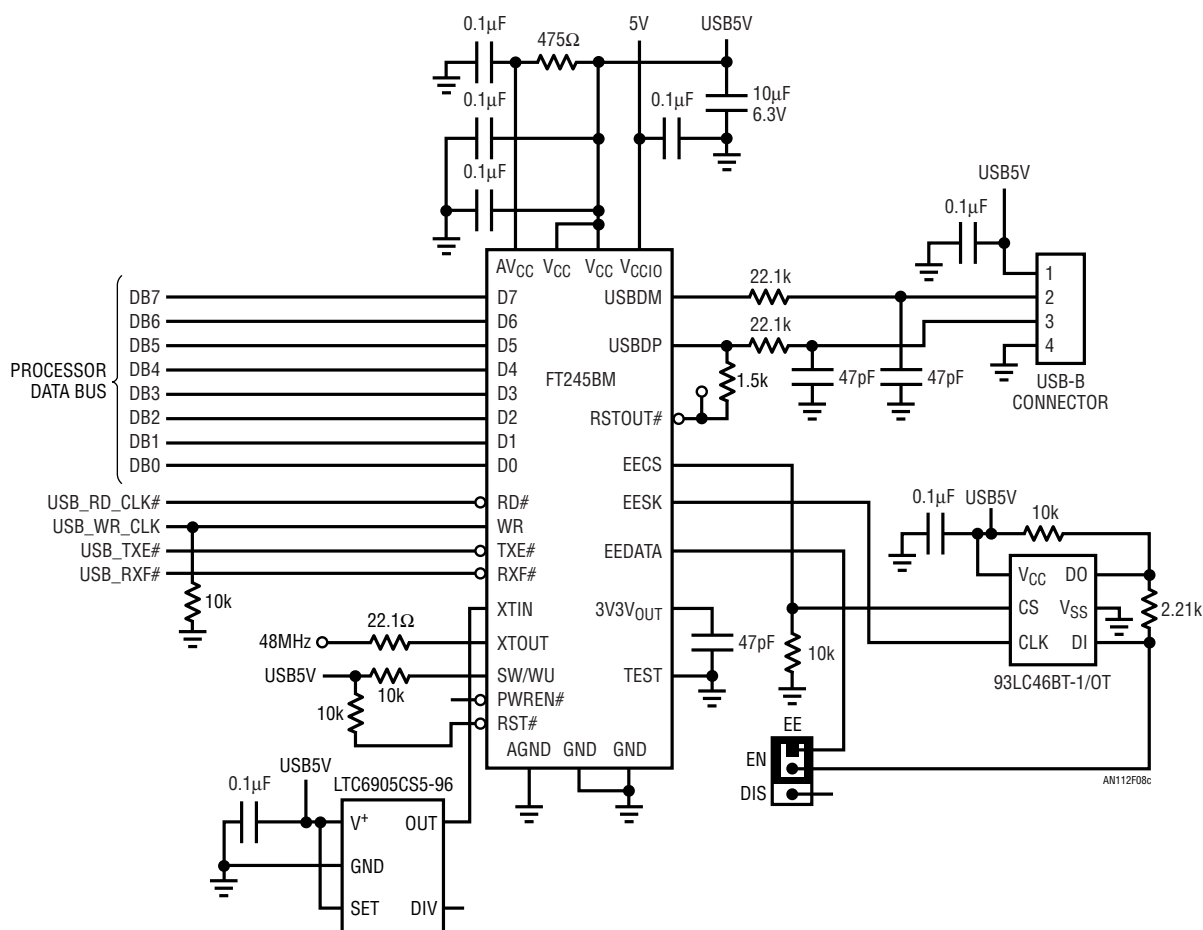


Figure 8c. USB Interface (for Development Only)

Firmware Description

The complete firmware code listing is in Appendix C. The code for this circuit is designed to be a good starting point for an actual product. Data is displayed to a PC via an FTDI FT242B USB interface IC. The PC has FTDI’s Virtual Com Port drivers installed, allowing control through any terminal program. Data for all channels is continuously displayed to the terminal, and simple text commands control program operation.

A timer interrupt is called 1000 times per second. It controls the pulse generators and ADC, and stores the ADC readings to an array that can be read at any time. Thus if the main program is reading the buffer, the most out-of-date any reading will be is 1ms.

Automatic calibration routines are also included. Two functions store a zero reading and a full-scale reading for

all channels, including the calibration voltages applied to channels 6 and 7, to nonvolatile memory. These are subsequently used to calibrate out the initial gain and offset errors as well as temperature dependent errors. The entire procedure is to apply zero volts to all inputs and issue a command to store the zero calibration, then apply 1.25V to all inputs and issue a command to store the full-scale calibration. Note that this is no more complicated than a basic functionality test that would be part of any manufacturing process. The 1.25V factory calibration source can be from a voltage calibrator, or from a selected “golden” LT1790-1.25 that is kept at a stable temperature.

A digital filter is also included for testing purposes. The filter is a simple exponential IIR (infinite impulse response) filter with a constant of 0.1. This reduces the noise seen in the readings by a factor of $\sqrt{10}$.

Application Note 112

Measurement Details

To take a reading from a given channel, the processor must apply the excitation to the transformer, wait for the voltage signal to settle out, take a reading with the ADC, and then remove the excitation. This is driven by an interrupt service routine that is called once every millisecond. Refer to Appendix C for the code listing. Figure 9 shows the digital signals, excitation pulse, and clamp voltage at the ADC input along with the C code that performs these operations.³

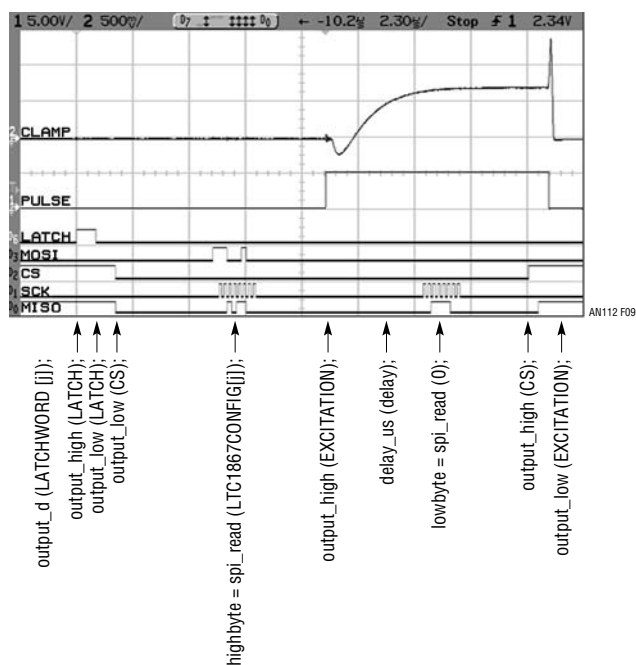


Figure 9. Pulse Generator and ADC Sequencing

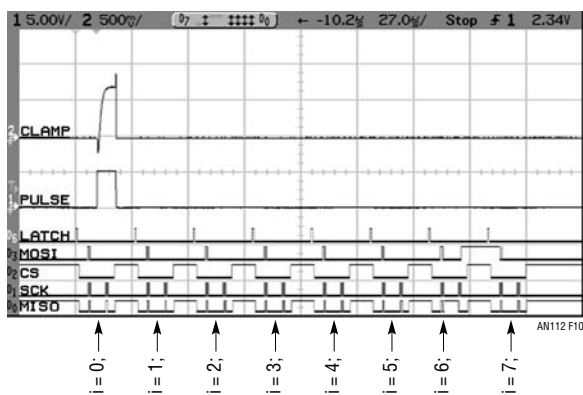


Figure 10. ISR Scanning 8 Channels

Individual channels are enabled by loading an 8 bit byte with one bit set high into the 74HC574 latch.

Note that the excitation is applied after 8 bits of the LTC1867 data are read out. This is perfectly acceptable, since there is no conversion taking place and all of the data in the LTC1867 output register is static. Depending on the specific timing of the processor being used, excitation may be applied before reading any data, in the middle of reading data, or after reading the data but before initiating a conversion. If the serial clock is very slow—1MHz for instance, applying excitation before reading any data would result in the excitation being applied for 16 μ s which is too long. The only constraint is that the voltage at the ADC input must have enough time to settle properly and that the excitation is not left on for too long. Figure 10 shows the same signals over the entire interrupt service routine. There are similar analog signals at each transformer and the other LTC1867 inputs.

Adding More Channels

There are lots of ways to add more channels to this circuit. Figure 11 shows a 64 channel concept. Figure 11 decodes the 64 channels into eight banks of eight channels using 74HC138 address decoders. The selected bank corresponds to one LTC1867 input that is programmed through the SPI interface. The additional analog multiplexing is done with 74HC4051 8:1 analog switches. A single 74HC4051 feeding each LTC1867 input gives 64 inputs. The LTC1867 is still a great choice in high channel count applications, rather than a single channel ADC, because it is good idea to break up multiplexer trees into several stages to minimize total channel capacitance. The LTC1867 takes care of the last stage. And with a maximum sample rate of 200ksps, it can digitize up to 200 channels at the maximum 1kps limitation of the sense transformer. That's a lot of batteries.

³Sometimes a jack-of-all-trades is exactly what you need. A high speed digital designer would never dream of trading a good logic analyzer for a mixed-signal oscilloscope to test signal integrity across a complicated backplane. And its 100MHz analog channels pale in comparison to a good four channel, half-gig scope. But for testing a circuit with a microcontroller and data converters up to a few megasamples per second, a good mixed signal oscilloscope is the master of the trade.

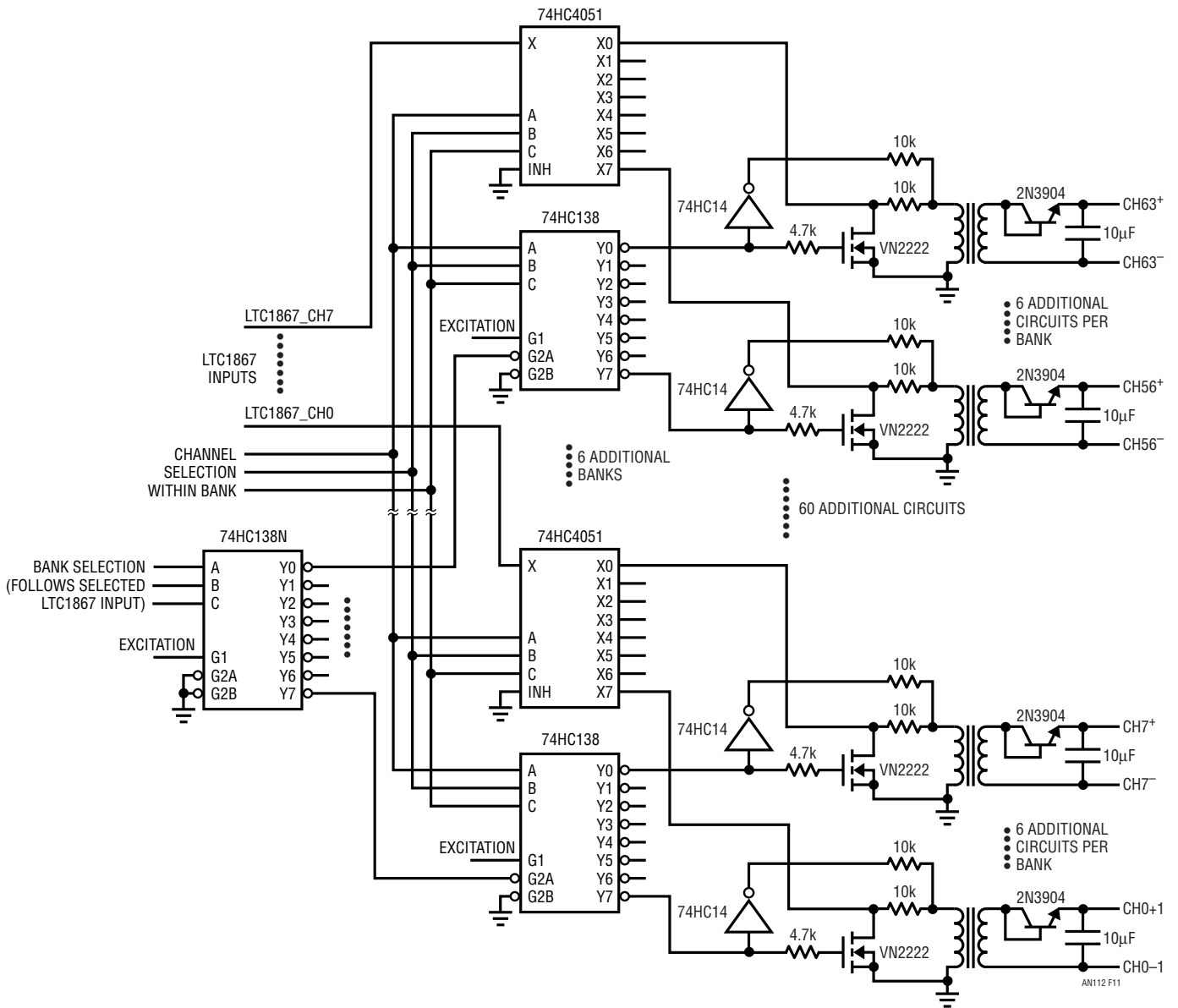


Figure 11. 64-Channel Concept

Application Note 112

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1. Williams, Jim, "Transformers and Optocouplers Implement Isolation Techniques," "Isolated Temperature Measurement," pp.116-117. EDN Magazine (January 1982)
2. Williams, Jim, "Isolated Temperature Sensor," LT198A Data Sheet. Linear Technology Corporation (1983)
3. Dobkin, R. C., "Isolated Temperature Sensor," LM135 Data Sheet. National Semiconductor Corporation (1978)
4. Williams, Jim, "Isolation Techniques for Signal Conditioning," "Isolated Temperature Measurement," pp.1-2. National Semiconductor Corporation, Application Note 298 (May 1982)
5. Sheingold, D. H., "Transducer Interfacing Handbook," "Isolation Amplifiers," pp. 81-85. Analog Devices Inc. (1980)
6. Williams, Jim, "Signal Sources, Conditioners and Power Circuitry," "0.02% Accurate Instrumentation Amplifier with $125 V_{CM}$ and 120dB CMRR," pp. 11-13. Linear Technology Corporation, Application Note 98 (November 2004)

APPENDIX A

A Lot of Cut Off Ears and No Van Goghs

Things That Don't Work

The “battery stack problem” has been around a long time. Various approaches have been tried, with varying degrees of success. The problem appears deceptively simple; technically and economically qualified solutions are notably elusive. Typical candidates and their difficulties are presented here.

Figure A1 presumably solves the problem by converting cell potentials to current, obviating the high common mode voltages. Op amps feed a multiplexed input A/D; the decoded A/D output presents individual cell voltages. This approach is seriously flawed. Required resistor precision and values are unrealistic, becoming progressively more unrealistic as the number of cells in the stack increases. Additionally, the resistors drain current from the cells, a distinct and often unallowable disadvantage.

An isolation amplifier based approach appears in Figure A2. Isolation amplifiers feature galvanically floating inputs, fully isolated from their output terminals. Typically, the device

contains modulation-demodulation circuitry and a floating supply which powers the signal input section⁴. The amplifier inputs monitor the cell; its isolation barrier prevents battery stack common mode voltage from corrupting output referred measurement results. This approach works quite well but, requiring an isolation amplifier per cell, is complex and quite expensive. Some simplification is possible; e.g., a single power driver servicing many amplifiers, but the method remains costly and involved.

Figure A3 employs a switched capacitor technique to measure individual cell voltage while rejecting common mode voltage. The clocked switches alternately connect the capacitor across its associated cell and discharge it into an output common referred capacitor.⁵ After a number of such cycles the output capacitor assumes the cell voltage. A buffer amplifier provides the output. This arrangement rejects common mode voltages but requires many expensive high voltage switches, a high voltage level shift and nonoverlapping switch drive. More subtly, switch leakage degrades accuracy, particularly as temperature

⁴See reference 5 for details on isolation amplifiers.

⁵Old timers amongst the readership will recognize this configuration as a derivative of the venerable reed switched “flying capacitor” multiplexer.

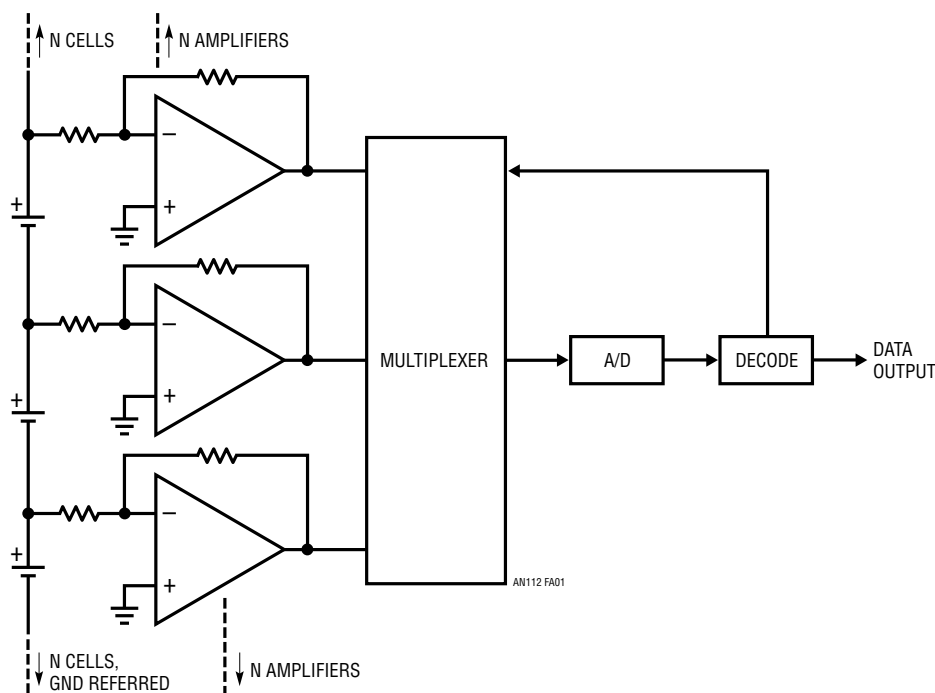


Figure A1. Unworkable Scheme Suppresses High Common Voltages by Converting Cell Potentials to Current. Circuit Decodes Amplifier Outputs to Derive Individual Cell Voltages. Required Resistor Precision and Values are Unrealistic. Resistors Draw Current from Cells

an112f

Application Note 112

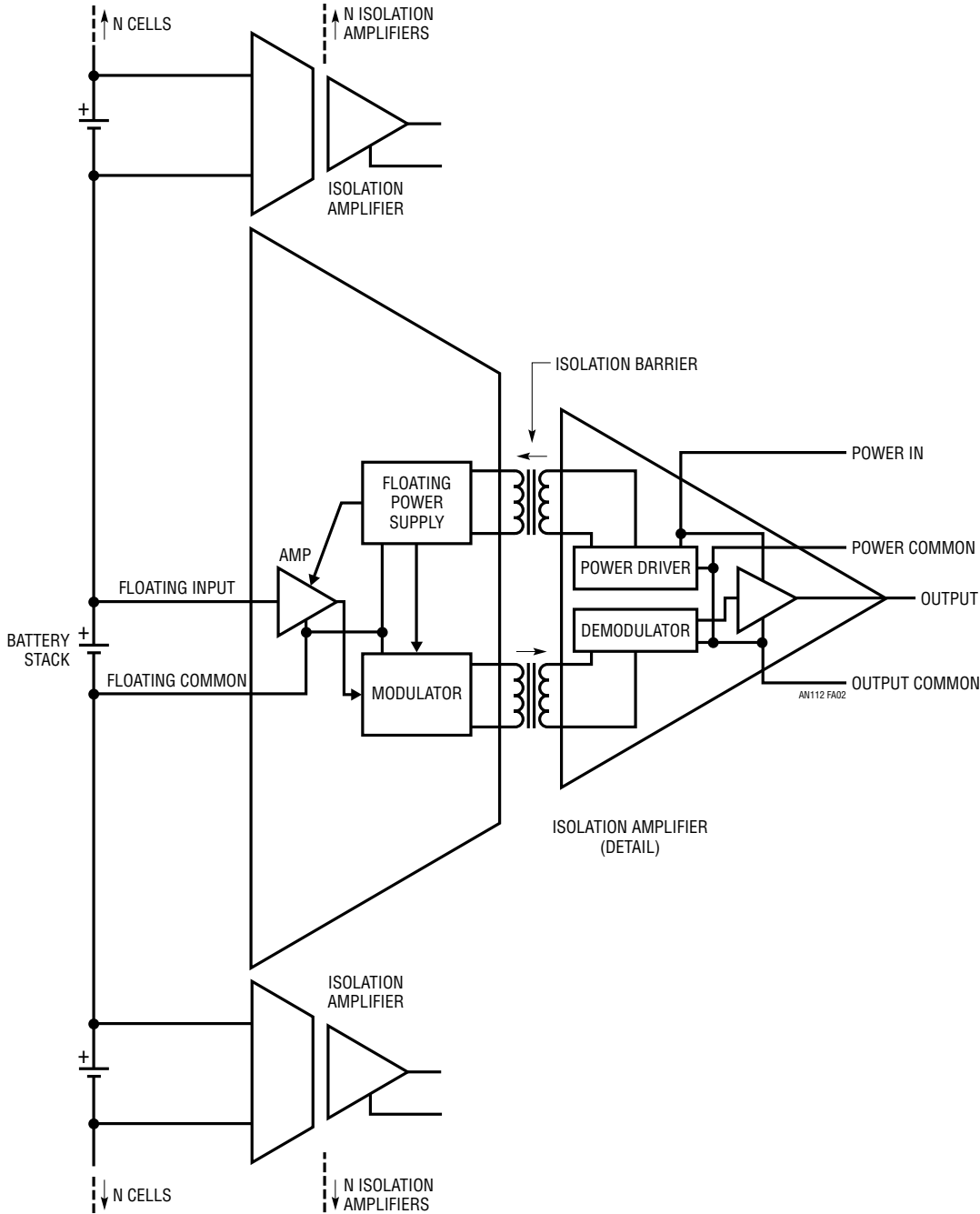


Figure A2. Isolation Amplifier's Galvanically Floating Input Eliminates Common Mode Voltage Effects. Approach Works, but is Complex and Expensive Requiring Isolation Amplifier per Cell

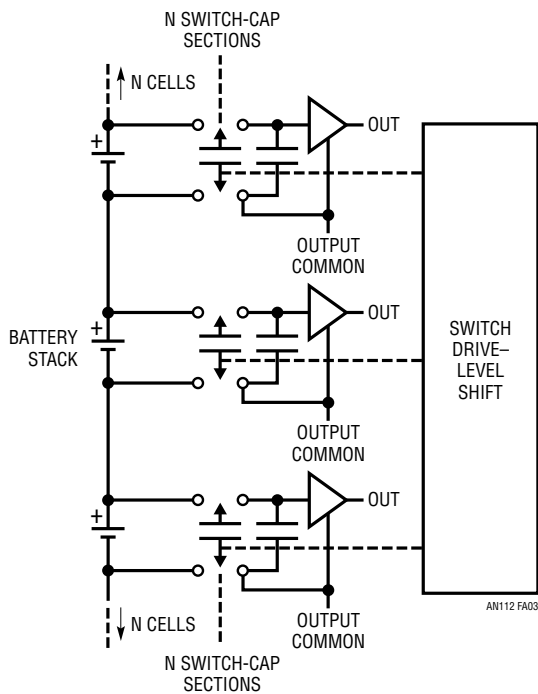


Figure A3. Switched Capacitor Scheme Rejects Common Mode Voltage but Requires High Voltage Switches, Nonoverlapping Drive and Level Shift. Switch Leakage Degrades Accuracy. Optically Driven Switches Can Simplify Level Shift but Breakdown and Leakage Issues Remain

risers. Optically driven switches, particularly those available as conveniently packaged LED driven MOSFETS, can simplify the level shift but expense, voltage breakdown and leakage concerns remain⁶.

Switch related disadvantages are eliminated by Figure A4's approach. Each cell's potential is digitized by a dedicated A/D converter. A/D output is transmitted across an isolation barrier via a data isolator (optical, transformer). In its most elementary form, each A/D is powered by a separate, isolated power supply. This isolated supply population is reducible, but cannot be eliminated. Constraints include cell voltage and the A/D's maximum permissible supply and input common mode voltages. Within these limitations, several A/D channels are serviceable by one isolated supply. Further refinement is possible through employment of multiplexed input A/Ds. Even with these improvements, numerous isolated supplies are still mandated by large battery stacks. Although this scheme is technologically sound, it is complex and expensive.

⁶An optically coupled variant of this approach is given in Reference 6.

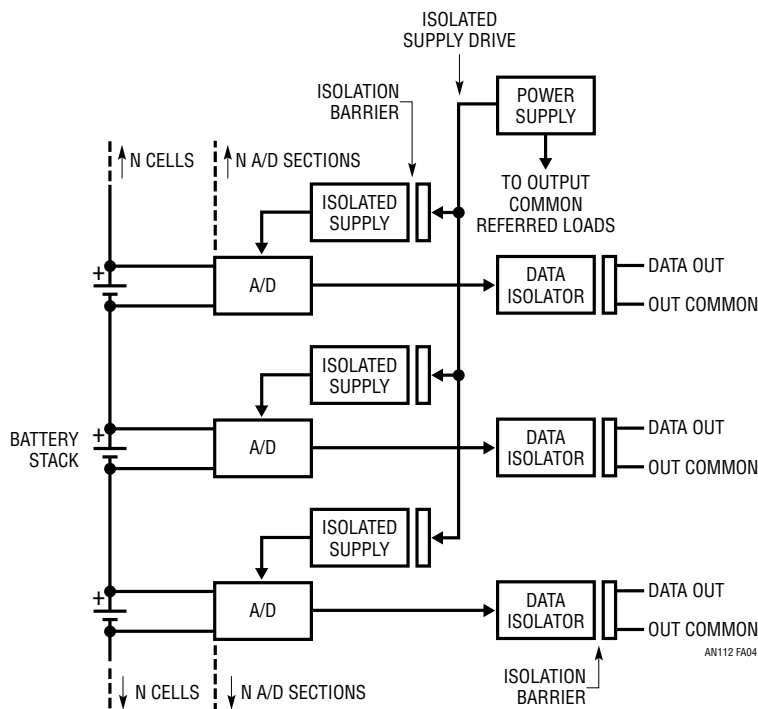


Figure A4. A/D per Cell Requires Isolated Supplies and Data Isolators. Multiplexed Input A/Ds can Minimize A/D Usage. Isolated Supply Population is Reducible, but Cannot be Eliminated

Application Note 112

APPENDIX B

A Floating Output, Variable Potential Battery Simulator

Battery stack voltage monitor development is aided by a floating, variable potential battery simulator. This capability permits accuracy verification over a wide range of battery voltage. The floating battery simulator is substituted for a cell in the stack and any desired voltage directly dialed out. Figure B1's circuit is simply a battery-powered follower (A1) with current boosted (A2) output. The LT1021 reference and high resolution potentiometric divider specified permits accurate output settling within 1mV. The composite amplifier unloads the divider and drives a 680 μ F capacitor to approximate a battery. Diodes preclude reverse biasing

the output capacitor during supply sequencing and the 1 μ F-150k combination provides stable loop compensation. Figure B2 depicts loop response to an input step; no overshoot or untoward dynamics occur despite A2's huge capacitive load. Figure B3 shows battery simulator response (trace B) to trace A's transformer clamp pulse. Closed-loop control and the 680 μ F capacitor limit simulator output excursion within 30 μ V. This error is so small that noise averaging techniques and a high gain oscilloscope preamplifier are required to resolve it.

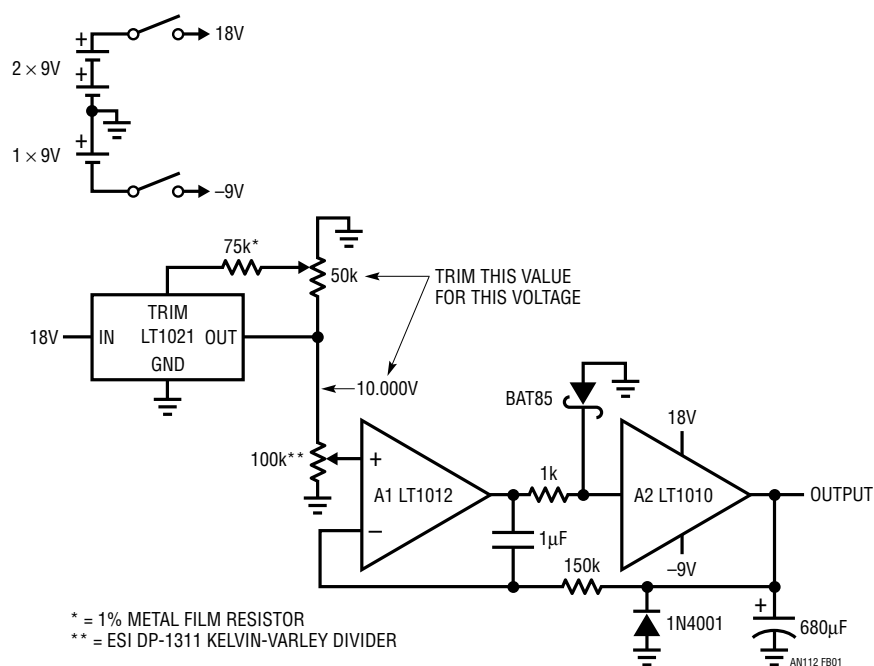


Figure B1. Battery Simulator Has Floating Output Settable Within 1mV. A1 Unloads Kelvin-Varley Divider; A2 Buffers Capacitive Load

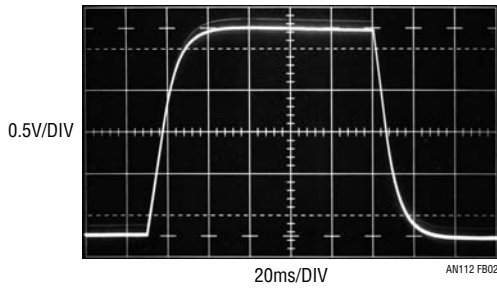


Figure 2B. 150k-1 μ F Compensation Network Provides Clean Response Despite 680 μ F Output Capacitor

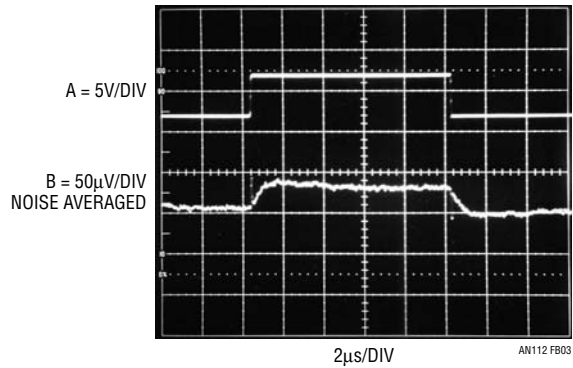


Figure 3B. Battery Simulator Output (Trace B) Responds to Trace A's Transformer Clamp Pulse. Closed-Loop Control and 680 μ F Capacitor Maintain Simulator Output Within 30 μ V. Noise Averaged, 50 μ V/Division Sensitivity is Required to Resolve Response

APPENDIX C

Microcontroller Code Listing

The microcontroller code consists of three files:

Battery_monitor.c contains the main program loop, including calibration and temperature correction, and support functions.

Interrupts.c is the code for the timer2 interrupt that drives the transformer excitation and controls the LTC1867 ADC.

Battery_monitor.h contains various defines, global variable declarations and function prototypes.

Application Note 112

```
/*  
battery_monitor.c
```

Six Channel Battery Monitor with continuous gain and offset correction. Includes a "factory calibration" feature. On first power up, apply zero volts to all inputs, allow data to settle, and type 'o'.

Next apply 1.25V to all inputs, allow data to settle, and type 'p'.

This calibrates the circuit, and it is ready to run.

Offset correction technique:

Present offset correction = init_offset[7] - voltage[7]
Hotter = less counts on voltage[7] so correction goes POSITIVE,
so ADD this to voltage[i]

```
voltage[i] = voltage[i] - init_offset[i] + present_offset
```

Slope correction Technique:

Initial slope = init_fs[6] - init_offset[7] counts per 1.25V
Present slope = voltage[6] - voltage[7] counts per 1.25V

Keyboard command summary:

```
'a': increment conversion period (default is 1ms)  
'z': decrement conversion period  
's': increment by 10  
'x': decrement by 10  
'd': increment pulse-convert delay (default is 2us)  
'c': decrement pulse-convert delay  
'f': increment pulse-convert delay by 10  
'v': decrement pulse-convert delay by 10  
'n': Calculate voltages for display  
'm': Display raw ADC values  
't': Echo text to terminal so you can insert comments into  
      data that is being captured. Terminate with '!'  
'k': Disable digital filter  
'l': Enable digital filter  
'o': Store offsets to nonvolatile memory  
'p': Store full-scale readings to nonvolatile memory
```

Written for CCS Compiler Version 3.242

Mark Thoren

Linear Technology Corporation

January 15, 2007

```
*****
```

```
#include "battery_monitor.h"  
#include "interrupts.c"
```

```
void main(void)  
{  
    int8 i;  
    unsigned int16 adccode;  
    float temp=0.0, offset_correction, slope, slope_correction;  
  
    initialize();           // Initialize hardware  
    rx_usb();              // Wait until any character is received  
    print_cal_constants(); // display calibration constants before starting.  
  
    while(1)  
    {  
        if(usb_hit()) parse(); // get keyboard command if necessary  
        for(i=0; i<=7; ++i) // Read raw data first  
        {  
            readflag[i] = 1; // Tell interrupt that we're reading!!  
        }  
    }  
}
```

an112f

```

adccode = data[i];
readflag[i] = 0;
temp = (float) adccode; // convert to floating point
if(filter) // Simple exponential IIR filter
{
    voltage[i] = 0.9 * voltage[i];
    voltage[i] += 0.1* temp;
}
else
{
    voltage[i] = temp;
}
}

if(calculate) // Display temperature corrected voltages
{
    // Calculate Corrections.
    // offset correction is stored CH7 reading minus the present reading
    offset_correction = read_offset_cal(7) - voltage[7];
    // Slope correction is the stored slope based on initial CH6 and CH7
    // readings divided by the present slope. Units are (dimensionless)
    slope_correction = (float) read_fs_cal(6) -
        (float) read_offset_cal(7); // Initial counts/1.25V
    slope_correction = slope_correction / (voltage[6] - voltage[7]);

    for(i=0; i<=5; ++i) // Print Measurement Channels
    {
        // Units on slope are "volts per ADC count"
        slope = 1.25000 / ((float) read_fs_cal(i) - // Inefficient but
            (float) read_offset_cal(i)); // we are RAM limited
        // Correct for initial offset and temperature dependent offset.
        // units on temp are "ADC counts"
        temp = voltage[i] - (float) read_offset_cal(i) + offset_correction;
        // Correct for initial slope
        temp = temp * slope;
        // Units on temp is now "volts"
        // Correct for temperature dependent slope
        temp = temp * slope_correction;
        busbusy = 1;
        printf(tx_usb, "%1.5f, ", temp);
        busbusy = 0;
    }
    busbusy = 1; // Print to terminal
    printf(tx_usb, "%1.6f, %1.1f, ", slope_correction, offset_correction);
    busbusy = 0;
}

else // Display raw ADC counts
{
    for(i=0; i<=7; ++i)
    {
        busbusy = 1; // Print to terminal
        printf(tx_usb, "%1.0f, ", voltage[i]);
        busbusy = 0;
    }
}

busbusy = 1;
printf(tx_usb, "D:%d, P:%d\r\n", delay, period); // print period and delay
busbusy = 0;
// Delay and blink light
delay_ms(100); output_high(PIN_C0); delay_ms(100); output_low(PIN_C0);
} //end of loop
} //end of main

```

Application Note 112

```

/*****
Parse keyboard commands
arguments: none
returns: void
*****/

void parse(void)
{
    char ch;
    switch(rx_usb())
    {
        case 'a': period += 1; break;    // increment period
        case 'z': period -= 1; break;    // decrement period
        case 's': period += 10; break;   // increment by 10
        case 'x': period -= 10; break;   // decrement by 10
        case 'd': delay += 1; break;     // increment pulse-convert delay
        case 'c': delay -= 1; break;     // decrement pulse-convert delay
        case 'f': delay += 10; break;    //      "      by 10
        case 'v': delay -= 10; break;    //      "      by 10
        case 'n': calculate = 1; break;  // Calculate voltages
        case 'm': calculate = 0; break;  // Display raw values
        case 't': // Echoes text to terminal so you can insert comments into
            { // data that is being captured. Terminate with '\!'
                busbusy = 1;
                printf(tx_usb, "enter comment\r\n");
                while((ch=rx_usb())!='\!') tx_usb(ch);
                tx_usb('\r');
                tx_usb('\n');
                busbusy = 0;
            } break;
        case 'k': filter = 0; break;     // Disable filter
        case 'l': filter = 1; break;     // Enable Filter
        case 'o': write_offset_cal(); break; // Store offset to nonvolatile mem.
        case 'p': write_fs_cal(); break; // Store FS to nonvolatile mem.
    }
    setup_timer_2(T2_DIV_BY_16,period,8); // Update period if necessary
}

/*****
write offset and full-scale calibration constants to non-volatile memory
arguments: none
returns: void
*****/
void write_offset_cal(void)
{
    int i;
    unsigned int16 intvoltage;
    for(i=0; i<=7; ++i)
    {
        intvoltage = (unsigned int16) voltage[i]; // Cast as unsigned int16
        write_eeprom (init_offset_base+(2*i), intvoltage >> 8); // Write high byte
        delay_ms(20);
        write_eeprom (init_offset_base+(2*i)+1, intvoltage); // Write low byte
        delay_ms(20);
    }
}

void write_fs_cal(void)
{
    int i;
    unsigned int16 intvoltage;
    for(i=0; i<=7; ++i)
    {

```

```

    intvoltage = (unsigned int16) voltage[i];    // Cast as unsigned int16
    write_eeprom (init_fs_base+(2*i), intvoltage >> 8); // Write high byte
    delay_ms(20);
    write_eeprom (init_fs_base+(2*i)+1, intvoltage); // Write low byte
    delay_ms(20);
}

/*****
read offset and full-scale calibration constants from non-volatile memory
arguments: none
returns: void
*****/
unsigned int16 read_offset_cal(int channel)
{
    return make16(read_eeprom(init_offset_base+(2*channel)),
                 read_eeprom(init_offset_base+(2*channel)+1));
}

unsigned int16 read_fs_cal(int channel)
{
    return make16(read_eeprom(init_fs_base+(2*channel)),
                 read_eeprom(init_fs_base+(2*channel)+1));
}

/*****
Print calibration constants (raw ADC counts)
arguments: none
returns: void
*****/
void print_cal_constants(void)
{
    int i;
    for(i=0; i<=7; ++i)
    {
        printf(tx_usb, "ch%d offset: %05Lu, fs: %05Lu\r\n",
              i, read_offset_cal(i), read_fs_cal(i));
    }
}

/*****
Interface to the FT24BM USB controller

usb_hit() arguments: none returns: 1 if data is ready to read, zero otherwise
rx_usb() arguments: none returns: character from USB controller
tx_usb() arguments: data to send to PC, returns: void
*****/
char usb_hit(void)
{
    return !input(RXF_);
}

char rx_usb(void)
{
    char buf;
    while(input(RXF_)) {} // Low when data is available, wait around
    output_low(RD_);
    delay_cycles(1);
    buf=input_d();
    output_high(RD_);
    return(buf);
}

```

Application Note 112

```
void tx_usb(int8 value)
{
    while(input(TXE_)) //Low when FULL, wait around
    {
    }
    output_d(value);
    output_high(WR);
    delay_cycles(1);
    output_low(WR);
    input_d();
}

/*****
Hardware initialization
arguments: none
returns: void
*****/
void initialize(void)
{
    output_high(ISO_PWR_SD_); //turn on power
    setup_adc_ports(NO_ANALOGS);
    setup_adc(ADC_OFF);
    setup_psp(PSP_DISABLED);
    setup_spi(SPI_CONFIG);
    CKP = 0; // Set up clock edges - clock idles low, data changes on
    CKE = 1; // falling edges, valid on rising edges.
    output_low(I2C_SPI_);
    output_low(AUX_MAIN_); // SPI is only MAIN
    setup_counters(RTCC_INTERNAL, RTCC_DIV_1);
    setup_timer_0(RTCC_INTERNAL|RTCC_DIV_1);
    setup_timer_1(T1_DISABLED);
    setup_timer_2(T2_DIV_BY_16, period, 8);
    setup_comparator(NC_NC_NC_NC);
    setup_vref(FALSE);

    output_low(PIN_C0);
    delay_ms(100);
    output_high(PIN_C0); // Turn off LEDs
    output_high(PIN_C1);
    output_high(PIN_C2);

// I/O Initialization
input(RXF_);
input(TXE_);
output_high(RD_);
output_low(WR);
delay_ms(100);
output_low(CS);
delay_us(5);
output_high(CS);
// Turn on interrupts (only one)
enable_interrupts(INT_TIMER2);
enable_interrupts(GLOBAL);
}
```

```

/*****
Timer 2 Interrupt
This interrupt service routine does all of the work of controlling transformer
excitation and controlling the LTC1867.
*****/
#include TIMER2 // Tell compiler that this is the Timer 2 ISR
TIMER2_isr()
{
    static int8 ledstatus;
    int8 j, highbyte, lowbyte;
    if(++ledstatus == 0x80) output_low(LED); // Blink light every 256 calls
    if(ledstatus == 0x00) output_high(LED);

    if(!busy) // If main() is using the bus, do nothing.
    {
        for(j=0; j<=7; ++j)
        {
            output_d(LATCHWORD[j]);
            output_high(LATCH);
            output_low(LATCH);
            output_low(CS);
            highbyte = spi_read(LTC1867CONFIG[j]);
            output_high(EXCITATION);
            delay_us(delay);
            lowbyte = spi_read(0);

            output_high(CS);
            output_low(EXCITATION);

            if(!readflag[j]) data[j] = make16(highbyte, lowbyte); // Don't write if main() is reading!!
            // This is a simple anti-collision technique. The worst
            // case latency is a single reading, or 1ms.

        } //end of for loop
    } //end of if(!busy)
} // end of ISR

```

Application Note 112

```
/*
battery_monitor.h
defines, global variables, function prototypes
*/

#include <16F877A.h> // Standard header
#define adc=8
#define delay(clock=2000000) // Clock frequency is 20MHz
#define rs232(baud=9600,parity=N,xmit=PIN_C6,rcv=PIN_C7,bits=9)
#define SPI_CONFIG SPI_MASTER|SPI_L_TO_H|SPI_CLK_DIV_4 // 5MHz SPI clk when
// master clk = 20MHz

// #fuses NOWDT,RC,NOPUT,NOPROTECT,NODEBUG,BROWNOUT,LVP,NOCPLD,NOWRT
// This is less confusing - set up configuration word with #rom statement
// Bit 13 12 11 10 9 8 7 6 5 4 3 2 1 0
// Function CP -- DEBUG WRT1 WRT0 CPD LVP BOREN -- PWRTEN# WDTEN FOSC1 FOSCO
//
#define rom 0x2007 = {0x3F3A}

// Battery Monitor Project Defines //

// Global variables
int16 data[8]; // Raw data from the LTC1867
int8 readflag[8]; // Tells ISR that main is reading data, do not write
int1 busbusy = 0; // Tells ISR that main is talking on the bus
int1 calculate = 1; // Send calculated voltages to terminal when asserted
int1 filter = 1; // Enables digital filter when asserted
unsigned int8 period = 40; // Period between reads
unsigned int8 delay = 2; // Additional settling time after applying excitation
float voltage[8]; // Holds floating point calculated voltages

// Non-volatile memory base addresses for calibration constants
#define init_offset_base 0
#define init_fs_base 16

// First, define the SDI words to be sent to the LTC1867
// All are Single ended, unipolar, 4.096V range.
#define LTC1867CH0 0x84
#define LTC1867CH1 0xC4
#define LTC1867CH2 0x94
#define LTC1867CH3 0xD4
#define LTC1867CH4 0xA4
#define LTC1867CH5 0xE4
#define LTC1867CH6 0xB4
#define LTC1867CH7 0xF4

// Excitation enable lines. Write this to the '574 register
// before enabling excitation pulse.
#define EXC0 0x01
#define EXC1 0x02
#define EXC2 0x04
#define EXC3 0x08
#define EXC4 0x10
#define EXC5 0x20
#define EXC6 0x40
#define EXC7 0x80
```



```
// Now define two lookup tables such that the excitation signal lines up with
// the selected LTC1867 input.
byte CONST LTC1867CONFIG [8] = {LTC1867CH1, LTC1867CH2, LTC1867CH3, LTC1867CH4,
                                LTC1867CH5, LTC1867CH6, LTC1867CH7, LTC1867CH0};
byte CONST LATCHWORD [8] = {EXC6, EXC5, EXC4, EXC3, EXC2, EXC1, EXC0, EXC7};

//Pin Definitions
#define EXCITATION    PIN_B0    // Enables excitation to the selected channel
#define LATCH         PIN_B1    // 74HC573 latch pin
#define LED           PIN_C1    // Spare blinky light

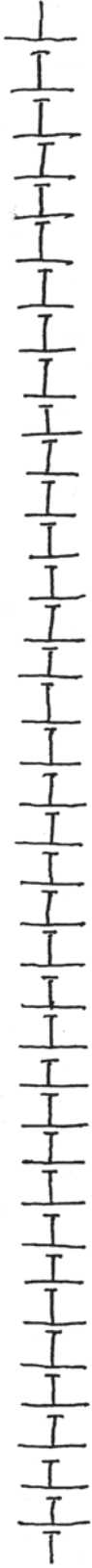
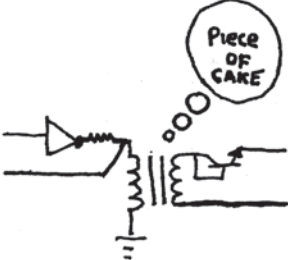
#define RD_           PIN_A0
#define RXF_          PIN_A1
#define WR_           PIN_A2
#define TXE_          PIN_A3
#define ISO_PWR_SD_  PIN_A4
#define LCD_EN_      PIN_A5
#define CS_           PIN_B5

#define AUX_MAIN_    PIN_E1
#define I2C_SPI_     PIN_E2

#define SSPCON       = 0x14
#define SSPSTAT      = 0x94
#define CKP          = SSPCON.4
#define CKE          = SSPSTAT.6

// Function Prototypes
void parse(void);
void write_offset_cal(void);
void write_fs_cal(void);
unsigned int16 read_offset_cal(int channel);
unsigned int16 read_fs_cal(int channel);
void print_cal_constants(void);
char usb_hit(void);
void initialize(void);
void tx_usb(int8 value);
char rx_usb(void);
```

Application Note 112



— Willw '07

Power Conversion, Measurement and Pulse Circuits

Tales From the Laboratory Notebook, 2005-2007

Jim Williams

INTRODUCTION

This ink marks LTC's eighth circuit collection publication.¹ We are continually surprised, to the point of near mystification, by these circuit amalgams seemingly limitless appeal. Reader requests ascend rapidly upon publication, remaining high for years, even decades. All LTC circuit collections, despite diverse content, share this popularity, although just why remains an open question. Why is it? Perhaps the form; compact, complete, succinct and insular. Perhaps the freedom of selection without commitment, akin to window shopping. Or, perhaps, simply the pleasure of new recruits for the circuit aficionados intellectual palate. Locally based electrosociologists, spinning elegantly contrived theories, offer explanation, but no convincing evidence is at hand. What is certain is that readers are attracted to these compendiums and that calls us to attention. As such, in accordance with our mission to serve customer preferences, this latest collection is presented. Enjoy.

JFET-Based DC/DC Converter Powered From 300mV Supply

A JFET's self-biasing characteristic can be utilized to construct a DC/DC converter powered from as little as 300mV. Solar cells, thermopiles and single-stage fuel cells,

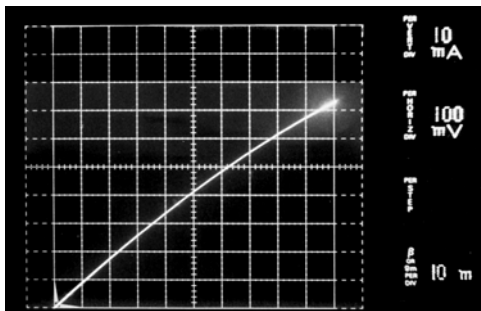


Figure 1. Zero Volt. Biased JFET I-V Curve Shows 10mA Conduction at 100mV, Rising Above 40mA at 500mV. Characteristic Permits DC/DC Converter Powered From 300mV Supply.

all with outputs below 600mV, are typical power sources for such a converter.

Figure 1, an N-channel JFET I-V plot, shows drain-source conduction under zero bias (gate and source tied together) conditions. This property can be exploited to produce a self-starting DC/DC converter that runs from 0.3V to 1.6V inputs.

Figure 2 shows the circuit. Q1 and T1 form an oscillator with T1's secondary providing regenerative feedback to Q1's gate. When power is applied, Q1's gate is at zero volts and its drain conducts current via T1's primary. T1's phase inverting secondary responds by going negative at Q1's gate, turning it off. T1's primary current ceases, its secondary collapses and oscillation commences. T1's primary action causes positive going "flyback" events at Q1's drain, which are rectified and filtered. Q2's $\approx 2V$

Note 1. Previous efforts include References 4, 6, 7 and 23-26.

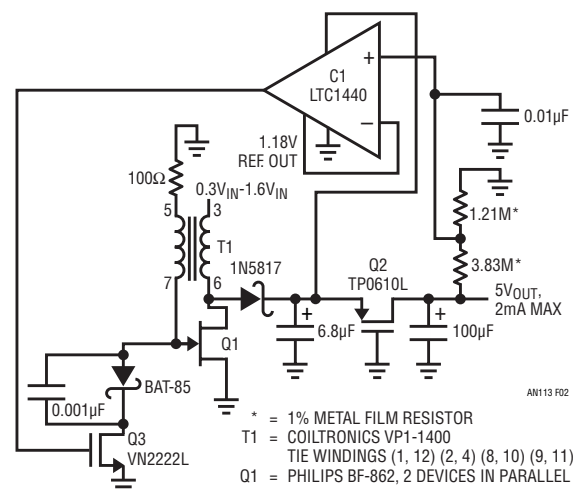


Figure 2. JFET-Based DC/DC Converter Runs From 300 Millivolt Input. Q1-T1 Oscillator Output Is Rectified and Filtered. Load Is Isolated Until Q2 Source Reaches $\approx 2V$, Aiding Start-Up. Comparator and Q3 Close Loop Around Oscillator, Controlling Q1's On-Time to Stabilize 5V Output.

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Application Note 113

turn-on potential isolates the load, aiding start-up. When Q2 turns on, circuit output heads towards 5V. C1, powered from Q2's source, enforces output regulation by comparing a portion of the output with its internal voltage reference. C1's switched output controls Q1's on-time via Q3, forming a control loop.

Waveforms for the circuit include the AC coupled output (Figure 3, trace A), C1's output (trace B) and Q1's drain flyback events (trace C). When the output drops below 5V, C1 goes low, turning on Q1. Q1's resultant flyback events continue until the 5V output is restored. This pattern repeats, maintaining the output.

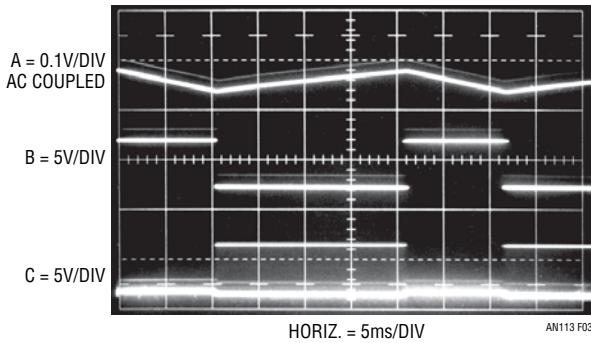


Figure 3. JFET-based Converter Waveforms. When Supply Output (Trace A) Decays, C1 (Trace B) Switches, Allowing Q1 to Oscillate. Resultant Flyback Events at Q1 Drain (Trace C) Restore Supply Output.

The 5V output can supply up to 2mA, sufficient to power circuitry or furnish bias to a higher power switching regulator when larger current is required. The circuit will start into loads of 300 μ A at 300mV input; 2mA loading requires a 475mV supply. Figure 4 plots minimum input voltage versus output current over a range of loads.

Q3's shunt control of Q1 is simple and effective, but results in 25mA quiescent current drain. Figure 5's modifications reduce this figure to 1mA by series switching T1's secondary. Here, Q3 switches series connected Q4, more efficiently controlling Q1's gate drive. Negative turn-off

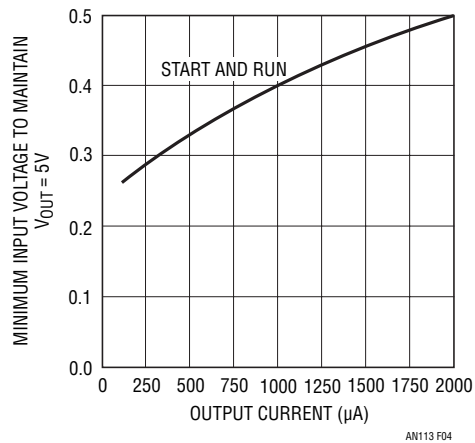


Figure 4. JFET-Based DC/DC Converter Starts and Runs into 100 μ A Load at $V_{IN} = 275$ mV. Regulation to 2mA Is Possible, Although Required V_{IN} Rises to 500mV.

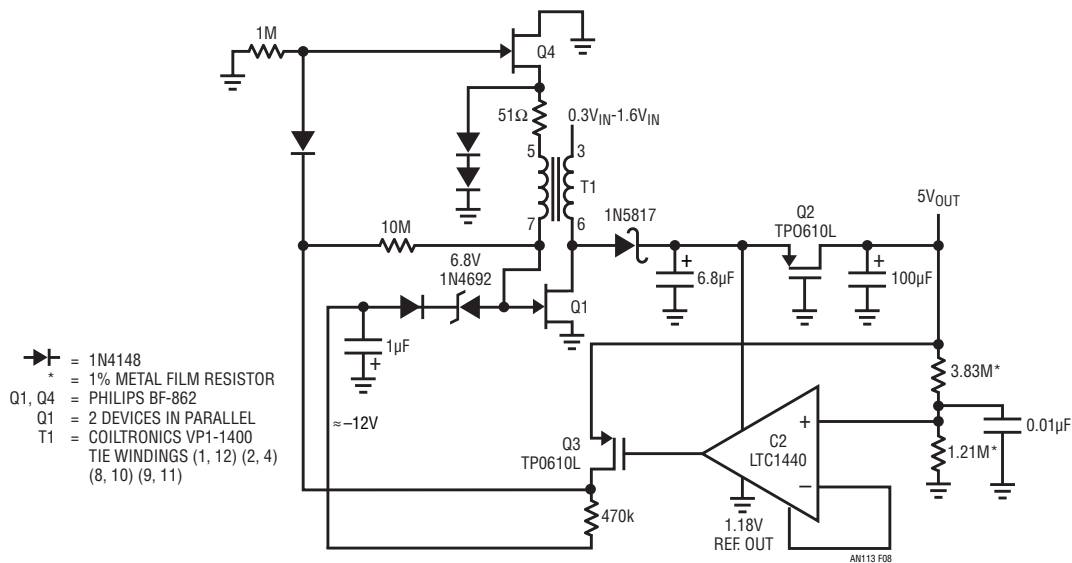


Figure 5. Adding Q3, Q4 and Bootstrapped Negative Bias Generator Reduces Quiescent Current. Comparator Directed Q3 Switches Q4, More Efficiently Controlling Q1's Gate Drive. Q2 and Zener Diode Isolate All Loading During Q1 Start-Up.

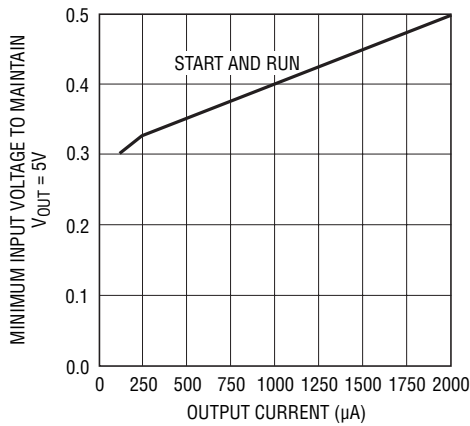
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bias for Q4 and Q1 is bootstrapped from T1's secondary; the 6.8V zener holds off bias supply loading during initial power application, aiding start-up. Figure 6's plot of minimum input voltage versus output current shows minimal penalty (versus Figure 4's data) imposed by the added quiescent current control circuitry.

Bipolar Transistor-Based 550mV Input DC/DC Converter

Bipolar transistors may be used to obtain higher output currents, although their V_{BE} drop raises input supply re-

quirements to 550mV. Figure 7's curve tracer plot shows base-emitter conduction just beginning at 450mV (25°C) with substantial current flow beyond 500mV. Figure 8's circuit operates similarly to FET-based Figure 2, although the bipolar transistor's normally off characteristic allows more efficient operation. Figure 9's operating waveforms are similar to Figure 3, except the comparator's output state is reversed to accommodate the bipolar transistor. Figure 10's start-run curves show 6mA output current at 550mV input—3 times the FET circuit's capacity. The "run" curve



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Figure 6. Start/Run Curve for Low Quiescent Current JFET-Based DC/DC Converter. Quiescent Current Control Circuitry Slightly Increases Input Voltage Required to Support Load.

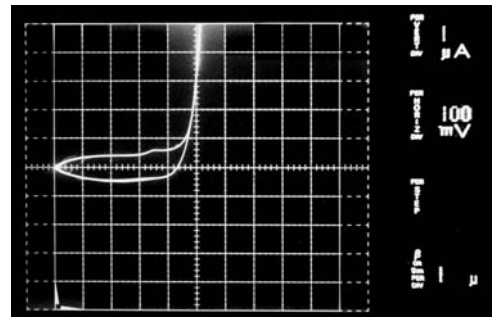


Figure 7. Bipolar Transistor Base Emitter Junction I-V Curve Shows Conduction Beginning at 450 Millivolts (25°C). Characteristic Forms Basis of DC/DC Converter Powered From 550 Millivolts.

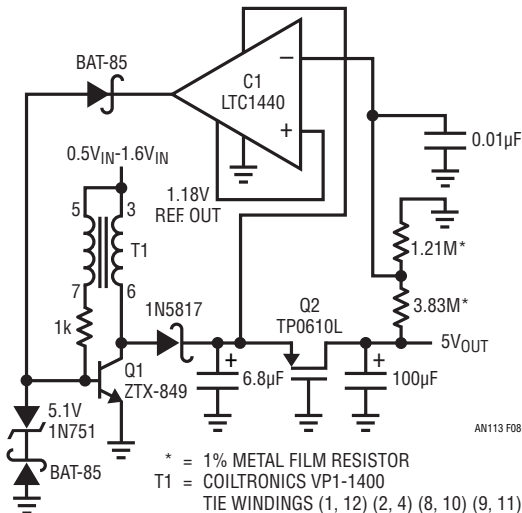
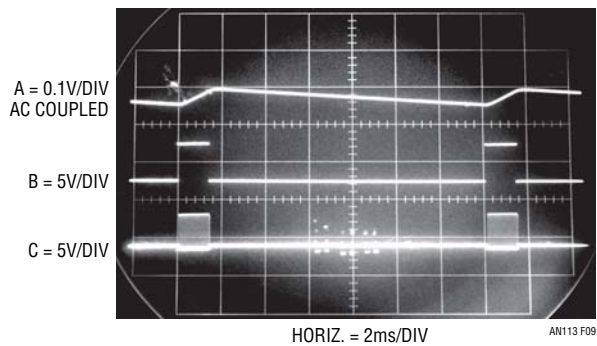


Figure 8. Bipolar Transistor-Based DC/DC Converter Runs From 500 Millivolt (25°C) Input. Q1-T1 Oscillator Output is Rectified and Filtered. Load is Isolated Until Q2's Source Reaches ≈2V, Aiding Start-Up. Comparator Closes Loop Around Oscillator, Controlling Q1's On-Time to Stabilize 5V Output.



AN113 F09

Figure 9. Converter Waveforms. When Output (Trace A) Decays, C1 (Trace B) Switches, Allowing Q1 to Oscillate. Resultant Flyback Events at Q1 Collector (Trace C) Restore Output.

Application Note 113

indicates that, once started, the circuit will run at input voltages as low as 300mV depending on loading.

When considering these circuits' extremely low input voltages and output power limits it is worth noting that the transformer specified is a standard product. A transformer specifically optimized for these applications would likely enhance performance.

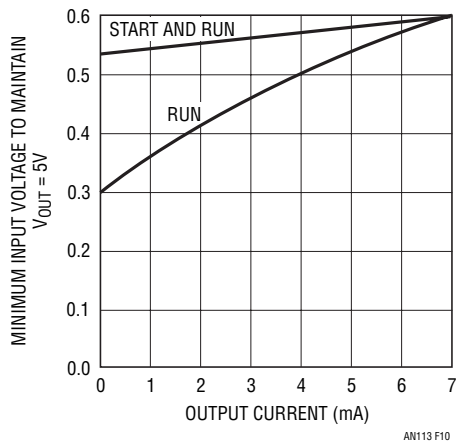


Figure 10. Bipolar Transistor-Based DC/DC Converter Requires $\approx 550\text{mV}$ (25°C) Input to Start into 0mA to 6mA Loading. Once Running, Converter Maintains Regulation Down to 300mV Inputs for $100\mu\text{A}$ Load.

5V to 200V Converter for APD Bias

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Avalanche photodiodes (APD) require high voltage bias. Figure 11's design provides 200V from a 5V input. The circuit is a basic inductor flyback boost regulator with a major important deviation. Q1, a high voltage device, has been interposed between the LT1172 switching regulator and the inductor. This permits the regulator to control Q1's high voltage switching without undergoing high voltage stress. Q1, operating as a "cascode" with the LT1172's internal switch, withstands L1's high voltage flyback events.² Diodes associated with Q1's source terminal clamp L1 originated spikes arriving via Q1's junction capacitance. The

Note 2. See References 1 (page 8), 2 (Appendix D), and 3.

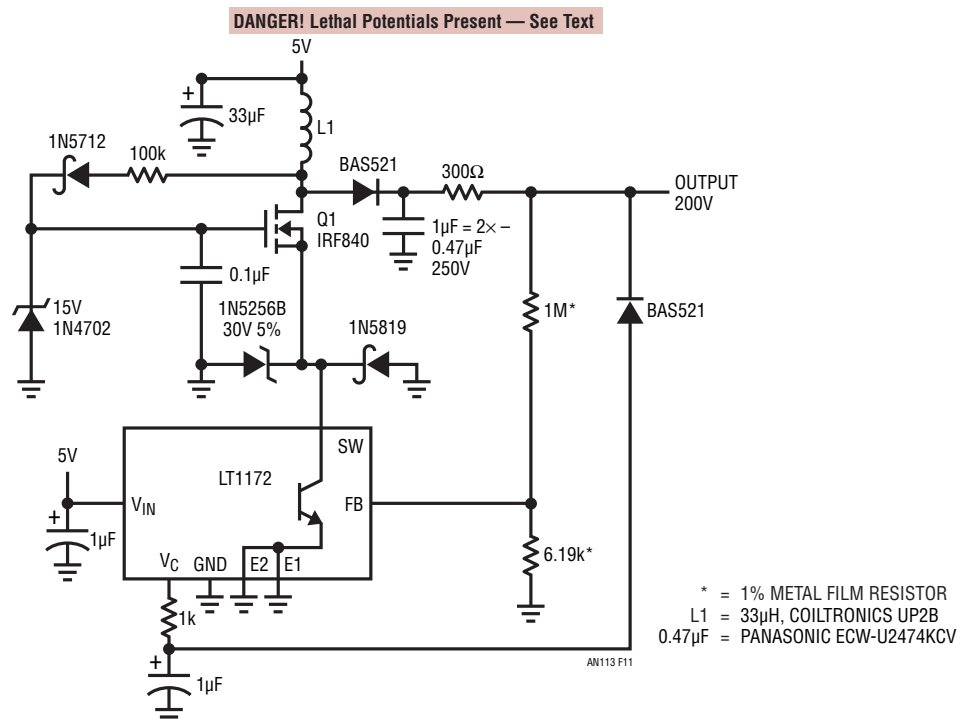


Figure 11. 5V to 200V Output Converter for APD Bias. Cascoded Q1 Switches High Voltage, Allowing Low Voltage Regulator to Control Output. Diode Clamps Protect Regulator from Transient Events; 100k Path Bootstraps Q1's Gate Drive from L1's Flyback Events. Output Connected 300Ω-Diode Combination Provides Short-Circuit Protection.

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high voltage is rectified and filtered, forming the circuit's output. Feedback to the regulator stabilizes the loop and the RC at the V_C pin provides frequency compensation. The 100k path from L1 bootstraps Q1's gate drive to about 10V, ensuring saturation.³ The output connected 300 Ω -diode combination provides short-circuit protection by shutting down the LT1172 if the output is accidentally grounded.

Figure 12 shows operating waveforms. Traces A and C are LT1172 switch current and voltage, respectively. Q1's drain is trace B. Current ramp termination results in a high voltage flyback event at Q1's drain. A safely attenuated version of the flyback appears at the LT1172 switch. The sinusoidal signature, due to inductor ring-off between conduction cycles, is harmless.

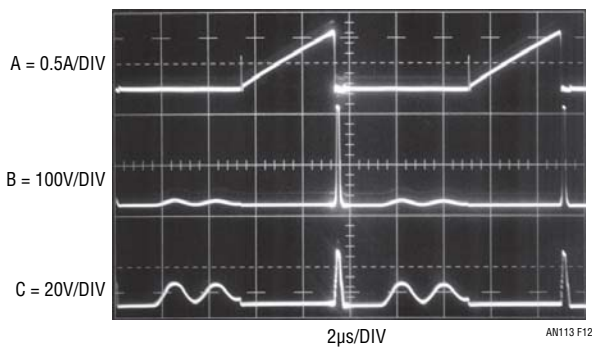


Figure 12. Waveforms for 5V to 200V Converter Include LT1172 Switch Current and Voltage (Traces A and C, Respectively) and Q1's Drain Voltage (Trace B). Current Ramp Termination Results in High Voltage Flyback Event at Q1 Drain. Safely Attenuated Version Appears at LT1172 Switch. Sinusoidal Signature, Due to Inductor Ring-Off Between Current Conduction Cycles, is Harmless. All Traces Intensified Near Center Screen for Photographic Clarity.

Battery Internal Resistance Meter

It is often desirable to determine a battery's internal resistance to evaluate its condition or suitability for an application. Accurate battery resistance determination is complicated by inherent capacitive terms which corrupt results taken with AC-based milliohmmeters operating in the kHz range. Figure 13, a very simplistic battery model, shows a resistive divider with a partial shunt capacitive term. This capacitive term introduces error in AC-based measurement. Additionally, the battery's unloaded internal resistance may significantly differ from its loaded value. As such, a realistic determination of internal resistance must be made under loaded conditions at or near DC.

Note 3. This circuit is not a fresh contribution but, rather, a belated *mea culpa*. The original version suffered temperature dependent output error due to its gate bias bootstrap scheme. See Reference 4.

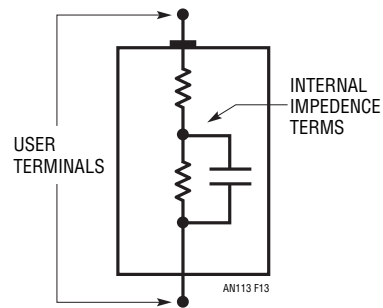


Figure 13. Simplistic Model Shows Battery Impedance Terms Including Resistive and Capacitive Elements. Capacitive Component Corrupts AC-Based Measurement Attempts to Determine Internal DC Resistance. More Realistic Results Occur if Battery Voltage Drop Is Measured Under Known Load.

Application Note 113

Figure 14's circuit meets these requirements, permitting accurate internal resistance determination of batteries up to 13V over a range of 0.001Ω to 1.000Ω. A1, Q1 and associated components form a closed loop current sink which loads the battery via Q1's drain. The 1N5821 provides reverse battery protection. The voltage across the 0.1Ω resistor, and hence the battery load, is determined by A1's "+" input voltage. This potential is alternately switched, via S1, between 0.110V and 0.010V derived from the 2.5V reference driven resistor string. S1's 0.5Hz square wave switching drive comes from the CD4040 frequency

divider. The result of this action is a 100mA biased 1A 0.5Hz square wave load applied to the battery. The battery's internal resistance causes a 0.5Hz amplitude modulated square wave to appear at the Kelvin-sensed S2-S3-A2 synchronous demodulator. The demodulator DC output is buffered by chopper stabilized A2 which provides the circuit output. A2's internal 1kHz clock, level shifted by Q2, drives the CD4040 frequency divider. One divider output supplies the 0.5Hz square wave; a second 500Hz output activates a charge pump, providing a -7V potential to A2. This arrangement allows A2 output swing to zero volts.

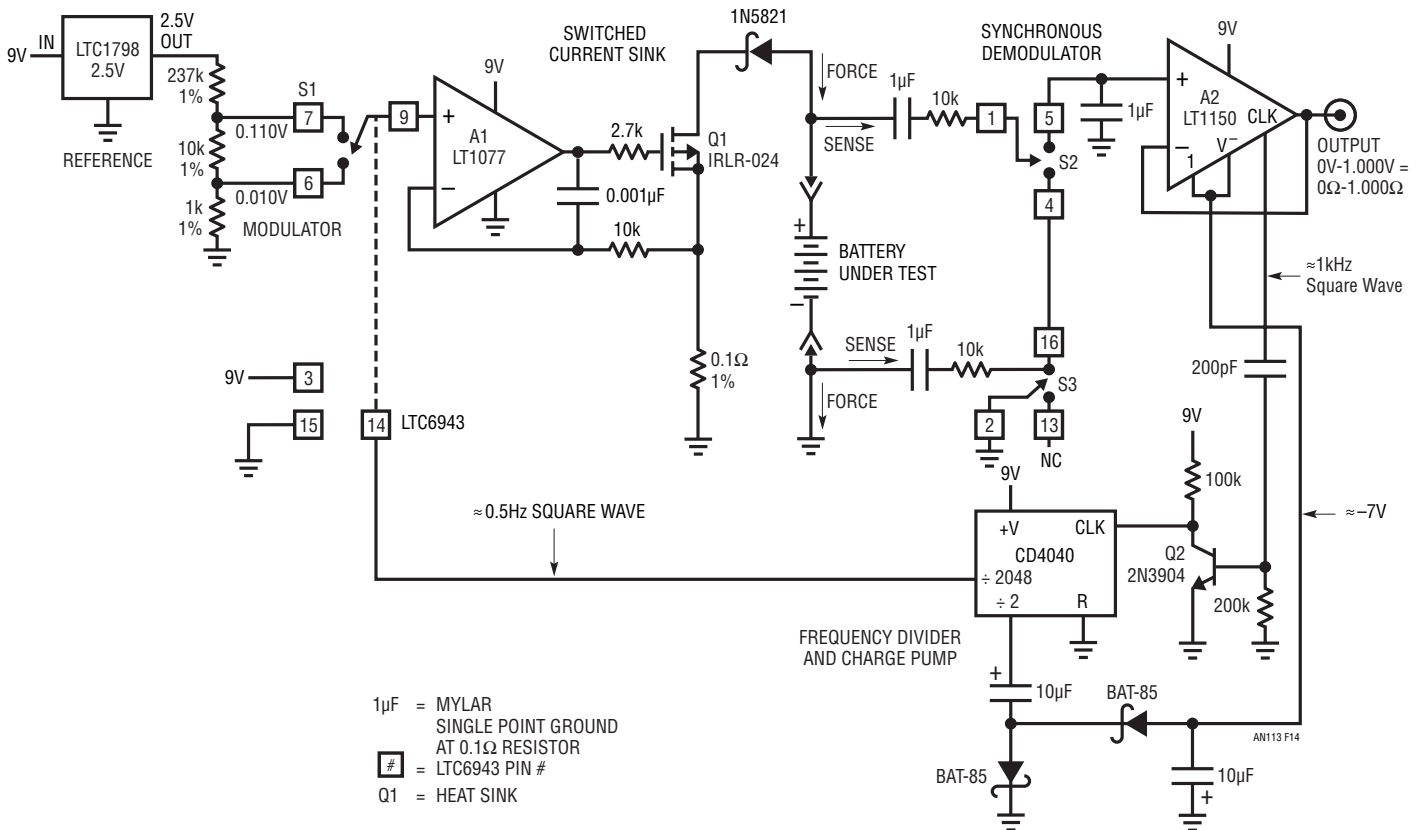


Figure 14. Battery Internal Resistance Is Determined by Repetitively Stepping Calibrated Discharge Current and Reading Resultant Voltage Drop. S1-Based Modulator, Clocked From Frequency Divider, Combines with A1-Q1 Switched Current Sink to Generate Stepped, 1 Ampere Battery Discharge Cycles. S2-S3-A2 Synchronous Demodulator Extracts Modulated Voltage Drop Information, Provides DC Output Calibrated in Ohms.

The circuit pulls 230 μ A from its 9V battery power supply, permitting about 3000 hours battery life. Other specifications include operation down to 4V with less than 1mV (0.001 Ω) output variation, 3% accuracy and battery-under-test range of 0.9V to 13V. Finally, note that battery discharge current and repetition rate are easily varied from the values given, permitting observation of battery resistance under a variety of conditions.

Floating Output, Variable Potential Battery Simulator

Battery stack voltage monitor development (Reference 5) is aided by a floating, variable potential battery simulator. This capability permits monitor accuracy verification over a

wide range of battery voltage. The floating battery simulator is substituted for a cell in the stack and any desired voltage directly dialed out. Figure 15's circuit is simply a battery powered follower (A1) with current boosted (A2) output. The LT1021 reference and high resolution potentiometric divider specified permits accurate output setting within 1mV. The composite amplifier unloads the divider and drives a 680 μ F capacitor to approximate a battery. Diodes preclude reverse biasing the output capacitor during supply sequencing and the 1 μ F - 150k combination provides stable loop compensation. Figure 16 depicts loop response to an input step; no overshoot or untoward dynamics occur despite A2's huge capacitive load. The battery monitor

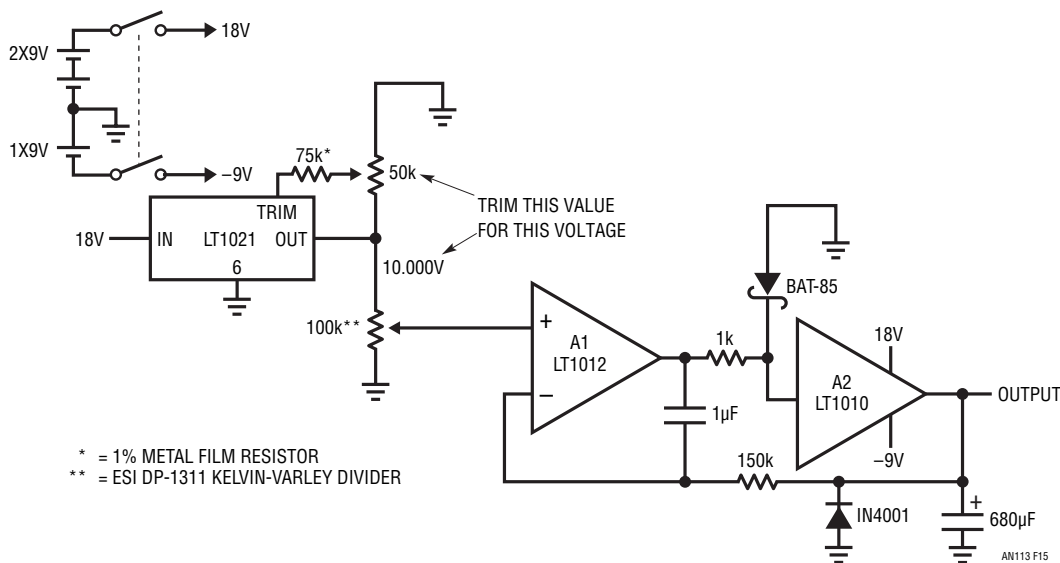


Figure 15. Battery Simulator Has Floating Output Settable within 1mV. A1 Unloads Kelvin-Varley Divider; A2 Buffers Capacitive Load.

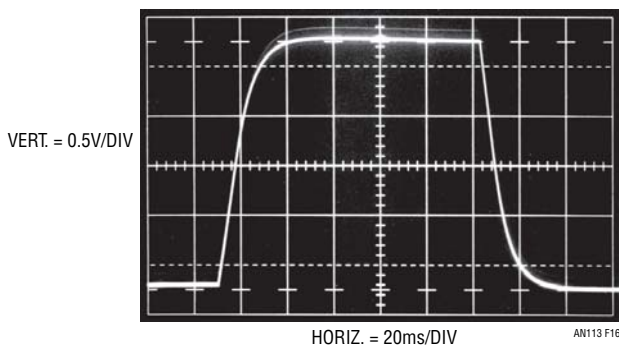


Figure 16. 150k-1 μ F Compensation Network Provides Clean Response Despite 680 μ F Output Capacitor.

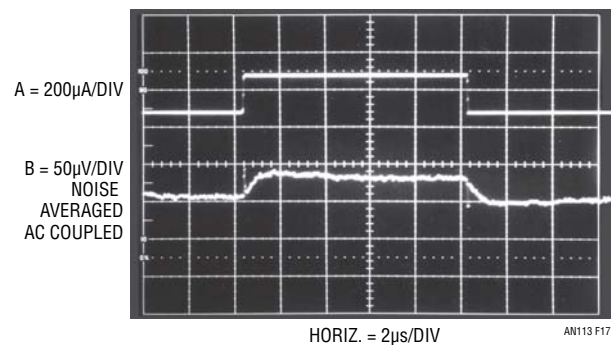


Figure 17. Battery Simulator Output (Trace B) Responds to Trace A's Monitor Current Pulse. Closed Loop Control and 680 μ F Capacitor Maintain Simulator Output within 30 μ V. Noise Averaged, 50 μ V/Division Sensitivity Is Required to Resolve Response.

an113f

Application Note 113

determines battery voltage by injecting current into the battery and measuring resultant clamp voltage (again, see Reference 5). Figure 17 shows battery simulator response (trace B) to trace A's monitor current pulse into the output. Closed loop control and the 680µF capacitor limit simulator output excursion within 30µV. This error is so small that noise averaging techniques and a high gain oscilloscope preamplifier are required to resolve it.⁴

40nV_{p-p} Noise, 0.05µV/°C Drift, Chopped FET Amplifier

Figure 18's circuit combines the LTC6241's rail-to-rail performance with a pair of extremely low noise JFETs configured in a chopper-based carrier modulation scheme to achieve extraordinarily low noise and DC drift. This circuit's performance suits demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The LTC1799's output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing the FET-A1 based stage to see a chopped version of the input voltage. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to DC output amplifier A2. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. The AC coupled input stage's DC errors do not affect overall circuit characteristics, resulting in the extremely low offset and drift noted.

Note 4. This may be viewed as a historic event in some thinly populated circles. Figure 17 marks the author's first published use of a digital oscilloscope (Tektronix 7603/7D20), updating him to the 1980s.

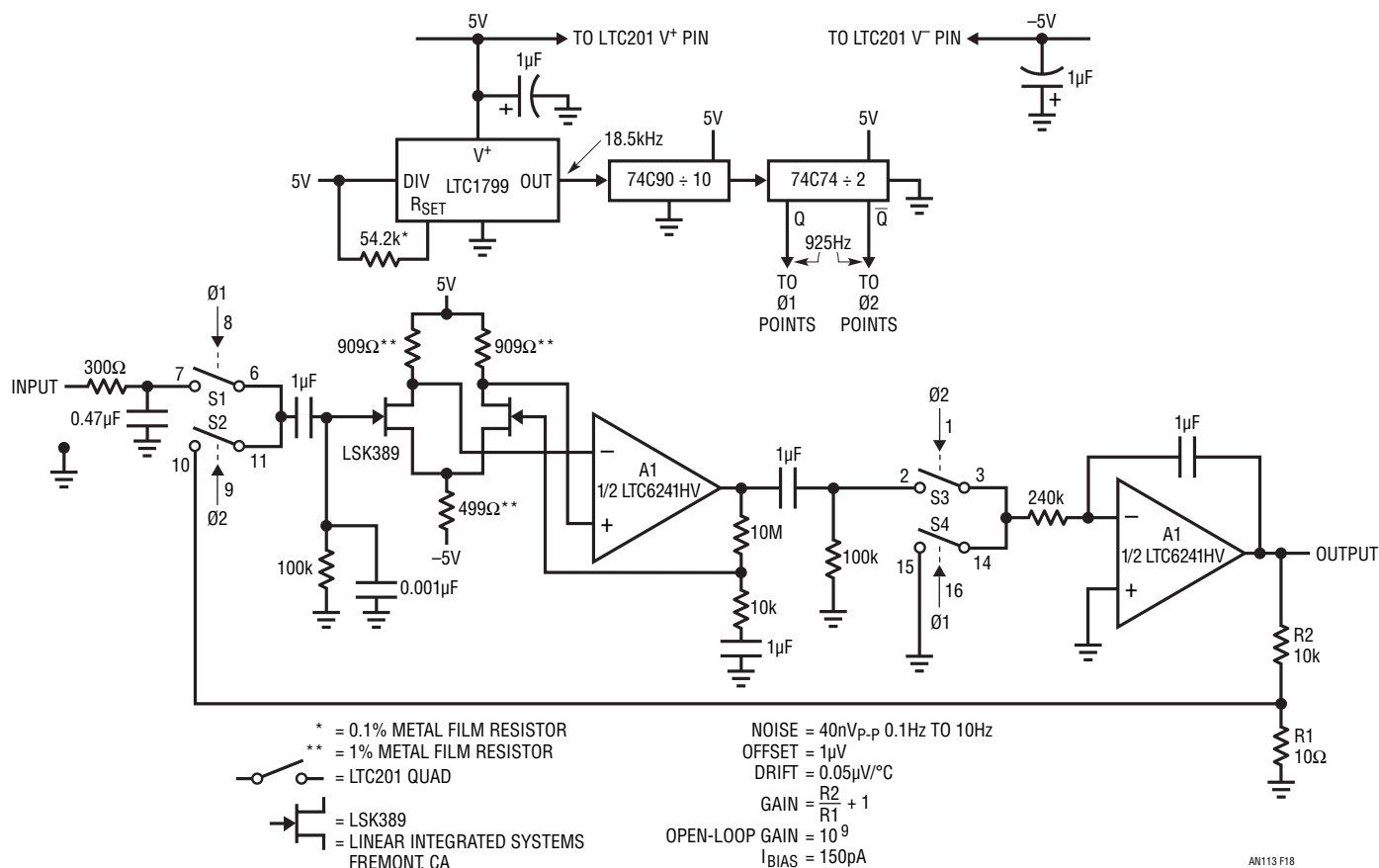


Figure 18. Chopped FET Amplifier Has 40nV_{p-p} Noise and 0.05µV/°C Drift. DC Input Is Carrier Modulated, Amplified by A1, Demodulated to DC and Fed Back From A2. 925Hz Carrier Clock Prevents Interaction with 60Hz Line Originated Components.

Figure 19, measured over a 50 second interval, shows 40nV_{p-p} noise in a 0.1Hz to 10Hz bandwidth. This is spectacularly low noise for a JFET-based design and is directly attributable to input pair area and current density.

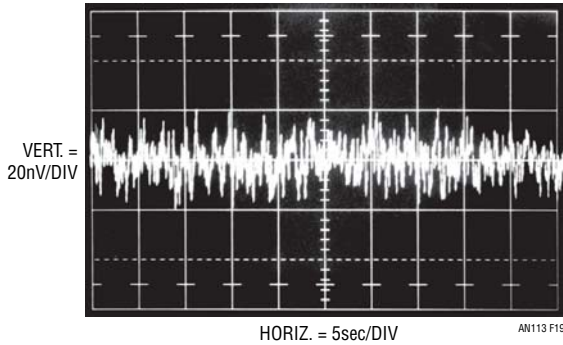


Figure 19. Amplifier 0.1Hz to 10Hz Noise Measures 40nV_{p-p} in 50 Second Sample Period.

Wideband, Chopper Stabilized FET Amplifier

The previous circuit's bandwidth is limited because the chopping occurs within the signal path. Figure 20's circuit circumvents this restriction by placing the stabilizing element in parallel with the signal path. This maintains DC performance although noise triples to 125nV in a 0.1Hz to 10Hz bandpass.

FET pair Q1 differentially feeds A2 to form a simple low noise op amp. Feedback, provided by R1 and R2, sets closed loop gain (in this case 1000) in the usual fashion. Although Q1 has extraordinarily low noise characteristics, its offset and drift are relatively high. A1, a chopper stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1A's channel current to minimize the difference. Q1's drain values ensure that A1 will be able to capture the

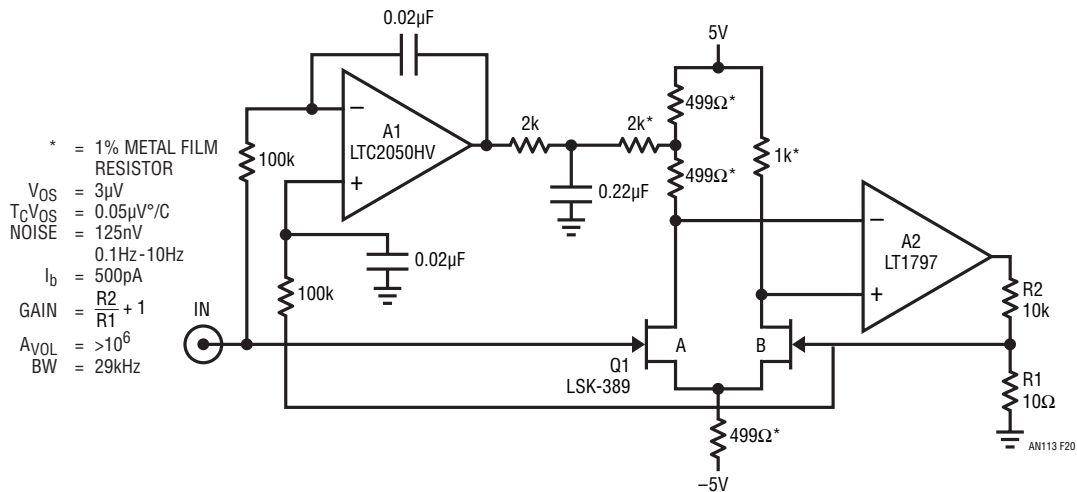


Figure 20. Placing Stabilizing Amplifier Outside Signal Path Permits Bandwidth Increase over Previous Circuit. Noise Triples to 125nV in 0.1Hz to 10Hz Bandpass.

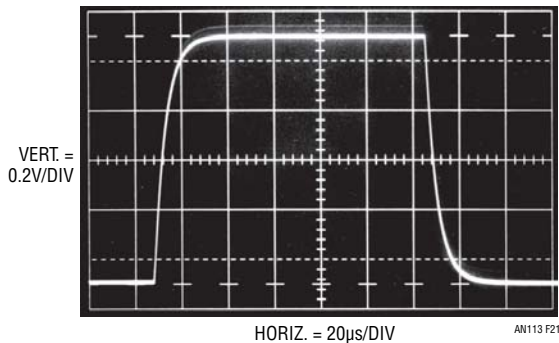


Figure 21. Figure 20 Responds to a 1mV Input. 12μs Rise Time Indicates 29kHz Bandwidth at A = 1000.

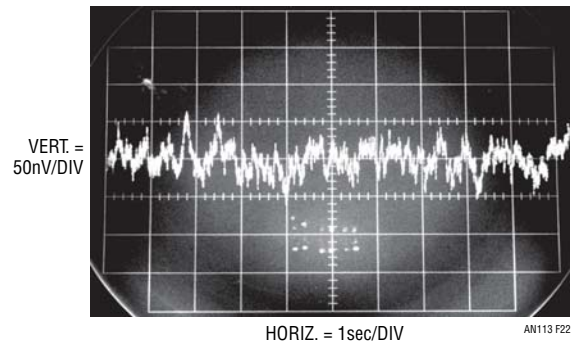


Figure 22. Chopper Stabilized FET Pair Noise Measures 125nV in 0.1Hz to 10Hz Bandpass.

an113f

Application Note 113

offset. A1 supplies whatever current is required to Q1A's channel to force offset within $5\mu\text{V}$. Additionally, A1's low bias current does not appreciably add to the overall 500pA amplifier bias current. As shown, the amplifier is set up for a noninverting gain of 1000, although other gains and inverting operation are possible.

Placing the offset correction in parallel with the signal path permits high bandwidth. Figure 21 shows response to a 1mV input. The $12\mu\text{s}$ risetime indicates 29kHz bandwidth at $A = 1000$.

Figure 22's photo measures noise in a 0.1Hz to 10Hz bandwidth. The performance obtained is almost 6 times

better than any monolithic chopper stabilized amplifier, while retaining low offset and drift.

Submicroampere RMS Current Measurement for Quartz Crystals

Quartz crystal RMS operating current is critical to long-term stability, temperature coefficient and reliability. Accurate determination of RMS crystal current, especially in micropower types, is complicated by the necessity to minimize introduced parasitics, particularly capacitance, which corrupt crystal operation. Figure 23's high gain, low noise amplifier combines with a commercially available

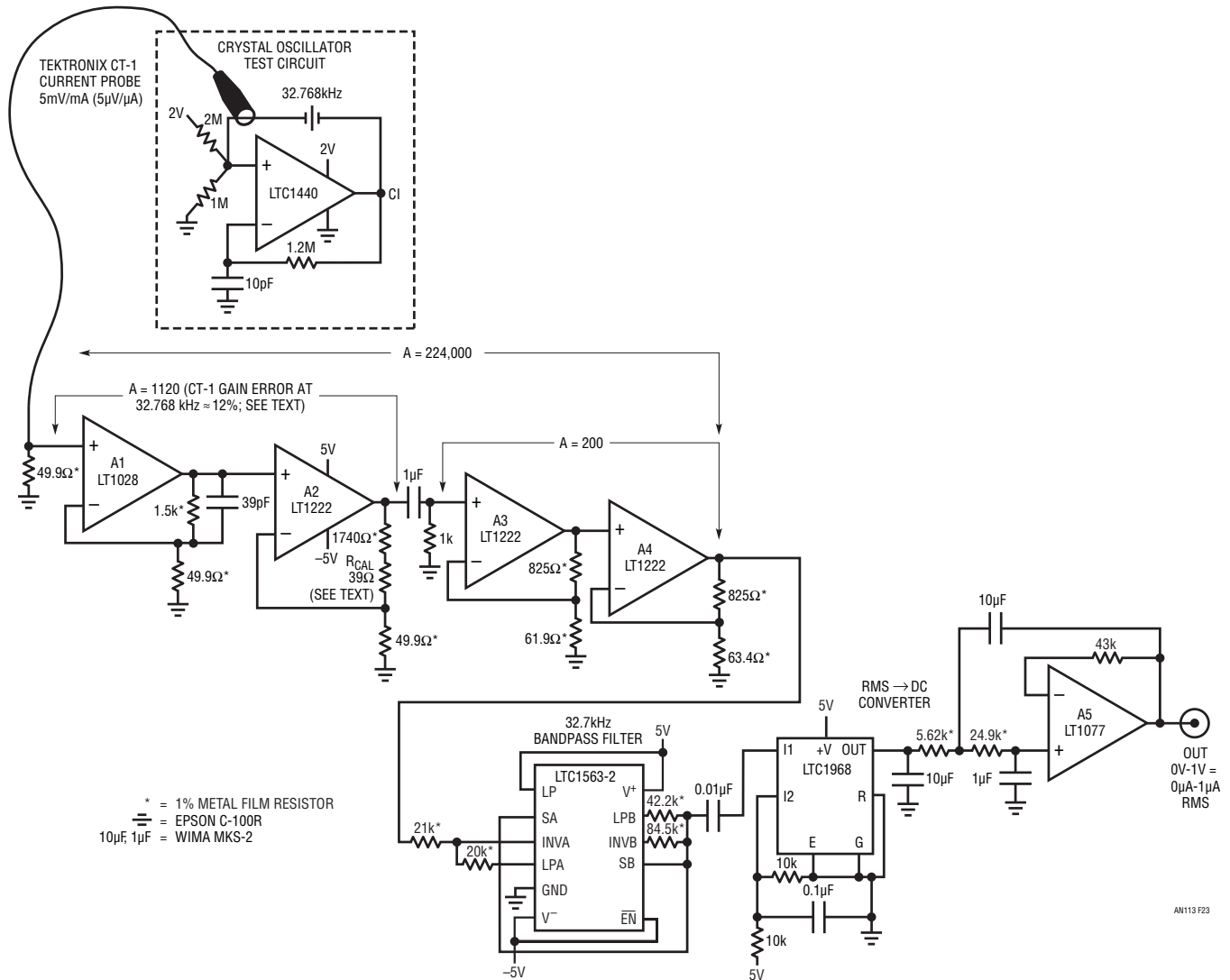


Figure 23. A1 to A4 Furnish Gain of >200,000 to Current Probe, Permitting Submicroamp Crystal Current Measurement. LTC1563-2 Bandpass Filter Smooths Residual Noise While Providing Unity Gain at 32.768kHz. LTC1968 Supplies RMS Calibrated Output.

an113f

closed core current probe to permit the measurement. An RMS-to-DC converter supplies the RMS value. The quartz crystal test circuit shown in dashed lines exemplifies a typical measurement situation. The Tektronix CT-1 current probe monitors crystal current while introducing minimal parasitic loading. The probe's 50Ω terminated output feeds A1. A1 and A2 take a closed loop gain of 1120; excess gain over a nominal gain of 1000 corrects for the CT-1's 12% low frequency gain error at 32.768kHz.⁵ A3 and A4 contribute a gain of 200, resulting in total amplifier gain of 224,000. This figure results in a $1\text{V}/\mu\text{A}$ scale factor at A4 referred to the gain corrected CT-1's output. A4's LTC1563-2 bandpass filtered output feeds an LTC1968-A5 based RMS \rightarrow DC converter which provides the circuits output. The signal processing path constitutes an extremely narrow band amplifier tuned to the crystal's frequency. Figure 24 shows typical circuit waveforms. Crystal drive, taken at C1's output (trace A), causes a 530nA RMS crystal current which is represented at A4's output (trace B) and the RMS \rightarrow DC converter input (trace C). Peaking visible in trace B's unfiltered presentation derives from parasitic paths shunting the crystal.

Typical circuit accuracy is 5%. Uncertainty terms include the transformer's tolerances, its $\approx 1.5\text{pF}$ loading and resistor/RMS \rightarrow DC converter error. Calibrating the circuit

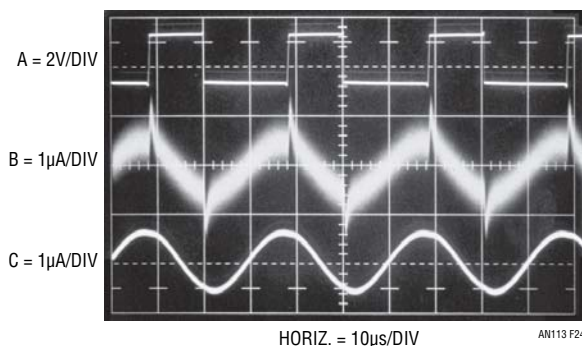


Figure 24. C1's 32.768kHz Output (Trace A) and Crystal Current Monitored at A4 Output (Trace B). RMS Converter Input Is Trace C. Peaks in Trace B's Unfiltered Waveform Derive From Inherent and Parasitic Paths Shunting Crystal.

reduces error to less than 1%. Calibration involves driving the transformer with $1\mu\text{A}$ at 32.7kHz. This is facilitated by biasing a 100k, 0.1% resistor with an oscillator set at 0.100V output. The output voltage should be verified with an RMS voltmeter having appropriate accuracy (see Reference 8's Appendix B). Figure 23 is calibrated by padding A2's gain with a small resistive correction, typically 39Ω .

Direct Reading Quartz Crystal-Based Remote Thermometer

Although quartz crystals have been used as temperature sensors (see References 7 and 10) there has been almost no adaptation of this technology. The primary impediment has been lack of standard product quartz crystal temperature sensors. The advantages of quartz-based temperature sensing include nearly purely digital signal conditioning, good stability and a direct, noise immune digital output ideally suited to remote sensing.

Figure 25 utilizes an economical, commercially available (Reference 9) quartz temperature sensor in a direct reading thermometer scheme suited to remote data collection. An LTC485 transceiver, set up in transmit mode, forms a quartz-based, Pierce class oscillator. The transceiver's differential line driving outputs provide frequency coded temperature data to a 1000 foot cable run. A second RS485 transceiver differentially receives the data, presenting a single ended output to the PIC-16F73 processor. The processor converts the frequency coded temperature data to its $^{\circ}\text{C}$ equivalent, which appears on the display. Figure 26 is a software listing of the processor's program.⁶ Accuracy over a sensed -40°C to 85°C range is about 2%.

Note 5. The validity of this gain error correction at one sinusoidal frequency – 32.768kHz – was investigated with a 7-sample group of Tektronix CT-1s. Device outputs were collectively within 0.5% of 12% down for a $1\mu\text{A}$ 32.768kHz sinusoidal input current. Although this tends to support the measurement scheme, it is worth noting that these results are as measured. Tektronix does not guarantee performance below the specified -3dB 25kHz low frequency roll-off.

Note 6. Mark Thoren of LTC designed the processor-based circuitry and authored Figure 26's software.

Application Note 113

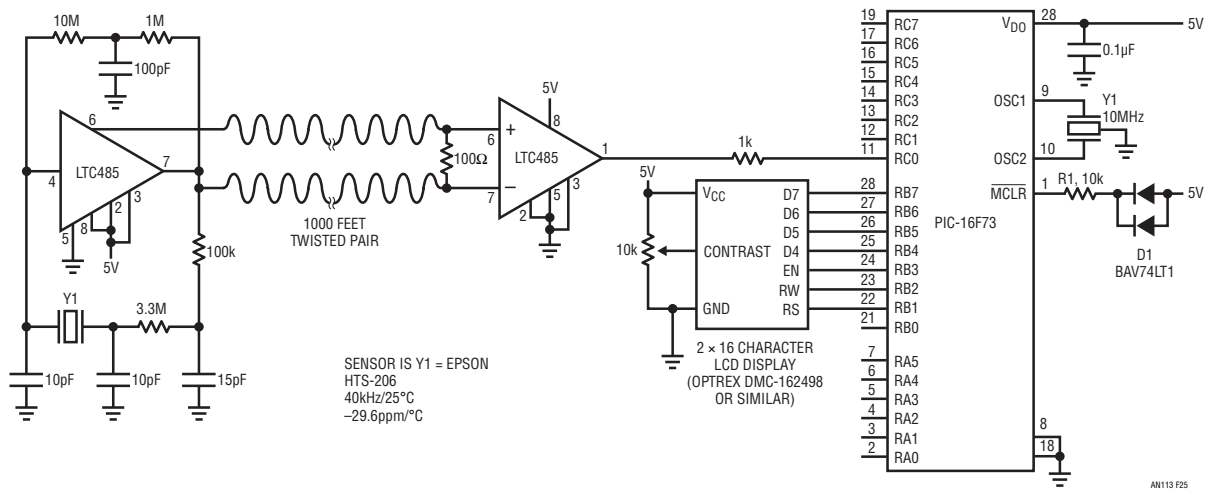


Figure 25. Quartz Crystal-Based Remote Thermometer Has 2% Accuracy over -40°C to 85°C Sensed Range, Drives 1000ft Cable. RS-485 Transceiver Oscillates at Y1 Quartz Sensor Determined Frequency and Drives Cable. Second Transceiver Receives Data and Feeds Processor. Display Reads Directly in °C.

```

/*
Thermometer based on Epson HT206 temperature sensing crystal.
Output is to a standard Epson HD447980 based alphanumeric
LCD display. LCD driver functions are part of compiler library

Written for CSS compiler version 3.182

*/

#include <16F73.h>
#device adc=8
#fuses NOWDT, HS, PUT, NOPROTECT, NOBROWNOUT
#use delay(clock=1000000) // Tell compiler how fast we're going
#use rs232(baud=9600, parity=N, xmit=PIN_C6, rcv=PIN_C7, bits=8)
#include "lcd.c" // LCD driver functions

void main( )
{
    int16 temp;
    unsigned int16 f;
    setup_adc_ports(NO_ANALOGS);
    setup_adc(ADC_OFF);
    setup_spi (FALSE);
    setup_counters (RTCC_INTERNAL, RTCC_DIV_1);
    setup_timer_1 (T1_EXTERNAL|T1_DIV_BY_1);
    setup_timer_2 (T2_DISABLED, 0, 1);
    lcd_init( ); // Initialize LCD

while(1)
    (
        set_timer1(0); // Reset counter
        setup_timer_1(T1_EXTERNAL|T1_DIV_BY_1); // Turn on counter
        delay_ms(845); // 0.845412 is the magic time to count
        delay_us(412); // -it gives 1 less plus per degree C
        setup_timer_1(T1_DISABLED); // turn off counter
        f = get_timer1(); // Read result
        temp = 33770 - f + 25; // Convert to temperature

        /** At this point 'f' is the temperature in degrees C **//
        /** For this experiment, dump to standard HD44780 type LCD display **//

        lcd_putc('\f'); // Clear screen
        lcd_gotoxy(1, 1); // Goto home position
        printf(lcd_putc, "%ld", temp); // And display result
    )
}

```

Figure 26. Software Listing for PIC Processor Program. Code Converts Frequency to °C Equivalent, Drives Display.

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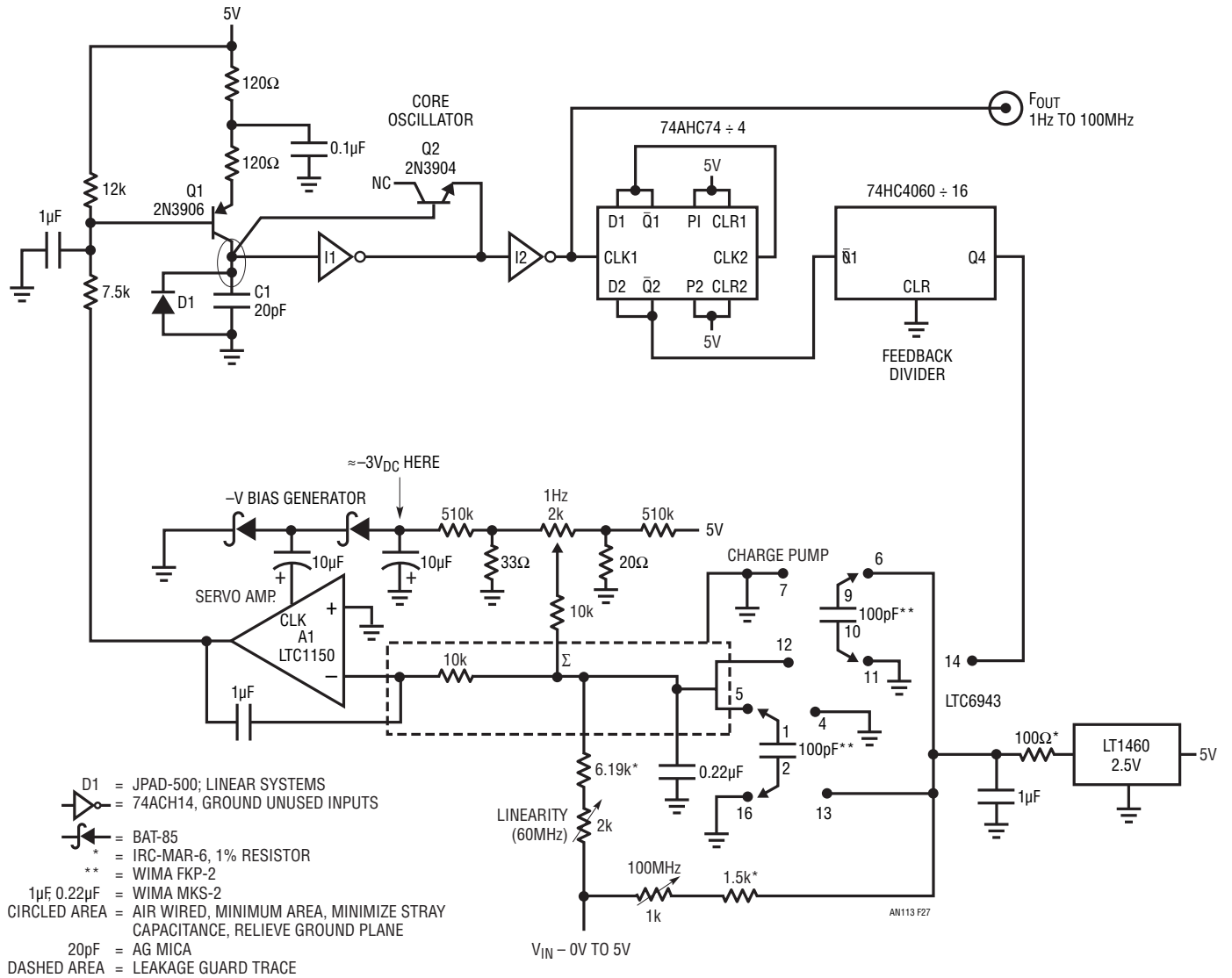


Figure 27. 1Hz to 100MHz V→F Converter Has 160dB Dynamic Range, Runs From 5V Supply. Input Biased Servo Amplifier Controls Core Oscillator, Stabilizing Circuit's Operating Point. Wide Range Operation Derives From Core Oscillator Characteristics, Divider/Charge Pump-Based Feedback and A1's Low DC Input Errors.

Application Note 113

1Hz-100MHz V→F Converter

Figure 27's circuit achieves a wider dynamic range and higher output frequency than any commercially available voltage to frequency ($V \rightarrow F$) converter. Its 100MHz full-scale output (10% overrange to 110MHz is provided) is at least ten times faster than available units. The circuit's 160dB dynamic range (8 decades) allows continuous operation down to 1Hz. Additional specifications include 0.1% linearity, 250ppm/ $^{\circ}C$ gain temperature coefficient, 1Hz/ $^{\circ}C$ zero shift, 0.1% frequency shift for $V_{SUPPLY} = 5V \pm 10\%$ and a 0V to 5V input range. A single 5V supply powers the circuit.⁷

A1, a chopper stabilized amplifier, servo biases a crude but wide range core oscillator in Figure 27. The core oscillator drives a charge pump via digital dividers. The averaged difference between the charge pump's output and the circuit's input appears at a summing node (Σ) and biases A1, closing a control loop around the wide range core oscillator. The circuit's extraordinary dynamic range and high speed derive from core oscillator characteristics, divider/charge pump-based feedback and A1's low DC input errors. A1 and the LTC6943-based charge pump stabilize circuit operating point, contributing high linearity and low drift. A1's low offset drift allows the circuit's 50nV/Hz gain slope, permitting operation down to 1Hz at 25 $^{\circ}C$.

The positive input voltage causes A1 to swing negatively, biasing Q1. Q1's resultant collector current ramps C1 (trace A, Figure 28) until Schmitt trigger inverter I1's output (trace B) goes low, discharging C1 via Q2. C1's discharge resets I1's output to its high state, Q2 goes off

and the ramp-and-reset action continues. D1's leakage dominates all parasitic currents in the core oscillator, ensuring operation down to 1Hz. The $\div 64$ divider chain's output clocks the LTC6943-based charge pump. The charge pump's two sections operate out-of-phase, resulting in charge transfer at each clock transition. Charge pump stability is primarily determined by the LT1460 2.5V reference, the switches low charge injection and the 100pF capacitors. The 0.22 μF capacitor averages the pumping action to DC. The averaged difference between the input derived current and the charge pump feedback signal is amplified by A1, which biases Q1 to control circuit operating point. Core oscillator nonlinearity and drift are compensated by A1's servo action, resulting in the high linearity and low drift previously noted. A1's 1 μF capacitor provides stable loop compensation. Figure 29 shows loop response (trace B) to an input step (trace A) is well controlled.

Some special techniques enable this circuit to achieve its specifications. D1's leakage current dominates all parasitic currents at I1's input; hence Q1 must always source current to sustain oscillation, assuring operation down to 1Hz. The 100MHz full-scale frequency sets stringent restrictions on core oscillator cycle time. Only 10ns is available for a

Note 7. Reference 12 (1986) contains a circuit with comparable specifications although considerably more complex than the one presented here. The advent of high speed CMOS logic permitted replacing the earlier designs ECL elements, facilitating a dramatic decrease in complexity. Comparing the designs permits viewing the impact a technology shift can have in realizing a circuit function. In this case, the effect is pervasive, directly or indirectly influencing nearly every aspect of circuit operation. While circuit architecture is consistent, this incarnation is substantially and favorably altered.

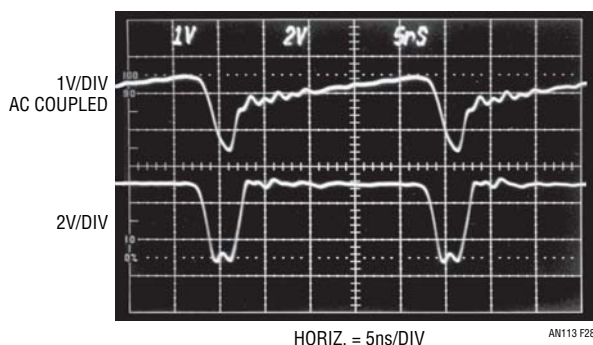


Figure 28. $V \rightarrow F$ Operation at 40MHz. Core Oscillator Waveforms Viewed in 670MHz Real Time Bandwidth Include Q1 Collector (Trace A) and Q2 Emitter (Trace B). Ramp-and-Reset Operating Characteristic Is Apparent; Reset Duration of 6ns Permits 100MHz Repetition Rate.

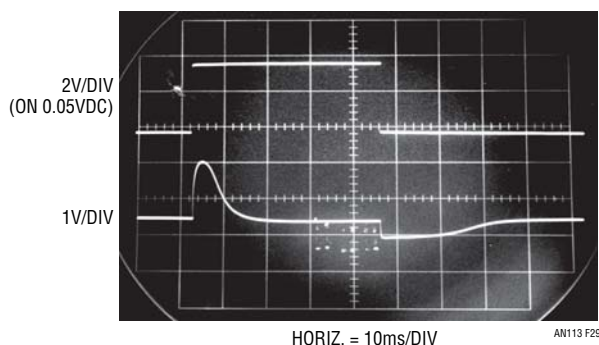


Figure 29. Response (Trace B) to an Input Step (Trace A) Shows 30ms Settling Time at Summing Junction (Σ). A1's 1 μF Capacitor Shapes Response, Stabilizing Feedback Loop. Clamped Response on Negative Going Input Step is Due to Summing Junction Limiting.

complete ramp-and-reset sequence. The ultimate speed limitation is the reset interval. Figure 28, trace B, shows a 6ns interval, comfortably within the 10ns limit.

A scaled resistive path from the input to the charge pump corrects small nonlinearities due to residual charge injection. This input derived correction is effective because the charge injections effect varies directly with input determined frequency.

Prototype and small lot construction may proceed using the schematic and its notes, but component selection should be considered for volume production. Figure 30 lists applicable components and their selection targets.

To calibrate this circuit apply 5.000V and trim the 100MHz adjustment for a 100.0MHz output. Next, ground the input and adjust the 1Hz trim for 1Hz output. Allow for long settling time, as charge pump update rate at this frequency is once every 32 seconds. Note that this trim accommodates either offset polarity because of the $-V$ bias derived from A1's clock output. Finally, set the 60MHz adjustment for 60.0MHz with $3.000V_{IN}$. Repeat these adjustments until all three points are fixed.

Delayed Pulse Generator with Variable Time Phase, Low Jitter Trigger Output

Fast circuitry often requires a pulse generator that also supplies a variable time phase trigger output. It is desirable that the main output pulse occurrence be continuously settable from before to after the trigger output with low time jitter. Figure 31's circuit produces a 360ps risetime output pulse with trigger output time phase variable from -30 ns to 100ns. Jitter is 40ps.

Q1 and Q2 form a current source that charges the 1000pF capacitor. When the LTC1799 clock is high (trace A, Figure 32) both Q3 and Q4 are on. The current source is off and A2's output (trace B) is at ground. C1's latch input prevents it from responding and its output remains high. When the clock goes low, C1's latch input is disabled and its output drops low. The Q3 and Q4 collectors lift and Q2 comes on, delivering constant current to the 1000pF capacitor. The resulting linear ramp at A2 (trace B) is applied to bounded current summing amplifiers A3 and A4. Both amplifiers compare ramp induced current with fixed, opposite polarity currents derived from A1 – Q6. A1-Q6, in turn, is referred to the +5 supply rail which also sets Q1-Q2 current and hence, ramp slope. This ratiometric connection promotes supply rejection. When A4 and A3 (traces C and F, respectively) come out of diode bound and cross zero, comparators C2 and C1 (traces D and G, respectively) are heavily overdriven and switch rapidly. C2's output path includes components which form trace E's trigger output pulse. C1 triggers output pulse generator Q5, operating in avalanche mode (trace H).⁸

The "delay adjust" control sets the ramp amplitude that A3-C1 switches the main output at, providing the desired variable time phase with respect to the A4-C2 controlled trigger output. Time jitter between C1 and C2 outputs is minimized because A3 and A4 effectively multiply ramp transition rate as their outputs enter the active region, provide gain and cross zero.

Note 8. Avalanche mode pulse generation is a subtle, arcane technique requiring extensive discussion. The text's cavalier treatment is deliberately brief in order to maintain focus on this circuit's low timing jitter characteristics. More studious coverage can be found in References 13-22.

COMPONENT	SELECTION PARAMETER (25°C)	TYPICAL YIELD (%)
Q1	$I_{CER} < 20\text{pA}$ at 3V	90
Q2	$I_{EBO} < 20\text{pA}$ at 3V	90
D1	$I_{REV} < 500\text{pA}$, $> 75\text{pA}$ at 3V	80
I1	$I_{IN} < 25\text{pA}$	80
A1	$I_B < 5\text{pA}$ at $V_{SUPPLY} = 5V$	90
74ACH74	Operate with 3.6nS Wide (50% Point) Input Pulse	80

Figure 30. Selection Criteria for Components Ensure $V \rightarrow F$ Performance. First Five Entries Enhance Operation Below 100Hz. Last Entry Assures Reliable Feedback Divider Operation.

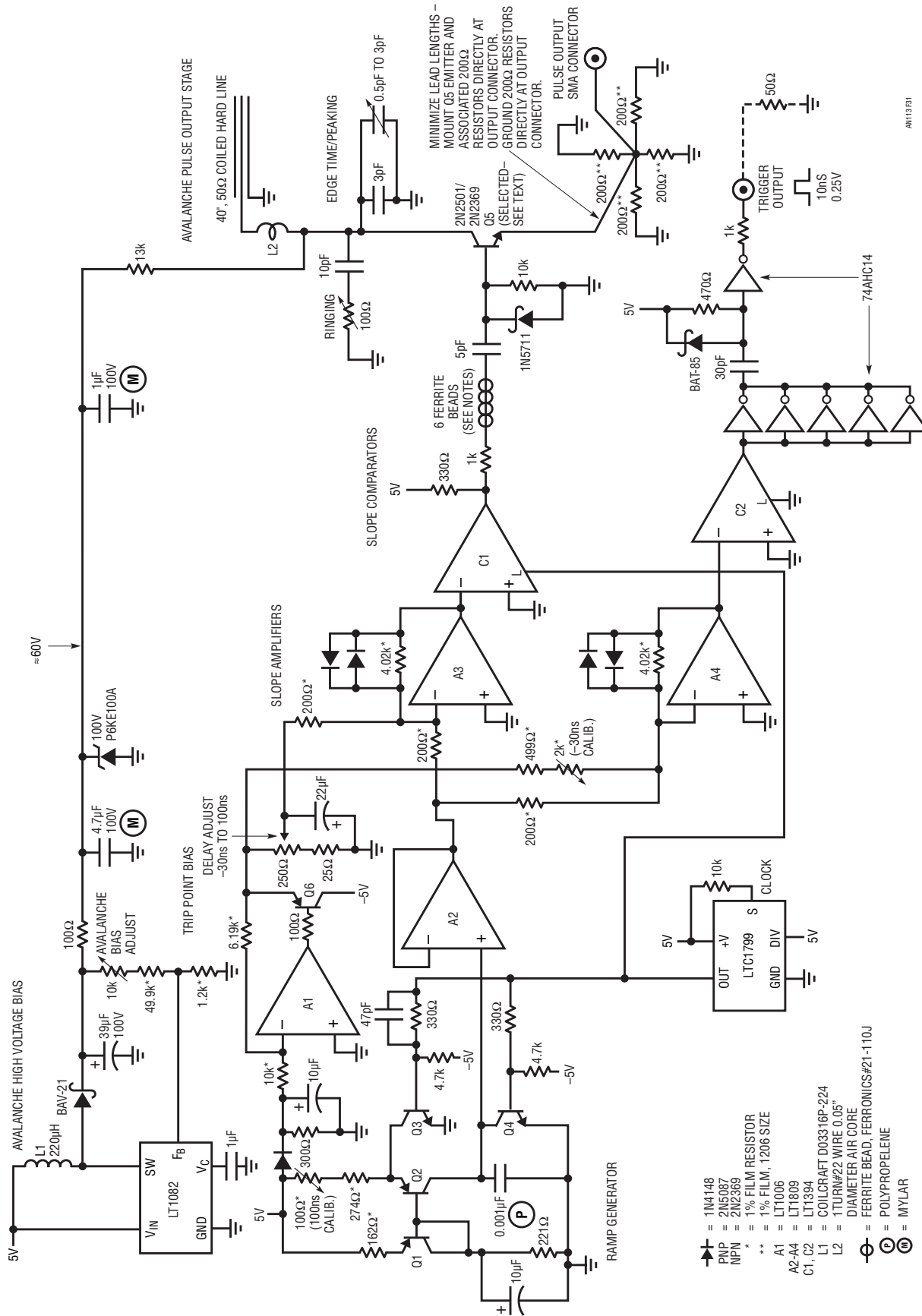


Figure 31. Pulse Generator Output Time Phase Varies -30ns to 100ns with Respect to Trigger Output; Jitter Is 40ps. Clocked Ramp at A2 Produces Variable (A3-C1) and Fixed (A4-C2) Delays Driving Pulse and Trigger Outputs, Respectively. A3-A4 Provide Gain to Comparators at Trip Point, Minimizing Time Jitter Between Outputs.

The A3-A4 amplifier gain is the key to low jitter between C1 and C2's switching times. The amplifiers augment the comparator's relatively low gain, promoting decisive switching despite the ramp input. Figure 33 shows A4 (trace A)-C2 (trace B) response to the ramp crossing the trip point. As the ramp nears the trip point A4 comes out of bound, providing an amplified version of the ramp's transition rate to C2. C2 responds by switching decisively 6ns after A4 crosses zero volts at center screen. A3-C1 waveforms are identical. Figure 34, Q5's pulse output, taken with the oscilloscope synchronized to the trigger output, shows 40ps jitter in a 3.9GHz sampled bandpass.

Circuit calibration is accomplished by first adjusting the “-30ns cal” so the main pulse output occurs 30ns before the trigger output with the “Delay Adjust” set to minimum. Next, with the “Delay Adjust” set to maximum, trim the “100ns cal” so the main pulse output occurs 100ns after the trigger output. Slight interaction between the 30ns and 100ns trims may require repeating their adjustments until both points are calibrated. As mentioned, the avalanche output stage is illustrative only and not detailed in this discussion. Its optimization and calibration are covered in Reference 13.

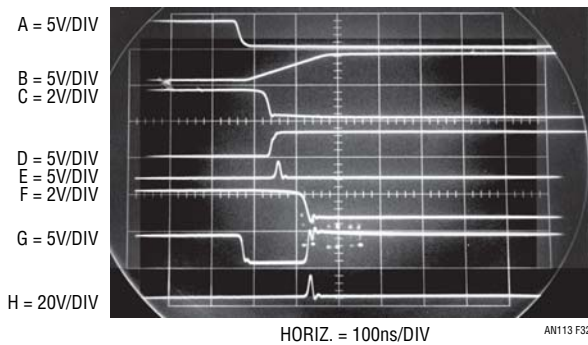


Figure 32. Low Jitter Delayed Pulser Waveforms Include Clock (Trace A), A2 Ramp (B), A4 (C), C2 (D), Trigger Output (E), A3 (F), C1 (G) and Delayed Output Pulse (H). Trigger-to-Output Pulse Delay Is Continuously Variable From -30ns to 100ns.

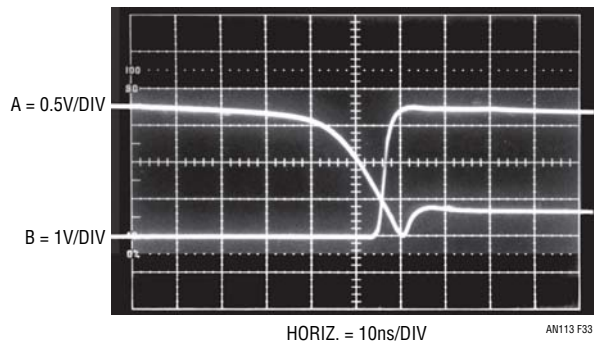


Figure 33. A4 (Trace A) - C2 (Trace B) Response to A2's Ramp Crossing Trip Point. C2 Goes High 6ns after A4 Crosses Zero (Center Screen). A3-C1 Waveforms Are Identical.

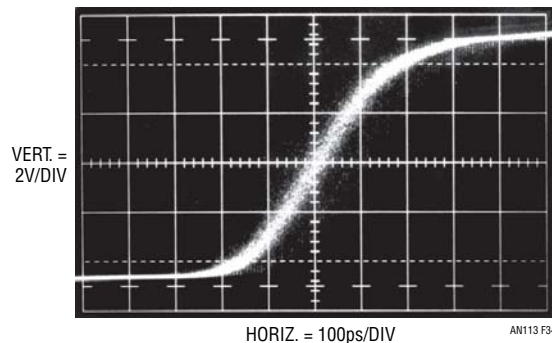


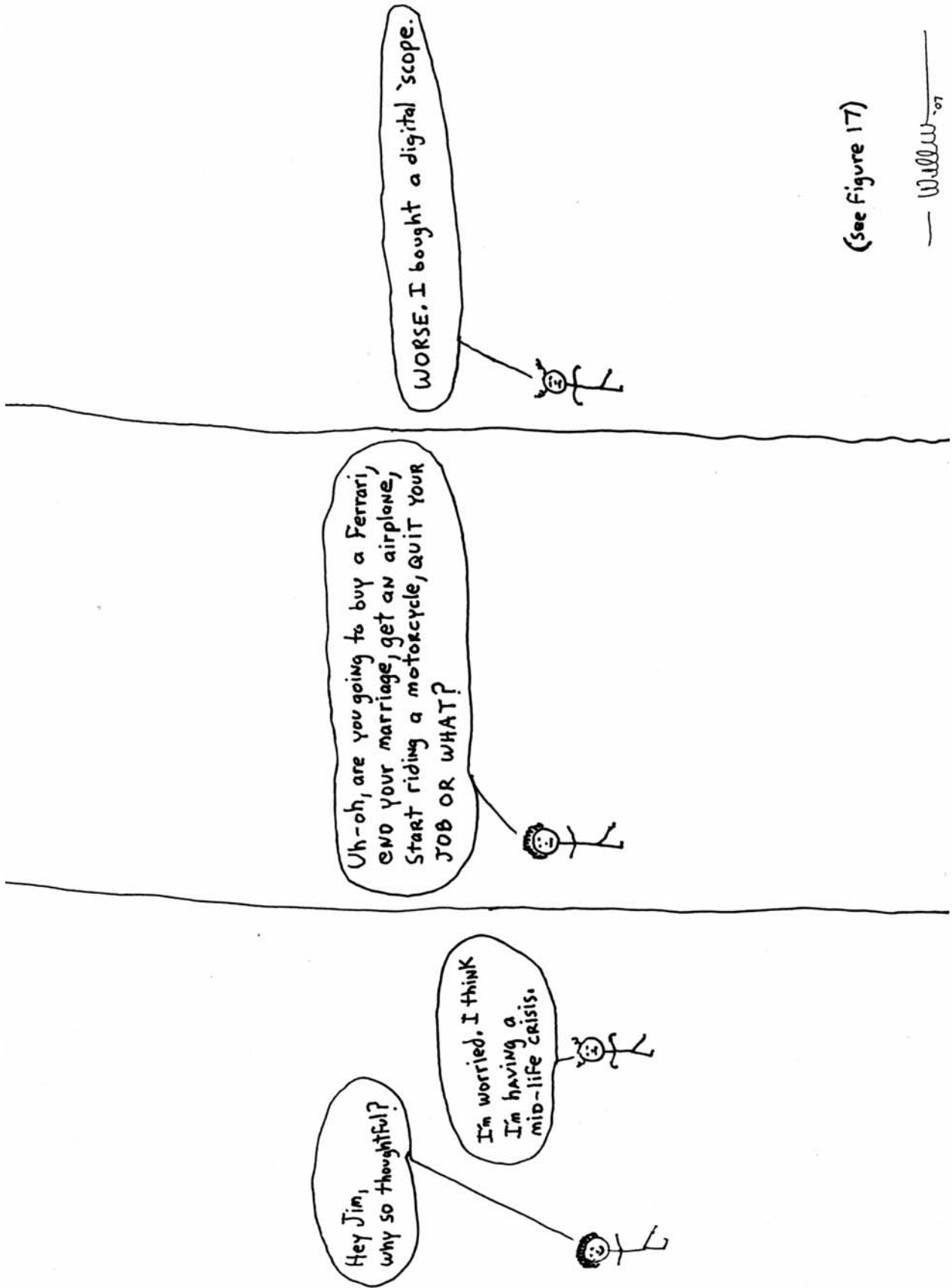
Figure 34. Main Pulse Output Synchronized to Trigger Output Shows 40ps Jitter in 3.9GHz. Sampled Bandpass.

Application Note 113

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20. Williams, Jim, "A Seven-Nanosecond Comparator for Single Supply Operation," "Programmable Subnanosecond Delayed Pulse Generator," p. 32-34, Linear Technology Corporation, Application Note 72, May 1998.
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22. R. B. Seeds, "Triggering of Avalanche Transistor Pulse Circuits," Technical Report No. 1653-1, August 5, 1960, Solid-State Electronics Laboratory, Stanford Electronics Laboratories, Stanford University, Stanford, California.

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24. Markell, R. Editor, "Linear Technology Magazine Circuit Collection, Volume II," Linear Technology Corporation, Application Note 66, August 1996.
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High Voltage, Low Noise, DC/DC Converters

A Kilovolt with 100 Microvolts of Noise

Jim Williams

Introduction

Photomultipliers (PMT), avalanche photodiodes (APD), ultrasonic transducers, capacitance microphones, radiation detectors and similar devices require high voltage, low current bias. Additionally, the high voltage must be pristinely free of noise; well under a millivolt is a common requirement with a few hundred microvolts sometimes necessary. Normally, switching regulator configurations cannot achieve this performance level without employing special techniques. One aid to achieving low noise is that load currents rarely exceed 5mA. This freedom permits output filtering methods that are usually impractical.

This publication describes a variety of circuits featuring outputs from 200V to 1000V with output noise below 100 μ V measured in a 100MHz bandwidth. Special techniques enable this performance, most notably power stages optimized to minimize high frequency harmonic content. Although sophisticated, all examples presented utilize standard, commercially available magnetics—no custom components are required. This provision is intended to assist the user in quickly arriving at a produceable design. Circuits and their descriptions are presented beginning with the next ink.

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THE TEXT'S CIRCUITS. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THESE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THESE CIRCUITS. REPEAT: THESE CIRCUITS CONTAIN DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Resonant Royer Based Converters

The resonant Royer topology is well suited to low noise operation due to its sinusoidal power delivery¹. Additionally, the resonant Royer is particularly attractive because

transformers originally intended for LCD display backlight service are readily available. These transformers are multiply sourced, well proven and competitively priced.

Figure 1's resonant Royer topology achieves 100 μ V_{P-P} noise at 250V output by minimizing high frequency harmonic in the power drive stage. The self oscillating resonant Royer circuitry is composed of Q2, Q3, C1, T1 and L1. Current flow through L1 causes the T1, Q2, Q3, C1 circuitry to oscillate in resonant fashion, supplying sine

Note 1. This publication sacrifices academic completeness for focus on the title subject. As such, operating details of the various switching regulator architectures utilized are not covered. Readers desiring background tutorial are directed to the References. Resonant Royer theory appears in Reference 1.

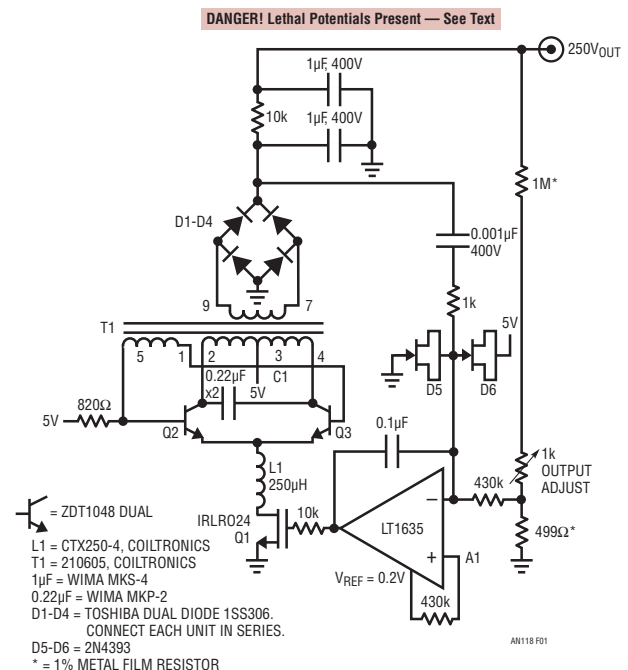


Figure 1. Current Fed Resonant Royer Converter Produces High Voltage Output. A1 Biases Q1 Current Sink, Enforcing Output Voltage Stabilizing Feedback Loop. A1's 0.001 μ F–1k Ω Network Phase Leads Output Filter, Optimizing Transient Response. D5-D6, Low Leakage Clamps, Protect A1

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Application Note 118

wave drive to T1's primary with resultant sine-like high voltage appearing across the secondary.

T1's rectified and filtered output is fed back to amplifier-reference A1 which biases the Q1 current sink, completing a control loop around the Royer converter. L1 ensures that Q1 maintains constant current at high frequency. Milliampere level output current allows the 10k resistor in the output filter. This greatly aids filter performance with minimal power loss.² The RC path to A1's negative input combines with the 0.1 μ F capacitor to compensate A1's loop. D5 and D6, low leakage clamps, protect A1 during start-up and transient events. Although Figure 2's collector waveforms are distorted, no high frequency content is present.

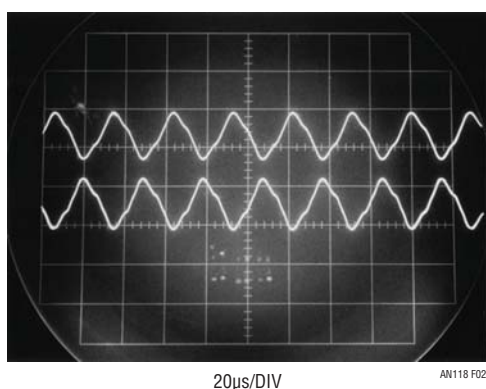


Figure 2. Resonant Royer Collector Waveforms Are Distorted Sinusoids; No High Frequency Content is Present

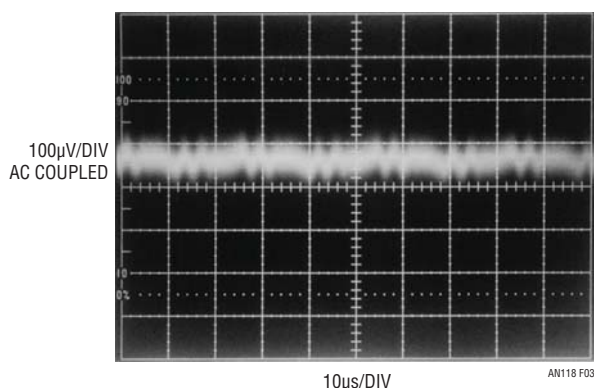


Figure 3. Figure 1's Output Noise is Just Discernible in Monitoring Instrumentation's 100 μ V Noise Floor

The circuit's low harmonic content combined with the RC output filter produces a transcendently clean output. Output noise (Figure 3) is just discernible in the monitoring instrumentation's 100 μ V noise floor³.

Figure 4's variant of Figure 1 maintains 100 μ V output noise while extending input supply range to 32V. Q1 may require heat sinking at high input supply voltage. Converter and loop operation is as before although compensation components are re-established to accommodate the LT1431 control element.

Note 2. As previously mentioned, low current requirements permit certain freedoms in the output filter and feedback network. See Appendix A for examples and discussion.

Note 3. Measurement technique and instrumentation choice for faithful low level noise measurement requires diligence. See Appendices B through E for practical considerations.

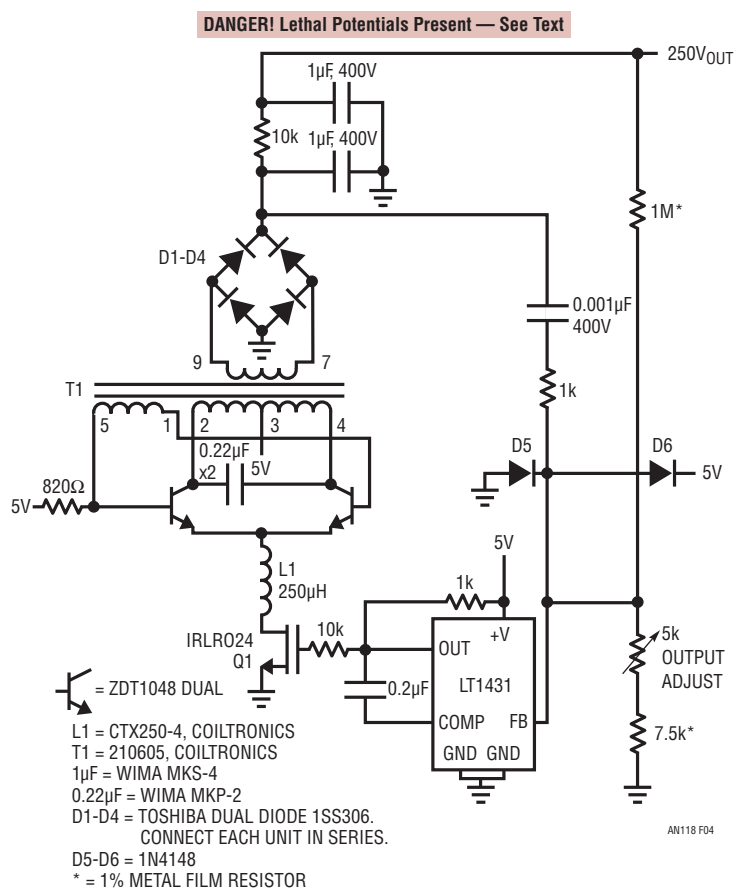


Figure 4. LT1431 Regulator Based Variant of Figure 1 Maintains 100 μ V Output Noise While Extending Input Supply Range to 32V. Q1 May Require Heat Sinking at High Input Supply Voltages

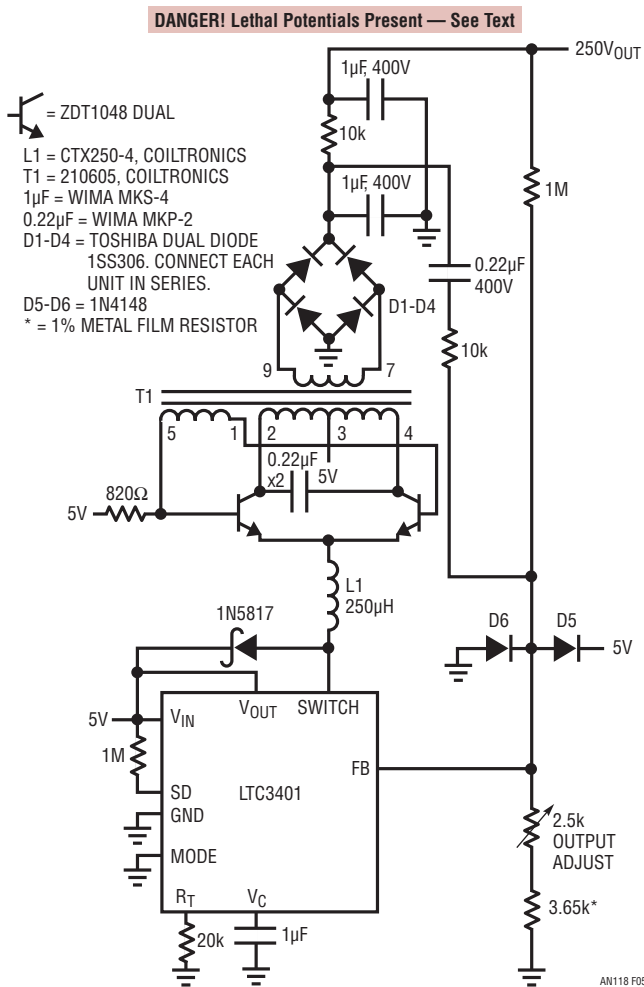


Figure 5. Replacing Linearly Operated Current Sink with Switching Regulator Minimizes Heating Although Output Noise Increases

Switched Current Source Based Resonant Royer Converters

The previous resonant Royer examples utilize linear control of converter current to furnish harmonic free drive. The trade off is decreased efficiency, particularly as input voltage scales. Improved efficiency is possible by employing switched mode current drive to the Royer converter. Unfortunately, such switched drive usually introduces noise. As will be shown, this undesirable consequence can be countered.

Figure 5 replaces the linearly operated current sink with a switching regulator. The Royer converter and its loop are as before; Figure 6's transistor collector waveshape (trace A) is similar to the other circuits. The high speed, switch mode current sink drive (trace B) efficiently feeds L1. This switched operation improves efficiency but degrades output noise. Figure 7 shows switching regulator harmonic clearly responsible for 3mV peak to peak output noise – about 30 times greater than the linearly operated circuits.

Careful examination of Figure 7 reveals almost no Royer based residue. The noise is dominated by switching regulator artifacts. Eliminating this switching regulator originated noise while maintaining efficiency requires special circuitry but is readily achievable.

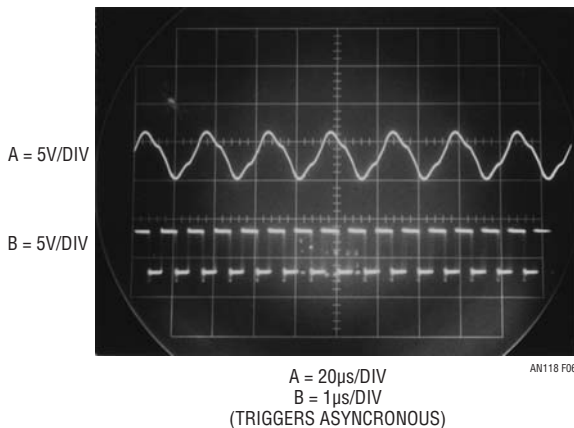


Figure 6. Resonant Royer Collector Waveshape (Trace A) is Similar to Previous Circuits. High Speed, Switched Mode Current Sink Drive (Trace B) Efficiency Feeds L1

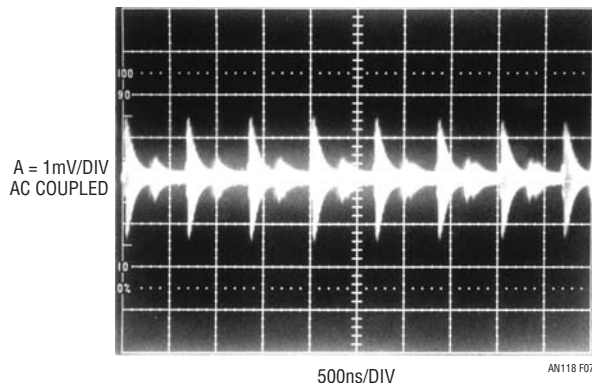


Figure 7. Switching Regulator Harmonic Results in 3mV_{p,p} Output Noise

Application Note 118

Low Noise Switching Regulator Driven Resonant Royer Converters

Figure 8 exemplifies the aforementioned “special circuitry”. The resonant Royer converter and its loop are reminiscent of previous circuits. The fundamental difference is the LT1534 switching regulator which utilizes controlled transition times to retard high frequency harmonic while maintaining efficiency. This approach blends switching and linear current sink benefits⁴. Voltage and current transition rate, set by R_V and R_I respectively, is a compromise between efficiency and noise reduction.

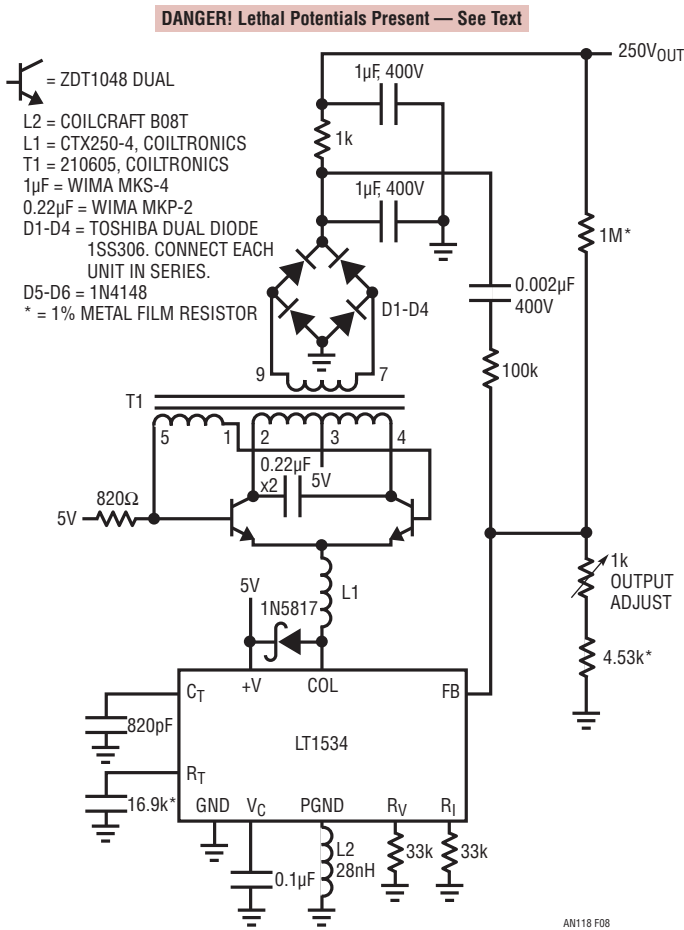


Figure 8. LT1534’s Controlled Transition Times Retard High Frequency Harmonic and Maintain Low Heat Dissipation. Approach Blends Switching and Linear Current Sink Benefits

Figure 9’s Royer collector wavscape (trace A) is nearly identical to the one produced by Figure 5’s circuit. Trace B, depicting LT1534 controlled transition times, markedly departs from its Figure 5 counterpart. These controlled transition times dramatically reduce output noise (Figure 10) to $150\mu\text{V}_{\text{P-P}}$ — a 20x improvement vs Figure 7’s LTC3401 based results.

Note 4. As stated, this forum must suffer brevity to maintain focus. The LT1534’s controlled transition time operation mandates further study. See Reference 3.

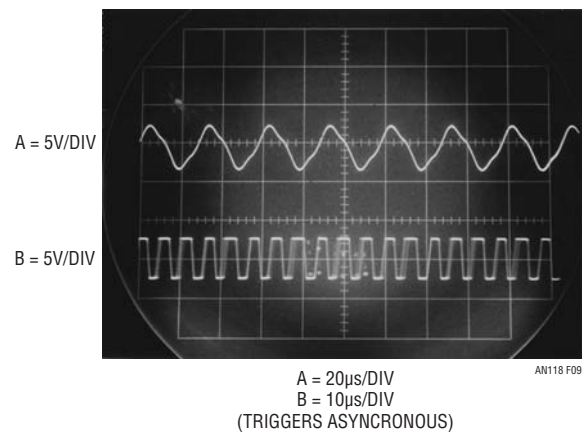


Figure 9. Resonant Royer Collector Wavscape (Trace A) is Identical to Figure 5’s LT3401 Circuit; LT1534 Current Sink’s Controlled Transition Times (Trace B) Attenuate High Frequency Harmonic

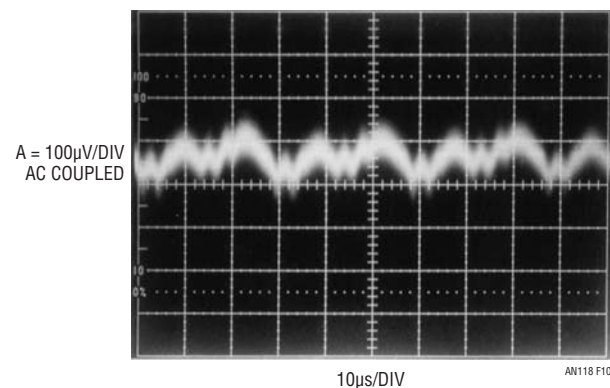


Figure 10. Switched Current Sinks Controlled Transition Times Dramatically Lower Noise to $150\mu\text{V}_{\text{P-P}}$ —A 20x Improvement vs Figure 7’s LTC3401 Results

Figure 11 is essentially identical to Figure 8 except that it produces a negative 1000V output. A1 provides low impedance, inverting feedback to the LT1534. Figure 12a's output noise measures inside 1mV. As before, resonant Royer ripple dominates the noise — no high frequency content is detectable. It is worth noting that this noise

figure proportionally improves with increased filter capacitor values. For example, Figure 12b indicates only 100µV noise with filter capacitor values increased by 10x, although capacitor physical size is large. The original values selected represent a reasonable compromise between noise performance and physical size.

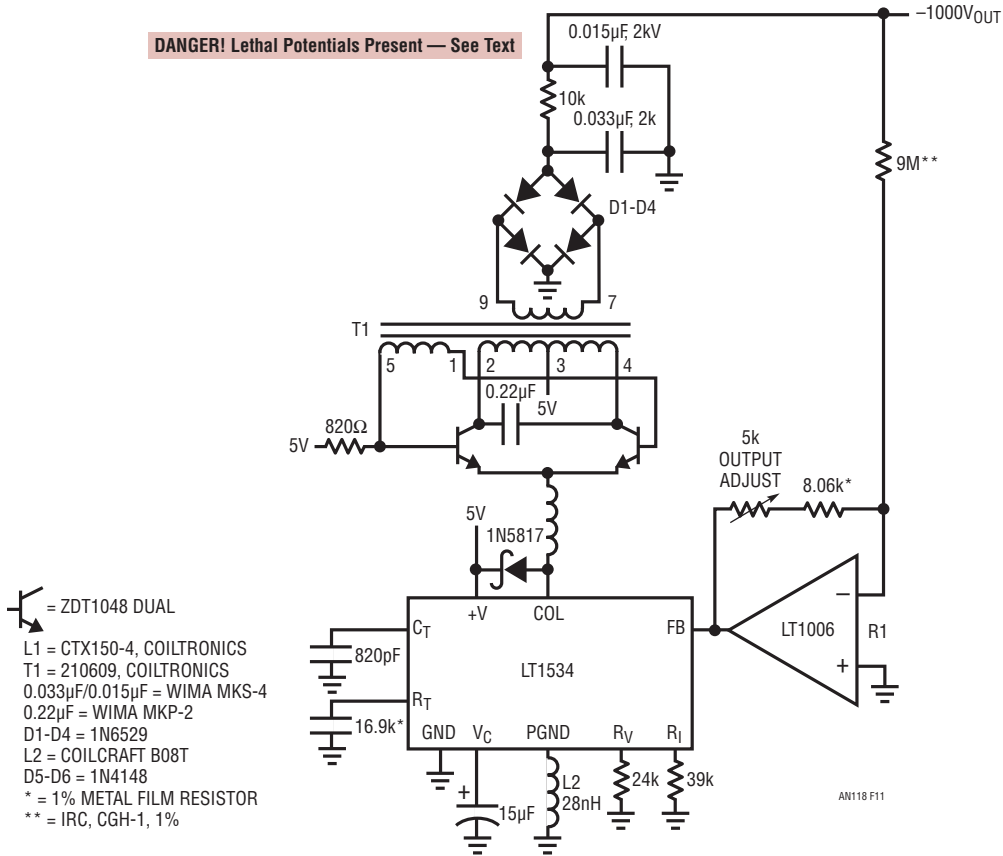


Figure 11. Controlled Transition Time Switching Regulator Applied to a Negative Output, 1000V Converter. A1 Provides Low Impedance, Inverting Feedback to LT1534

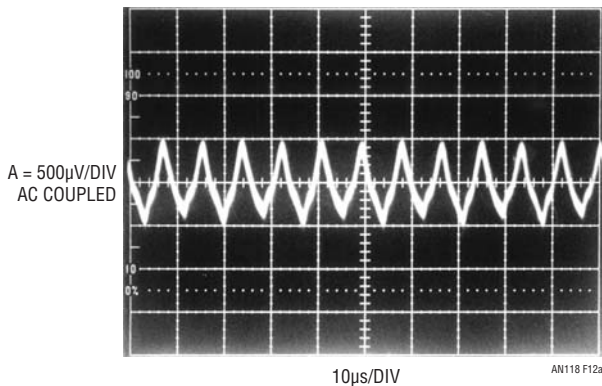


Figure 12a. -1000V Converter Output Noise Measures Inside 1mV (1PPM-0.0001%) in 100MHz Bandwidth. Resonant Royer Related Ripple Dominates Residue— No High Frequency Content is Detectable

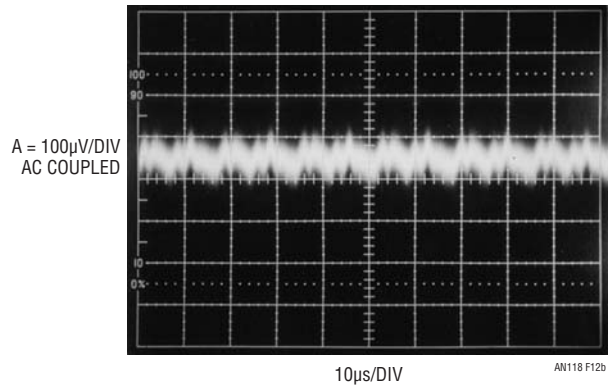


Figure 12b. 10x Increase in Figure 11's Filter Capacitor Values Reduces Noise to 100µV. Penalty is Capacitor Physical Size

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Application Note 118

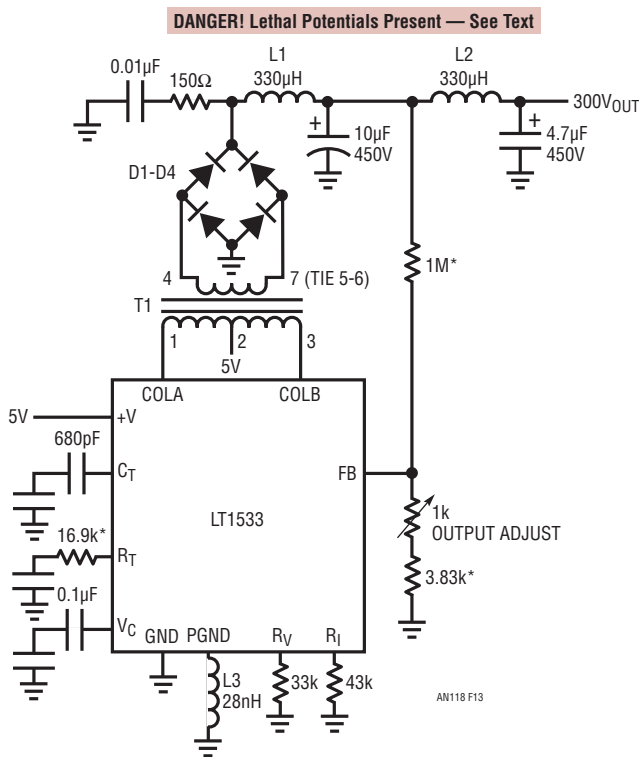
Controlled Transition Push-Pull Converters

Controlled transition techniques are also directly applicable to push-pull architectures. Figure 13 uses a controlled transition push-pull regulator in a simple loop to control a 300V output converter. Symmetrical transformer drive and controlled switching edge times promote low output noise. The D1-D4 connected damper further minimizes residual aberrations. In this case, inductors are used in the output filter although appropriate resistor values could be employed.

Figure 14 displays smooth transitions at the transformer secondary outputs (trace A is T1 Pin 4, trace B, T1 Pin 7). Absence of high frequency harmonic results in extremely low noise. Figure 15's fundamental related output residue approaches the $100\mu\text{V}$ measurement noise floor in a 100MHz bandpass. This is spectacularly low noise

performance in any DC/DC converter and certainly in one providing high voltage. Here, at 300V output, noise represents less than 1 part in 3 million.

Figure 16 is similar except that output range is variable from 0V to 300V. The LT1533 is replaced by an LT3439 which contains no control elements. It simply drives the transformer with 50% duty cycle, controlled switching transitions. Feedback control is enforced by A1-Q1-Q2 driving current into T1's primary center tap. A1 compares a resistively derived portion of the output with a user supplied control voltage. The values shown produce a 0V to 300V output in response to a 0V to 1V control voltage. An RC network from Q2's collector to A1's positive input compensates the loop. Collector waveforms and output noise signature are nearly identical to Figure 13. Output noise is $100\mu\text{V}_{\text{P-P}}$ over the entire 0V to 300V output range.



* = 1% METAL FILM RESISTOR
 L3 = COILCRAFT B08T
 L1, L2 = COILCRAFT LPS5010-334MLB
 D1-D4 = 1N6529
 T1 = PICO 32195

Figure 13. A Push-Pull Drive, Controlled Transition, 300V Output Converter. Symmetrical Transformer Drive and Slow Edges Promote Low Output Noise

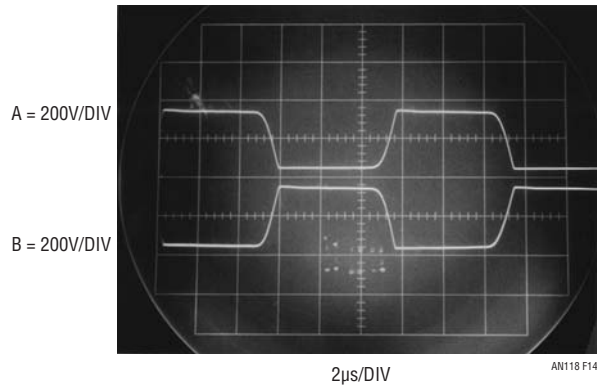


Figure 14. Transformer Secondary Outputs Show No High Frequency Artifacts

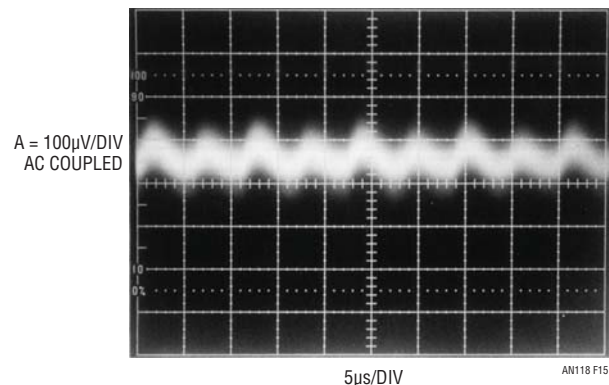


Figure 15. Push-Pull Converter Related Residue Approaches $100\mu\text{V}$ Measurement Noise Floor. No Wideband Components Appear in 100MHz Measurement Bandpass

Flyback Converters

Flyback converters, due to their abrupt, poorly controlled energy delivery, are not usually associated with low noise output. However, careful magnetic selection and layout can provide surprisingly good performance, particularly at low output current.

Figure 17's design provides 200V from a 5V input⁵. The scheme is a basic inductor flyback boost regulator with some important deviations. Q1, a high voltage device, has been interposed between the LT1172 switching regulator and the inductor. This permits the regulator to control Q1's high voltage switching without undergoing high

voltage stress. Q1, operating as a "cascode" with the LT1172's internal switch, withstands L1's high voltage flyback events⁶.

Diodes associated with Q1's source terminal clamp L1 originated spikes arriving via Q1's junction capacitance. The high voltage is rectified and filtered, forming the circuit's output. The ferrite bead, 100Ω and 300Ω resistors aid filter

Note 5. LTC application note veterans, a weary crew, will recognize material in this section from AN98 and AN113. The original circuits and text have been modified as necessary to suit low noise operation. See References.

Note 6. See References 13-17 for historical perspective and study on cascodes.

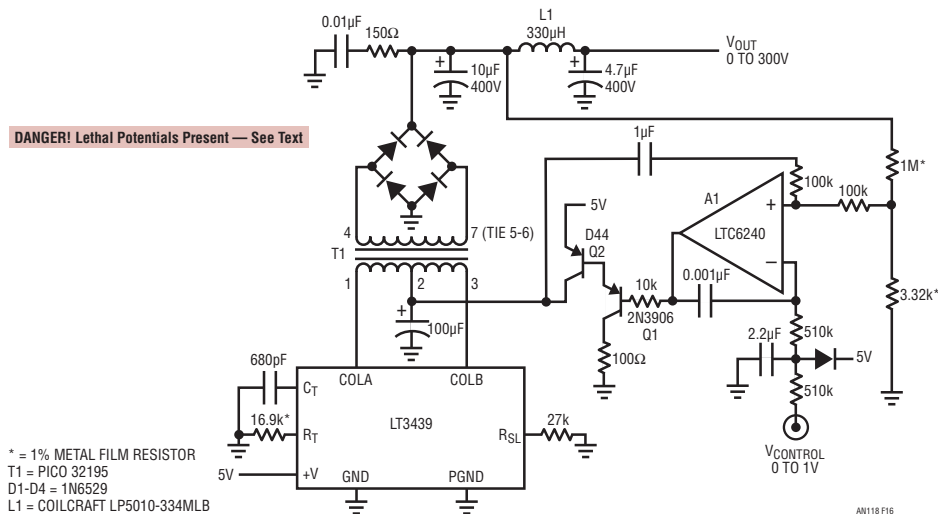


Figure 16. Full Range Adjustable Version of Figure 13. $V_{CONTROL}$ Directed A1 Sets T1 Drive Via Q1-Q2. 1M-3.32k Divider Provides Feedback, Stabilized by A1's Input Capacitors. Waveforms Are Similar to Figure 13. Output Noise is 100μV_{p-p}

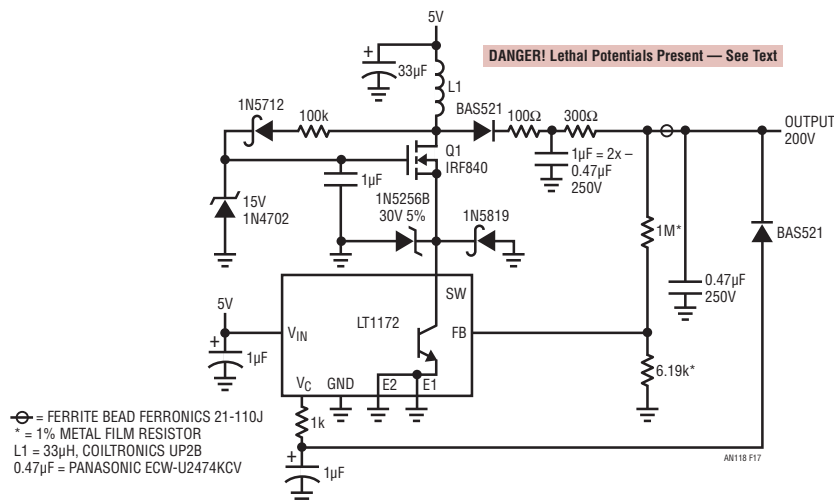


Figure 17. 5V to 200V Output Converter. Cascoded Q1 Switches High Voltage, Allowing Low Voltage Regulator to Control Output. Diode Clamps Protect Regulator from Transients; 100k Path Bootstraps Q1's Gate Drive from L1's Flyback Events. Output Connected 300Ω-Diode Combination Provides Short-Circuit Protection. Ferrite Bead, 100Ω and 300Ω Resistors Minimize High Frequency Output Noise

an118fa

Application Note 118

efficiency⁷. Feedback to the regulator stabilizes the loop and the V_C pin network provides frequency compensation. A 100k path from L1 bootstraps Q1's gate drive to about 10V, ensuring saturation. The output connected diode provides short-circuit protection by shutting down the LT1172 if the output is accidentally grounded.

Figure 18's traces A and C are LT1172 switch current and voltage, respectively. Q1's drain is trace B. Current ramp termination results in a high voltage flyback event at Q1's drain. A safely attenuated version of the flyback appears at the LT1172 switch. The sinusoidal signature, due to inductor ring-off between conduction cycles, is harmless.

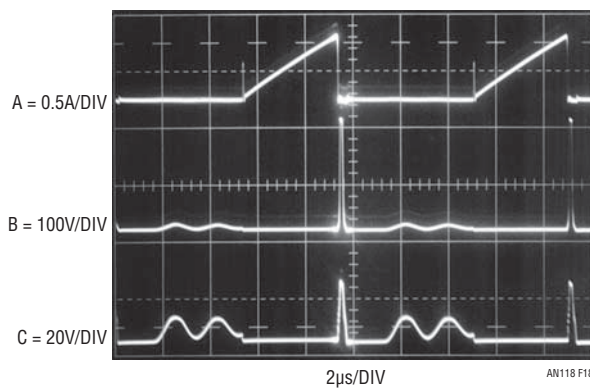


Figure 18. Waveforms for 5V to 200V Converter Include LT1172 Switch Current and Voltage (Traces A and C, Respectively) and Q1's Drain Voltage (Trace B). Current Ramp Termination Results in High Voltage Flyback Event at Q1 Drain. Safely Attenuated Version Appears at LT1172 Switch. Sinusoidal Signature, Due to Inductor Ring-Off Between Current Conduction Cycles, is Harmless. All Traces Intensified Near Center Screen for Photographic Clarity

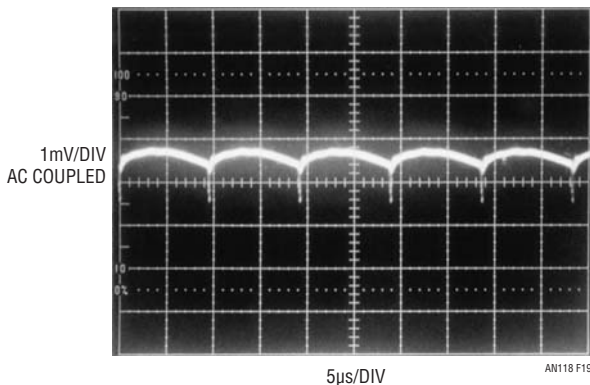


Figure 19. Figure 17's Output Noise, Composed of Low Frequency Ripple and Wideband, Flyback Related Spikes, Measures 1mV_{p-p} in 100MHz Bandpass

Figure 19, output noise, is composed of low frequency ripple and wideband, flyback related spikes measuring 1mV_{p-p} in a 100MHz bandpass.

Figure 20, contributed by Albert M. Wu of LTC, is a transformer coupled flyback circuit. The transformer secondary provides voltage step-up referred to the flyback driven primary. The 4.22M resistor supplies feedback to the regulator, closing a control loop. A 10k-0.68µF filter network attenuates high frequency harmonic with minimal voltage drop. Flyback related transients are clearly visible in Figure 21's output noise although within 300µV_{p-p}.

Note 7. Tutorial on ferrite beads appears in Appendix F.

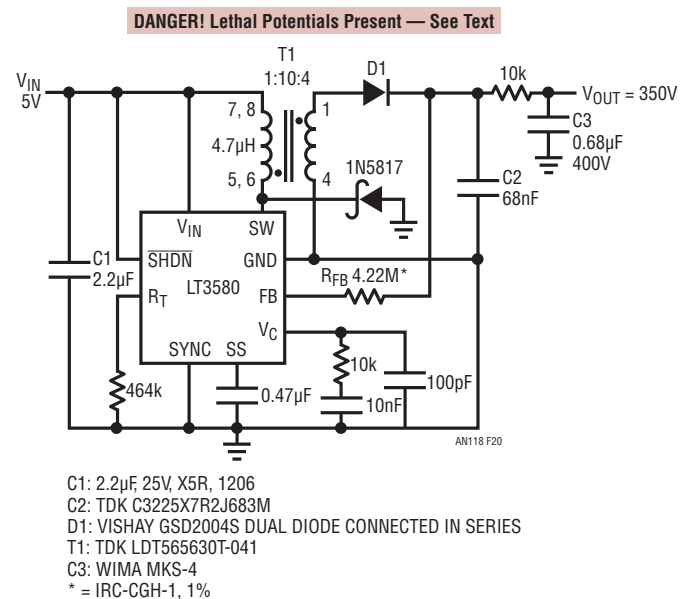


Figure 20. 5V Powered Transformer Coupled Flyback Converter Produces 350V Output

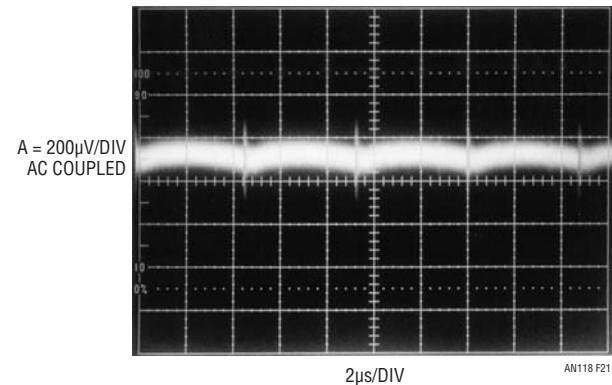


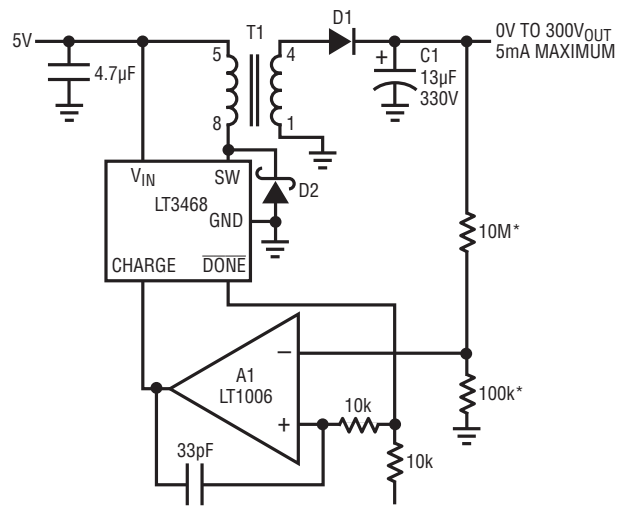
Figure 21. High Speed Transients in Figure 20's Noise Signature are Within 300µV_{p-p}

Figure 22 employs the LT3468 photoflash capacitor charger as a general purpose high voltage DC/DC converter. Normally, the LT3468 regulates its output at 300V by sensing T1's flyback pulse characteristic. This circuit allows the LT3468 to regulate at lower voltages by truncating its charge cycle before the output reaches 300V. A1 compares a divided down portion of the output with the program input voltage. When the program voltage (A1 + input) is exceeded by the output derived potential (A1 - input) A1's output goes low, shutting down the LT3468. The feedback capacitor provides AC hysteresis, sharpening A1's output to prevent chattering at the trip point. The LT3468 remains shut down until the output voltage drops low enough to trip A1's output high, turning it back on. In this way, A1 duty cycle modulates the LT3468, causing the output voltage to stabilize at a point determined by the program input.

Figure 23's 250V DC output (Trace B) decays down about 2V until A1 (Trace A) goes high, enabling the LT3468 and restoring the loop. This simple circuit works well, regulating over a programmable 0V to 300V range, although its inherent hysteretic operation mandates the (unacceptable) 2V output ripple noted. Loop repetition rate varies with input voltage, output set point and load but the ripple is always present. The following circuit greatly reduces ripple amplitude although complexity increases.

Figure 24's post-regulator reduces Figure 22's output ripple and noise to only 2mV. A1 and the LT3468 are identical to the previous circuit, except for the 15V zener diode in series with the 10M-100k feedback divider. This component causes C1's voltage, and hence Q1's collector, to regulate 15V above the $V_{PROGRAM}$ input dictated point. The $V_{PROGRAM}$ input is also routed to the A2-Q2-Q1 linear post-regulator. A2's 10M-100k feedback divider does not include a zener, so the post-regulator follows the $V_{PROGRAM}$ input with no offset. This arrangement forces 15V across Q1 at all output voltages. This figure is high enough to eliminate undesirable ripple and noise from the output while keeping Q1 dissipation low.

Q3 and Q4 form a current limit, protecting Q1 from overload. Excessive current through the 50Ω shunt turns Q3 on. Q3 drives Q4, shutting down the LT3468. Simultaneously, a portion of Q3's collector current turns Q2 on hard, shutting off Q1. This loop dominates the normal regulation feedback, protecting the circuit until the overload is removed.



- *1% METAL FILM RESISTOR
 - C1: RUBYCON 330FW13AK6325
 - D1: TOSHIBA DUAL DIODE 1SS306,
CONNECT DIODES IN SERIES
 - D2: PANASONIC MA2Z720
 - T1: TDK LDT565630T-002
- AN118 F22

Figure 22. A Voltage Programmable 0V to 300V Output Regulator. A1 Controls Regulator Output by Duty Cycle Modulating LT3468/T1 DC/DC Converter Power Delivery

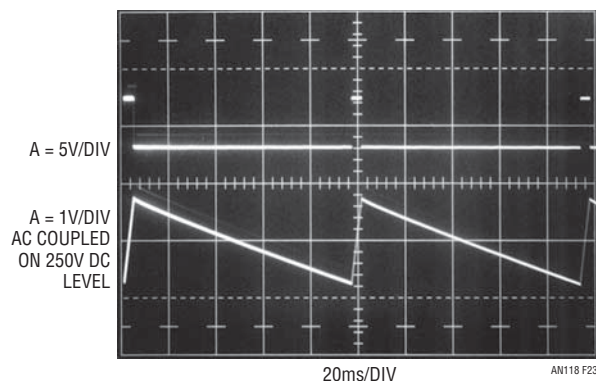
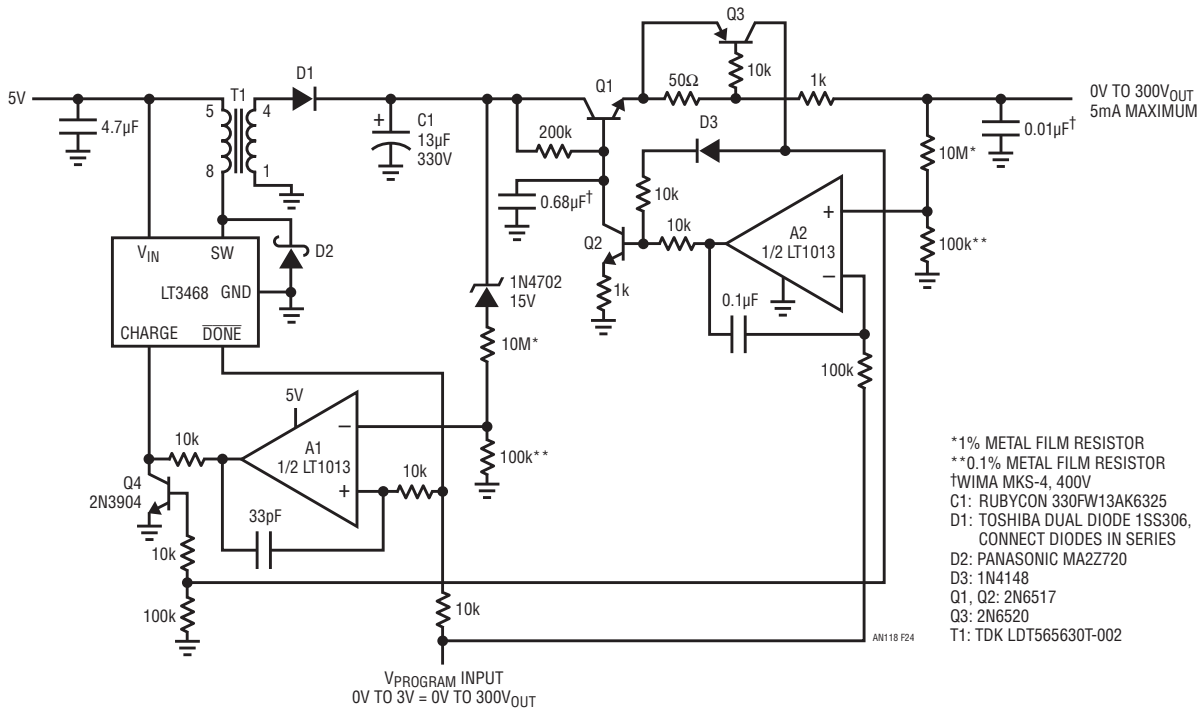


Figure 23. Details of Figure 22's Duty Cycle Modulated Operation. High Voltage Output (Trace B) Ramps Down Until A1 (Trace A) Goes High, Enabling LT3468/T1 to Restore Output. Loop Repetition Rate Varies with Input Voltage, Output Set Point and Load

DANGER! Lethal Potentials Present — See Text



- *1% METAL FILM RESISTOR
- **0.1% METAL FILM RESISTOR
- †WIMA MKS-4, 400V
- C1: RUBYCON 330FW13AK6325
- D1: TOSHIBA DUAL DIODE 1SS306, CONNECT DIODES IN SERIES
- D2: PANASONIC MA2Z720
- D3: 1N4148
- Q1, Q2: 2N6517
- Q3: 2N6520
- T1: TDK LDT565630T-002

Figure 24. Post-Regulation Reduces Figure 22's 2V Output Ripple to 2mV. LT3468-Based DC/DC Converter, Similar to Figure 22, Delivers High Voltage to Q1 Collector. A2, Q1, Q2 Form Tracking, High Voltage Linear Regulator. Zener Sets Q1 V_{CE} = 15V, Ensuring Tracking with Minimal Dissipation. Q3-Q4 Limit Short-Circuit Output Current

Figure 25 shows just how effective the post regulator is. When A1 (trace A) goes high, Q1's collector (trace B) ramps up in response (note LT3468 switching artifacts on ramps upward slope). When the A1-LT3468 loop is satisfied, A1 goes low and Q1's collector ramps down. The output post-regulator (trace C), however, rejects the ripple, showing only 2mV of noise. Slight trace blurring, right of photo center, derives from A1-LT3468 loop jitter.

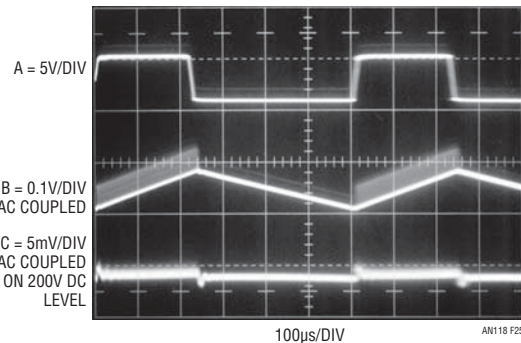


Figure 25. Low Ripple Output (Trace C) is Apparent in Post-Regulator's Operation. Traces A and B are A1 Output and Q1's Collector, Respectively. Trace Blurring, Right of Photo Center, Derives from Loop Jitter

Summary of Circuit Characteristics

Figure 26 summarizes the circuits presented with salient characteristics noted. This chart is only a generalized guideline and not an indicator of capabilities or limits. There are too many variables and exceptions to accommodate the categorical statement a chart implies. The interdependence of circuit parameters makes summarizing or rating various approaches a hazardous exercise. There is simply no intellectually responsible way to streamline the selection and design process if optimum results are desired. A meaningful choice *must* be the outcome of laboratory-based experimentation. There are just too many interdependent variables and surprises for a systematic,

theoretically based selection. Charts seek authority through glib simplification and simplification is Disaster's deputy. Nonetheless, Figure 26, in all its appropriated glory, lists input supply range, output voltage and current along with comments for each circuit⁸.

Note 8. Readers detecting author ambivalence at Figure 26's inclusion are not hallucinating. Locally based marketers champion such charts; the writer is less enthusiastic.

CIRCUIT TYPE	FIGURE NUMBER	SUPPLY RANGE (1mA LOAD)	MAXIMUM OUTPUT CURRENT AT TEST VOLTAGE	COMMENTS
LT1635 - Linear Resonant Royer	1	2.7V to 12V	2mA at 250V	<100 μ V Wideband Noise. Easily Voltage Controlled. Potential Dissipation Issue at High Supply Voltages.
LT1431 - Linear Resonant Royer	4	2.7V to 32V	2mA at 250V	<100 μ V Wideband Noise. Wide Supply Range. Potential Dissipation Issue at High Supply Voltages.
LT3401 - Switched Resonant Royer	5	2.7V to 5V	3.5mA at 250V	3mV Wideband Noise. High Output Current, Better Efficiency than Figures 1 and 4.
LT1534 - Switched Resonant Royer	8	2.7V to 15V	2mA at 250V	\approx 100 μ V Wideband Noise. Good Trade-Off Between Figures 1, 4 and 5.
LT1534 - Switched Resonant Royer	11	4.5V to 15V	1.2mA at -1000V	1mV Wideband Noise Reducable to 100 μ V. Negative 1000V Output Suits Photomultiplier Tubes.
LT1533 Push-Pull	13	2.7V to 15V	2mA at 300V	\approx 100 μ V Wideband Noise.
LT3439 Push-Pull	16	4.5V to 6V	2mA at 0V to 300V	Full Range Adjustable Version of Figure 13. \approx 100 μ V Wideband Noise.
LT1172 - Cascode Inductor Flyback	17	3.5V to 30V	2mA at 200V	V_{OUT} Limit \approx 200V. \approx 1mV Wideband Noise.
LT3580 - XFMR Flyback	20	2.7V to 20V	4mA at 350V	300 μ V Wideband Noise. Wide Supply Range. High Output Current. Small Transformer.
LT3468 - LT1006 XFMR Flyback	22	3.8V to 12V	5mA at 250V	1.5V Noise. Simple Voltage Control Input $0V_{IN}$ to $3V_{IN}$ = $0V_{OUT}$ - $300V_{OUT}$.
LT3468 - LT1013 XFMR Flyback - Linear	24	3.8V to 12V	5mA at 250V	2mV Wideband Noise. Voltage Control Input $0V_{IN}$ to $3V_{IN}$ = $0V_{OUT}$ to $300V_{OUT}$.

Figure 26. Summarized Characteristics of Techniques Presented. Applicable Circuit Depends on Application Specifics

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

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Application Note 118

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APPENDIX A

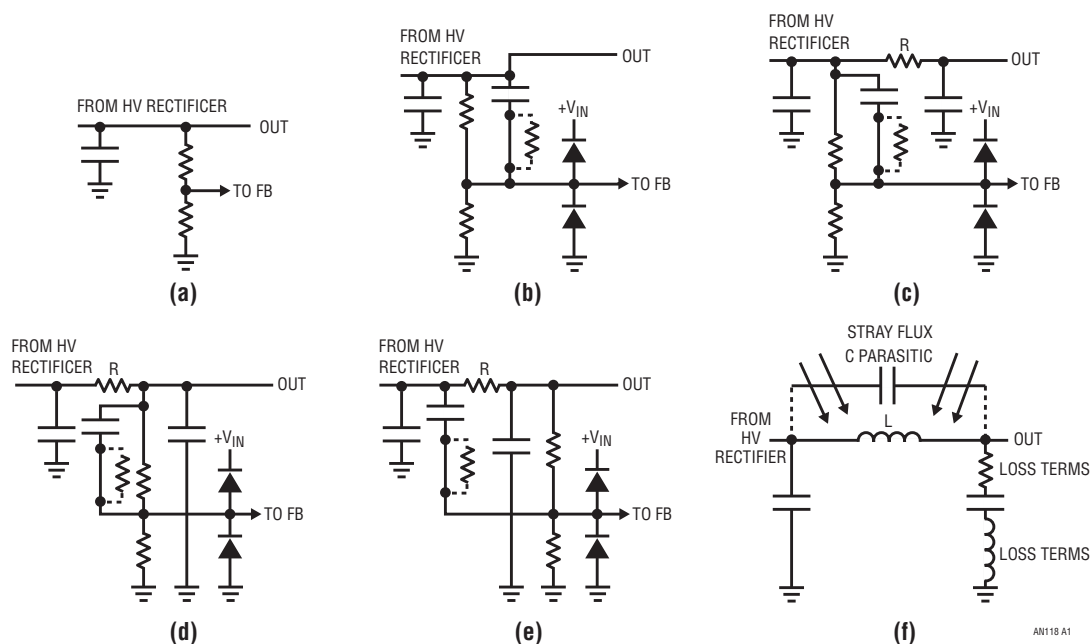


Figure A1. Feedback Network Options. (a) Is Basic DC Feedback. (b) Adds AC Lead Network for Improved Dynamics. Diode Clamps Protect Feedback Node from Capacitor's Differentiated Response. (c)'s Low Ripple Two Section Filter Slows Loop Transmission but Lead Network Provides Stability. Resistor R Sets DC Output Impedance. (d) Encloses R in DC Loop, Lowering Output Resistance. Feedback Capacitor Supplies Leading Response. (e) Moves Feedback Capacitor to Filter Input, Further Extending (d)'s Leading Response. (f), Replacing Filter Resistor (R) with Inductor, Lowers Output Resistance but Introduces Parasitic Shunt Capacitive Path and Stray Flux Sensitivity

Feedback Considerations in High Voltage DC/DC Converters

A high voltage DC/DC converter feedback network is a study in compromise. The appropriate choice is application dependent. Considerations include desired output impedance, loop stability, transient response and high

voltage induced overstress protection. Figure A1 lists typical options.

(a) is basic DC feedback and requires no special commentary. (b) adds an AC lead network for improved dynamics. Diode clamps protect the feedback node from the capacitors differentiated response. (c)'s low ripple,

two section filter slows transient response but a lead network provides stability. Resistor R, outside the loop, sets DC output impedance. (d) encloses R within the DC loop, lowering output resistance but delaying loop transmission. A feedback capacitor supplies corrective leading response. (e) moves the feedback capacitor to the filter input, further extending (d)'s leading response. (f) replaces filter resistor R with an inductor, lowering output resistance but introducing parasitic shunt capacitance which combines with capacitor loss terms to degrade filtering. The inductor also approximates a transformer secondary, vulnerable to stray flux pick-up with resulting increased output noise¹.

A common concern in any high voltage feedback network is reliability. Components must be quite carefully chosen. Voltage ratings should be conservative and strictly adhered to. While component ratings are easily ascertained, more subtle effects such as ill-suited board material and board

wash contaminants can be reliability hazards. Long term electro-migration effects can have undesirable results. Every potential unintended conductive path should be considered as an error source and layout planned accordingly. Operating temperature, altitude, humidity and condensation effects must be anticipated. In extreme cases, it may be necessary to rout the board under components operating at high voltage. Similarly, it is common practice to use several units in series to minimize voltage across the output connected feedback resistor. Contemporary packaging requirements emphasize tightly packed layout which may conflict with high voltage standoff requirements. This tradeoff must be carefully reviewed or reliability will suffer. The potentially deleterious (disastrous) effects of environmental factors, layout and component choice over time cannot be overstated. Clear thinking is needed to avoid unpleasant surprises.

Note 1. See Appendix G.

Editor's Note: Appendices B through E are thinly edited and modified versions of tutorials first appearing in AN70. Although originally intended to address controlled transition applications (e.g. LT1533, 4 and LT3439) the material is directly relevant and warrants inclusion here.

APPENDIX B

SPECIFYING AND MEASURING SOMETHING CALLED NOISE

Undesired output components in switching regulators are commonly referred to as "noise." The rapid, switched mode power delivery that permits high efficiency conversion also creates wideband harmonic energy. This undesirable energy appears as radiated and conducted components, or "noise." Actually switching regulator output "noise" isn't really noise at all, but coherent, high frequency residue directly related to the regulator's switching. Unfortunately, it is almost universal practice to refer to these parasitics as "noise," and this publication maintains this common, albeit inaccurate, terminology.¹

Measuring Noise

There are an almost uncountable number of ways to specify noise in a switching regulator's output. It is common industrial practice to specify peak-to-peak noise in

a 20MHz bandpass.² Realistically, electronic systems are readily upset by spectral energy beyond 20MHz, and this specification restriction benefits no one.³ Considering all this, it seems appropriate to specify peak-to-peak noise in a verified 100MHz bandwidth. Reliable low level measurements in this bandpass require careful instrumentation choice and connection practices.

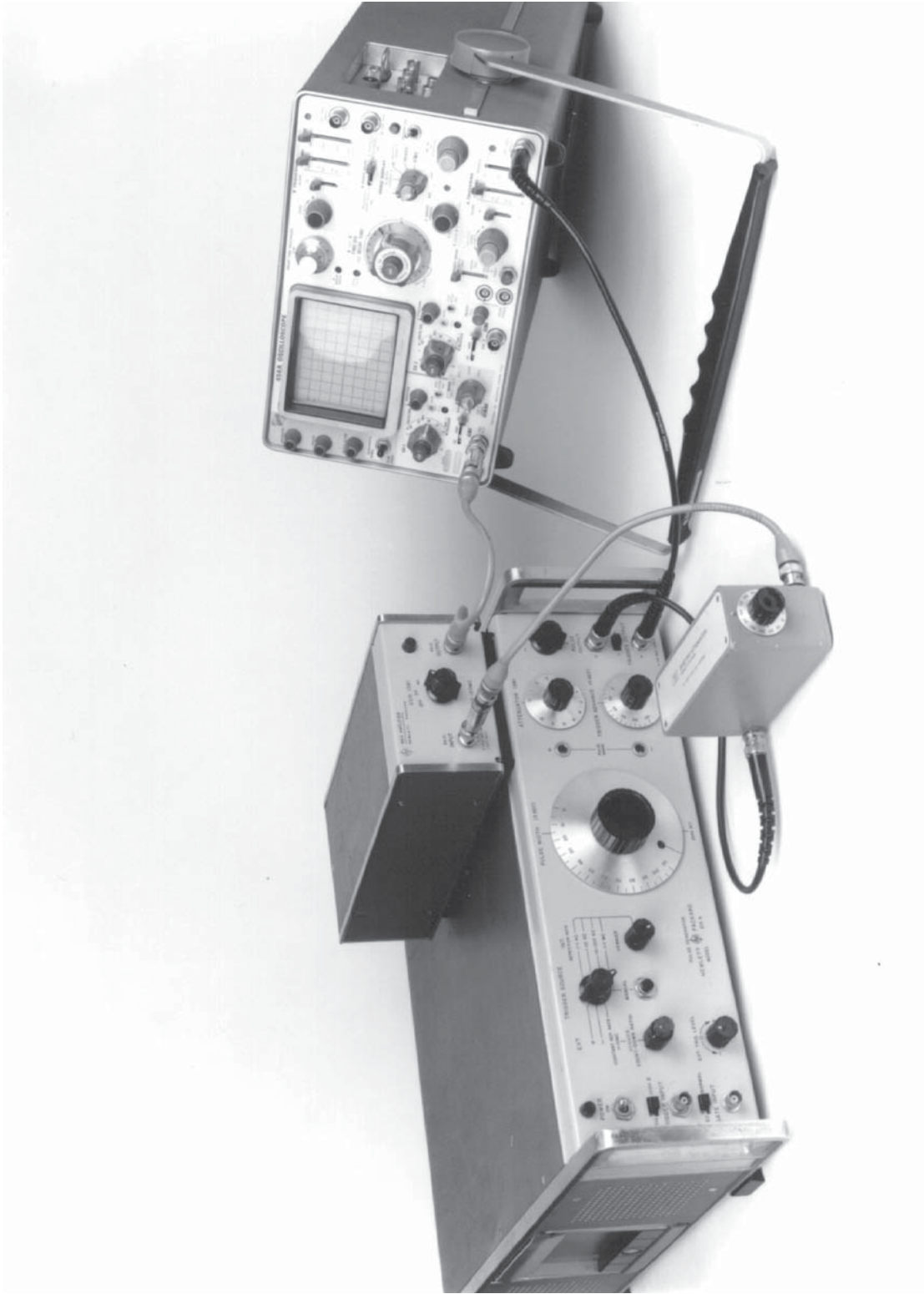
Our study begins by selecting test instrumentation and verifying its bandwidth and noise. This necessitates the arrangement shown in Figure B1. Figure B2 diagrams signal flow. The pulse generator supplies a subnanosec-

Note 1. Less genteelly, "If you can't beat 'em, join 'em."

Note 2. One DC/DC converter manufacturer specifies RMS noise in a 20MHz bandwidth. This is beyond deviousness and unworthy of comment.

Note 3. Except, of course, eager purveyors of power sources who specify them in this manner.

an118fa



**Figure B1. 100MHz Bandwidth Verification Test Setup.
Note Coaxial Connections for Wideband Signal Integrity**

ond rise time step to the attenuator, which produces a $<1\text{mV}$ version of the step. The amplifier takes 40dB of gain ($A = 100$) and the oscilloscope displays the result. The “front-to-back” cascaded bandwidth of this system should be about 100MHz ($t_{RISE} = 3.5\text{ns}$) and Figure B3 reveals this to be so. Figure B3’s trace shows 3.5ns rise

time and about $100\mu\text{V}$ of noise. The noise is limited by the amplifier’s 50Ω noise floor.⁴

Note 4. Observed peak-to-peak noise is somewhat affected by the oscilloscope’s “intensity” setting. Reference 11 describes a method for normalizing the measurement.

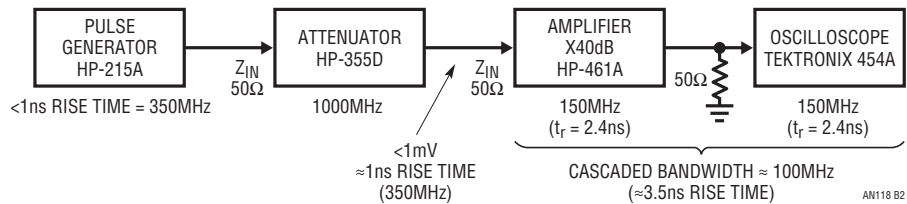


Figure B2. Subnanosecond Pulse Generator and Wideband Attenuator Provide Fast Step to Verify Test Setup Bandwidth

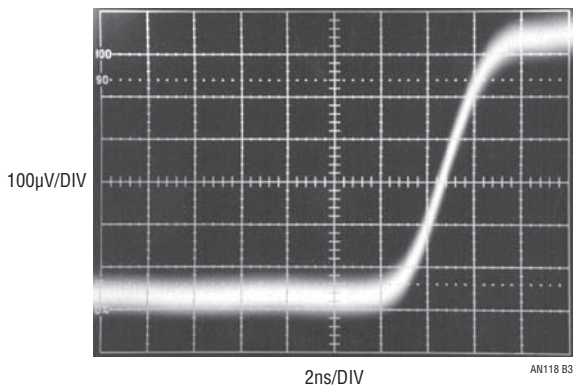


Figure B3. Oscilloscope Display Verifies Test Setup’s 100MHz (3.5ns Rise Time) Bandwidth. Baseline Noise Derives from Amplifier’s 50Ω Input Noise Floor

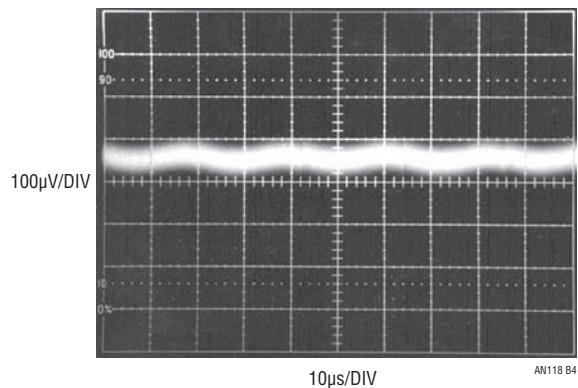


Figure B4. Output Switching Noise Is Just Discernible in a 100MHz Bandpass

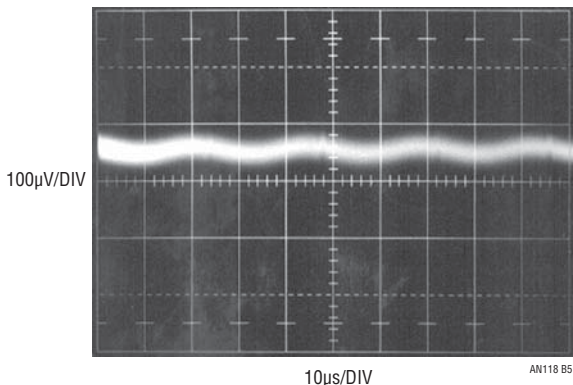


Figure B5. 10MHz Band Limited Version of Preceding Photo. All Switching Noise Information is Preserved, Indicating Adequate Bandwidth

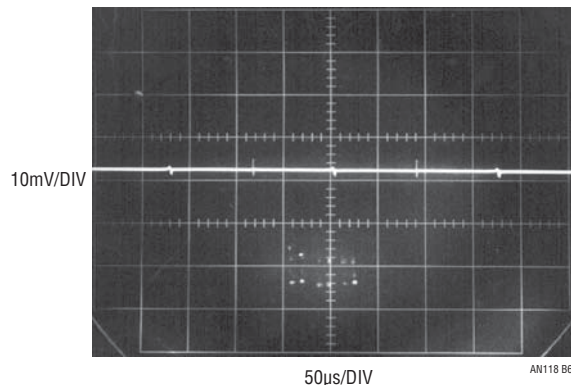


Figure B6. Commercially Available Switching Regulator’s Output Noise in a 1MHz Bandpass. Unit Appears to Meet its $5\text{mV}_{\text{P-P}}$ Noise Specification

Application Note 118

Figure B4's presentation of output noise shows barely visible switching artifacts (at vertical graticule lines 4, 6 and 8) in the 100MHz bandpass. Fundamental ripple is seen more clearly, although similarly noise floor dominated. Restricting measurement bandwidth to 10MHz (Figure B5) reduces noise floor amplitude, although switching noise and ripple amplitudes are preserved. This indicates that there is no signal power beyond 10MHz. Further measurements as bandwidth is successively reduced can determine the highest frequency content present.

The importance of measurement bandwidth is further illustrated by Figures B6 to B8. Figure B6 measures a commercially available DC/DC converter in a 1MHz bandpass. The unit appears to meet its claimed 5mV_{P-P} noise specification. In Figure B7, bandwidth is increased

to 10MHz. Spike amplitude enlarges to 6mV_{P-P}, about 1mV outside the specification limit. Figure B8's 50MHz viewpoint brings an unpleasant surprise. Spikes measure 30mV_{P-P}—six times the specified limit!⁵

Low Frequency Noise

Low frequency noise is rarely a concern, because it almost never affects system operation. Low frequency noise is shown in Figure B9. It is possible to reduce low frequency noise by rolling off control loop bandwidth. Figure B10 shows about a five times improvement when this is done, even with greater measurement bandwidth. A possible disadvantage is loss of loop bandwidth and slower transient response.

Note 5. Caveat Emptor.

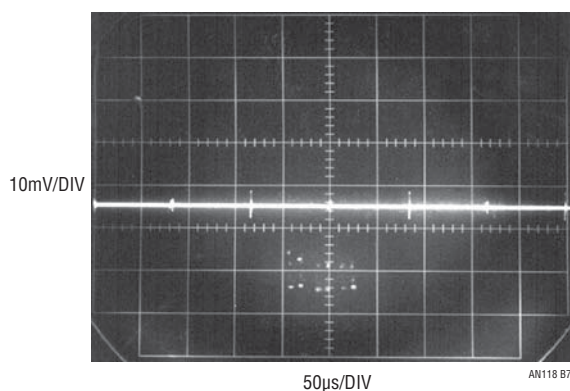


Figure B7. Figure B6's Regulator Noise in a 10MHz Bandpass. 6mV_{P-P} Noise Exceeds Regulator's Claimed 5mV Specification

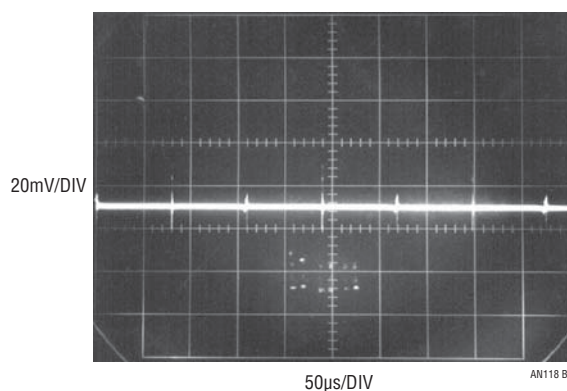


Figure B8. Wideband Observation of Figure B7 Shows 30mV_{P-P} Noise—Six Times the Regulator's Specification!

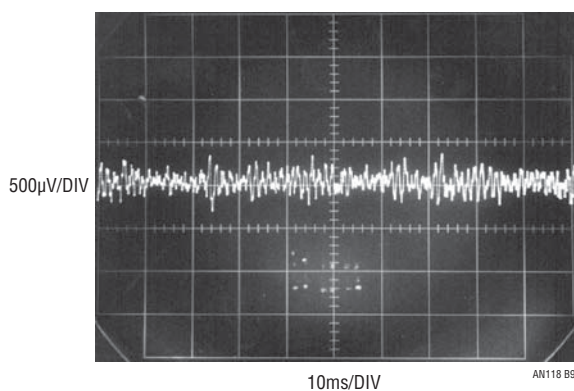


Figure B9. 1Hz to 3kHz Noise Using Standard Frequency Compensation. Almost All Noise Power is Below 1kHz

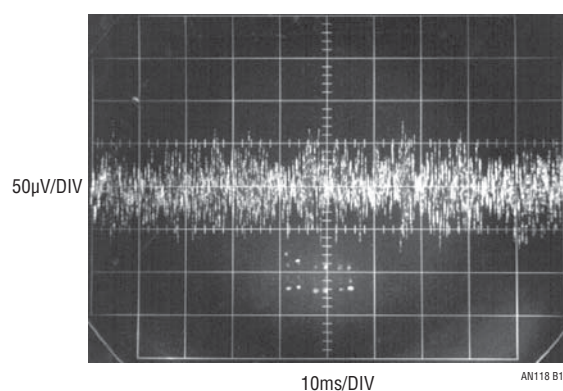


Figure B10. Feedback Lead Network Decreases Low Frequency Noise, Even as Measurement Bandwidth Expands to 100kHz

Preamplifier and Oscilloscope Selection

The low level measurements described require some form of preamplification for the oscilloscope. Current generation oscilloscopes rarely have greater than 2mV/DIV sensitivity, although older instruments offer more capability. Figure B11 lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These units feature wideband, low noise performance. It is particularly significant that the majority of these instruments are no longer produced. This is in keeping with current instrumentation trends, which emphasize digital signal acquisition as opposed to analog measurement capability.

The monitoring oscilloscope should have adequate bandwidth and exceptional trace clarity. In the latter regard high quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments is well-suited to low level noise measurement.⁶ The digitizing uncertainties and raster scan limitations of DSOs impose display resolution penalties. Many DSO displays will not even register the small levels of switching-based noise.

Note 6. In our work we have found Tektronix types 454, 454A, 547 and 556 excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise floor limited background.

INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	-3dB BANDWIDTH	MAXIMUM SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Amplifier	Hewlett-Packard	461A	175MHz	Gain = 100	Secondary Market	50Ω Input, Stand-Alone. 100μV _{P-P} (≈20μV RMS) noise in 100MHz bandwidth. Best of this group for noise measurement described in text.
Differential Amplifier	Tektronix	1A5	50MHz	1mV/DIV	Secondary Market	Requires 500 Series Mainframe
Differential Amplifier	Tektronix	7A13	100MHz	1mV/DIV	Secondary Market	Requires 7000 Series Mainframe
Differential Amplifier	Tektronix	11A33	150MHz	1mV/DIV	Secondary Market	Requires 11000 Series Mainframe
Differential Amplifier	Tektronix	P6046	100MHz	1mV/DIV	Secondary Market	Stand-Alone
Differential Amplifier	Preamble	1855	100MHz	Gain = 10	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Tektronix	1A7/1A7A	1MHz	10μV/DIV	Secondary Market	Requires 500 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	7A22	1MHz	10μV/DIV	Secondary Market	Requires 7000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	5A22	1MHz	10μV/DIV	Secondary Market	Requires 5000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	ADA-400A	1MHz	10μV/DIV	Current Production	Stand-Alone with Optional Power Supply, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 100	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Stanford Research Systems	SR-560	1MHz	Gain = 50000	Current Production	Stand-Alone, Settable Bandstops, Battery or Line Operation
Differential Amplifier	Tektronix	AM-502	1MHz	Gain = 100000	Secondary Market	Requires TM-500 Series Power Supply

Figure B11. Some Applicable High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Bandwidth, Sensitivity and Availability. All Require Protective Input Network to Prevent Catastrophic Failure. See Figure B12 and Associated Text

Application Note 118

Auxiliary Measurement Circuits

Figure B12 is the clamp circuit referred to in the preceding figure caption. It must be employed with any of Figure B12's amplifiers to insure protection against catastrophic overloading.⁷ The network is simply an AC coupled diode clamp. The coupling capacitor specified withstands the text examples high voltage outputs and the 10M resistors bleed residual capacitor charge. Built into a small BNC equipped enclosure, its output should be *directly* connected to the amplifier. 50Ω inputs may be directly driven; high impedance input amplifiers should be shunted with a coaxial 50Ω terminator.

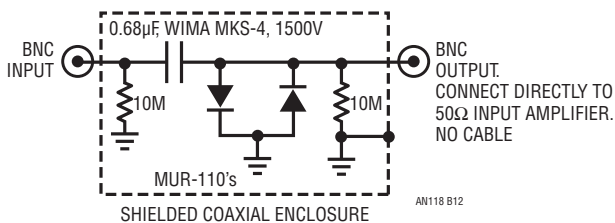


Figure B12. Coaxially Fixtured Clamp Protects Figure B11's Low Noise Amplifiers From High Voltage Inputs. Resistors Insure Capacitor Discharge

B13's battery powered, 1 MHz, 1mV square wave amplitude calibrator facilitates "end-to-end" amplifier—oscilloscope path gain verification. The 221k resistor associated area is sensitive to variations in stray capacitance and is shielded as per the schematic. A 4.5V reference stabilizes output amplitude against battery voltage change and a peaking trim optimizes front and trailing corner fidelity. Figure B14 shows that the simple peaking network does not quite achieve square corners, but 1mV pulse amplitude is clearly delineated. Trace thickening in the waveform flats indicates amplifier noise floor.

Note 7. Don't say we didn't warn you.

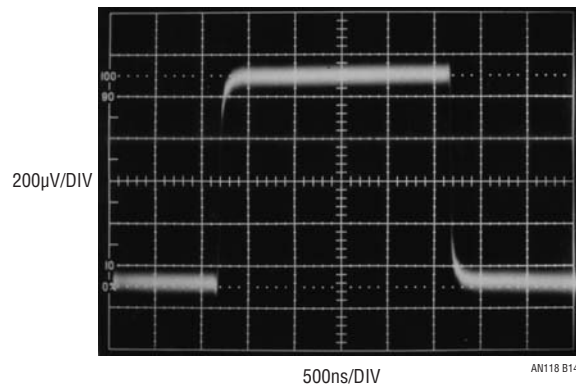


Figure B14. 1mV Amplitude Calibrator Output Has Minor Corner Rounding but Pulse Flats Indicate Desired Amplitude. Trace Thickening Describes Amplifier Noise Floor

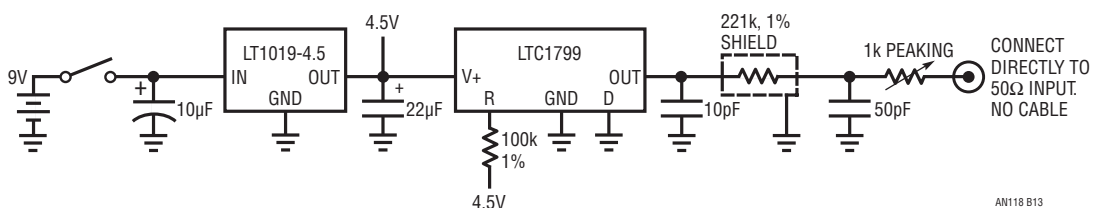


Figure B13. Battery Powered, 1MHz, 1mV Square Wave Amplitude Calibrator Permits Signal Path Gain Verification. Peaking Trim Optimizes Front and Trailing Corner Fidelity

APPENDIX C

PROBING AND CONNECTION TECHNIQUES FOR LOW LEVEL, WIDEBAND SIGNAL INTEGRITY

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. The low level, wideband measurements demand care in routing signals to test instrumentation.

Ground Loops

Figure C1 shows the effects of a ground loop between pieces of line-powered test equipment. Small current flow between test equipment's nominally grounded chassis creates 60MHz modulation in the measured circuit output.

This problem can be avoided by grounding all line powered test equipment at the same outlet strip or otherwise ensuring that all chassis are at the same ground potential.

Similarly, any test arrangement that permits circuit current flow in chassis interconnects must be avoided.

Pickup

Figure C2 also shows 60Hz modulation of the noise measurement. In this case, a 4-inch voltmeter probe at the feedback input is the culprit. *Minimize the number of test connections to the circuit and keep leads short.*

Poor Probing Technique

Figure C3's photograph shows a short ground strap affixed to a scope probe. The probe connects to a point which provides a trigger signal for the oscilloscope. Circuit output noise is monitored on the oscilloscope via the coaxial cable shown in the photo.

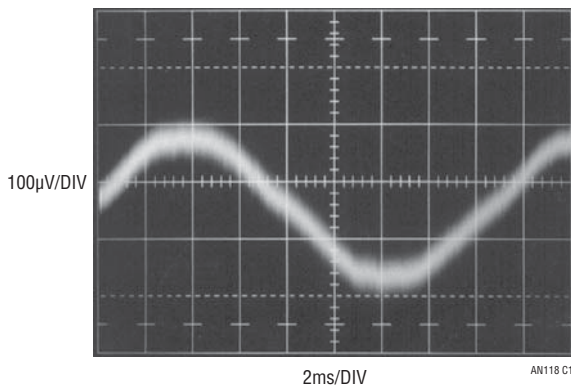


Figure C1. Ground Loop Between Pieces of Test Equipment Induces 60Hz Display Modulation

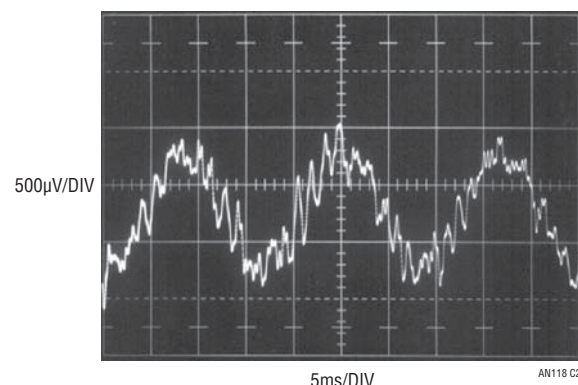


Figure C2. 60Hz Pickup Due to Excessive Probe Length at Feedback Node

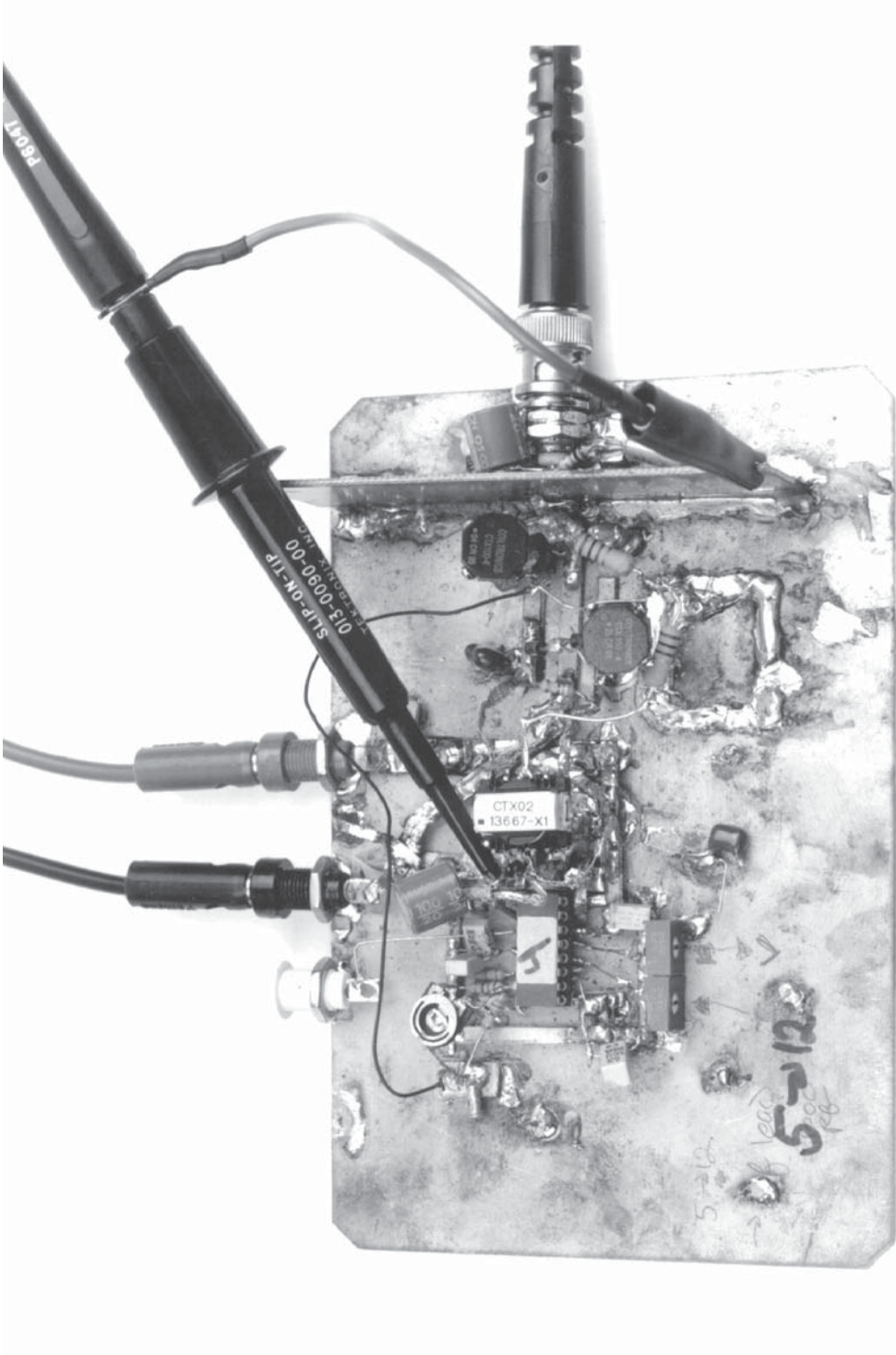


Figure C3. Poor Probing Technique. Trigger Probe Ground Lead Can Cause Ground Loop-Induced Artifacts to Appear in Display

Figure C4 shows results. A ground loop on the board between the probe ground strap and the ground referred cable shield causes apparent excessive ripple in the display. *Minimize the number of test connections to the circuit and avoid ground loops.*

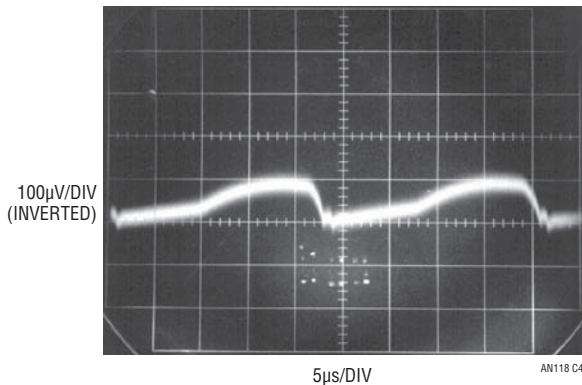


Figure C4. Apparent Excessive Ripple Results from Figure C3's Probe Misuse. Ground Loop on Board Introduces Serious Measurement Error

Violating Coaxial Signal Transmission—Felony Case

In Figure C5, the coaxial cable used to transmit the circuit output noise to the amplifier-oscilloscope has been replaced with a probe. A short ground strap is employed as the probe's return. The error inducing trigger channel probe in the previous case has been eliminated; the scope is triggered by a noninvasive, isolated probe.¹ Figure C6 shows excessive display noise due to breakup of the coaxial signal environment. The probe's ground strap violates coaxial transmission and the signal is corrupted by RF. *Maintain coaxial connections in the noise signal monitoring path.*

Violating Coaxial Signal Transmission—Misdemeanor Case

Figure C7's probe connection also violates coaxial signal flow, but to a less offensive extent. The probe's ground strap is eliminated, replaced by a tip grounding attachment. Figure C8 shows better results over the preceding case, although signal corruption is still evident. *Maintain coaxial connections in the noise signal monitoring path.*

Proper Coaxial Connection Path

In Figure C9, a coaxial cable transmits the noise signal to the amplifier-oscilloscope combination. In theory, this affords the highest integrity cable signal transmission. Figure C10's trace shows this to be true. The former examples aberrations and excessive noise have disappeared. The switching residuals are now faintly outlined in the amplifier noise floor. *Maintain coaxial connections in the noise signal monitoring path.*

Direct Connection Path

A good way to verify there are no cable-based errors is to eliminate the cable. Figure C11's approach eliminates all cable between breadboard, amplifier and oscilloscope. Figure C12's presentation is indistinguishable from Figure C10, indicating no cable-introduced infidelity. *When results seem optimal, design an experiment to test them. When results seem poor, design an experiment to test them. When results are as expected, design an experiment to test them. When results are unexpected, design an experiment to test them.*

Test Lead Connections

In theory, attaching a voltmeter lead to the regulator's output should not introduce noise. Figure C13's increased noise reading contradicts the theory. The regulator's output impedance, albeit low, is not zero, especially as frequency scales up. The RF noise injected by the test lead works against the finite output impedance, producing the 200µV of noise indicated in the figure. If a voltmeter lead must be connected to the output during testing, it should be done through a 10kΩ-10µF filter. Such a network eliminates Figure C13's problem while introducing minimal error in the monitoring DVM. *Minimize the number of test lead connections to the circuit while checking noise. Prevent test leads from injecting RF into the test circuit.*

Note 1. To be discussed. Read on.

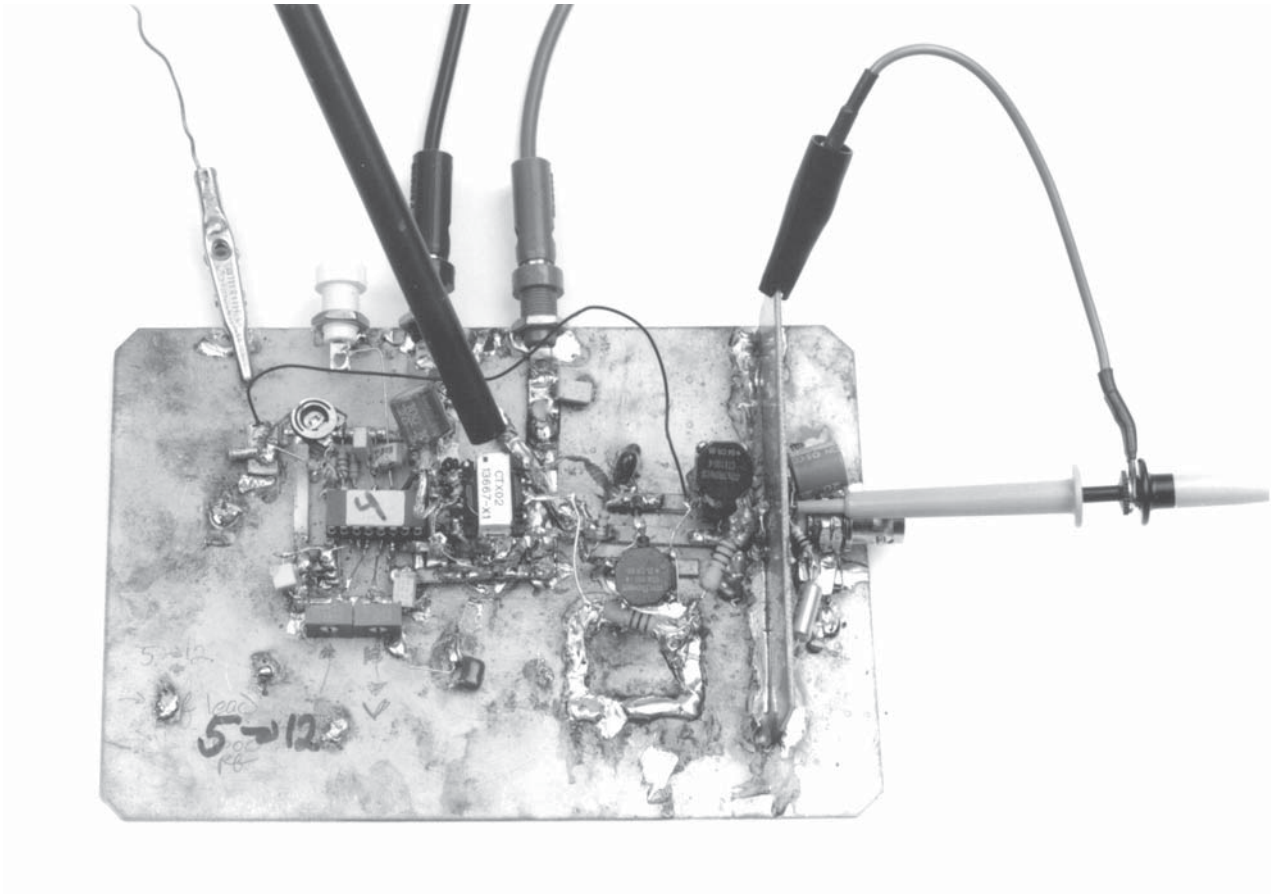


Figure C5. Floating Trigger Probe Eliminates Ground Loop, but Output Probe Ground Lead (Photo Upper Right) Violates Coaxial Signal Transmission

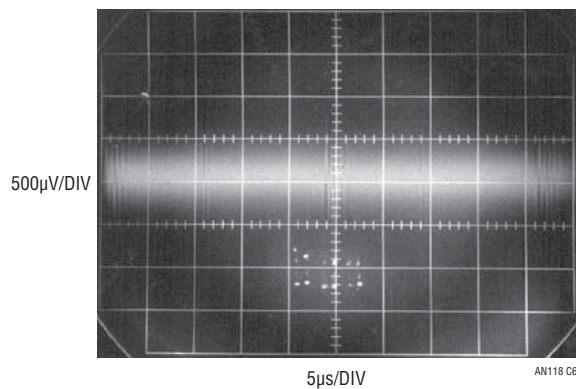


Figure C6. Signal Corruption Due to Figure C5's Noncoaxial Probe Connection

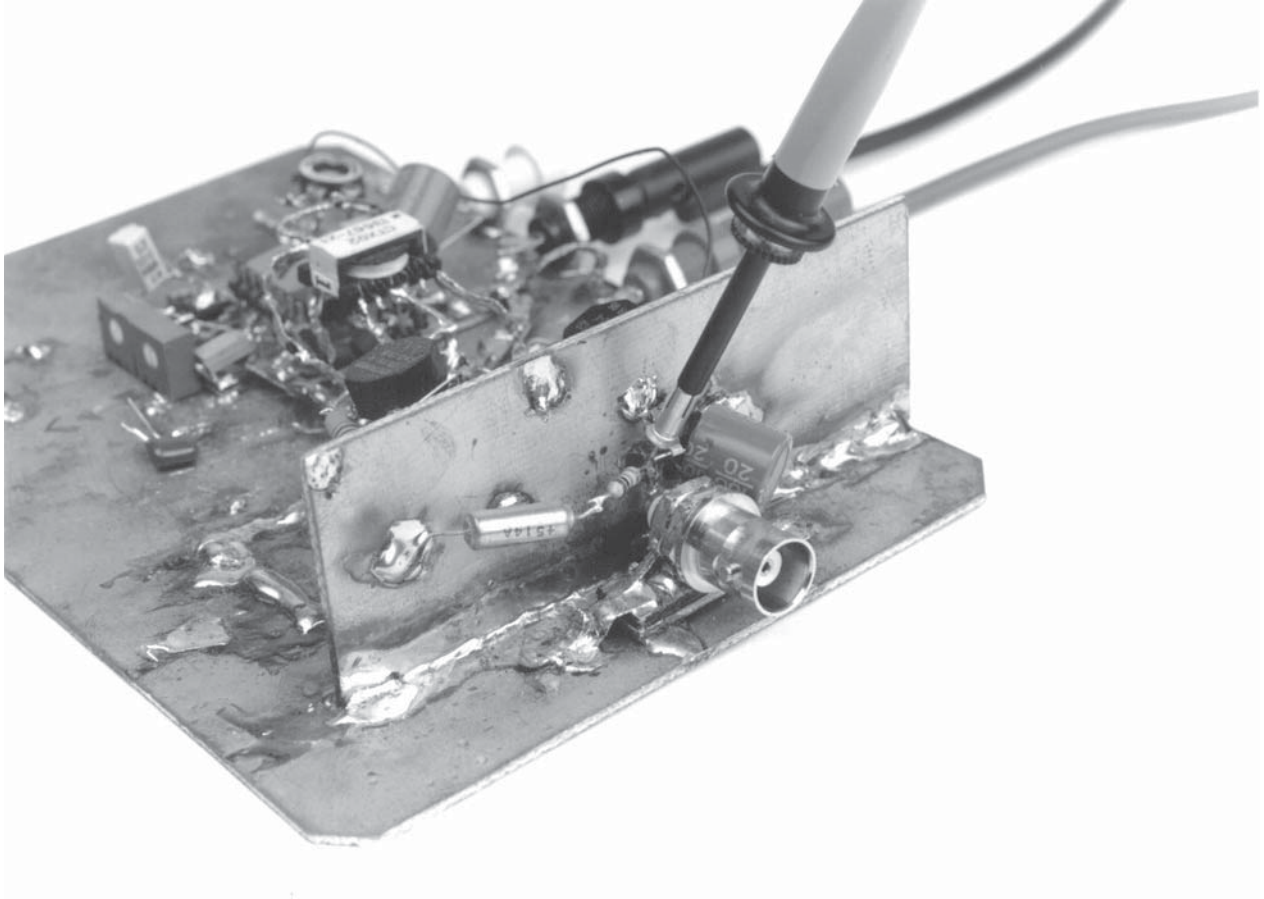


Figure C7. Probe with Tip Grounding Attachment Approximates Coaxial Connection

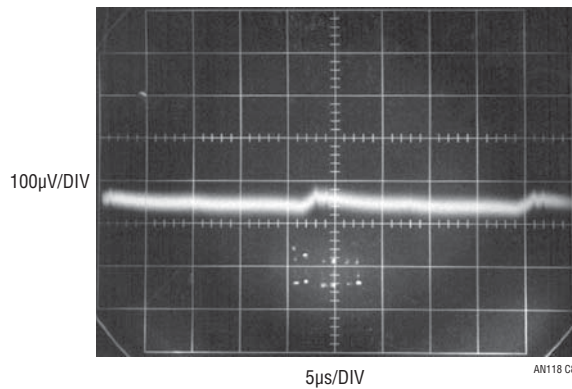


Figure C8. Probe with Tip Grounding Attachment Improves Results. Some Corruption Is Still Evident

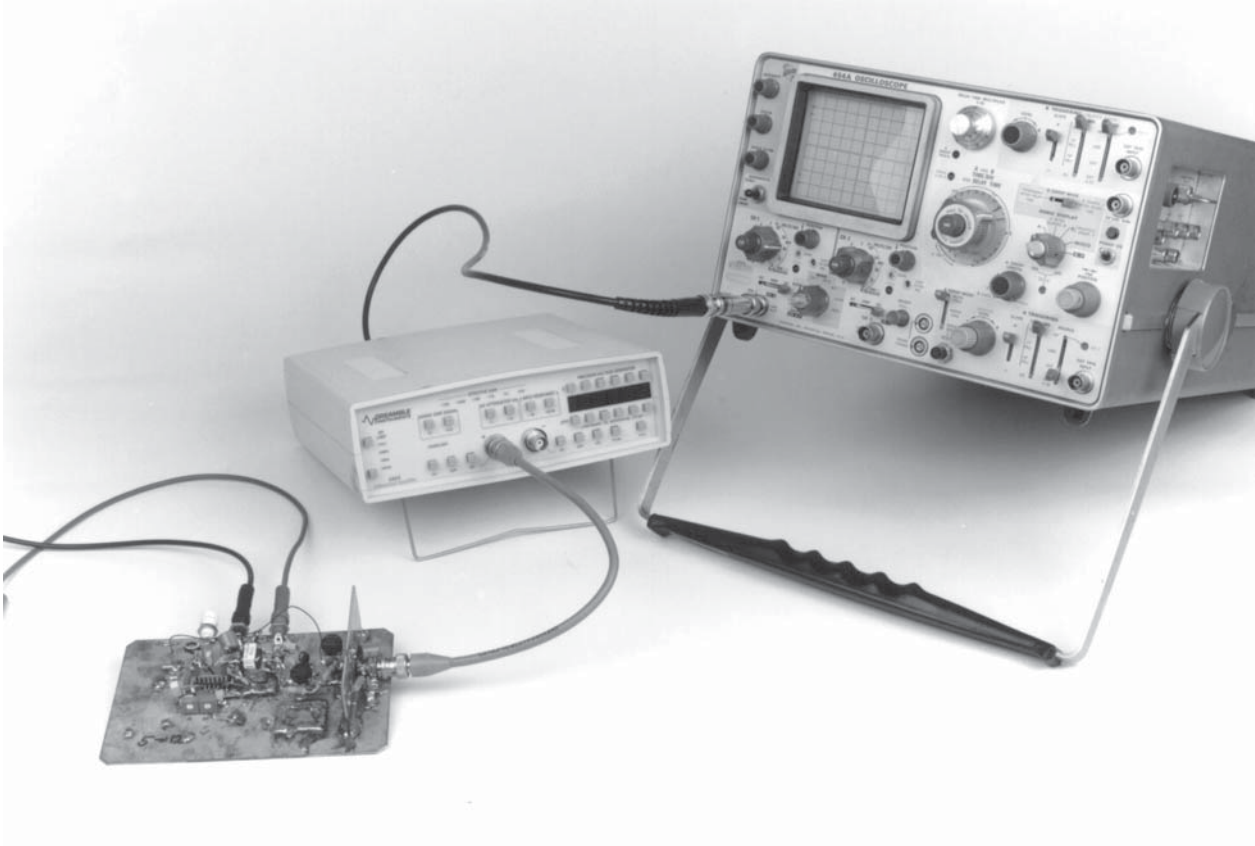


Figure C9. Coaxial Connection Theoretically Affords Highest Fidelity Signal Transmission

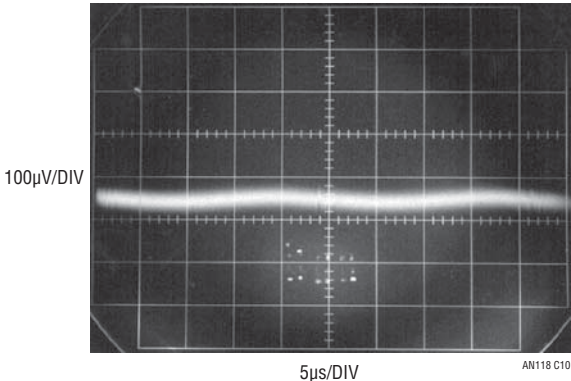


Figure C10. Life Agrees with Theory. Coaxial Signal Transmission Maintains Signal Integrity. Switching Residuals Are Faintly Outlined in Amplifier Noise

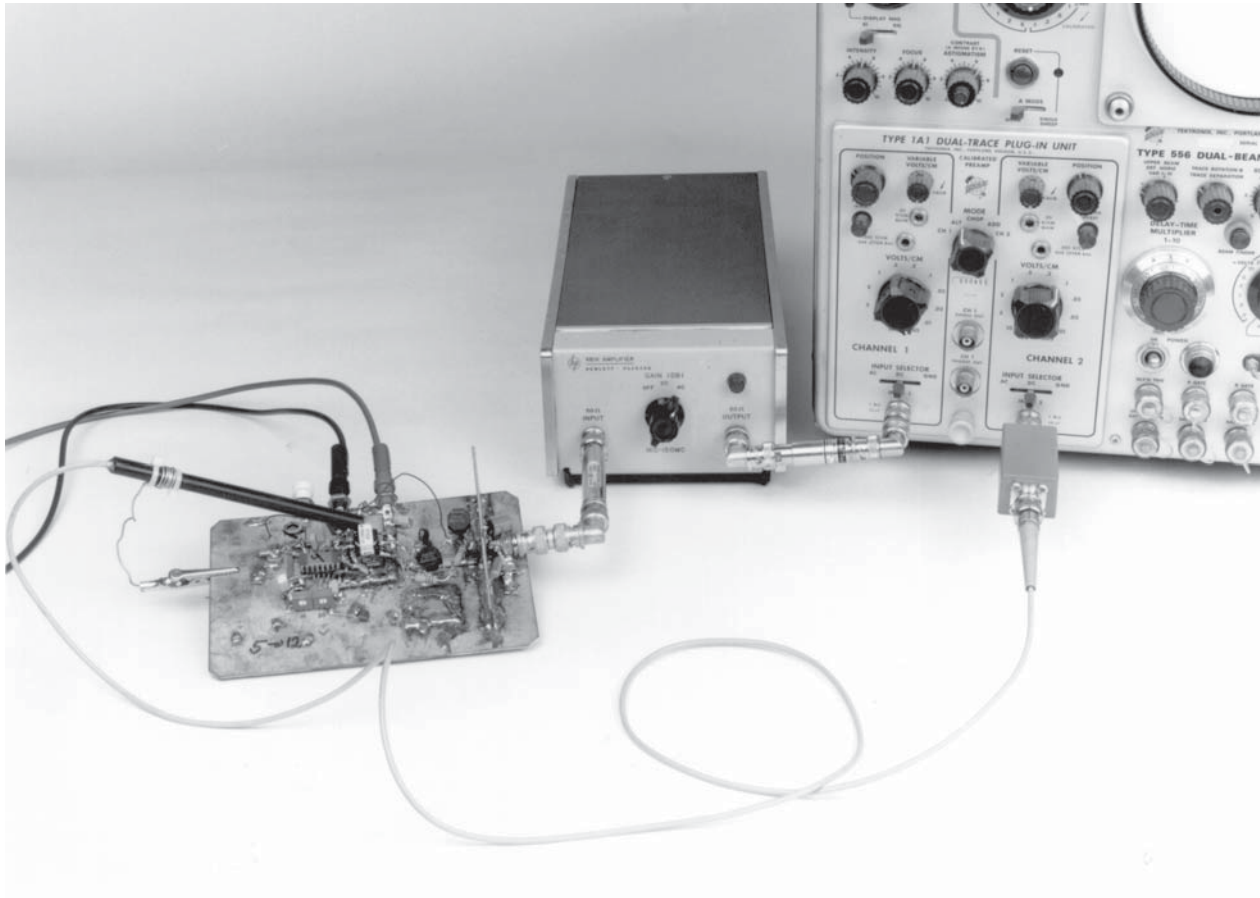


Figure C11. Direct Connection to Equipment Eliminates Possible Cable-Termination Parasitics, Providing Best Possible Signal Transmission

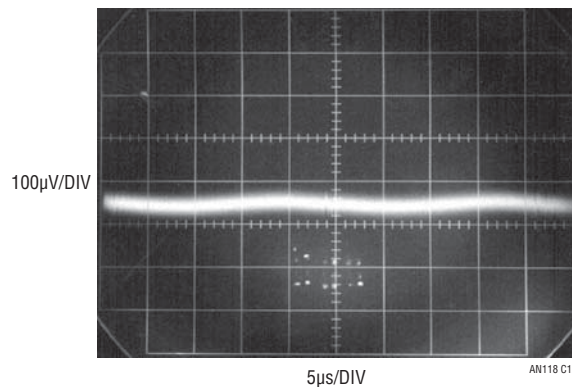


Figure C12. Direct Connection to Equipment Provides Identical Results to Cable-Termination Approach. Cable and Termination Are Therefore Acceptable

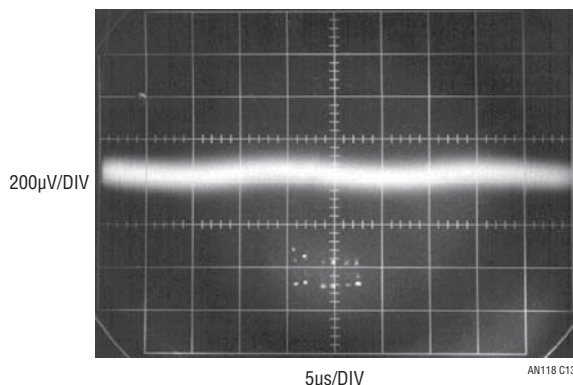


Figure C13. Voltmeter Lead Attached to Regulator Output Introduces RF Pickup, Multiplying Apparent Noise Floor

Isolated Trigger Probe

The text associated with Figure C5 somewhat cryptically alluded to an “isolated trigger probe.” Figure C14 reveals this to be simply an RF choke terminated against ringing. The choke picks up residual radiated field, generating an isolated trigger signal. This arrangement furnishes a 'scope trigger signal with essentially no measurement corruption. The probe's physical form appears in Figure C15. For good results the termination should be adjusted for minimum ringing while preserving the highest possible amplitude output. Light compensatory damping produces Figure C16's output, which will cause poor 'scope triggering. Proper adjustment results in a more favorable output (Figure C17), characterized by minimal ringing and well-defined edges.

Trigger Probe Amplifier

The field around the switching magnetics is small and may not be adequate to reliably trigger some oscilloscopes. In such cases, Figure C18's trigger probe amplifier is useful. It uses an adaptive triggering scheme to compensate for variations in probe output amplitude. A stable 5V trigger output is maintained over a 50:1 probe output range. A1, operating at a gain of 100, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of

A1's output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394's positive input. The LT1394's negative input is biased directly from A1's output. The LT1394's output, the circuit's trigger output, is unaffected by >50:1 signal amplitude variations. An X100 analog output is available at A1.

Figure C19 shows the circuit's digital output (trace B) responding to the amplified probe signal at A1 (trace A).

Figure C20 is a typical noise testing setup. It includes the breadboard, trigger probe, amplifier, oscilloscope and coaxial components.

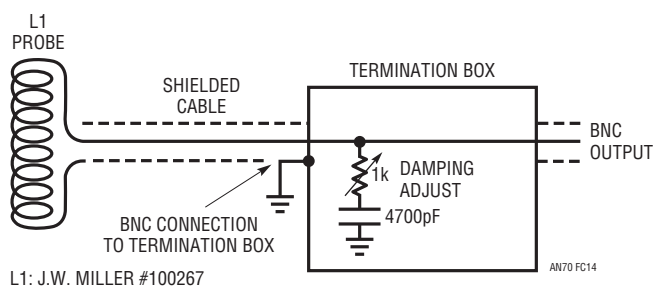


Figure C14. Simple Trigger Probe Eliminates Board Level Ground Loops. Termination Box Components Damp L1's Ringing Response

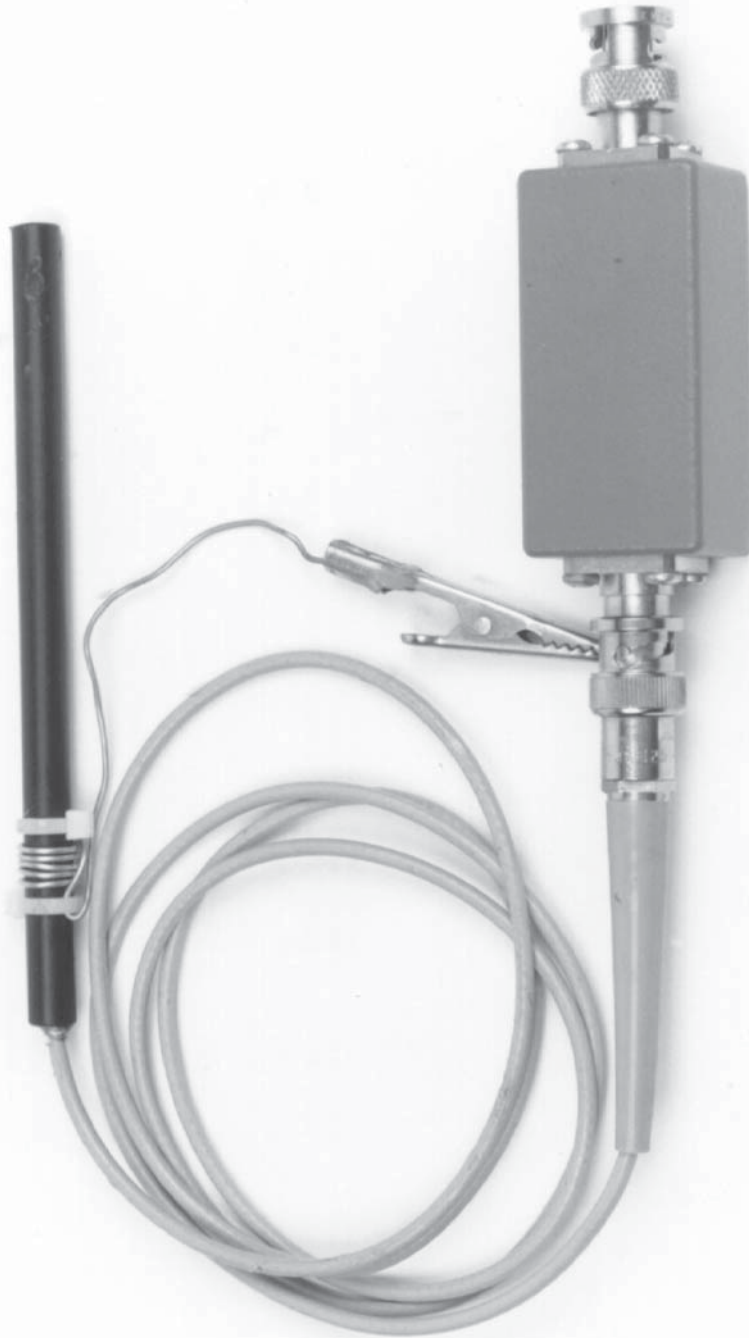


Figure C15. The Trigger Probe and Termination Box. Clip Lead Facilitates Mounting Probe, Is Electrically Neutral

Application Note 118

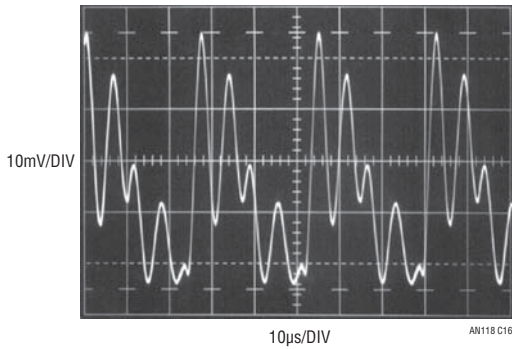


Figure C16. Misadjusted Termination Causes Inadequate Damping. Unstable Oscilloscope Triggering May Result

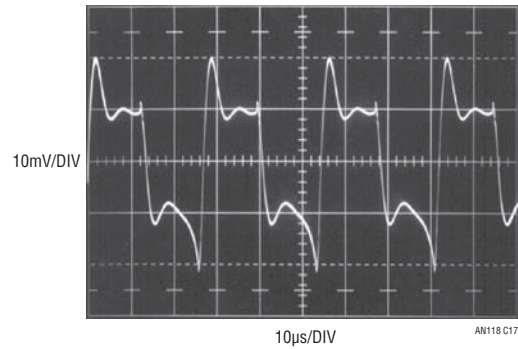


Figure C17. Properly Adjusted Termination Minimizes Ringing with Small Amplitude Penalty

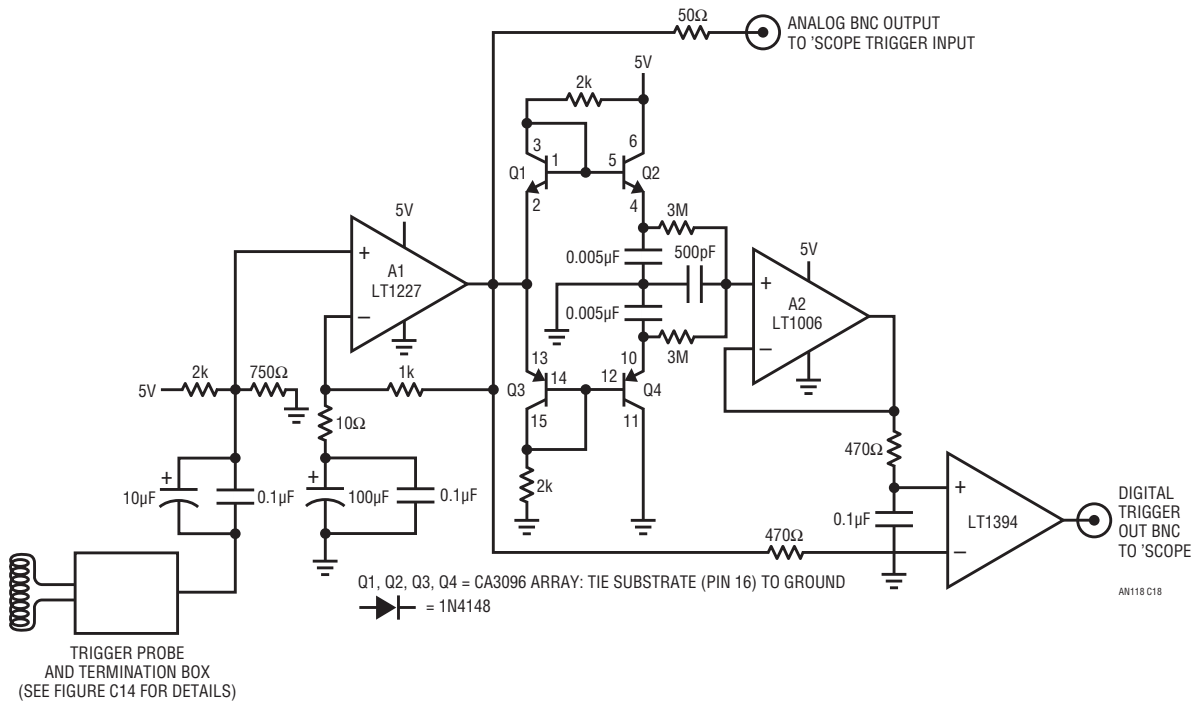


Figure C18. Trigger Probe Amplifier Has Analog and Digital Outputs. Adaptive Threshold Maintains Digital Output Over 50:1 Probe Signal Variations

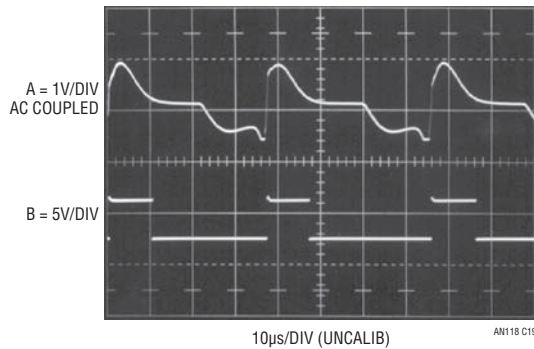


Figure C19. Trigger Probe Amplifier Analog (Trace A) and Digital (Trace B) Outputs

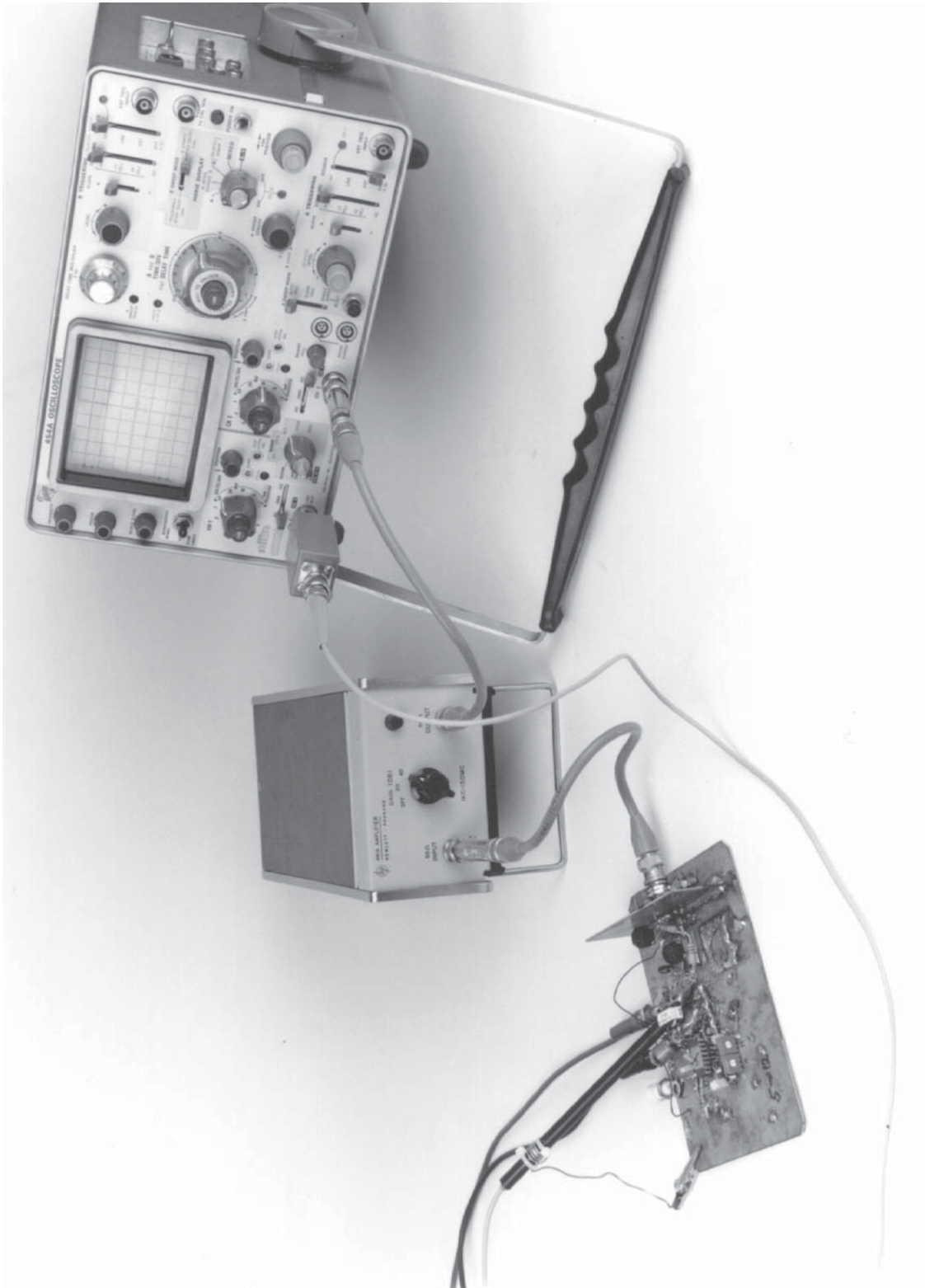


Figure C20. Typical Noise Test Setup Includes Trigger Probe, Amplifier, Oscilloscope and Coaxial Components

APPENDIX D

BREADBOARDING, NOISE MINIMIZATION AND LAYOUT CONSIDERATIONS

LT1533-based circuit's low harmonic content allows their noise performance to be less layout sensitive than other switching regulators. However, some degree of prudence is in order. As in all things, cavaliness is a direct route to disappointment. Obtaining the absolute lowest noise figure requires care, but performance below 500 μ V is readily achieved. In general, lowest noise is obtained by preventing mixing of ground currents in the return path. Indiscriminate disposition of ground currents into a bus or ground plane will cause such mixing, raising observed output noise. The LT1533's restricted edge rates mitigate against corrupted ground path-induced problems, but best noise performance occurs in a "single-point" ground scheme. Single-point return schemes may be impractical in production PC boards. In such cases, provide the lowest possible impedance path to the power entry point from the inductor associated with the LT1533's power ground pin. (Pin 16). Locate the output component ground returns as close to the circuit load point as possible. Minimize return current mixing between input and output sections by restricting such mixing to the smallest possible common conductive area.

Noise Minimization

The LT1533's controlled switching times allow extraordinarily low noise DC/DC conversion with surprisingly little design effort. Wideband output noise well below 500 μ V is easily achieved. In most situations this level of performance is entirely adequate. Applications requiring the lowest possible output noise will benefit from special attention to several areas.

Noise Tweaking

The slew time versus efficiency trade-off should be weighted towards lowest noise to the extent tolerable. Typically, slew times beyond 1.3 μ s result in "expensive" noise reduction in terms of lost efficiency, but the benefit is available. The issue is how much power is expendable to obtain incremental decreases in output noise. Similarly, the layout techniques

previously discussed should be reviewed. Rigid adherence to these guidelines will result in correspondingly lower noise performance. The text's breadboards were originally constructed to provide the lowest possible noise levels, and then systematically degraded to test layout sensitivity. This approach allows experimentation to determine the best layout without expanding fanatical attention to details that provide essentially no benefit.

The slow edge times greatly minimize radiated EMI, but experimentation with the component's physical orientation can sometimes improve things. Look at the components (yes, literally!) and try and imagine just what their residual radiated field impinges on. In particular, the optional output inductor may pick up field radiated by other magnetics, resulting in increased output noise. Appropriate physical layout will eliminate this effect, and experimentation is useful. The EMI probe described in Appendix E is a useful tool in this pursuit and highly recommended.

Capacitors

The filter capacitors used should have low parasitic impedance. Sanyo OS-CON types are excellent in this regard and contributed to the performance levels quoted in the text. Tantalum types are nearly as good. The input supply bypass capacitor, which should be located directly at the transformer center tap, needs similarly good characteristics. Aluminum electrolytics are not suitable for any service in LT1533 circuits.

Damper Network

Some circuits may benefit from a small (e.g., 300 Ω -1000pF) damper network across the transformer secondary if the absolutely lowest noise is needed. Extremely small (20 μ V to 30 μ V) excursions can briefly appear during the switching interval when no energy is coming through the transformer. These events are so minuscule that they are barely measurable in the noise floor, but the damper will eliminate them.

Measurement Technique

Strictly speaking, measurement technique is not a way to obtain lowest noise performance. Realistically, it is essential that measurement technique be trustworthy. Uncountable

hours have been lost chasing “circuit problems” that in reality are manifestations of poor measurement technique. Please read Appendices B and C before pursuing solutions to circuit noise that isn’t really there.¹

Note 1. I do not wax pedantic here. My guilt in this offense runs deep.

APPENDIX E

APPLICATION NOTE E101: EMI “SNIFFER” PROBE

Bruce Carsten Associates, Inc.

6410 NW Sisters Place, Corvallis, Oregon 97330

541-745-3935

The EMI Sniffer Probe¹ is used with an oscilloscope to locate and identify magnetic field sources of electromagnetic interference (EMI) in electronic equipment. The probe consists of a miniature 10 turn pickup coil located in the end of a small shielded tube, with a BNC connector provided for connection to a coaxial cable (Figure E1). The Sniffer Probe output voltage is essentially proportional to the rate of change of the ambient magnetic field, and thus to the rate of change of nearby currents.

The principal advantages of the Sniffer Probe over simple pickup loops are:

1. Spatial resolution of about a millimeter.
2. Relatively high sensitivity for a small coil.
3. A 50Ω source termination to minimize cable reflections with unterminated scope inputs.
4. Faraday shielding to minimize sensitivity to electric fields.

The EMI Sniffer Probe was developed to diagnose sources of EMI in switch mode power converters, but it can also be used in high speed logic systems and other electronic equipment.

SOURCES OF EMI

Rapidly changing voltages and currents in electrical and electronic equipment can easily result in radiated and conducted noise. Most EMI in switch mode power converters is thus generated during switching transients when power transistors are turned on or off.

Conventional scope probes can readily be used to see dynamic voltages, which are the principal sources of common mode conducted EMI. (High dV/dt can also feed through poorly designed filters as normal mode voltage spikes and may radiate fields from a circuit without a conductive enclosure.)

Dynamic currents produce rapidly changing magnetic fields which radiate far more easily than electric fields as they are more difficult to shield. These changing magnetic fields can also induce low impedance voltage transients in other circuits, resulting in unexpected normal and common mode conducted EMI.

These high dI/dt currents and resultant fields can not be directly sensed by voltage probes, but are readily detected and located with the Sniffer Probe. While current probes can sense currents in discrete conductors and wires, they are of little use with printed circuit traces or in detecting dynamic magnetic fields.

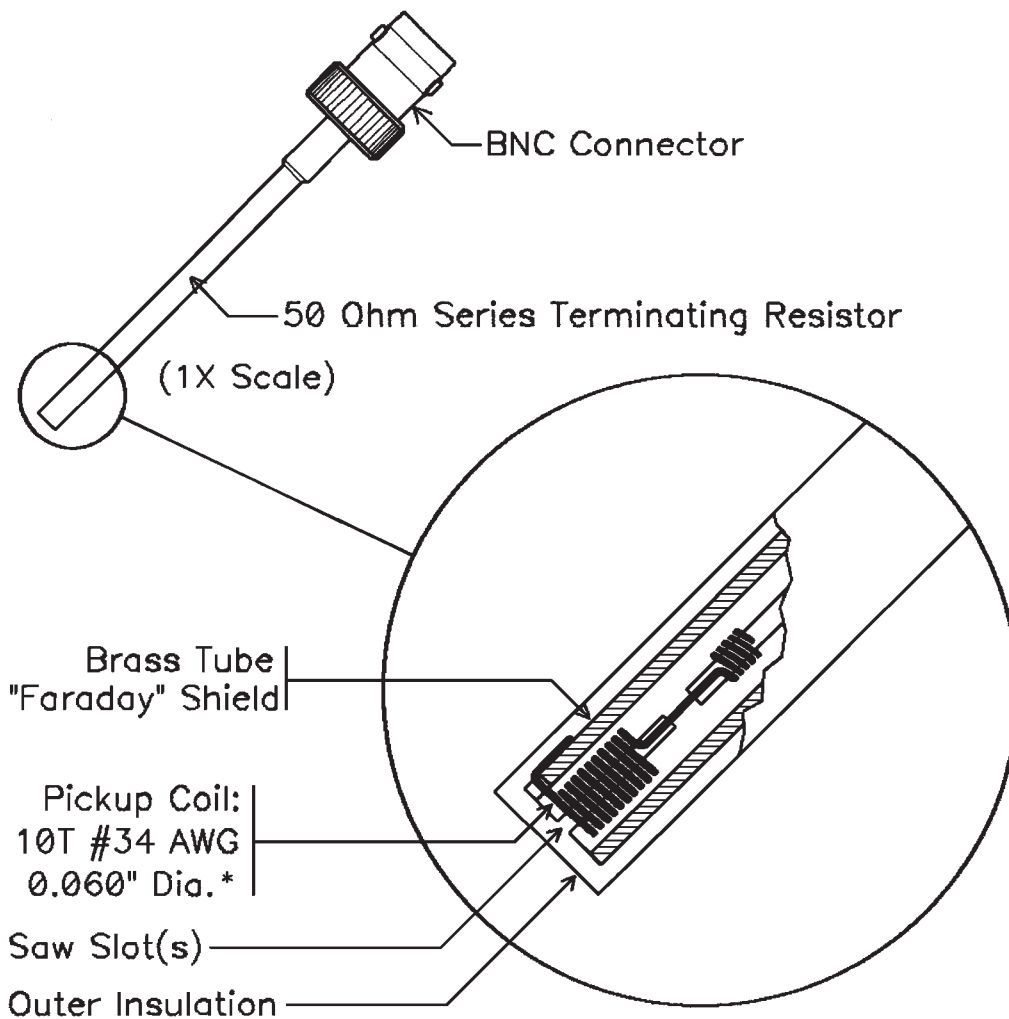
PROBE RESPONSE CHARACTERISTICS

The Sniffer Probe is sensitive to magnetic fields only along the probe axis. This directionality is useful in locating the paths and sources of high dI/dt currents. The resolution is usually sufficient to locate which trace on a printed circuit board, or which lead on a component package, is conducting the EMI generating current.

For “isolated” single conductors or PC traces, the Probe response is greatest just to either side of the conductor

Note 1. The EMI Sniffer Probe is available from Bruce Carsten Associates at the address noted in the title of this appendix.

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*Approx. 160 μ Wire, 1.5mm Coil Dia.

Figure E1. Construction of the EMI "Sniffer Probe" for Locating and Identifying Magnetic Field Sources of EMI

where the magnetic flux is along with probe axis. (Probe response may be a little greater with the axis tilted towards the center of the conductor.) As shown in Figure E2, there is a sharp response null in the middle of the conductor, with a 180° phase shift to either side and a decreasing response with distance. The response will increase on the inside of a bend where the flux lines are crowded together, and is reduced on the outside of a bend where the flux lines spread apart.

When the return current is in an adjacent parallel conductor, the Probe response is greatest between the two conductors as shown in Figure E3. There will be a sharp null and phase shift over each conductor, with a lower peak response outside the conductor pair, again decreasing with distance.

The response to a trace with a return current on the opposite side of the board is similar to that of a single isolated trace, except that the probe response may be greater with the Probe axis tilted away from the trace. A "ground plane" below a trace will have a similar effect, as there will be a counter-flowing "image" current in the ground plane.

The Probe frequency response to a uniform magnetic field is shown in Figure E4. Due to large variations in field strength around a conductor, the Probe should be considered as a qualitative indicator only, with no attempt made to "calibrate" it. The response fall-off near 300MHz is due to the pickup coil inductance driving the coax cable impedance, and the mild resonant peaks (with a 1M Ω scope termination) at multiples of 80MHz are due to transmission line reflections.

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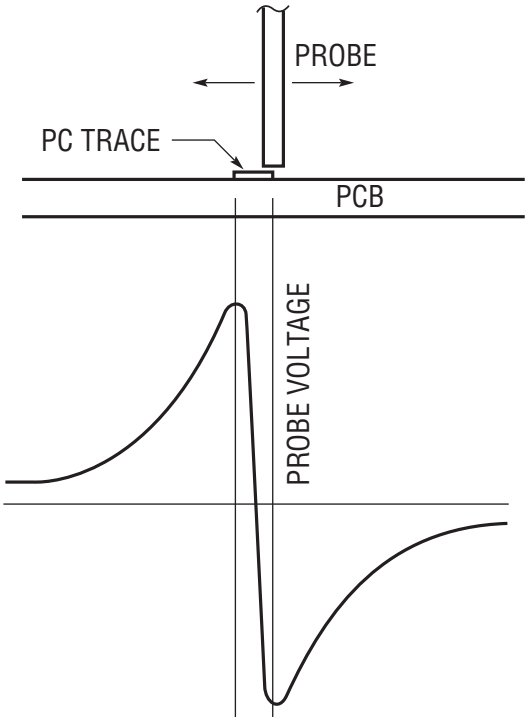


Figure E2. Sniffer Probe Response to Current in a Physically "Isolated" Conductor

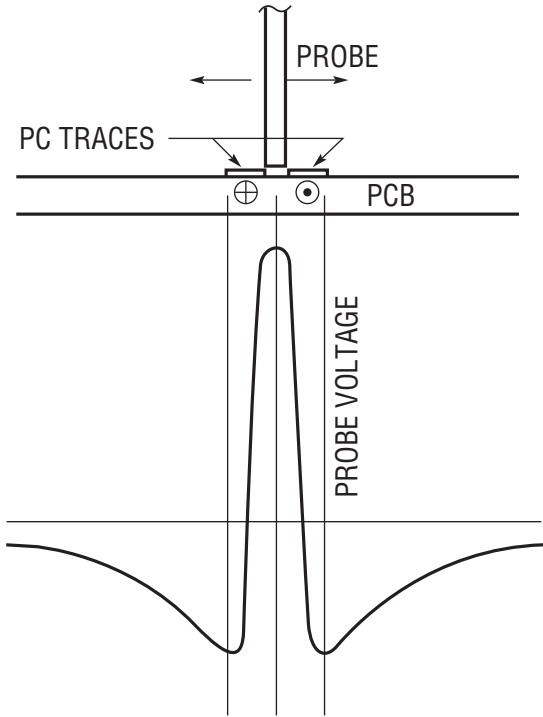
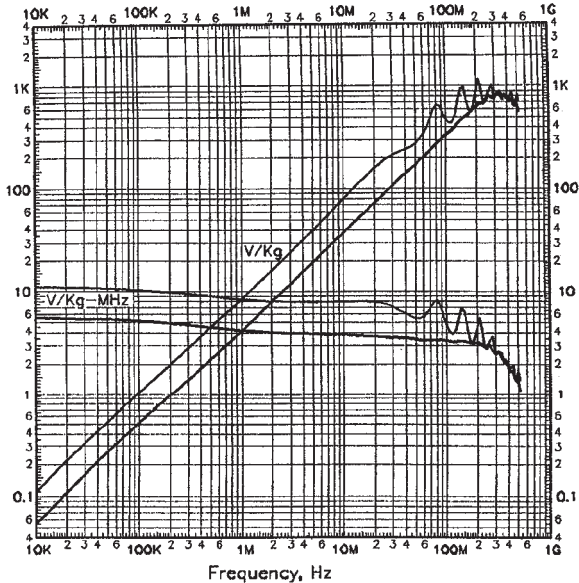


Figure E3. Sniffer Probe Response with Return Current in a Parallel Conductor



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Figure E4. Typical EMI "Sniffer" Probe Frequency Response Measured with 1.3m (51") of 50Ω Coax to Scope
 Upper Traces: 1Meg Scope Input Impedance
 Lower Traces: 50Ω Scope Input Impedance

an118fa

Application Note 118

PRINCIPLES OF PROBE USE

The Sniffer Probe is used with at least a 2-channel scope. One channel is used to view the noise whose source is to be located (which may also provide the scope trigger) and the other channel is used for the Sniffer Probe. The probe response nulls make it inadvisable to use this scope channel for triggering.

A third scope trigger channel can be very useful, particularly if it is difficult to trigger on the noise. Transistor drive waveforms (or their predecessors in the upstream logic) are ideal for triggering; they are usually stable, and allow immediate precursors of the noise to be viewed.

Start with the Probe at some distance from the circuit with the Probe channel at maximum sensitivity. Move the probe around the circuit, looking for “something happening” in the circuit’s magnetic fields at the same time as the noise problem. A precise “time domain” correlation between EMI noise transients and internal circuit fields is fundamental to the diagnostic approach.

As a candidate noise source is located, the Probe is moved closer while the scope sensitivity is decreased to keep the probe waveform on-screen. It should be possible to quickly bring the probe down to the PC board trace (or wiring) where the probe signal seems to be a maximum. This may not be near the point of EMI generation, but it should be near a PC trace or other conductor carrying the current from the EMI source. This can be verified by moving the

probe back and forth in several directions; when the appropriate PC trace is crossed at roughly right angles, the probe output will go through a sharp null over the trace, with an evident phase reversal in probe voltage on each side of the trace (as noted above).

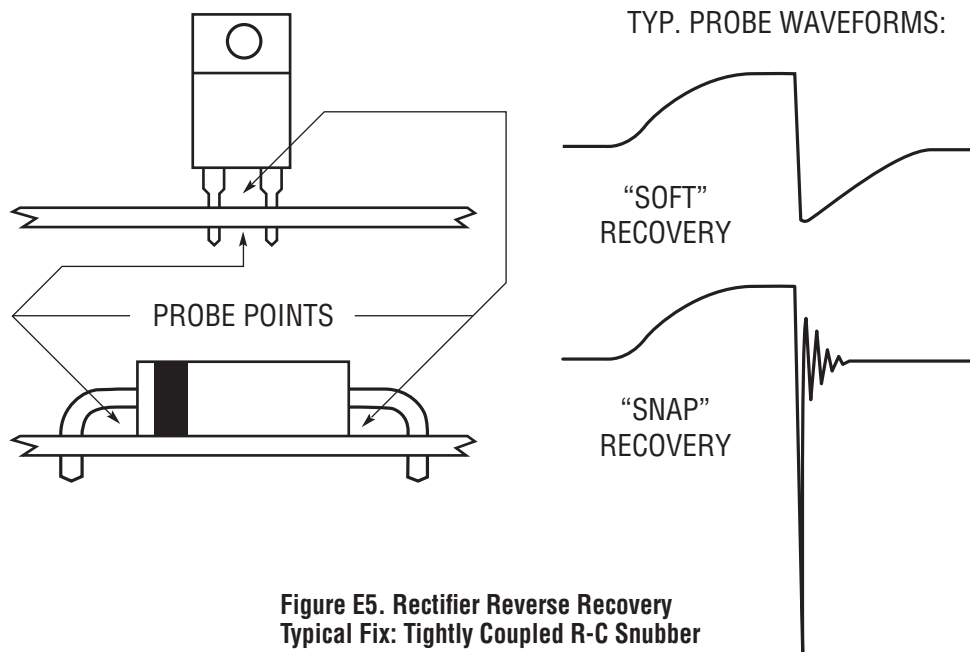
This EMI “hot” trace can be followed (like a bloodhound on the scent trail) to find all or much of the EMI generating current loop. If the trace is hidden on the back side (or inside) of the board, mark its path with a felt pen and locate the trace on disassembly, on another board or on the artwork. From the current path and the timing of the noise transient, the source of the problem usually becomes almost self-evident.

Several not-uncommon problems (all of which have been diagnosed with various versions of the Sniffer Probe) are discussed here with suggested solutions or fixes.

TYPICAL DI/DT EMI PROBLEMS

Rectifier Reverse Recovery

Reverse recovery of rectifiers is the most common source of di/dt-related EMI in power converters; the charge stored in P-N junction diodes during conduction causes a momentary reverse current flow when the voltage reverses. This reverse current may stop very quickly (<1ns) in diodes with a “snap” recovery (more likely in devices with a PIV rating of less than 200V), or the reverse current



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may decay more gradually with a “soft” recovery. Typical Sniffer Probe waveforms for each type of recovery are shown in Figure E5.

The sudden change in current creates a rapidly changing magnetic field, which will both radiate external fields and induce low impedance voltage spikes in other circuits. This reverse recovery may “shock” parasitic L-C circuits into ringing, which will result in oscillatory waveforms with varying degrees of damping when the diode recovers. A series R-C damper circuit in parallel with the diode is the usual solution.

Output rectifiers generally carry the highest currents and are thus the most prone to this problem, but this is often recognized and they may be well-snubbed. It is not uncommon for unsnubbed catch or clamp diodes to be *more* of an EMI problem. (The fact that a diode in an R-C-D snubber may need its *own* R-C snubber is not always self-evident, for example).

The problem can usually be identified by placing the Sniffer Probe near a rectifier lead. The signal will be strongest on the inside of a lead bend in an axial package, or between the anode and cathode leads in a TO-220, TO-247 or similar type of package, as shown in Figure E5.

Using “softer” recovery diodes is a possible solution and Schottky diodes are ideal in low voltage applications. However, it must be recognized that a P-N diode with soft recovery is also inherently lossy (while a “snap” recovery is not), as the diode simultaneously develops a reverse voltage while still conducting current: The fastest possible diode (lowest recovered charge) with a moderately soft recovery is usually the best choice. Sometimes a faster, slightly “snappy” diode with a tightly coupled R-C snubber works as well or better than a soft but excessively slow recovery diode.

If significant ringing occurs, a “quick-and-dirty” R-C snubber design approach works fairly well: increasingly large damper capacitors are placed across the diode until the ringing frequency is halved. We know that the total ringing capacity is now quadrupled or that the original ringing capacity is 1/3 of the added capacity. The damper resistance required is about equal to the capacitive reactance of the original ringing capacity at the original ringing frequency.

The “frequency halving” capacity is then connected in series with the damping resistance and placed across the diode, as tightly coupled as possible.

Snubber capacitors must have a high pulse current capability and low dielectric loss. Temperature stable (disc or multilayer) ceramic, silvered mica and some plastic filmfoil capacitors are suitable. Snubber resistors should be noninductive; metal film, carbon film and carbon composition resistors are good, but wirewound resistors must be avoided. The maximum snubber resistor dissipation can be estimated from the product of the damper capacity, switching frequency and the square of the peak snubber capacitor voltage.

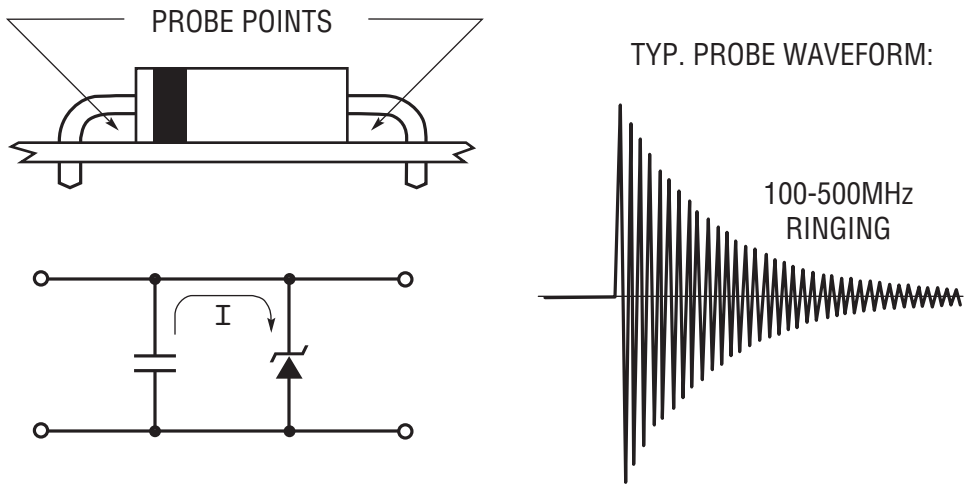
Snubbers on passive switches (diodes) or active switches (transistors) should always be coupled as closely as physically possible, with minimal loop inductance. This minimizes the radiated field from the change in current path from the switch to the snubber. It also minimizes the turn-off voltage overshoot “required” to force the current to change path through the switch-snubber loop inductance.

Ringling in Clamp Zeners

A capacitor-to-capacitor ringling problem can occur when a voltage clamping Zener or TransZorb® is placed across the output of a converter for overvoltage protection (OVP). Power Zeners have a large junction capacity, and this can ring in series with the lead ESL and the output capacitors, with some of the ringling voltage showing up on the output. This ringling current can be most easily detected near the Zener leads, particularly on the inside of a bend as shown in Figure E6.

R-C snubbers have not been found to work well in this case as the ringling loop inductance is often as low or lower than the obtainable parasitic inductance in the snubber. Increasing the external loop inductance to allow damping is not advisable as this would limit dynamic clamping capability. In this case, it was found that a small ferrite bead on one or both of the Zener leads dampened the HF oscillations with minimal adverse side effects (a high permeability ferrite bead quickly saturates as soon as the Zener begins to conduct significant current).

Application Note 118



**Figure E6. Ringing Between Clamp Zener and Capacitor
Typical Fix: Small Ferrite Bead on Zener Lead(s)**

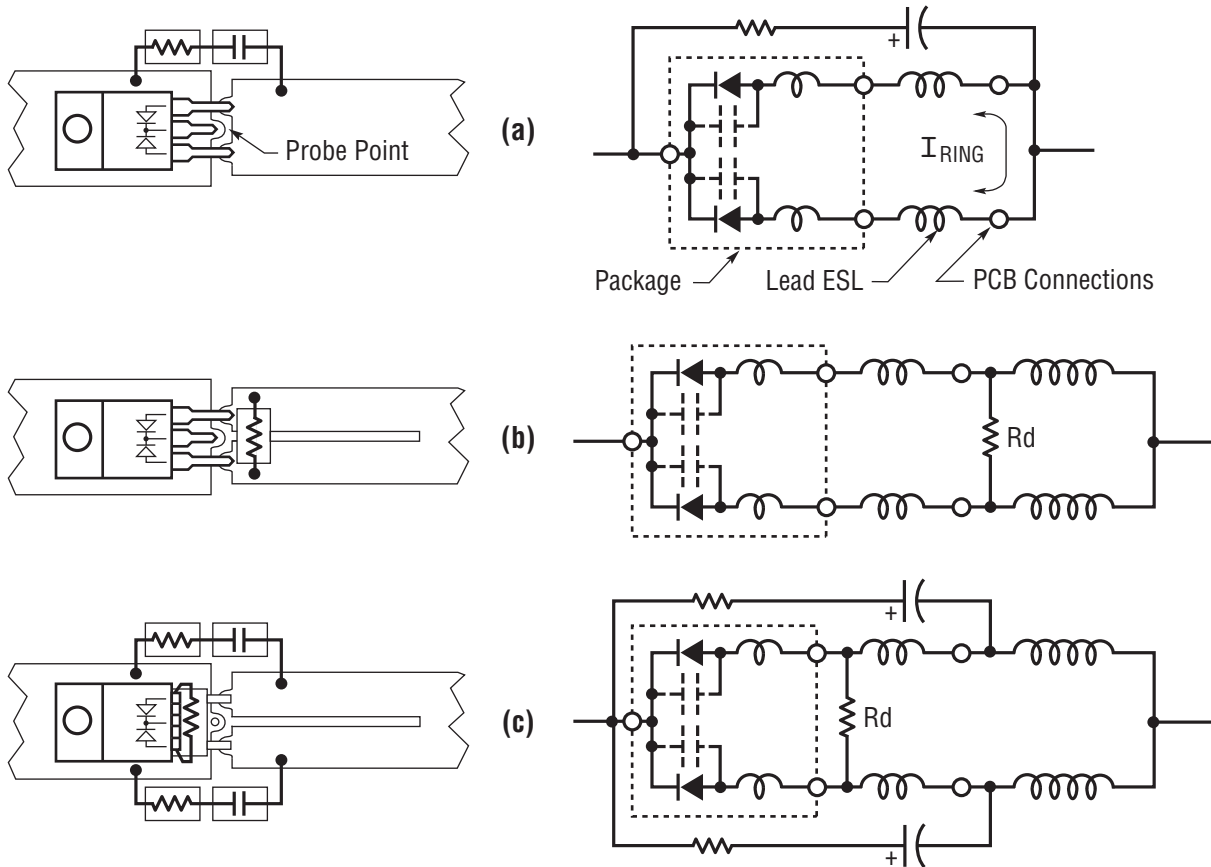


Figure E7. Ringing in Paralleled Dual Rectifiers

Paralleled Rectifiers

A less evident problem can occur when dual rectifier diodes in a package are paralleled for increased current capability, even with a tightly coupled R-C snubber. The two diodes seldom recover at exactly the same time, which can cause a very high frequency oscillation (hundreds of MHz) to occur between the capacities of the two diodes in series with the anode lead inductances, as shown in Figure E7. This effect can really only be observed by placing the probe between the two anode leads, as the ringing current exists almost nowhere else (the ringing is nearly “invisible” to a conventional voltage probe, like many other EMI effects that can be easily found with a magnetic field Sniffer Probe).

This “teeter-totter” oscillation has a voltage “null” about where the R-C snubber is connected, so it provides little or no damping (see Figure E7a). It is actually very difficult to insert a suitable damping resistance into this circuit.

The easiest way to dampen the oscillation is to “slit” the anode PC trace for an inch or so and place a damping resistor at the anode leads as shown in Figure E7b. This increases the inductance in series with the diode-diode loop external to the package and leads, while having minimal effect on the effective series inductance. Even better damping is obtained by placing the resistor across the anode leads at the entry point to the case, as shown in Figure E7c, but this violates the mindset of many production engineers.

It is also preferable to split the original R-C damper into two (2R) - (C/2) dampers, one on each side of the dual

rectifier (also shown in Figure E7c). In practice, it is always preferable to use dual R-C dampers, one each side of the diode; loop inductance is cut about in half, and the external di/dt field is reduced even further due to the oppositely “handed” currents in the two snubber networks.

Paralleled Snubber or Damper Caps

A problem similar to that with the paralleled diodes occurs when two or more low loss capacitors are paralleled and driven with a sudden current change. There is a tendency for a current to ring between the two capacitors in series with their lead inductances (or ESL), as shown in Figure E8a. This type of oscillation can usually be detected by placing the Sniffer Probe between the leads of the paralleled capacitors. The ringing frequency is much lower than with the paralleled diodes (due to the larger capacity), and the effect *may* be benign if the capacitors are sufficiently closer together.

If the resultant ringing *is* picked up externally, it can be damped in a similar way as with the parallel diodes as shown in Figure E8b. In either case, the dissipation in the damping resistor tends to be relatively small.

Ringing in Transformer Shield Leads

The capacity of a transformer shield to other shields or windings (C_S in Figure E9) forms a series resonant circuit with its “drain wire” inductance (L_S) to the bypass point. This resonant circuit is readily excited by typical square wave voltages on windings, and a poorly damped oscillatory current may flow in the drain wire. The shield cur-

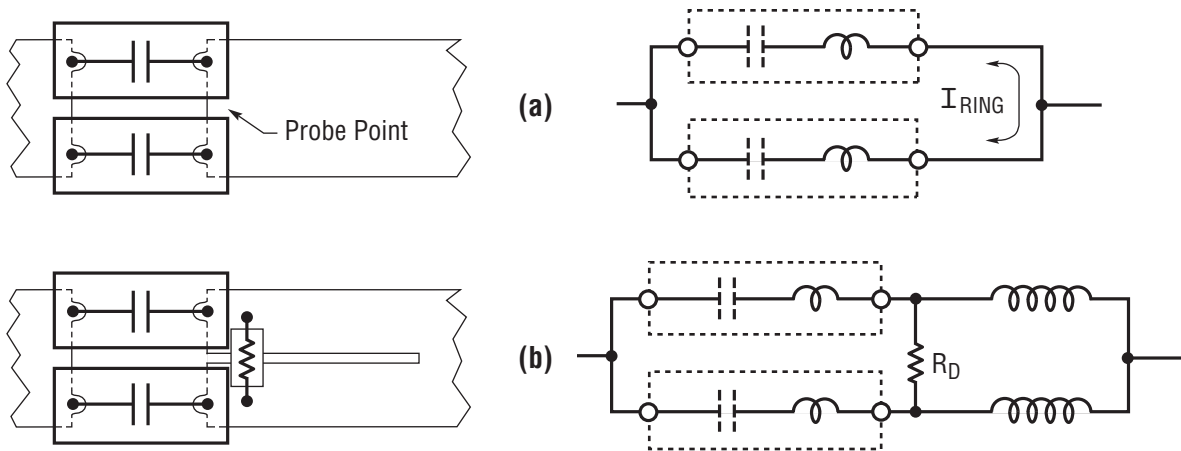
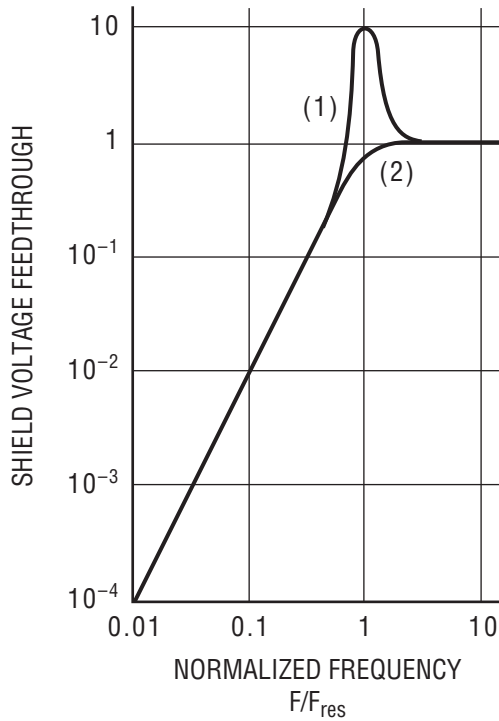
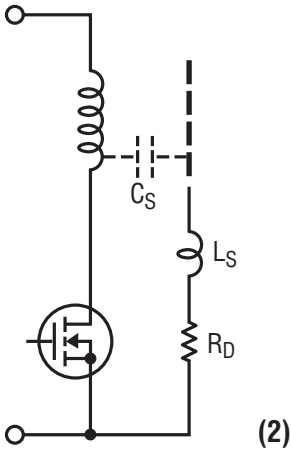
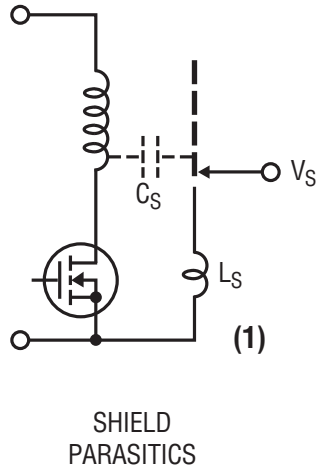


Figure E8. Ringing in Paralleled “Snubber” Capacitors

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Application Note 118



SHIELD RESONANCE
CAN BE DAMPED WITH
A RESISTOR “ R_D ” OR A
SMALL FERRITE BEAD:

$$R_D \approx \sqrt{\frac{L_S}{C_S}}$$

Figure E9. Shield Effectiveness at High Frequencies is Limited by Shield Capacity and Lead Inductance

rent may radiate noise into other circuits, and the shield voltage will often show up as common mode conducted noise. The shield voltage is very difficult to detect with a voltage probe in most transformers, but the ringing shield current can be observed by holding the Sniffer Probe near the shield drain wire (Figure E10), or the shield current's return path in the circuit.

This ringing can be dampened by placing a resistor R_D in series with the shield drain wire, whose value is approximately equal to the surge impedance of the resonant circuit, which may be calculated from the formula in Figure E9.

The shield capacitance (C_S) can readily be measured with a bridge (as the capacity from the shield to all facing shields and/or windings), but L_S is usually best calculated from C_S and the ringing frequency (as sensed by the Sniffer Probe). This resistance is typically on the order of tens of ohms.

One or more small ferrite beads can also be placed on the drain wire instead to provide damping. This option may be preferable as a late "fix" when the PC board has already been laid out.

In either case, the damper losses are typically quite small. The damper resistor has a moderately adverse impact on shield effectiveness below the shield and drain wire resonant frequency; damper beads are superior in this respect as their impedance is less at lower frequencies. The drain wire connection should also be as short as possible to the circuit bypass point, both to minimize EMI and to raise the shield's maximum effective (i.e., resonant) frequency.

Leakage Inductance Fields

Transformer leakage inductance fields emanate from between primary and secondary windings. With a single primary and secondary, a significant dipole field is created, which may be seen by placing the Sniffer Probe near the winding ends as shown in Figure E11a. If this field is generating EMI, there are two principal fixes:

1. Split the Primary *or* Secondary in two, to "sandwich" the other winding, and/or:
2. Place a shorted copper strap "electromagnetic shield" around the *complete-core and winding* assembly as shown in Figure E12. Eddy currents in the shorted strap largely cancel the external magnetic field.

The first approach creates a "quadrupole" instead of a dipole leakage field, which significantly reduces the distant field intensity. It also reduces the eddy current losses in any shorted strap electromagnetic shield used, which may or may not be an important consideration.

External Air Gap Fields

External air gaps in an inductor, such as those in open "bobbin core" inductors or with "E" cores spaced apart (Figure E11b), can be a major source of external magnetic fields when significant ripple or AC currents are present. These fields can also be easily located with the Sniffer Probe; response will be a maximum near an air gap or near the end of an open inductor winding.

"Open" inductor fields are not readily shielded and if they present an EMI problem the inductor must usually be redesigned to reduce external fields. The external field around spaced E cores can be virtually eliminated by placing all of the air gap in the center leg. Fields due to a (possibly intentional) residual or minor outside air gap can be minimized with the shorted strap electromagnetic shield of Figure E12, if eddy current losses prove not to be too high.

A less obvious problem may occur when inductors with "open" cores are used as second stage filter chokes. The minimal ripple current may not *create* a significant field, but such an inductor can "pick up" external magnetic fields and convert them to noise voltages or be an EMI *susceptibility* problem.²

Poorly Bypassed High Speed Logic

Ideally, all high speed logic should have a tightly coupled bypass capacitor for each IC and/or have power and ground distribution planes in a multilayer PCB.

At the other extreme, I have seen *one* bypass capacitor used at the power entrance to a logic board, with power and ground led to the ICs from opposite sides of the board. This created large spikes on the logic supply voltage and produced significant electromagnetic fields around the board.

Note 2. Ed Note. See Appendix D for additional commentary.

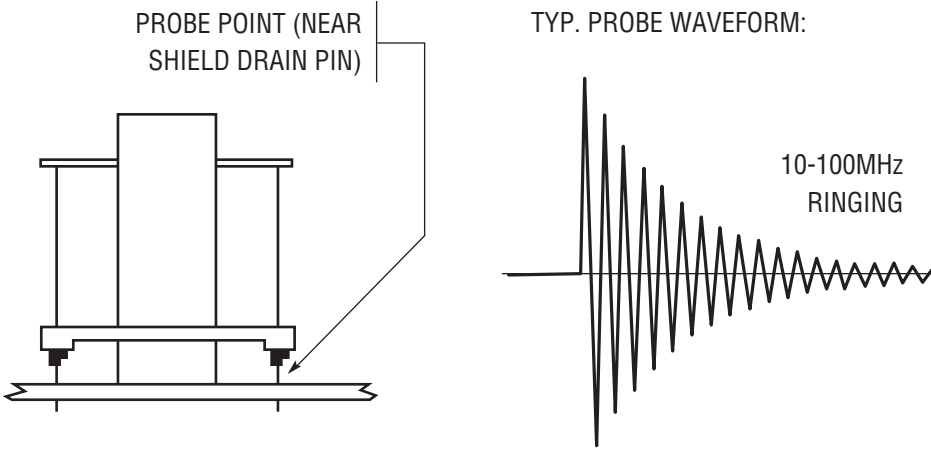


Figure E10. Transformer Shield Ringing Typical Fix: 10Ω to 100Ω Resistor (or Ferrite Bead in Drain Wire)

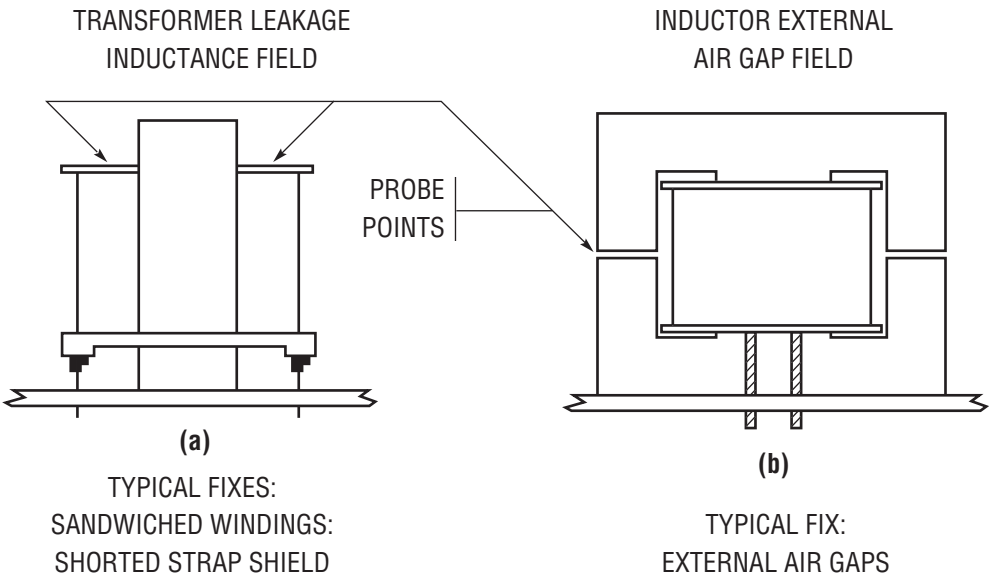


Figure E11. Probe Voltages Resemble the Transformer and Inductor Winding Waveforms

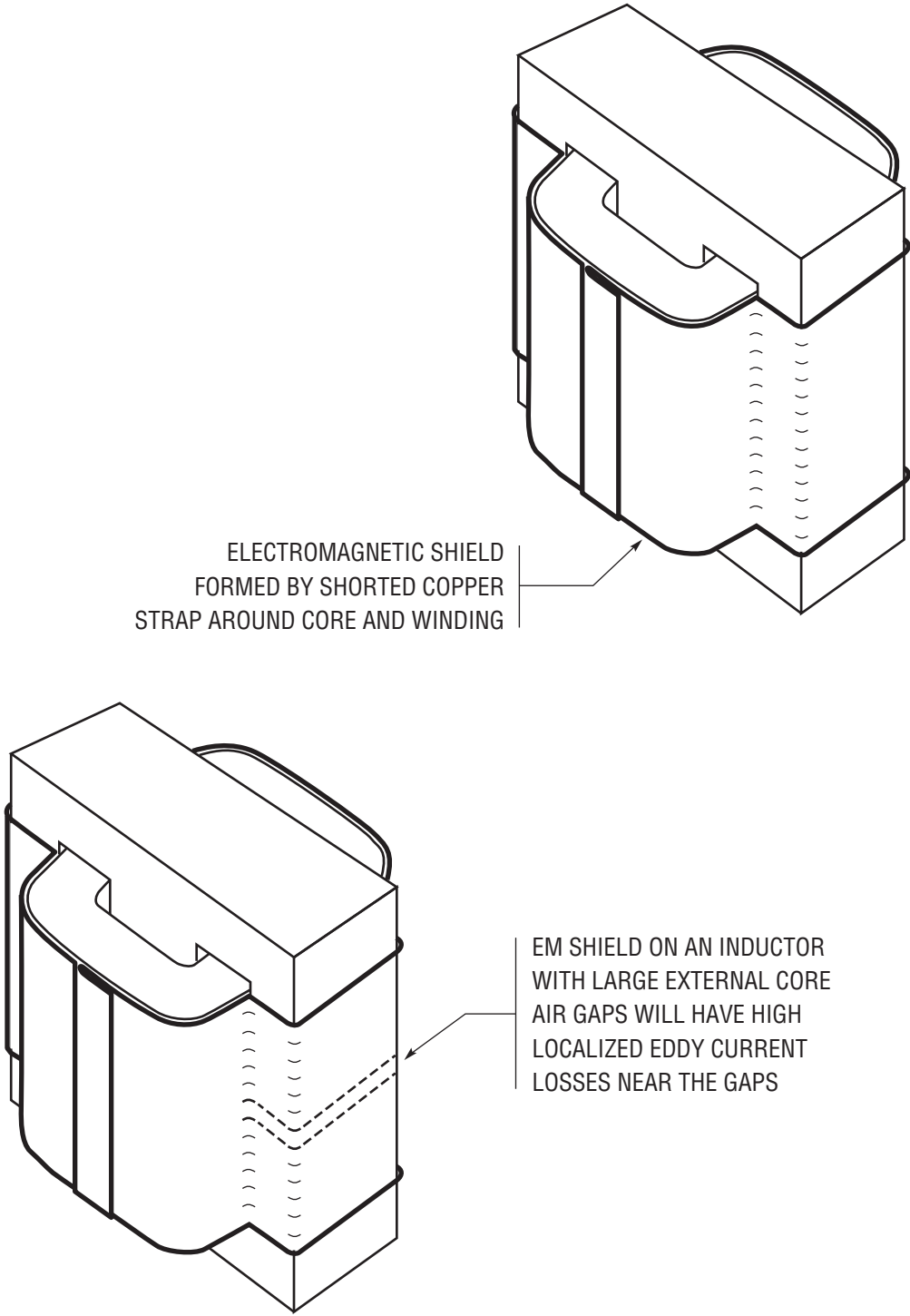


Figure E12. A “Sandwiched” PRI-SEC Transformer Winding Construction Reduces Electromagnetic Shield Eddy Current Losses

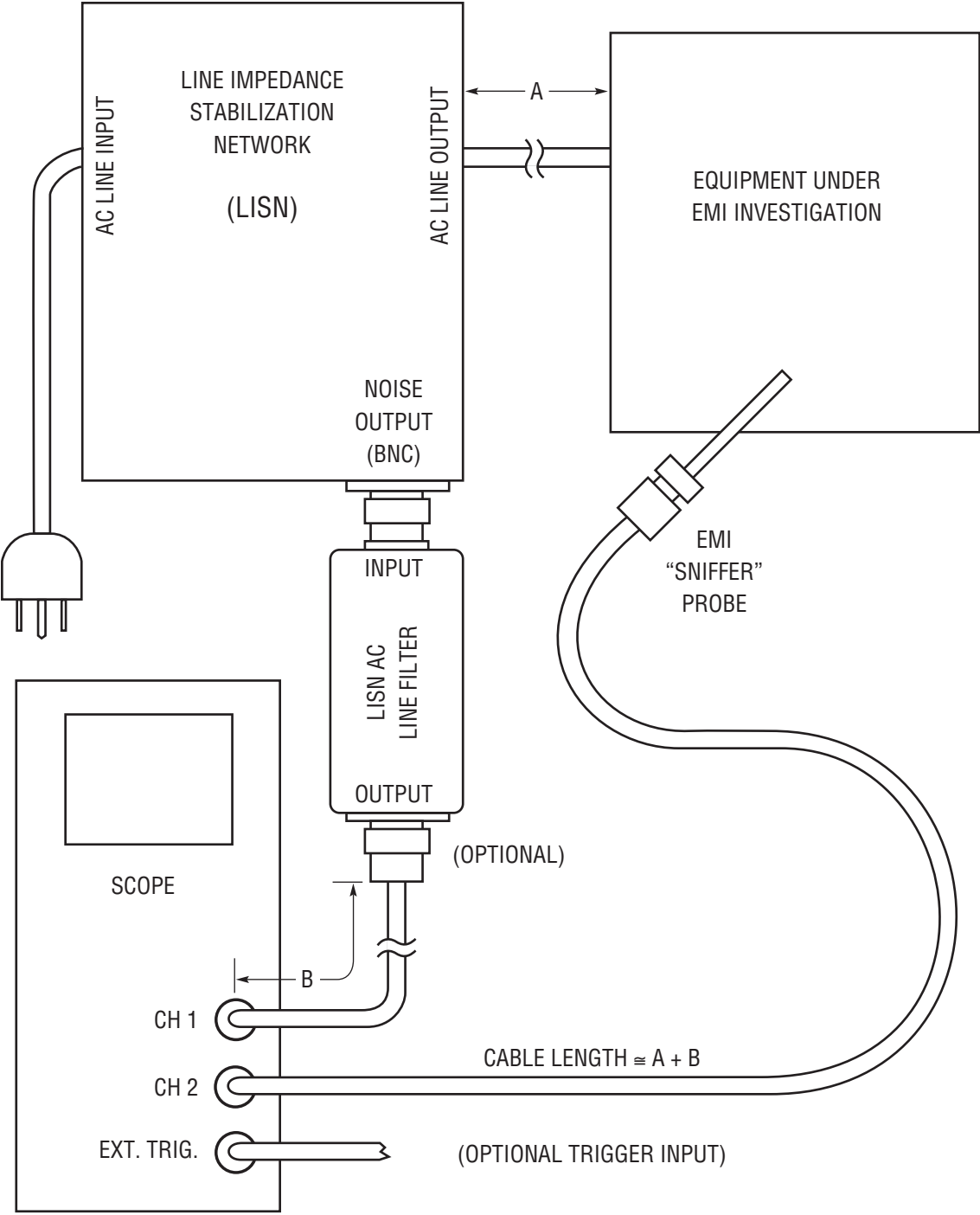
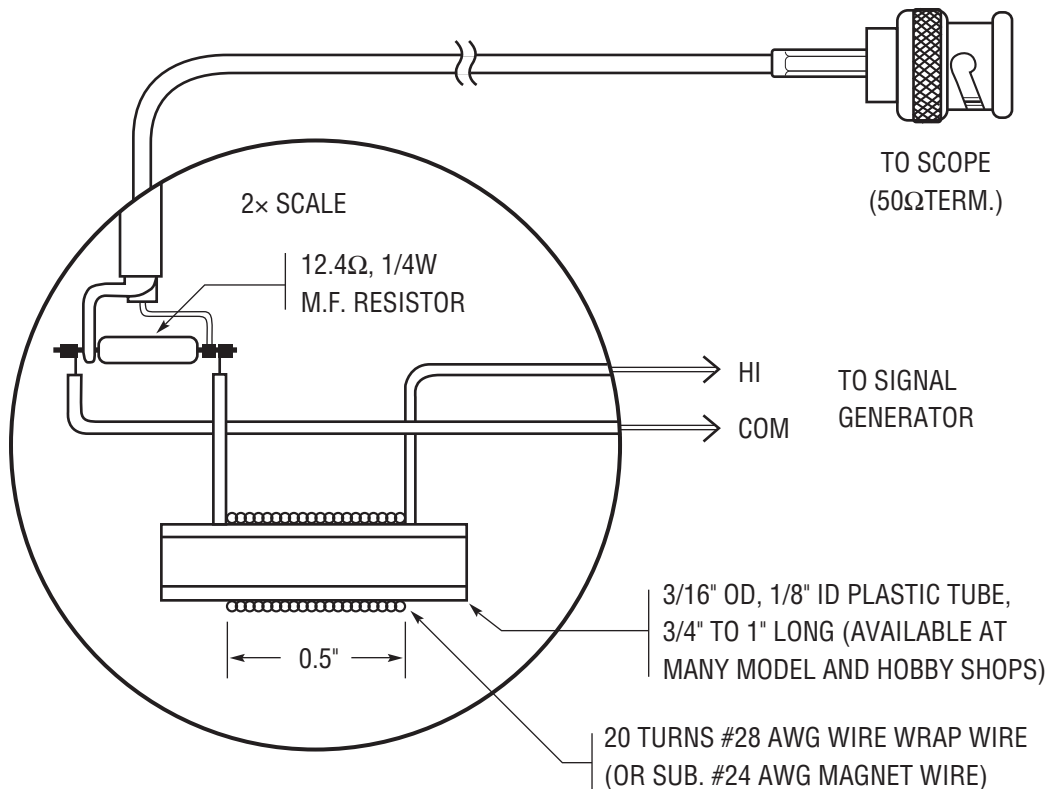


Figure E13. Using the Probe with a "LISN"



The Sniffer Probe Tip is centered inside the test coil where the Probe voltage is greatest. The approximate flux density in the middle of a coil can be calculated from the formula:

$$B = H = 1.257 NI/I \quad (\text{CGS Units})$$

For the 1.27cm long, 20-turn test coil, the flux density is about 20 Gauss per amp. At 1MHz, the Sniffer Probe voltage is 19mV_{p-p} (±10%) per 100mA_{p-p} for a 1MΩ load impedance, and half that for a 50Ω load.

Figure E14. EMI "Sniffer" Probe Test Coil

With a Sniffer Probe, I was able to show which pins of which ICs had the larger current transients *in synchronism* with the supply voltage transients. (The logic design engineers were accusing the power supply vendor of creating the noise. I found that the supplies were fairly quiet; it was the poorly designed logic power distribution system that was the problem.)

Probe Use with a “LISN”

A test setup using the Sniffer Probe with a Line Impedance Stabilization Network (LISN) is shown in Figure E13. The optional “LISN AC LINE FILTER” reduces AC line voltage feedthrough from a few 100mV to microvolt levels, simplifying EMI diagnosis when a suitable DC voltage source is not available or cannot be used.

TESTING THE SNIFFER PROBE

The Sniffer Probe can be functionally tested with a jig similar to that shown in Figure E14, which is used to test probes in production.

CONCLUSION

The Sniffer Probe is a simple, but very fast and effective means to locate di/dt sources of EMI. These EMI sources are very difficult to locate with conventional voltage or current probes.

SUMMARY

A summarized procedure for using the EMI “Sniffer” Probe appears in Figure E15.

- 1) Use a 2-channel scope, preferably one with an external trigger.
- 2) One scope channel is used for the Sniffer Probe, which is not to be used for triggering.
- 3) The second channel is used to view the noise transient whose source is to be located, which may also be used for triggering if practical.
- 4) More stable and reliable triggering is achieved with an “external trigger” (or a 3rd channel) on a transistor drive waveform (or preceding logic transition), allowing immediate precursors to the transient to be viewed. (Nearly all noise transients occur during, or just after, a power transistor turn-on or turn-off.
- 5) Start with the Probe at some distance from the circuit with maximum sensitivity and “sniff around” for something happening in *precise sync* with the noise transient. The Probe waveform will not be identical to the noise transient, but will usually have a strong resemblance.
- 6) Move the Probe closer to the suspected source while decreasing sensitivity. The conductor carrying the responsible current is located by the sharp response null on top of the conductor with inverted polarity on each side.
- 7) Trace out the noise current path as much as possible. Identify the current path on the schematic.
- 8) The source of the noise transient is usually evident from the current path and the timing information.

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Figure E15. EMI “Sniffer” Probe Procedure Outline

SNIFFER PROBE AMPLIFIER

Figure E16 shows a 40MHz amplifier for the Sniffer Probe. A gain of 200 allows an oscilloscope to display probe output over a wide range of sensed inputs. The amplifier is built into a small aluminum box. The probe should connect to the amplifier via BNC cable, although the 50Ω termination does not have to be a high quality coaxial type. The

probe's uncalibrated, relative output means high frequency termination aberrations are irrelevant. A simple film resistor, contained in the amplifier box, is adequate. Figure E17 shows the Sniffer Probe and the amplifier.

An alternate approach utilizes Appendix B's (Figure B11) HP-461A 50Ω amplifier.

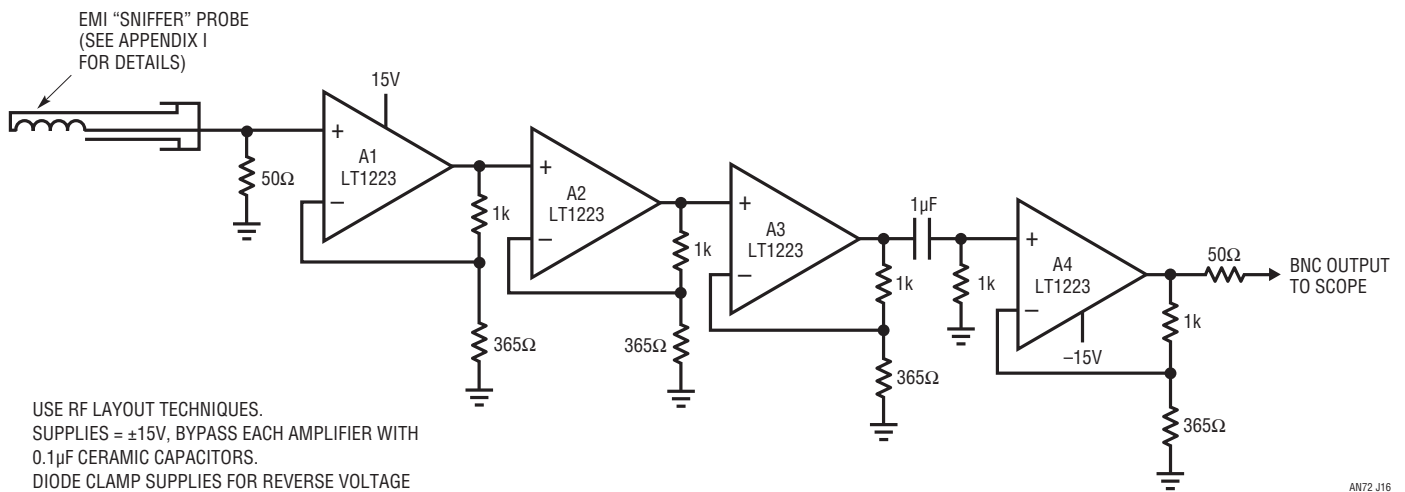


Figure E16. 40MHz Amplifier for EMI Probe

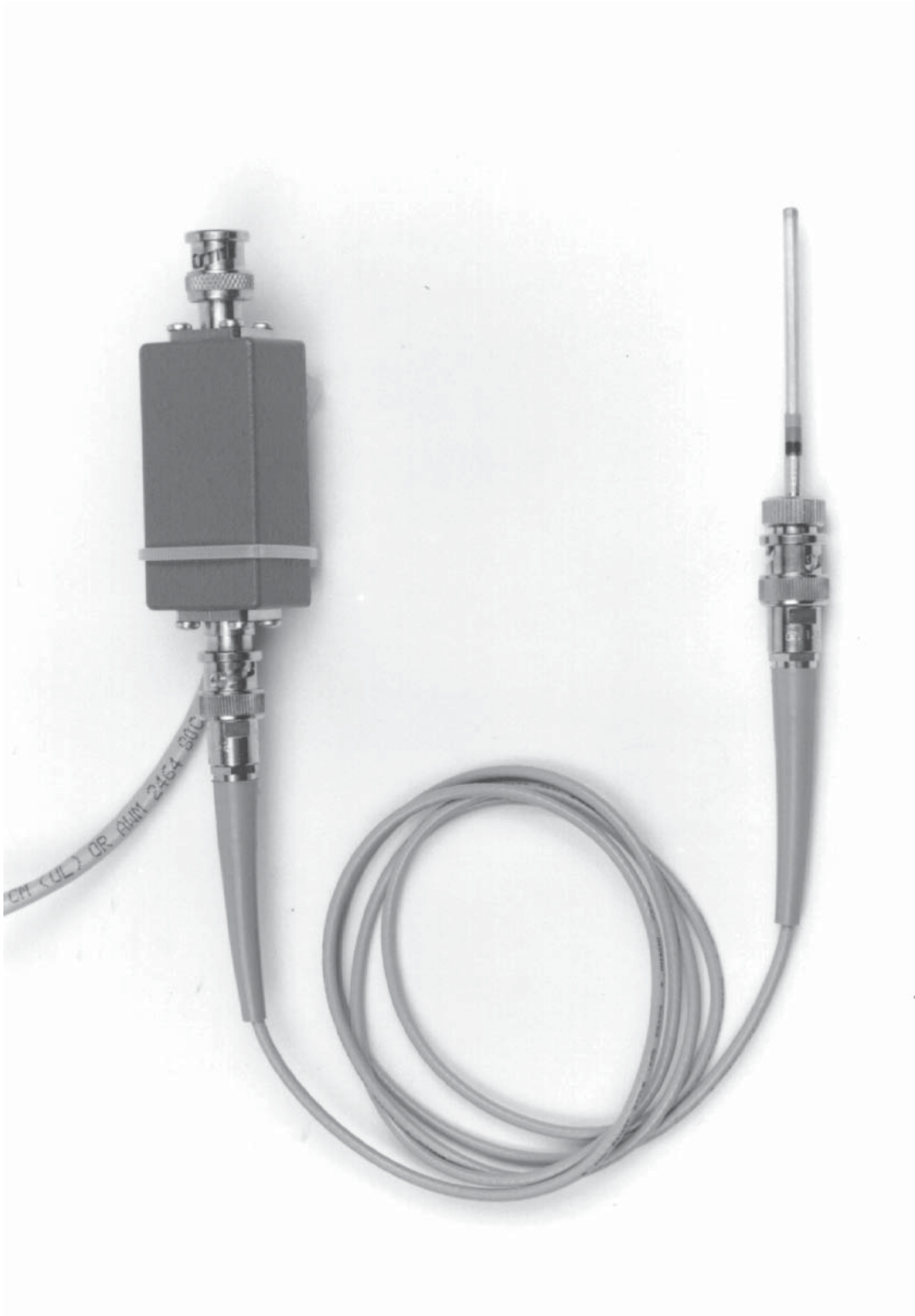


Figure E17. Sniffer Probe and Amplifier. Note All BNC-Based Signal Transmission. $\pm 15V$ Power Enters Box via Separate Cable

APPENDIX F

About Ferrite Beads

A ferrite bead enclosed conductor provides the highly desirable property of increasing impedance as frequency rises. This effect is ideally suited to high frequency noise filtering of DC and low frequency signal carrying conductors. The bead is essentially lossless within a linear regulator's passband. At higher frequencies the bead's ferrite material interacts with the conductors magnetic field, creating the loss characteristic. Various ferrite materials and geometries result in different loss factors versus frequency and power level. Figure F1's plot shows this. Impedance rises from 0.01Ω at DC to 50Ω at 100MHz . As DC current, and hence constant magnetic field bias, rises, the ferrite becomes less effective in offering loss. Note that beads can be "stacked" in series along a conductor, proportionally increasing their loss contribution. A wide variety of bead materials and physical configurations are available to suit requirements in standard and custom products.

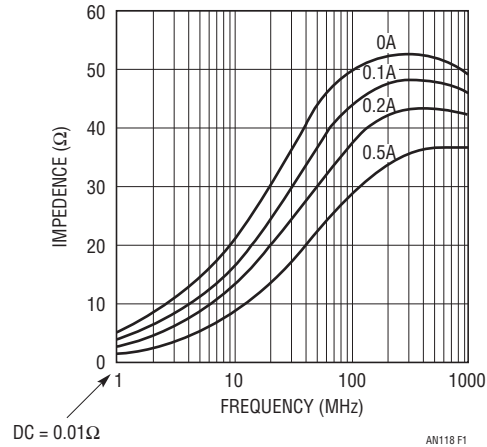


Figure F1. Impedance vs Frequency at Various DC Bias Currents for a Surface Mounted Ferrite Bead (Fair-Rite 2518065007Y6). Impedance is Essentially Zero at DC and Low Frequency, Rising Above 50Ω Depending on Frequency and DC Current. Source: Fair-Rite 2518065007Y6 Datasheet

APPENDIX G

Inductor Parasitics

Inductors can sometimes be used for high frequency filtering instead of beads but parasitics must be kept in mind. Advantages include wide availability and better effectiveness at lower frequencies, e.g., $\leq 100\text{kHz}$. Figure G1 shows disadvantages are parasitic shunt capacitance and potential susceptibility to stray switching regulator radiation. Parasitic shunt capacitance allows unwanted high frequency feedthrough. The inductors circuit board position may allow stray magnetic fields to impinge its

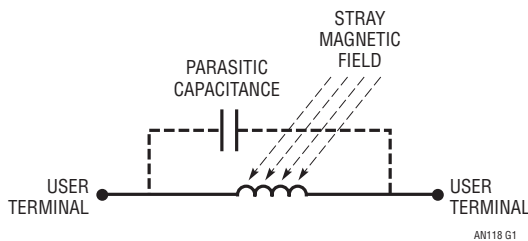


Figure G1. Some Parasitic Terms of an Inductor. Unwanted Capacitance Permits High Frequency Feedthrough. Stray Magnetic Field Induces Erroneous Inductor Current

winding, effectively turning it into a transformer secondary. The resulting observed spike and ripple related artifacts masquerade as conducted components, degrading performance.

Figure G2 shows a form of inductance based filter constructed from PC board trace. Such extended length traces, formed in spiral or serpentine patterns, look inductive at high frequency. They can be surprisingly effective in some circumstances, although introducing much less loss per unit area than ferrite beads.

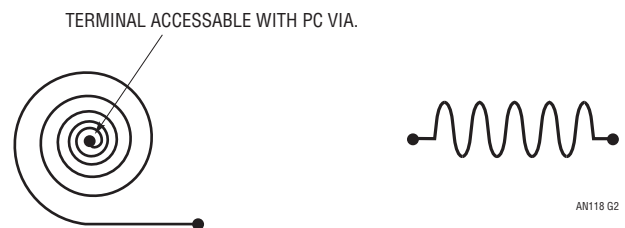
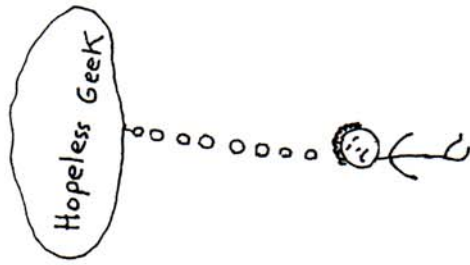
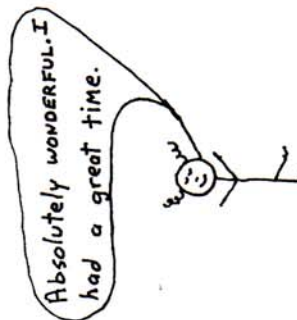
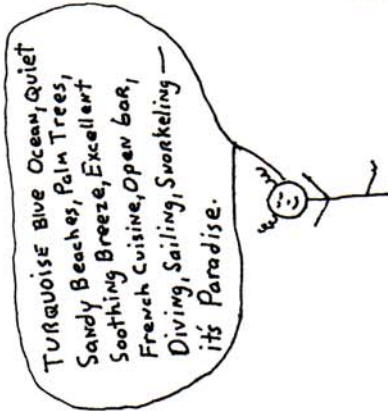
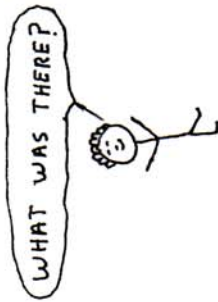
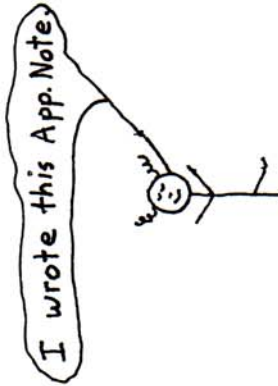


Figure G2. Spiral and Serpentine PC Patterns are Sometimes Used as High Frequency Filters, Although Less Effective Than Ferrite Beads

Application Note 118



— Wabman '08



1ppm Settling Time Measurement for a Monolithic 18-Bit DAC

When Does the Last Angel Stop Dancing on a Speeding Pinhead?

Jim Williams

Introduction

Performance requirements for instrumentation, function generation, inertial navigation systems, trimming, calibrators, ATE, medical apparatus and other precision applications are beginning to eclipse capabilities of 16-bit data converters. More specifically, 16-bit digital-to-analog converters (DACs) have been unable to provide required resolution in an increasing number of ultra-precision applications.

New components (see Components for 18-bit Digital-to-Analog Conversion, page 2) have made 18-bit DACs a practical design alternative¹. These ICs provide 18-bit performance at reasonable cost compared to previous modular and hybrid technologies. The monolithic DACs DC and AC specifications approach or equal previous converters at significantly lower cost.

DAC Settling Time

DAC DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, the settling time of a DAC and its output amplifier is extraordinarily difficult to determine to 18-bit (4ppm) resolution. DAC settling time is the elapsed time from input code application until the output arrives at, and remains within, a specified error band around the final value. To measure a new 18-bit DAC, a settling time measurement technique has been developed with 20-bit (1ppm) resolution for times as short as 265ns. The new method will work with any DAC. Realizing this measurement capability and its performance verification has required an unusually intense, extensive and protracted effort. Hopefully, the data converter community will find the results useful².

DAC settling time is usually specified for a full-scale 10V transition. Figure 1 shows that DAC settling time has three

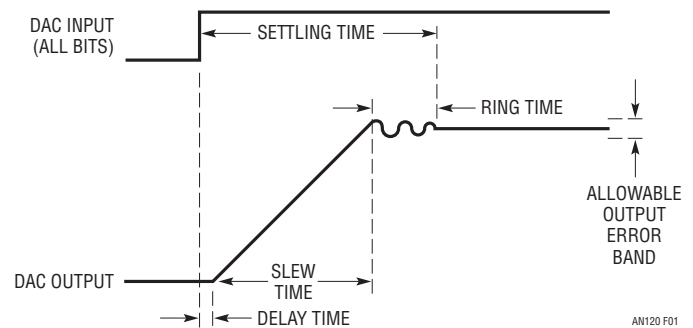


Figure 1. DAC Settling Time Components Include Delay, Slew and Ring Times. Fast Amplifiers Reduce Slew Time, Although Longer Ring Time Usually Results. Delay Time is Normally a Small Term

distinct components. The *delay time* is very small and is almost entirely due to propagation delay through the DAC and output amplifier. During this interval, there is no output movement. During *slew time*, the output amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency

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Note 1. See Appendix A, "A History of High Accuracy Digital-to-Analog Conversion".

Note 2. A historical note is in order. In early 1997, LTC's DAC design group tasked the author to measure 16-bit DAC settling time. The result was published in July 1998 as Application Note 74, "Component and Measurement Advances Ensure 16-Bit DAC Settling Time". Almost exactly 10 years later, the DAC group raised the ante, requesting 18-bit DAC settling time measurement. This constitutes 2 bits of resolution improvement per decade of author age. Since it was unclear how many decades the author (born 1948) had left, it was decided to double jump the performance requirement and attempt 20-bit resolution. In this way, even if the author is unavailable in 10 years, the DAC group will still get its remaining 2 bits.

COMPONENTS FOR 18-BIT D/A CONVERSION

Components suitable for 18-bit D/A conversion are members of an elite class. 18 binary bits is one part in 262,144—just 0.0004% or 4 parts-per-million. This mandates a vanishingly small error budget and the demands on components are high. The LTC2757 digital-to-analog converter listed in the chart uses Si-Chrome thin-film resistors for high stability and linearity over

temperature. Gain drift is typically 0.25ppm/°C or about 4.6LSBs over 0°C to 70°C. Some amplifiers shown contribute less than 1LSB error over 0°C to 70°C with 18-bit DAC driven settling times of 1.8μs available. The references offer drifts as low as 1LSB over 0°C to 70°C with initial trimmed accuracy to 0.05%

Short Form Descriptions of Components Suitable for 18-Bit Digital-to-Analog Conversion

COMPONENT TYPE	ERROR CONTRIBUTION OVER 0°C TO 70°C	COMMENTS
LTC [®] 2757 DAC	≈4.6LSB Gain Drift 1LSB Linearity	Full Parallel Inputs Current Output
LT [®] 1001 Amplifier	<1LSB	Good Low Speed Choice 10mA Output Capability
LT1012 Amplifier	<1LSB	Good Low Speed Choice Low Power Consumption
LT1468/LT1468-2 Amplifier	<8LSB	1.8μs Settling to 18 Bits Fastest Available
LTC1150 Amplifier	<1LSB	Lowest Error. ≈10ms Settling Time. Requires LT1010 Output Buffer. Special Case. See Appendix E
LTZ1000A Reference	<1LSB	Lowest Drift Reference in This Group. 4ppm (1LSB)/Yr. Time Stability Typical
LM199A Reference-6.95V	≈4LSB	Low Drift. 10ppm (2.5LSB) Yr. Time Stability Typical
LT1021 Reference-10V	≈16LSB	Good General Purpose Choice
LT1027 Reference-5V	≈16LSB	Good General Purpose Choice
LT1236 Reference-10V	≈40LSB	Trimmed to 0.05% Absolute Accuracy

compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs which degrade DC error terms³.

Measuring anything at any speed to 20-bit resolution (1ppm) is hard. Dynamic measurement to 20-bit resolution is particularly challenging. Reliable 1ppm DAC settling time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique. This publication's remaining sections describe a method enabling an oscilloscope to accurately display DAC settling time information for a 10V step with 1ppm resolution (10μV) within 265ns. The approach employed permits observation of small amplitude information at the excursion limits of large waveforms without overdriving the oscilloscope.

Considerations for Measuring DAC Settling Time

Historically, DAC settling time has been measured with circuits similar to that in Figure 2. The circuit uses the “false sum node” technique. The resistors and DAC form a bridge type network. Assuming ideal components, the DAC output will step to $-V_{REF}$ when the DAC inputs move to all ones. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half of the DAC's settled voltage.

Note 3. This issue is treated in detail in latter portions of the text. Also see Appendix D, “Practical Considerations for DAC-Amplifier Compensation”.

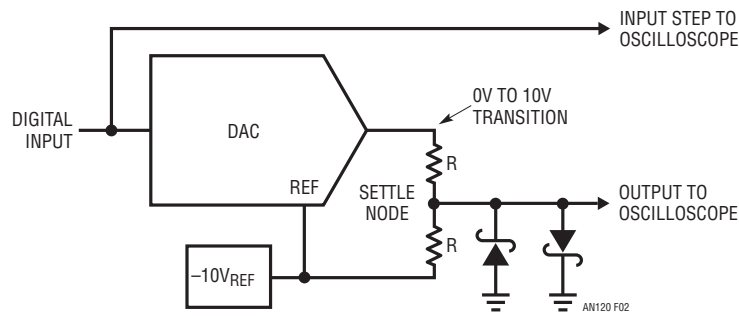


Figure 2. Popular Summing Scheme for DAC Settling Time Measurement Provides Misleading Results. 18-Bit Measurement Causes >800x Oscilloscope Overdrive. Displayed Information is Meaningless

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. A 10pF probe alleviates this problem but its 10x attenuation sacrifices oscilloscope gain. 1x probes are not suitable because of their excessive input capacitance. An active 1x FET probe will work, but a more significant issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question⁴.

At 10-bit resolution (10mV at the DAC output, resulting in 5mV at the oscilloscope), the oscilloscope typically undergoes a 2x overdrive at 50mV/DIV, and the desired 5mV baseline is just discernible. At 12-bit or higher resolution, the measurement becomes hopeless with this arrangement. Increasing oscilloscope gain brings commensurate increased vulnerability to overdrive induced errors. At 18 bits, there is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring 18-bit settling time requires a high gain oscilloscope that is somehow immune to overdrive. The gain issue is addressable with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling 'scope⁵. Unfortunately, these instruments are no longer manufactured (although still available on the secondary market). It is possible, however, to construct a circuit that utilizes sampling techniques to avoid the overload problem. Additionally, the circuit can be endowed with features particularly suited for measuring 20-bit DAC settling time.

Sampling Based High Resolution DAC Settling Time Measurement

Figure 3 is a conceptual diagram of the 20-bit DAC settling time measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the preamplified oscilloscope is connected to the settle point by a switch. The switch state is determined by a delayed pulse generator, which is triggered from the same pulse that controls the DAC. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way, the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

Note 4. For a discussion of oscilloscope overdrive considerations, see Appendix B, "Evaluating Oscilloscope Overdrive Performance".

Note 5. Classical sampling oscilloscopes should not be confused with modern era digital sampling 'scopes that have overdrive restrictions. See Appendix B, "Evaluating Oscilloscope Overload Performance" for comparisons of various type oscilloscopes with respect to overdrive. For detailed discussion of classical sampling oscilloscope operation, see references 17 through 21 and 23 through 25. Reference 18 is noteworthy; it is the most clearly written, concise explanation of classical sampling instruments the author is aware of. A 12-page jewel.

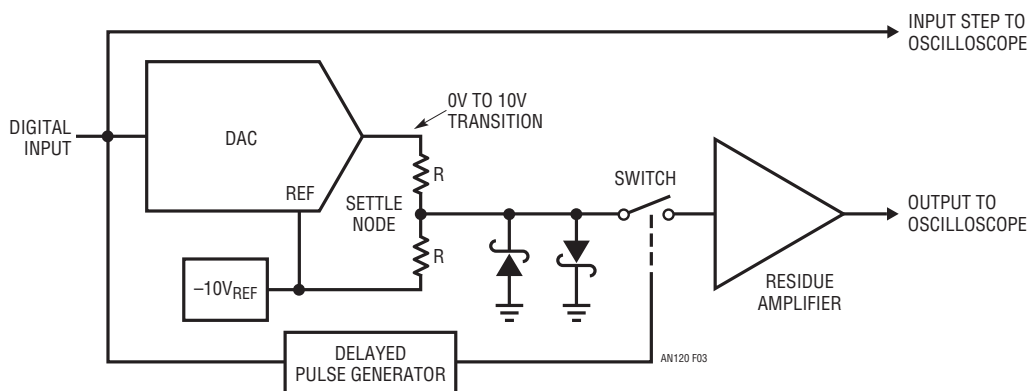


Figure 3. Conceptual Arrangement Eliminates Oscilloscope Overdrive. Delayed Pulse Generator Controls Switch, Preventing Oscilloscope from Monitoring Settle Node Until Settling is Nearly Complete

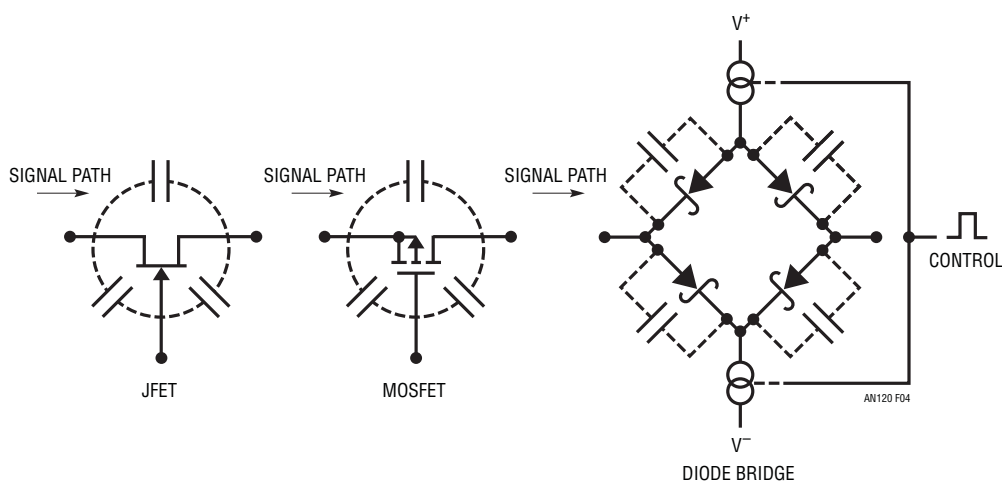


Figure 4. Conventional Choices for the Sampling Switch Include JFET, MOSFET and Diode Bridge. FET Parasitic Capacitances Result in Large Gate Drive Originated Feedthrough to Signal Path. Diode Bridge is Better; Its Small Parasitic Capacitances Tend to Cancel. Bridge Requires DC and AC Trims and Complex Drive Circuitry

Developing a Sampling Switch

Requirements for Figure 3's sampling switch are stringent. It must faithfully pass signal path information without introducing alien components, particularly those deriving from the switch command channel. Figure 4 shows conventional choices for the sampling switch. They include FETs and the diode bridge. The FET's parasitic gate to channel capacitances result in large gate drive originated feedthrough into the signal path. For almost all FETs, this feedthrough is many times larger than the signal to be observed, inducing overload and obviating the switches' purpose. The diode bridge is better; its small parasitic capacitances tend to cancel and the symmetrical, differential structure results in very low feedthrough. Practically, the bridge requires

DC and AC trims and complex drive and support circuitry. This approach, incarnated with great care, can reliably measure DAC settling time to 16-bit resolution⁶. Beyond 16 bits, residual feedthrough becomes objectionable and another approach is needed.

Electronic Switch Equivalents

A low feedthrough, high resolution "switch" can be constructed with wideband active components. The great advantage of this approach is that the switch control channel can be maintained "in-band"; that is, its transition

Note 6. LTC Application Note 74, "Component and Measurement Advances Ensure 16-bit DAC Settling Time" utilized such a sampling bridge and it is detailed in that text.

rate is within the circuits' bandpass. The circuit's wide bandwidth means the switch command transition is under control at all times. There are no out-of-band responses, greatly reducing feedthrough. Figure 5 lists some candidates for low feedthrough electronic switch equivalents. A and B, while theoretically possible, are cumbersome to implement. C and D are practical. C must be optimized for low feedthrough on rising and falling control pulse edges because of the multiplier's unrestricted wideband response. D's falling edge feedthrough is inherently minimized by the g_m amplifier's transconductance collapse when the control pulse goes low. This allows feedthrough to be optimized for the control pulse's rising edge without regard to falling edge effects. This is a significant advantage in constructing an electronic equivalent switch.

Transconductance Amplifier Based Switch Equivalent

Figure 6 is a conceptual transconductance amplifier based "switch". The wideband control and signal paths faithfully track 1000:1 transconductance change, resulting in exceptionally pure switch dynamics. The switched current source is carefully optimized for lowest feedthrough on the rising control edge without regard to falling edge characteristics. The g_m amplifier's transconductance

collapse on the falling edge ensures low feedthrough for that condition, preventing oscilloscope overdrive. Figure 7 details the transconductance amplifier-based switch. This design switches signals over a $\pm 30\text{mV}$ range with peak control channel feedthrough of millivolts and settling times inside 40ns.

The circuit approximates switch action by varying A1A's transconductance; the maximum gain is unity. At low transconductance, A1A's gain is nearly zero, and essentially no signal is passed. At maximum transconductance, signal

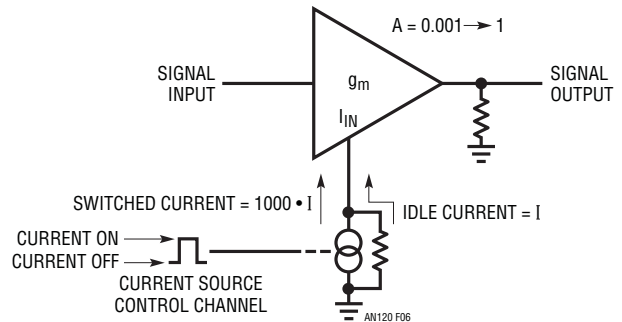


Figure 6. Transconductance Amplifier Based "Switch" Has Minimal Control Channel Feedthrough. Wideband Control and Signal Paths Faithfully Track 1000:1 Transconductance Change, Resulting in Exceptionally Pure Switch Dynamics

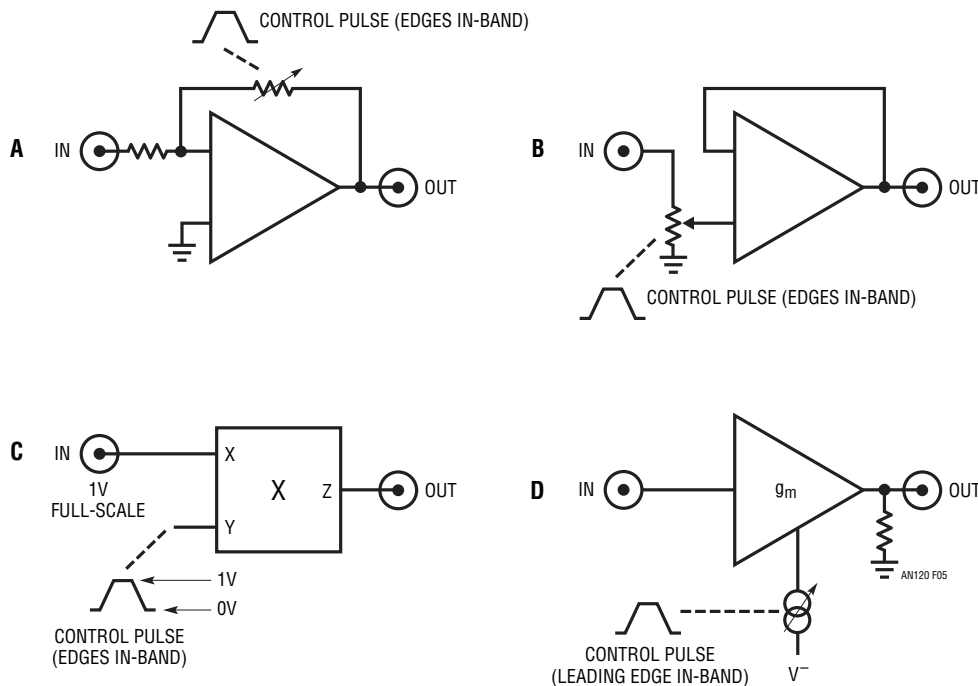


Figure 5. Conceptual Low Feedthrough Electronic Switch Equivalents. A and B are Difficult to Implement, C and D are Practical. C Must be Optimized for Low Feedthrough on Rising and Falling Control Pulse Edges. D's Falling Edge Feedthrough is Inherently Minimized by Attendant Bandwidth Reduction

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Application Note 120

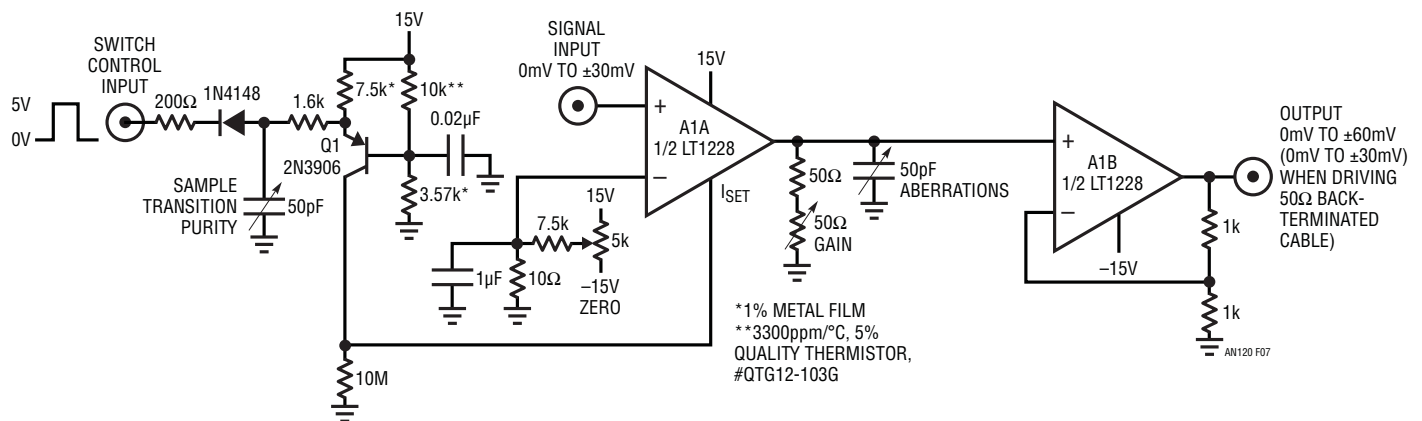


Figure 7. Transconductance Amplifier-Based 100MHz Low Level Switch Has Minimal Control Channel Feedthrough. A1A's Unity-Gain Output is Cleanly Switched by Logic Controlled Q1's Transconductance Bias. A1B Provides Buffering and Signal Path Gain

passes at unity gain. The amplifier and its transconductance control channel are very wideband, permitting them to faithfully track rapid variations in transconductance setting. This characteristic means the amplifier is never out of control, affording clean response and rapid settling to the “switched” input’s value.

A1A, one section of an LT1228, is the wideband transconductance amplifier. Its voltage gain is determined by its output resistor load and the current magnitude into its “I_{SET}” terminal. A1B, the second LT1228 section, unloads A1A’s output. As shown, it provides a gain of 2, but when driving a back-terminated 50Ω cable, its effective gain is unity at the cable’s receiving end. The back termination enforces a 50Ω environment. Current source Q1, controlled by the “switch control input”, sets A1A’s transconductance, and, hence, gain. With Q1 gated off (control input at zero), the 10M resistor supplies about 1.5μA into A1A’s I_{SET} pin, resulting in a voltage gain of nearly zero, blocking the input signal. When the switch control input goes high, Q1 turns on, sourcing approximately 1.5mA into the I_{SET} pin. This 1000:1 set current change forces maximum transconductance, causing the amplifier to assume unity gain and pass the input signal. Trims for zero and gain ensure accurate input signal replication at the circuit’s output. The Q1 associated 50pF variable capacitor purifies turn-on switching. The specified 10k resistor at Q1 has a 3300ppm/°C temperature coefficient, compensating A1A’s complementary transconductance temperature dependence to minimize gain drift.

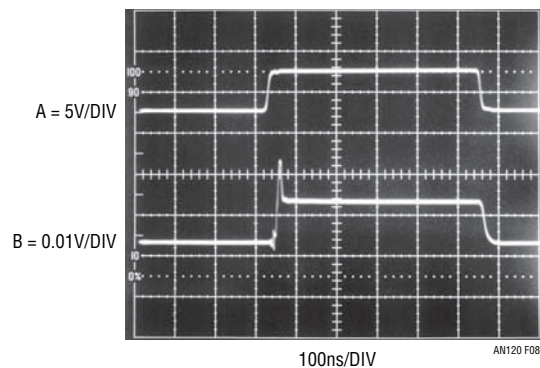


Figure 8. Control Input (Trace A) Dictates Switch Output’s (Trace B) Representation of 0.01V DC Input. Control Channel Feedthrough, Evident at Switch Turn-On, Settles in 20ns. Turn-Off Feedthrough is Undetectable Due to Deceased Signal Channel Transconductance and Bandwidth. C_{ABERRATION} ≈ 35pF for this Test

Figure 8 shows circuit response for a switched 10mV DC input and C_{ABERRATION} = 35pF. When the control input (trace A) is low, no output (trace B) occurs. When the control input goes high, the output reproduces the input with “switch” feedthrough settling in about 20ns. Note that turn-off feedthrough is undetectable due to the 1000x transconductance reduction and attendant 25x bandwidth drop. Figure 9 speeds the sweep up to 10ns/division to examine zero volt settling detail. The output (trace B) settles inside 1mV 40ns after the switch control (trace A) goes high. Peak feedthrough excursion, damped by C_{ABERRATION}, is only 5mV. Figure 10 was taken under identical conditions, except that C_{ABERRATION} = 0pF. Feedthrough

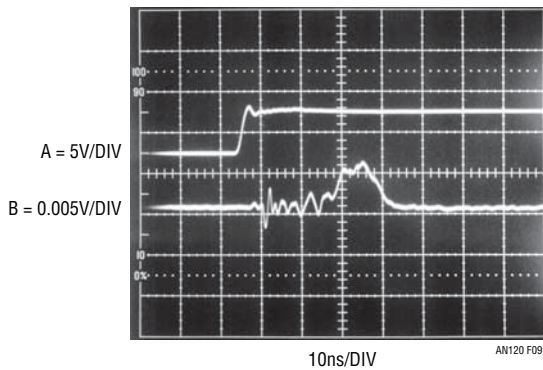


Figure 9. High Speed Delay and Feedthrough for 0V Signal Input. Output (Trace B) Peaks Only 0.005V Before Settling Inside 0.001V 40ns After Switch Control Command (Trace A). $C_{ABERRATION} \approx 35\text{pF}$ for This Test

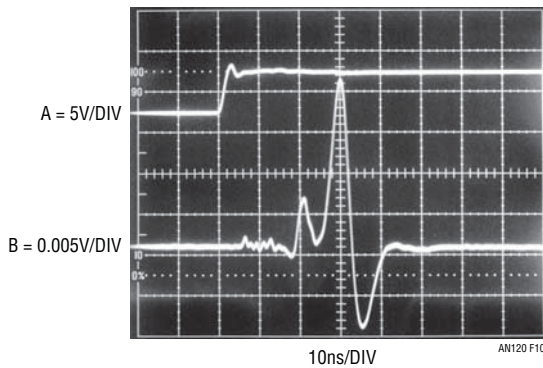


Figure 10. Identical Conditions as Figure 9 Except $C_{ABERRATION} = 0\text{pF}$. Feedthrough Related Peaking Increases to $\approx 0.02\text{V}$; 0.001V Settling Time Remains at 40ns

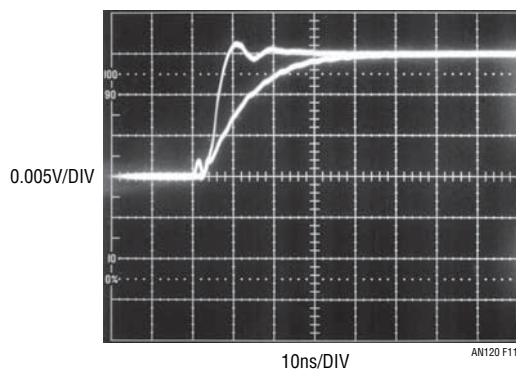


Figure 11. Signal Channel Rise Time for $C_{ABERRATION} = 0\text{pF}$ (Leftmost Trace) and $\approx 35\text{pF}$ (Rightmost Trace) Record 3.5ns and 25ns, Respectively. Switch Control Input High for this Measurement. Photograph Utilizes Double Exposure Technique

increases to approximately 20mV, although settling time to 1mV remains at 40ns. Figure 11, using double exposure technique, compares signal channel rise times for $C_{ABERRATION} = 0\text{pF}$ (leftmost trace) and approximately 35pF (rightmost trace) with the control channel tied high. The larger $C_{ABERRATION}$ value, while minimizing feedthrough amplitude (see Figure 9), increases rise time by 7x versus $C_{ABERRATION} = 0\text{pF}$.

The transconductance switches' small DC and AC errors nicely accommodate the applications' requirements. The low feedthrough, already sufficient, becomes irrelevant because its small time and amplitude error will be buried in the DAC ring time interval. The transconductance amplifier based "switch" points the way towards practical 1ppm DAC settling time measurement.

DAC Settling Time Measurement Method

Figure 12, a more complete representation of Figure 3, utilizes the above described sampling switch. Figure 3's blocks appear in greater detail and some new refinements show up. The DAC-amplifier summing area is unchanged. Figure 3's delayed pulse generator has been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that compensates settling time-measurement path propagation delay. This path includes settle node, amplifier and sample gate delays. The transconductance sampling switch ("sample gate"), driven from a non-saturating residue amplifier, feeds the oscilloscope. Placing the sampling switch after the residue amplifier gain further minimizes sample command feedthrough impact.

Detailed Settling Time Circuitry

Figure 13 is a detailed schematic of the 20-bit DAC settling time measurement circuitry. The input pulse switches all DAC bits simultaneously and is also routed to the oscilloscope via the delay compensation network. The delay network, composed of CMOS inverters and an adjustable RC network, compensates the oscilloscope's input step signal for the 44ns delay through the circuit measurement path⁷. The DAC-amplifier output is compared against the

Note 7. See Appendix C, "Measuring and Compensating Signal Path Delay and Circuit Trimming Procedures".

Application Note 120

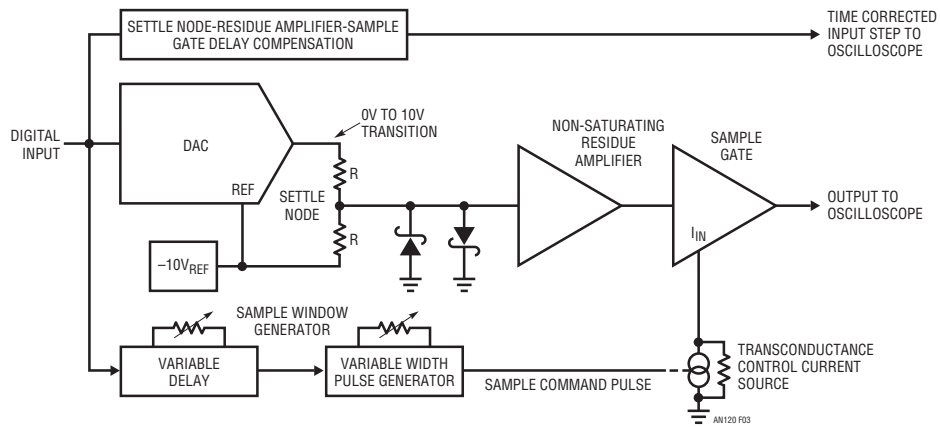


Figure 12. Block Diagram of Sampling-Based DAC Settling Time Measurement Scheme. Placing Transconductance Controlled Sample Gate After Residue Amplifier Minimizes Sample Command Feedthrough Impact, Eliminating Oscilloscope Overdrive. Input Step Time Reference is Compensated for Settle Node, Residue Amplifier and Sample Gate Delays

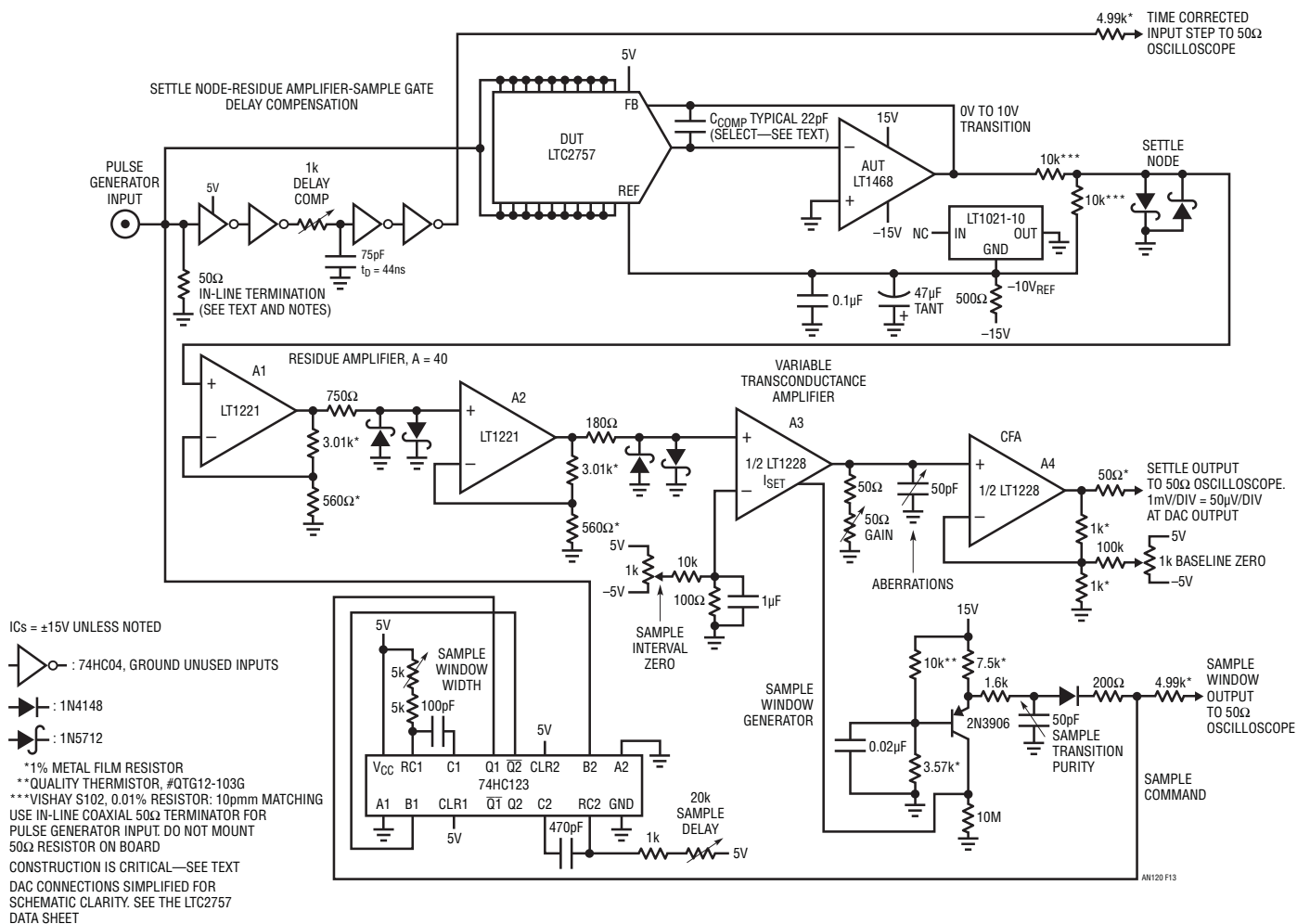


Figure 13. Detailed DAC Settling Time Measurement Circuit Closely Follows Preceding Figure. Optimum Performance Requires Attention to Layout

LT1021 10V reference via the precision 10k summing resistors. The LT1021 also furnishes the DAC reference, making the measurement ratiometric. The clamped settle node is unloaded by A1, which takes gain. A2 provides additional clamped gain for a total summing node referred amplification of 40. A2's output feeds the sampling switch whose operation is identical to Figure 7's description. The A1-A2 amplifier's clamping and gain are arranged so saturation never occurs—the amplifier is always in its active region.

The input pulse triggers the 74HC123 dual one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets sampling switch on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining activity is observable. In this way, the oscilloscope output is reliable and meaningful data may be taken.

Figure 14 shows circuit waveforms. Trace A is the time corrected input pulse, trace B the sample gate, trace C the DAC-amplifier output and trace D the circuit output. When the sample gate goes high, trace D's switching is clean, the last millivolt of ring time is easily observed and the amplifier settles nicely to final value bounded by broadband noise. When the sample gate goes low, the transconductance switch goes off and no feedthrough is discernible. Note that there is no off-screen activity at any time—the oscilloscope is never subjected to overdrive.

The circuit requires trimming to achieve this level of performance⁸. Figure 15 shows a typical display resulting from poor "Sample Interval Zero" adjustment. This

adjustment, corrected in Figure 16, results in a continuous baseline. Sample command feedthrough is just visible at trace B's leading edge. Figure 17 shows output response (trace B) to the sample command (trace A) turn-on before trimming "aberrations" and "transition purity"⁹. Delay is approximately 20ns with aberrations peaking 350μV and

Note 8. To maintain text flow and focus, trimming procedures are not presented here. Detailed trimming information appears in Appendix C.

Note 9. A1's positive input was grounded via 5kΩ (precision 10k resistors disconnected) for Figure 17 and 18's tests.

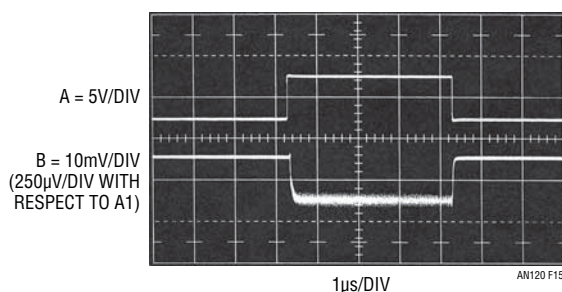


Figure 15. Poor Sample Interval Zero Adjustment Causes Shifted Output Baseline (Trace B) During Trace A's Sample Interval

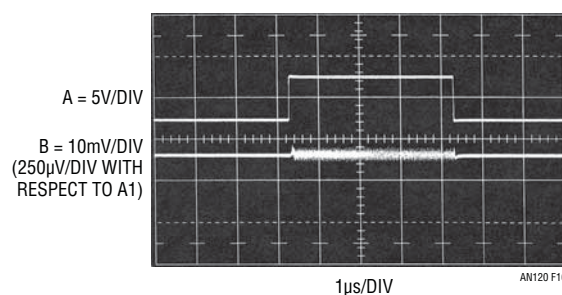


Figure 16. Trimmed Sample Interval Zero Has No Output Baseline Deviation (Trace B) During Sample Interval (Trace A). Sample Command Feedthrough is Just Visible at Trace B's Leading Edge

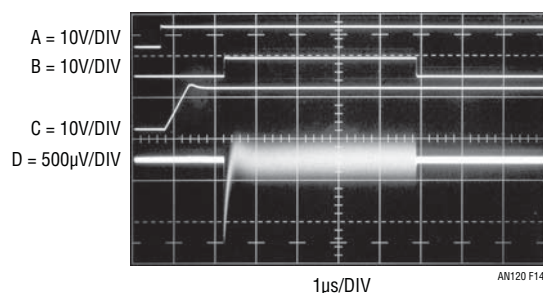


Figure 14. Settling Time Circuit Waveforms Include Time Corrected Input Pulse (Trace A), Sample Command (Trace B), DAC Output (Trace C) and Settling Time Output (Trace D). Sample Window Delay and Width are Variable

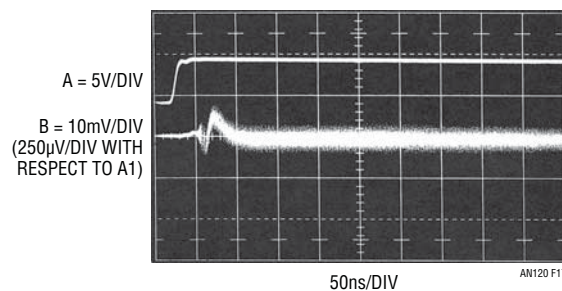


Figure 17. Output Response (Trace B) To Sample Command (Trace A) Turn-On Before Trimming Aberrations and Transition Purity. Delay is ≈20ns. Aberrations Peak 350μV, Settle in 50ns. A1's Positive Input Grounded via 5kΩ for This and Succeeding Figures

an120f

Application Note 120

settling in 50ns. Figure 18 shows post trim response to sample command turn-on. Delay increases to 70ns but aberrations peak only 50 μ V, settling in 50ns. Figure 19 shows output response (trace B) to sample command (trace A) turn-off. The 1000:1 transconductance drop ensures a clean transition independent of the turn-on optimized trims.

Circuit gain is adjusted with the indicated potentiometer.

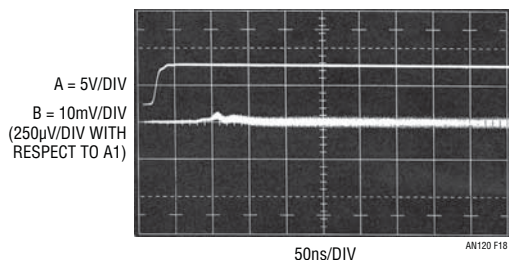


Figure 18. Post-Trim Output Response (Trace B) To Sample Command Turn-On, Trace A. Delay Increases to 70ns but Aberrations Peak Only 50 μ V, Settling in 50ns

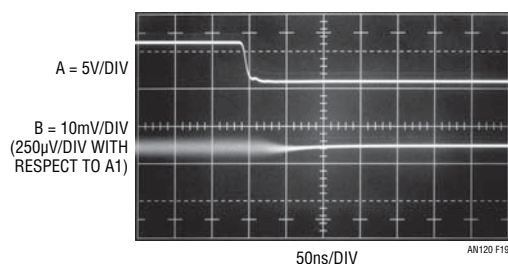


Figure 19. Output Response (Trace B) To Sample Command (Trace A) Turn-Off. 1000:1 Transconductance Drop Ensures Clean Transition, Independent of Trim State

Settling Time Circuit Performance

Figure 20 summarizes settling time circuit performance. The graph indicates the minimum measurable settling time for a given resolution. Speed limitations are imposed by sample command path delays and sample gate switching residue profile¹⁰. Minimum measurable settling time below 160ns is available to 16-bit resolution. Beyond this point, the sample gate's switching residue profile dictates increased minimum measurable settling time to about 265ns at 20 bits. Circuit noise limitations are imposed by the DAC/amplifier, summing resistors, and residue amplifier/sampling switch with about equal weighting. Because of this, resolution beyond approximately 15ppm requires filtering or noise averaging techniques.

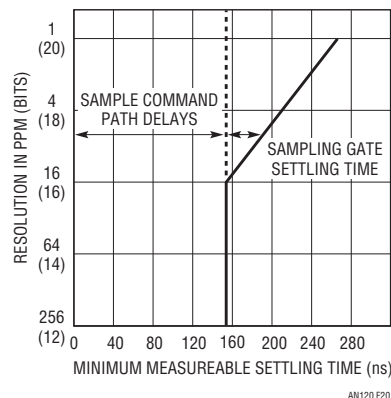


Figure 20. Minimum Measurable Settling Time vs Resolution. Limits are Imposed by Sample Command Path Delays and Sample Gate Settling Profile. Resolution Beyond \approx 15ppm Requires Filtering or Noise Averaging

Using the Sampling-Based Settling Time Circuit

It is good practice to “walk” the sampling window backwards in time from the settled region up to the last 100 μ V or so of amplifier movement so ring time cessation is observable. The sampling-based approach provides this capability and it is a very powerful measurement tool. Additionally, slower amplifiers may require extended delay and/or sampling window times. This may necessitate larger capacitor values in the 74HC123 one-shot timing networks.

Figure 21 shows DAC settling in an unfiltered bandpass. The DAC settles (trace B) to 16 bits 1.7 μ s after trace A's time corrected input step¹¹. Sample gate feedthrough is undetectable, indicating higher resolution is possible without overdriving the oscilloscope. Noise is the fundamental measurement limit. Figure 22 attenuates noise by reducing measurement bandwidth to 250kHz. Trace assignments are as in the previous photo. 18-bit settling (4ppm) requires approximately 5 μ s. The reduced bandwidth permits higher resolution although the indicated settling time is likely pessimistic due to the filter's lag. Figure 23, decreasing bandwidth to 50kHz, permits 19-bit (2ppm) resolution with indicated settling in about 9 μ s. Again, the same filtering which permits high resolution almost certainly lengthens observed settling time.

Note 10. Driving the sample command path (74HC123 B2 input) with a phase-advanced version of the pulse generator input largely eliminates sample command path delay induced error, considerably improving minimum measurable settling time. This benefit is not germane to the present efforts purposes and was not implemented

Note 11. Settling time is significantly affected by the DAC-amplifier compensation capacitor. See Appendix D, “Practical Considerations for DAC-amplifier Compensation” for tutorial.

an120f

Figure 24 uses noise averaging techniques to measure settling time to 20 bits (1ppm-10 μ V) without the band limiting filter's time penalty¹². Photo A shows the DAC-amplifier adjusted for overdamped response, B and C

underdamped and optimum responses, respectively. Averaging eliminates noise, permitting determination of settling time due to DAC dynamics¹³. Settling time ranges from 4 μ s to 6 μ s with fractional LSB tailing evident.

Note: This application note was derived from a manuscript originally prepared for publication in EDN magazine.

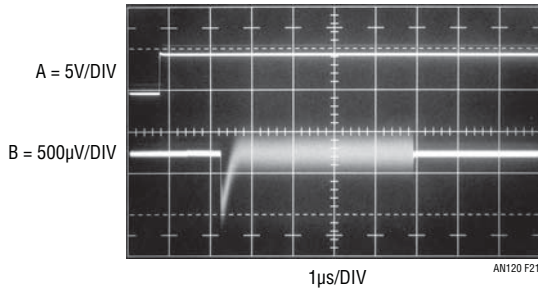


Figure 21. 0V to 10V DAC Settling in Unfiltered Bandpass. DAC Settles (Settle Output, Trace B) to 16 Bits (15ppm) <2 μ s After Trace A's Time Corrected Input Step. Sample Gate Feedthrough is Well Controlled, Indicating Higher Resolution is Possible Without Overdriving Oscilloscope. Noise Limits Measurement

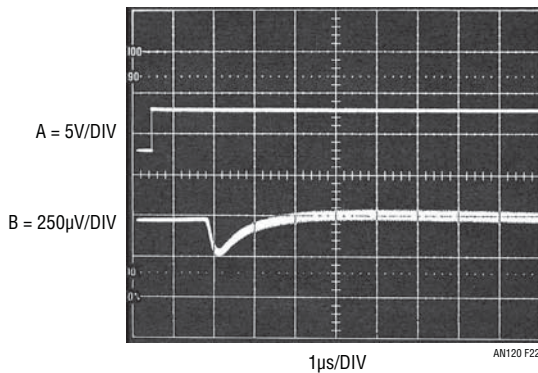


Figure 22. Same Trace Assignments as Previous Photo; Measurement Taken in 250kHz Bandpass. Settling to 18 Bits (4ppm) Requires \approx 5 μ s. Filtering Permits Increased Resolution Although Indicated Settling Time Increases

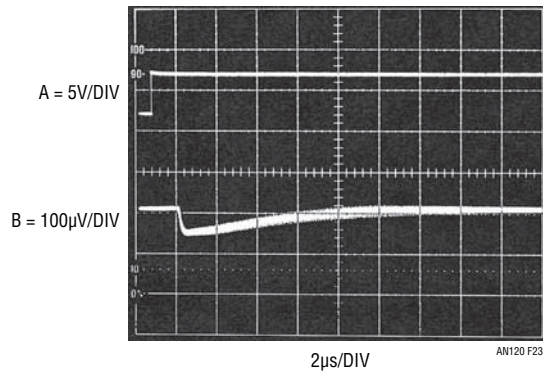
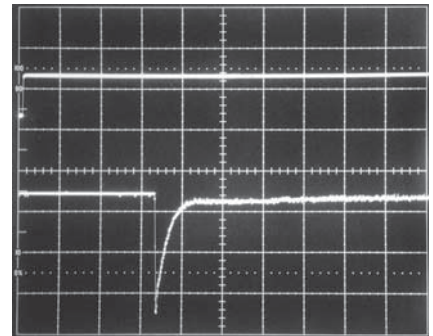
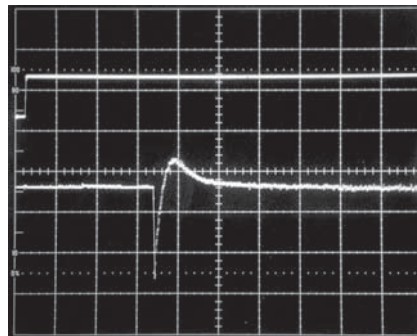
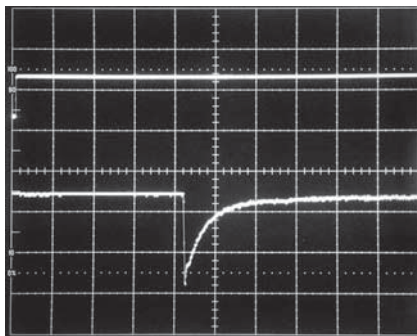


Figure 23. 19 Bit (2ppm) Settling is Discernable About 9 μ s After Input Command in 50kHz Bandwidth



ALL PHOTOS
TRACE A = 5V/DIV
TRACE B = 25 μ V/DIV (AVERAGED)
HORIZ = 1 μ s/DIV

A

B

C

AN120 F24

Figure 24. Noise Averaging Oscilloscope Permits 1ppm, (10 μ V) Settling Time Measurement Without Bandlimiting Filter Time Penalty. Photo A Shows Overdamped Response, B and C Underdamped and Optimum Responses, Respectively. Averaging Eliminates Noise, Permitting Determination of Settling Time Due To DAC Dynamics. Settling Times Range From 4 μ s to 6 μ s; Fractional LSB Tailing is Evident

an120f

Application Note 120

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APPENDIX A

A HISTORY OF HIGH ACCURACY DIGITAL-TO-ANALOG CONVERSION

People have been converting digital-to-analog quantities for a long time. Probably among the earliest uses was the summing of calibrated weights (Figure A1, left) in weighing applications. Early electrical digital-to-analog conversion inevitably involved switches and resistors of different values, usually arranged in decades. The application was often the calibrated balancing of a bridge or reading, via null detection, some unknown voltage. The most accurate resistor-based DAC of this type is Lord Kelvin's Kelvin-Varley divider (Figure, large box). Based on switched resistor ratios, it can achieve ratio accuracies of 0.1 ppm (23+ bits) and is still widely employed in standards laboratories. High speed digital-to-analog conversion resorts to electronically switching the resistor network. Early electronic DACs were built at the board level using discrete precision resistors and Germanium transistors (Figure, center foreground, is a 12-bit DAC from a Minuteman missile D-17B inertial

navigation system, circa 1962). The first electronically switched DACs available as standard product were probably those produced by Pastoriza Electronics in the mid 1960s. Other manufacturers followed and discrete-and monolithically-based modular DACs (Figure, right and left) became popular by the 1970s. The units were often potted (Figure, left) for ruggedness, performance or to (hopefully) preserve proprietary knowledge. Hybrid technology produced smaller package size (Figure, left foreground). The development of Si-Chrome resistors permitted precision monolithic DACs such as the LTC2757 (Figure, immediate foreground). In keeping with all things monolithic, the cost-performance trade-off of modern high resolution IC DACs is a bargain. Think of it! An 18-bit DAC in an IC package. What Lord Kelvin would have given for a credit card and LTC's phone number.

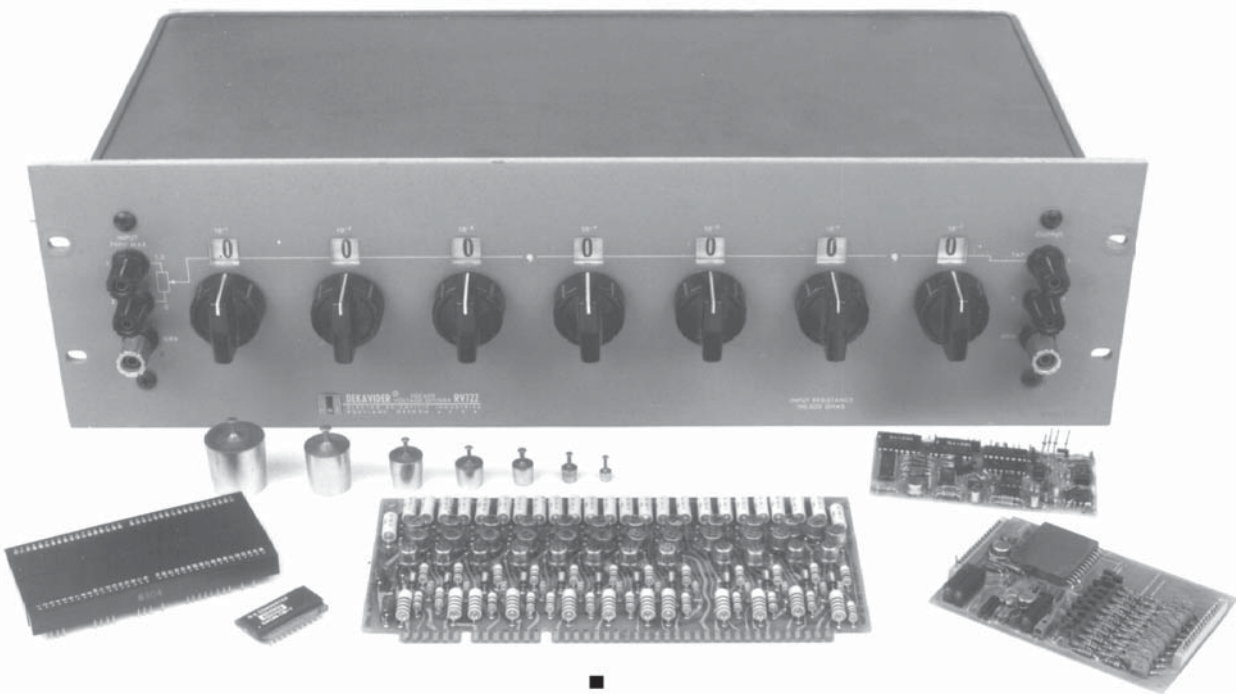


Figure A1. Historically Significant Digital-to-Analog Converters Include: Weight Set (Center Left), 23+ Bit Kelvin-Varley Divider (Large Box), Hybrid, Board and Modular Types, and the LTC2757 IC (Foreground). Where Will It All End?

APPENDIX B

EVALUATING OSCILLOSCOPE OVERDRIVE PERFORMANCE

The settling-time circuit is heavily oriented towards eliminating overdrive at the monitoring oscilloscope. Oscilloscope recovery from overdrive is a murky area and almost never specified. How long must one wait after an overdrive before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overdrive, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overdrive varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100x overload at 0.005V/DIV may be very different than at 0.1V/DIV. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overdrive must be approached with caution.

Why do most oscilloscopes have so much trouble recovering from overdrive? The answer to this question requires some study of the three basic oscilloscope types' vertical paths. The types include analog (Figure B1A), digital (Figure B1B) and classical sampling (Figure B1C) oscilloscopes. Analog and digital 'scopes are susceptible to overdrive. The classical sampling 'scope is the only architecture that is inherently immune to overdrive.

An analog oscilloscope (Figure B1A) is a real-time, continuous linear system¹. The input is applied to an attenuator, which is unloaded by a wideband buffer. The vertical preamp provides gain, and drives the trigger pick-off, delay line and the vertical output amplifier. The attenuator and delay line are passive elements and require little comment. The buffer, preamp and vertical output amplifier are complex linear gain blocks, each with dynamic operating range restrictions. Additionally, the operating point of each block may be set by inherent circuit balance, low frequency stabilization paths or both. When the input is overdriven, one or more of these stages may saturate, forcing internal nodes and components to abnormal operating points and temperatures. When the overload ceases, full recovery of the electronic and thermal time constants may require surprising lengths of time².

The digital sampling oscilloscope (Figure B1B) eliminates the vertical output amplifier, but has an attenuator buffer and amplifiers ahead of the A/D converter. Because of this, it is similarly susceptible to overdrive recovery problems.

The classical sampling oscilloscope is unique. Its nature of operation makes it inherently immune to overload. Figure B1C shows why. The sampling occurs before any gain is taken in the system. Unlike Figure B1B's digitally sampled 'scope, the input is fully passive to the sampling point. Additionally, the output is fed back to the sampling bridge, maintaining its operating point over a very wide range of inputs. The dynamic swing available to maintain the bridge output is large and easily accommodates a wide range of oscilloscope inputs. Because of all this, the amplifiers in this instrument do not see overload, even at 1000x overdrives, and there is no recovery problem. Additional immunity derives from the instrument's relatively slow sample rate—even if the amplifiers were overloaded, they would have plenty of time to recover between samples³.

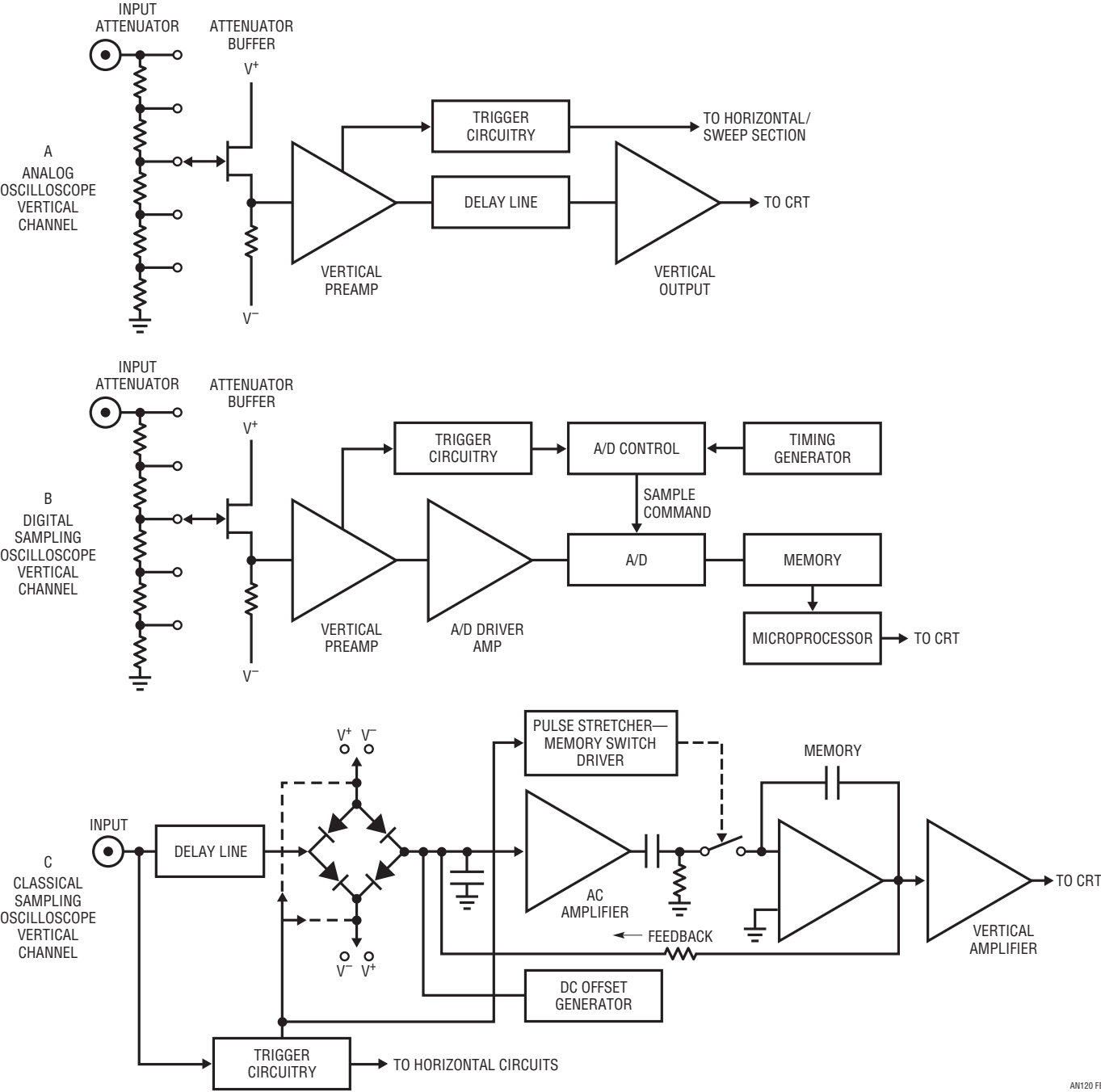
The designers of classical sampling 'scopes capitalized on the overdrive immunity by including variable DC offset generators to bias the feedback loop (see Figure B1C, lower right). This permits the user to offset a large input, so small amplitude activity on top of the signal can be accurately observed. This is ideal for, among other things, settling time measurements. Unfortunately, classical sampling oscilloscopes are no longer manufactured, so if you have one, take care of it!

Although analog and digital oscilloscopes are susceptible to overdrive, many types can tolerate some degree of this abuse. The early portion of this Appendix stressed that measurements involving oscilloscope overdrive must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

Note 1: Ergo, the Real Thing. Hopelessly bigoted residents of this locale mourn the passing of the analog 'scope era and frantically hoard every instrument they can find.

Note 2: Some discussion of input overdrive effects in analog oscilloscope circuitry is found in reference 13.

Note 3: Additional information and detailed treatment of classical sampling oscilloscope operation appears in references 17-20 and 23-25.



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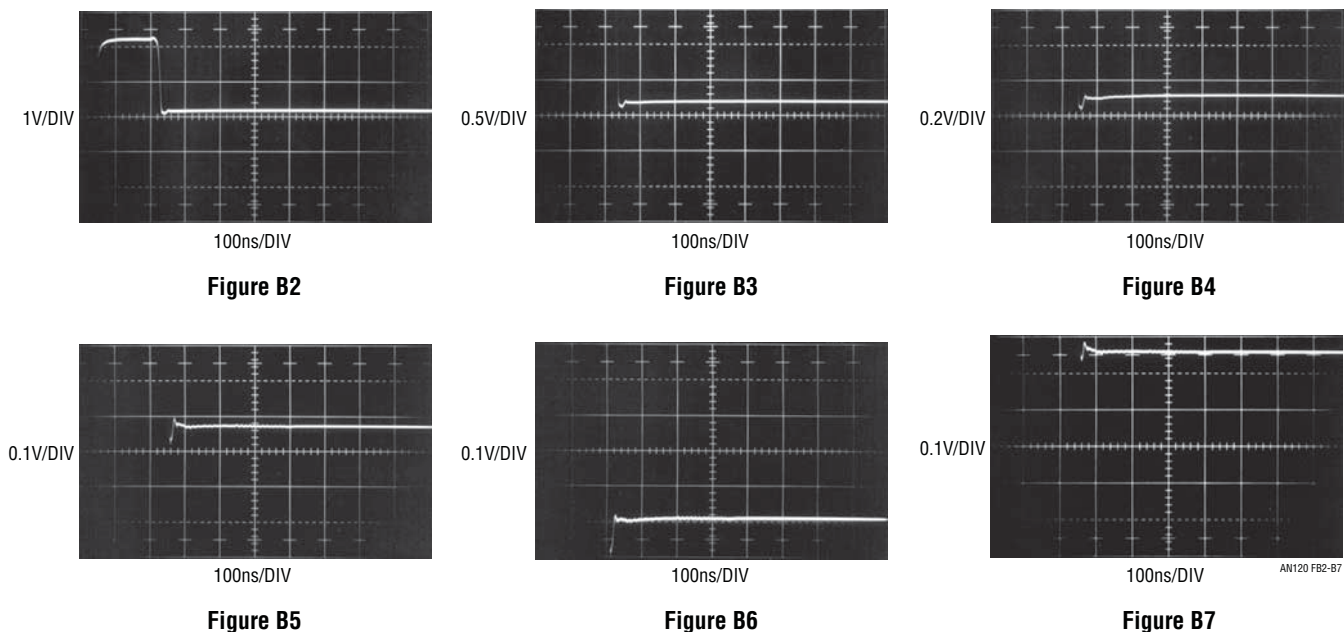
Figure B1. Simplified Vertical Channel Diagrams for Different Type Oscilloscopes. Only the Classical Sampling Scope (C) Has Inherent Overdrive Immunity. Offset Generator Allows Viewing Small Signals Riding on Large Excursions

Application Note 120

The waveform to be expanded is placed on the screen at a vertical sensitivity that eliminates all off-screen activity. Figure B2 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure B3) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure B4, gain has been further increased, and all the features of Figure B3 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure B5 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears

less broad than in Figure B4. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure B6, gain remains the same but the vertical position knob has been used to reposition the display at the screen's bottom.⁴ This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure B7). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

Note 4: *Knobs* (derived from Middle English, "knobbe", akin to Middle Low German, "knubbe"), cylindrically shaped, finger rotatable panel controls for controlling instrument functions, were utilized by the ancients.



Figures B2-B7. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

APPENDIX C

MEASURING AND COMPENSATING SIGNAL PATH DELAY AND CIRCUIT TRIMMING PROCEDURES

Delay Compensation

The settling time circuit utilizes an adjustable delay network to time correct the input pulse for delays in the signal-processing path. Typically, these delays introduce errors of a few percent, so a first-order correction is adequate. Setting the delay trim involves observing the network's input-output delay and adjusting for the appropriate time interval. Determining the "appropriate" time interval is somewhat more complex. Measuring the settling time circuit's signal path delay involves modifications to Figure 13, shown in Figure C1. These changes lock the circuit into its "sample" mode, permitting an input-to-output delay measurement under signal-level conditions similar to normal operation. In Figure C2, trace A is the

pulse-generator input at 200 μ V/DIV (note 10k-1 Ω divider feeding the settle node). Trace B shows the circuit output at A4, delayed by about 44ns. This delay is a small error, but is readily corrected by adjusting the delay network for the same time lag. If appendix F's serial interface is utilized, 10ns should be added to the delay correction. Similarly, if appendix I's post amplifier is used, the delay correction must be increased by 17ns.

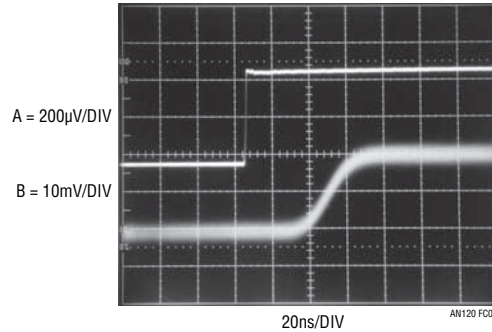


Figure C2. Sampling Circuit Input-Output Delay Measures About 44ns

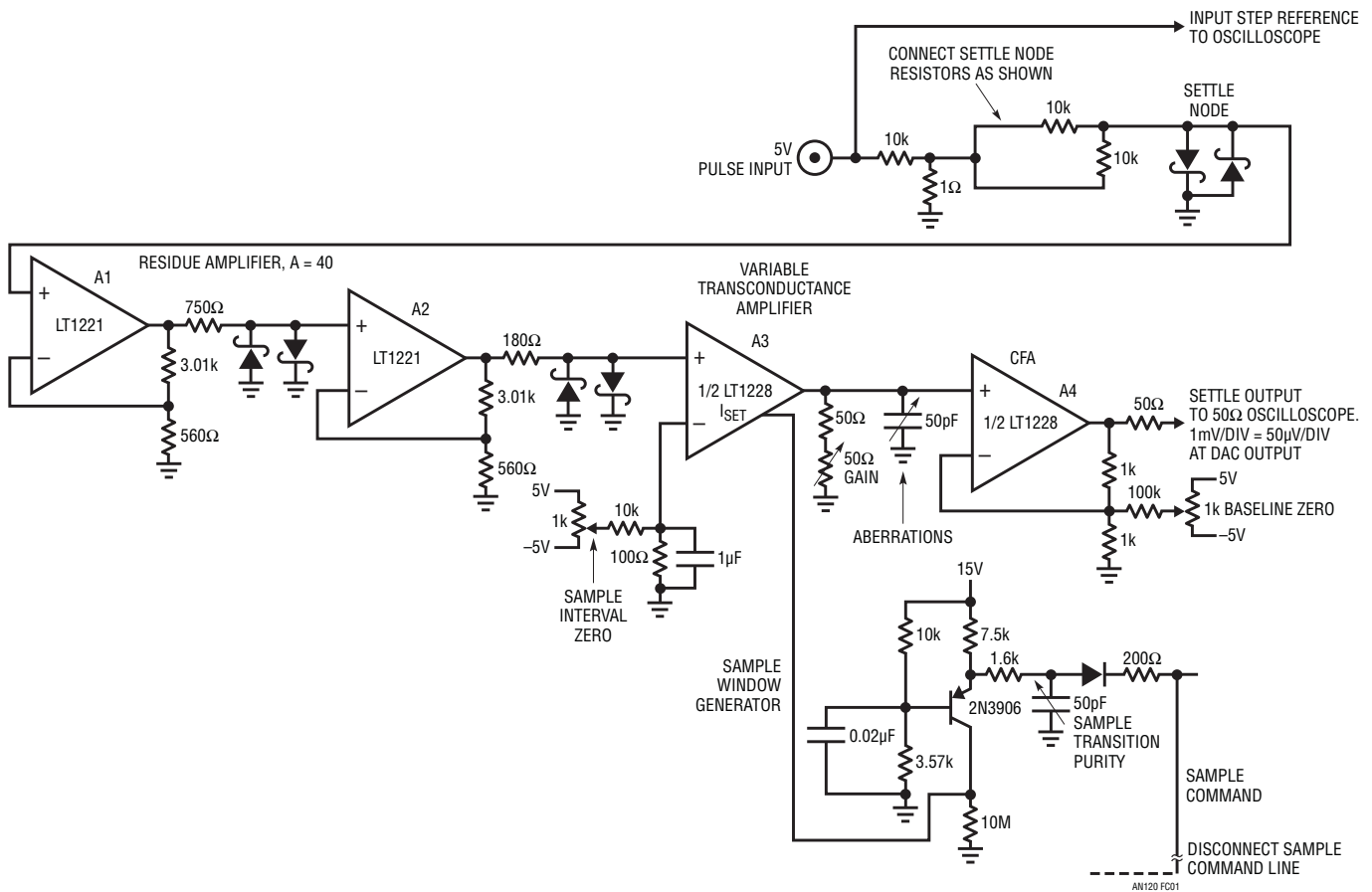


Figure C1. Partial Text Figure 13 Schematic Shows Modifications for Measuring Signal Path Delay. Changes Lock Circuit into Sample Mode, Permitting Input-to-Output Delay Measurement

an120f

Application Note 120

Circuit Trimming Procedure

The following procedure, given in numerical order, trims the settling time circuit for optimum performance. It is advisable to execute trimming in the order given, avoiding out-of-sequence adjustments.

1. Turn off input pulses.
2. Trim “Baseline Zero” for 0V out at oscilloscope at 10mV per division or less.
3. Disconnect precision 10k resistors and ground settle node via 5.1k Ω .
4. Set sample delay to mid-range, sample window width to minimum.
5. Drive pulse generator input with 40kHz square wave.
6. Adjust “Sample Interval Zero” for no offset between the sample interval and the unsampled baseline¹.
7. Adjust “Sample Transition Purity” and “Aberration” trims for minimum amplitude disturbances when the sample gate opens with oscilloscope horizontal at 50ns per division and vertical sensitivity of 10mV per division.
8. Reconnect precision 10k resistors and remove 5.1k Ω unit from the settle node.
9. Adjust “Delay Compensation” for 44ns delay from the pulse generator input to the time corrected output pulse.

10. Turn off input pulses. Disconnect the pulse generator and its 50 Ω termination. Apply 5V DC to the pulse input.
11. Connect Figure C3’s network to the settle node. The added components shown furnish a 250 μ V DC gain calibration source when the input pulses are replaced by a 5V level. Under the figure’s conditions, the DAC assumes a 10V output with the 5.1k resistor mimicking the 10k Ω divider output impedance at A1. Figure 13’s “Gain” trim is adjusted for a 10mV DC deflection at the oscilloscope. This completes the trimming procedure and the circuit is ready for use.

Note 1. The “Sample Interval Zero” trim is unnecessary if Appendix I’s optional auto-zero circuitry is used.

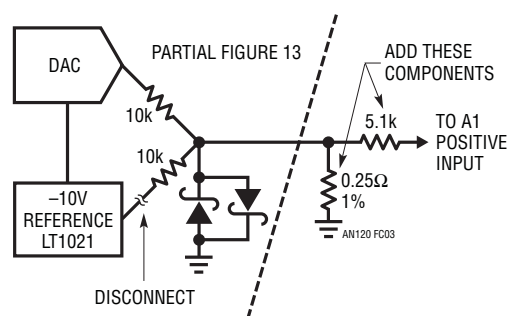


Figure C3. Added Components Furnish 250 μ V Gain Calibration Source with Input Pulses Replaced by 5V Level. DAC Output Assumes 10V Reference Potential Under These Conditions; 5.1k Resistor Mimics 10k Ω Divider Output Impedance at A1

APPENDIX D

PRACTICAL CONSIDERATIONS FOR DAC-AMPLIFIER COMPENSATION

There are a number of practical considerations in compensating the DAC-amplifier pair to get fastest settling time. Our study begins by revisiting text Figure 1 (repeated here as Figure D1). Settling time components include delay, slew and ring times. Delay is due to propagation time through the DAC-amplifier and is a very small term. Slew time is set by the amplifier’s maximum speed. Ring time defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. Once a DAC-amplifier pair have been chosen, only ring time is

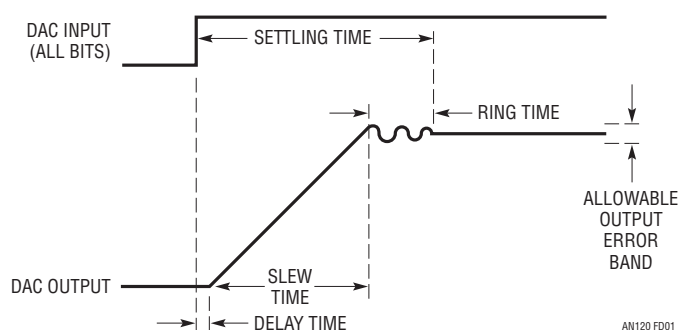


Figure D1. DAC-Amplifier Settling Time Components Include Delay, Slew and Ring Times. For Given Components, Only Ring Time is Readily Adjustable

readily adjustable. Because slew time is usually the dominant lag, it is tempting to select the fastest slewing amplifier available to obtain best settling. Unfortunately, fast slewing amplifiers usually have extended ring times, negating their brute force speed advantage. The penalty for raw speed is, invariably, prolonged ringing, which can only be damped with large compensation capacitors. Such compensation works, but results in protracted settling times. The key to good settling times is to choose an amplifier with the right balance of slew rate and recovery characteristics and compensate it properly. This is harder than it sounds because amplifier settling time cannot be predicted or extrapolated from any combination of data sheet specifications. It must be measured in the intended configuration. In the case of a DAC-amplifier, a number of terms combine to influence settling time. They include amplifier slew rate and AC dynamics, DAC output resistance and capacitance, and the compensation capacitor. These terms interact in a complex manner, making predictions hazardous¹. If the DAC's parasitics are eliminated and replaced with a pure resistive source, amplifier settling time is still not readily predictable. The DAC's output impedance terms just make a difficult problem more messy. The only real handle available to deal with all this is the feedback compensation capacitor, C_F . C_F 's purpose is to roll off amplifier gain at the frequency that permits best dynamic response. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the DAC's parasitic capacitance to ground at the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to "hunt" and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, typically 100pF, and it varies with code.

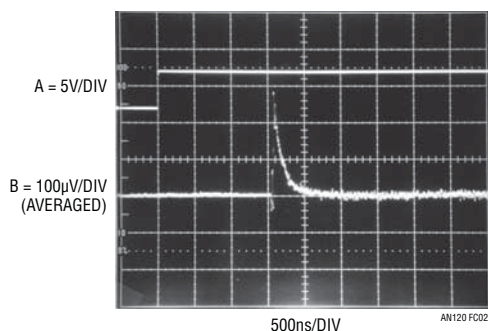


Figure D2. Optimized Compensation Capacitor Permits Nearly Critically Damped Response, Faster Settling Time, $t_{SETTLE} = 1.8\mu s$ to 0.0004% (18 Bits)

Best settling results when the compensation capacitor is selected to functionally compensate for all the above parasitics. Figure D2, taken with an LTC2757/LT1468 DAC-Amplifier combination, shows results for an optimally selected (in this case, 20pF) feedback capacitor. Trace A is the DAC input pulse and trace B the amplifier's settle signal. The amplifier is seen to come cleanly out of slew and settle very quickly.

In Figure D3, the feedback capacitor is too large (27pF). Settling is smooth, although overdamped, and a 300ns penalty results. Figure D4's feedback capacitor is too small (15pF), causing a somewhat underdamped response with resultant excessive ring time excursions. Settling time goes out to 2.8µs. Note that the above compensation values for 18-bit settling are not necessarily indicative of results for 16 or 20 bits. Optimal compensation values must be established for any given desired resolution. Typical values range from 15pF to 39pF.

Note 1. Spice aficionados take notice.

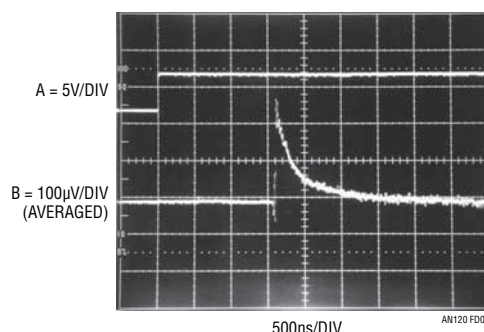


Figure D3. Overdamped Response Ensures Freedom from Ringing, Even with Production Component Variations. Penalty is Increased Settling Time. $t_{SETTLE} = 2.1\mu s$ to 0.0004% (18 Bits)

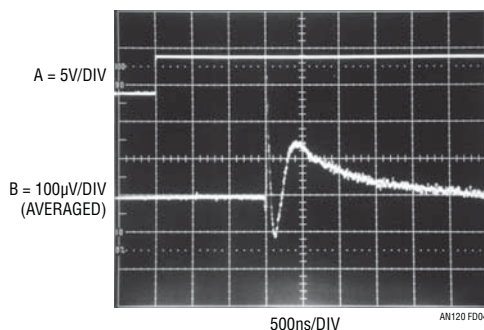


Figure D4. Underdamped Response Results from Undersized Capacitor. Component Tolerance Budgeting Will Prevent This Behavior. $t_{SETTLE} = 2.8\mu s$ to 0.0004% (18 Bits)

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Application Note 120

When feedback capacitors are individually trimmed for optimal response, DAC, amplifier and compensation capacitor tolerances are irrelevant. If individual trimming is not used, these tolerances must be considered to determine the feedback capacitor's production value. Ring time is affected by DAC capacitance and resistance, as well as the feedback capacitor's value. The relationship is nonlinear, although some guidelines are possible. The DAC impedance terms can vary by $\pm 50\%$ and the feedback capacitor is typically a $\pm 5\%$ component. Additionally, amplifier slew rate has a significant tolerance, which is stated on the data sheet. To obtain a production feedback capacitor value,

determine the optimum value by individual trimming with the production board layout (board layout parasitic capacitance counts too!). Then, factor in the worst-case percentage values for DAC impedance terms, slew rate and feedback capacitor tolerance. Combine this information with the trimmed capacitors measured value to obtain the production value. This budgeting is perhaps unduly pessimistic (RMS error summing may be a defensible compromise), but will keep you out of trouble².

Note 2: The potential problems with RMS error summing become clear when sitting in an airliner that is landing in a snowstorm.

APPENDIX E

A VERY SPECIAL CASE—MEASURING SETTLING TIME OF CHOPPER-STABILIZED AMPLIFIERS

The text box section (page 2) lists the LTC1150 chopper-stabilized amplifier. The term “special case” appears in the “comments” column. A special case it is! To see why requires some understanding of how these amplifiers work. Figure E1 is a simplified block diagram of the LTC1150 CMOS chopper-stabilized amplifier. There are actually two amplifiers. The “fast amp” processes input signals directly to the output. This amplifier is relatively quick, but has poor DC offset characteristics. A second, clocked, amplifier is employed to periodically sample the offset of the fast channel and maintain its output “hold” capacitor at whatever value is required to correct the fast amplifier's offset errors. The DC stabilizing amplifier is clocked to permit it to operate (internally) as an AC amplifier, eliminating its DC terms as an error source¹. The clock

chops the stabilizing amplifier at about 500Hz, providing updates to the hold capacitor-offset control every 2ms².

The settling time of this composite amplifier is a function of the fast and stabilizing paths response. Figure E2 shows amplifier short-term settling. Trace A is the DAC input pulse and trace B the settle signal. Damping is reasonable and the 10 μ s settling time and profile appear typical. Figure E3 brings an unpleasant surprise. If the DAC slewing interval happens to coincide with the amplifier's sampling cycle, serious error is induced. In Figure E3, trace A is the amplifier output and trace B the settle signal. Note the slow horizontal scale. The amplifier initially settles quickly (settling is visible in the 2nd

Note 1. This AC processing of DC information is the basis of all chopper and chopper-stabilized amplifiers. In this case, if we could build an inherently stable CMOS amplifier for the stabilizing stage, no chopper stabilization would be necessary.

Note 2. Those finding this description intolerably brief are commended to reference 31.

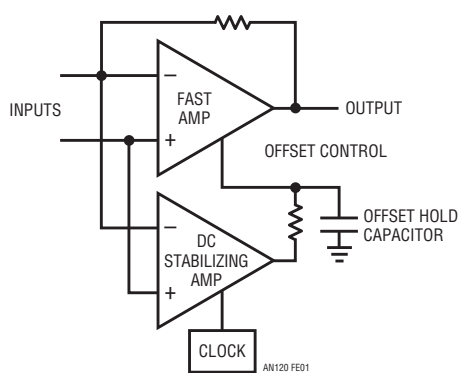


Figure E1. Highly Simplified Block Diagram of Monolithic Chopper-Stabilized Amplifier. Clocked Stabilizing Amplifier and Hold Capacitor Cause Settling Time Lag

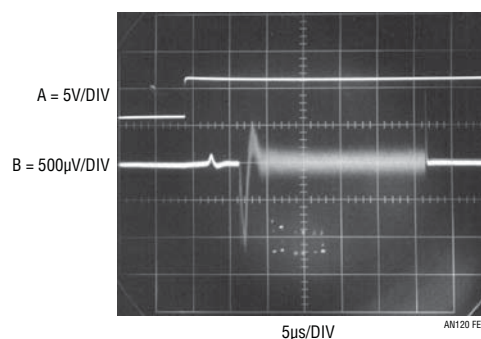


Figure E2. Short-Term Settling Profile of Chopper-Stabilized Amplifier Seems Typical. Settling Appears to Occur in 10 μ s

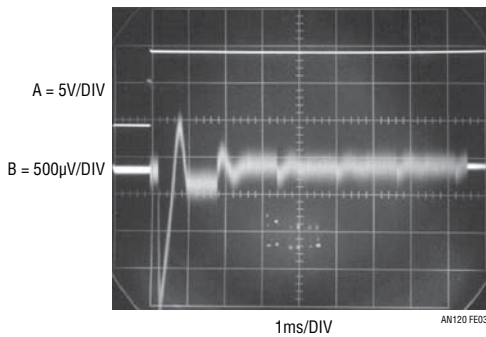


Figure E3. Surprise! Actual Settling Requires 700× More Time Than Figure E2 Indicates. Slow Sweep Reveals Monstrous Tailing Error (Note Horizontal Scale Change) Due to Amplifier’s Clocked Operation. Stabilizing Loop’s Iterative Corrections Progressively Reduce Error Before Finally Disappearing Into Noise

vertical division region) but generates a huge error 200µs later when its internal clock applies an offset correction. Successive clock cycles progressively chop the error into the noise but 7 *milliseconds* are required for complete recovery. The error occurs because the amplifier sampled offset when its input was driven well outside its bandpass. This caused the stabilizing amplifier to acquire erroneous offset information. When this “correction” was applied, the result was a huge output error.

This is admittedly a worst case. It can only happen if the DAC slewing interval coincides with the amplifier’s internal clock cycle, but it can happen^{3,4}.

Note 3. Readers are invited to speculate on the instrumentation requirements for obtaining Figure E3’s photo.

Note 4. The spirit of Appendix D’s footnote 2 is similarly applicable in this instance.

APPENDIX F

SETTLING TIME MEASUREMENT OF SERIALLY LOADED DACS

Measuring serially loaded DACs settling time requires additional circuitry. This circuitry must provide a “start” pulse to the settling time measurement circuit after serially

loading a full-scale step into the DAC. Figure F1’s processor based circuitry, designed and constructed by LTC’s Mark Thoren, does this. The “start” pulse (trace A, Figure F2) initiates the measurement. Traces B, C and D are \overline{CS}/LD , SCK, and SDI, respectively. Trace E, the resultant DAC output, is measured for settling time in (what should be by now) familiar fashion. Figure F3 is a complete processor software code listing.

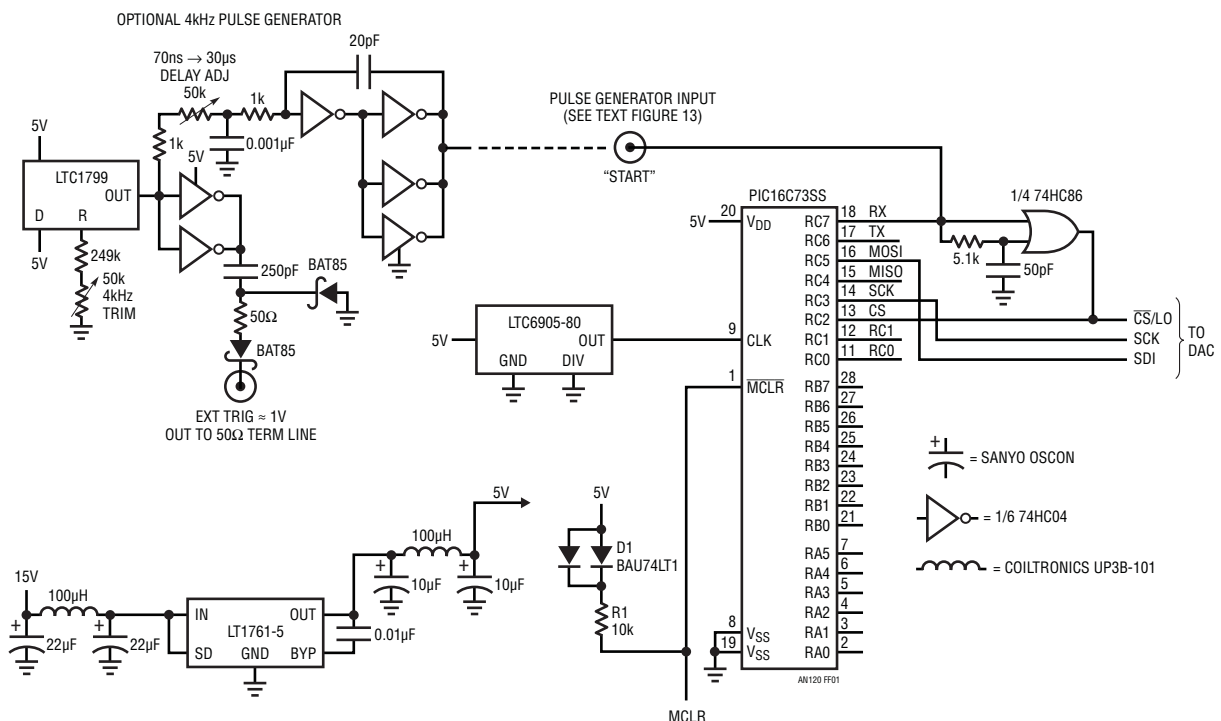


Figure F1. The Serial Interface. Processor Responds to Input Pulse, Directs DAC to Perform 10V Steps

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Application Note 120

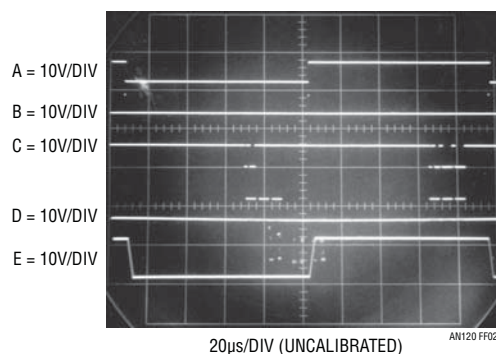


Figure F2. Serial Interface Operation Includes Input Start Pulse (Trace A), $\overline{CS/LD}$ (Trace B), SCK (C), SDI (D) and Resultant DAC Output (E), Digital Data Lines are Static During Measurement Interval, Precluding Crosstalk Induced Corruption

```
/*  
Serial DAC step program. Makes controlling the serial DAC as easy as the old way of  
tying all the digital lines of a parallel DAC to a pulse generator.
```

```
the serial DAC CS/LD signal is the output of an XOR gate edge detector that gives  
a 1µs pulse on either the rising edge or falling edge of CONTROL signal.  
Program enters main loop when CONTROL is high. When CONTROL goes low, the code  
for +5V is sent. When CONTROL goes high, the code for -5V is sent. Thus the  
timing of the load pulse accurately follows the input signal by about 20ns.
```

```
A delay of 60µs is inserted after the load pulse so that you can look at  
settling details without having to worry about digital feedthrough.
```

```
*/
```

```
#include <16F73.h>  
#include "pcm73a.h"  
#use delay(clock=20000000) // 20 meg clock  
#fuses HS, NOWDT, PUT//, MCLR
```

```
// Defines for DAC addresses  
#define DACA 0  
#define DACB 2  
#define DACC 4  
#define DACD 6
```

```
#define PM10 0x03  
#define PM5 0x02
```

```
// Control input  
#define CONTROL PIN_C7
```

```
void init(void);
```

```
void main()
```

```
{  
    init(); // set up hardware
```

```
    // This just allows the program to sync up to a pulse generator that  
    // may not have a clean output on power-up. You need to see at least one rising  
    // and one falling edge before continuing.  
    while(!input(CONTROL)){} delay_us(2); // wait for rising edge  
    while(input(CONTROL)){} delay_us(2); // wait for falling edge  
    delay_ms(100);  
    while(!input(CONTROL)){} delay_us(2); // wait for rising edge  
    while(input(CONTROL)){} delay_us(2); // wait for falling edge
```

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```

// Okay, now we're all synchronized.
// Since program does not have direct access to the CS/LD line, you
// have to rely on the externally applied pulse.
while(!input(CONTROL)){ delay_us(2); // wait for rising edge
while(input(CONTROL)){ delay_us(2); // wait for falling edge
spi_write(0x6F); // Set all DACs to +/-10V range
spi_write(0x00);
spi_write(PM5);

while(!input(CONTROL)){ delay_us(2); // wait for rising edge
spi_write(0x70 | DACB); // Set DACB to -10 volts
spi_write(0x00);
spi_write(0x00);

while(input(CONTROL)){ delay_us(2); // wait for falling edge
spi_write(0x70 | DACC); // Set DACC to 0 volts
spi_write(0x80);
spi_write(0x00);

while(!input(CONTROL)){ delay_us(2); // wait for rising edge
spi_write(0x70 | DACD); // Set DACD to +10 volts
spi_write(0xFF);
spi_write(0xFF);

while(1)
{
while(input(CONTROL)){ delay_us(80); // wait for falling edge
spi_write(0x70 | DACA); // Set DACA to 0 volts
spi_write(0xFF);
spi_write(0xFF);

while(!input(CONTROL)){ delay_us(80); // wait for rising edge
spi_write(0x70 | DACA); // Set DACA to +10 volts
spi_write(0x00);
spi_write(0x00);
}
}

void init()
{
setup_adc_ports(NO_ANALOGS);
setup_adc(ADC_CLOCK_DIV_2);
setup_spi(SPI_MASTER|SPI_L_TO_H|SPI_CLK_DIV_4|SPI_SS_DISABLED);
CKP = 0; // Set up clock edges - clock idles low, data changes on
CKE = 1; // falling edges, valid on rising edges.
setup_counters(RTCC_INTERNAL,RTCC_DIV_2);
setup_timer_1(T1_DISABLED);
setup_timer_2(T2_DISABLED,0,1);
setup_ccp1(CCP_OFF);
setup_ccp2(CCP_OFF);
set_tris_a(0b00000000);
set_tris_b(0b00000000);
set_tris_c(0b10000100); // Make sure control signal is input
}

```

Figure F3. Software Listing for PIC16C73SS Processor. Code Directs DAC to Step 10V at Each Input Pulse Transition

APPENDIX G

BREADBOARDING, LAYOUT AND CONNECTION TECHNIQUES

The measurement results presented in this publication required painstaking care in breadboarding, layout and connection techniques. Wideband, 10 μ V resolution measurement does not tolerate cavalier laboratory attitude. The oscilloscope photographs presented, devoid of ringing, hops, spikes and similar aberrations, are the result of an exhaustive (and frustrating) breadboarding exercise¹. The breadboard was rebuilt numerous times and required weeks of layout and shielding experimentation before obtaining a noise/uncertainty floor worthy of 20-bit measurement. In particular, extreme measures were required to minimize sample command signal feedthrough. Layout techniques include minimization and restriction of radiative paths, ground plane current management and mounting the LT1228 “switch” upside down, allowing its V-referred substrate to approximate a monolithic shield for the IC’s internal circuitry.

Ohm’s Law

It is worth considering Ohm’s Law is a key to successful layout². Consider that 1mA running through 0.1 Ω generates 100 μ V—almost 3LSB at 18 bits! Now, run that milliampere at 5ns to 10ns rise times (approximately 75MHz) and the need for layout care becomes clear. A paramount concern is disposal of circuit ground return current and disposition of current in the ground plane. The impedance of the ground plane between any two points is not zero, particularly as frequency scales up. This is why the entry point and flow of “dirty” ground returns must be carefully placed within the grounding system. In the sampler-based breadboard, the approach was separate “dirty” and “signal” ground planes, tied together at the supply ground origin.

A good example of the importance of grounding management involves delivering the input pulse to the breadboard. The pulse generator’s 50 Ω termination must be an in-line coaxial type, and it cannot be directly tied to the signal ground plane. The high speed, high density (5V pulses through the 50 Ω termination generate 100mA current spikes) current flow must return directly to the pulse

generator. The coaxial terminator’s construction ensures this substantial current does this, instead of being dumped into the signal ground plane (100mA termination current flowing through 1m Ω of ground plane produces approximately 3LSB of error!). The 50 Ω termination is physically distanced from the breadboard via a coaxial extension tube (visible in Figure H7)³. This further ensures that pulse generator return current circulates in a tight local loop at the terminator and does not mix into the signal plane.

It is worth mentioning that every ground return in the entire circuit must be evaluated with these concerns in mind. A paranoiac mindset is quite useful.

Shielding

The most obvious way to handle radiation-induced errors is shielding. Various following figures show shielding. Determining where shields are required should come *after* considering what layout will minimize their necessity. Often, grounding requirements conflict with minimizing radiation effects, precluding maintaining distance⁴ between sensitive points. Shielding⁵ is usually an effective compromise in such situations.

A similar approach to ground path integrity should be pursued with radiation management. Consider what points are likely to radiate, and try to lay them out at a distance from sensitive nodes. When in doubt about odd effects, experiment with shield placement and note results, iterating towards favorable performance⁶. *Above all, never rely on filtering or measurement bandwidth limiting to “get rid of” undesired signals whose origin is not fully understood.* This is not only intellectually dishonest, but may produce wholly invalid measurement “results”, even if they look pretty on the oscilloscope.

Note 1. “War” is perhaps a more accurate descriptive.

Note 2. I do not wax pedantic here. My abuse of this postulate runs deep.

Note 3. Strictly considered, this technique introduces mis-termination originated transmission line reflections but no appreciable error results at the bandwidth of interest.

Note 4. Distance is the physicist’s approach to reducing radiation induced effects.

Note 5. Shielding is the engineer’s approach to reducing radiation induced effects.

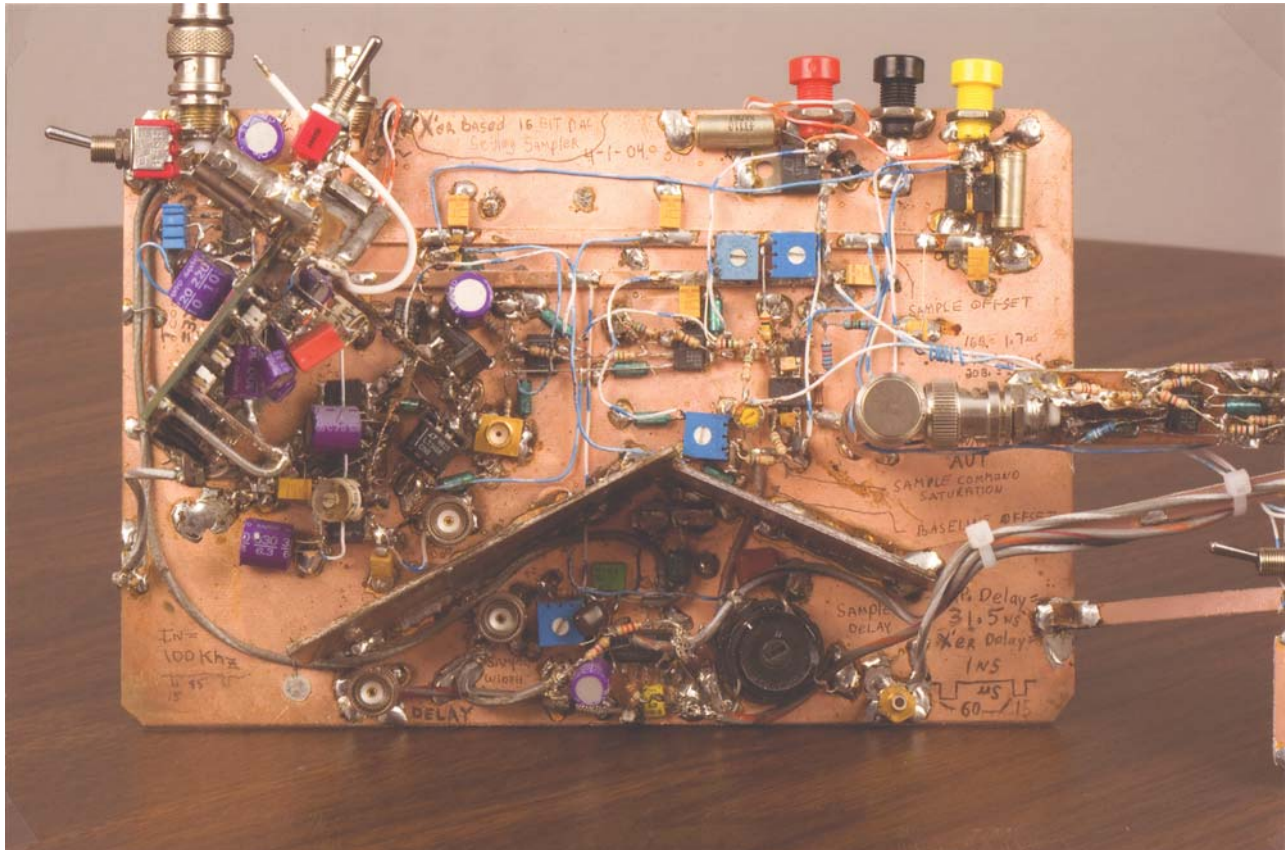
Note 6. After it works, you can figure out why.

Connections

All signal connections to the breadboard must be coaxial. Ground wires used with oscilloscope probes are forbidden. A one inch ground lead used with a 'scope probe can easily generate several LSBs of observed "noise". Use

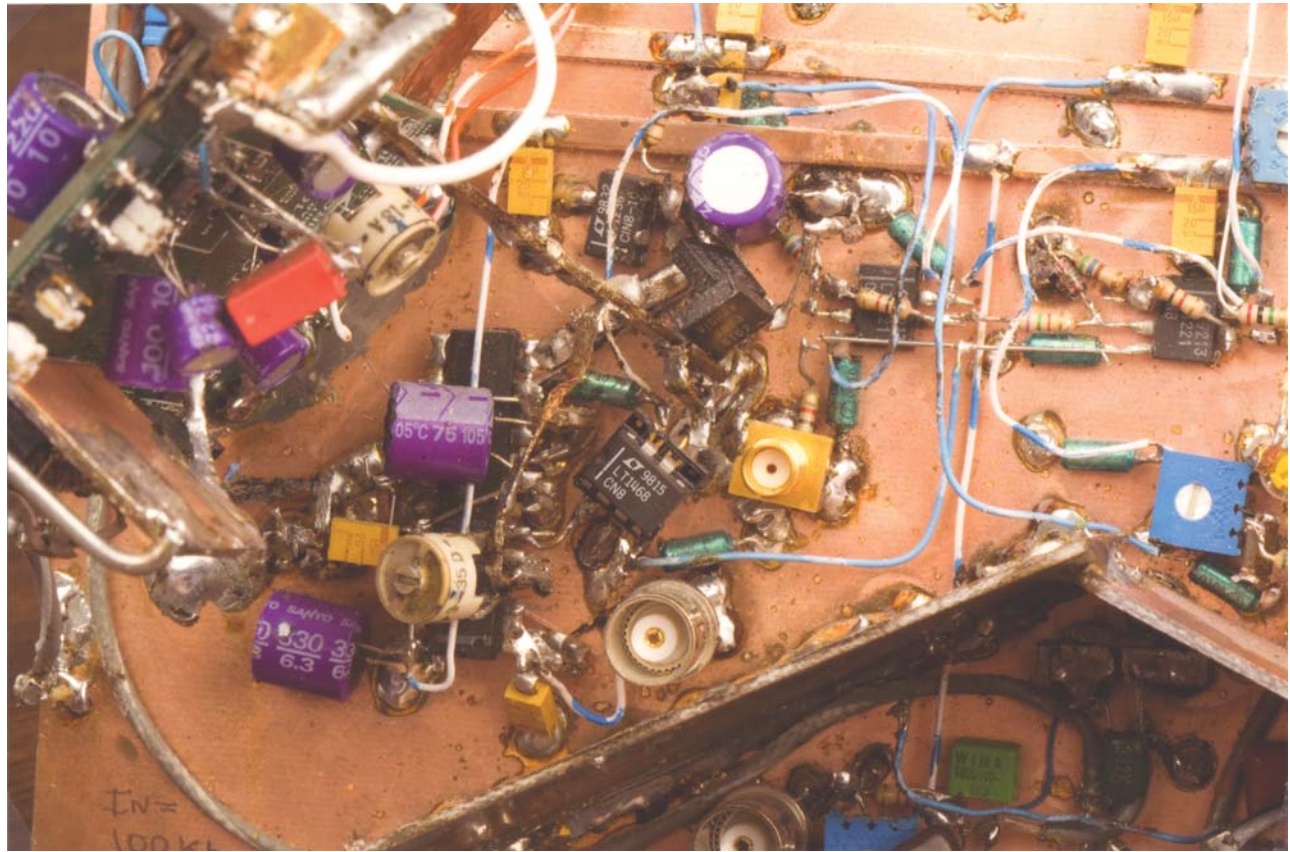
coaxially mounting probe tip adapters⁷. Figures G1 to G5 restate the above sermon in visual form while annotating the text's circuits.

Note 7. See reference 28 for additional nagging along these lines.



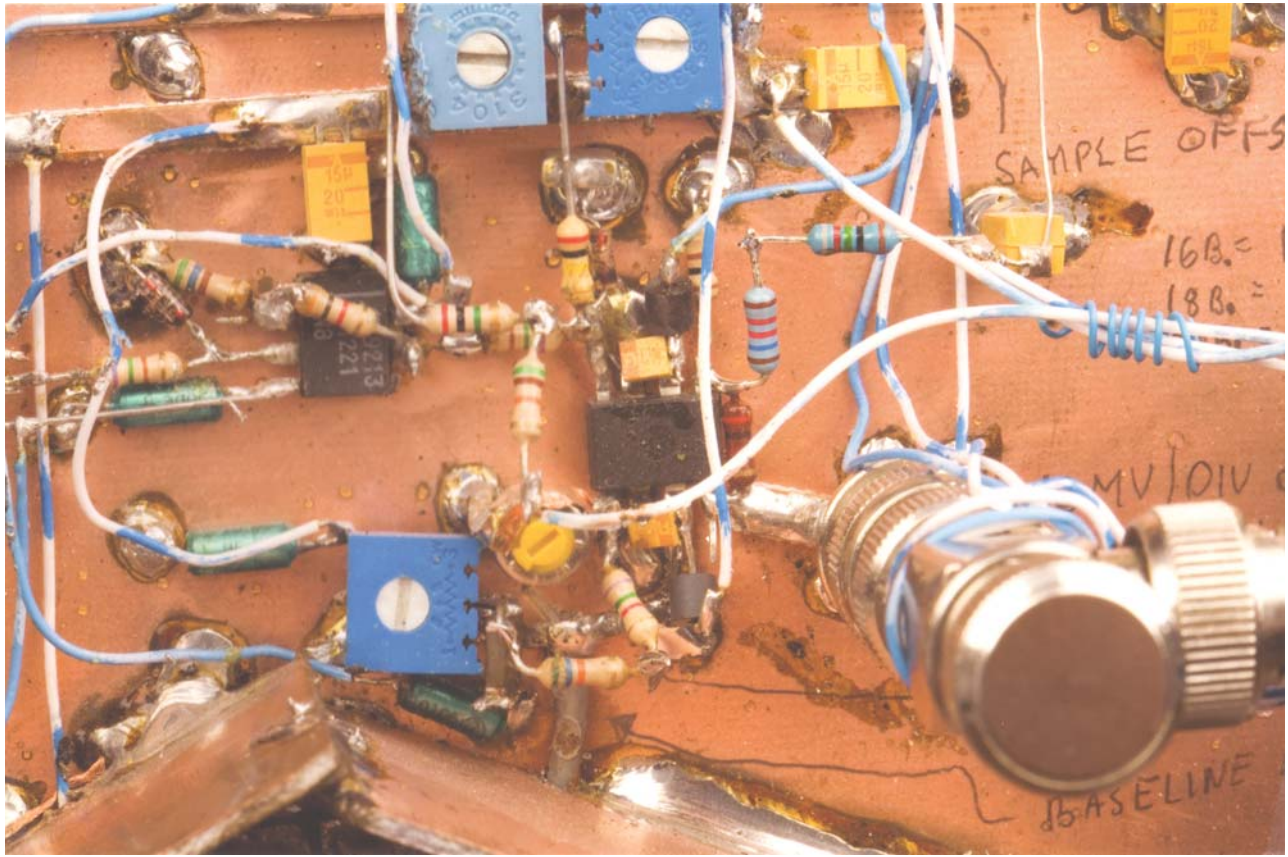
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Figure G1. Settling Time Breadboard Overview. Pulse Generator Input Enters Top Left— 50Ω Coaxial Terminator Mounted On Extension Tube (Not Visible—See Appendix H, Figure H7) Minimizes Pulse Generator Return Current Mixing Into Signal Ground Plane. DAC-amplifier and Support Circuitry are at Left. Sampler Circuitry Occupies Board Right. Sampler Digital Support Circuitry is Contained Within Large Shield (Board Lower). Nonsaturating Amplifier Occupies Board Center. Partially Visible X10 Post Amplifier (See Appendix I) is BNC Fixtured, Thin Board at Photo Right. Auto-Zero Circuit (see Appendix I), Mounted on Thin Strut (Lower Right), is Not Visible



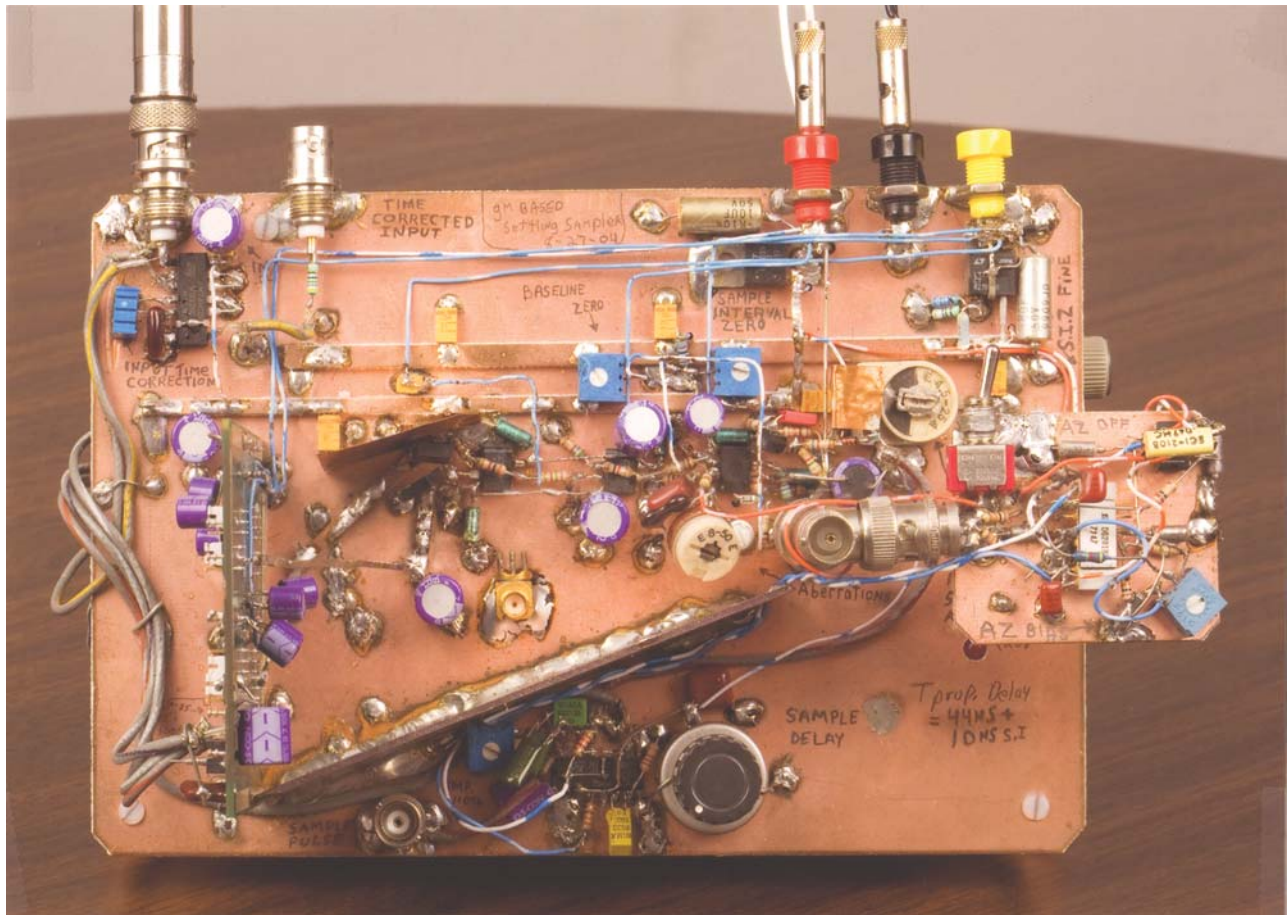
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Figure G2. DAC-Amplifier Detail. DAC and Output Amplifier are at Photo Center Left. Precision Summing Resistors (Box-Shaped, Just Below Large Round Capacitor Near Photo Center) are Oriented to Restrict Radiative Coupling While Minimizing Summing Node Capacitance. Variable Capacitor (Lower Left Center) Sets Amplifier (Photo Center) Compensation. Non-Saturating Amplifier Appears at Right. Shield (Bottom) Restricts Sampler Digital Section's Radiation. Vertically Mounted Board (Extreme Upper Left) is Optional Serial DAC Interface (See Appendix F). Coaxial Connectors (Center Lower) Facilitate High Purity Signal Extraction



AN120 FG03

Figure G3. LT1228 Sampling “Switch” (Photo Center) Is Mounted Upside Down, Permitting V^- Referred Die Backside To Shield Residual Radiative Coupling, Reducing Sampling Switch Drive Feedthrough. Switch Signal Channel Is Fed From Non-Saturating Amplifier (Photo Left). Sample Command From Shielded Digital Section (Lower) Arrives Via Coaxial Cable Tunneling Through Shield (Lower Center)



AN120 F004

Figure G4. A Dedicated, Serially Interfaced Settling Time Breadboard. Serial Interface Digital Board is Obscured Beneath Visible Analog Board (See Appendix H, Figure H7). Note Insulating Nylon Screws (Right and Left Lower Corners and Upper Edge Between BNC Connectors) Used to Attach Digital and Analog Boards. Digital Board Ground is Single-Point Connected at Analog Board Ground Entry Point (Middle Banana Jack). Serial Signals Access Vertical DAC Board Via Coax (Photo Left). Shields Isolate Sample Switch Digital Section (Lower) and Summing Node (Left Center). Non-Saturating Amplifier and Sampling Switch are as in Figure G1. Optional Auto-Zero Board (See Appendix I) Mounts from BNC Fitting at Center Right. Upper Left Corner Components are Input Pulse Time Correction

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AN120 FG05

Figure G5. Serially Interfaced Settling Time Breadboard Signal Path Detail. DAC Board is at Left. Precision Resistors Feed Summing Node and Non-Saturating Amplifier (Photo Upper Center). Shield Protects Summing Node from Input Pulse Originated Radiation. LT1228 Sampling “Switch” (Far Right) is Mounted Upside Down, Permitting V^- Referred Die Backside to Shield Radiative Coupling, Reducing Switch Drive Feedthrough. Switch Drive Level Shift-Current Source (Extreme Right Upper) Receives Sample Command Via Coax, Partially Visible at Lower Right. Large Vertical Shield Confines Sample Command Digital Section Radiation (Lower). SMA Connector (Center) Enables Test and Calibration Signal Connection

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APPENDIX H

HOW DO YOU KNOW IT WORKS? Settling Time Circuit Performance Verification

High Purity Pulse Generator

Any prudent investigation requires performance verification of the test method. Strictly considered, it may not be possible to furnish indisputable proof that the circuit in question is functioning at its design limits, particularly in a state-of-the-art measurement. However, a reasonable level of confidence is a realistic goal. Performance verification for the settling time test circuit requires a high purity pulse generator that transitions and settles to 1ppm as quickly as possible. This is a high order difficulty requirement and the author is unaware of any electronic means of achieving this capability. Fortunately, electro-mechanical technology offers a solution.

Figure H1 shows a conceptual mercury wetted reed relay pulse generator. Theoretically, when the contacts open, an infinitely fast falling edge appears across the 50Ω termination with zero settling time to 0V. Figure H2 reveals this to be not the case. This photograph, taken with a typical commercially available relay, shows <math><5\text{ns}</math> transition time with a 500MHz ring off over ¹. These imperfections are not surprising when Figure H3's parasitic terms are considered. Figure H1's deceptively simple schematic is revealed to have a number of unintentional terms which severely limit performance. These terms include, but are not limited to, parasitic resistance, inductance, and capacitance as well as undesirable field interaction within the relay. Additionally, the connection through the relay to the output terminal constitutes an ill-defined transmission line which promotes additional vagaries. The parasitic terms

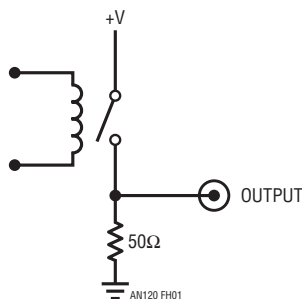


Figure H1. Conceptual Mercury Wetted Reed Relay Pulse Generator Produces Infinitely Fast Falling Edge Across 50Ω Termination with Zero Settling Time to 0V

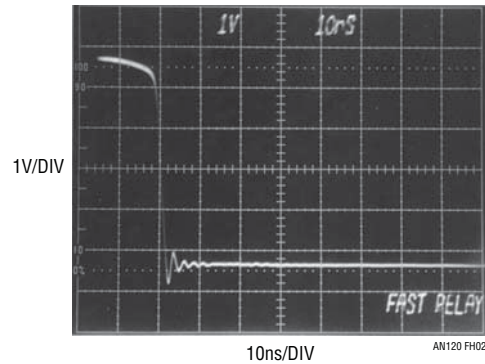


Figure H2. Mercury Wetted Reed Relay Opens in <math><5\text{ns}</math>, Settles Quickly to Zero. 500MHz Ring Off Derives from Source-Termination Impedance Mismatch

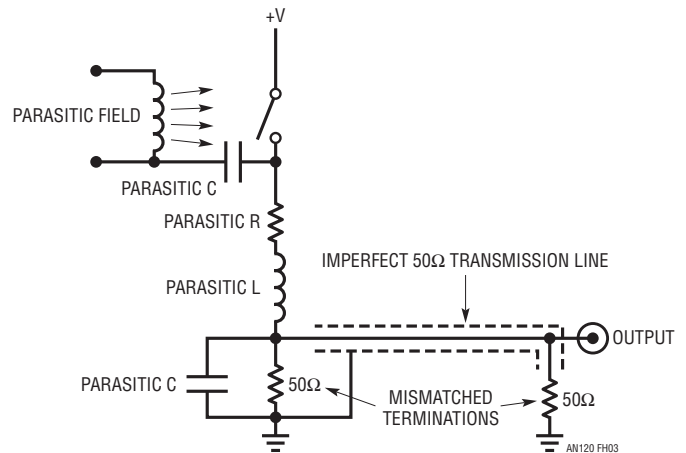


Figure H3. Parasitic Terms Limit Achievable Performance. Transmission Line, Required to Route Output Pulse, Adds Termination Mismatch Errors and Line Related Infidelities

interact in a haphazard and unpredictable way, resulting in alien terms at the pulse output. What is really needed is a relay specifically designed and constructed for inclusion into a wideband 50Ω system.

A True 50Ω, Wideband Mercury Wetted Reed Relay

In the 1960s, Tektronix manufactured the type 109 mercury wetted reed relay, intended for use as a pulse generator. In its preferred configuration, energized charge lines are

Note 1. Tangential to this discussion, but nonetheless interesting, is the corner rounding at the pulse top just before its rapid fall. This may be due to "teasing" of the mercury, causing its resistance to increase just before it fully opens. John Willison of Stanford Research Systems suggests the mechanism may be charge displacement in the capacitor formed as the relay contacts just open. Scott Hamilton, Manchester University (UK), has raised the possibility of quantum tunneling across the brief, small contact gap *a la* scanning tunneling microscope operation. Comments from the readership are welcome.

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switched by the relay into a 50Ω termination, resulting in a 250ps risetime pulse. Here, charge lines are not employed; rather, the device is used as a simple switch. Advantage is taken of the exquisite care at manufacture to make the relay transparent in a 50Ω system. Figure H4's large scale transition reveals 800ps fall time in a 1GHz bandwidth. Actual fall time is probably somewhat faster as the monitoring oscilloscope has a 350ps risetime². The transition is singularly clean and devoid of discontinuities with the exception of the previously noted pre-fall corner rounding. Figure H5's remarkable photograph uses sampling switch techniques similar to those described in the

text to measure type 109 fall-time purity to microvolts³. The 109 output (trace B) moves the final $220\mu\text{V}$, settling inside $10\mu\text{V}$ approximately 265ns after the relay contacts open (trace A). Actual 109 settling time may be faster as the measurement is likely sampling circuit limited⁴. Figure H6 is a simplified version of the test circuit which

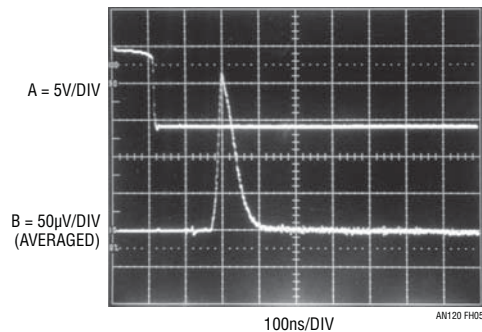
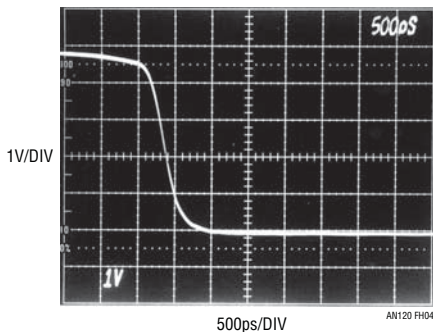


Figure H4. High Grade Mercury Wetted Reed Relay (Tektronix Type 109) Falls in 800ps Viewed in 1GHz Real Time Bandwidth. Strict Attention To Parasitic Minimization in Relay Structure and Transmission Path Produces High Fidelity Transition Without Alien Components

Figure H5. Sampling Switch Techniques Permit Measuring Type 109 Falling Edge Residue to Microvolts in 20MHz Bandpass. Trace A is 109 Falling Edge, Trace B the Last $220\mu\text{V}$ of Movement Before Settling to 1ppm in Indicated 265ns

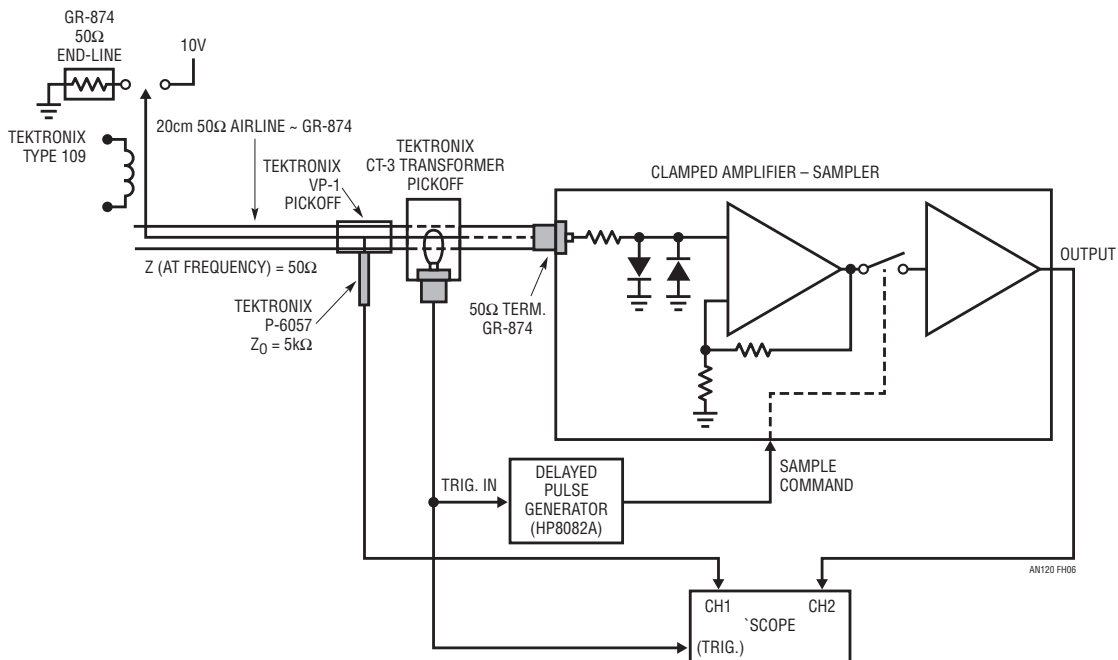


Figure H6. Simplified Test Circuit. Attention to Hg Wetted Reed Relay and Transmission Line Allow 1ppm Residue $\approx 265\text{ns}$ After Contacts Open

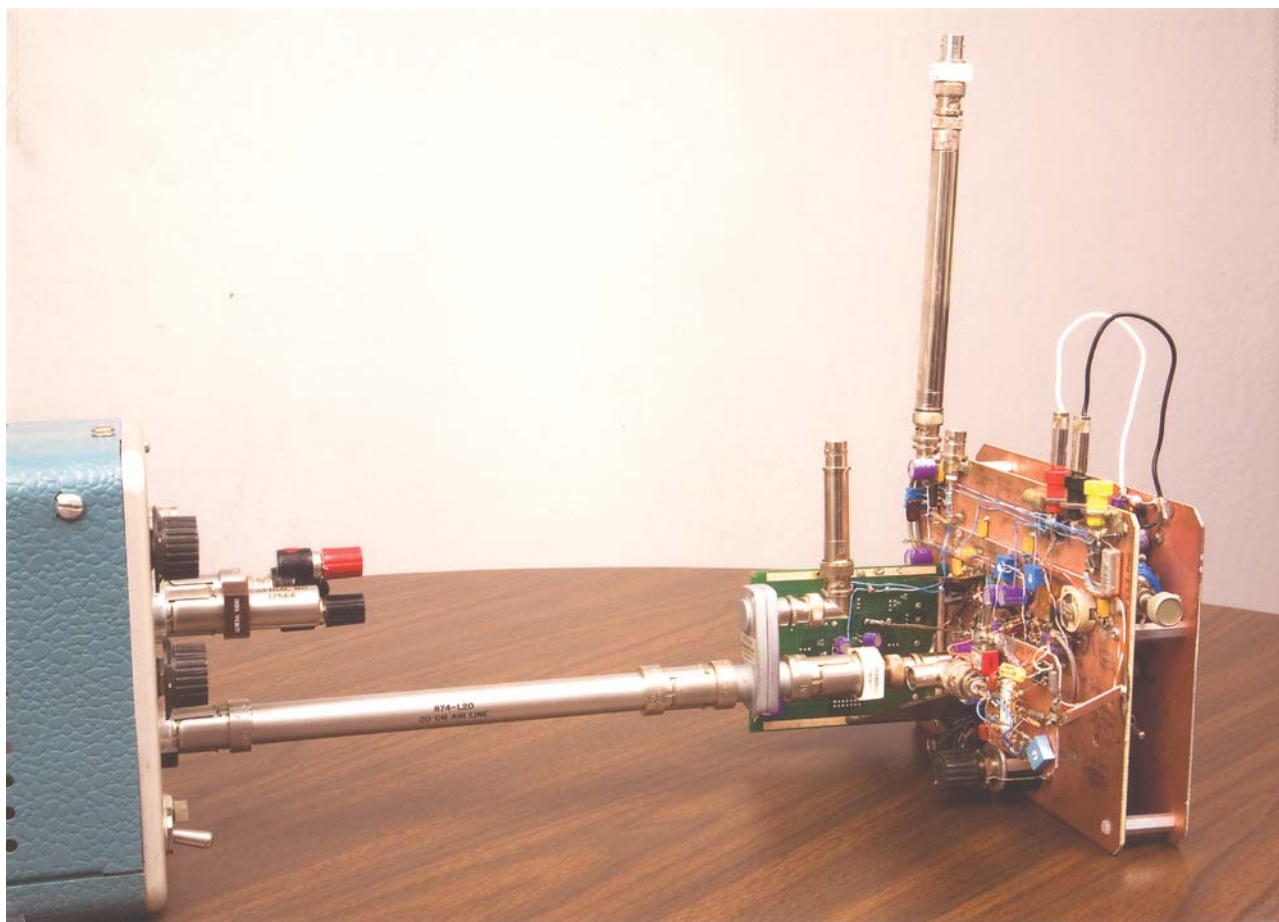
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Application Note 120

produced these results. The type 109 drives 20 centimeters of 50Ω GR-874 airline into a high quality GR-874 50Ω termination at the clamped amplifier-sampling switch. The delayed pulse generator and oscilloscope are set up similarly to the main text description. The Tektronix pickoff components noted allow signal extraction from the airline without degrading transmission line integrity. It is interesting to note that airline is a non-negotiable requirement. The highest quality Teflon 50Ω cable produced impure response, albeit minor.

Figure H7's photograph shows the high purity step generator connected to Figure G4's settling time breadboard. The

type 109 (photo left) delivers its pulse via a General Radio 20 centimeter airline. The Tektronix CT-3 coaxial transformer (right end of airline) supplies the trigger pick-off via the vertically mounted 50Ω BNC connector. A GR-874 50Ω load (right side of CT-3) terminates the airline and supplies the pulse to the breadboard. Pulse amplitude is set by a DC voltage applied at the 109 via banana inputs. The unused 109 contact is terminated with an endline GR-874 fitting. All connections must be polished and mechanically secured to ensure a high fidelity 50Ω environment. Any component substitution or mechanical connection imperfection will degrade Figure H5's results.



AN120 FH07

Figure H7. High Purity Step Generator Connected to Figure G4's Settling Time Breadboard. Tektronix Type 109 Mercury Wetted Relay Based Pulse Generator (Photo Left) Delivers Pulse Via General Radio 20 Centimeter Airline. Tektronix CT-3 Coaxial Transformer (Right End of Air Line) Supplies Trigger Pick-Off Via 50Ω BNC Vertical Connector. GR-874 Coaxial 50Ω Load (Right Side of CT-3) Terminates Line And Supplies Pulse to Breadboard. Pulse Amplitude is Set by DC Voltage Applied to Tektronix 109 Via Banana Input Adapter. Unused Type 109 Contact is Terminated with End-Line GR-874 Fitting. All Connections Must Be Polished and Mechanically Secure to Ensure High Fidelity 50Ω Environment. Long Coaxial Extension Tube On Breadboard Isolates Input Pulse Termination (Tube Top) Current from Board Ground Plane (see Text and Figure G1 For Commentary). Lower Board Contains Digital Serial Interface (See Appendix F and Figure G4)

an120f

“Pretty Good” Mercury Wetted Reed Relay Pulse Generator

It may be unrealistic for readers to duplicate the Tektronix 109 based results. The specified exotic apparatus is difficult and expensive to obtain and the set up requires arduous labor and almost fanatical attention to detail. In this spirit, Figure H8’s “pretty good” mercury wetted reed relay pulse generator is offered. Its performance, while falling well short of Figure H6, still furnishes a 10V step which settles to 1ppm in 950ns⁵. A simple clock (“resonance set”) furnishes low frequency drive to the relay via the transistor level shift and the LT1010 power buffer. Trigger pick-off is provided by the paralleled CMOS inverters. Separate packages for the “resonance set” and trigger functions must be used to avoid output pulse contamination. Figure H9 shows results for the “pretty good” step generator. Its slower settling and alien residue components compared to the Tektronix 109 approach are apparent. The event at the 10th vertical division is sample gate turn-off feedthrough related.

Circuit calibration involves adjusting “resonance set” until the relay emits a reasonably pure audible tone. Next, set the 20V supply to a value which promotes the cleanest settling characteristics.

Note 5. Footnote 4’s 70ns timing allowance applies here. Figure H8 likely settles in ≈ 880 ns.

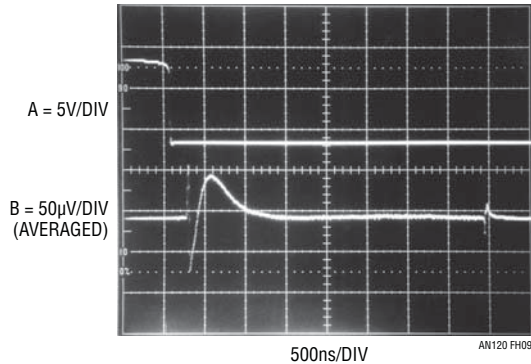


Figure H9. “Pretty Good” Step Generator Output (Trace A) Settles (Trace B) to 1ppm (10µV) in 950ns. Ill-Defined Relay Impedance Results in Approximately 3.6× Slower Settling and Alien Residue Components Compared to Figure H5’s Tektronix 109 Based Results. Event at 10th Vertical Division is Sample Gate Turn-Off Feedthrough

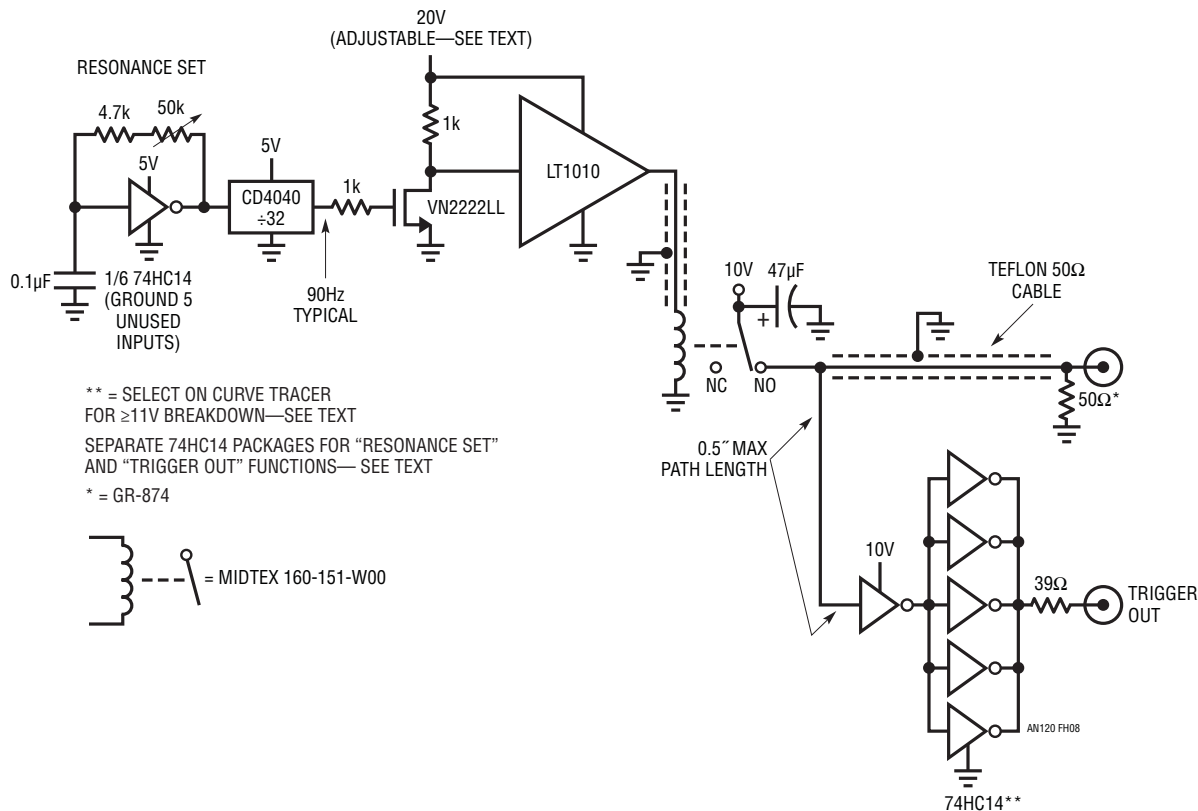


Figure H8. “Pretty Good” Substitute for Figure H6’s Tektronix 109, Constructed from Commercially Available Components, Settles 10V Step to 1ppm in 950ns

an120f

Application Note 120

APPENDIX I

Auxiliary Circuits

Several auxiliary circuits have been found useful in the DAC settling time work described in the text. Figure I1 is a simple, wideband, X10 preamplifier for oscilloscopes lacking the required sensitivity for 1ppm (10 μ V) settling time resolution. This preamplifier should be placed directly (no cable) at the oscilloscope input and connected via 50 Ω terminated BNC cable to the settling time fixture output.

Figure I2, an auto-zero circuit, locks the sample interval zero value to the non-sampled region baseline. It eliminates the need for periodic readjustment of the "Sample Interval Zero" trim when working at the highest levels of resolution over a protracted time. Synchronously switched A1 compares sample interval and non-sampled region zero values and applies an appropriate offset, closing a correction loop around the LT1228. M1's extended pulse precludes settling activity from influencing the sample interval zero value. The "Auto-Zero Bias" trim corrects

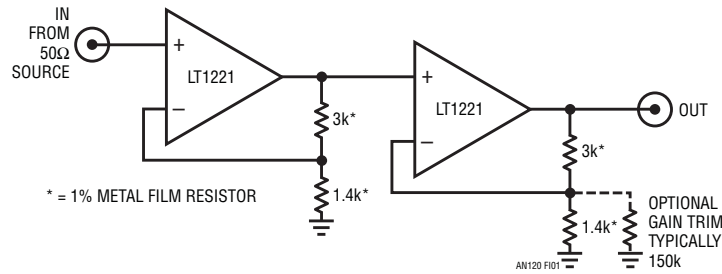


Figure I1. Simple X10 Pre-Amplifier for Oscilloscopes Lacking Required Sensitivity for 1ppm (10 μ V) Settling Time Resolution

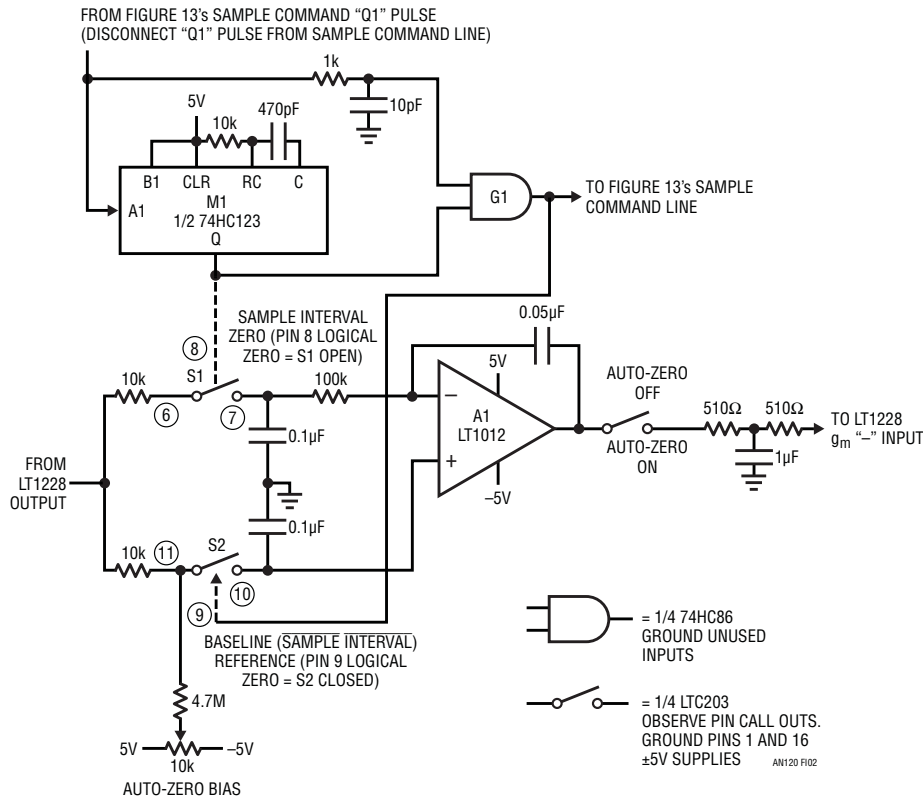


Figure I2. Auto-Zero Locks Sample Interval Zero Value to Non-Sampled Region Baseline. Synchronously Switched A1 Compares Sample Interval and Non-Sampled Region Values and Applies Appropriate Offset, Closing Correction Loop Around LT1228. M1 Precludes Settling Activity from Influencing Sample Interval Zero Value

for slight errors and should not require readjustment once set to equalize the sample interval zero value and the non-sample region baseline. The commented schematic provides information for the auto-zero's interconnection to the settling time circuit. Figure 13 shows auto-zero related waveforms. They include the time corrected input pulse (trace A), DAC output (B), sample delay (C), M1 input (D), M1's sample interval zero pulse (E), G1's sample command (F), and settle signal output (G). M1's delayed output maintains the sample interval zero value independent of the settling signature.

Figure 14 is a simple time calibrator used to verify oscilloscope time base accuracy. Q1 and Q2 form a 1MHz quartz oscillator. The 74C90 provides switch selectable output periods of 2µs and 5µs and the attenuator supplies a 50Ω output impedance. The period values have been selected for calibration points appropriate for expected DAC settling times. Other periods are available by varying oscillator frequency, division ratio or both. 9V battery drain is about 10mA.

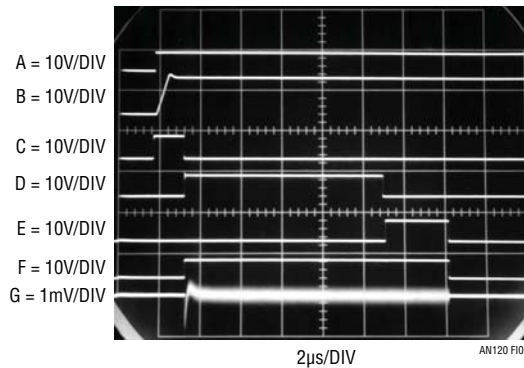


Figure 13. Auto-Zero Related Waveforms Include Time Corrected Input Pulse (Trace A), DAC Output (B), Sample Delay (C), M1's Input (D), M1's Sample Interval Zero Pulse (E), G1's Sample Command (F) and Settle Signal Output (G). M1's Delayed Output Maintains Sample Interval Zero Value Independent of Settling Signature

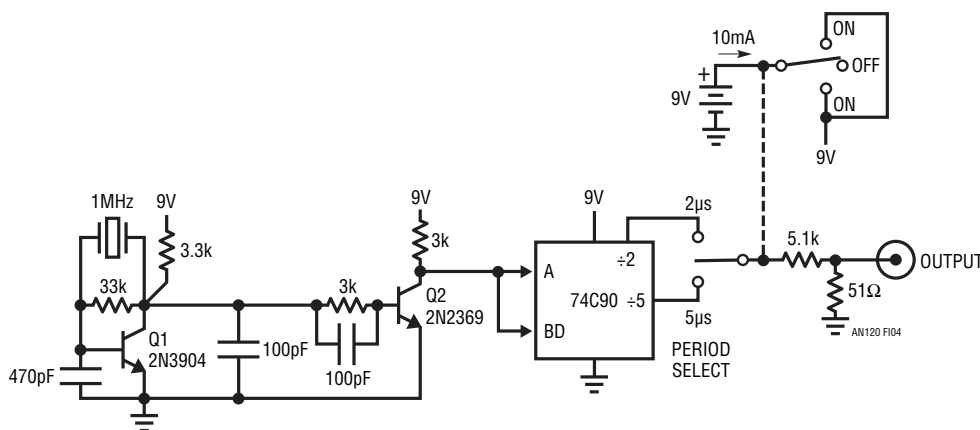
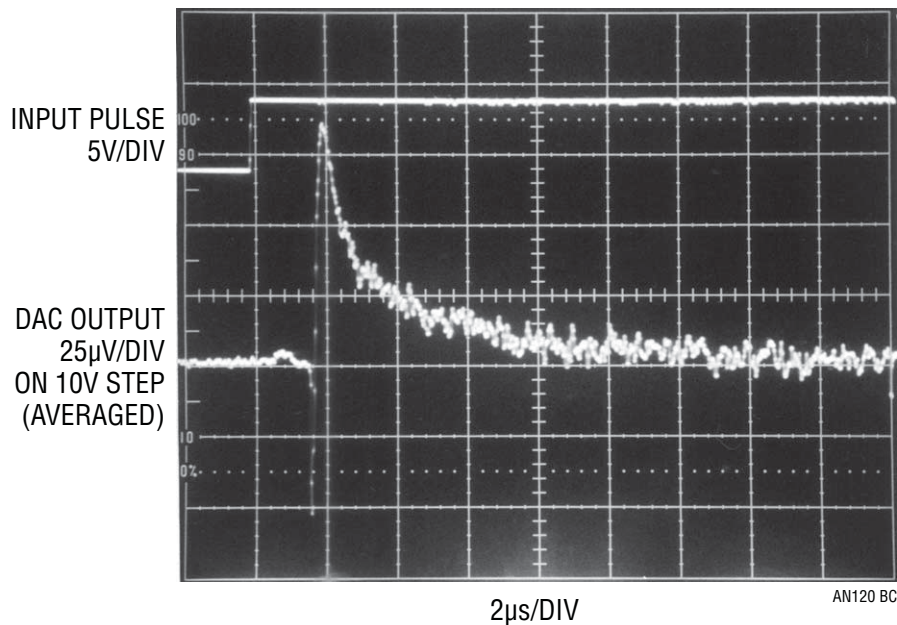


Figure 14. Battery-Powered Oscilloscope Time Base Verifier Has 2µs and 5µs Period Outputs. Quartz Oscillator Q1 Is Buffered by Q2; Digital Divider Supplies Outputs Via Attenuator

Application Note 120



“A part-per-million is a part-per-million. It’s magic. It’s the brass ring. It’s the holy grail of every measurement artist. It will mesmerize you, it will goad you, it will drive you crazy and, if you’re lucky, it will reward you. A part-per-million is a part-per-million.”

Jerrold R. Zacharias

M.I.T. physicist, mentoring a young,
very naïve investigator.

— 1971

Diode Turn-On Time Induced Failures in Switching Regulators

Never Has so Much Trouble Been Had By so Many with so Few Terminals

Jim Williams
 David Beebe

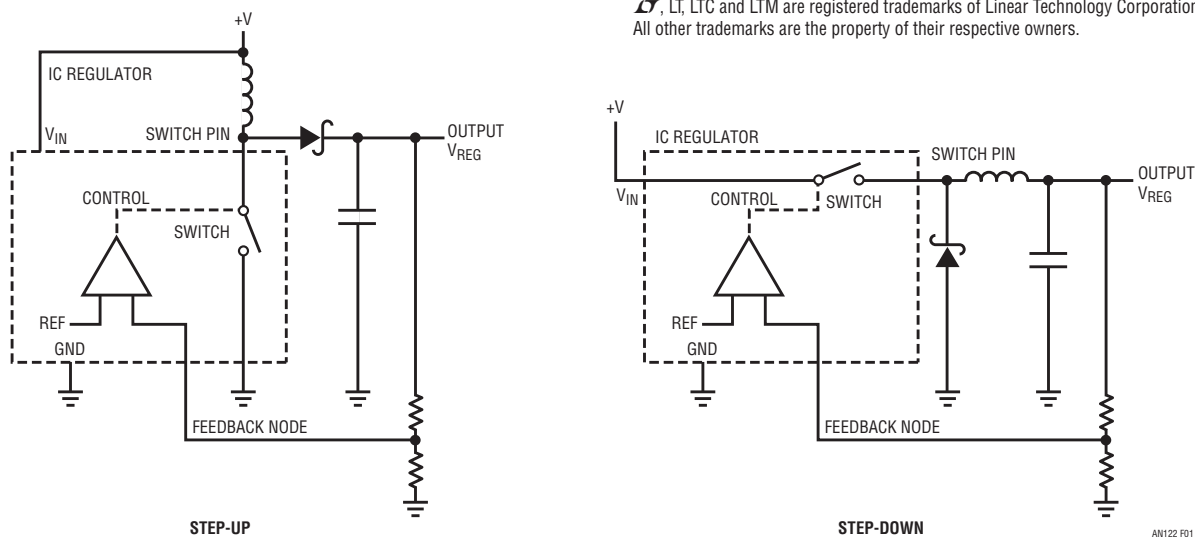
Introduction

Most circuit designers are familiar with diode dynamic characteristics such as charge storage, voltage dependent capacitance and reverse recovery time. Less commonly acknowledged and manufacturer specified is diode forward turn-on time. This parameter describes the time required for a diode to turn on and clamp at its forward voltage drop. Historically, this extremely short time, units of nanoseconds, has been so small that user and vendor alike have essentially ignored it. It is rarely discussed and almost never specified. Recently, switching regulator clock rate and transition time have become faster, making diode turn-on time a critical issue. Increased clock rates are mandated to achieve smaller magnetics size; decreased transition times somewhat aid overall efficiency but are principally needed to minimize IC heat rise. At clock speeds beyond about 1MHz, transition time losses are the primary source of die heating.

A potential difficulty due to diode turn-on time is that the resultant transitory “overshoot” voltage across the diode, even when restricted to nanoseconds, can induce overvoltage stress, causing switching regulator IC failure. As such, careful testing is required to qualify a given diode for a particular application to insure reliability. This testing, *which assumes low loss surrounding components and layout in the final application*, measures turn-on overshoot voltage due to diode parasitics only. Improper associated component selection and layout will contribute additional overstress terms.

Diode Turn-On Time Perspectives

Figure 1 shows typical step-up and step-down voltage converters. In both cases, the assumption is that the diode clamps switch pin voltage excursions to safe limits. In the step-up case, this limit is defined by the switch pins maximum allowable forward voltage. The step-down case limit is set by the switch pins maximum allowable reverse voltage.



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Figure 1. Typical Voltage Step-Up/Step-Down Converters. Assumption is Diode Clamps Switch Pin Voltage Excursion to Safe Limits

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Application Note 122

Figure 2 indicates the diode requires a finite length of time to clamp at its forward voltage. This *forward turn-on time* permits transient excursions above the nominal diode clamp voltage, potentially exceeding the IC's breakdown limit. The turn-on time is typically measured in nanoseconds, making observation difficult. A further complication is that the turn-on overshoot occurs at the amplitude extreme of a pulse waveform, precluding high resolution amplitude measurement. These factors must be considered when designing a diode turn-on test method.

Figure 3 shows a conceptual method for testing diode turn-on time. Here, the test is performed at 1A although other currents could be used. A pulse steps 1A into the diode under test via the 5Ω resistor. Turn-on time voltage

excursion is measured directly at the diode under test. The figure is deceptively simple in appearance. In particular, the current step must have an exceptionally fast, high-fidelity transition and faithful turn-on time determination requires substantial measurement bandwidth.

Detailed Measurement Scheme

A more detailed measurement scheme appears in Figure 4. Necessary performance parameters for various elements are called out. A sub-nanosecond rise time pulse generator, 1A, 2ns rise time amplifier and a 1GHz oscilloscope are required. These specifications represent realistic operating conditions; other currents and rise times can be selected by altering appropriate parameters.

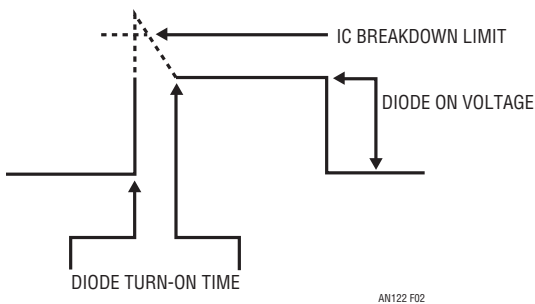


Figure 2. Diode Forward Turn-On Time Permits Transient Excursion Above Nominal Diode Clamp Voltage, Potentially Exceeding IC Breakdown Limit

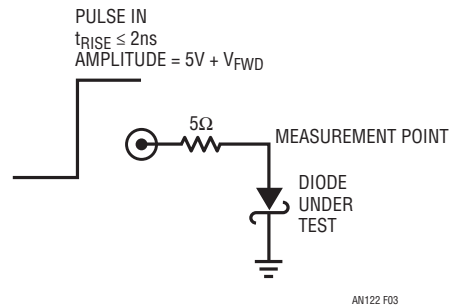


Figure 3. Conceptual Method Tests Diode Turn-On Time at 1A. Input Step Must Have Exceptionally Fast, High Fidelity Transition

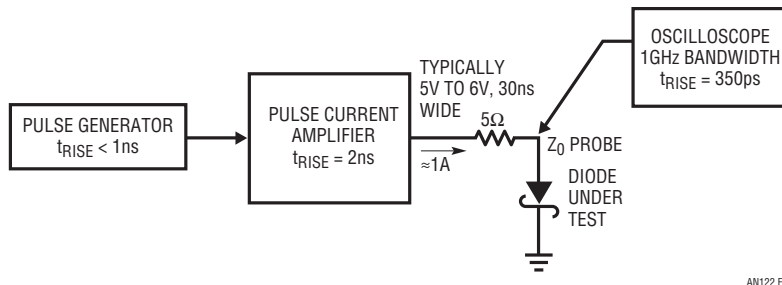
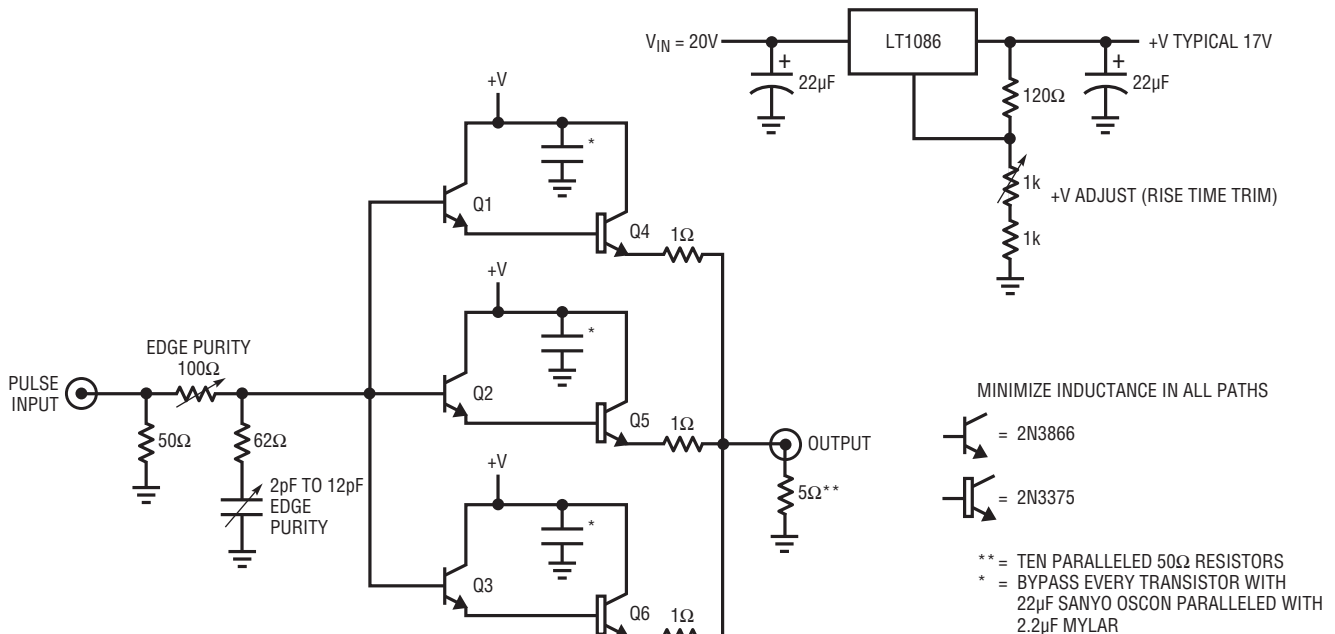


Figure 4. Detailed Measurement Scheme Indicates Necessary Performance Parameters for Various Elements. Sub-Nanosecond Rise Time Pulse Generator, 1A, 2ns Rise Time Amplifier and 1GHz Oscilloscope are Required

The pulse amplifier necessitates careful attention to circuit configuration and layout. Figure 5 shows the amplifier includes a paralleled, Darlington driven RF transistor output stage. The collector voltage adjustment (“rise time trim”) peaks Q4 to Q6 F_T ; an input RC network optimizes output pulse purity by slightly retarding input pulse rise time to within amplifier passband. Paralleling allows Q4 to Q6 to operate at favorable individual currents, maintain-

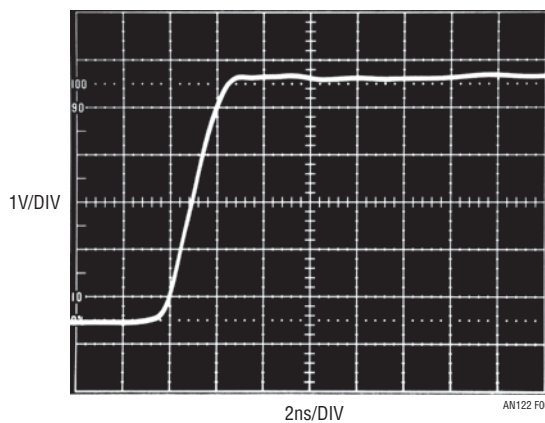
ing bandwidth. When the (mildly interactive) edge purity and rise time trims are optimized, Figure 6 indicates the amplifier produces a transcendentally clean 2ns rise time output pulse devoid of ringing, alien components or post-transition excursions. Such performance makes diode turn-on time testing practical.¹

Note 1. An alternate pulse generation approach appears in Appendix F, “Another Way to Do It.”



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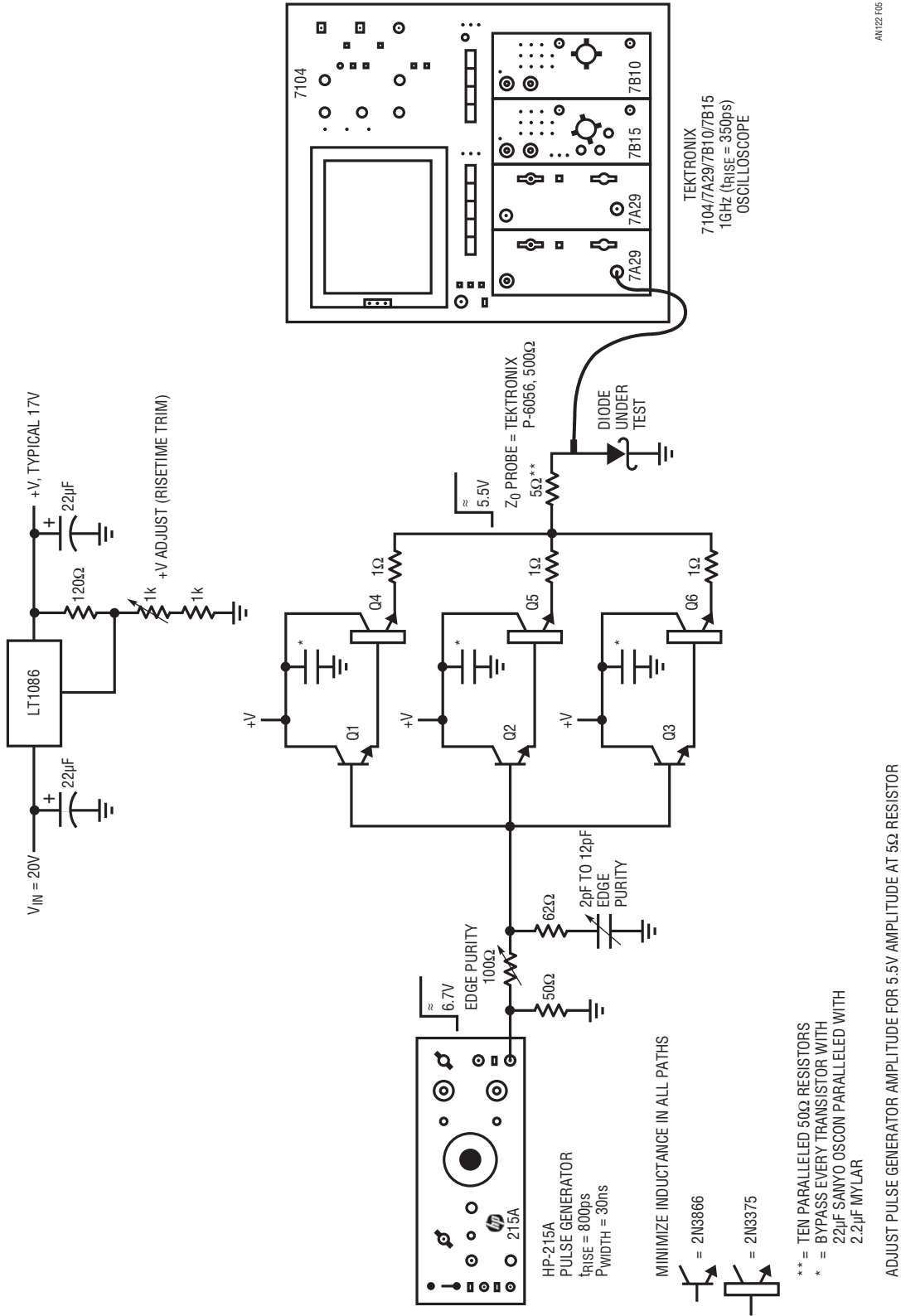
Figure 5. Pulse Amplifier Includes Paralleled, Darlington Driven RF Transistor Output Stage. Collector Voltage Adjustment (“Rise Time Trim”) Peaks Q4 to Q6 F_T , Input RC Network Optimizes Output Pulse Purity. Low Inductance Layout is Mandatory



AN122 F06

Figure 6. Pulse Amplifier Output into 5Ω. Rise Time is 2ns with Minimal Pulse-Top Aberrations

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AN122 F05

Figure 7. Complete Diode Forward Turn-On Time Measurement Arrangement Includes Sub-Nanosecond Rise Time Pulse Generator, Pulse Amplifier, Z_0 Probe and 1GHz Oscilloscope

Figure 7 depicts the complete diode forward turn-on time measurement arrangement. The pulse amplifier, driven by a sub-nanosecond pulse generator, drives the diode under test. A Z_0 probe monitors the measurement point and feeds a 1GHz oscilloscope.^{2, 3, 4}

Diode Testing and Interpreting Results

The measurement test fixture, properly equipped and constructed, permits diode turn-on time testing with excellent time and amplitude resolution.⁵ Figures 8 through 12 show results for five different diodes from various manufacturers. Figure 8 (Diode Number 1) overshoots steady state forward voltage for 3.6ns, peaking 200mV. This is the best performance of the five. Figures 9 through 12 show increasing turn-on amplitude and time which are detailed in the figure captions. In the worst cases, turn-on amplitudes exceed nominal clamp voltage by more than

1V while turn-on times extend for tens of nanoseconds. Figure 12 culminates this unfortunate parade with huge time and amplitude errors. Such errant excursions can and will cause IC regulator breakdown and failure. The lesson here is clear. Diode turn-on time must be characterized and measured in any given application to insure reliability.

Note 2. Z_0 probes are described in Appendix C, “About Z_0 Probes”. See also References 27 thru 34.

Note 3. The sub-nanosecond pulse generator requirement is not trivial. See Appendix B, “Subnanosecond Rise Time Pulse Generators For The Rich and Poor.”

Note 4. See Appendix E, “Connections, Cables, Adapters, Attenuators, Probes and Picoseconds” for relevant commentary.

Note 5. See Appendix A, “How Much Bandwidth is Enough?” for discussion on determining necessary measurement bandwidth.

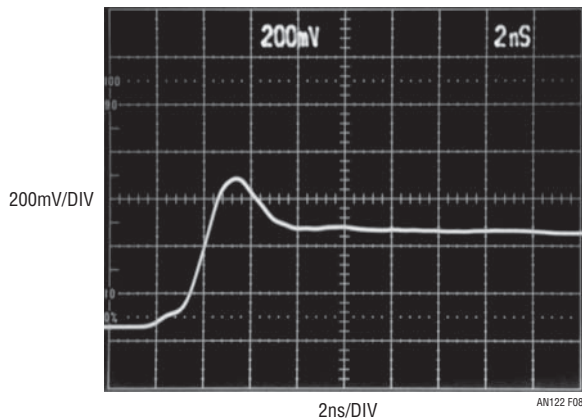


Figure 8. “Diode Number 1” Overshoots Steady State Forward Voltage for ≈ 3.6 ns, Peaking 200mV

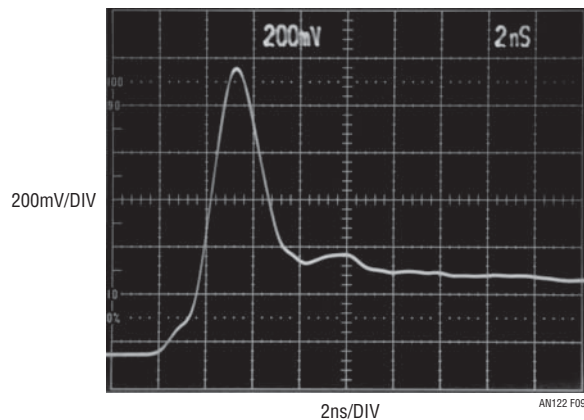


Figure 9. “Diode Number 2” Peaks ≈ 750 mV Before Settling in 6ns... $> 2x$ Steady State Forward Voltage

Application Note 122

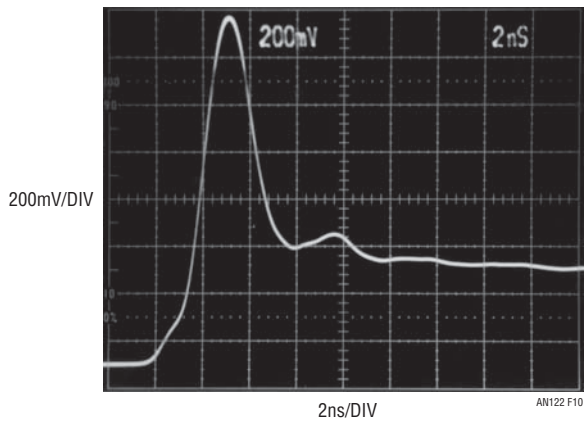


Figure 10. “Diode Number 3” Peaks 1V Above Nominal 400mV V_{FWD} , a 2.5x Error

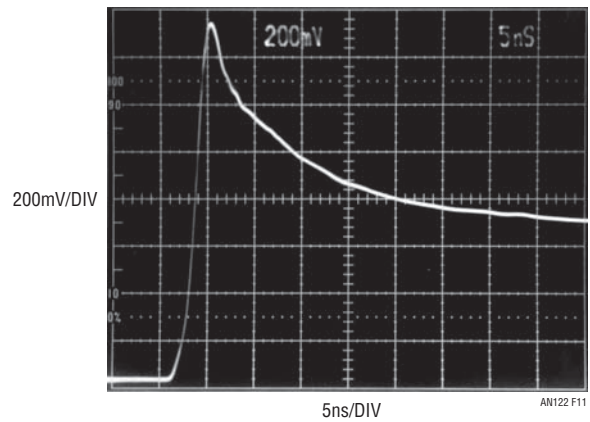


Figure 11. “Diode Number 4” Peaks $\approx 750\text{mV}$ with Lengthy (Note Horizontal 2.5x Scale Change) Tailing Towards V_{FWD} Value

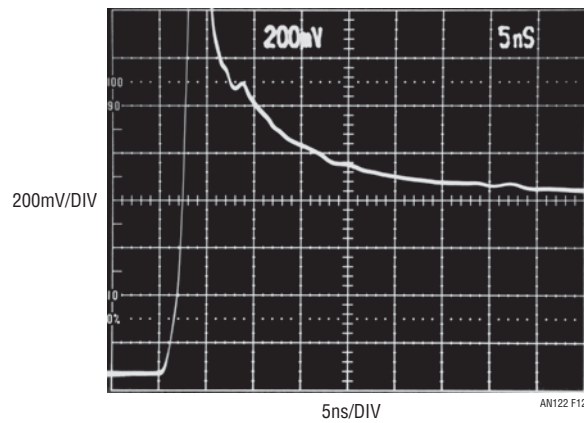


Figure 12. “Diode Number 5” Peaks Offscale with Extended Tailing (Note Horizontal Slower Scale Compared to Figures 8 thru 10)

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Application Note 122

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APPENDIX A

HOW MUCH BANDWIDTH IS ENOUGH?

Accurate wideband oscilloscope measurements require bandwidth. A good question is just how much is needed. A classic guideline is that "end-to-end" measurement system rise time is equal to the root-sum-square of the system's individual components' rise times. The simplest case is two components; a signal source and an oscilloscope.

Figure A1's plot of $\sqrt{\text{Signal}^2 + \text{Oscilloscope}^2}$ rise time versus error is illuminating. The figure plots signal-to-oscilloscope rise time ratio versus observed rise time (rise time is bandwidth restated in the time domain, where:

$$\text{Rise Time (ns)} = \frac{350}{\text{Bandwidth(MHz)}}$$

The curve shows that an oscilloscope 3 to 4 times faster than the input signal rise time is required for measurement accuracy inside about 5%. This is why trying to measure a 1ns rise time pulse with a 350MHz oscilloscope ($t_{\text{RISE}} = 1\text{ns}$) leads to erroneous conclusions. The curve indicates a monstrous 41% error. Note that this curve does not

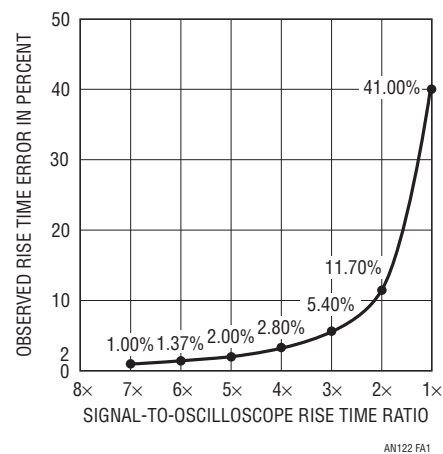


Figure A1. Oscilloscope Rise Time Effect on Rise Time Measurement Accuracy. Measurement Error Rises Rapidly as Signal-to-Oscilloscope Rise Time Ratio Approaches Unity. Data, Based on Root-Sum-Square Relationship, Does Not Include Probe, Which May Not Follow Root-Sum-Square Law

include the effects of passive probes or cables connecting the signal to the oscilloscope. Probes do not necessarily follow root-sum-square law and must be carefully chosen

and applied for a given measurement. Figure A2, included for reference, gives 10 cardinal points of rise time/bandwidth equivalency between 1MHz and 5GHz.

Figures A3 through A10 illustrate pertinent effects of these considerations by viewing the text's diode turn-on time measurement at various bandwidths.¹ Figure A3 displays a typical diode turn-on in a 2.5GHz sampled bandpass, showing 500mV turn-on amplitude.² Figure A4's 1GHz bandwidth measurement has nearly identical character-

istics, indicating adequate oscilloscope bandwidth. The dramatic error in observed turn-on overshoot amplitude as bandwidth decreases in succeeding figures is readily apparent and should not be lost to the experimenter.

Note 1. Prudent investigation requires verifying bandwidth of all elements in the signal path. See Appendix D, "Verifying Rise Time Measurement Integrity."

Note 2. 3.9GHz oscilloscope + 3.5GHz probe = 2.5GHz probe tip bandwidth.

RISE TIME	BANDWIDTH
70ps	5GHz
350ps	1GHz
700ps	500MHz
1ns	350MHz
2.33ns	150MHz
3.5ns	100MHz
7ns	50MHz
35ns	10MHz
70ns	5MHz
350ns	1MHz

Figure A2. Some Cardinal Points of Rise Time/Bandwidth Equivalency. Data is Based on Rise Time/Bandwidth Formula in Text

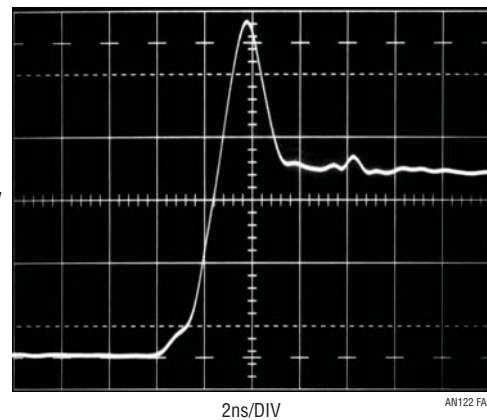


Figure A3. Typical Diode Turn-On Viewed in 2.5GHz Sampled Bandpass Displays 500mV Turn-On Peak

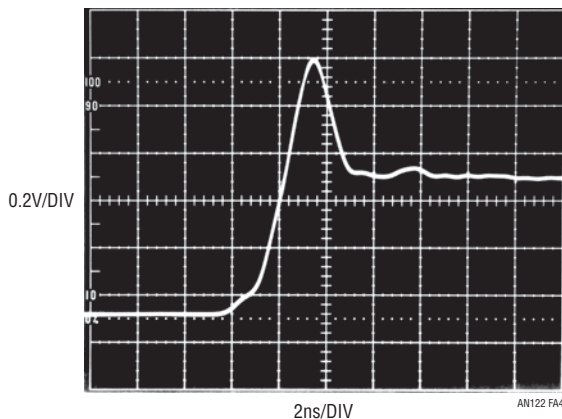


Figure A4. Figure A3's Diode Turn-On Observed in 1GHz Real Time Bandwidth Has Nearly Identical Characteristics, Indicating Adequate Oscilloscope Bandwidth

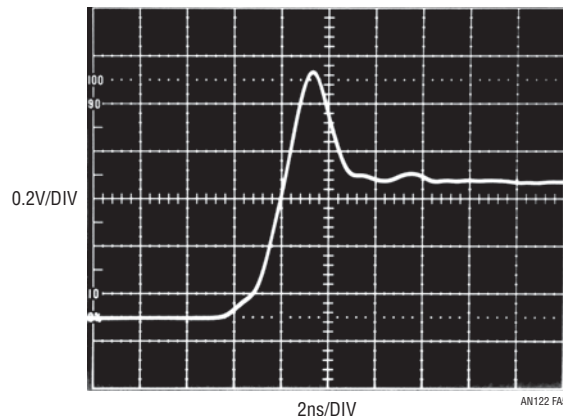


Figure A5. 600MHz Oscilloscope Bandwidth Results in ~440mV Observed Peak, an 12% Amplitude Error

Application Note 122

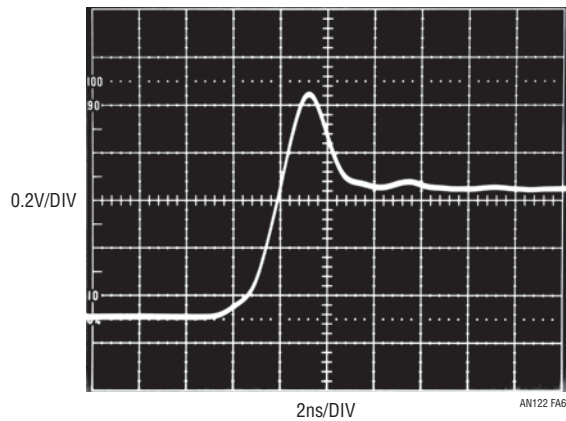


Figure A6. 400MHz Measurement Bandwidth Causes 20% Error

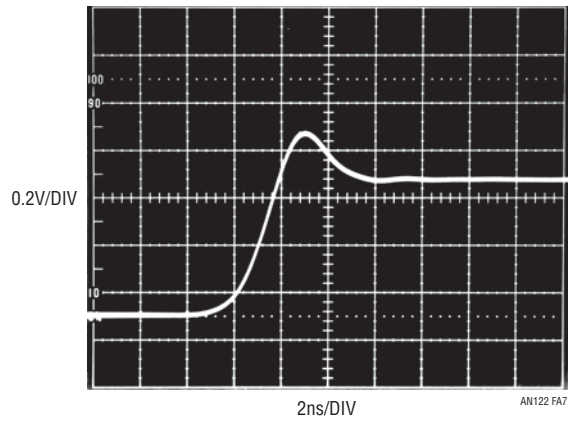


Figure A7. 60% Error Occurs with 200MHz Oscilloscope Bandwidth

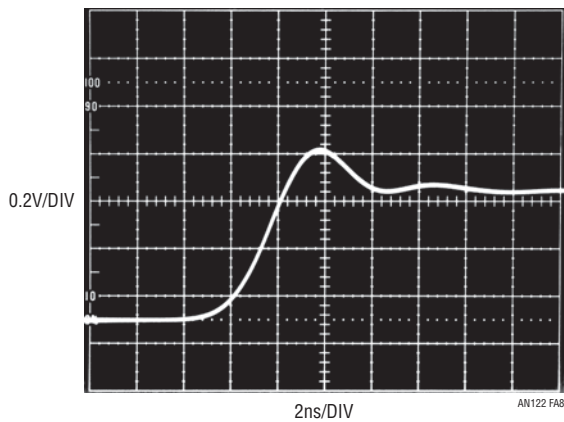


Figure A8. 65% Error (!) in 75MHz Bandwidth

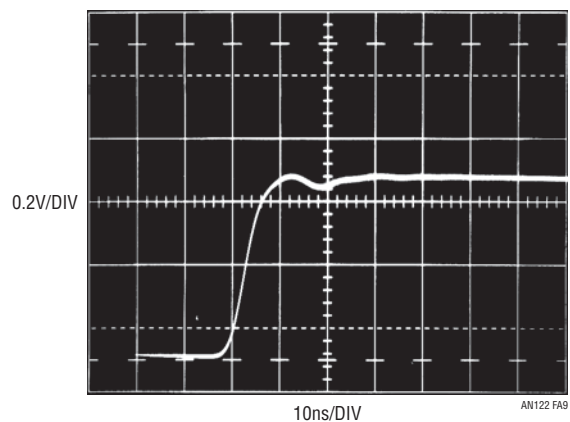


Figure A9. 50MHz Oscilloscope Just Hints at Peaking. Note 5x Horizontal Scale Change vs Figures A3 through A8

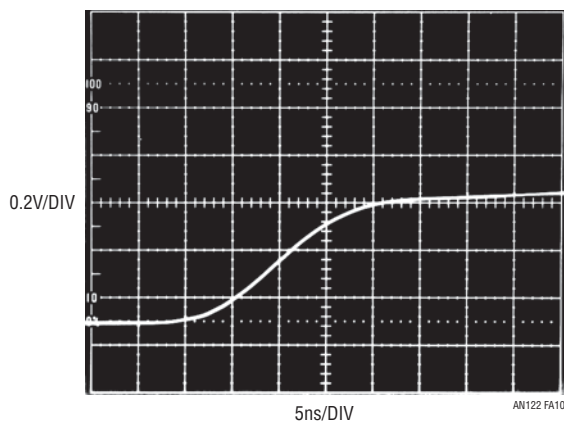


Figure A10. 20MHz Oscilloscope Bandwidth Presentation is Smooth...and Worthless. Note 2.5x Horizontal Scale Change vs Figures A3 through A8

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APPENDIX B

SUBNANOSECOND RISE TIME PULSE GENERATORS FOR THE RICH AND POOR

The pulse amplifier requires a sub-nanosecond input rise time pulse to cleanly switch current to the diode under test. The majority of general purpose pulse generators have rise times in the 2.5ns to 10ns range. Instrument rise times below 2.5ns are relatively rare, with only a select few types getting down to 1ns. The ranks of sub-nanosecond rise time generators are even thinner, and costs are, in this author's view, excessive. Sub-nanosecond rise time generation, particularly if relatively large swings (e.g. 5V to 10V) are desired, employs arcane technologies and exotic construction techniques. Available instruments in this class work well, but can easily cost \$10,000 with prices rising towards \$30,000 depending on features. For bench work, or even production testing, there are substantially less expensive approaches.

The secondary market offers sub-nanosecond rise time pulse generators at attractive cost. The Hewlett-Packard HP-8082A transitions in under 1ns, has a full complement of controls and costs about \$500. The Tektronix type 111 has edge times of 500ps, with fully variable repetition rate and external trigger capabilities. Pulse width is set by external charge line length. Price is usually about \$25. The HP-215A, long out of manufacture, has 800ps edge times and is a clear bargain, with typical price below \$50.¹ This instrument also has a very versatile trigger output, permitting continuous trigger time phase adjustment from before to after the main output. External trigger impedance, polarity and sensitivity are also variable. The output, controlled by a stepped attenuator, will put a clean $\pm 10V$ pulse into 50Ω in 800ps.²

400ps Rise Time Avalanche Pulse Generator

A potential problem with older instruments is availability.³ As such, Figure B1 shows a circuit for producing sub-nanosecond rise time pulses. Rise time is 400ps, with adjustable pulse amplitude. Output pulse occurrence is settable from before-to-after a trigger output. This circuit uses an avalanche pulse generator to create extremely fast rise time pulses.⁴

Q1 and Q2 form a current source that charges the 1000pF capacitor. When the LTC1799 clock is high (trace A, Fig-

ure B2) both Q3 and Q4 are on. The current source is off and Q2's collector (trace B) is at ground. C1's latch input prevents it from responding and its output remains high. When the clock goes low, C1's latch input is disabled and its output drops low. The Q3 and Q4 collectors lift and Q2 comes on, delivering constant current to the 1000pF capacitor (trace B). The resulting linear ramp is applied to C1 and C2's positive inputs. C2, biased from a potential derived from the 5V supply, goes high 30ns after the ramp begins, providing the "trigger output" (trace C) via its output network. C1 goes high when the ramp crosses the potentiometer programmed delay at its negative input, in this case about 170ns. C1 going high triggers the avalanche-based output pulse (trace D), which will be described. This arrangement permits the delay programming control to vary output pulse occurrence from 30ns before to 300ns after the trigger output. Figure B3 shows the output pulse (trace D) occurring 25ns before the trigger output. All other waveforms are identical to Figure B2.

When C1's output pulse is applied to Q5's base, it avalanches. The result is a quickly rising pulse across Q5's emitter termination resistor. The collector capacitors and the charge line discharge, Q5 collector voltage falls and breakdown ceases. The collector capacitors and the charge line then recharge. At C1's next pulse, this action repeats. The capacitors supply initial pulse response, with the charge lines prolonged discharge contributing the pulse body. The 40" charge line length forms an output pulse width about 12ns in duration.

Avalanche operation requires high voltage bias. The LT1533 low noise switching regulator and associated components supply this high voltage. The LT1533 is a "push-pull" output switching regulator with controllable transition times.

Note 1. The absurdly low valuation may be due to the instrument's front panel controls and markings, which only subtly hint at its capabilities.

Note 2. Instrument aficionados would do well to study this instrument's elegant step-recovery diode based output stage, a thing of exotic beauty. See Reference 35.

Note 3. Residents of Silicon Valley tend towards inbred techno-provincialism. Citizens of other locales cannot simply go to a flea market, junk store or garage sale and buy a sub-nanosecond pulse generator.

Note 4. The circuit's operation essentially duplicates the aforementioned Tektronix type 111 pulse generator (see Reference 11). Information on avalanche operation appears in References 7 through 25.

Application Note 122

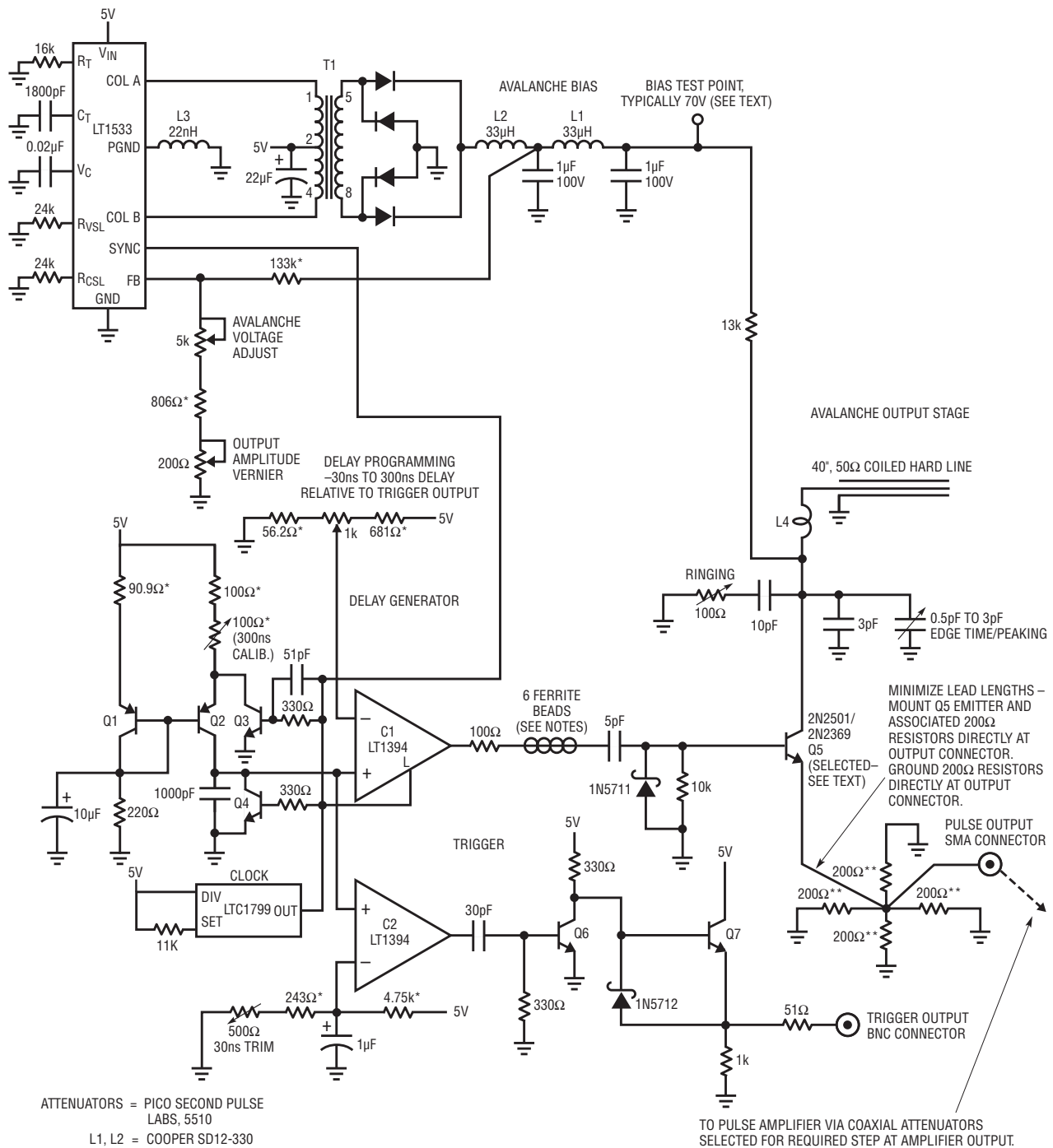


Figure B1. Variable Delay Triggers a Sub-Nanosecond Rise Time Pulse Generator. Charge Line at Q5's Collector Determines ~10ns Output Width. Output Pulse Occurrence is Settable from Before-to-After Trigger Output

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Output harmonic content (“noise”) is notably reduced with slower switch transition times.⁵ Switch current and voltage transition times are controlled by resistors at the R_{CSL} and R_{VSL} pins, respectively. In all other respects the circuit behaves as a classical push-pull, step-up converter.

Circuit Optimization

Circuit optimization begins by setting the “Output Amplitude Vernier” to maximum and grounding Q4’s collector. Next, set the “Avalanche Voltage Adjust” so free running pulses *just* appear at Q5’s emitter, noting the bias test points voltage. Readjust the “Avalanche Voltage Adjust” 5V below this voltage and unground Q4’s collector. Set the “30ns Trim” so the trigger output goes low 30ns after the clock goes low. Adjust the delay programming control to maximum and set the “300ns Calib.” so C1 goes high 300ns after the clock goes low. Slight interaction between the 30ns and 300ns trims may require repeating their adjustments until both points are calibrated.

Q5 requires selection for optimal avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 30 2N2501s, spread over a 17-year date code span, yielded $\approx 90\%$. All “good” devices switched in less than 475ps with some below 300ps.⁶ In practice, Q5 should be selected for “in-circuit” rise time under 400ps. Once this is done, output pulse shape is optimized by adjusting Q5’s collector damping trims (“edge time/peaking” and “ringing”).

The trims are somewhat interactive, but not unduly so, and optimal adjustment converges nicely. The pulse edge is carefully adjusted so that maximum transition speed is attained with minimal sacrifice of pulse purity.⁷ Figures B4 through B6 detail the optimization procedure. In Figure B4, the trims are set for significant effect, resulting in a reasonably clean pulse but sacrificing rise time.⁸ Figure B5 represents the opposite extreme. Minimal trim effect accentuates rise time, but promotes post-transition ring. Figure B6’s compromise trimming is more desirable. Edge rate is only slightly reduced, but post-transition ring is significantly retarded, resulting in a 400ps rise time with high pulse purity.^{9, 10}

Note 5. The LT1533’s low noise performance and its measurement are discussed in Reference 25.

Note 6. 2N2501s are available from Semelab plc. Sales@semelab.co.uk; Tel. 44-0-1455-556565. A more common transistor, the 2N2369, may also be used but switching times are rarely less than 450ps.

Note 7. Optimization procedures for obtaining high degrees of pulse purity while preserving rise time appear in Reference 11.

Note 8. The strata is becoming rarefied when a sub-nanosecond rise time is described as “sacrificed”.

Note 9. Faster rise times are possible, although considerable finesse is required in Q5’s selection, layout, mounting, terminal impedance choice and triggering. The 400ps rise time quoted represents readily reproducible results. Rise times below 300ps have been achieved, but require tedious effort.

Note 10. Accurate rise time determination at these speeds mandates verifying measurement signal path (cables, attenuators, probes, oscilloscope) integrity. See Appendix D, “Verifying Rise Time Measurement Integrity” and Appendix E, “Connections, Cables, Adapters, Attenuators, Probes and Picoseconds.”

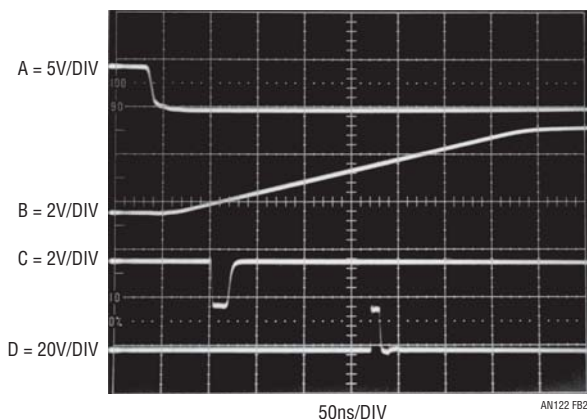


Figure B2. Pulse Generator’s Waveforms Include Clock (Trace A), Q2’s Collector Ramp (Trace B), Trigger Output (Trace C) and Pulse Output (Trace D). Delay Sets Output Pulse ≈ 170 ns After Trigger Output

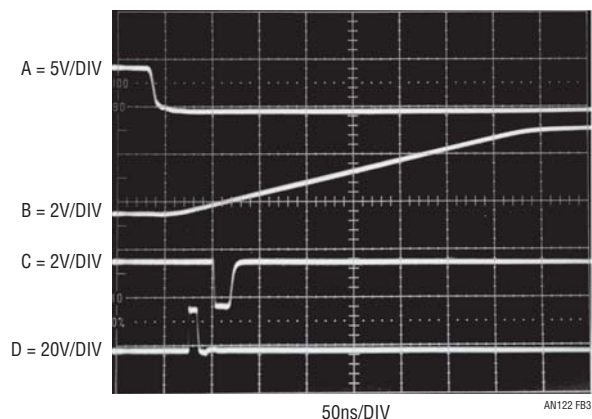


Figure B3. Pulse Generator’s Waveforms with Delay Adjusted for Output Pulse Occurrence (Trace D) 25ns Before Trigger Output (Trace C). All Other Activity is Identical to Previous Figure

Application Note 122

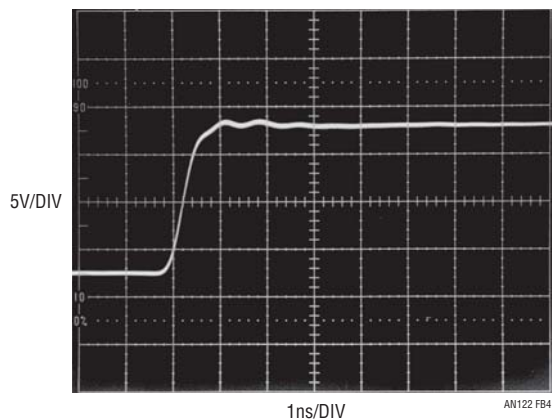


Figure B4. Excessive Damping is Characterized by Front Corner Rounding and Minimal Pulse-Top Aberrations. Trade Off is Relatively Slow Rise Time

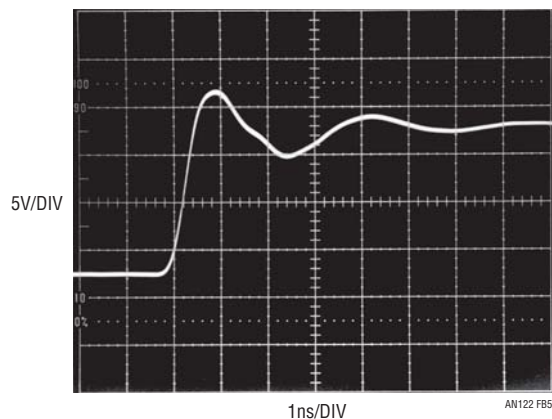


Figure B5. Minimal Damping Accentuates Rise Time, Although Pulse-Top Ringing is Excessive

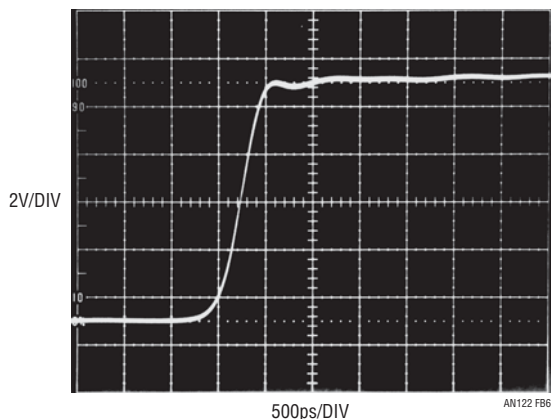


Figure B6. Optimal Damping Retards Pulse-Top Ringing While Preserving Rise Time

APPENDIX C

ABOUT Z_0 PROBES

When to Roll Your Own and When to Pay the Money

Z_0 (e.g. “low impedance”) probes provide the most faithful high speed probing mechanism available for low source impedances. Their sub-picofarad input capacitance and near ideal transmission characteristic make them the first choice for high bandwidth oscilloscope measurement. Their deceptively simple operation invites “do-it-yourself” construction but numerous subtleties mandate difficulty for

prospective constructors. Arcane parasitic effects introduce errors as speed increases beyond about 100MHz (t_{RISE} 3.5ns). The selection and integration of probe materials and the probes physical incarnation require extreme care to obtain high fidelity at high speed. Additionally, the probe must include some form of adjustment to compensate small, residual parasitics. Finally, true coaxiality must be maintained when fixturing the probe at the measurement point, implying a high grade, readily disconnectable, coaxial connection capability.

Figure C1 shows that a Z_0 probe is basically a voltage divided input 50Ω transmission line. If $R1$ equals 450Ω , $10\times$ attenuation and 500Ω input resistance result. $R1$ of 4950Ω causes a $100\times$ attenuation with $5k$ input resistance. The 50Ω line theoretically constitutes a distortionless transmission environment. The apparent simplicity seemingly permits “do-it-yourself” construction but this section’s remaining figures demonstrate a need for caution.

Figure C2 establishes a fidelity reference by measuring a clean $700ps$ rise time pulse using a 50Ω line terminated via a coaxial attenuator – no probe is employed. The waveform is singularly clean and crisp with minimal edge and

post-transition aberrations. Figure C3 depicts the same pulse with a commercially produced $10\times Z_0$ probe in use. The probe is faithful and there is barely discernible error in the presentation. Photos C4 and C5, taken with two separately constructed “do-it-yourself” Z_0 probes, show errors. In C4, “Probe #1” introduces pulse front corner rounding; “Probe #2” in C5 causes pronounced corner peaking. In each case, some combination of resistor/cable parasitics and incomplete coaxiality are likely responsible for the errors. In general, “do-it-yourself” Z_0 probes cause these types of errors beyond about $100MHz$ ($t_{RISE} = 3.5ns$). At higher speeds, if waveform fidelity is critical, it’s best to pay the money.

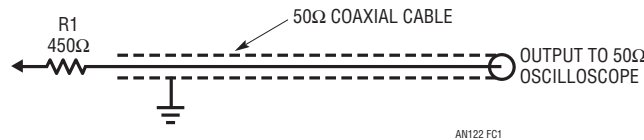


Figure C1. Conceptual 500Ω , “ Z_0 ”, $10\times$ Oscilloscope Probe. If $R1 = 4950\Omega$, $5k$ Input Resistance with $100\times$ Signal Attenuation Results. Terminated Into 50Ω , Probe Theoretically Constitutes a Distortionless Transmission Line. “Do It Yourself” Probes Suffer Uncompensated Parasitics, Causing Unfaithful Response Above $\approx 100MHz$ ($t_{RISE} = 3.5ns$)

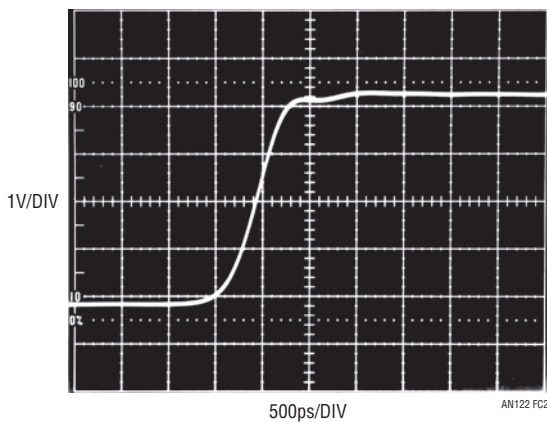


Figure C2. $700ps$ Rise Time Pulse Observed Via 50Ω Line and Coaxial Attenuator Has Good Pulse Edge Fidelity With Controlled Post-Transition Events

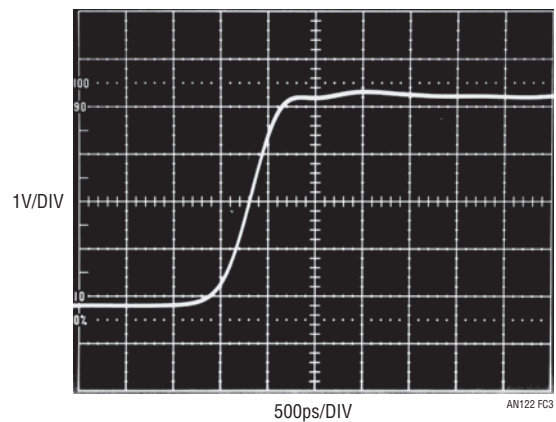


Figure C3. Figure C2’s Pulse Viewed With Tektronix Z_0 500Ω Probe (P-6056) Introduces Barely Discernible Error

Application Note 122

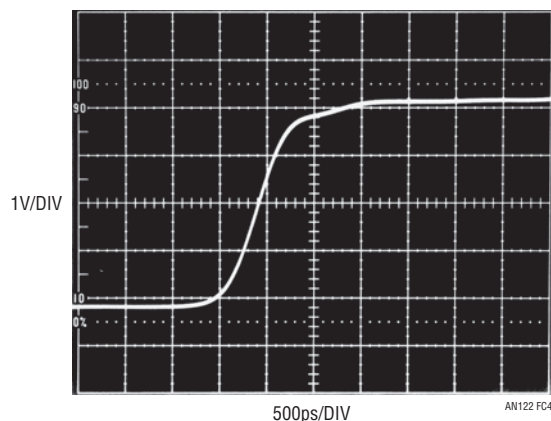


Figure C4. “Do It Yourself” Z_0 Probe #1 Introduces Pulse Corner Rounding, Likely Due to Resistor/Cable Parasitic Terms or Incomplete Coaxiality. “Do It Yourself” Z_0 Probes Typically Manifest This Type Error at Rise Times ≤ 2 ns

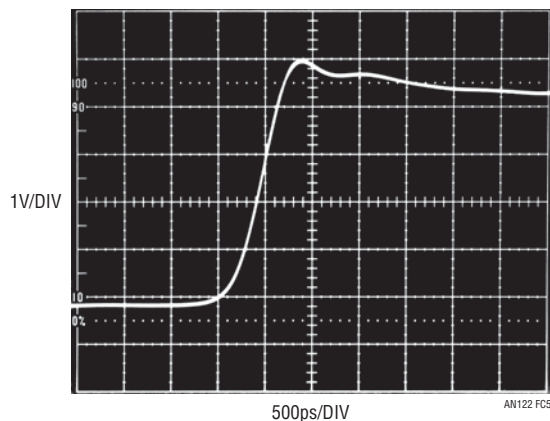


Figure C5. “Do It Yourself” Z_0 Probe #2 Has Overshoot, Again Likely Due to Resistor/Cable Parasitic Terms or Incomplete Coaxiality. Lesson: At These Speeds, Don’t “Do It Yourself”

APPENDIX D

VERIFYING RISE TIME MEASUREMENT INTEGRITY

Any measurement requires the experimenter to insure measurement confidence. Some form of calibration check is always in order. High speed time domain measurement is particularly prone to error and various techniques can promote measurement integrity.

Figure D1’s battery-powered 200MHz crystal oscillator produces 5ns markers, useful for verifying oscilloscope time base accuracy. A single 1.5 AA cell supplies the LTC3400 boost regulator, which produces 5V to run the oscillator. Oscillator output is delivered to the 50 Ω load via a peaked attenuation network. This provides well defined 5ns markers (Figure D2) and prevents overdriving low level sampling oscilloscope inputs.

Once time base accuracy is confirmed it is necessary to check rise time. The lumped signal path rise time, including attenuators, connections, cables, probes, oscilloscope and anything else, should be included in this measurement. Such “end-to-end” rise time checking is an effective way to promote meaningful results. A guideline for insuring accuracy is to have 4x faster measurement path rise time than the rise time of interest. Thus, Appendix Figure B6’s 400ps rise time measurement requires a verified 100ps measurement path rise time to support it. Verifying the 100ps measurement path rise time, in turn, necessitates a 25ps rise time test step. Figure D3 lists some very fast edge generators for rise time checking.¹

The Hewlett-Packard 1105A/1106A, specified at 20ps rise time, was used to verify Appendix Figure A3’s measurement signal path. Figure D4 indicates a 140ps rise time, promoting measurement confidence.

Note 1. This is a fairly exotic group, but equipment of this caliber really is necessary for rise time verification.

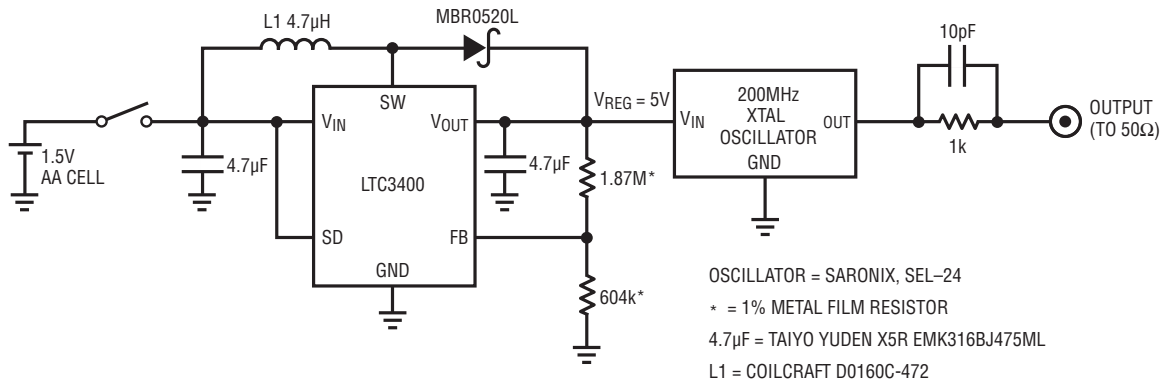


Figure D1. 1.5V Powered, 200MHz Crystal Oscillator Provides 5ns Time Markers. Switching Regulator Converts 1.5V to 5V to Power Oscillator

MANUFACTURER	MODEL NUMBER	RISE TIME	AMPLITUDE	AVAILABILITY	COMMENTS
Avtech	AVP2S	40ps	0V to 2V	Current Production	Free Running or Triggered Operation, 0MHz to 1MHz
Hewlett-Packard	213B	100ps	≈175mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Hewlett-Packard	1105A/1108A	60ps	≈200mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Hewlett-Packard	1105A/1106A	20ps	≈200mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Picosecond Pulse Labs	TD1110C/TD1107C	20ps	≈230mV	Current Production	Similar to Discontinued HP1105/1106/8A. See above.
Stanford Research Systems	DG535 OPT 04A	100ps	0.5V to 2V	Current Production	Must be Driven with Stand-alone Pulse Generator
Tektronix	284	70ps	≈200mV	Secondary Market	50kHz Repetition Rate. Pre-trigger 75ns to 150ns Before Main Output. Calibrated 100MHz and 1GHz Sine Wave Auxiliary Outputs.
Tektronix	111	500ps	≈±10V	Secondary Market	10kHz to 100kHz Repetition Rate. Positive or Negative Outputs. 30ns to 250ns Pre-trigger Output. External Trigger Input. Pulse Width Set with Charge Lines
Tektronix	067-0513-00	30ps	≈400mV	Secondary Market	60ns Pre-trigger Output. 100kHz Repetition Rate
Tektronix	109	250ps	0V to ±55V	Secondary Market	≈600Hz Repetition Rate (High Pressure Hg Reed Relay Based). Positive or Negative Outputs. Pulse Width Set by Charge Lines

Figure D3. Picosecond Edge Generators Suitable for Rise Time Verification. Considerations Include Speeds, Features and Availability

Application Note 122

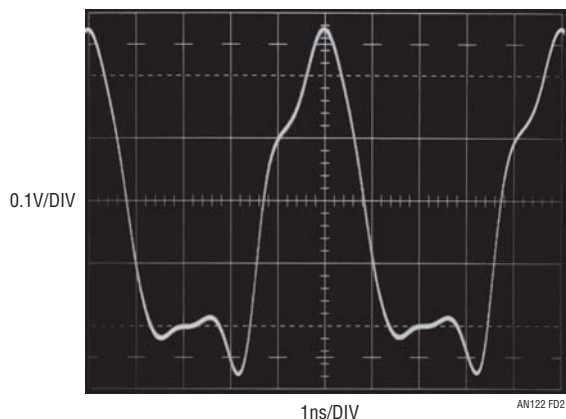


Figure D2. Time Mark Generator Output Terminated into 50Ω. Peaked Waveform is Optimal for Verifying Time Base Calibration

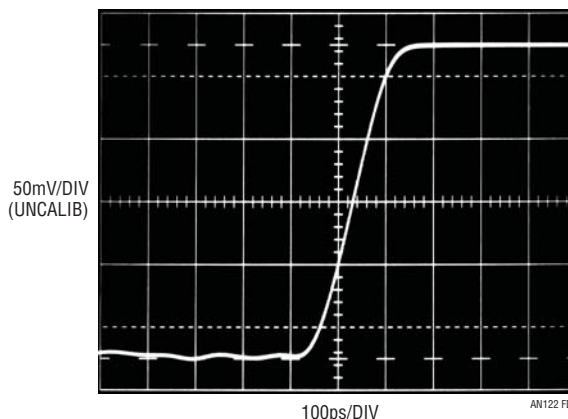


Figure D4. 20ps Step Produces ~140ps Probe/Oscilloscope Rise Time, Verifying Appendix Figure A3's Signal Path Rise Time

APPENDIX E

CONNECTIONS, CABLES, ADAPTERS, ATTENUATORS, PROBES AND PICOSECONDS

Sub-nanosecond rise time signal paths must be considered as transmission lines. Connections, cables, adapters, attenuators and probes represent discontinuities in this transmission line, deleteriously affecting its ability to faithfully transmit desired signal. The degree of signal corruption contributed by a given element varies with its deviation from the transmission lines nominal impedance. The practical result of such introduced aberrations is degradation of pulse rise time, fidelity, or both. Accordingly, introduction of elements or connections to the signal path should be minimized and necessary connections and elements must be high grade components. Any form of connector, cable, attenuator or probe must be fully specified for high frequency use. Familiar BNC hardware becomes lossy at rise times much faster than 350ps. SMA components are preferred for the rise times described in the text. Additionally, to minimize inductance and cable induced mismatch and distortion, the text's pulse amplifier output should be connected *directly* (no cable) to the diode under test. Mixing signal path hardware types via adapters (e.g. BNC/SMA) should be avoided. Adapters introduce significant parasitics, resulting in reflections, rise time degradation, resonances and other degrading behavior.

Similarly, oscilloscope connections should be made directly to the instrument's 50Ω inputs, avoiding probes. If probes must be used, their introduction to the signal path mandates attention to their connection mechanism and high frequency compensation. Passive "Z₀" types, commercially available in 500Ω (10x) and 5kΩ (100x) impedances, have input capacitance below 1pF.¹ Any such probe must be carefully frequency compensated before use or misrepresented measurement will result. Inserting the probe into the signal path necessitates some form of signal pick-off which nominally does not influence signal transmission. In practice, some amount of disturbance must be tolerated and its effect on measurement results evaluated. High quality signal pick-offs always specify insertion loss, corruption factors and probe output scale factor.

The preceding emphasizes vigilance in designing and maintaining a signal path. Skepticism, tempered by enlightenment, is a useful tool when constructing a signal path and no amount of hope is as effective as preparation and directed experimentation.

Note 1. See Appendix C, "About Z₀ Probes"

APPENDIX F

ANOTHER WAY TO DO IT

If some restrictions are tolerable, an elegantly simple alternative method for generating the fast rise 1A pulse is available. The Tektronix type 109 mercury wetted reed relay based pulse generator will put a 50V pulse into 50Ω (1A) in 250ps.¹ Pulse width is set by an externally connected charge line with an approximate scale factor of 2ns/ft. Figure F1, a simplified schematic, shows type 109 operation. When the relay contacts close, the charge line discharges via the 50Ω-diode path. The pulse extends until the line depletes; depletion time depends on line length. The relay

structure is very carefully arranged to assume wideband, 50Ω characteristics. Figure F2 shows the result. The 109 drives the monitoring 1GHz oscilloscope to its 350ps rise time limit with a 50V high fidelity pulse.

Operating restrictions include finite relay life (≈ 200 hours), obtaining the instrument (out of production for 20+ years), difficulty in observing its low frequency output on some oscilloscopes and test fixture layout sensitivity due to the 250ps rise time. Additionally, the faster rise time may not approximate actual circuit operating conditions as closely as the text's 2ns circuit.

Note 1. See Reference 36.

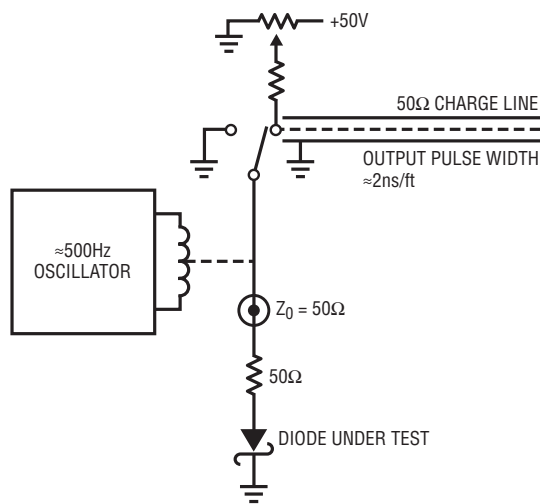


Figure F1. Simplified Operation of Tektronix Type 109 Mercury Wetted Reed Relay Based Pulse Generator. When Right Side Contacts Close, Charge Line Discharges Into 50Ω-Diode Load. Strict Attention to Construction Allows Wideband, 50Ω Characteristics, Permitting 250ps Rise Time, High Purity Output Pulse

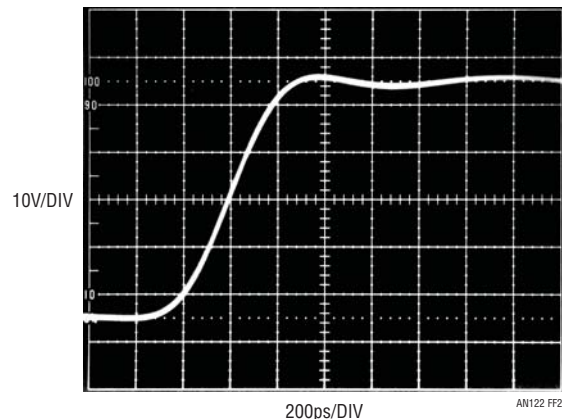
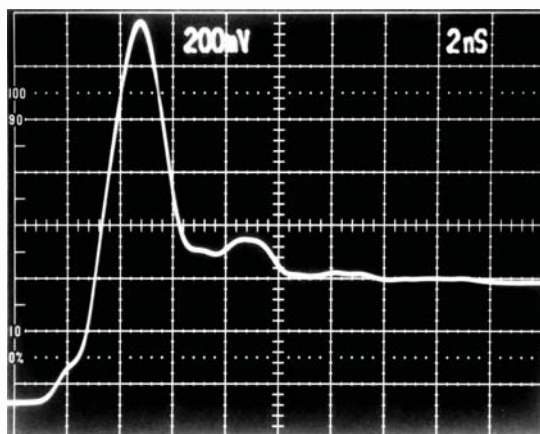


Figure F2. Tektronix Type 109 Produces High Purity, 50V, 1A Pulse, Driving Monitoring 1GHz Oscilloscope to its 350ps Rise Time Limit



"Now I am become Death, the destroyer of worlds."

Vishnu, to the Prince.

Bhagavad Gita

775 Nanovolt Noise Measurement for A Low Noise Voltage Reference

Quantifying Silence

Jim Williams

Introduction

Frequently, voltage reference stability and noise define measurement limits in instrumentation systems. In particular, reference noise often sets stable resolution limits. Reference voltages have decreased with the continuing drop in system power supply voltages, making reference noise increasingly important. The compressed signal processing range mandates a commensurate reduction in reference noise to maintain resolution. Noise ultimately translates into quantization uncertainty in A to D converters, introducing jitter in applications such as scales, inertial navigation systems, infrared thermography, DVMs and medical imaging apparatus. A new low voltage reference, the LTC6655, has only 0.3ppm (775nV) noise at 2.5V_{OUT}. Figure 1 lists salient specifications in tabular form. Accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

Noise Measurement

Special techniques are required to verify the LTC6655's extremely low noise. Figure 2's approach appears innocently straightforward but practical implementation represents a high order difficulty measurement. This 0.1Hz to 10Hz noise

testing scheme includes a low noise pre-amplifier, filters and a peak-to-peak noise detector. The pre-amplifier's 160nV noise floor, enabling accurate measurement, requires special design and layout techniques. A forward gain of 10⁶ permits readout by conventional instruments.

Figure 3's detailed schematic reveals some considerations required to achieve the 160nV noise floor. The reference DC potential is stripped by the 1300μF, 1.2k resistor combination; AC content is fed to Q1. Q1-Q2, extraordinarily low noise J-FET's, are DC stabilized by A1, with A2 providing a single-ended output. Resistive feedback from A2 stabilizes the configuration at a gain of 10,000. A2's output is routed to amplifier-filter A3-A4 which provides 0.1Hz to 10Hz response at a gain of 100. A5-A8 comprise a peak-to-peak noise detector read out by a DVM at a scale factor of 1 volt/microvolt. The peak-to-peak noise detector provides high accuracy measurement, eliminating tedious interpretation of an oscilloscope display. Instantaneous noise value is supplied by the indicated output to a monitoring oscilloscope. The 74C221 one-shot, triggered by the oscilloscope sweep gate, resets the peak-to-peak noise detector at the end of each oscilloscope 10-second sweep.

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LTC6655 Reference Tabular Specifications

SPECIFICATION	LIMITS
Output Voltages	1.250, 2.048, 2.500, 3.000, 3.300, 4.096, 5.000
Initial Accuracy	0.025%, 0.05%
Temperature Coefficient	2ppm/°C, 5ppm/°C
0.1Hz to 10Hz Noise	0.775μV at V _{OUT} = 2.500V, Peak-to-Peak Noise is within this Figure in 90% of 1000 Ten Second Measurement Intervals
Additional Characteristics	5ppm/Volt Line Regulation, 500mV Dropout, Shutdown Pin, I _{SUPPLY} = 5mA, V _{IN} = V _O + 0.5V to 13.2V _{MAX} , I _{OUT(SINK/SOURCE)} = ±5mA, I _{SHORT Circuit} = 15mA.

Figure 1. LTC6655 Accuracy and Temperature Coefficient Are Characteristic of High Grade, Low Voltage References. 0.1Hz to 10Hz Noise, Particularly Noteworthy, Is Unequalled by Any Low Voltage Electronic Reference

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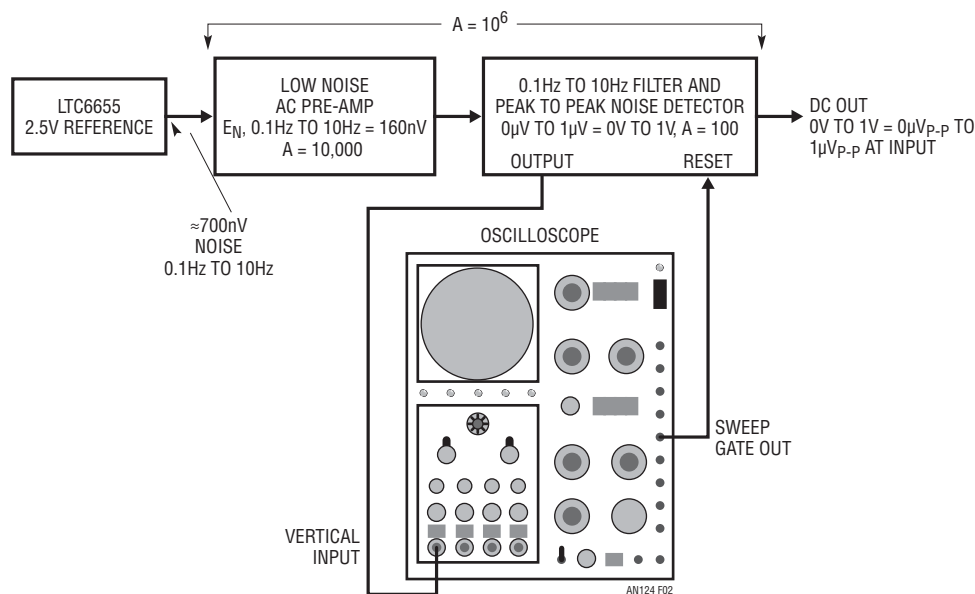


Figure 2. Conceptual 0.1Hz to 10Hz Noise Testing Scheme Includes Low Noise Pre-Amplifier, Filter and Peak to Peak Noise Detector. Pre-Amplifier's 160nV Noise Floor, Enabling Accurate Measurement, Requires Special Design and Layout Techniques

Numerous details contribute to the circuit's performance. The 1300 μ F capacitor, a highly specialized type, is selected for leakage in accordance with the procedure given in Appendix B. Further, it, and its associated low noise 1.2k resistor, are fully shielded against pick-up. FETs Q1 and Q2 differentially feed A2, forming a simple low noise op amp. Feedback, provided by the 100k - 10 Ω pair, sets closed loop gain at 10,000. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1 corrects these deficiencies by adjusting Q1's channel current via Q3 to minimize the Q1-Q2 input difference. Q1's skewed drain values ensure that A1 is able to capture the offset. A1 and Q3 supply whatever current is required into Q1's channel to force offset within about 30 μ V. The FETs' V_{GS} can vary over a 4:1 range. Because of this, they must be selected for 10% V_{GS} matching. This matching allows A1 to capture the offset without introducing significant noise. Q1 and Q2 are thermally mated and lagged in epoxy at a time constant much greater than A1's DC stabilizing loop roll-off, preventing offset instability and hunting. The entire A1-Q1-Q2-A2 assembly and the reference under test are completely enclosed within a shielded can.¹ The reference is powered by a 9V battery to minimize noise and insure freedom from ground loops.

Peak-to-peak detector design considerations include J-FET's used as peak trapping diodes to obtain lower leakage than

afforded by conventional diodes. Diodes at the FET gates clamp reverse voltage, further minimizing leakage.² The peak storage capacitors highly asymmetric charge-discharge profile necessitates the low dielectric absorption polypropylene capacitors specified.³ Oscilloscope connections via galvanically isolated links prevent ground loop induced corruption. The oscilloscope input signal is supplied by an isolated probe; the sweep gate output is interfaced with an isolation pulse transformer. Details appear in Appendix C.

Noise Measurement Circuit Performance

Circuit performance must be characterized prior to measuring LTC6655 noise. The pre-amplifier stage is verified for >10Hz bandwidth by applying a 1 μ V step at its input (reference disconnected) and monitoring A2's output. Figure 4's 10ms risetime indicates 35Hz response, insuring the entire 0.1Hz to 10Hz noise spectrum is supplied to the succeeding filter stage.

Note 1. The pre-amplifier structure must be carefully prepared. See Appendix A, "Mechanical and Layout Considerations", for detail on pre-amplifier construction.

Note 2. Diode connected J-FET's superior leakage derives from their extremely small area gate-channel junction. In general, J-FET's leak a few picoamperes (25°C) while common signal diodes (e.g. 1N4148) are about 1,000X worse (units of nanoamperes at 25°C).

Note 3. Teflon and polystyrene dielectrics are even better but the Real World intrudes. Teflon is expensive and excessively large at 1 μ F. Analog types mourn the imminent passing of the polystyrene era as the sole manufacturer of polystyrene film has ceased production.

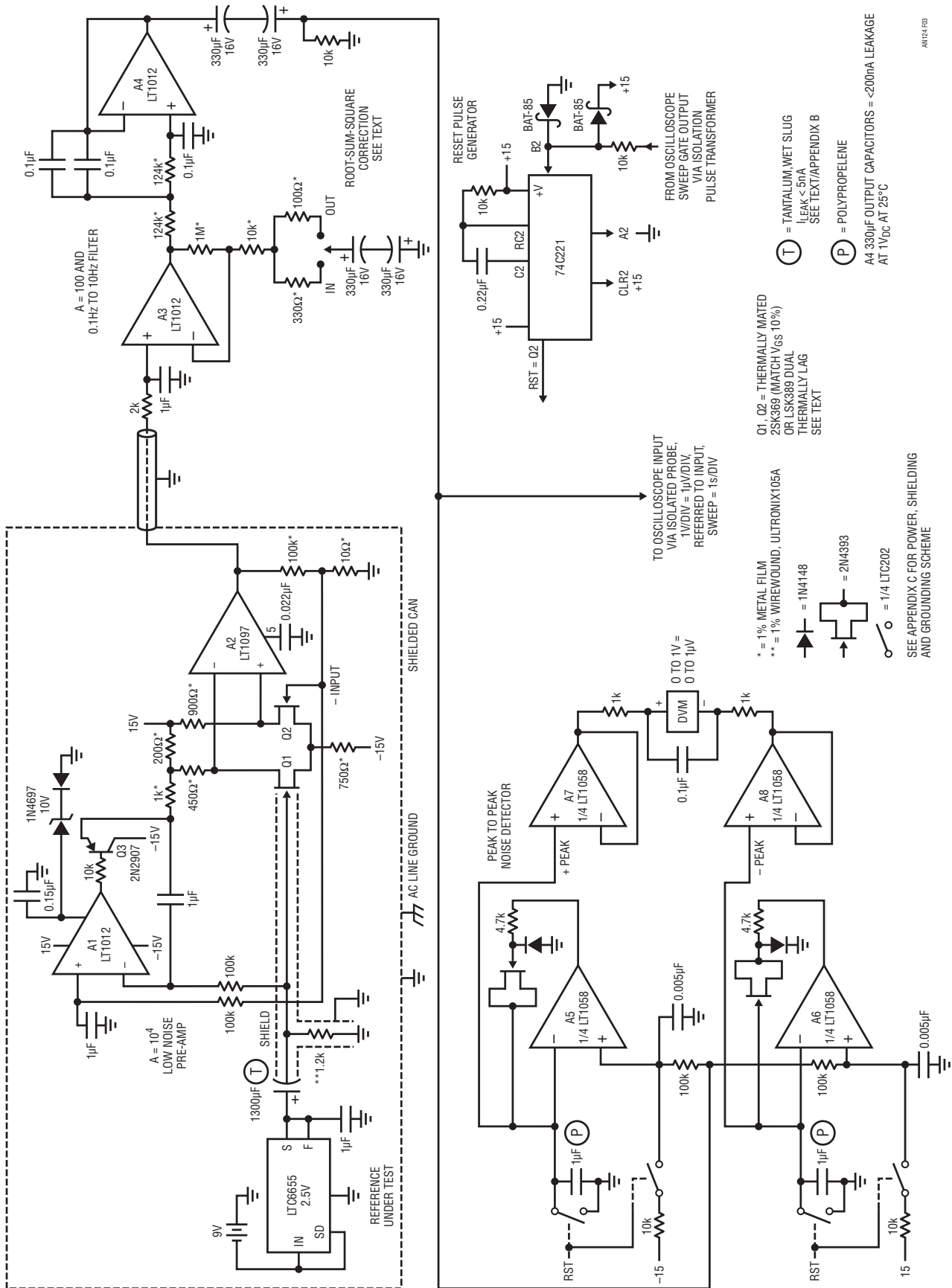


Figure 3. Detailed Noise Test Circuitry. Thermally Lagged Q1-Q2 Low Noise J-FET Pair is DC Stabilized by A1-Q3; A2 Delivers A = 10,000 Pre-Amplifier Output. A3-A4 form 0.1Hz to 10Hz, A = 100, Bandpass Filter; Total Gain Referred to Pre-Amplifier Input is 10⁶. Peak to Peak Noise Referred to Pre-Amplifier Input is 10⁶.

Application Note 124

Figure 5 describes peak-to-peak noise detector operation. Waveforms include A3's input noise signal (Trace A), A7 (Trace B) positive/A8 (Trace C) negative peak detector outputs and DVM differential input (Trace D). Trace E's oscilloscope supplied reset pulse has been lengthened for photographic clarity.

Circuit noise floor is measured by replacing the LTC6655 with a 3V battery stack. Dielectric absorption effects in the large input capacitor require a 24-hour settling period before measurement. Figure 6, taken at the circuit's oscilloscope output, shows 160nV 0.1Hz to 10Hz noise in a 10 second sample window. Because noise adds in root-sum-square fashion, this represents about a 2% error in

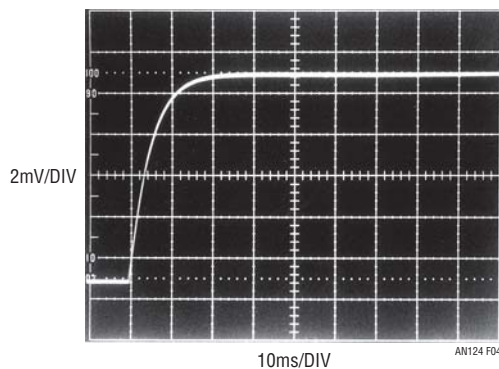


Figure 4. Pre-Amplifier Rise Time Measures 10ms; Indicated 35Hz Bandwidth Ensures Entire 0.1Hz to 10Hz Noise Spectrum Is Supplied to Succeeding Filter Stage

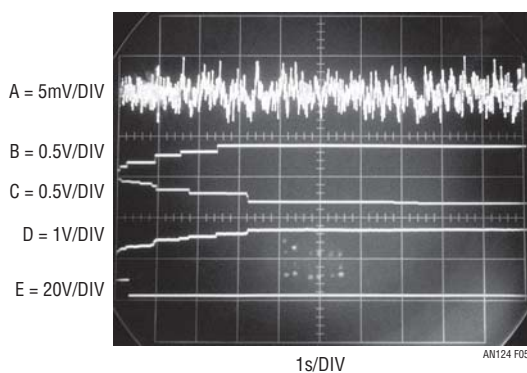


Figure 5. Waveforms for Peak to Peak Noise Detector Include A3 Input Noise Signal (Trace A), A7 (Trace B) Positive/A8 (Trace C) Negative Peak Detector Outputs and DVM Differential Input (Trace D). Trace E's Oscilloscope Supplied Reset Pulse Lengthened for Photographic Clarity

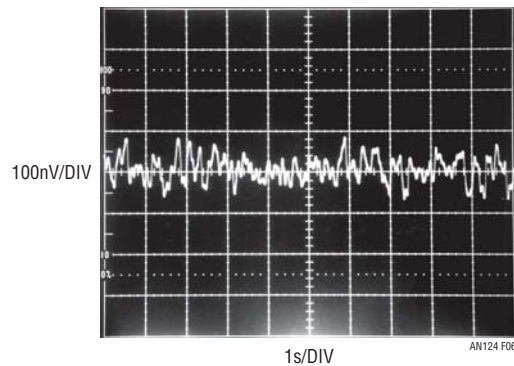


Figure 6. Low Noise Circuit/Layout Techniques Yield 160nV 0.1Hz to 10Hz Noise Floor, Ensuring Accurate Measurement. Photograph Taken at Figure 3's Oscilloscope Output with 3V Battery Replacing LTC6655 Reference. Noise Floor Adds \approx 2% Error to Expected LTC6655 Noise Figure Due to Root-Sum-Square Noise Addition Characteristic; Correction is Implemented at Figure 3's A3

the LTC 6655's expected 775nV noise figure. This term is accounted for by placing Figure 3's "root-sum-square correction" switch in the appropriate position during reference testing. The resultant 2% gain attenuation first order corrects LTC6655 output noise reading for the circuit's 160nV noise floor contribution. Figure 7, a strip-chart recording of the peak-to-peak noise detector output over 6 minutes, shows less than 160nV test circuit noise.⁴ Resets occur every 10 seconds. A 3V battery biases the input capacitor, replacing the LTC6655 for this test.

Figure 8 is LTC6655 noise after the indicated 24-hour dielectric absorption soak time. Noise is within 775nV peak-to-peak in this 10 second sample window with the root-sum-square correction enabled. The verified, extremely low circuit noise floor makes it highly likely this data is valid. In closing, it is worth mention that the approach taken is applicable to measuring any 0.1Hz to 10Hz noise source, although the root-sum-square error correction coefficient should be re-established for any given noise level.

Note 4. That's right, a *strip-chart recording*. Stubborn, locally based aberrants persist in their use of such archaic devices, forsaking more modern alternatives. Technical advantage could account for this choice, although deeply seated cultural bias may be indicated.

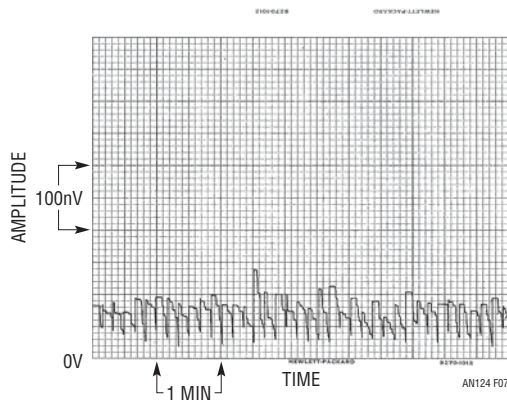


Figure 7. Peak to Peak Noise Detector Output Observed Over 6 Minutes Shows <160nV Test Circuit Noise. Resets Occur Every 10 seconds. 3V Battery Biases Input Capacitor, Replacing LTC6655 for This Test

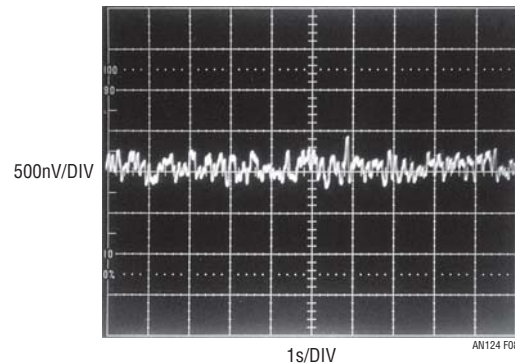


Figure 8. LTC6655 0.1Hz to 10Hz Noise Measures 775nV in 10 Second Sample Time

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Application Note 124

APPENDIX A

Mechanical and Layout Considerations

The low noise X10,000 preamplifier, crucial to the noise measurement, must be quite carefully prepared. Figure A1 shows board layout. The board is enclosed within a shielded can, visible in A1A. Additional shielding is provided to the input capacitor and resistor (A1A left); the resistor's wirewound construction has low noise but is particularly susceptible to stray fields. A1A also shows the socketed LTC6655 reference under test (below the large input capacitor shield) and the JFET input amplifier associated components. Q3 (A1A upper right), a heat source, is located away from the JFET printed circuit lands,

preventing convection currents from introducing noise. Additionally, the JFET's are contained within an epoxy filled plastic cup (Figure A1B center), promoting thermal mating and lag.¹ This thermal management of the FETs prevents offset instability and hunting in A1's stabilizing loop from masquerading as low frequency noise. $\pm 15V$ power enters the enclosure via banana jacks; the reference is supplied by a 9V battery (both visible in A1A). The A = 100 filter and peak-peak detector circuitry occupies a separate board outside the shielded can. No special commentary applies to this section although board leakage to the peak detecting capacitors should be minimized with guard rings or flying lead/Teflon stand-off construction.

Note 1. The plastic cup, supplied by Martinelli and Company, also includes, at no charge, 10 ounces of apple juice.

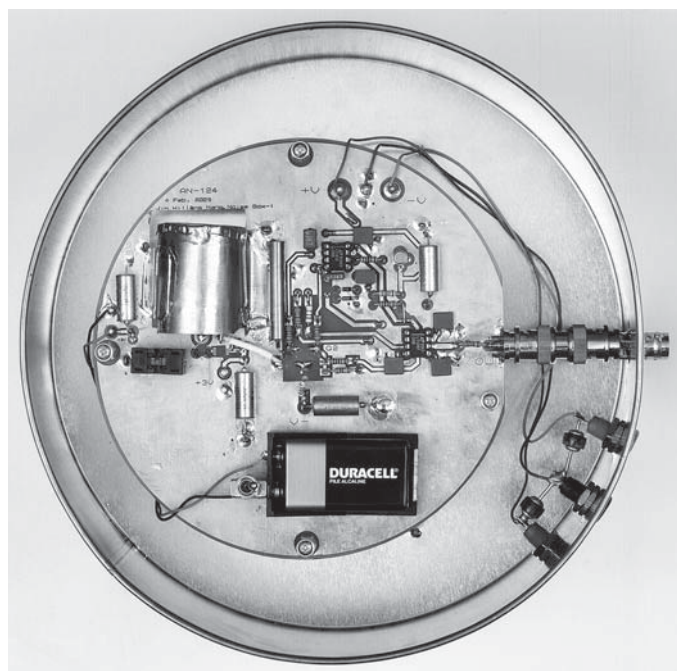


Figure A1A.

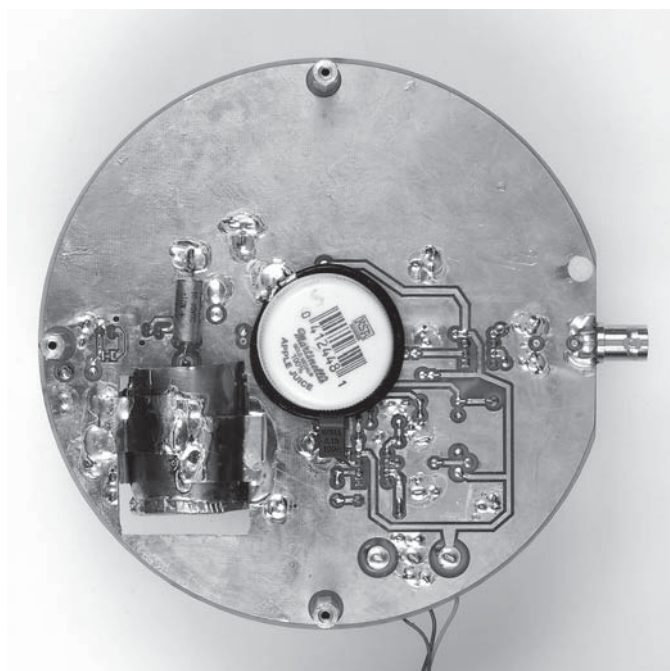


Figure A1B.

Figure A1. Preamplifier Board Top (Figure A1A) and Bottom (A1B) Views. Board Top Includes Shielded Input Capacitor (Upper Left) and Input Resistor (Upper Center Left). Stabilized JFET Input Amplifier Occupies Board Upper Center Right; Output Stage Adjoins BNC Fitting. Reference Under Test Resides in Socket Below Input Capacitor. $\pm 15V$ Power Enters Shielded Enclosure Via Banana Jacks (Extreme Right). 9V Battery (Lower) Supplies Reference Under Test. Board Bottom's Epoxy Filled Plastic Cup (A1B Center) Contains JFETs, Provides Thermal Mating and Lag

APPENDIX B

Input Capacitor Selection Procedure

The input capacitor, a highly specialized type, must be selected for leakage. If this is not done, resultant errors can saturate the input pre-amplifier or introduce noise. The highest grade wet slug 200°C rated tantalum capacitors are utilized. The capacitor operates at a small fraction of its rated voltage at room temperature, resulting in much lower leakage than its specification indicates.

The capacitor's dielectric absorption requires a 24-hour charge time to insure meaningful measurement. Capacitor leakage is determined by following the 5-step procedure given in the figure. Yield to required 5-nanoampere leakage exceeds 90%.¹

Note 1. This high yield is most welcome because the specified capacitors are spectacularly priced at almost \$400.00. There may be a more palatable alternative. Selected commercial grade aluminum electrolytics can approach the required DC leakage although their aperiodic noise bursts (mechanism not understood; reader comments invited) are a concern.

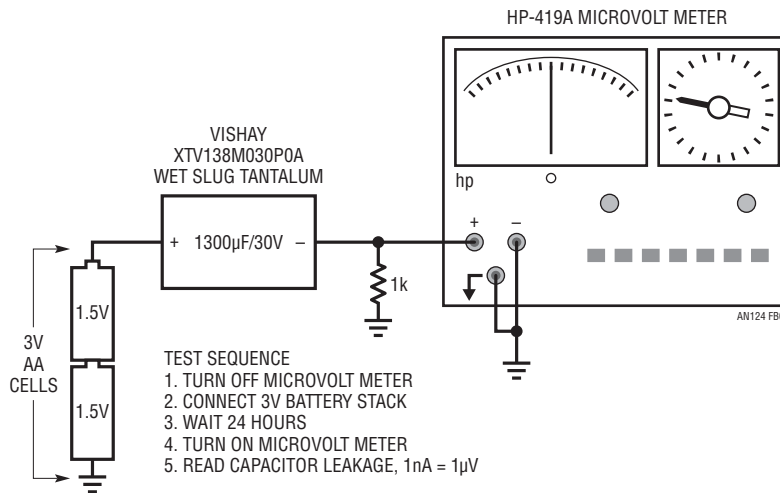


Figure B1. Pre-Amplifier Input Capacitor Selected for <5nA Leakage to Minimize DC Error and Capacitor Introduced Noise. Capacitor Dielectric Absorption Requires 24 Hour Charge Time to Insure Meaningful Measurement. Highest Grade Wet Slug Tantalum Capacitors are Required to Pass This Test

Application Note 124

APPENDIX C

Power, Grounding and Shielding Considerations

Figure 3's circuit requires great care in power distribution, grounding and shielding to achieve the reported results. Figure C1 depicts an appropriate scheme. A low shunt capacitance line isolation transformer powers an instrument grade $\pm 15V$ supply, furnishing clean, low noise power. The pre-amplifier's shielded can is tied to the 110V AC ground terminal, directing pick-up to earth ground. Filter/peak-to-peak detector oscilloscope connections are made via an isolated probe and a pulse isolation transformer, precluding error inducing ground loops.¹ The indicated loop, included to verify no current flow between circuit common and earth ground, is monitored with a current probe. Figures C2 and C3, both optional, show battery powered supplies which replace the line isolation transformer and instrumentation

grade power supplies. C2 uses linear regulators to furnish low noise $\pm 15V$. Because the batteries float, positive regulators suffice for both positive and negative rails. In C3, a single battery stack supplies an extremely low noise DC-DC converter to furnish positive and negative rails via low noise discrete linear regulators.² Both of these battery supplied approaches are economical compared to the AC line powered version but require battery maintenance.

The indicated commercial products accompanying Figure C1's blocks represent typical applicable units which have been found to satisfy requirements. Other types may be employed but should be verified for necessary performance.

Note 1. An acceptable alternative to the isolated probe is monitoring Figure 3's A4 output current into a grounded 1k resistor with a DC stabilized current probe (e.g. Tektronix P6042, AM503). The resultant isolated $1V/\mu V$ oscilloscope presentation requires 10Hz lowpass filtering (see Appendix D) due to inherent current probe noise.

Note 2. References 6 and 8 detail the specialized DC-DC converter used.

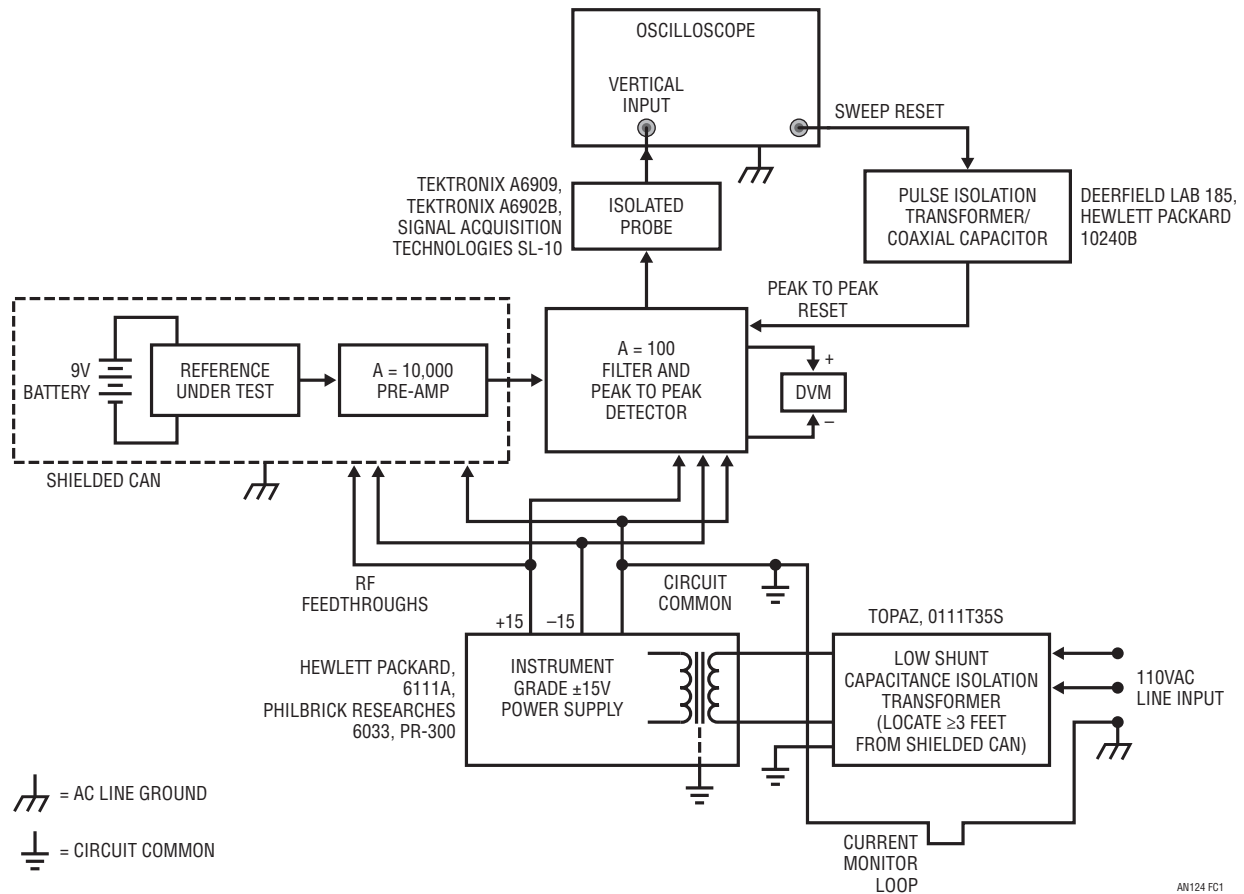


Figure C1. Power/Grounding/Shielding Scheme for Low Noise Measurement Minimizes AC Line Originated Interference and Mixing of Circuit Return and AC Line Ground Current. No Current Should Flow in Current Monitor Loop

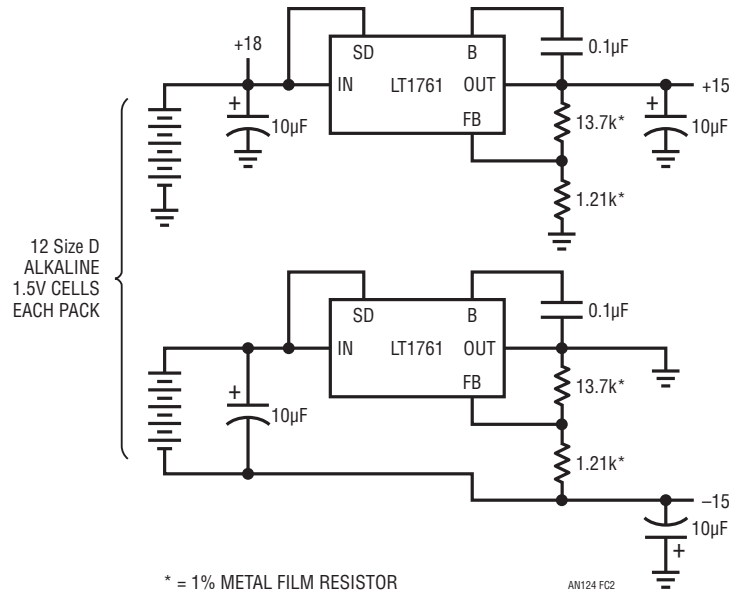


Figure C2. LT1761 Regulators form $\pm 15V$, Low Noise Power Supply. Isolated Battery Packs Permit Positive Regulator to Supply Negative Output and Eliminate Possible AC Line Referred Ground Loops

Application Note 124

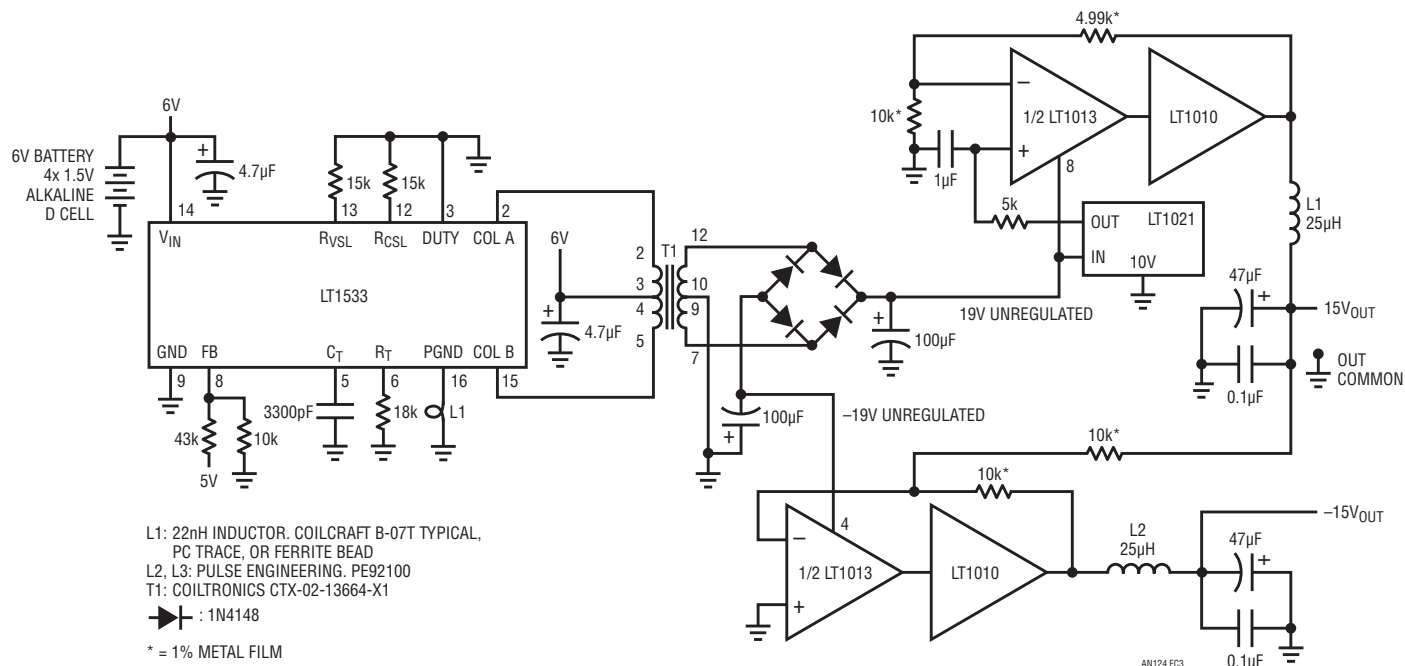


Figure C3. A Low Noise, Bipolar, Floating Output Converter. Grounding LT1533 “DUTY” Pin and Biasing FB Puts Regulator into 50% Duty Cycle Mode. LT1533’s Controlled Transition Times Permit <100µV Broadband Output Noise; Discrete Linear Regulators Maintain Low Noise, Provide Regulation

APPENDIX D

High Sensitivity, Low Noise Amplifiers

Figure D1 lists some useful low level amplifiers for setting up and troubleshooting the texts' circuit. The table lists both oscilloscope plug-in amplifiers and stand-alone types. Two major restrictions apply. The filters in these units

are single-pole types resulting in somewhat pessimistic bandwidth cut-offs. Additionally, the amplifiers listed do not include 10Hz lowpass frequency filters, although they are easily modified to provide this capability. Figure D2 lists four amplifiers with the necessary modification information.¹

Note 1. See References 14-17.

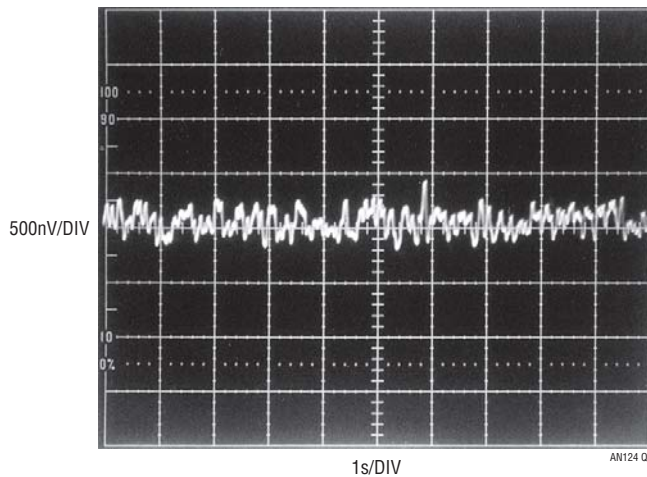
INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	-3dB BANDWIDTH	MAXIMUM SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Differential Amplifier	Tektronix	1A7/1A7A	1MHz	10 μ V/DIV	Secondary Market	Requires 500 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	7A22	1MHz	10 μ V/DIV	Secondary Market	Requires 7000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	5A22	1MHz	10 μ V/DIV	Secondary Market	Requires 5000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	ADA-400A	1MHz	10 μ V/DIV	Current Production	Stand-Alone with Optional Power Supply, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 1000	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Stanford Research Systems	SR-560	1MHz	Gain = 50000	Current Production	Stand-Alone, Settable Bandstops, Battery or Line Operation
Differential Amplifier	Tektronix	AM-502	1MHz	Gain = 100000	Secondary Market	Requires TM-500 Series Power Supply, Settable Bandstops

Figure D1. Some Useful High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Bandwidth, Sensitivity and Availability

MANUFACTURER	MODEL NUMBER	MODIFICATION
Tektronix	1A7	Parallel C370A with 1 μ F
Tektronix	1A7A	Parallel C445A with 1 μ F
Tektronix	7A22	Parallel C426H with 3 μ F
Tektronix	AM502	Parallel C449 with 3 μ F

Figure D2. Modification Information for Various Tektronix Low Level Oscilloscope Plug-In's and Amplifiers Permits 10Hz High Frequency Filter Operation in 100Hz Panel Switch Position. All Cases Utilize 100V, Mylar Capacitors

Application Note 124



“...Singeth a quiet tune.”

Samuel Coleridge

– The Ancient Mariner

1798

2-Wire Virtual Remote Sensing for Voltage Regulators

Clairvoyance Marries Remote Sensing

Jim Williams, Jesus Rosales, Kurk Mathews, Tom Hack

Introduction

Wires and connectors have resistance. This simple, unavoidable truth dictates that a power source's remote load voltage will be less than the source's output voltage. Figure 1 shows this, and implies that intended load voltage can be maintained by raising regulator output. Unfortunately, line resistance and load variations introduce uncertainties, limiting achievable performance.

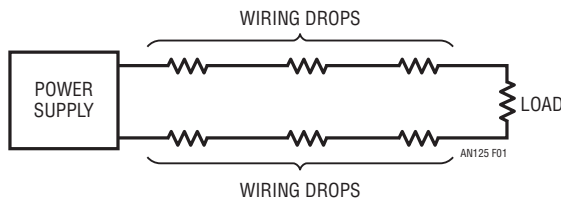


Figure 1. Unavoidable Wiring Drops Cause Low Load Voltage. Line and Load Resistance Variations Introduce Additional Load Voltage Uncertainty, Mitigating Against Compensation by Raising Supply Voltage

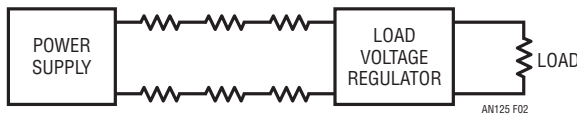


Figure 2. Local Regulation Stabilizes Load Voltage But is Inefficient

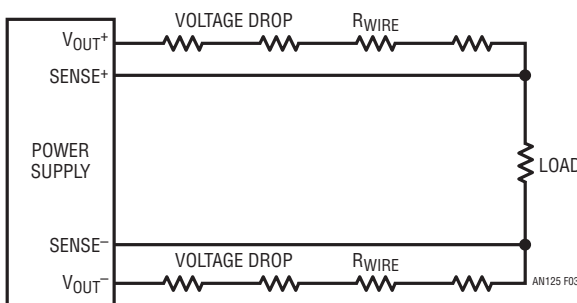


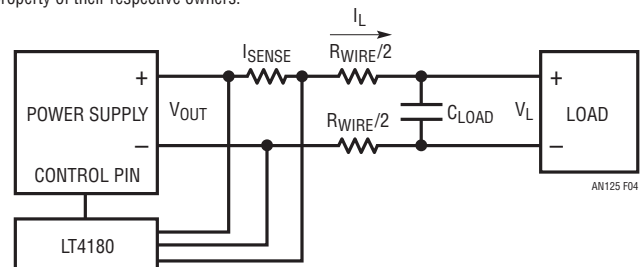
Figure 3. Classical "4-Wire" Remote Sensing. V_{OUT} Line Voltage Drops Are Compensated by Regulator Sensing at Load. High Impedance Sense Inputs Negate Sense Wire Resistance. Approach Requires Four Wires

Figure 2 illustrates one compensatory approach. Locally positioned regulation stabilizes load voltage against line drops but is inefficient due to regulator losses. Figure 3, the classical approach, utilizes "4-wire" remote sensing to eliminate line drop effects. The power supply sense inputs are fed from load referred sense wires. The sense inputs are high impedance, negating sense line resistance effects. This scheme works well, but requires dedicated sense wires, a significant disadvantage in many applications.

"Virtual" Remote Sensing

Figure 4 retains the advantages of classical 4-wire remote sensing while eliminating the sense leads. Here, the LT4180 Virtual Remote Sense™ (VRS) IC alternates output current between 95% and 105% of the nominal required output current. The LT4180 forces the power supply to provide a DC current plus a small square wave current with peak-to-peak amplitude equal to 10% of the DC current. Decoupling capacitor C_{LOAD} , normally required for low impedance under transient conditions in non-VRS systems, takes an additional role by filtering out the VRS square wave excursions.

LT, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks and Virtual Remote Sense is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.



$V_{OUT} = DC + \text{SQUAREWAVE FROM WIRING VOLTAGE DROP}$
 C_{LOAD} REMOVES SQUAREWAVE, SO V_L CONTAINS ONLY DC.
 $I_L = DC + \text{SQUAREWAVE}$

Figure 4. LT4180 2-Wire Virtual Remote Sense Estimates Wiring Voltage Drops, Compensates by Adjusting Supply Output Voltage. Wiring Loss Is Determined by Measuring Small Signal Square Wave Carrier Induced Voltage Drop. Load Capacitor Absorbs Square Wave; Load Is at DC

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Application Note 126

Because C is sized to produce an “AC short” at the square wave frequency, a square wave voltage is produced at the power supply equal to $V_{OUTAC} = 0.1 \cdot I_{DC} \cdot R_{WIRE} V_{P-P}$. The square wave voltage at the power supply has a peak-to-peak amplitude equal to one tenth the DC wiring drop. This is a direct measurement of wiring drop, not an estimate, accurate over all load currents. Signal processing produces a DC voltage from this AC signal which is introduced into the supply feedback loop to provide accurate load regulation¹. Note that the “power supply” may be an IC linear or switching regulator, a module or any other power source capable of variable output. Power supplies can be synchronized to the LT4180 and VRS operating frequency is adjustable over more than three decades. Optional spread spectrum operation provides partial immunity from single-tone interference and a 3V to 50V input range simplifies design. Because this technique is based on an estimate of load voltage, not a direct measurement, the resultant correction is an approximation, but a very good one.

Typical LT4180 load regulation is plotted in Figure 5. In this example, load current increases from zero until it produces a 2.5V wiring drop. Load voltage drops only 73mV at maximum current. A voltage drop equivalent to 50% of load voltage results in only a 1.5% shift in load voltage value. Smaller wiring drops produce even better results.

Note 1. Readers finding their intellectual prowess unsatiated by this admittedly cursory description will find more studious coverage in Appendix A, “A Primer on LT4180 VRS Operation.”

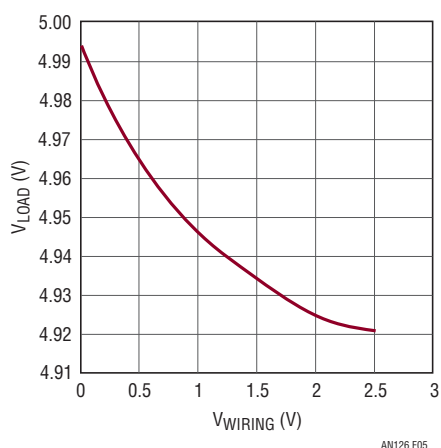


Figure 5. Typical LT4180 Virtual Remote Sense Performance Shows 1.6% Regulation vs 0V → 2.5V Wiring Drop

Applications

The following applications are all VRS augmented voltage regulators of various descriptions. The power regulation stages employed are, with one exception, generic LTC designs and are spared exhaustive commentary, permitting emphasis on the LT4180 VRS role. Additionally, the similarity of the VRS associated circuitry across the broad array of applications shown should be noted, and is indicative of the relative ease of implementation. Surprisingly little change is needed to use the VRS in the different situations presented.

VRS Linear Regulators

Figure 6 adds a simple stage to the LT4180 to implement a complete VRS aided linear regulator. The LT4180 senses current via the 0.2Ω shunt and feedback controls Q1 with Q2, completing a control loop. Cascoded Q2 permits the IC's 5V capable open drain output to control a high voltage at Q1's gate. Components at the compensation pin furnish loop stability, promoting good transient response². Figure 7 shows Figure 6's load step waveforms. They include V_{SENSE} (trace A), V_{LOAD} (B) and I_{LOAD} (C). Transient response is determined by loop compensation, load capacitance and remote sense sample rate. Figure 8 shows response with C_{LOAD} increased to $1100\mu F$. Load voltage transient excursion reduces and duration increases.

Figure 9, employing a monolithic regulator, adds current limiting and simplifies loop compensation. Transient response approximates Figure 6's. As before, the LT4180's low voltage drain pin requires a cascode transistor to control the high voltage at the LT3080 set pin.

Note 2. Value selection procedure for LT4180 VRS circuits is detailed in Appendix B, “Design Guidelines for LT4180 VRS Circuits.”

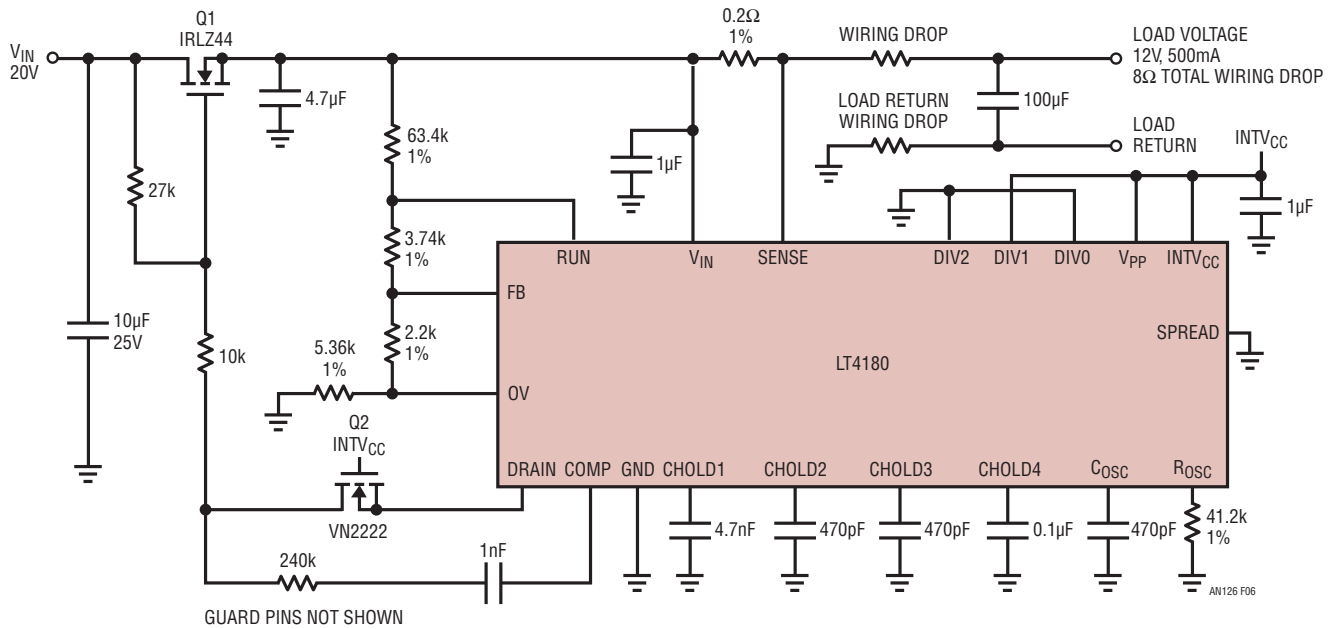


Figure 6. Virtual Remote Sense Controls Discrete Linear Regulator. Q2 Cascodes Drain Output, Buffering High Voltage Q1 Gate Drive. COMP Pin Associated Components Stabilize Loop

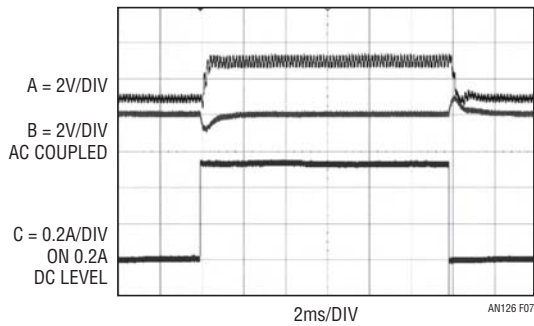


Figure 7. Figure 6's Load Step Waveforms with 100µF Load Capacitor Include V_{SENSE} (Trace A), V_{LOAD} (B) and I_{LOAD} (C). Transient Response is Determined by Loop Compensation, Load Capacitance and Remote Sense Sample Rate

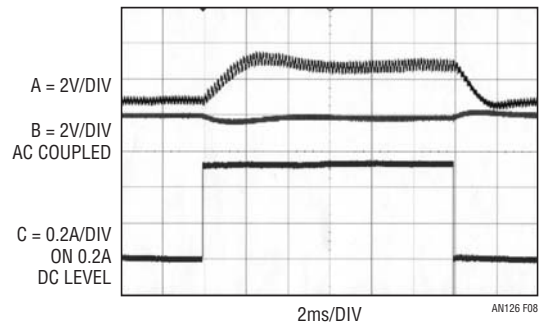


Figure 8. Same Conditions as Figure 7 with C_{LOAD} Increased to 1100µF. V_{LOAD} Transient Excursion Reduces, Duration Extends

Application Note 126

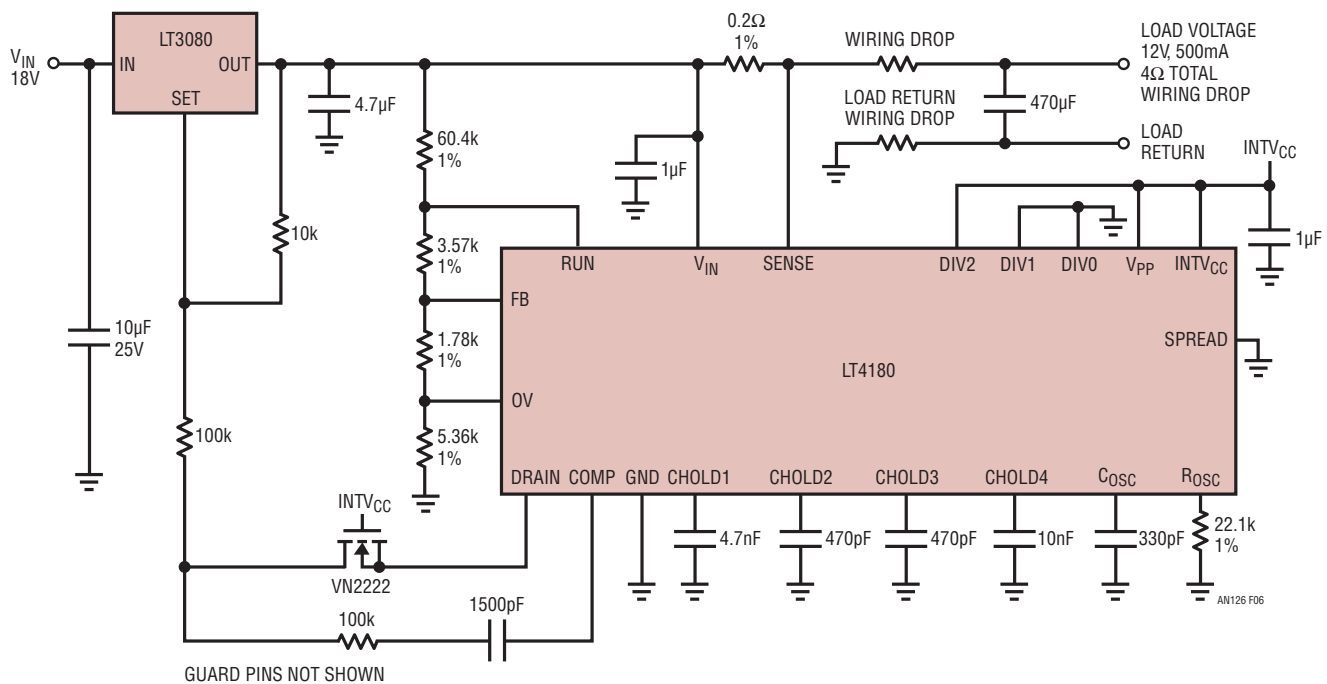


Figure 9. Figure 6's Approach Utilizing IC Regulator Adds Current Limiting, Simplifies Loop Compensation. Transient Response Approximates Figure 6's

VRS Equipped Switching Regulators

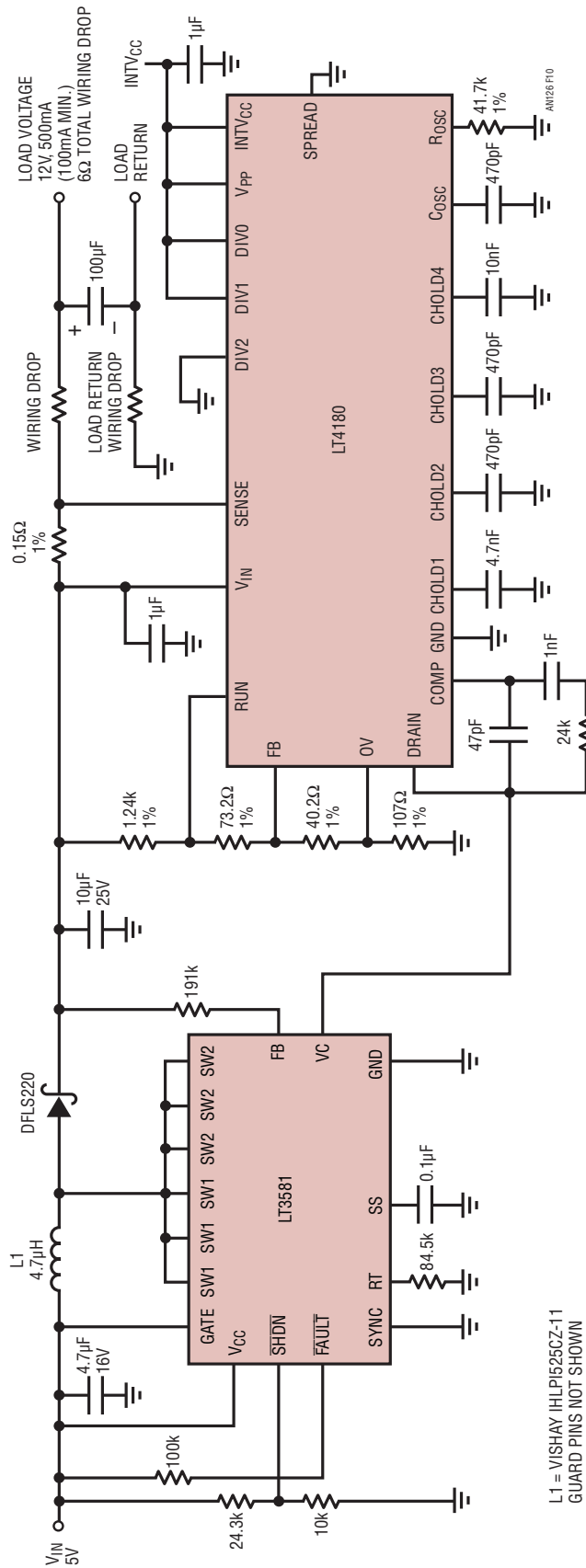
VRS based switching regulators are readily constructed. Figure 10's flyback voltage boost configuration has similar architecture to the linear examples although output voltage is above the input. In this case, the LT4180 open drain output is directly compatible with the LT3581 boost regulator low voltage V_C pin—no cascode stage is necessary.

Step down ("Buck") VRS equipped switching regulators are similarly easily achieved. Figure 11's scheme, reminiscent of the previously described linear regulators, substitutes an LT3685 step down regulator which is directly controlled from the LT4180 open drain output. A single pole roll-off stabilizes the loop and a 12V, 1.5A output is maintained from a 22V to 36V input despite a 0Ω to 2.5Ω wiring drop loss. Figure 11A is similar, except that it provides a 5V, 3A output from a 12V to 36V input.

VRS Based Isolated Switching Supplies

The VRS approach is adaptable to isolated output supplies. Figure 12's 24V output converter utilizes an approach similar to the previous examples except that it supplies a fully isolated output. The virtual remote sense feature accommodates a 10Ω wire resistance. The LT3825 and T1 form a transformer coupled power stage. Opto-coupled feedback maintains output isolation.

Figure 13's 48V → 3.3V, 3A design also has a fully isolated output, facilitated by power delivery through a transformer and optically coupled feedback loop closure. The LT3758 drives T1 via Q1. T1's rectified and filtered secondary supplies output power which is corrected for line drops by the LT4180. Isolation is maintained by transmitting the feedback signal with an opto-isolator. The opto-isolators output collector ties back to the LT3578 V_C pin, closing the control loop.



**Figure 10. Virtual Remote Sensed Voltage Boost Configuration.
LT4180 Drain Output Controls Flyback Regulator via LT3581 V_C Pin**

L1 = VISHAY HPLP1525CZ-11
GUARD PINS NOT SHOWN

Application Note 126

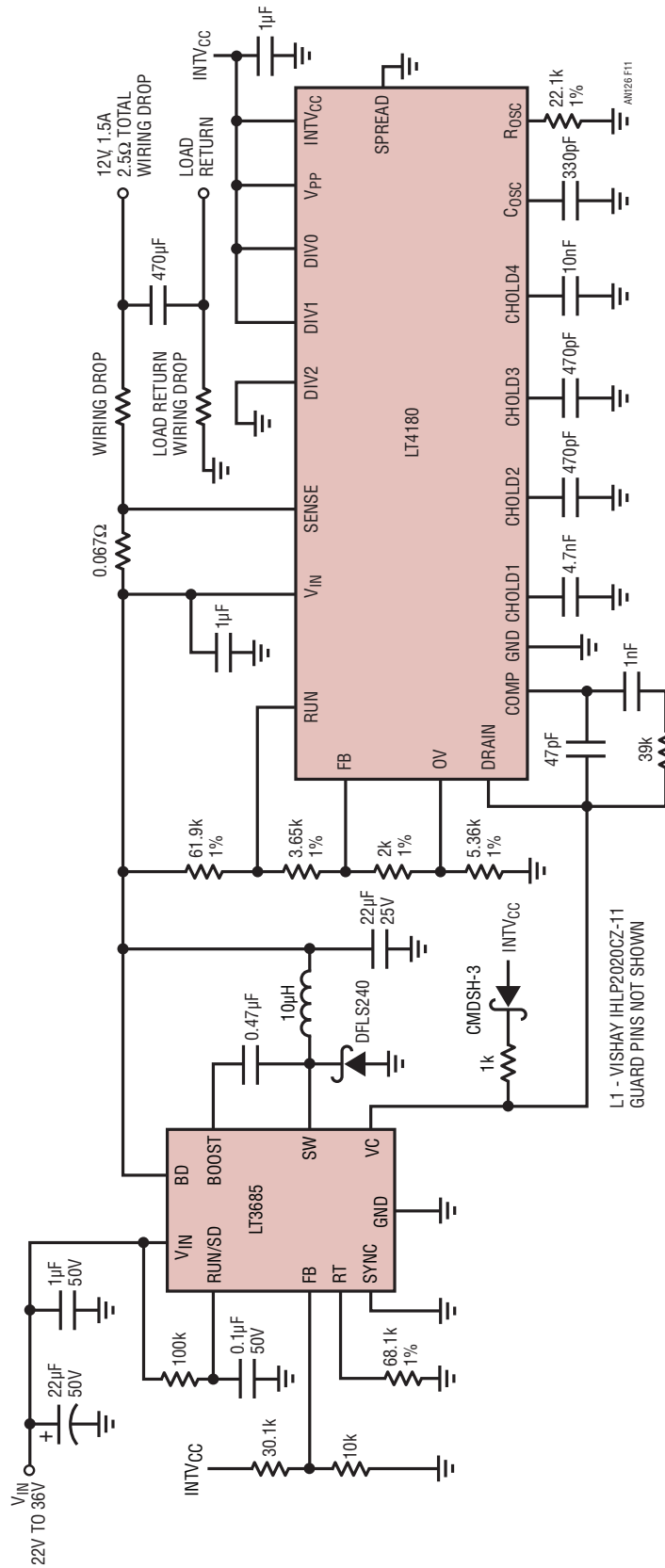


Figure 11 . Remote Sense Corrected 22V_{IN} to 36V_{IN} Step-Down Regulator Maintains 12V Output Despite Wiring Losses

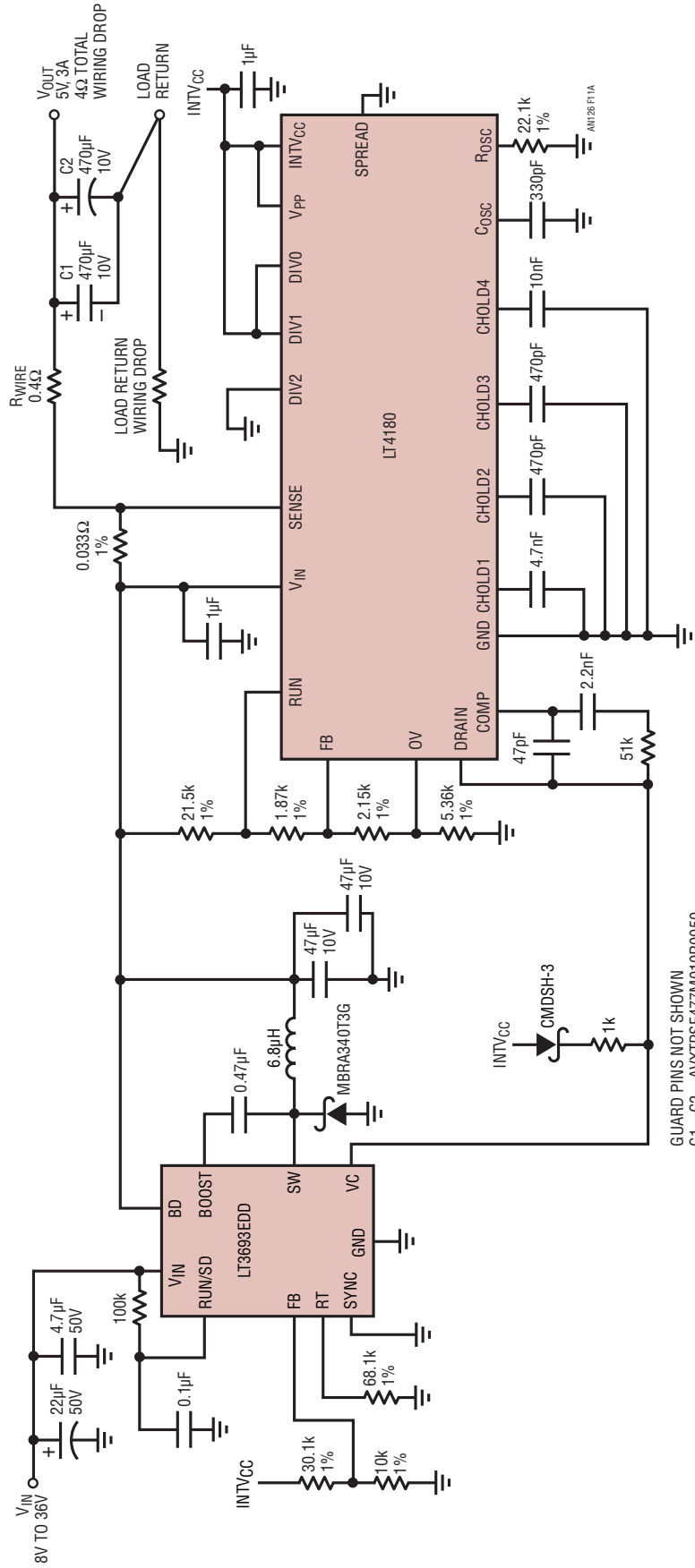
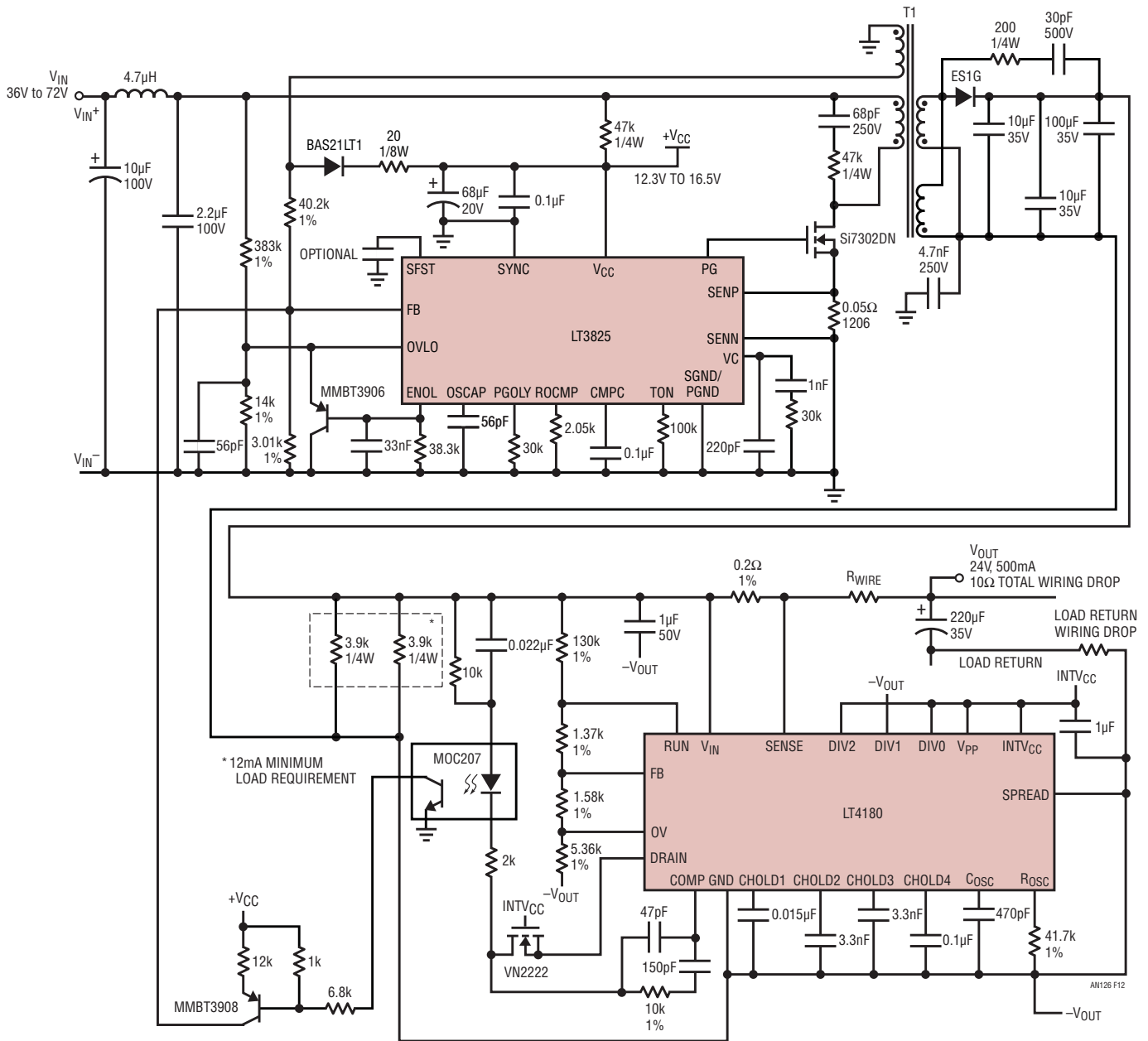


Figure 11A. 12V_{IN} → 36V_{IN} to 5V_{OUT} Step-Down Remote Sensed Regulator Has Similar Architecture to Figure 11

Application Note 126



- 10μF TANYO YUDEN GMK325BJ106KN 1210
- 100μF 36V NICHICON PL (M)
- 10μF 100V SANYO 100CE10FS
- 68μF 20V KEMET T491D686K020AS
- 4.7nF 250V MURATA GA343DR7GD472KW01L
- 4.7μH COOPER BUSSMANN SO3814-4R7-R
- 1/4W RESISTORS ARE 1206
- 1/8W RESISTORS ARE 0805
- T1 PULSE PA2925NL
- GUARD PINS NOT SHOWN

⊥ = INPUT COMMON

Figure 12. Virtual Remote Sensed, Isolated 36V_{IN} → 72V_{IN} to 24V_{OUT} Converter Accommodates 10Ω Lead Wire Resistance. LT3825/T1 Form Transformer Coupled Power Stage. LT4180 Provides Virtual Remote Sense, Opto-Coupled Feedback Maintains Output Isolation

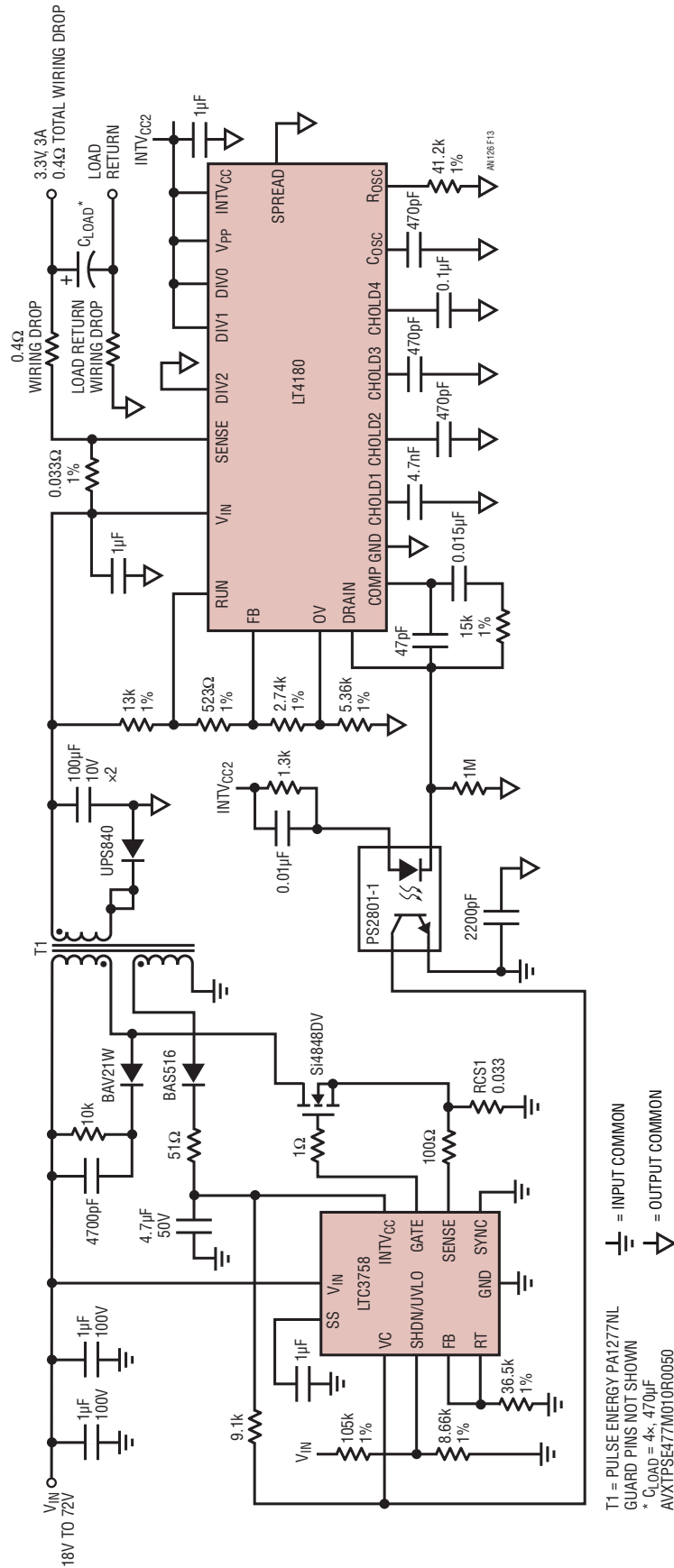


Figure 13. 48V → 3.3V Isolated Step-Down, Remote Sensed Regulator. T1 Delivers Isolated Power, LT4180 Remotely Senses Output, Supplies Feedback via Opto-Isolator

Application Note 126

Figure 14, also a VRS isolated step-down supply, uses a commercially produced 48V isolated input module augmented with virtual remote sensing. The module sense terminals are unused. The LT4180 wiring drop correction is introduced at the module trim pin. Component values are shown for 3.3 and 5V outputs. The “black box” Vicor module trim pin transient response defines available control bandwidth. Figure 15, trace A, is the trim pin input step (see test circuit A), trace B, the module output. The trim pin directed dynamics set practical expectations for VRS equipped loop response around the module. Figures 16 and 17 do not disappoint. Figure 14’s load step response appears in Figure 16. Trace A is load step current, trace B, the resultant output voltage transient. The response envelope, bounded by module trim pin dynamics, is clean and well controlled. Figure 17 shows Figure 14’s turn-on into a 2.5Amp load. LT4180 activation arrests the initial abrupt rise at the 3rd vertical division. The ascent’s conclusion is controlled to the regulation point in damped fashion.

LT4180 sampling square wave residue is just discernible in the waveforms settled portion.

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, AC LINE CONNECTED POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, AC LINE CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 18’s VRS aided “Off-Line” isolated output supply has a 5V output with 2A capacity. The schematic appears complex, but inspection reveals it to be essentially an AC line powered variant of Figure 13’s isolated approach. The LT4180 provides remote sensing and closes an isolated feedback loop with optical transmission.

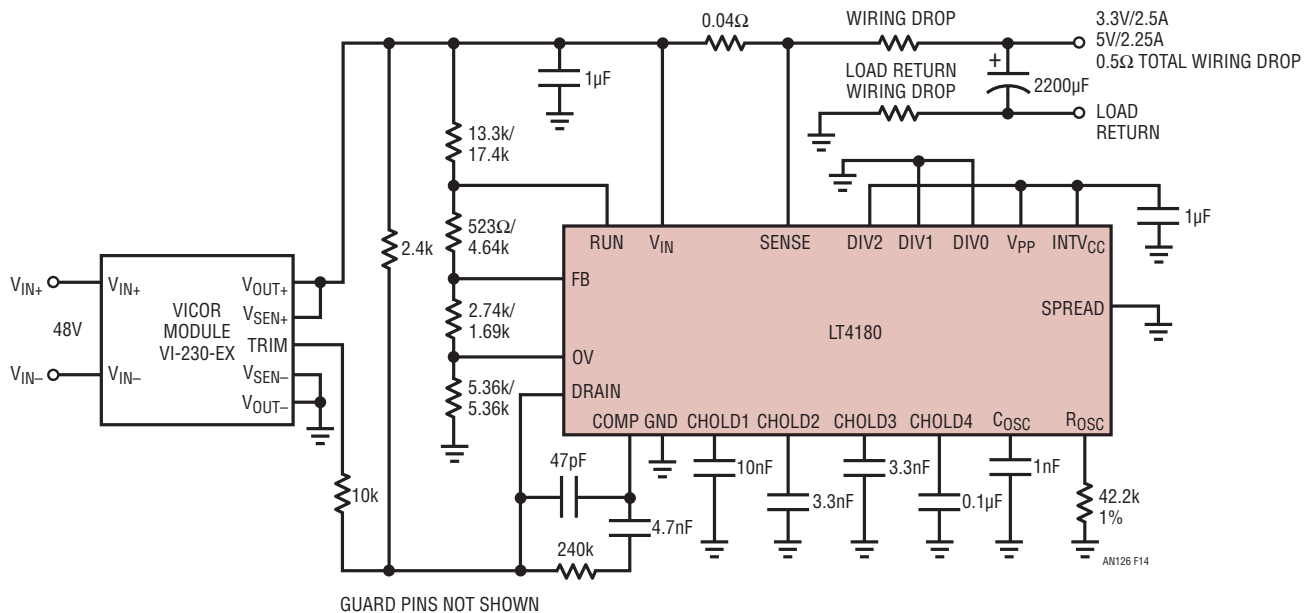


Figure 14. Commercially Produced, Isolated 48V Input Module Augmented with Virtual Remote Sense. Module Sense Terminals Are Unused. Wiring Drop Correction Introduced at Module Trim Pin. Component Values Shown for 3.3V/5V Outputs

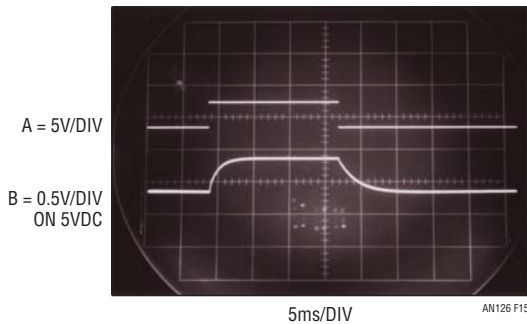
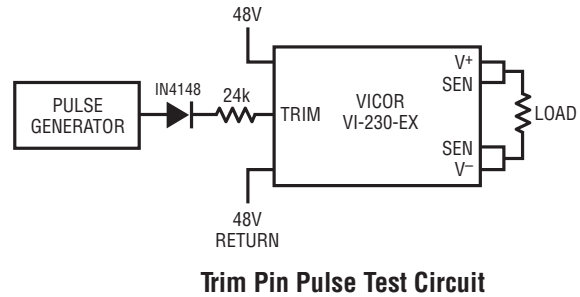


Figure 15. Vicor Module Trim Pin Transient Response Defines Available Control Bandwidth. Trace A is Trim Pin Input Step (See Test Circuit), Trace B, Module Output



Trim Pin Pulse Test Circuit

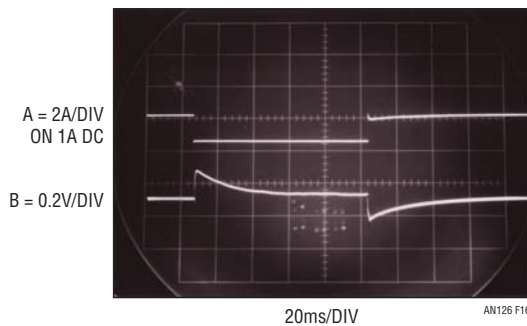


Figure 16. Figure 14's Load Step Response. Trace A is Load Step Current, Trace B Resultant Output Voltage Transient. Response Envelope, Bounded by Module Trim Pin Dynamics, is Well Controlled

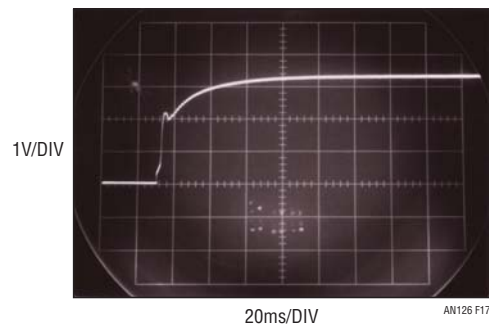


Figure 17. Figure 14's Turn-On into a 2.5A Load. LT4180 Activation Arrests Initial Abrupt Rise at Third Vertical Division. Ascent Conclusion is Controlled to Regulation Point. LT4180 Sampling Square Wave Residue is Discernible

VRS Halogen Lamp Drive Circuit

A final circuit, Figure 19, uses the VRS to stabilize drive to a halogen lamp, in this case a 12V, 30W automotive type. Lamp output power remains constant despite 9V to 15V input variation and line resistance/connection uncertainties. Additional benefits include constant color output and extended lamp life. The circuit, a step up/down ("SEPIC") converter, maintains 12V at the lamp despite the 9V to 15V input range³. The VRS functions in the manner previously described. Line resistance losses due to switches, wiring and connectors are obviated by VRS action. Figure 20 plots unaided vs remote sensed and regulated halogen lamp light output. VRS equipped luminosity is flat over the 9 to 15V input range while unregulated performance

Note 3. SEPIC operation is described in Reference 2.

suffers dramatically. The regulation also benefits lamp life by greatly reducing lamp turn-on current. Figure 21 shows unregulated lamp turn-on exceeding 20A without regulation. In Figure 22, regulation cuts current peaking to 7A, a 3x reduction. This soft turn-on and constant 12V drive under high/low line conditions optimizes illumination and improves lamp life.

References

1. LT4180 Data Sheet, Linear Technology Corporation, 2010.
2. Ridley, R. "Analyzing the Sepic Converter", Power Systems Design Europe, November, 2006.

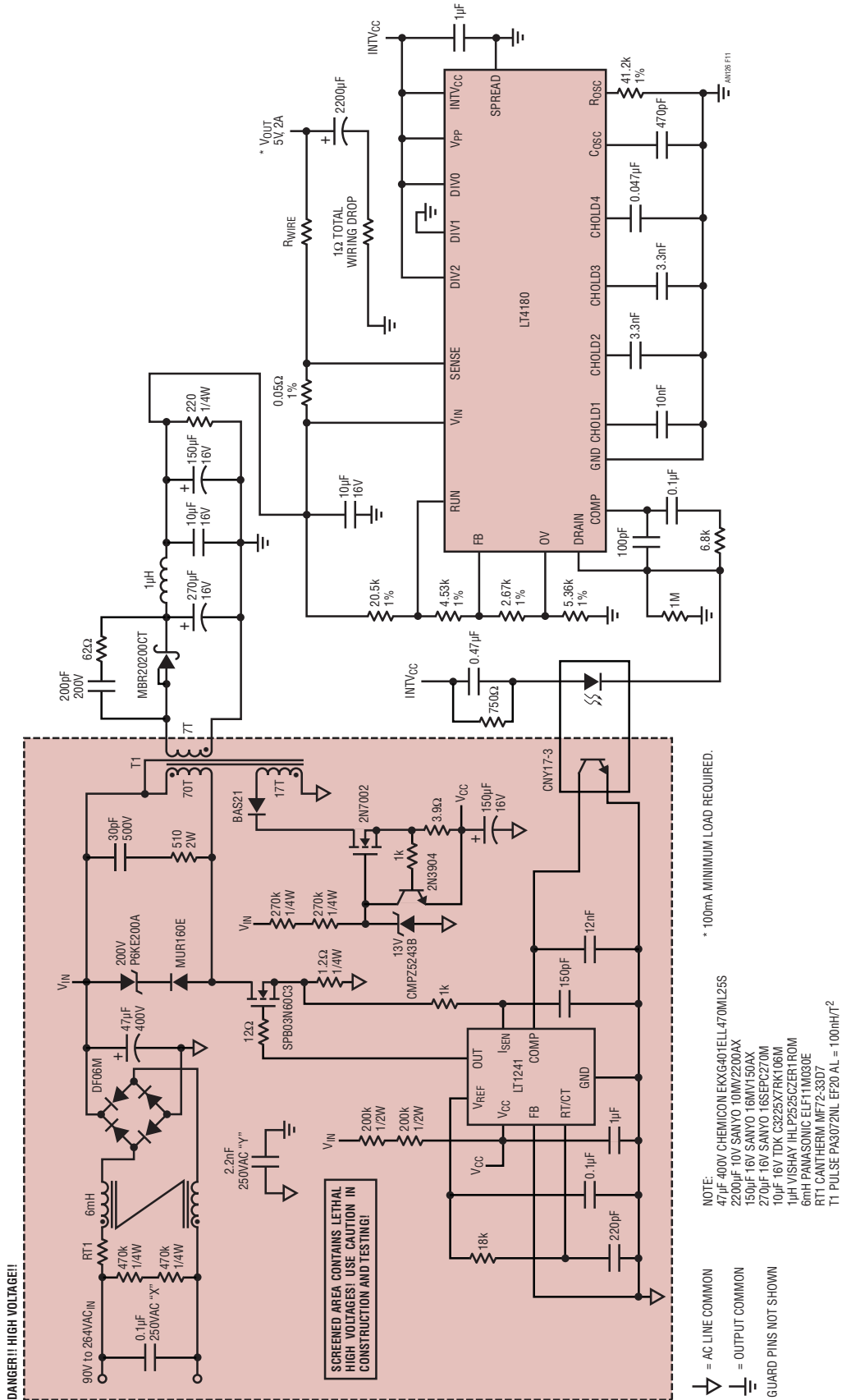
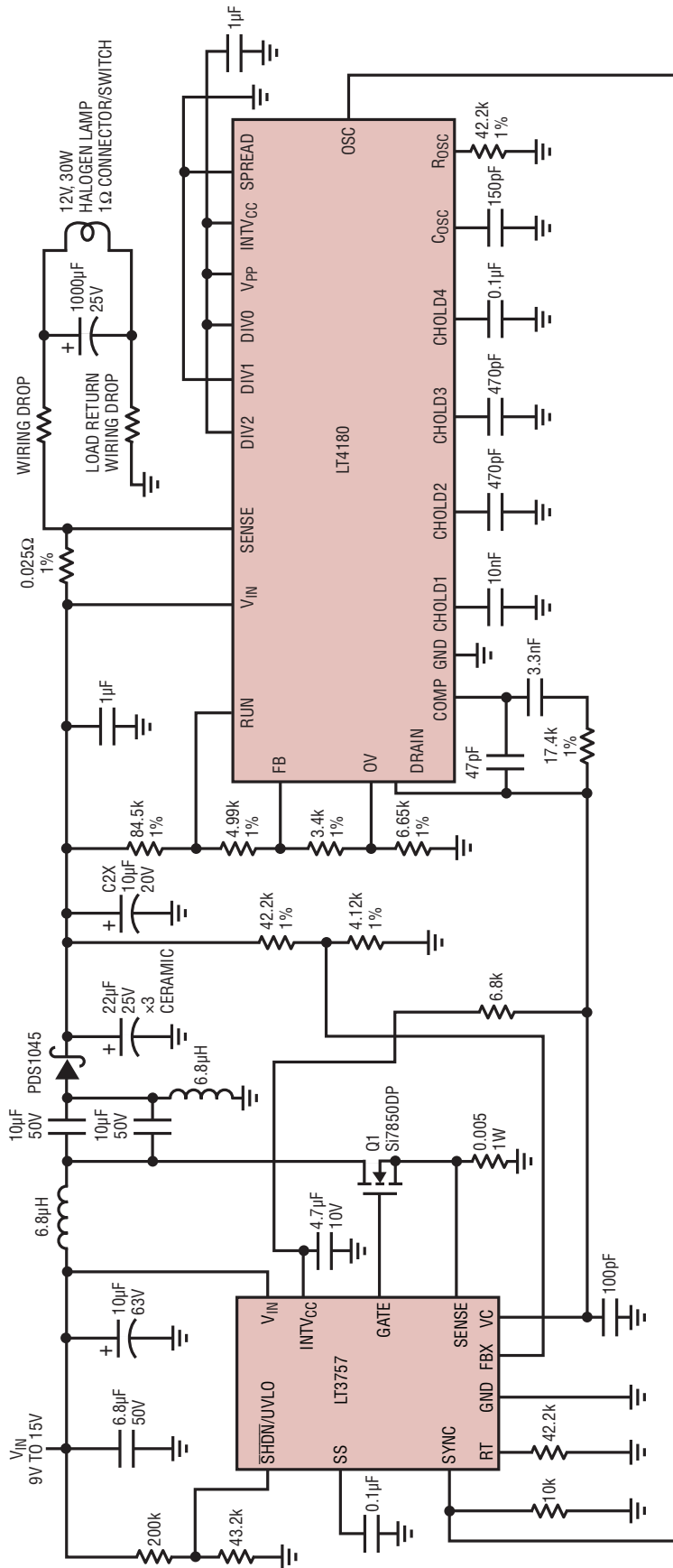


Figure 18. A 5V Output “Off-Line” Converter Equipped with Virtual Remote Sense. LT4180 Provides Remote Sensing, Closes Isolated Feedback Loop via Opto-Isolator

WARNING! SCREENED AREA CONTAINS LETHAL AC LINE CONNECTED HIGH VOLTAGES. USE CAUTION IN CONSTRUCTION AND TESTING.



AN126 F19

GUARD PINS NOT SHOWN
 IHL P4040DZR5R8M11 = 6.8µH
 UMK325B6106MM-T = 10µF, 50V
 TMK80226MM-T = 22µF
 C2X = ZOSVPIO

Figure 19. LT4180 Step Up/Down Converter Stabilizes 12V Drive to 30W Halogen Automotive Lamp Despite 9V → 15V Input Variation and Line Resistance Uncertainties

Application Note 126

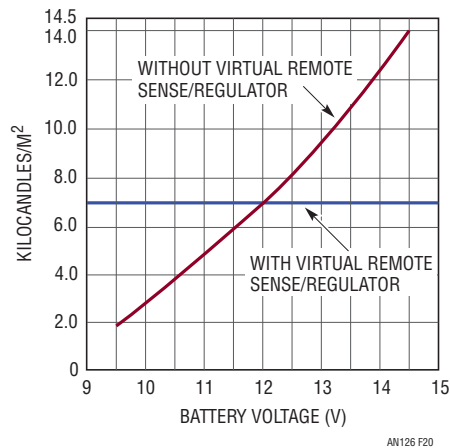


Figure 20. Unaided vs Remote Sensed/Regulated Halogen Lamp Light Output. Regulation Benefits Include Stable Illumination, Constant Color Output and Extended Lamp Life

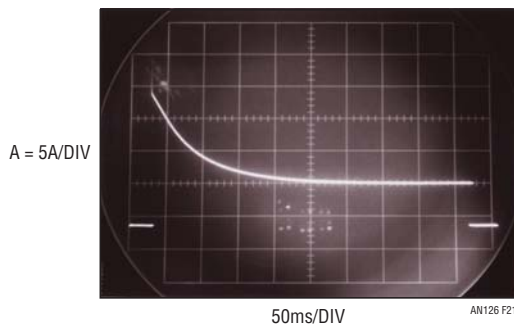


Figure 21. Lamp Turn-On Current Exceeds 20A Without Regulation, Degrading Lifetime

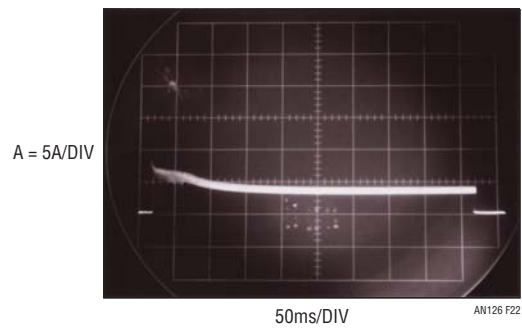


Figure 22. Regulation Promotes Soft Turn-On, 12V Drive Under High/Low Line Conditions, Optimizing Illumination and Improving Lamp Life

APPENDIX A

A Primer on LT4180 VRS Operation

Voltage drops in wiring can produce considerable load regulation errors in electrical systems (Figure A1). As load current I_L increases, voltage drop in the wiring ($I_L \cdot RW$) increases and the voltage delivered to the system (V_L) drops. The traditional approach to solving this problem, remote sensing, regulates the voltage at the load, increasing the power supply voltage (V_{OUT}) to compensate for voltage drops in the wiring. While remote sensing works well, it does require an additional pair of wires to measure at the load, which may not always be practical.

The LT4180 eliminates the need for a pair of remote sense wires by creating a virtual remote sense. Virtual remote sensing is achieved by measuring the incremental change in voltage that occurs with an incremental change in current in the wiring (Figure A2). This measurement can be used to infer the total DC voltage drop in the wiring, which can then be compensated for. The Virtual Remote Sense takes over control of the power supply via its feedback pin (V_{FB}), maintaining tight regulation of load voltage V_L .

Figure A3 shows the timing diagram for Virtual Remote Sensing (VRS). A new cycle begins when the power supply and VRS close the loop around V_{OUT} (Regulate $V_{OUT} = H$). Both V_{OUT} and I_{OUT} slew and settle to a new value, and these values are stored in the Virtual Remote Sense (Track $V_{OUTHIGH} = L$ and Track $I_{OUT} = L$). The V_{OUT} feedback loop is opened and a new feedback loop is set up commanding the power supply to deliver 90% of the previously measured current ($0.9 I_{OUT}$). V_{OUT} drops to a new value as the power supply reaches a new steady state, and this information is also stored in the Virtual Remote Sense. At this point, the change in the output voltage (ΔV_{OUT}) for a -10% change in output current has been measured and is stored in the Virtual Remote Sense. This voltage is used during the next VRS cycle to compensate for voltage drops due to wiring resistance.

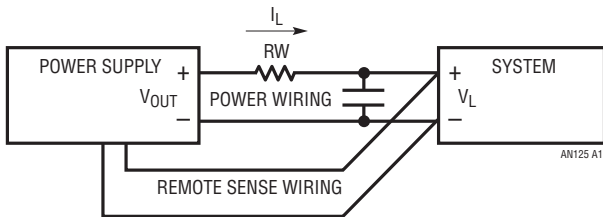


Figure A1. Traditional Remote Sensing Works Well But Requires Two Sense Wires

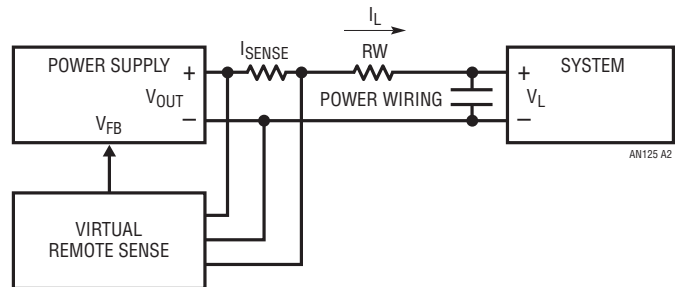


Figure A2. Virtual Remote Sensing Eliminates Sense Wires

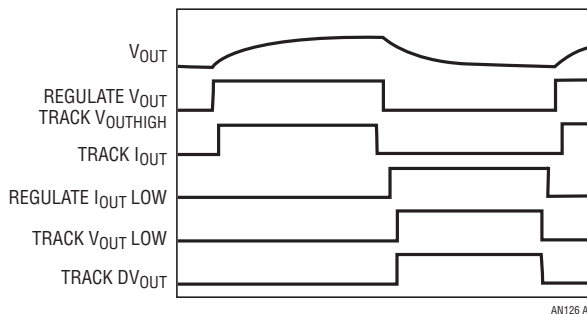


Figure A3. Simplified Virtual Remote Sense Timing Diagram. State Machine Driven Sequence Samples and Stores Information Necessary to Set Appropriate Power Supply Voltage to Correct for Wiring Losses

APPENDIX B

Design Guidelines for LT4180 VRS Circuits

INTRODUCTION

The LT4180 is designed to interface with a variety of power supplies and regulators having either an external feedback or control pin. In Figure B1, the regulator error amplifier (which is a g_m amplifier) is disabled by tying its inverting input to ground. This converts the error amplifier into a constant-current source which is then controlled by the drain pin of the LT4180. This is the preferred method of interfacing because it eliminates the regulator error amplifier from the control loop which simplifies compensation and provides best control loop response.

For proper operation, increasing control voltage should correspond to increasing regulator output. For example, in the case of a current mode switching power supply, the control pin I_{TH} should produce higher peak currents as the I_{TH} pin voltage is made more positive.

Isolated power supplies and regulators may also be used by adding an opto-coupler (Figure B2). LT4180 output voltage $INTV_{CC}$ supplies power to the opto-coupler LED. In situations where the control pin V_C of the regulator may exceed 5V, a cascode may be added to keep the DRAIN pin of the LT4180 below 5V (Figure B3). Use a Low V_T MOSFET for the cascode transistor.

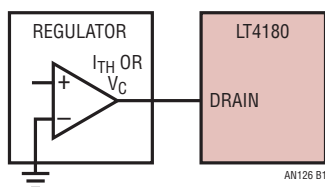


Figure B1. Nonisolated Regulator Interface

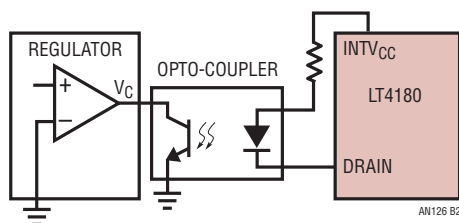


Figure B2. Isolated Power Supply Interface

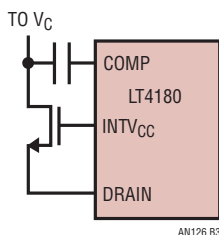


Figure B3. Cascoded DRAIN Pin for Isolated Supplies

DESIGN PROCEDURE

The first step in the design procedure (Figure B4) is to determine whether the LT4180 will control a linear or switching supply/regulator. If using a switching power supply or regulator, it is recommended that the supply be synchronized to the LT4180 by connecting the OSC pin to the SYNC pin (or equivalent) of the supply.

If the power supply is synchronized to the LT4180, the power supply switching frequency is determined by:

$$f_{osc} = \frac{4}{R_{osc} \cdot C_{osc}}$$

Recommended values for R_{osc} are between 20k and 100k (with 30.1k the optimum for best accuracy) and greater than 100pF for C_{osc} . C_{osc} may be reduced to as low as 50pF, but oscillator frequency accuracy will be somewhat degraded.

The following example synchronizes a 250kHz switching power supply to the LT4180. In this example, start with $R_{osc} = 30.1k$:

$$C_{osc} = \frac{4}{250kHz \cdot 30.1k} = 531pF$$

This example uses 470pF. For 250kHz:

$$R_{osc} = \frac{4}{250kHz \cdot 470pF} = 34.04k$$

The closest standard 1% value is 34k.

The next step is to determine the highest practical dither frequency. This may be limited either by the response time of the power supply or regulator, or by the propagation time of the wiring connecting the load to the power supply or regulator.

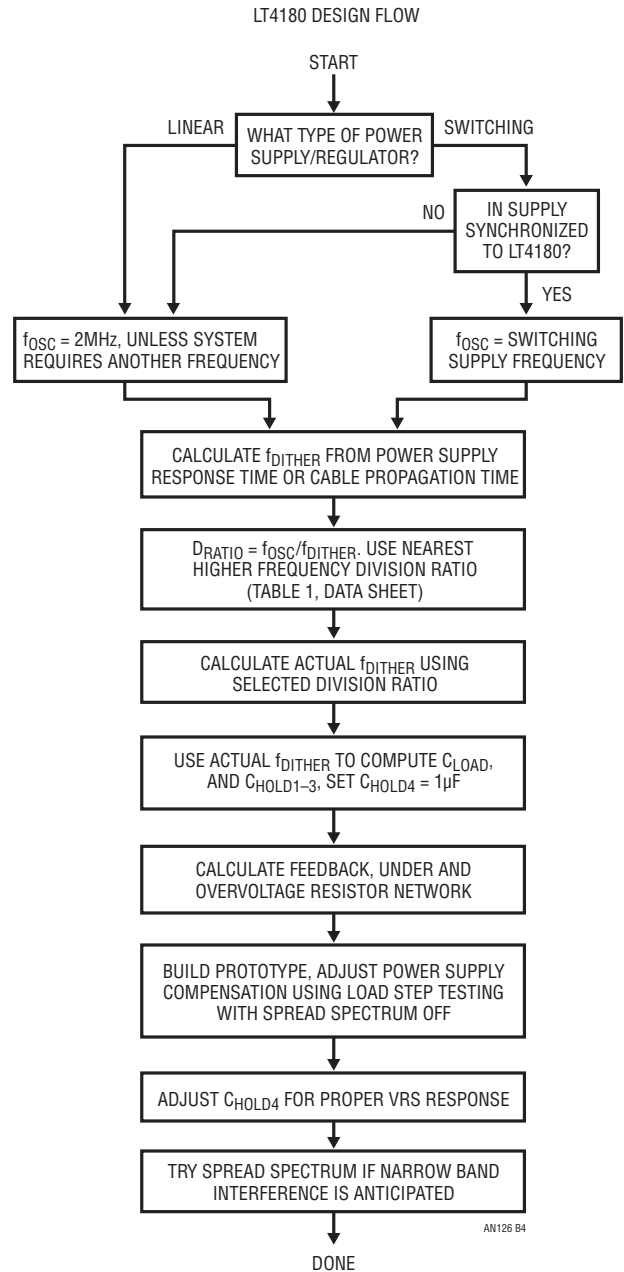


Figure B4. Design Flow Chart

Application Note 126

First determine the settling time (to 1% of final value) of the power supply. The settling time should be the worst-case value (over the whole operating envelope: V_{IN} , I_{LOAD} , etc.).

$$F1 = \frac{1}{2 \cdot t_{SETTLING}} \text{ Hz}$$

For example, if the power supply takes 1ms to settle (worst-case) to within 1% of final value:

$$F1 = \frac{1}{2 \cdot 1e-3} = 500\text{Hz}$$

Next, determine the propagation time of the wiring. In order to ignore transmission line effects, the dither period should be approximately twenty times longer than this. This will limit dither frequency to:

$$F2 = \frac{V_F}{20 \cdot 1.017\text{ns/ft} \cdot L} \text{ Hz}$$

where V_F is the velocity factor (or velocity of propagation), and L is the length of the wiring (in feet).

For example, assume the load is connected to a power supply with 1000ft of CAT5 cable. Nominal velocity of propagation is approximately 70%.

$$F2 = \frac{0.7}{20 \cdot 1.017e-9 \cdot 1000} = 34.4\text{kHz}$$

The maximum dither frequency should not exceed $F1$ or $F2$ (whichever is less):

$$f_{DITHER} < \min(F1, F2).$$

Continuing this example, the dither frequency should be less than 500Hz (limited by the power supply).

With the dither frequency known, the division ratio can be determined:

$$D_{RATIO} = \frac{f_{OSC}}{f_{DITHER}} = \frac{250,000}{500} = 500$$

The nearest division ratio is 512 (set DIV0 = L, DIV1 = DIV2 = H). Based on this division ratio, nominal dither frequency will be:

$$f_{DITHER} = \frac{f_{OSC}}{D_{RATIO}} = \frac{250,000}{512} = 488\text{Hz}$$

After the dither frequency is determined, the minimum load decoupling capacitor can be determined. This load capacitor must be sufficiently large to filter out the dither signal at the load.

$$C_{LOAD} = \frac{2.2}{R_{WIRE} \cdot 2 \cdot f_{DITHER}}$$

where C_{LOAD} is the minimum load decoupling capacitance, R_{WIRE} is the minimum wiring resistance of one conductor of the wiring pair, and f_{DITHER} is the minimum dither frequency.

Continuing the example, our CAT5 cable has a maximum 9.38 Ω /100m conductor resistance.

Maximum wiring resistance is:

$$R_{WIRE} = 2 \cdot 1000\text{ft} \cdot 0.305\text{m/ft} \cdot 0.0938\Omega/\text{m}$$

$$R_{WIRE} = 57.2\Omega$$

With an oscillator tolerance of $\pm 15\%$, the minimum dither frequency is 414.8Hz, so the minimum decoupling capacitance is:

$$C_{LOAD} = \frac{2.2}{57.2\Omega \cdot 2 \cdot 414.8\text{Hz}} = 46.36\mu\text{F}$$

This is the minimum value. Select a nominal value to account for all factors which could reduce the nominal, such as initial tolerance, voltage and temperature coefficients and aging.

CHOLD Capacitor Selection and Compensation

With dither frequency determined, use the following equations to determine CHOLD values:

$$C_{\text{HOLD1}} = \frac{11.9\text{nF}}{f_{\text{DITHER}}(\text{kHz})}$$

and

$$C_{\text{HOLD2}} = C_{\text{HOLD3}} = \frac{2.5\text{nF}}{f_{\text{DITHER}}(\text{kHz})}$$

So, with a dither frequency of 488Hz:

$$C_{\text{HOLD1}} = \frac{11.9\text{nF}}{0.488\text{kHz}} = 24.4\text{nF}$$

and

$$C_{\text{HOLD2}} = C_{\text{HOLD3}} = \frac{2.5\text{nF}}{0.488(\text{kHz})} = 5.12\text{nF}$$

NPO ceramic or other capacitors with low leakage and dielectric absorption should be used for all hold capacitors.

Set C_{HOLD4} to $1\mu\text{F}$.

Start with a 47pF capacitor between the COMP and DRAIN pins of the LT4180. Add an RC network in parallel with the 47pF capacitor. 10k and 10nF are good starting values. Connect a DC load corresponding to full-scale load current and verify that V_{OUT} produces a rounded squarewave without any noticeable overshoot or ringing (similar to the V_{OUT} waveform in Figure 16). If overshoot or ringing is observed, decrease the value of the resistor until it just disappears. If overshoot or ringing is not observed, increase the value of the resistor until it is observed, then slightly decrease the value of the resistor so that overshoot and ringing disappear. Check for proper voltage drop correction and converter behavior (start-up, regulation etc.), over the load range, and repeat the above procedure with a smaller value of the compensation capacitor, if necessary. Decrease C_{HOLD4} capacitance until V_{OUT} exhibits slight low frequency instability, then increase C_{HOLD4} slightly from this value.

Setting Output Voltage, Undervoltage and Overvoltage Thresholds

The RUN pin has accurate rising and falling thresholds which may be used to determine when Virtual Remote Sense operation begins. Undervoltage threshold should never be set lower than the minimum operating voltage of the LT4180 (3.1V).

The overvoltage threshold should be set slightly greater than the highest voltage which will be produced by the power supply or regulator:

$$V_{\text{OUT(MAX)}} = V_{\text{LOAD(MAX)}} + V_{\text{WIRE(MAX)}}$$

$V_{\text{OUT(MAX)}}$ should never exceed $1.5 \cdot V_{\text{LOAD}}$

Since the RUN and OV pins connect to MOSFET input comparators, input bias currents are negligible and a common voltage divider can be used to set both thresholds (Figure B5).

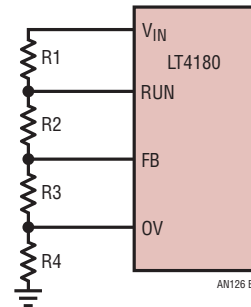


Figure B5. Voltage Divider for UVL and OVL

The voltage divider resistors can be calculated from the following equations:

$$R_T = \frac{V_{\text{OV}}}{200\mu\text{A}}, \quad R_4 = \frac{1.22\text{V}}{200\mu\text{A}}$$

where R_T is the total divider resistance and V_{OV} is the overvoltage set point.

Application Note 126

Find the equivalent series resistance for R2 and R3 (R_{SERIES}). This resistance will determine the RUN voltage level.

$$R_{\text{SERIES}} = \left(\frac{1.22 \cdot R_T}{V_{\text{UVL}}} \right) - R_4$$

$$R_1 = R_T - R_{\text{SERIES}} - R_4$$

$$R_3 = \frac{1.22V - \left(\frac{V_{\text{OUT(NOM)}} \cdot R_4}{R_T} \right)}{\frac{V_{\text{OUT(NOM)}}}{R_T}}$$

$$R_2 = R_{\text{SERIES}} - R_3$$

Where V_{UVL} is the RUN voltage and $V_{\text{OUT(NOM)}}$ is the nominal output voltage desired.

For example, with $V_{\text{UVL}} = 4V$, $V_{\text{OV}} = 7.5V$ and $V_{\text{OUT(NOM)}} = 5V$,

$$R_T = \frac{7.5V}{200\mu A} = 37.5k$$

$$R_4 = \frac{1.22V}{200\mu A} = 6.1k$$

$$R_{\text{SERIES}} = \left(\frac{1.22V \cdot 37.5k}{4V} \right) - 6.1k = 5.34k$$

$$R_1 = 37.5k - 5.34k - 6.1k = 26.06k$$

$$R_3 = \frac{1.22V - \left(\frac{5V \cdot 6.1k}{37.5k} \right)}{\frac{5V}{37.5k}} = 3.05k$$

$$R_2 = R_{\text{SERIES}} - R_3 = 2.29k$$

R_{SENSE} SELECTION

Select the value of R_{SENSE} so that it produces a 100mV voltage drop at maximum load current. For best accuracy, V_{IN} and SENSE should be Kelvin connected to this resistor.

Soft-Correct Operation

The LT4180 has a soft-correct function which insures orderly start-up (Figure B6). When the RUN pin rising threshold is first exceeded (indicating V_{IN} has crossed its undervoltage lockout threshold), power supply output voltage is set to a value corresponding to zero wiring voltage drop (no correction for wiring). Over a period of time (determined by C_{HOLD4}), the power supply output voltage ramps up to account for wiring voltage drops, providing best load-end voltage regulation. A new soft-correct cycle is also initiated whenever an overvoltage condition occurs.

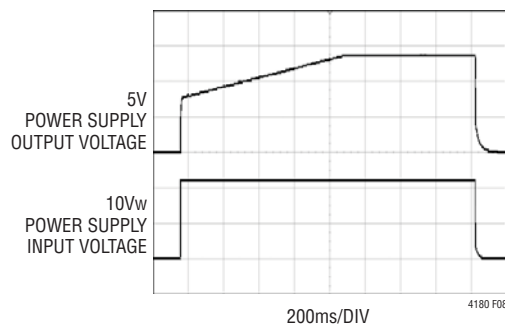


Figure B6. Soft-Correct Operation, $C_{\text{HOLD4}} = 1\mu F$

Using Guard Rings

The LT4180 includes a total of four track/holds in the Virtual Remote Sense path. For best accuracy, all leakage sources on the CHOLD pins should be minimized.

At very low dither frequencies, the circuit board layout may include guard rings which should be tied to their respective guard ring drivers.

To better understand the purpose of guard rings, a simplified model of hold capacitor leakage (with and without guard rings) is shown in Figure B7. Without guard rings, a large difference voltage may exist between the hold capacitor (Pin 1) node and adjacent conductors (Pin 2) producing substantial leakage current through the leakage resistance (R_{LKG}). By adding a guard ring driver with approximately the same voltage as the voltage on the hold capacitor node, the difference voltage across R_{LKG1} is reduced substantially thereby reducing leakage current on the hold capacitor.

Synchronization

Linear and switching power supplies and regulators may be used with the LT4180. In most applications regulator interference should be negligible. For those applications where accurate control of interference spectrum is desirable, an oscillator output has been provided so that

switching supplies may be synchronized to the LT4180 (Figure B8). The OSC pin was designed so that it may directly connect to most regulators, or drive opto-isolators (for isolated power supplies).

Spread Spectrum Operation

Virtual remote sensing relies on sampling techniques. Because switching power supplies are commonly used, the LT4180 uses a variety of techniques to minimize potential interference (in the form of beat notes which may occur between the dither frequency and power supply switching frequency). Besides several types of internal filtering, and the option for VRS/power supply synchronization, the LT4180 also provides spread spectrum operation.

By enabling spread spectrum operation, low modulation index pseudo-random phasing is applied to Virtual Remote Sense timing. This has the effect of converting any remaining narrow-band interference into broadband noise, reducing its effect.

Increasing Voltage Correction Range

Correction range may be slightly improved by regulating $INTV_{CC}$ to 5V. This may be done by placing an LDO between V_{IN} and $INTV_{CC}$. Contact Linear Technology Applications for more information.

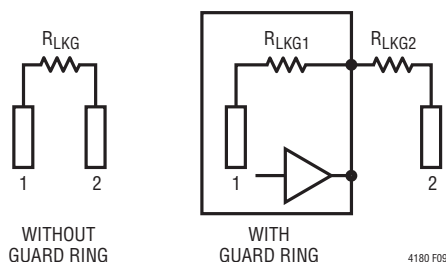


Figure B7. Simplified Leakage Models (with and without Guard Rings)

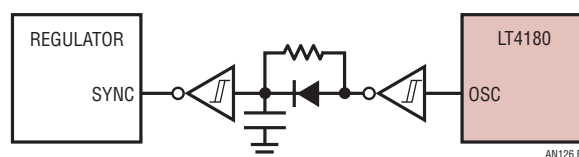
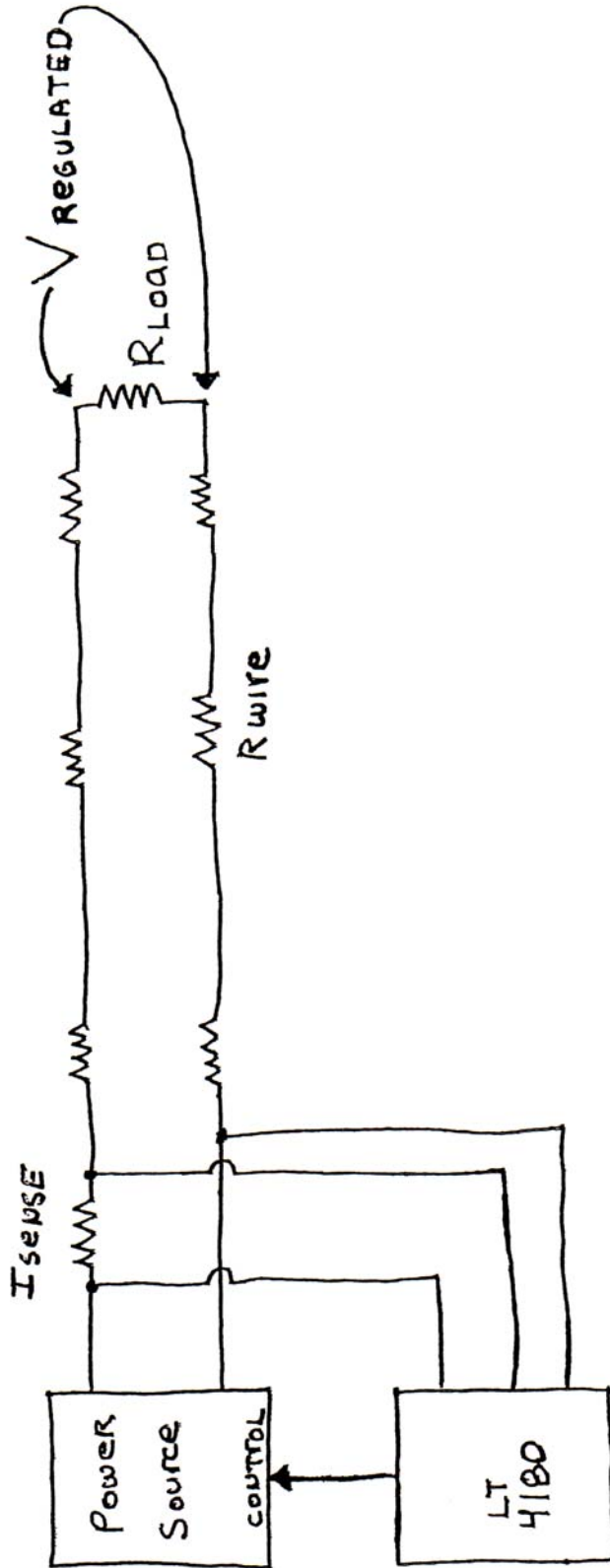


Figure B8. Clock Interface for Synchronization

Application Note 126



"Any sufficiently advanced technology is indistinguishable from magic."

— Arthur C. Clarke

2 Nanosecond, .1% Resolution Settling Time Measurement for Wideband Amplifiers

Quantifying Quick Quiescence

Jim Williams

INTRODUCTION

Instrumentation, waveform synthesis, data acquisition, feedback control systems and other application areas utilize wideband amplifiers. Current generation components (see box section, page 2, “A Precision Wideband Amplifier with 9ns Settling Time”) feature good DC precision while maintaining high speed operation. Verifying precision operation at high speed is essential, and presents a high order measurement challenge.

SETTLING TIME DEFINED

Amplifier DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, amplifier settling time is extraordinarily difficult to determine. Settling time is the elapsed time from input application until the output arrives at and remains within a specified error band around the final value. It is usually specified for a full-scale transition. Figure 1 shows that settling time has three distinct components. The *delay time* is small and almost entirely due to amplifier propagation delay. During this interval there is no output movement.

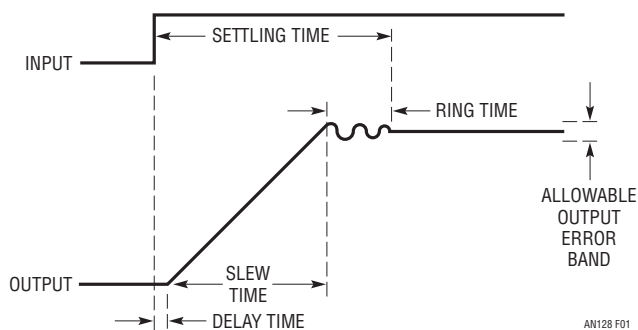


Figure 1. Settling Time Components Include Delay, Slew and Ring Times. Fast Amplifiers Reduce Slew Time, Although Longer Ring Time Usually Results. Delay Time Is Normally a Small Term

During *slew time* the amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs which degrade DC error terms¹.

Measuring anything at any speed requires care. Dynamic measurement is particularly challenging. Reliable nanosecond region settling time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique².

CONSIDERATIONS FOR MEASURING NANOSECOND REGION SETTLING TIME

Historically, settling time has been measured with circuits similar to that in Figure 2. The circuit uses the “false sum node” technique. The resistors and amplifier form a bridge type network. Assuming ideal resistors, the amplifier output will step to $-V_{IN}$ when the input is driven. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider’s attenuation means the probe’s output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. Several flaws exist. The

Note 1. This issue is treated in detail in latter portions of the text. Also see Appendix B, “Practical Considerations for Amplifier Compensation”.

Note 2. The approach used for settling time measurement and its description, while new, borrows from previous publications. See References 1-5, and Reference 9.

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an128f

Application Note 128

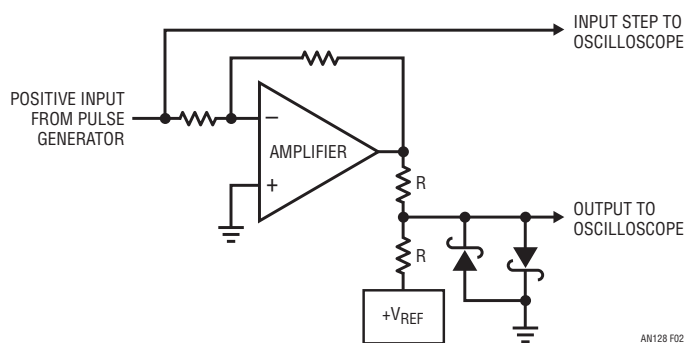


Figure 2. Popular Summing Scheme for Settling Time Measurement Provides Misleading Results. Pulse Generator Post-Transition Aberrations Appear at Output. Large Oscilloscope Overdrive Occurs. Displayed Information Is Meaningless

circuit requires the input pulse to have a flat top within the required measurement limits. Typically, settling within 5mV or less for a 5V step is of interest. No general purpose pulse generator is meant to hold output amplitude and noise within these limits. Generator output-caused aberrations appearing at the oscilloscope probe will be indistinguishable from

amplifier output movement, producing unreliable results. The oscilloscope connection also presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. 1x probes are not suitable because of their excessive input capacitance. A 10x probe's attenuation sacrifices oscilloscope gain and its 10pF capacitance still introduces significant lag at nanosecond speeds. An active 1x, 1pF FET probe largely alleviates the problem but a more serious issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope will undergo an unacceptable overload, bringing displayed results into question³.

At 0.1% resolution (5mV at the amplifier output –2.5mV at the oscilloscope), the oscilloscope typically undergoes a 10x overdrive at 10mV/DIV, and the desired 2.5mV baseline is unattainable. At nanosecond speeds, the measurement becomes hopeless with this arrangement. There is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring amplifier settling time requires an oscilloscope that is somehow immune to overdrive and a “flat top” pulse generator. These become the central issues in wideband amplifier settling time measurement.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling ‘scope⁴. Unfortunately, these instruments are no longer manufactured (although still available on the secondary market). It is possible, however, to construct a circuit that borrows the overload advantages of classical sampling ‘scope technology. Additionally, the circuit can be endowed with features particularly suited for measuring nanosecond range settling time.

Note 3. For a discussion of oscilloscope overdrive considerations, see Appendix C, “Evaluating Oscilloscope Overdrive Performance”.

Note 4. Classical sampling oscilloscopes should not be confused with modern era digital sampling ‘scopes that have overdrive restrictions. See Appendix C, “Evaluating Oscilloscope Overload Performance” for comparisons of various type ‘scopes with respect to overdrive. For detailed discussion of classical sampling ‘scope operation, see References 23-26 and 29-31. Reference 24 is noteworthy; it is the most clearly written, concise explanation of classical sampling instruments the author is aware of—a 12-page jewel.

A PRECISION WIDEBAND AMPLIFIER WITH 9ns SETTLING TIME

Historically, wideband amplifiers provided speed, but sacrificed precision and, often, settling time. The LT1818 op amp does not require this compromise. It features low offset voltage and bias current with adequate gain for 0.1% accuracy. Settling time is 9ns to 0.1% for a 5V step. The output will drive a 100Ω load to ±3.75V with ±5V supplies, and up to 20pF capacitive loading is permissible at unity gain. The table below provides short form specifications.

LT1818 Short Form Specifications

CHARACTERISTIC	SPECIFICATION
Offset Voltage	0.2mV
Offset Voltage vs Temperature	10μV/°C
Bias Current	2μA
DC Gain	2500
Noise Voltage	6nV/√Hz
Output Current	70mA
Slew Rate	2500V/μs
Gain-Bandwidth	400MHz
Delay	1ns
Settling Time	9ns/0.1%
Supply Current	9mA

The flat-top pulse generator requirement can be avoided by switching current, rather than voltage. It is much easier to gate a quickly settling current into the amplifier's summing node than to control a voltage. This makes the input pulse generator's job easier, although it still must have a rise time of about 1 nanosecond to avoid measurement errors.

PRACTICAL NANOSECOND SETTLING TIME MEASUREMENT

Figure 3 is a conceptual diagram of a settling time measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the oscilloscope is connected to the settle point by a switch. The switch state is determined by a delayed pulse generator, which is triggered from the input pulse. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way, the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

A switch at the amplifier's summing junction is controlled by the input pulse. This switch gates current to the amplifier via a voltage-driven resistor. This eliminates the “flat-top” pulse generator requirement, although the switch must be fast and devoid of drive artifacts.

Figure 4 is a more complete representation of the settling time scheme. Figure 3's blocks appear in greater detail and some new refinements show up. The amplifier summing area is unchanged. Figure 3's delayed pulse generator has

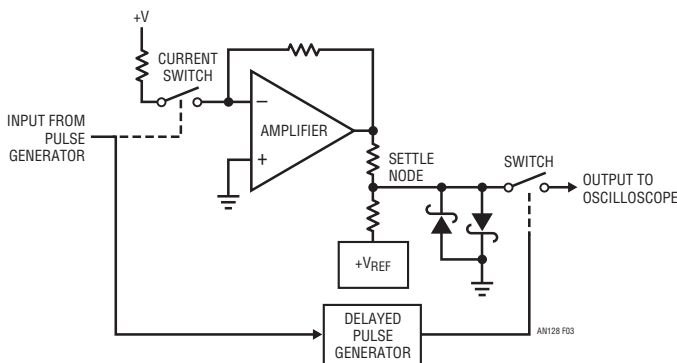


Figure 3. Conceptual Arrangement Is Insensitive to Pulse Generator Aberrations and Eliminates Oscilloscope Overdrive. Input Switch Gates Current Step to Amplifier. Second Switch, Controlled by Delayed Pulse Generator, Prevents Oscilloscope from Monitoring Settle Node Until Settling Is Nearly Complete

been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that compensates for the propagation delay of the settling time measurement path. Similarly, another delay compensates sample gate pulse generator propagation delay. This delay causes the sample gate pulse generator to be driven with a phase-advanced version of the pulse which triggers the amplifier under test. This considerably improves minimum measurable settling time by making sample gate pulse generator propagation delay irrelevant.

The most striking new aspects of the diagram are the diode bridge switch and the multiplier. The diode bridge's balance, combined with matched, low capacitance Schottky diodes and high speed drive, yields clean switching. The bridge switches current into the amplifier's summing point very quickly, with settling inside a nanosecond. The diode clamp to ground prevents excessive bridge drive swings and ensures that non-ideal input pulse characteristics are nearly irrelevant.

Requirements for Figure 4's sample gate are stringent. It must faithfully pass wideband signal path information without introducing alien components, particularly those deriving from the switch command channel (“sample gate pulse”)⁵.

The sample gate multiplier functions as a wideband, high resolution, extremely low feedthrough switch. The great advantage of this approach is that the switch control channel can be maintained in-band; that is, its transition rate is held within the multiplier's 250MHz bandpass. The multiplier's wide bandwidth means the switch command transition is under control at all times. There are no out-of-band responses, greatly reducing feedthrough and parasitic artifacts.

Note 5. Conventional choices for the sample gate switch include FETs and the sampling diode bridge. FET parasitic gate to channel capacitances result in large gate drive originated feedthrough into the signal path. For almost all FETs, this feedthrough is many times larger than the signal to be observed, inducing overload and obviating the switches' purpose. The diode bridge is better; its small parasitic capacitances tend to cancel and the symmetrical, differential structure results in very low feedthrough. Practically, the bridge requires DC and AC trims and complex drive and support circuitry. LTC Application Note 74, “Component and Measurement Advances Ensure 16-bit DAC Settling Time” utilized such a sampling bridge and it is detailed in that text. See Reference 3. References 2, 9 and 11 describe a similar sampling bridge based approach.

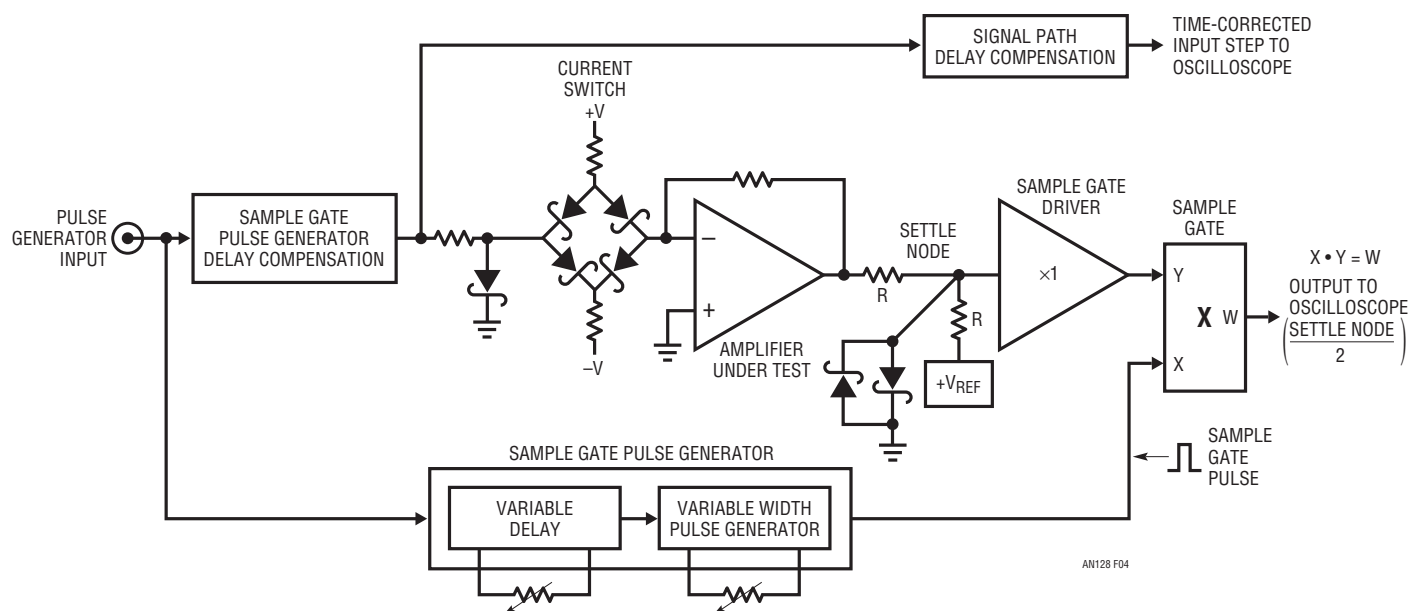


Figure 4. Block Diagram of Settling Time Measurement Scheme. Diode Bridge Cleanly Switches Input Current to Amplifier. Multiplier Based Sampling “Switch” Eliminates Signal Paths Pre-Settling Excursion, Preventing Oscilloscope Overdrive. Input Step Time Reference and Sample Gate Pulse Generator Are Compensated for Test Circuit Delays

DETAILED SETTLE TIME CIRCUITRY

Figure 5 is a detailed schematic of the settling time measurement circuitry. The input pulse switches the input bridge via a delay network (“A” inverters) and a driver stage (“C” inverters). The delay compensates the sample gate pulse generator’s delayed response, ensuring that the sample gate pulse can occur immediately after the amplifier-under-tests’ slew time ends. The delay range is chosen so that the sample gate pulse can be adjusted to occur *before* the amplifier slews. This capability is obviously unused in operation although it guarantees that the settling interval will always be capturable.

The “C” inverters form a non-inverting driver stage to switch the diode bridge. Various trims optimize driver output pulse shape, providing a clean, fast impulse to the diode bridge⁶. The high fidelity pulse, devoid of undamped components, prevents radiation and disruptive ground currents from degrading the measurement noise floor. The driver also activates the “B” inverters, which supply a time corrected input step to the oscilloscope.

The driver output pulse transitions through the 1N5712 diode clamp potential in under a nanosecond, causing essentially instantaneous diode bridge switching. The resultant cleanly settling current into the amplifier under tests’ summing point causes proportionate amplifier output

movement. The negative bias current at the amplifiers summing point combined with the current step produces a +2.5V to –2.5V amplifier output transition. The amplifier’s output is compared against a 5V supply derived reference via the summing resistors. The clamped “settle node” is unloaded by A1, which feeds the sample gate signal path information.

The comparator based sample gate pulse generator produces a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 2k potentiometer) sets sample gate on-time. The Q1 stage forms the sample gate pulse into a fast rise, exceptionally clean event, furnishing high purity, calibrated amplitude, “on-off” switching instruction to the sample gate multiplier. If the sample gate pulse delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way, the oscilloscope’s output is reliable and meaningful data may be taken.

Figure 6 shows circuit waveforms. Trace A is the time-corrected input pulse, Trace B the amplifier output, Trace C the

Note 6. To maintain text flow and focus, trimming procedures are not presented here. Detailed trimming information appears in Appendix A, “Measuring and Compensating Settling Circuit Delay and Trimming Procedures.”

Application Note 128

sample gate pulse and Trace D the settling time output⁷. When the sample gate pulse goes high, the sample gate switches cleanly, and the last 20mV of slew are easily observed. Ring time is also clearly visible, and the amplifier settles nicely to final value. When the sample gate pulse goes low, the sample gate switches off with only 2mV of feedthrough. Note that there is no off-screen activity at any time—the oscilloscope is never subjected to overdrive.

Figure 7 expands vertical and horizontal scales so that settling detail is more visible⁸. Trace A is the time-corrected input pulse and Trace B the settling output. The last 50mV of slew are easily observed, and the amplifier settles inside 5mV (0.1%) in 9 nanoseconds when CF (see Figure 5) is optimized⁹.

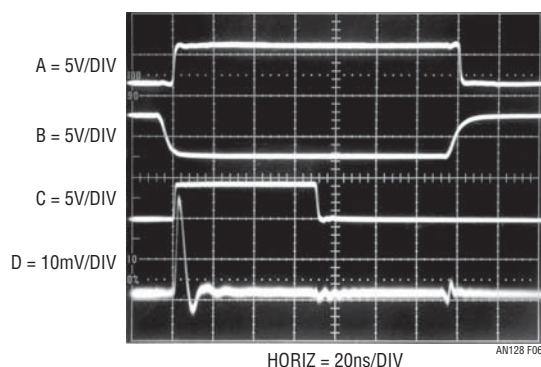


Figure 6. Settling Time Circuit Waveforms Include Time-Corrected Input Pulse (Trace A), Amplifier-Under-Test Output (Trace B), Sample Gate (Trace C) and Settling Time Output (Trace D). Sample Gate Window's Delay and Width Are Variable. Trace B Appears Time Skewed Relative to Time Corrected Trace A.

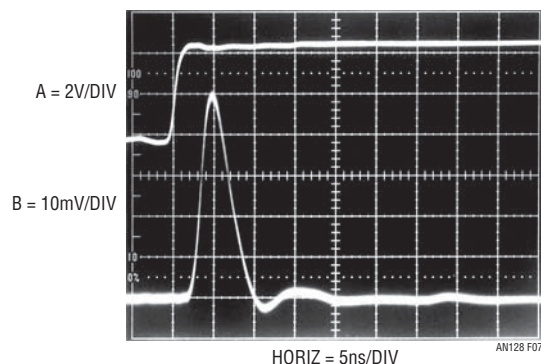


Figure 7. Expanded Vertical and Horizontal Scales Show 9ns Amplifier Settling within 5mV (Trace B). Trace A Is Time Corrected Input Step

Note 7. When interpreting waveform placement note that trace B appears time skewed relative to time corrected trace A. This accounts for trace B's falsely apparent movement before trace A's ascent.

USING THE SAMPLING-BASED SETTLING TIME CIRCUIT

In general, it is good practice to walk the sampling window “backwards” in time up to the last 50mV or so of amplifier slewing so that the onset of ring time is observable without encountering oscilloscope overdrive. The sampling based approach provides this capability and it is a very powerful measurement tool. Slower amplifiers may require extended delay and/or sampling window times, necessitating larger capacitor values in the delayed pulse generator timing networks.

VERIFYING RESULTS—ALTERNATE METHOD

The sampling-based settling time circuit appears to be a useful measurement solution. How can its results be tested to ensure confidence? A good way is to make the same measurement with an alternate method and see if results agree. It was stated earlier that classical sampling oscilloscopes were inherently immune to overdrive¹⁰. If this is so, why not utilize this feature and attempt settling time measurement directly at the clamped settle node? Figure 8 does this. Under these conditions, the sampling scope¹¹ is heavily overdriven, but is ostensibly immune to the insult. Figure 9 puts the sampling oscilloscope to the test. Trace A is the time corrected input pulse and Trace B the settle signal. Despite a brutal overdrive, the ‘scope appears to respond cleanly, giving a very plausible settle signal presentation.

SUMMARY OF RESULTS AND MEASUREMENT LIMITS

The simplest way to summarize the different method's results is by visual comparison. Ideally, if both approaches represent good measurement technique and are properly constructed, results should be identical. If this is the case, the data produced by the two methods has a high probability of being valid. Examination of Figures 9 and 10 shows

Note 8. In this and all following photos, settling time is measured from the onset of the time-corrected input pulse. Additionally, settling signal amplitude is calibrated with respect to the amplifier, not the settle node. This eliminates ambiguity due to the settle node's resistance ratio.

Note 9. This section mentions amplifier frequency compensation within the context of sampling-based settling time measurement. As such, it is necessarily brief. Considerably more detail is available in Appendix B, “Practical Considerations for Amplifier Compensation.”

Note 10. See Appendix C, “Evaluating Oscilloscope Overdrive Performance” for in-depth discussion.

Note 11. Tektronix type 661 with 4S1 vertical and 5T3 timing plug-ins.

nearly identical settling times and highly similar settling waveform signatures. This kind of agreement provides a high degree of credibility to the measured results.

Close observation of settling time circuit operation indicates a noise floor/feedthrough imposed amplitude

resolution limit of 2mV. The time resolution limit is about 2 nanoseconds to 5mV settling. For details, see the section “Measurement Limits and Uncertainties”, in Appendix A, “Measuring and Compensating Settling Circuit Delay and Trimming Procedures.”

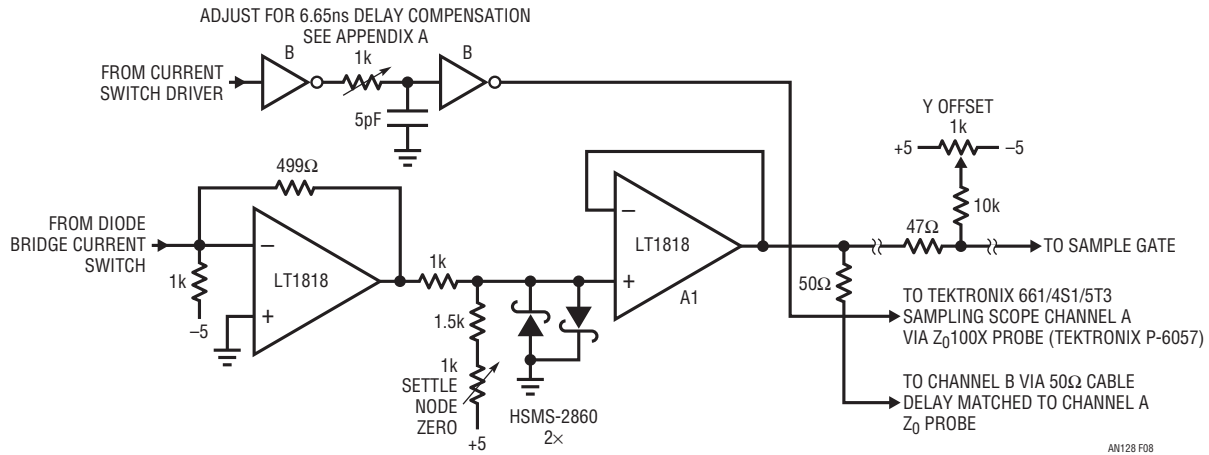


Figure 8. Settling Time Test Circuit Modifications Using Classical Tektronix 661/4S1/5T3 1GHz Sampling Oscilloscope. Sampling ‘Scope’s Inherent Overload Immunity Permits Large Off-Screen Excursions without Degrading Measurement Fidelity

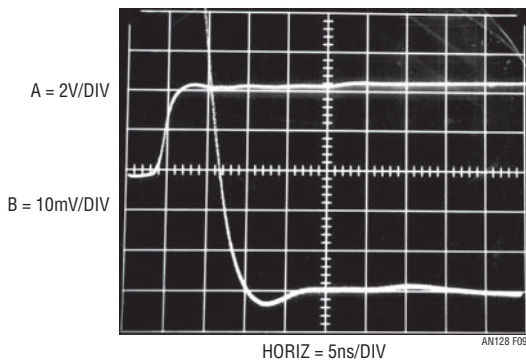


Figure 9. Settling Time Measurement with Classical Sampling ‘Scope. Oscilloscope’s Overload Immunity Allows Accurate Measurement Despite Extreme Overdrive. 9ns Settling Time and Waveform Profile Are Consistent with Figure 7

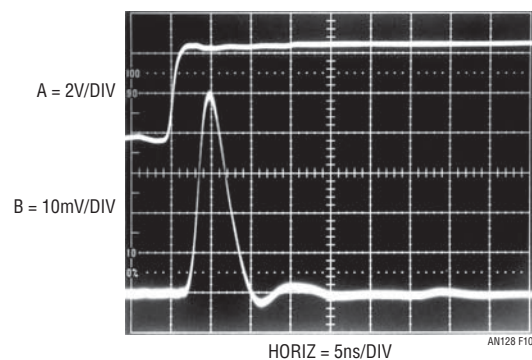


Figure 10. Settling Time Measurement Using Figure 5’s Circuit. $T_{SETTLE} = 9ns$. Results Correlate with Figure 9

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an128f

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APPENDIX A

Measuring and Compensating Settling Circuit Delay and Trimming Procedures

The settling time circuit requires trimming to achieve quoted performance. The trims fall into four loosely defined categories including current switch bridge drive pulse shaping, circuit delays, sample gate pulse purity and sample gate feedthrough/DC adjustments¹.

Bridge Drive Trims

The current switch bridge drive is trimmed first. Disconnect all 5 bridge drive related trims and apply a 5V, 1MHz, 10 to 15 nanosecond wide pulse at the circuit input. The paralleled “C” inverter output viewed at the 43Ω back termination’s undriven end should resemble Figure A1. Waveform edge times are fast but poorly controlled parasitic excursions risk corrupting the measurement noise floor and must be eliminated. Reconnect all 5 trims and adjust them according to their titles for Figure A2’s much improved presentation. There is some interaction between the adjustments but it is limited and favorable results are easily attained. Figure A2’s edge times are slightly slower than Figure A1’s, but still pass through the 1N5712 clamp level in <1 nanosecond.

Delay Determination and Compensation

Circuit delay related trims come next. Before making these measurements and adjustments, probe/oscilloscope channel-to-channel time skewing must be corrected. Figure A3 shows 40 picosecond time skew error with both channel probes connected to a 100 picosecond rise time pulse source². The error is corrected in Figure A4 by utilizing the oscilloscopes vertical amplifier variable delay feature (Tektronix 7A29, option 04, installed in a Tektronix 7104 mainframe). This correction permits high accuracy delay measurements to be made³.

Note 1. The trims require considerable care in instrumentation selection as well as thoughtful wideband probing and oscilloscope measurement technique. See Appendixes D through H for tutorial guidance before proceeding.

Note 2. See Appendix H, “Verifying Rise Time and Delay Measurement Integrity” for fast pulse source recommendations.

Note 3. This assumes the oscilloscope time base has been verified for accuracy. For recommendations, see Appendix H, “Verifying Rise Time and Delay Measurement Integrity”.

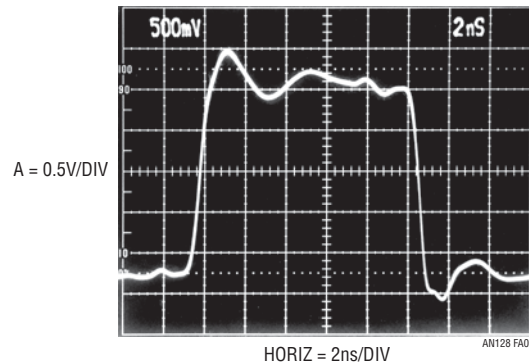


Figure A1. Untrimmed Current Switch Driver Response at 43Ω Back Termination Viewed in 1GHz, Real Time Bandwidth. Edge Times Are Fast, But Poorly Controlled. Undamped Waveform Artifacts Risk Corrupting Signal Path Noise Floor Via Radiation and Ground Current Disruption Induced Errors

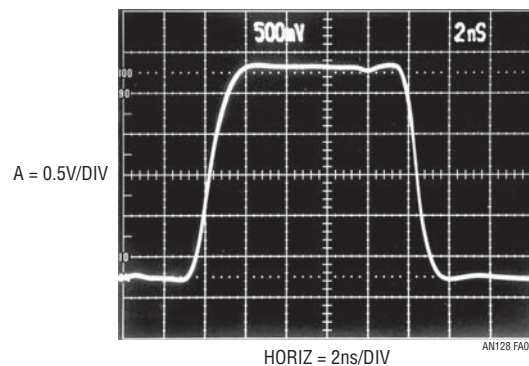


Figure A2. Trimmed Current Switch Driver Output at 43Ω Back Termination Passes Through 0.6V Diode Clamp Potential in <1 Nanosecond. AC Trims Promote Clean, Well Controlled Waveform

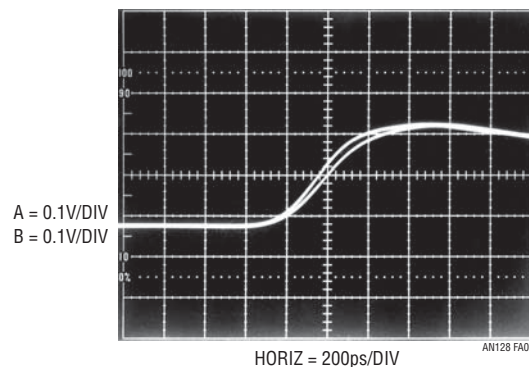


Figure A3. Probe-Oscilloscope Channel-to-Channel Timing Skew Measures 40 Picoseconds

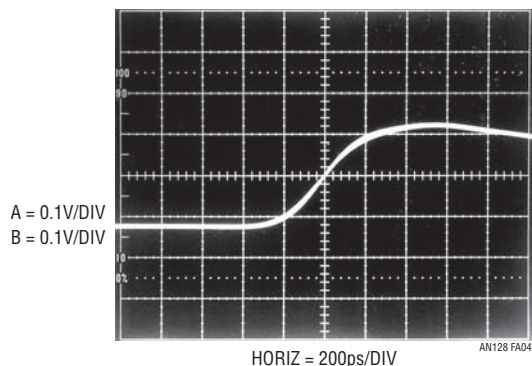


Figure A4. Corrected Probe/Channel/Skew Shows Nearly Identical Time and Amplitude Response

The settling time circuit utilizes an adjustable delay network to time correct the input pulse for delays in the signal-processing path. Typically, these delays introduce errors approaching 10 nanoseconds, so an accurate correction is required. Setting the delay trim involves observing the network’s input-output delay and adjusting for the appropriate time interval. Determining the “appropriate” time interval is somewhat more complex.

Referring to Figure 5, it is apparent that three delay measurements are of interest. The current switch driver to amplifier-under-test negative input, the amplifier-under-test output to circuit output and the sample gate multiplier delay. Figure A5 indicates 250 picoseconds delay from the current switch driver to the amplifier-under-test input. Figure A6 reveals 8.4 nanoseconds delay from the amplifier-under-test output to circuit output and Figure A7 shows sample gate multiplier delay of 2 nanoseconds. The measurements indicate a current switch driver-to-circuit output delay of 8.65 nanoseconds; the correction is implemented by adjusting the 1k trim in the “Signal Path Delay Compensation” network for that amount. Similarly, when the sampling ‘scope is used, the relevant delays are Figure A5 plus A6 minus Figure A7, a total of 6.65 nanoseconds. This factor is adjusted into the signal path delay compensation network when the sampling ‘scope-based measurement is taken.

The “Sample Gate Pulse Generator Path Delay Compensation” trim is less critical. The sole requirement is that it overlap the sample gate pulse generator’s delay. Setting the 1k potentiometer in the “A” inverter chain to 15 nanoseconds satisfies this criteria, completing the delay related trims.

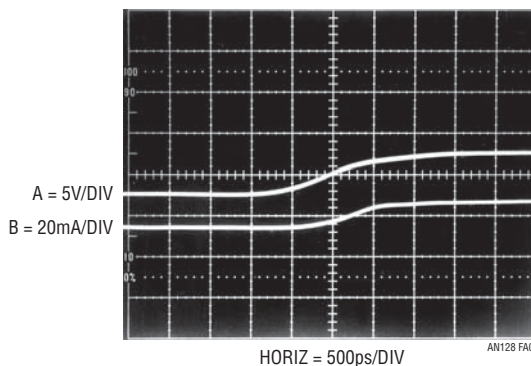


Figure A5. Current Switch Driver (Trace A) to Amplifier-Under-Test Negative Input (Trace B) Delay Is 250 Picoseconds

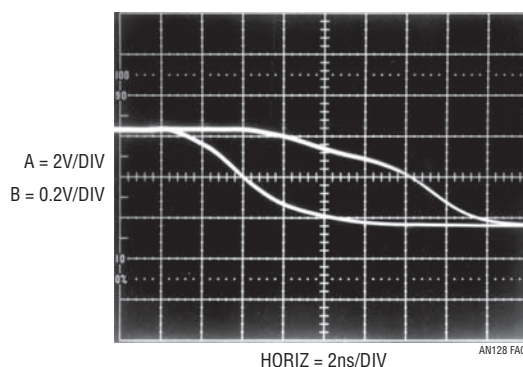


Figure A6. Amplifier-Under-Test (Trace A) to Circuit Output (Trace B) Delay Measures 8.4 Nanoseconds. Multiplier X Input Held at 1V DC for This Test

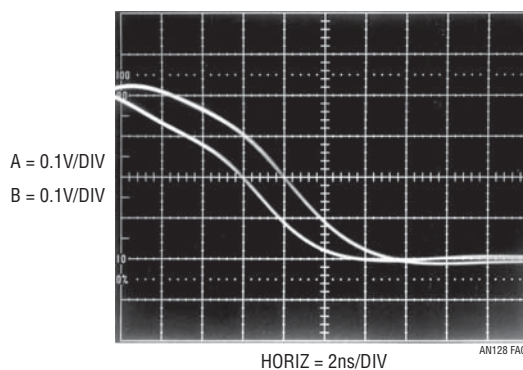


Figure A7. Multiplier Delay with X Input Held at 1V DC Measures 2ns

Sample Gate Pulse Purity Adjustment

The Q1 sample gate pulse edge shaping stage is adjusted for an optimized front corner, minimum rising edge time, pulse top smoothing and 1V amplitude with the indicated trims. The mildly interactive adjustments converge to

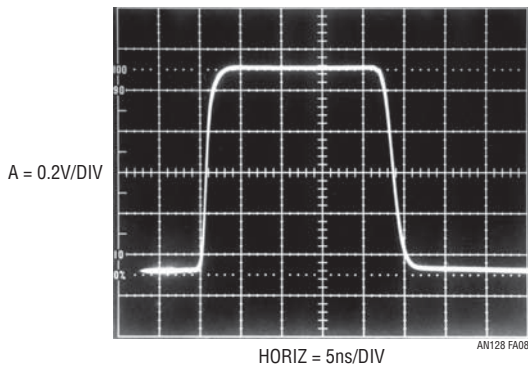


Figure A8. Sample Gate Pulse Characteristics, Controlled by Edge Shaping, Circuit Configuration and Transistor Choice, Are Kept Within Multiplier's 250MHz ($T_{RISE} = 1.4ns$) Bandwidth. Accurate, Low Feedthrough, Y Input Signal Path Switching Results

Figure A8's display, taken at the sample gate multiplier's X input. The pulse's 2 nanosecond rise time promotes rapid sample gate acquisition but remains within the multiplier's 250MHz ($T_{RISE} = 1.4ns$) bandwidth, assuring freedom from out-of-band parasitic responses. The clean, 1V amplitude pulse top provides calibrated, consistent multiplier output devoid of aberrations which would masquerade as settling signal artifacts. Pulse fall time is irrelevant; it is not germane to the measurement and its clean falling transition assures controlled multiplier turn-off, precluding off-screen excursions.

Sample Gate Path Optimization

The sample gate path adjustments are the final trims. First, put in 5V DC to the pulse generator input to lock the amplifier-under-test into its $-2.5V$ output state. Adjust the "settle node zero" trim for zero volts within 1mV at A1's output. Next, restore the pulsed circuit input, disconnect the settle node from A1 and ground A1's input with a 750Ω resistor. Figure A9 is typical of the resultant untrimmed response. Ideally, the circuit output (trace B) should be static during sample gate (trace A) switching. The photo reveals errors; correction requires trimming DC offset and dynamic feedthrough related residue. The DC errors are eliminated by adjusting the "X" and "Y" offset trims for a continuous trace B baseline regardless of trace A's sample gate pulse state. Additionally, set the output offset adjustment for minimum multiplier baseline offset voltage. Sample gate gain is set to unity by shutting off the input pulse generator, applying 5V DC to C2's "+" input

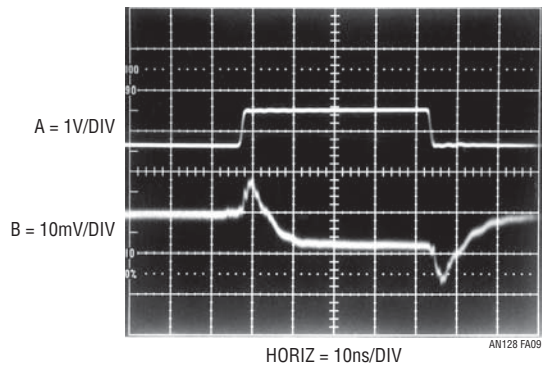


Figure A9. Settling Time Circuit's Output (Trace B) with Unadjusted Sample Gate Feedthrough and DC Offset. A1's Input Grounded for This Test. Excessive Switch Drive Feedthrough and Baseline Offset Are Present. Trace A Is Sample Gate Pulse

and forcing 1.00V DC at the previously inserted 750Ω resistor. Under these conditions, adjust "scale factor" for 1.00V DC output. After completing this step, remove the DC bias voltages and the 750Ω resistor, reconnect the settle node and restore the pulsed input.

Feedthrough compensation is accomplished via feedthrough "time phase" and "amplitude" trims. These adjustments set timing and amplitude of the feedthrough correction applied at the multiplier "Z" input. Optimal adjustment results in Figure A10's presentation. This photograph shows the DC and feedthrough trims dramatic effect on Figure A9's pre-trim errors⁴.

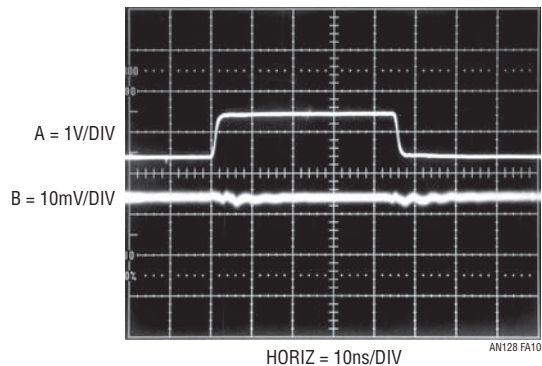


Figure A10. Settling Time Circuit's Output (Trace B) with Sample Gate Trimmed. As in Figure A9, A1's Input Is Grounded for This Test. Switch Drive Feedthrough and Baseline Offset Are Minimized. Trace A Is Sample Gate Pulse. Measurement Defines Circuit's 2mV Minimum Amplitude Resolution Limit

Note 4. The writer is not much for Hollywood's offerings, but does find drama in feedthrough trims.

Application Note 128

Measurement Limits and Uncertainties

Figure A10's post trim response includes a flat baseline and greatly attenuated feedthrough. The measurement defines the circuit's minimum amplitude resolution at 2mV. In another test, A1's input is disconnected from the settle node and biased at 20mV DC via a 750Ω resistor to simulate an infinitely fast settling amplifier. Figure A11 shows circuit output (trace B) settling within 5mV in 2 nanoseconds, arriving inside the 2mV baseline noise limit in 3.6 nanoseconds. This data, taken with sample gate conduction beginning immediately after the time corrected input (trace A) rises, defines the circuit's minimum time resolution limit. Uncertainties in the quoted time and amplitude resolution limits are primarily due to delay compensation limitations, noise and residual feedthrough. Considering likely delay and measurement errors, a time uncertainty of ±500 picoseconds and a 2mV resolution limit

is probably realistic. Noise averaging would not improve the amplitude resolution limit because it is imposed by feedthrough residue, a coherent term.

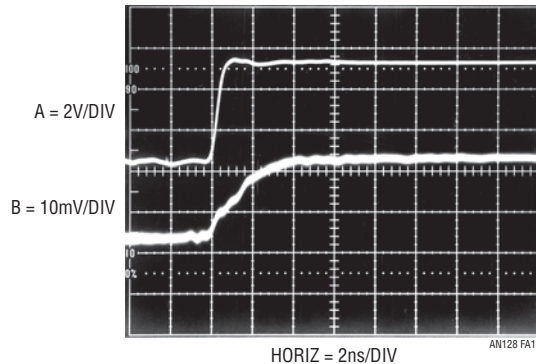


Figure A11. Circuit Response with 20mV DC Forced at A1's Input. Output (Trace B) Is within 5mV in 2ns, Arriving Inside 2mV Baseline Noise in 3.6ns. Measurement Defines Circuits Minimum Time Resolution Limit. Trace A Is Time Corrected Input Pulse

APPENDIX B

Practical Considerations for Amplifier Compensation

There are a number of practical considerations in compensating the amplifier to get fastest settling time. Our study begins by revisiting text Figure 1 (repeated here as Figure B1). Settling time components include delay, slew and ring times. Delay is due to propagation time through the amplifier and is a relatively small term. Slew time is set by the amplifier's maximum speed. Ring time defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. Once an amplifier has been chosen, only ring time is readily adjustable. Because slew time is usually the dominant lag, it is tempting to select the fastest slewing amplifier

available to obtain best settling. Unfortunately, fast slewing amplifiers usually have extended ring times, negating their brute force speed advantage. The penalty for raw speed is, invariably, prolonged ringing, which can only be damped with large compensation capacitors. Such compensation works, but results in protracted settling times. The key to good settling times is to choose an amplifier with the right balance of slew rate and recovery characteristics and compensate it properly. This is harder than it sounds because amplifier settling time cannot be predicted or extrapolated from any combination of data sheet specifications. It must be measured in the intended configuration. A number of terms combine to influence settling time. They include amplifier slew rate and AC dynamics, layout capacitance, source resistance and capacitance, and the compensation capacitor. These terms interact in a complex manner, making predictions hazardous¹. If the parasitics are eliminated and replaced with a pure resistive source, amplifier settling time is still not readily predictable. The parasitic impedance terms just make a difficult problem more messy. The only real handle available to deal with all this is the feedback compensation capacitor, C_F . C_F 's purpose is to roll off amplifier gain at the frequency that permits best dynamic response.

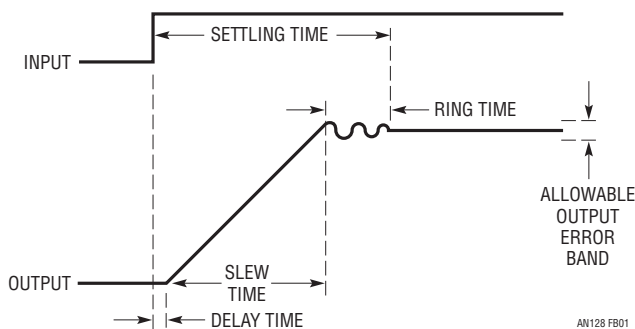


Figure B1. Settling Time Components Include Delay, Slew and Ring Times. For Given Components, Only Ring Time Is Readily Adjustable

Note 1. Spice aficionados take notice.

Best settling results when the compensation capacitor is selected to functionally compensate for all the above terms. Figure B2 shows results for an optimally selected feedback capacitor. Trace A is the time-corrected input pulse and trace B the amplifier's settle signal. The amplifier comes cleanly out of slew (sample gate opens just after the second vertical division) and settles to 5mV in 9 nanoseconds. Waveform signature is tight and nearly critically damped.

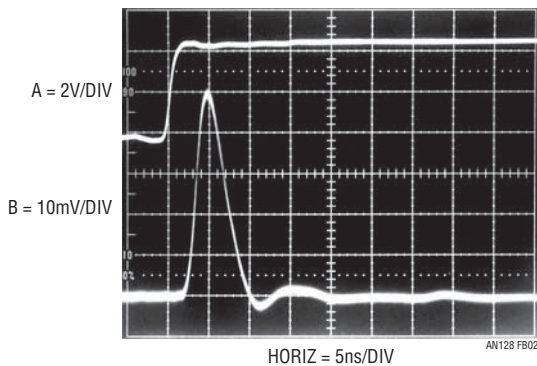


Figure B2. Optimized Compensation Capacitor Permits Tight Waveform Signature, Nearly Critically Damped Response and Fastest Settling Time. $T_{SETTLE} = 9ns$. Trace A Is Time Corrected Input Step, Trace B, the Settle Signal

In Figure B3, the feedback capacitor is too large. Settling is smooth, although overdamped; a 13 nanosecond penalty results in 22 nanosecond settling. Figure B4 has no feedback capacitor, causing severely underdamped response with resultant excessive ring time excursions. Settling time goes out to 33 nanoseconds. B5 improves on B4 by restoring the feedback capacitor, but the value is too small, resulting in an underdamped response requiring 27 nanoseconds to settle. Note that Figures B3 to B5 require vertical scale reduction to capture non-optimal response.

When feedback capacitors are individually trimmed for optimal response, the source, stray, amplifier and compensation capacitor tolerances are irrelevant. If individual trimming is not used, these tolerances must be considered to determine the feedback capacitor's production value. Ring time is affected by stray and source capacitance and output loading, as well as the feedback capacitor's value. The relationship is nonlinear, although some guidelines are

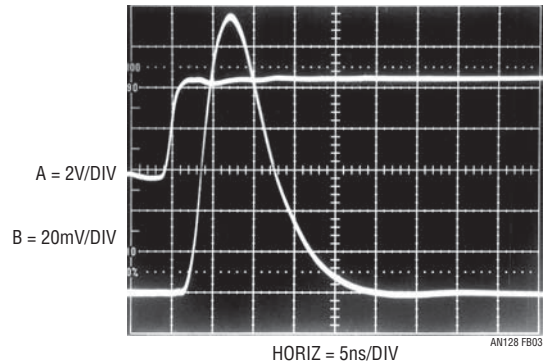


Figure B3. Overdamped Response Ensures Freedom from Ringing, Even with Component Variations in Production. Penalty Is Increased Settling Time. Note 2X Vertical Scale Change vs. Figure B2. $T_{SETTLE} = 22ns$. Trace Assignments Same as Previous Figure

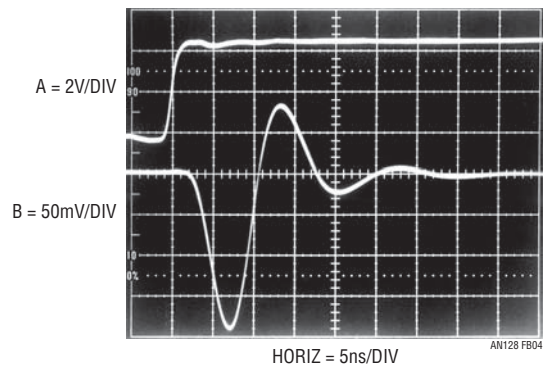


Figure B4. Severely Underdamped Response Due to No Feedback Capacitor. Note 5X Vertical Scale Change vs Figure B2. $T_{SETTLE} = 33ns$. Trace Assignments as in Figure B2

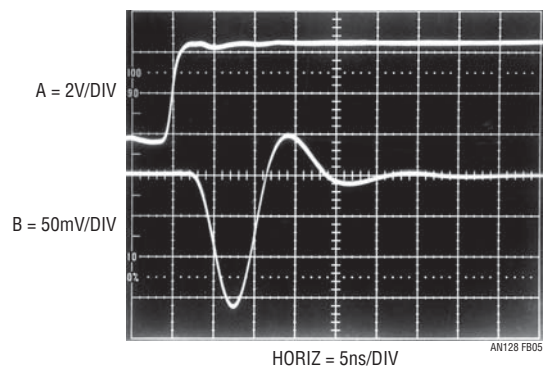


Figure B5. Underdamped Response Results from Undersized Capacitor. Component Tolerance Budgeting Will Prevent This Behavior. Note 5x Vertical Scale Change vs. Figure B2. $T_{SETTLE} = 27ns$. Trace Assignments as in Figure B2

possible. The stray and source terms can vary by $\pm 10\%$ and the feedback capacitor is typically a $\pm 5\%$ component². Additionally, amplifier slew rate has a significant tolerance, which is stated on the data sheet. To obtain a production feedback capacitor value, determine the optimum value by individual trimming with the production board layout (board layout parasitic capacitance counts too!). Then, factor in the worst-case percentage values for stray and source impedance terms, slew rate and feedback

capacitor tolerance. Add this information to the trimmed capacitors measured value to obtain the production value. This budgeting is perhaps unduly pessimistic (RMS error summing may be a defensible compromise), but will keep you out of trouble³.

Note 2. This assumes a resistive source. If the source has substantial parasitic capacitance (photodiode, DAC, etc.), this number can easily enlarge to $\pm 50\%$.

Note 3. The potential problems with RMS error summing become clear when sitting in an airliner that is landing in a snowstorm.

APPENDIX C

Evaluating Oscilloscope Overdrive Performance

The sampling based settling time circuit is heavily oriented towards preventing overdrive to the monitoring oscilloscope. This is done to avoid overdriving the oscilloscope. Oscilloscope recovery from overdrive is a grey area and almost never specified. How long must one wait after an overdrive before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overdrive, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overdrive varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100x overload at 0.005V/DIV may be very different than at 0.1V/DIV. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overdrive must be approached with caution.

Why do most oscilloscopes have so much trouble recovering from overdrive? The answer to this question requires some study of the three basic oscilloscope types' vertical path. The types include analog (Figure C1A), digital (Figure C1B) and classical sampling (Figure C1C) oscilloscopes. Analog and digital 'scopes are susceptible to overdrive. The classical sampling 'scope is the only architecture that is inherently immune to overdrive.

An analog oscilloscope (Figure C1A) is a real time, continuous linear system¹. The input is applied to an attenuator, which is unloaded by a wideband buffer. The vertical preamp provides gain, and drives the trigger pick-off, delay line and the vertical output amplifier. The attenuator and delay line

are passive elements and require little comment although they can display reactive behavior at speed and resolution extremes. The buffer, preamp and vertical output amplifier are complex linear gain blocks, each with dynamic operating range restrictions. Additionally, the operating point of each block may be set by inherent circuit balance, low frequency stabilization paths or both. When the input is overdriven, one or more of these stages may saturate, forcing internal nodes and components to abnormal operating points and temperatures. When the overload ceases, full recovery of the electronic and thermal time constants may require surprising lengths of time².

The digital sampling oscilloscope (Figure C1B) eliminates the vertical output amplifier, but has an attenuator buffer and amplifiers ahead of the A/D converter. Because of this, it is similarly susceptible to overdrive recovery problems.

The classical sampling oscilloscope is unique. Its nature of operation makes it inherently immune to overload. Figure C1C shows why. The sampling occurs before any gain is taken in the system. Unlike Figure C1B's digitally sampled 'scope, the input is fully passive to the sampling point. Additionally, the output is fed back to the sampling bridge, maintaining its operating point over a very wide range of inputs. The dynamic swing available to maintain the bridge output is large and easily accommodates a wide range of oscilloscope inputs. Because of all this, the amplifiers in this instrument do not see overload, even at 1000x overdrives, and there is no recovery problem. Additional immunity derives from the instrument's relatively slow

Note 1. Ergo, the Real Thing. Hopelessly bigoted residents of this locale mourn the passing of the analog 'scope era and frantically hoard every instrument they can find.

Note 2. Some discussion of input overdrive effects in analog oscilloscope circuitry is found in Reference 17.

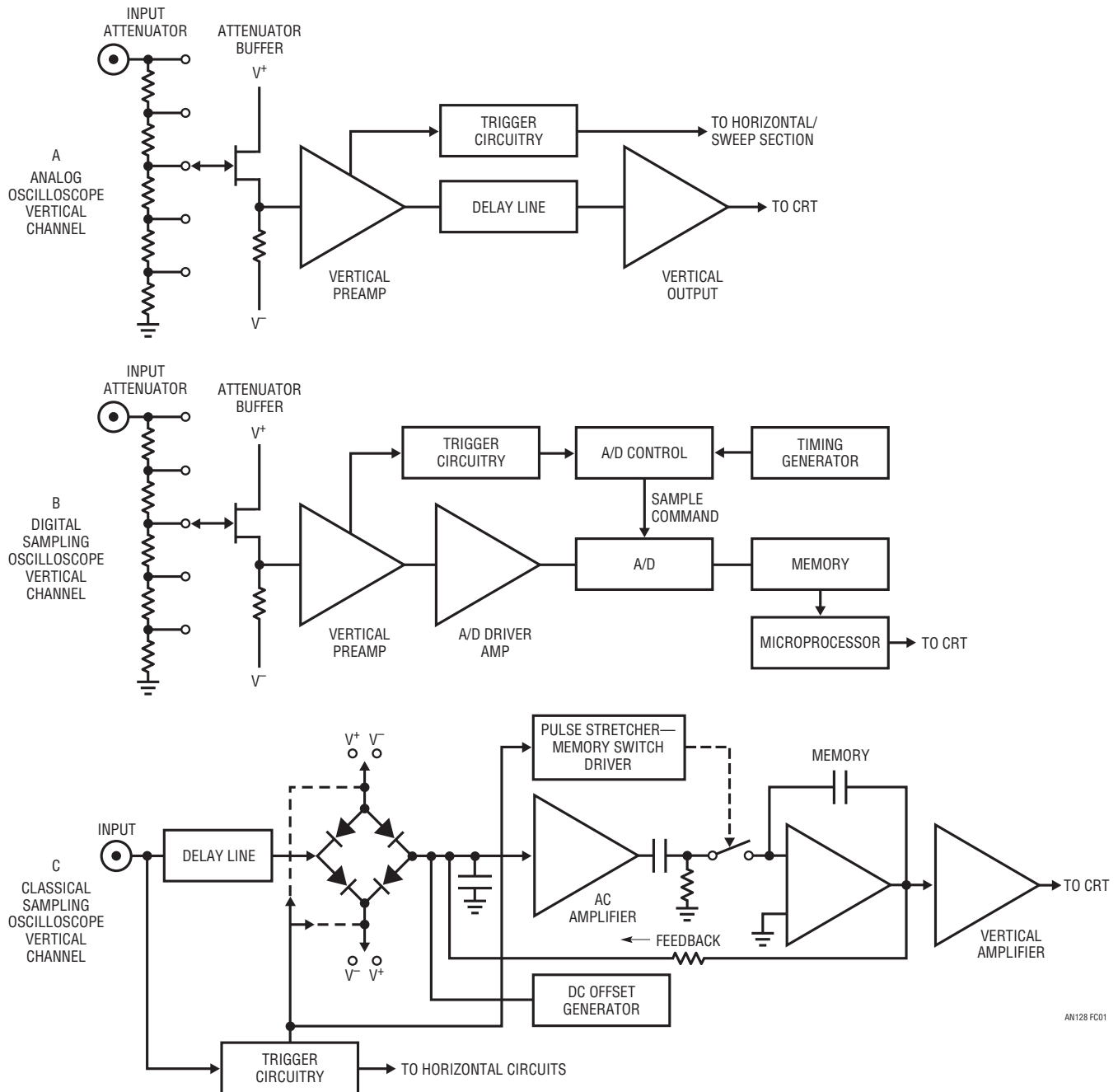


Figure C1. Simplified Vertical Channel Diagrams for Different Type Oscilloscopes. Only the Classical Sampling 'Scope (C) Has Inherent Overdrive Immunity. Offset Generator Allows Viewing Small Signals Riding On Large Excursions

sample rate—even if the amplifiers were overloaded, they would have plenty of time to recover between samples³.

The designers of classical sampling 'scopes capitalized on the overdrive immunity by including variable DC offset generators to bias the feedback loop (see Figure C1C, lower right). This permits the user to offset a large input, so small amplitude activity on top of the signal can be accurately

observed. This is ideal for, among other things, settling time measurements. Unfortunately, classical sampling oscilloscopes are no longer manufactured, so if you have one, take care of it⁴!

Note 3. Additional information and detailed treatment of classical sampling oscilloscope operation appears in References 23-26 and 29-31.

Note 4. Modern variants of the classical architecture (e.g., Tektronix 11801B) may provide similar capability, although we have not tried them.

Application Note 128

Although analog and digital oscilloscopes are susceptible to overdrive, many types can tolerate some degree of this abuse. The early portion of this appendix stressed that measurements involving oscilloscope overdrive must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity that eliminates all off-screen activity. Figure C2 shows the display. The lower right hand portion

is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure C3) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure C4, gain has been further increased, and all the features of Figure C3 are amplified

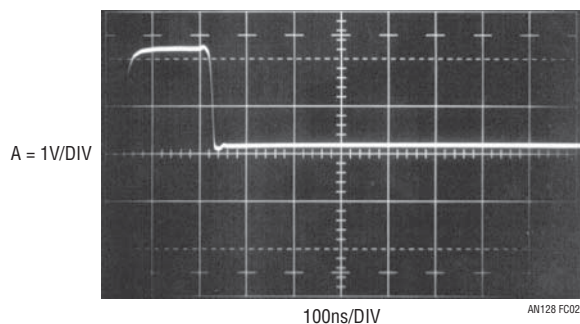


Figure C2

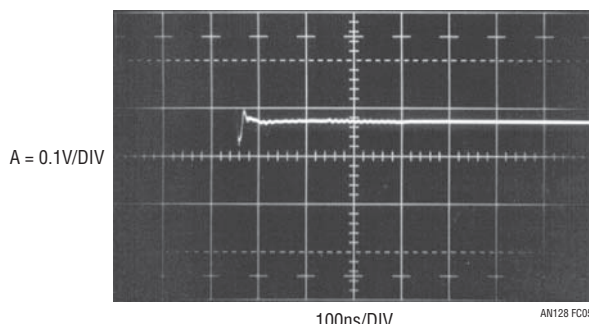


Figure C5

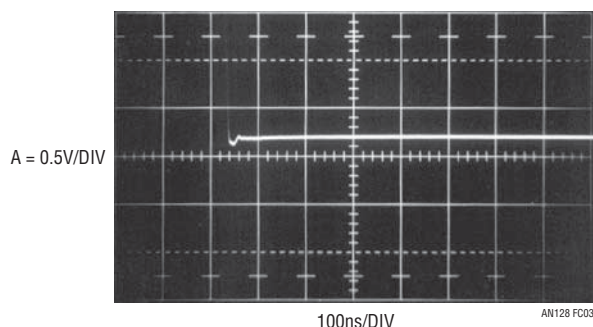


Figure C3

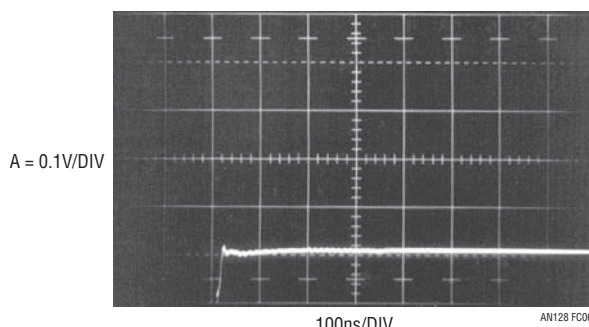


Figure C6

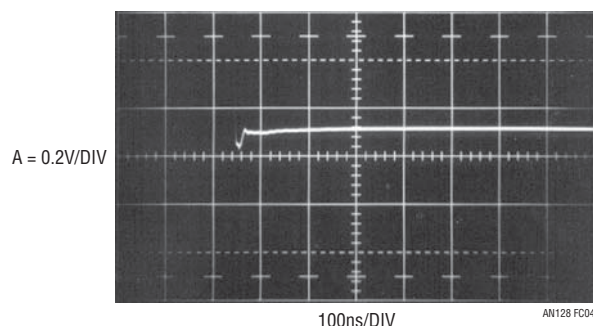


Figure C4

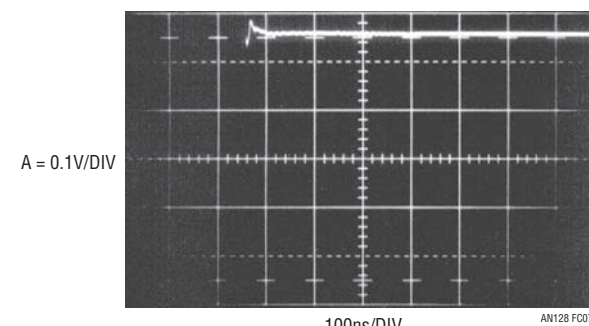


Figure C7

Figure C2 to C7. The Overdrive Limit Is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure C5 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure C4. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure C6 the gain remains the same

but the vertical position knob has been used to reposition the display at the screen's bottom⁵. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure C7). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

Note 5. Knobs (derived from Middle English, “knobbe”, akin to Middle Low German, “knubbe”), cylindrically shaped, finger rotatable panel controls for controlling instrument functions, were utilized by the ancients.

APPENDIX D

ABOUT Z_0 PROBES

When to Roll Your Own and When to Pay the Money

Z_0 (e.g. low impedance) probes provide the most faithful high speed probing mechanism available for low source impedances. Their sub-picofarad input capacitance and near ideal transmission characteristic make them the first choice for high bandwidth oscilloscope measurement. Their deceptively simple operation invites “do-it-yourself” construction but numerous subtleties mandate difficulty for prospective constructors. Arcane parasitic effects introduce errors as speed increases beyond about 100MHz ($t_{RISE} = 3.5ns$). The selection and integration of probe materials and the probes physical incarnation require extreme care to obtain high fidelity at high speed. Additionally, the probe must include some form of adjustment to compensate small, residual parasitics. Finally, true coaxiality must be maintained when fixturing the probe at the measurement point, implying a high grade, readily disconnectable, coaxial connection capability.

Figure D1 shows that a Z_0 probe is basically a voltage divided input 50Ω transmission line. If $R1$ equals 450Ω , 10x attenuation and 500Ω input resistance result. $R1$ of 4950Ω causes a 100x attenuation with 5k input resistance. The 50Ω line theoretically constitutes a distortionless transmission environment. The apparent simplicity seemingly permits “do-it-yourself” construction but this section's remaining figures demonstrate a need for caution.

Figure D2 establishes a fidelity reference by measuring a clean 700ps rise time pulse using a 50Ω line terminated



Figure D1. Conceptual 500Ω , “ Z_0 ”, 10x Oscilloscope Probe. If $R1 = 4950\Omega$, 5k Input Resistance with 100x Signal Attenuation Results. Terminated Into 50Ω , Probe Theoretically Constitutes Distortionless Transmission Line. “Do-It-Yourself” Probes Suffer Uncompensated Parasitics, Causing Unfaithful Response Above $\approx 100MHz$ ($t_{RISE} = 3.5ns$)

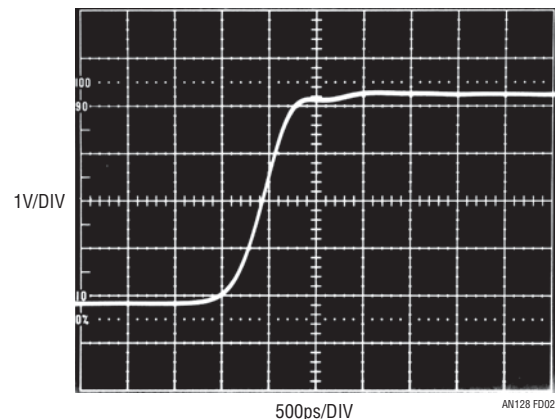


Figure D2. 700ps Rise Time Pulse Observed via 50Ω Line and 10x Coaxial Attenuator Has Good Pulse Edge Fidelity with Controlled Post-Transition Events

via a 10x coaxial attenuator—no probe is employed. The waveform is singularly clean and crisp with minimal edge and post-transition aberrations. Figure D3 depicts the same pulse with a commercially produced 10x Z_0 probe in use. The probe is faithful and there is barely discernible error in the presentation. Photos D4 and D5, taken with

an128f

Application Note 128

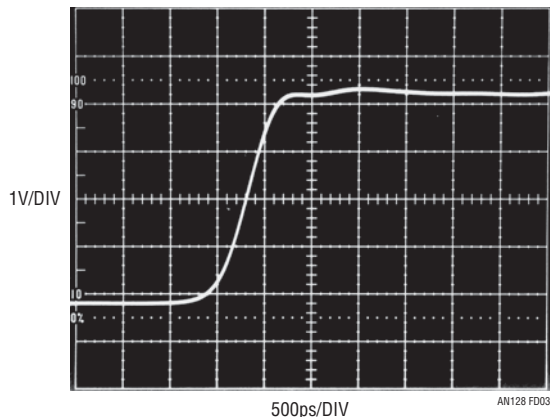


Figure D3. Figure D2's Pulse Viewed with Tektronix 10x, Z_0 500 Ω Probe (P-6056) Introduces Barely Discernible Error

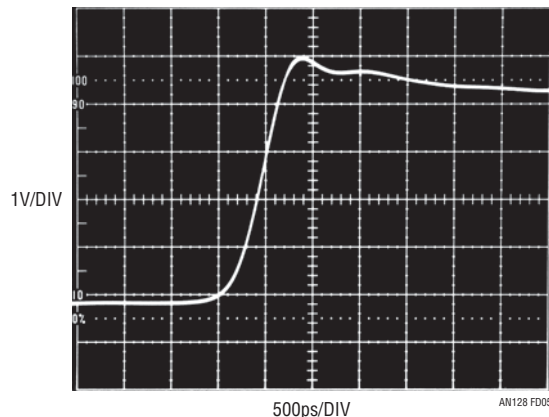


Figure D5. "Do-It-Yourself" Z_0 Probe #2 Has Overshoot, Again Likely Due to Resistor/Cable Parasitic Terms or Incomplete Coaxiality. Lesson: At These Speeds, Don't "Do-It-Yourself"

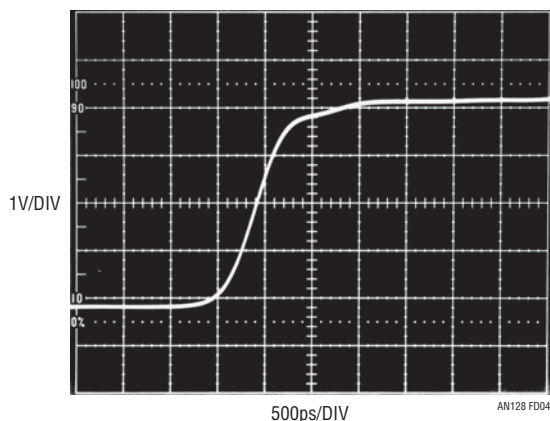


Figure D4. "Do-It-Yourself" Z_0 Probe #1 Introduces Pulse Corner Rounding, Likely Due to Resistor/Cable Parasitic Terms or Incomplete Coaxiality. "Do-It-Yourself" Z_0 Probes Typically Manifest This Type of Error at Rise Times ≤ 2 ns

two separately constructed "do-it-yourself" Z_0 probes, show errors. In D4, Probe #1 introduces pulse front corner rounding; Probe #2 in D5 causes pronounced corner peaking. In each case, some combination of resistor/cable parasitics and incomplete coaxiality are likely responsible for the errors. In general, "do-it-yourself" Z_0 probes cause these types of errors beyond about 100MHz (t_{RISE} 3.5ns). At higher speeds, if waveform fidelity is critical, it's best to pay the money. For additional terror and wisdom along these lines, see pg. 2-4 \rightarrow 2-8 of Reference 30 and Reference 35. Both are excellent, informative and, hopefully, sobering to still undaunted do-it-yourselfers.

APPENDIX E

Connections, Cables, Adapters, Attenuators, Probes and Picoseconds

Subnanosecond rise time signal paths must be considered as a transmission line. Connections, cables, adapters, attenuators and probes represent discontinuities in this transmission line, deleteriously affecting its ability to faithfully transmit desired signal. The degree of signal corruption contributed by a given element varies with its deviation from the transmission lines nominal impedance. The practical result of such introduced aberrations is degradation of pulse rise time, fidelity, or both. Accordingly, introduction of elements or connections to the signal path should be minimized and necessary connections and elements must be high grade components. Any form of connector, cable, attenuator or probe must be fully specified for high frequency use. Familiar BNC hardware becomes lossy at rise times much faster than 350ps. SMA components are preferred for the rise times described in the text. Additionally, cable should be 50Ω “hard line” or, at least, Teflon-based coaxial cable fully specified for high frequency operation. Optimal connection practice eliminates any cable by coupling the signal output *directly* to the measurement input.

Mixing signal path hardware types via adapters (e.g. BNC/SMA) should be avoided. Adapters introduce significant parasitics, resulting in reflections, rise time degradation, resonances and other degrading behavior. Similarly, oscilloscope connections should be made directly to the instrument’s 50Ω inputs, avoiding probes. If probes must be used, their introduction to the signal path mandates attention to their connection mechanism and high frequency compensation. Passive Z_0 types, commercially available in 500Ω (10x) and 5kΩ (100x) impedances, have input capacitance below 1pf¹. Any such probe must be carefully frequency compensated before use or misrepresented measurement will result. Inserting the probe into the signal path necessitates some form of signal pick-off which nominally does not influence signal transmission. In practice, some amount of disturbance must be tolerated and its effect on measurement results evaluated. High quality signal pick-offs always specify insertion loss, corruption factors and probe output scale factor.

The preceding emphasizes vigilance in designing and maintaining a signal path. Skepticism, tempered by enlightenment, is a useful tool when constructing a signal path and no amount of hope is as effective as preparation and directed experimentation.

Note 1. See Appendix D, “About Z_0 Probes”.

APPENDIX F

Breadboarding, Layout and Connection Techniques

The measurement results presented in this publication required painstaking care in breadboarding, layout and connection techniques. Nanosecond domain, high resolution measurement does not tolerate cavalier laboratory attitude. The oscilloscope photographs presented, devoid of ringing, hops, spikes and similar aberrations, are the result of a careful breadboarding exercise. The breadboard required considerable experimentation before obtaining a noise/uncertainty floor worthy of the measurement.

Ohm's Law

It is worth considering that Ohm's law is a key to successful layout¹. Consider that 10mA running through 1 Ω generates 10mV—twice the measurement limit! Now, run that current at 1 nanosecond rise times (\approx 350MHz) and the need for layout care becomes clear. A paramount concern is disposal of circuit ground return current and disposition of current in the ground plane. The impedance of the ground plane between any two points is *not* zero, particularly at nanosecond speeds. This is why the entry point and flow of “dirty” ground returns must be carefully placed within the grounding system.

A good example of the importance of grounding management involves delivering the input pulse to the breadboard. The pulse generator's 50 Ω termination *must* be an in-line coaxial type. This ensures that pulse generator return current circulates in a tight local loop at the terminator, and does not mix into the signal plane. It is worth mentioning that, because of the nanosecond speeds involved, inductive parasitics may introduce more error than resistive terms. This often necessitates using flat wire braid for connections to minimize parasitic inductive and skin effect-based

losses. Every ground return and signal connection in the entire circuit must be evaluated with these concerns in mind. A paranoiac mindset is quite useful.

Shielding

The most obvious way to handle radiation-induced errors is shielding. Determining where shields are required should come *after* considering what layout will minimize their necessity. Often, grounding requirements conflict with minimizing radiation effects, precluding maintaining distance between sensitive points. Shielding is usually an effective compromise in such situations.

A similar approach to ground path integrity should be pursued with radiation management. Consider what points are likely to radiate, and try to lay them out at a distance from sensitive nodes. When in doubt about odd effects, experiment with shield placement and note results, iterating towards favorable performance². *Above all, never rely on filtering or measurement bandwidth limiting to “get rid of” undesired signals whose origin is not fully understood.* This is not only intellectually dishonest, but may produce wholly invalid measurement “results,” even if they look pretty on the oscilloscope.

Connections

All signal connections to the breadboard must be coaxial. Ground wires used with oscilloscope probes are forbidden. A 1" ground lead used with a scope probe can easily generate large amounts of observed “noise” and seemingly inexplicable waveforms. Use coaxially mounting probe tip adapters³!

Note 1. I do not wax pedantic here. My guilt in this matter runs deep.

Note 2. After it works, you can figure out why.

Note 3. See Reference 34 for additional nagging along these lines.

APPENDIX G

How Much Bandwidth is Enough?

Accurate wideband oscilloscope measurements require bandwidth. A good question is just how much is needed. A classic guideline is that “end-to-end” measurement system rise time is equal to the root-sum-square of the system’s individual component’s rise times. The simplest case is two components; a signal source and an oscilloscope.

Figure G1’s plot of $\sqrt{\text{signal}^2 + \text{oscilloscope}^2}$ rise time versus error is illuminating. The figure plots signal-to-oscilloscope rise time ratio versus observed rise time (rise time is bandwidth restated in the time domain, where:

$$\text{Rise Time (ns)} = \frac{350}{\text{Bandwidth (MHz)}}$$

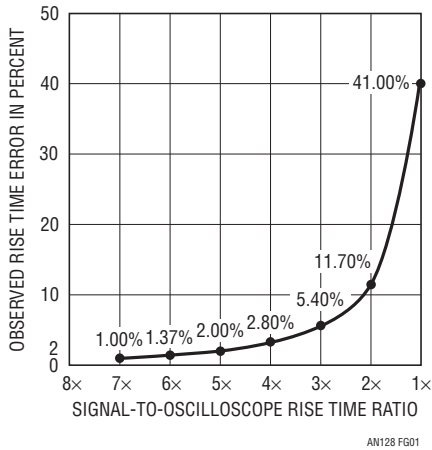


Figure G1. Oscilloscope Rise Time Effect on Rise Time Measurement Accuracy. Measurement Error Rises Rapidly as Signal-to-Oscilloscope Rise Time Ratio Approaches Unity. Data, Based on Root-Sum-Square Relationship, Does Not Include Passive Probe, Which Does Not Follow Root-Sum-Square Law

The curve shows that an oscilloscope 3 to 4 times faster than the input signal rise time is required for measurement accuracy inside about 5%. This is why trying to measure a 1ns rise time pulse with a 350MHz oscilloscope ($t_{\text{RISE}} = 1\text{ns}$) leads to erroneous conclusions. The curve indicates a monstrous 41% error. Note that this curve does not include the effects of passive probes or cables connecting the signal to the oscilloscope. Probes do not necessarily follow root-sum-square law and must be carefully chosen and applied for a given measurement. For details, see Appendix D. Figure G2, included for reference, gives 10 cardinal points of rise time/bandwidth equivalency between 1MHz and 5GHz.

RISE TIME	BANDWIDTH
70ps	5GHz
350ps	1GHz
700ps	500MHz
1ns	350MHz
2.33ns	150MHz
3.5ns	100MHz
7ns	50MHz
35ns	10MHz
70ns	5MHz
350ns	1MHz

Figure G2. Some Cardinal Points of Rise Time/Bandwidth Equivalency. Data Is Based on Text’s Rise Time/Bandwidth Formula

Application Note 128

APPENDIX H

Verifying Rise Time and Delay Measurement Integrity

Any measurement requires the experimenter to insure measurement confidence. Some form of calibration check is always in order. High speed time domain measurement is particularly prone to error and various techniques can promote measurement integrity.

Figure H1's battery-powered 200MHz crystal oscillator produces 5ns markers, useful for verifying oscilloscope time base accuracy. A single 1.5V AA cell supplies the LTC3400 boost regulator, which produces 5V to run the oscillator. Oscillator output is delivered to the 50Ω load via a peaked attenuation network. This provides well defined 5ns markers (Figure H2) and prevents overdriving low level sampling oscilloscope inputs.

Once time base accuracy is confirmed it is necessary to check rise time. The lumped signal path rise time, including

attenuators, connections, cables, probes, oscilloscope and anything else, should be included in this measurement. Such "end-to-end" rise time checking is an effective way to promote meaningful results. A guideline for insuring accuracy is to have 4x faster measurement path rise time than the rise time of interest. Thus, verifying the sample gate multipliers 250MHz (1.4ns risetime) bandwidth requires 1GHz ($t_{RISE} = 350ps$) oscilloscope bandwidth. Verifying the oscilloscope's 350 picosecond rise time, in turn, necessitates a 90 picosecond rise time step to ensure the 'scope is driven to its rise time limit. Figure H3 lists some very fast edge generators for rise time checking¹. The Tektronix 284, specified at 70ps rise time, was used to check 'scope rise time. Figure H4 indicates 350ps rise time, promoting measurement confidence.

Note 1. This is a fairly exotic group, but equipment of this caliber is necessary for rise time verification.

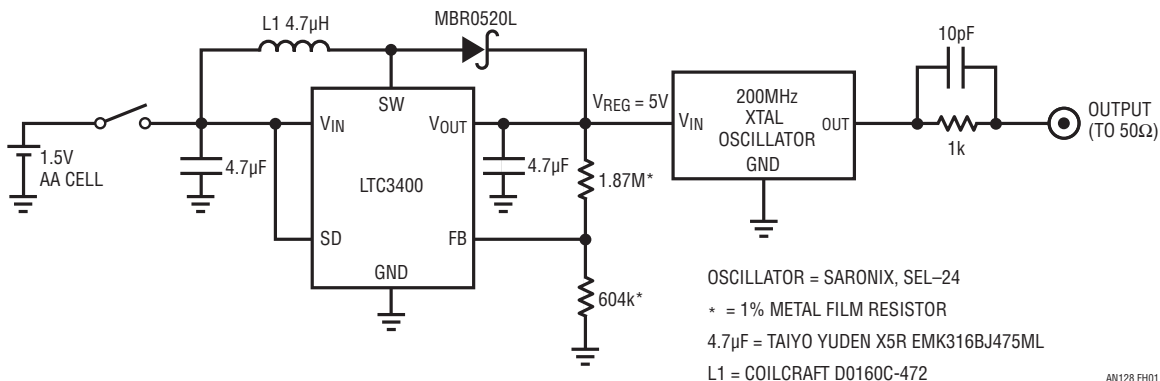


Figure H1. 1.5V Powered, 200MHz Crystal Oscillator Provides 5ns Time Markers. 1.5V to 5V Switching Regulator Powers Oscillator

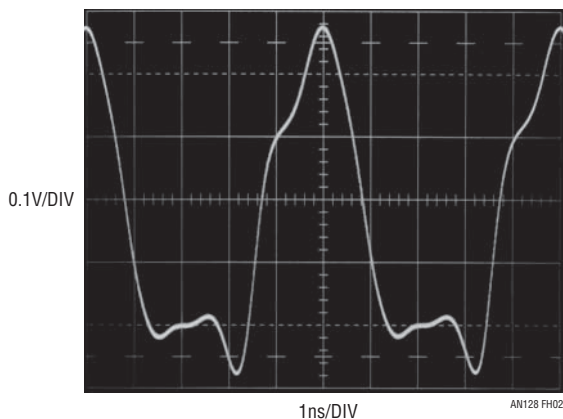


Figure H2. Time Mark Generator Output Terminated into 50Ω. Peaked Waveform Is Optimal for Verifying Time Base Calibration

MANUFACTURER	MODEL NUMBER	RISE TIME	AMPLITUDE	AVAILABILITY	COMMENTS
Avtech	AVP2S	40ps	0V to 2V	Current Production	Free Running or Triggered Operation, 0MHz to 1MHz
Hewlett-Packard	213B	100ps	≈175mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Hewlett-Packard	1105A/1108A	60ps	≈200mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Hewlett-Packard	1105A/1106A	20ps	≈200mV	Secondary Market	Free Running or Triggered Operation to 100kHz
Picosecond Pulse Labs	TD1110C/TD1107C	20ps	≈230mV	Current Production	Similar to Discontinued HP1105/1106/8A. See above.
Stanford Research Systems	DG535 OPT 04A	100ps	0.5V to 2V	Current Production	Must be Driven with Stand-alone Pulse Generator
Tektronix	284	70ps	≈200mV	Secondary Market	50kHz Repetition Rate. Pre-trigger 5ns, 75ns or 150ns Before Main Output. Calibrated 100MHz and 1GHz Sine Wave Auxiliary Outputs.
Tektronix	111	500ps	≈±10V	Secondary Market	10kHz to 100kHz Repetition Rate. Positive or Negative Outputs. 30ns to 250ns Pre-trigger Output. External Trigger Input. Pulse Width Set with Charge Lines
Tektronix	067-0513-00	30ps	≈400mV	Secondary Market	60ns Pre-trigger Output. 100kHz Repetition Rate
Tektronix	109	250ps	0V to ±55V	Secondary Market	≈600Hz Repetition Rate (High Pressure Hg Reed Relay Based). Positive or Negative Outputs. Pulse Width Set by Charge Lines

Figure H3. Picosecond Edge Generators Suitable for Rise Time Verification. Considerations Include Speeds, Features and Availability

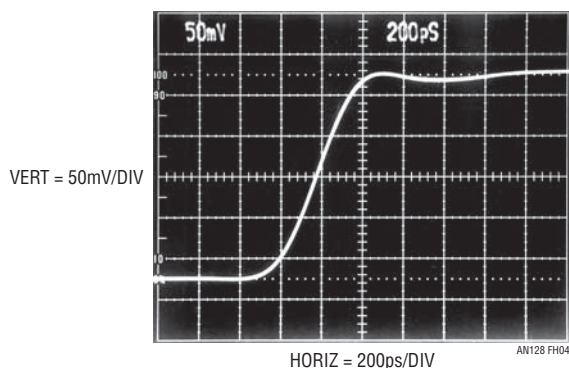


Figure H4. 70 Picosecond Edge Drives Oscilloscope to its 350 Picosecond Rise Time Limit, Verifying 1GHz Bandwidth



Contemplating Nanosecond Settling Time Measurement
at Punta Cana, Dominican Republic, where this
Application Note was written

An Introduction to Acoustic Thermometry

An Air Filled Olive Jar Teaches Signal Conditioning

Jim Williams and Omar Sanchez-Felipe

Introduction

We occasionally lecture to university engineering students. A goal of these lectures is to present technology in a novel, even charming, way. This hopefully entices the student towards the topic; an aroused curiosity is fertile ground for education. One such lecture investigates acoustic thermometry as an example of signal conditioning techniques. This subject has drawn enough interest that it is presented here for wider dissemination and as supplementary material for future acoustic thermometry lectures.

Acoustic Thermometry

Acoustic thermometry is an arcane, elegant temperature measurement technique. It utilizes sound's temperature dependent transit time in a medium to measure temperature. The medium may be a solid, liquid or gas. Acoustic thermometers function in environments that conventional sensors cannot tolerate. Examples include extreme temperatures, applications where the sensor would be subjected to destructive physical abuse and nuclear reactors. Gas path acoustic thermometers respond very quickly to temperature changes because they have essentially no thermal mass or lag. An acoustic thermometer's "body"

is the measurand. Additionally, an acoustic thermometer's reported "temperature" represents the total measurement path transit time as opposed to a conventional sensor's single point determination. As such, an acoustic thermometer is blind to temperature variations within the measurement path. It reports the measurement path's delay as its "temperature," whether or not the path is iso-thermal.

A pleasant surprise is that the sonic transit time in a gas path thermometer is almost entirely insensitive to pressure and humidity, leaving temperature as the sole determinant. Additionally, sonic speed in air varies predictably as the square root of temperature.

Practical Considerations

A practical acoustic thermometer demonstration begins with selecting a sonic transducer and a dimensionally stable measurement path. A wideband ultrasonic transducer is desirable to promote fast, low jitter, hi-fidelity response free of resonances and other parasitics. The electrostatic type specified in Figure 1 meets these requirements. A single transducer serves as both transmitter and receiver.

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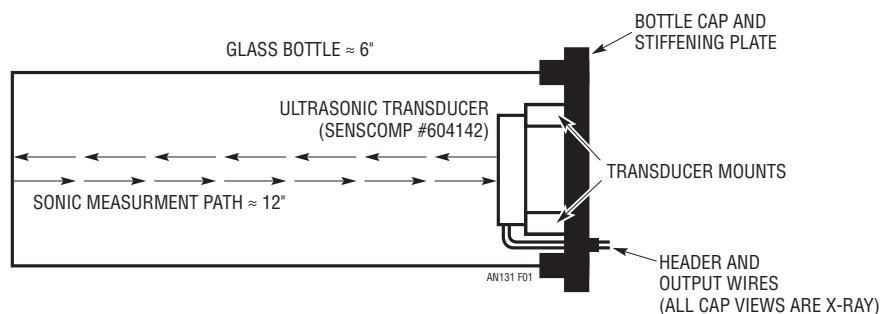


Figure 1. Ultrasonic Transducer Rigidly Mounts Within Stiffened Cap Affixed to Bottle. Structure Defines Fixed Length Measurement Path Essentially Independent of Physical Variables. Sonic Transit Time at 75°F ≈ 900µs with ≈1µs/°F Variation

Application Note 131

The device is rigidly mounted within the stiffened metal cap of a glass enclosure, promoting measurement path dimensional stability. The enclosure and its cap are conveniently furnished by a bottle of “Reese” brand “Cannonball” olives (Figure 2). After removing the olives and their residue, the bottle and cap are baked out at 100°C prior to joining. The transducer leads pass through the cap via a coaxial header. This arrangement, along with the glass enclosure’s relatively small thermal expansion coefficient, yields a path distance stable against temperature, pressure and mechanically induced changes. Path length, including enclosure bottom bounce and return to transducer, is about 12". This sets a two-way trip time of around 900µs (speed of sound in air ≈ 1.1 ft/ms). At 75°F, this path’s temperature dependent variation is approximately 1µs/°F. A desired 0.1°F resolution mandates mechanical and electronic induced path length uncertainty inside 100ns; approximately 0.001" dimensional stability referred to the 12" path length. Considering likely error sources, this is a realistic goal.



Figure 2. Photograph Details Cap Assembly, Partially Views Glass Enclosed Measurement Path. Ultrasonic Transducer Visible Within Cap. Stiffening Plate, Bonded to Cap Top, Prevents Ambient Pressure or Temperature Changes from Deforming Thin Metal Cap, Promoting Measurement Path Length Stability. Coaxial Header Provides Transducer Connections

Overview

Figure 3 is a simplified overview of the acoustic thermometer. The transducer, which can be considered a capacitor, is biased at 150V_{DC}. The start pulse clock drives it with a short impulse, launching an ultrasonic event into the measurement path. Simultaneously, the width decoding flip-flop is set high. The sonic impulse bounces off the enclosure bottom, returns to the transducer and impinges on it. The resulting minuscule mechanical displacement causes the transducer to give up charge ($Q = \Delta C \cdot V$), which appears as a voltage at the receiver amplifier input. The trigger converts the amplifier’s output excursion into a logic compatible level which resets the flip-flop. The flip-flop output width represents the measurement path’s temperature dependent sonic transit time. The microprocessor, equipped with the measurement path’s temperature/delay calibration constants, calculates the temperature and supplies this information to the display.¹ The start pulse generator has a second output which gates the trigger output off during nearly the entire measurement cycle. The trigger output only passes during the immediate time vicinity when a return pulse is expected. This discriminates against unwanted sonic events originating outside the measurement path, eliminating false triggers. A second gating, sourced from the width decoding flip-flop, shuts down the 150V bias supply switching regulator during the measuring interval. Return pulse amplitude is under 2mV at the transducer and the high gain, wideband receiver amplifier is vulnerable to parasitic inputs. Shutting down the 150V bias supply during the measurement prevents its switching harmonics from corrupting the amplifier. Figure 4 describes the system’s event sequence. A measurement cycle begins with a start pulse (A) driving the transducer and setting the flip-flop (B) high. After the sonic impulse’s transit time, the amplifier responds (C, diagram right), tripping the trigger (D, diagram right) which resets the flip-flop. Gate signals (E and F) protect the trigger from unwanted sonic events and start pulse artifacts and shut off the high voltage regulator during measurement.

Note 1. See Appendix A, “Measurement Path Calibration” for details on determining calibration constants.

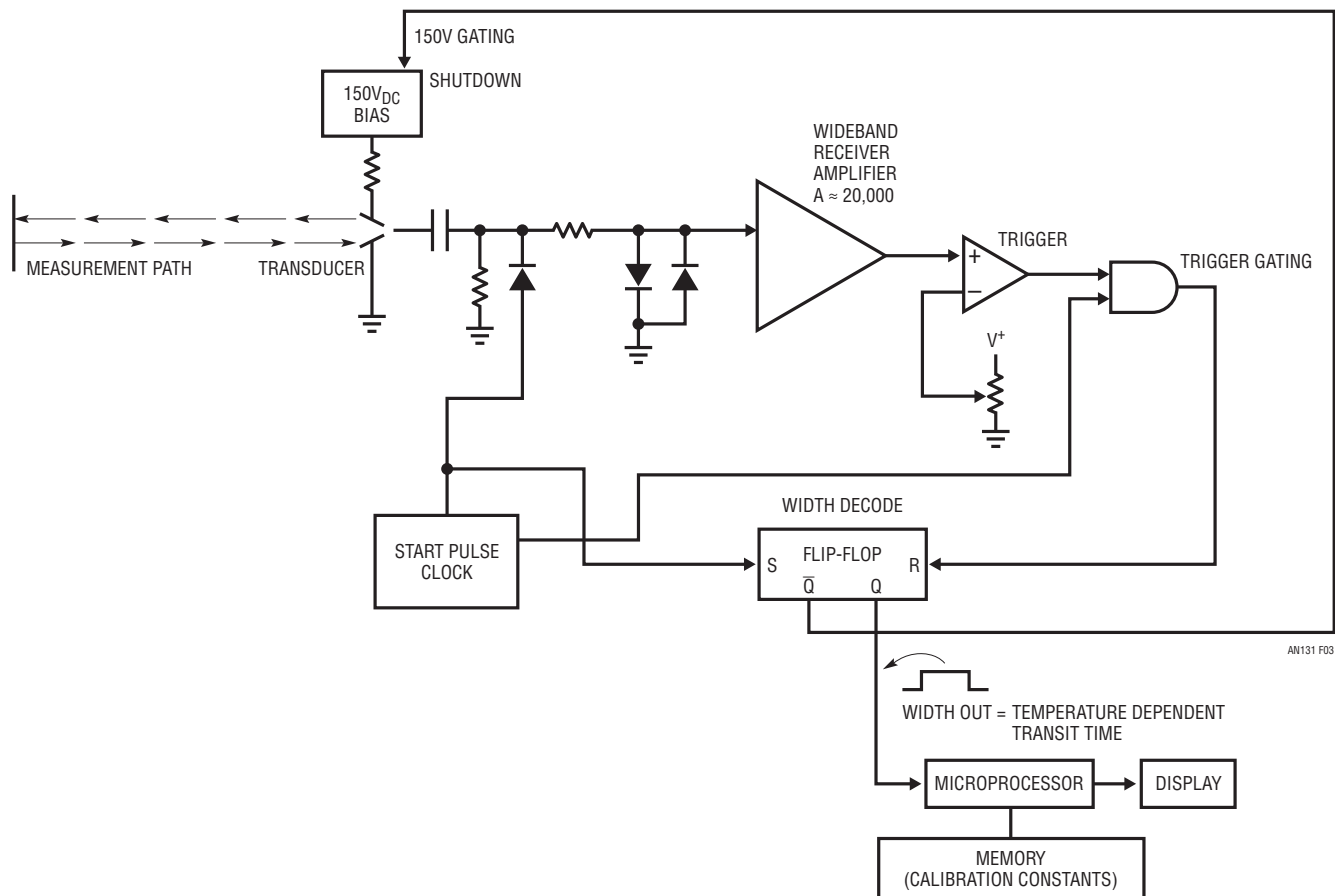


Figure 3. Conceptual Signal Conditioning for Acoustic Thermometer. Start Clock Launches Acoustic Pulse into Measurement Path, Sets Width Decode Flip-Flop High. Acoustic Paths Return Pulse, Amplified by Receiver, Trips Trigger, Resetting Flip-Flop. Resultant “Q” Width Output, Representing Path’s Temperature Dependent Transit Time, is Converted to Temperature Reading by Microprocessor. Gating High Voltage Supply and Trigger Prevents Spurious Outputs

Application Note 131

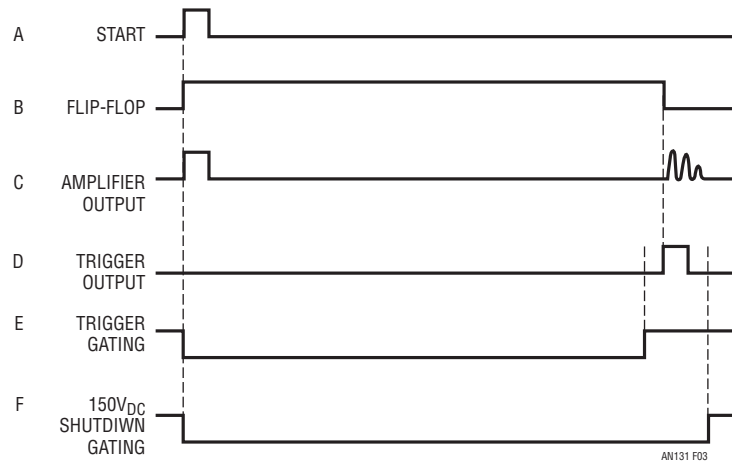


Figure 4. Figure 3's Event Sequence. Start Pulse (A) Drives Transducer, Sets Flip-Flop (B) High. Sonic Pulse Return Activates Amplifier (C, Extreme Right), Causing Trigger Output (D) to Reset Flip-Flop (B). Trigger Gating (E) Prevents Erroneous Trigger Response to Start Pulse Caused Amplifier Output (C, Extreme Left) and External Sonic Events. Gating (F) Turns Off 150V Switching Converter During Measurement, Precluding Amplifier Output Corruption

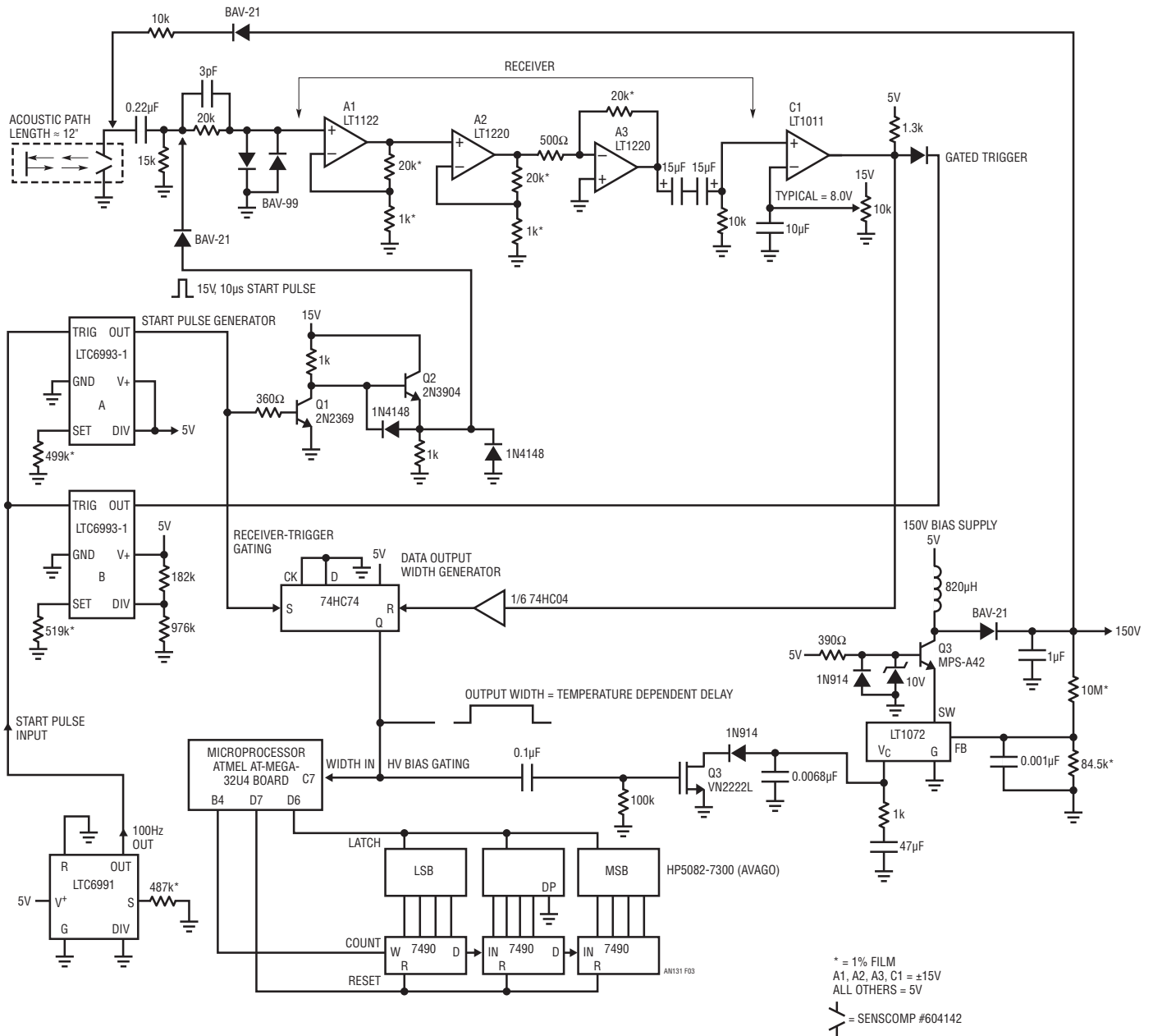


Figure 5. Detailed Circuitry Closely Follows Figure 3's Concept. Start Pulse Generator is Comprised of 100Hz Clock, One-Shot Multivibrators and Q1-Q2 Driver Stage. A ≈ 20,000 Receiver Amplifier Splits Gain Among Three Stages, Biases Trigger Comparator. Flip-Flop Output Width Feeds Microprocessor Which Calculates and Displays Temperature. Capacitive Coupling Isolates High Voltage DC Transducer Bias, Diode Clamping Prevents Destructive Overloads. Switching Regulator Controls High Voltage Via Cascode. Gating Obviates Switching Regulator Noise Originated Interference, Minimizes External Sonic Corruption

Application Note 131

Detailed Circuitry

Figure 5's detailed schematic closely follows Figure 3's concepts. An LTC®6991 oscillator furnishes the 100Hz clock. LTC®6993-1 monostable "A" provides a 10µs width to the Q1-Q2 driver, which capacitively couples the start pulse (Trace A, Figure 6) to the transducer. Simultaneously, the monostable sets the flip-flop (E) high. The flip-flop high output shuts down the LT®1072 based high voltage converter during the measurement. Monostable "B" produces a pulse (B) which gates off C1's trigger output for a time just shorter than the fastest expected sonic return.

The launched sonic pulse travels down the measurement path, bounces, returns, and impinges on the transducer. The transducer, biased at 150V_{DC}, releases charge ($Q = \Delta C \cdot V$) which appears as a voltage at the receiver amplifier.

The cascaded amplifier, with an overall gain of $\approx 17,600$, produces A2's output (C) and a further amplified version at A3. C1 triggers (D) at the first event that exceeds its negative input threshold, resetting the flip-flop. The resultant flip-flop width, representing the temperature dependent transit time, is read by the microprocessor which determines the temperature and displays it.²

Figure 7 studies receiver amplifier operation at the critical return impulse trip point. The returning sonic pulse is viewed at A2 (Trace A). A3 (B) adds gain, softly saturating the signals leading response. C1's trigger output (C) responds to multiple triggers but the flip-flop output (D) remains high after the initial trigger, securing transit time data.

Note 2. Complete processor software code appears in Appendix B, "Software Code."

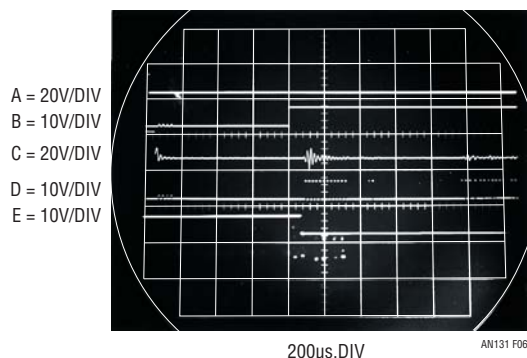


Figure 6. Figure 5's Waveforms Include Start Pulse (A), Trigger Gate (B), A2 Output (C), Trigger (D) and Flip-Flop Q Output Width (E). Amplifier Output Causes Multiple Trigger Transitions, But Flip-Flop Maintains Pulse Width Integrity. A2-Trigger Outputs at Photo Right, Due to Acoustic Pulse Second Bounce, Are Inconsequential

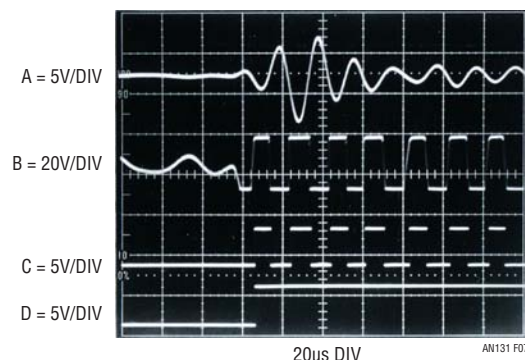


Figure 7. Receiver Amplifier—Trigger Operating Detail at Trip Point. Returning Sonic Pulse Viewed at A2 Output (Trace A) After X440 Gain. A3's Output (B) Adds X40, Softly Saturating Signals Leading Response. C1's Output (C) Responds to Multiple Triggers But Flip-Flop Output (D) Remains High After Initial Trigger

Gating prevents high voltage supply switching harmonics from producing spurious amplifier-trigger outputs. Figure 8 shows gate-off detail. The flip-flop output (Trace A) going high shuts down high voltage switching (B) at the measurement onset. This state persists during the entire transit time, preventing erroneous amplifier-trigger outputs. Figure 9's flip-flop fall (Trace A) combines with LT1072 V_C pin associated components, producing delayed high voltage turn-on (B) after the vulnerable, small amplitude return pulse trip point. This assures a clean, noise-free trigger.

Several circuit attributes aid performance. As mentioned, gating the trigger output prevents sonic interference from outside sources. Similarly, gating the 150V converter off prevents its harmonics from corrupting the high gain, wideband receiver amplifier. Additionally, the 150V sup-

ply value is a gain term, making its regulation loss during the measurement a potential concern. Practically, the $1\mu\text{F}$ output capacitor decays only 30mV in this time, or about 0.02%. This small variation is constant, insignificant and may be ignored. Deriving the trigger trip point and the start pulse from the same supply allows trigger voltage to vary ratiometrically with received signal amplitude, enhancing stability. Finally, the transducer used is wideband, highly sensitive and free from resonances, promoting repeatable, jitter-free operation.³ All of the above directly contribute to the circuit's $< 100\text{ns}$ (0.1°F) resolution of the $\approx 1\text{ms}$ path length – less than 100ppm uncertainty. Absolute accuracy from 60°F to 90°F is within 1°F referenced to Appendix A's calibration.

Note 3. Readers rich in years will recognize the specified transducer descends from 1970's era Polaroid SX-70 automatic focus cameras (every baby boomer had to have one).

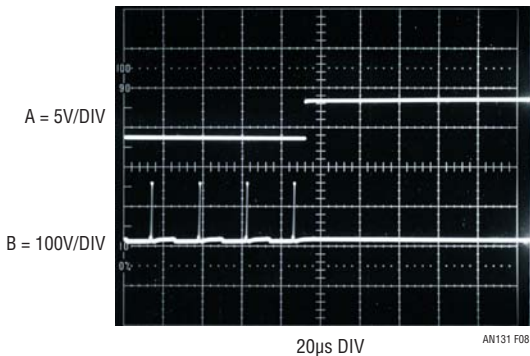


Figure 8. High Voltage Bias Supply Gate-Off Detail. Flip-Flop Output (Trace A) Going High Shuts Down LT1072 Switching Regulator, Turning Off 150V Flyback Events (B). Off-Time Extends During Measurement Interval, Precluding Receiver Amplifier Corruption

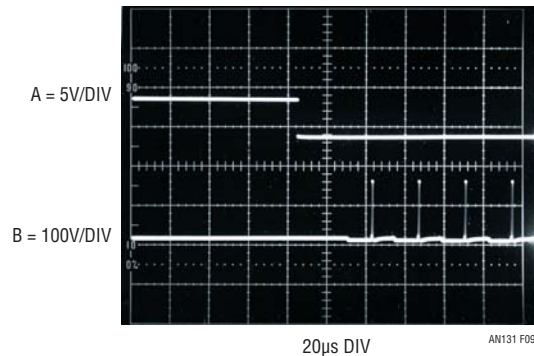


Figure 9. High Voltage Bias Supply Gate-On Detail. Flip-Flop Output (Trace A) Drops Low at Sonic Pulse Return. Components at LT1072 Switching Regulator V_C Pin Delay Bias Supply Turn-On (B). Sequencing Ensures Bias Supply is Off During Amplifier-Trigger's Vulnerable Response to Sonic Pulse Arrival

Application Note 131

Triggering on later bounces offers the potential benefit of easing timing tolerances and merits consideration. Figure 10 shows multiple sonic bounces, discernible in A2's output, decaying into acoustic dispersion induced noise contained within the glass enclosure. Triggering on a later bounce would relax timing margins, but incurs unfavorable signal-to-noise characteristics. Signal processing techniques could overcome this, but the increased resolutions utility would have to justify the effort.

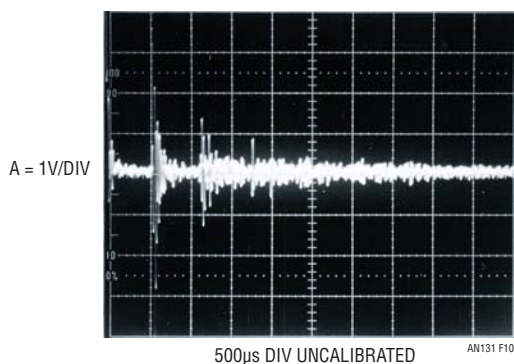


Figure 10. Multiple Sonic Bounces, Discernable in A2's Output, Decay into Acoustic Dispersion Induced Noise Contained Within Glass Enclosure. Triggering on Later Bounce Would Ease Timing Tolerances, But Incur Signal-to-Noise Degradation

REFERENCES

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2. Mi, X.B. Zhang, S.Y. Zhang, J.J. and Yang, Y.T., "Automatic Ultrasonic Thermometry." Presented at Fifteenth Symposium on Thermophysical Properties, June 22-27, 2003, Boulder, Colorado, U.S.A.
3. Williams, Jim, "Some Techniques For Direct Digitization of Transducer Outputs," Linear Technology Corporation, Application Note 7, p.4-6, Feb. 1985.
4. Analog Devices Inc., "Multiplier Applications Guide," "Acoustic Thermometer," Analog Devices Inc., p. 11-13, 1978.

APPENDIX A

Measurement Path Calibration

Theoretically, temperature calibration constants can be calculated from measurement path length. In practice, it is difficult to determine path length to the required accuracy. Enclosure, transducer and mounting dimensional uncertainties necessitate calibration vs known temperatures. Figure A1 shows the calibration arrangement. The enclosure is placed in a controllable thermal chamber equipped with an accurate thermometer iso-thermal with the enclosure. Ten evenly spaced temperature points from

60°F to 90°F are generated by stepping chamber set-point. The enclosure has a 30 minute time constant to 0.25°F settling, so adequate time must be allowed for each step to stabilize before readings are taken. Readings consist of noting the counter indicated pulse width at each temperature and recording the data. This information is then loaded into the microprocessor memory. See Appendix B, “Software Code.”

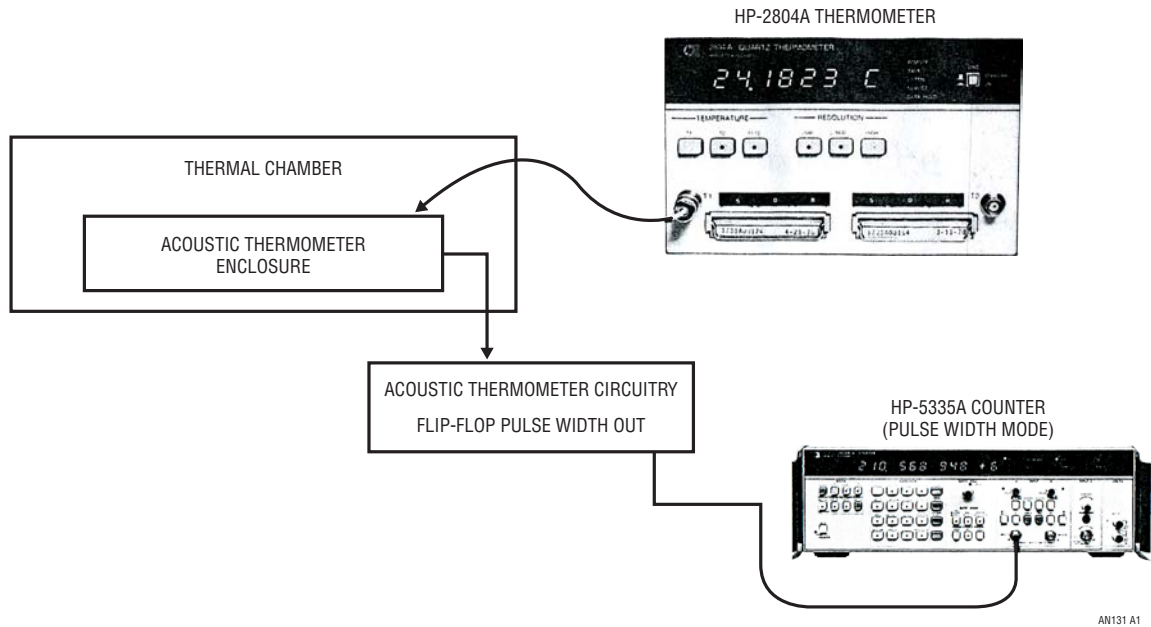


Figure A1. Calibration Arrangement Consists of Thermometer, Counter, Acoustic Conditioning Circuitry and Enclosure in Thermal Chamber. Temperature is Stepped Every 3°F Between 60°F and 90°F Allowing 30 Minute Stabilization Time Per Point

Application Note 131

APPENDIX B

The software code for the Atmel AT-Mega 32U4 microprocessor, combined with the calibration constants stored in its memory (see Appendix A), enables the processor to calculate and display the sensed temperature. This code, written by Omar Sanchez-Felipe of LTC, appears below.

```
// OLIVER.C:
//
// Hot temps from a jar of olives.
//
// The microprocessor is the Atmel ATmega32U4. See 'atmel.com' for its
// datasheet. The code is compiled with the current version of the
// 'avr-gcc' compiler obtainable at 'winavr.sourceforge.net'.
//
// Calibration data:
// Pulse len (usecs)      Temp (deg)
// 877.40                 84.2
// 884.34                 76.0
// 887.40                 72.4
// 892.56                 66.4
// 897.60                 60.7
//
#include <avr/io.h>
#include <avr/wdt.h>

// Some useful defs
#define BYTE      unsigned char
#define WORD      unsigned short
#define DWORD     unsigned long
#define BOOL      unsigned char
#define NULL      (void *)0
#define TRUE      1
#define FALSE     0

#define BSET(r, n)  r |= (1<<n)      // set/clr/tst nth bit of reg
#define BCLR(r, n)  r &= ~(1<<n)
#define BTST(r, n)  (r & (1<<n))
#define DDOUT(r, v) (r |= (v))      // config (set) bits for OUT
#define DDIN(r, v)  (r &= ~(v))     // config (clear) bits for IN
#define SETBITS(r, v) (r |= (v))    // set multiple bits on register
#define CLRBITS(r, v) (r &= ~(v))   // clear ""

#define SYS_CLK    16000000L        // clock (Hz)
#define CLKPERIOD  625
#define POSEDGE    1                // edge definitions for timerwait
#define NEGEDGE    0
#define TMRGATE    PORTC7           // I/O pins
#define BCDRSET    PORTD7
#define BCDPULS    PORTB4
#define DPYLATCH   PORTD6
```

```

// Calibration table and entry.
// Using small units of time and temp allows all calcs
// to be done in fixed point.
struct calpoint
{
    DWORD pulse;           // pulse duration, in tenths of nsecs
    WORD temp;             // temperature, in tenths of degrees
    WORD slope;            // slope (in tenths of nsecs/tenths of degree)
};

struct calpoint caltab[] = // the calibration table
{
    {8774000L, 842, 0},
    {8843400L, 760, 0},
    {8874000L, 724, 0},
    {8925600L, 664, 0},
    {8976000L, 607, 0}
};
#define NCALS      (sizeof(caltab)/sizeof(struct calpoint))
#define TEMPERR    999

void spin(WORD);
BOOL timerwait(BYTE v, long tmo, WORD *p);
void setdpy(WORD);
void dobackgnd(void);
WORD dotemp();

int main()
{
    WORD temp, i;

    // set master clock divisor
    CLKPR = (1<<CLKPCE); CLKPR = 0;

    // clear WDT
    MCUSR = 0;
    WDTCR |= (1<<WDCE) | (1<<WDE);
    WDTCR = 0x00;

    // init the display I/O pins
    BCLR(PORTD, BCDRSET);
    BCLR(PORTD, DPYLATCH);
    DDOUT(DDR, ((1<<BCDRSET) | (1<<DPYLATCH)));
    BCLR(PORTB, BCDPULS);
    DDOUT(DDR, (1<<BCDPULS));

    // init pulse-width counter (timer #3)
    TCCR3A = 0x00;
    TCCR3B = 0x01;           // no clk prescaling
    DDIN(DDRC, (1<<DDC7));   // PC7 is gate
    BSET(PORTC, PORTC7);     // enable pullup

    // compute the slope for each entry in the cal table
    // the first slope is never used, so we leave it at 0
    // note we're inverting the sign of the slope
    for (i = 1; i < NCALS; i++)
        caltab[i].slope = (caltab[i].pulse - caltab[i-1].pulse) /
            (caltab[i-1].temp - caltab[i].temp);

    setdpy(0);
}

```

Application Note 131

```
for (;;)
{
    temp = dotemp();    // compute temperature
    setdpy(temp);      // set the display
    spin(1000);        // spin a second and repeat
}
} // main

//      Set the display LED's to specified count by brute-force
//      incrementing the BCD counter that feeds it.
//
void    setdpy(WORD cnt)
{
    // reset BCD counter
    BSET(PORTD, BCDRSET);
    asm("nop"); asm("nop");
    BCLR(PORTD, BCDRSET);

    while (cnt--)
    {
        BSET(PORTB, BCDPULS);
        asm("nop"); asm("nop");
        BCLR(PORTB, BCDPULS);
        asm("nop"); asm("nop");
    }

    // latch current val (to avoid flicker)
    BCLR(PORTD, DPYLATCH);
    asm("nop"); asm("nop");
    BSET(PORTD, DPYLATCH);
}

//      Set up the edge detector to trigger on either a positive or
//      negative edge, depending on the 'edge' flag, and then wait for
//      it to happen. See defines for POSEDGE/NEGEDGE above.
//      if param 'tmo' is TRUE, a timeout is set so that we dont wait
//      forever if no pulse materializes. Returns the counter value
//      at which the edge occurs via pointer 'p'.
//
#define tcnTMO (SYS_CLK/20000L)    // approx 1 msec
BOOL    timerwait(BYTE edge, long tmo, WORD *p)
{
    if (edge == NEGEDGE)
        BCLR(TCCR3B, ICES3);    // falling edge
    else BSET(TCCR3B, ICES3);    // rising edge
    BSET(TIFR3, ICF3);
    tmo *= tcnTMO;
    while (!BTST(TIFR3, ICF3))
        {if (tmo-- < 0)
            return FALSE;
        }
    *p = ICR3;    // return current counter
    return TRUE;
}
```



```
// Measure the next POSITIVE pulse and map into temperature.
//
WORD dotemp()
{
    WORD strt, end, i;
    DWORD dur, temp;

    strt = end = dur = 0;
    // wait for any ongoing pulse to complete
    if (!timerwait(NEGEDGE, 5000, &strt))
        return 0;
    // now catch the first positive pulse
    if (!timerwait(POSEDGE, 5000, &strt))
        return 0;
    // and wait for it to complete
    if (!timerwait(NEGEDGE, 5000, &end))
        return 0;
    dur = (end - strt);
    dur *= CLKPERIOD; // duration now in tenths of nsecs

    // compute temp. If warmer than highest calibrated temp
    // or cooler than lowest calibrated temp, return TEMPERR
    //
    if (dur < caltab[0].pulse || dur > caltab[NCALS-1].pulse)
        temp = TEMPERR;
    else { // an entry will always be found, but we (re)init
        // temp to avoid complaints from the compiler
        temp = TEMPERR;
        for (i = 1; i < NCALS; i++)
            {if (dur <= caltab[i].pulse)
                {temp = caltab[i].temp +
                    (caltab[i].pulse - dur) /
                    caltab[i].slope;
                    break;
                }
            }
        }
    return temp;
}

// -----
// Spin for 'ms' millisecs. Spin constant is empirically determined.
//
#define SPINC (SYS_CLK / 21600L)
volatile WORD spinx;
void spin(WORD ms)
{
    WORD i;
    while (ms--)
        for (i = 0; i < SPINC; i++) spinx = i*i;
}

// END
```

Application Note 131

```
#      GCC MAKEFILE:
#
#      GMAKE file for the "oliver" code running on the ATmega32U4.
#
CC      = avr-gcc.exe
MCU     = atmega32u4

#      These are common to compile, link and assembly rules
#      The 'no-builtin' opt keeps gcc from assuming defs for putchar() and
#      others
#
COMMON  = -mmcu=$(MCU) -fno-builtin

CF      = $(COMMON)
CF      += -Wall -gdwarf-2
##CF    += -Wall -gdwarf-2 -O0

AF      = $(COMMON)
AF      += $(CF)
AF      += -x assembler-with-cpp -Wa,-gdwarf2

LF      = $(COMMON)
LF      += -Wl,-Map=$(TMP)$ (APP).map

#      weird intel flags
#
HEX_FLASH_FLAGS = -R .eeprom

HEX_EEPROM_FLAGS = -j .eeprom
HEX_EEPROM_FLAGS += --set-section-flags=.eeprom="alloc,load"
HEX_EEPROM_FLAGS += --change-section-lma .eeprom=0 --no-change-warnings

#      -----
#      MAKE DIRECTIVES
#
#      The "target directory" TMP is standard for the intermediate files
#      (.obj) and the final product.
#      -----
TMP     = ./tmp/

APP     = oliver
ELF     = $(TMP)$ (APP).elf
OBJS    = $(TMP)oliver.o

all:    $(TMP) $(ELF) $(TMP)$ (APP).hex $(TMP)$ (APP).eep size

$(TMP):
    rm -rf .\tmp
    mkdir .\tmp

$(TMP)oliver.o: oliver.c
    $(CC) $(INCLUDES) $(CF) -O1 -c  $< -o $*.o

oliver.asm: oliver.c
    $(CC) $(INCLUDES) $(CF) -O1 -S  $< -o oliver.asm
```

```
#      Linker -----
$(ELF): $(OBJS)
        $(CC) $(LF) $(OBJS) $(LINKONLYOBJS) $(LIBDIRS) $(LIBS) -o $(ELF)

%.hex: $(ELF)
        avr-objcopy -O ihex $(HEX_FLASH_FLAGS) $< $@

%.eep:  $(ELF)
        -avr-objcopy $(HEX_EEPROM_FLAGS) -O ihex $< $@ || exit 0

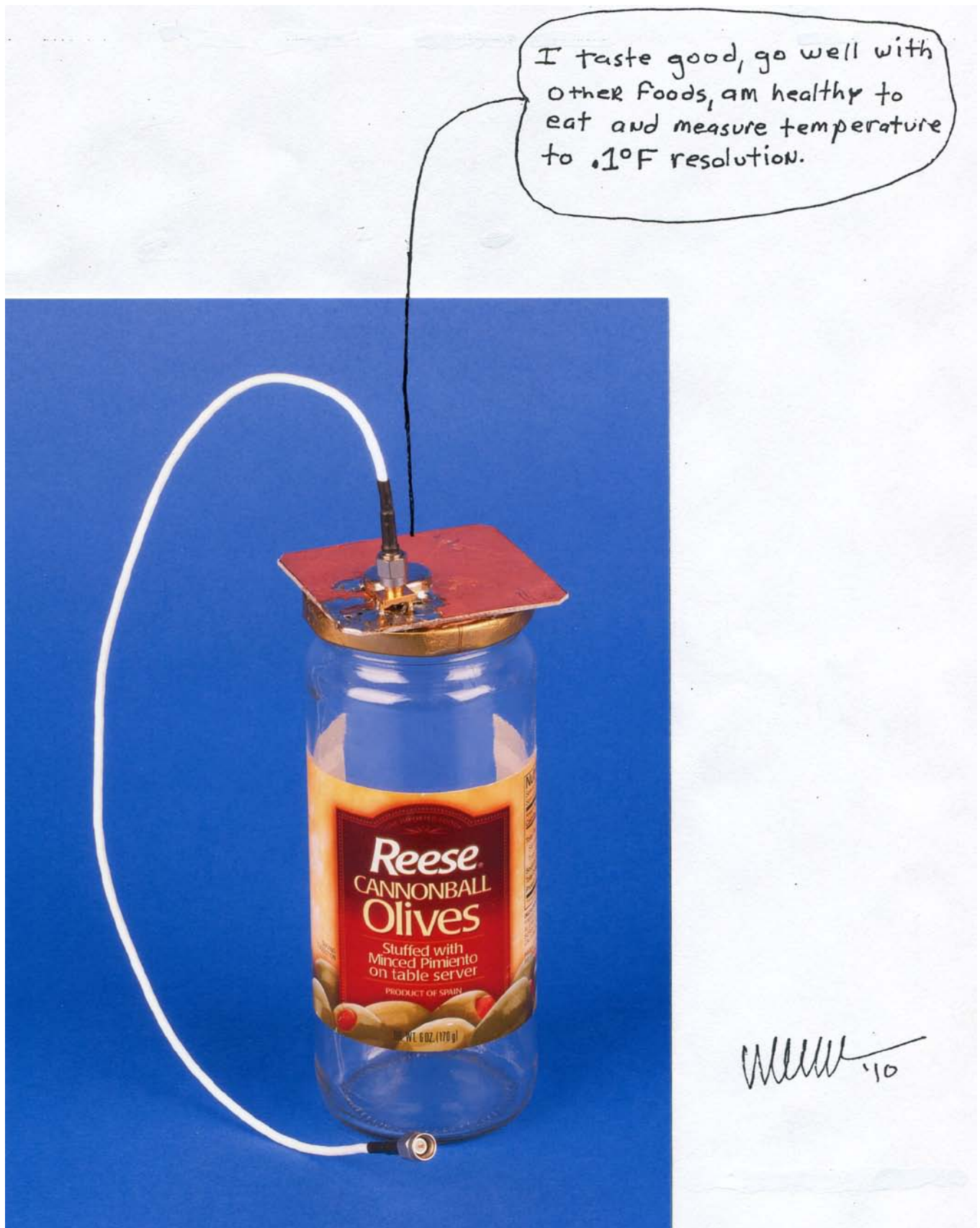
%.lss:  $(ELF)
        avr-objdump -h -S $< > $@

size:   $(ELF)
        @echo
        @avr-size -C --mcu=${MCU} $(ELF)

#      Misc -----
clean:
        -rm -rf $(OBJS) $(TMP)$(APP).elf ./dep/* $(TMP)$(APP).hex $(TMP)$(APP).eep
        $(TMP)$(APP).map $(TMP)$(APP).d

#      end
```

Application Note 131



Fidelity Testing for A→D Converters

Proving Purity

Jim Williams and Guy Hoover

Introduction

The ability to faithfully digitize a sine wave is a sensitive test of high resolution A→D converter fidelity. This test requires a sine wave generator with residual distortion products approaching one part-per-million. Additionally, a computer-based A→D output monitor is necessary to read and display converter output spectral components. Performing this testing at reasonable cost and complexity requires construction of its elements and performance verification prior to use.

Overview

Figure 1 diagrams the system. A low distortion oscillator drives the A→D via an amplifier. The A→D output interface formats converter output and communicates with the computer which executes the spectral analysis software and displays the resulting data.

Oscillator Circuitry

The oscillator is the system's most difficult circuit design aspect. To meaningfully test 18-bit A→Ds, the oscillator must have transcendently low levels of impurity, and these characteristics must be verified by independent means. Figure 2 is basically an "all inverting" 2kHz Wien

bridge design (A1-A2) adapted from work by Winfield Hill of Harvard University. The original designs J-FET gain control is replaced with a LED driven CdS photocell isolator, eliminating J-FET conductivity modulation introduced errors and the trim required to minimize them. Band limited A3 receives A2 output and DC offset bias, providing output via a 2.6 KHz filter which drives the A→D input amplifier. Automatic gain control (AGC) for the A1-A2 oscillator is taken from the circuit output ("AGC sense") by AC-coupled A4 which feeds rectifier A5-A6. A6's DC output represents the AC amplitude of the circuit output sine wave. This value is balanced against the LT®1029 reference by current summing resistors which terminate into AGC amplifier A7. A7, driving Q1, closes a gain control loop by setting LED current, and hence CdS cell resistance, to stabilize oscillator output amplitude. Deriving gain control feedback from the circuit's output maintains output amplitude despite the attenuating band-limiting response of A3 and the output filter. It also places demands on A7 loop closure dynamics. Specifically, A3's band limiting combines with the output filter, A6's lag and ripple reduction components in Q1's base to generate significant phase delay. A 1μF dominant pole at A7 along with an RC zero accommodates the

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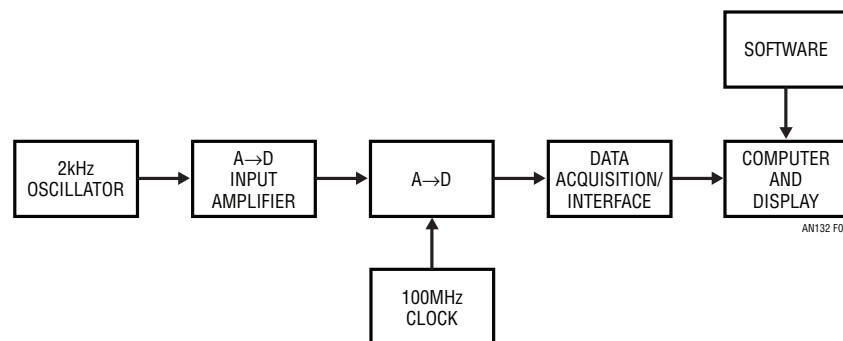


Figure 1. Block Diagram of A→D Spectral Purity Test System. Assuming a Distortionless Oscillator, Computer Displays Four Components Due to Amplifier and A→D Infidelties

an132f

Application Note 132

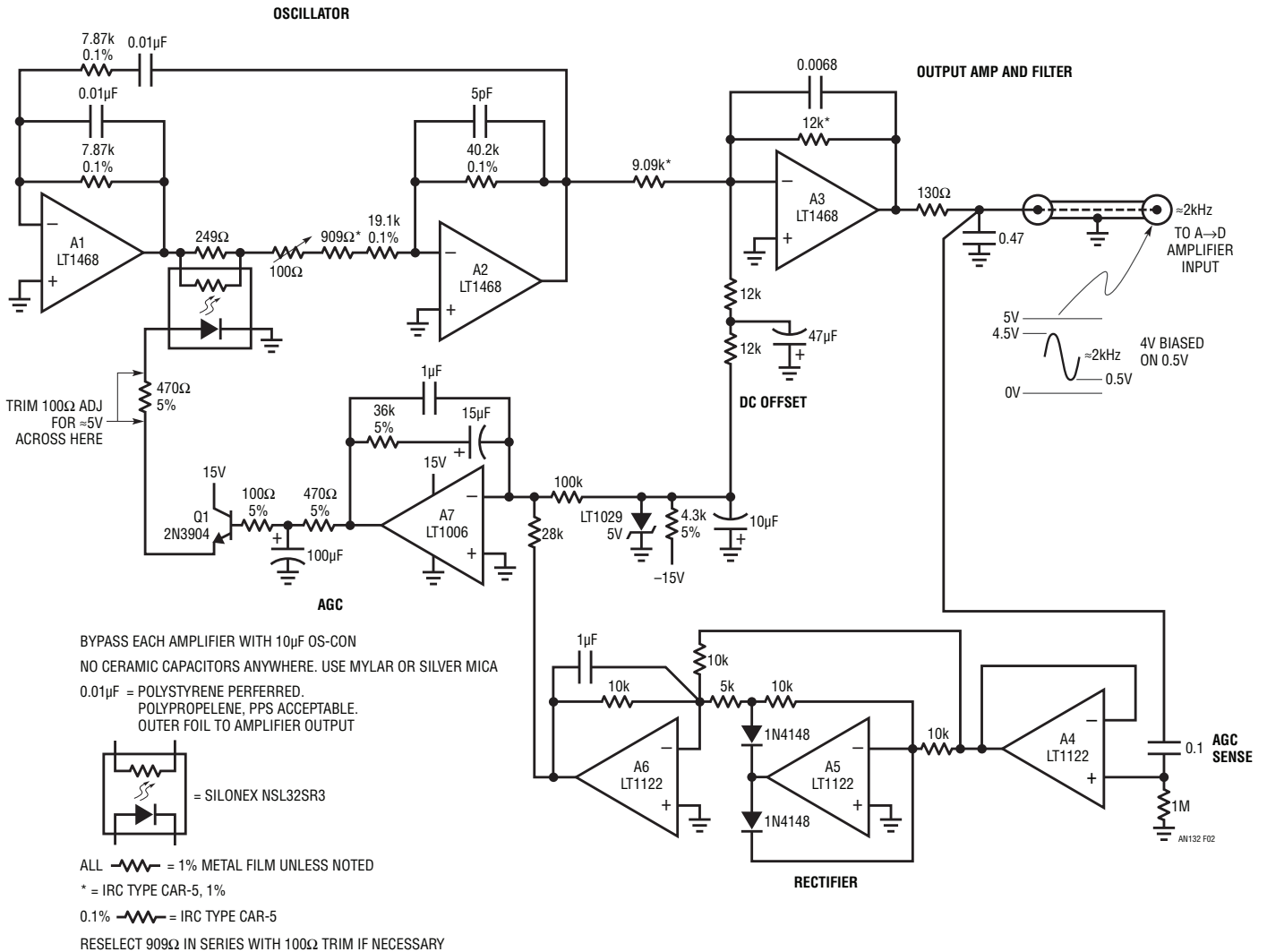


Figure 2. Wien Bridge Oscillator Uses Inverting Amplifiers in Signal Path, Achieves 3ppm Distortion. LED Photocell Replaces Usual J-FET as Gain Control, Eliminating Conductivity Modulation Induced Distortion. A3 Associated Filtering Attenuation is Compensated by Sensing AGC Feedback at Circuit Output. DC Offset Biases Output Into A→D Input Amplifier Range

delay, achieving stable loop compensation. This approach replaces closely tuned high order output filters with simple RC roll-offs, minimizing distortion while maintaining output amplitude¹.

Eliminating oscillator related components from the LED bias is essential to maintaining low distortion. Any such residue will amplitude modulate the oscillator, introducing impure components. The band-limited AGC signal forward path is well filtered and the heavy RC time constant in Q1's base provides a final, steep roll-off. Figure 3, Q1's emitter current, shows about 1nA of oscillator related ripple out of a 10mA total, less than 0.1ppm.

Note 1. This is loosely akin to forcing food through a meat grinder to produce purée.

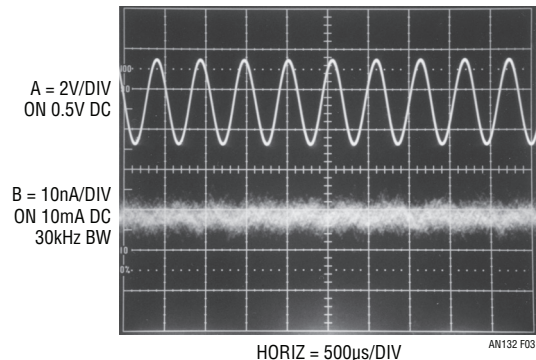


Figure 3. Oscillator (Trace A) Related Residue (Trace B), Just Discernible in Q1 Emitter Noise, ≈1nA, About 0.1ppm of LED Current. Characteristic, Deriving From Heavy AGC Signal Path Filtering, Prevents Modulation Products From Influencing Photocell Response

The oscillator achieves its performance using only a single trim. This adjustment, which centers AGC capture range, is set in accordance with the schematic note.

Verifying Oscillator Distortion

Verifying oscillator distortion necessitates sophisticated measurement techniques. Attempts to measure distortion with a conventional distortion analyzer, even a high grade type, encounter limitations. Figure 4 shows oscillator output (Trace A) and its indicated distortion residuals at the analyzer output (Trace B). Oscillator related activity is faintly outlined in the analyzer noise and uncertainty floor. The HP-339A employed specifies a minimum measurable distortion of 18ppm; this photograph was taken with the instrument indicating 9ppm. This is beyond specification, and highly suspect, because of the pronounced uncertainties introduced when measuring distortion at or near equipment limits². Specialized analyzers with exquisitely low uncertainty floors are needed to meaningfully measure oscillator distortion. The Audio Precision 2722, specified at a 2.5ppm Total Harmonic Distortion + Noise (THD + N) limit (1.5ppm typical), supplied Figure 5's data. This figure

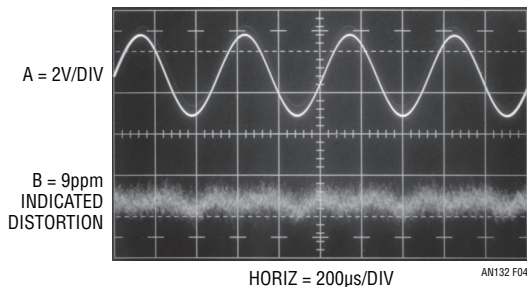


Figure 4. HP-339A Distortion Analyzer Operating Beyond Its Resolution Limit Provides Misleading Distortion Indication (Trace B). Analyzer Output Contains Uncertain Combination of Oscillator and Instrument Signatures and Cannot Be Relied Upon. Trace A Is Oscillator Output

indicates a Total Harmonic Distortion (THD) of -110dB , or about 3ppm. Figure 6, taken with the same instrument, shows THD + N of 105dB , or about 5.8ppm. In Figure 7's final test, the analyzer determines the oscillator's spectral components with the third harmonic dominating at -112dB , or about 2.4ppm. These measurements provide confidence in applying the oscillator to A→D fidelity characterization.

A→D Testing

A→D testing routes oscillator output to the A→D via its input amplifier. The test measures distortion products produced by the input amplifier/A→D combination. A→D output is examined by the computer, which quantitatively indicates spectral error components in Figure 8's display.³ The display includes time domain information showing the biased sine wave centered into the converter's operating range, a Fourier transform indicating spectral error components and detailed tabulated readings. The LTC®2379 18-Bit A→D/LT6350 amplifier combination under test produces 2nd harmonic distortion of -111dB , about 2.8ppm, with higher frequency harmonics well below this level. This indicates the A→D and its input amplifier are operating properly and within specifications. Possible harmonic cancellation between the oscillator and amplifier/A→D mandates testing several amplifier/A→D samples to enhance measurement confidence⁴.

Note 2. Distortion measurements at or near equipment limits are full of unpleasant surprises. See LTC Application Note 43, "Bridge Circuits", Appendix D, "Understanding Distortion Measurements" by Bruce Hofer of Audio Precision.

Note 3. Input amplifier/A→D converter, computer data acquisition and clock boards, necessary for testing, are available from LTC. Software code may be downloaded at www.linear.com. See Appendix A "Tools for A→D Fidelity Testing" for details.

Note 4. Review text section, "Verifying Oscillator Distortion" and footnote 2 for relevant commentary.

Application Note 132

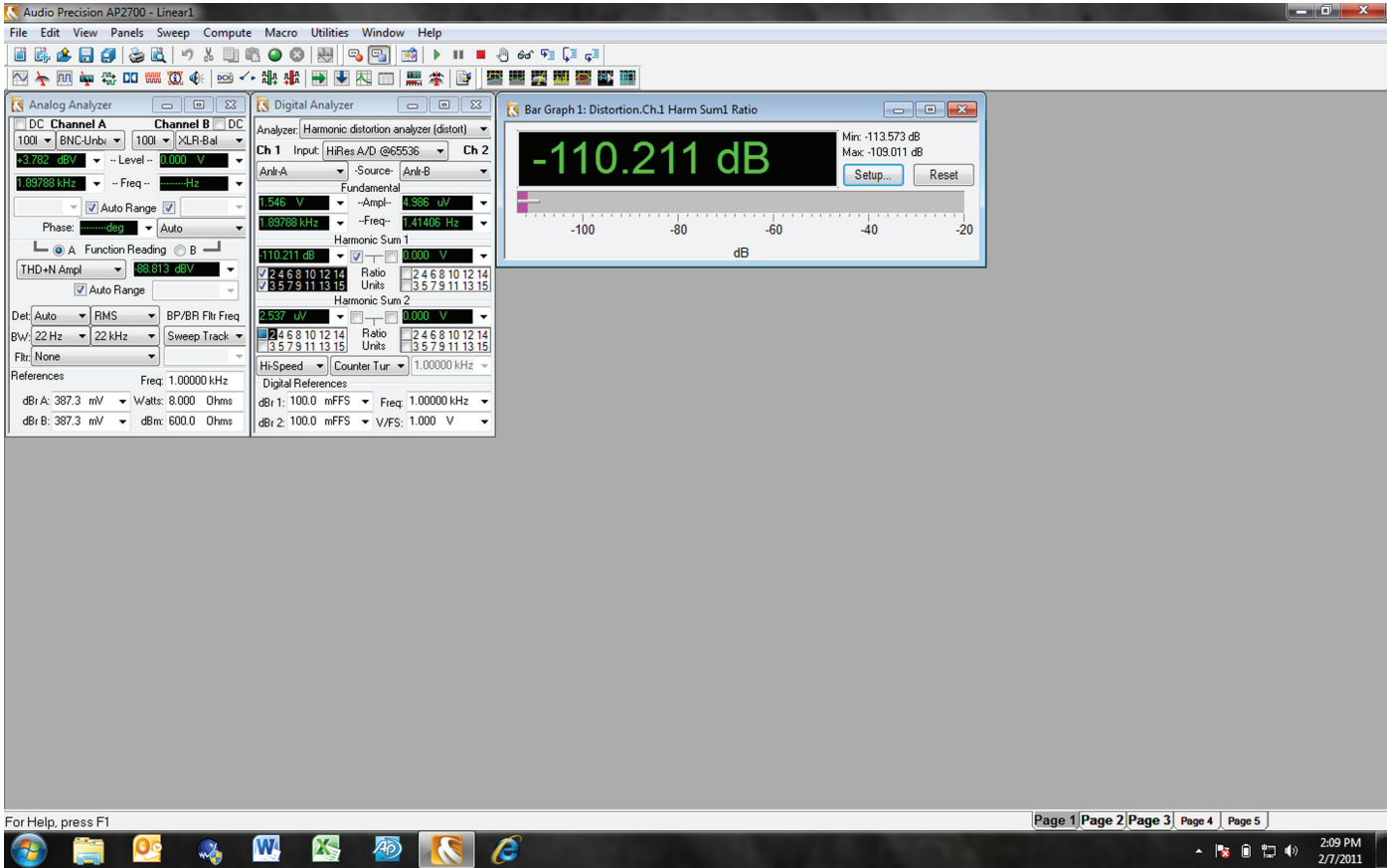


Figure 5. Audio Precision 2722 Analyzer Measures Oscillator THD at -110dB, About 3ppm

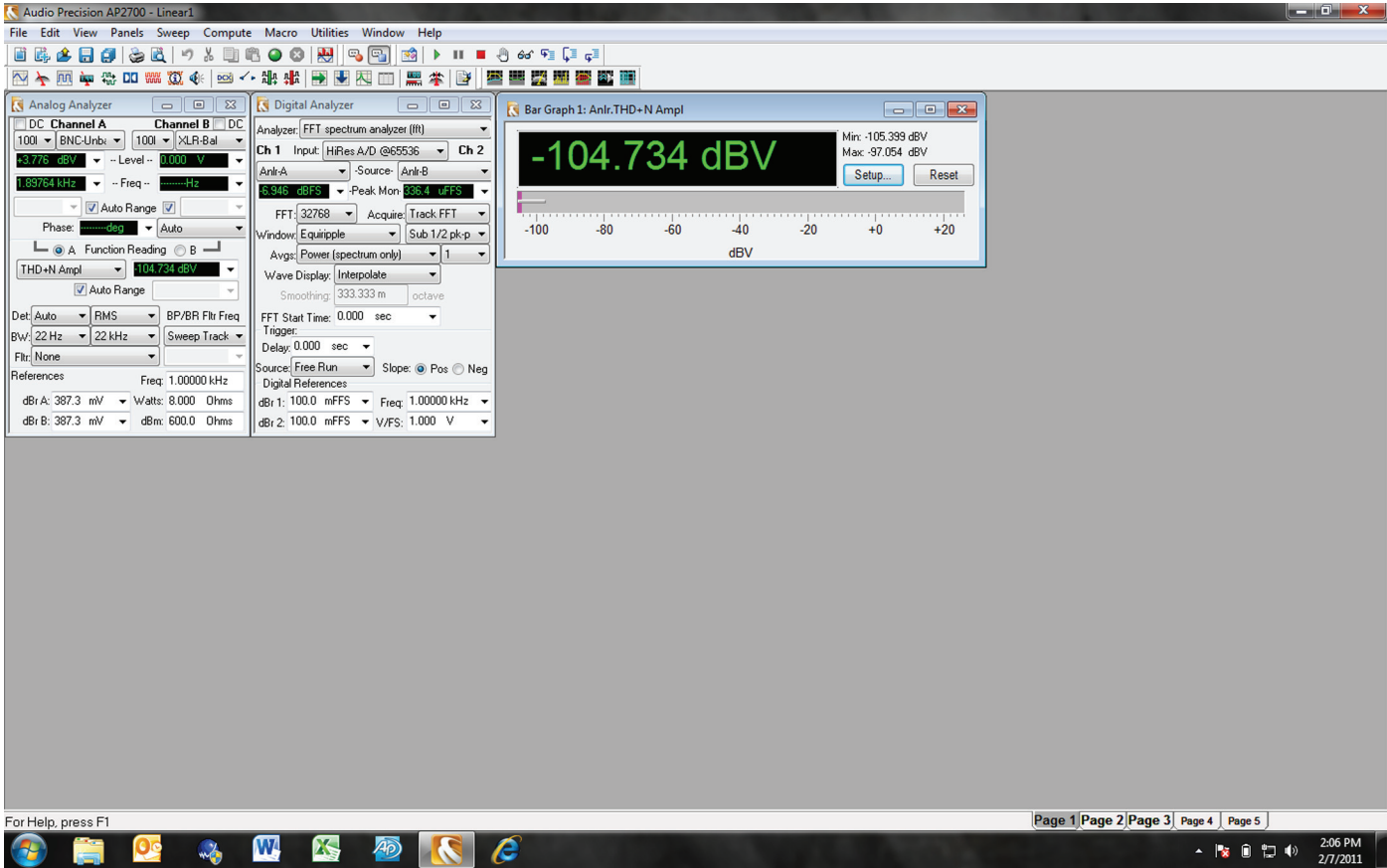


Figure 6. AP-2722 Analyzer Measures Oscillator THD + N at ≈ -105 dB, About 5.8ppm

Application Note 132

Audio Precision

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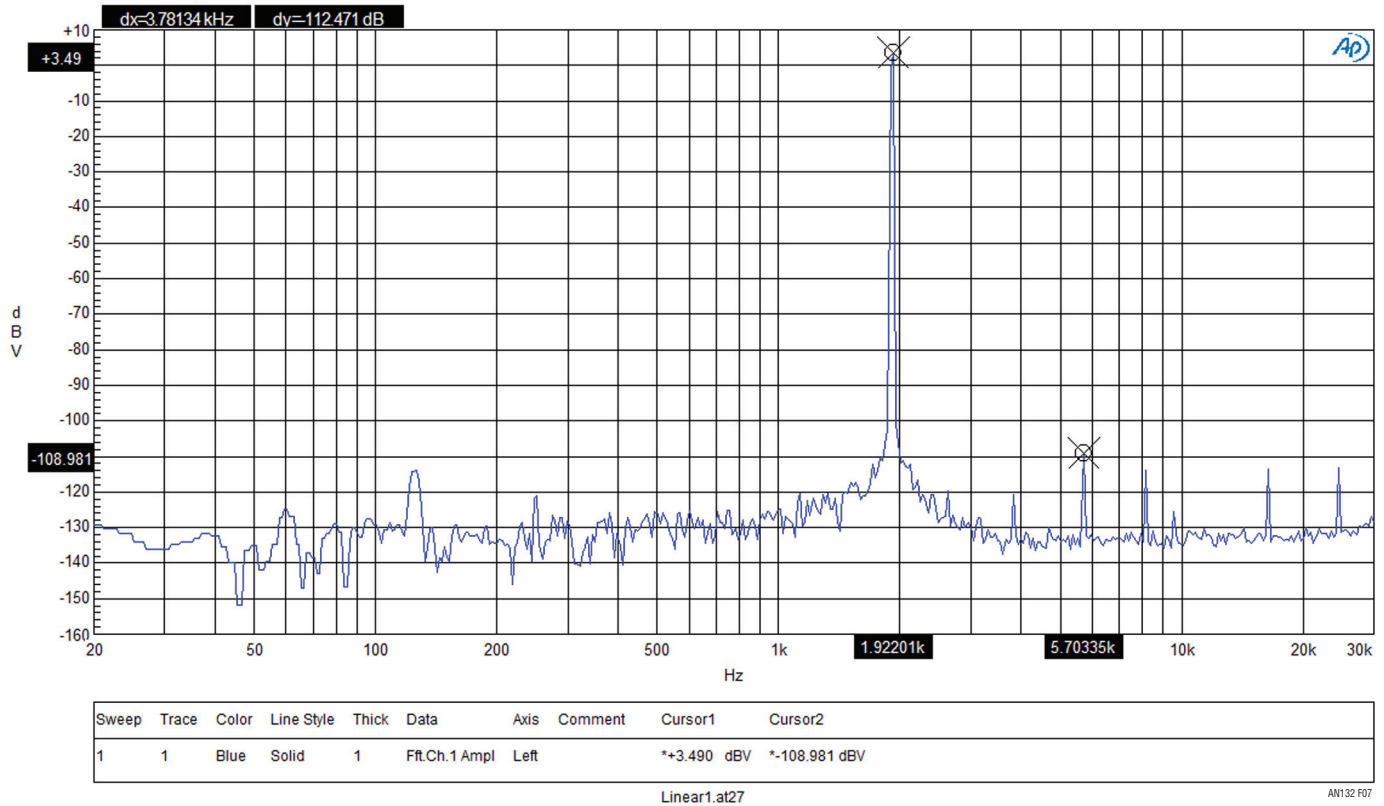


Figure 7. AP-2722 Spectral Output Indicates 3rd Harmonic Peak at -112.5dB, ≈2.4ppm

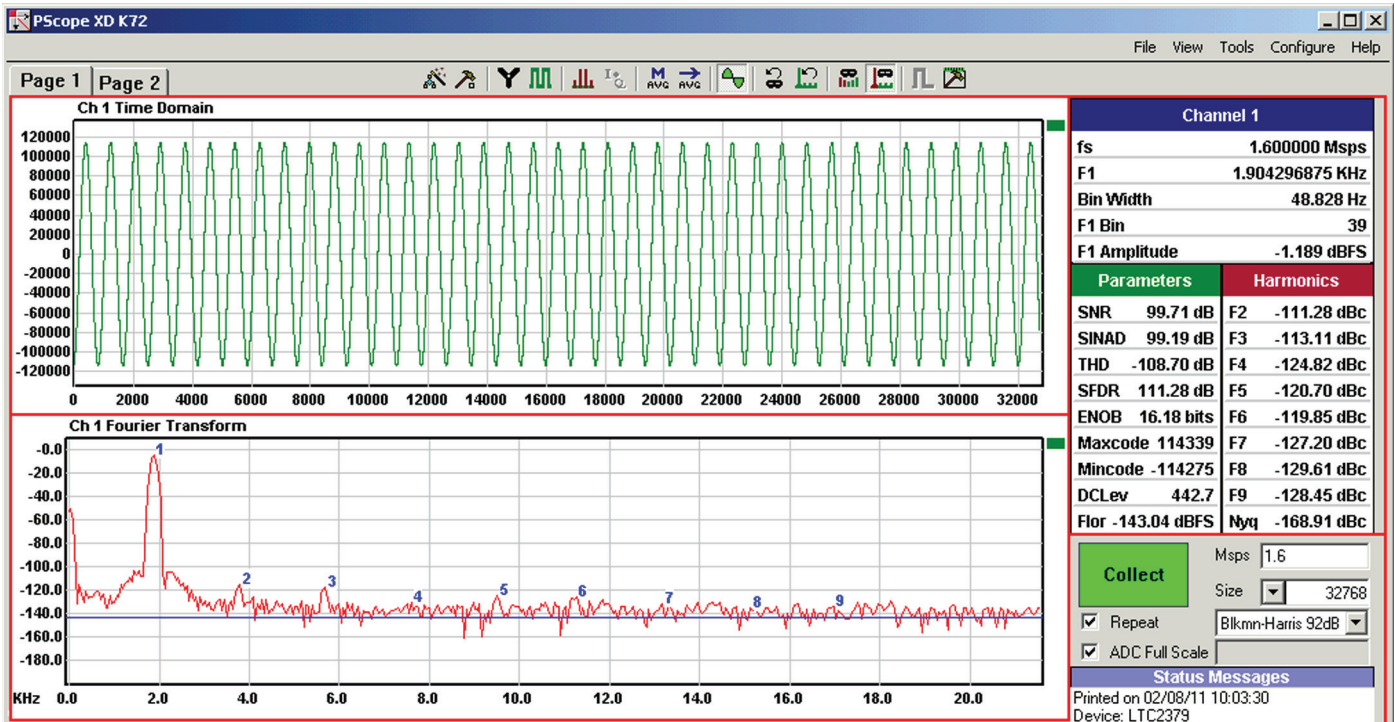


Figure 8. Figure 1's Test System Partial Display Includes Time Domain Information, Fourier Spectral Plot and Detailed Tabular Readings for LTC2379 18-Bit A→D Driven by LT6350 Amplifier

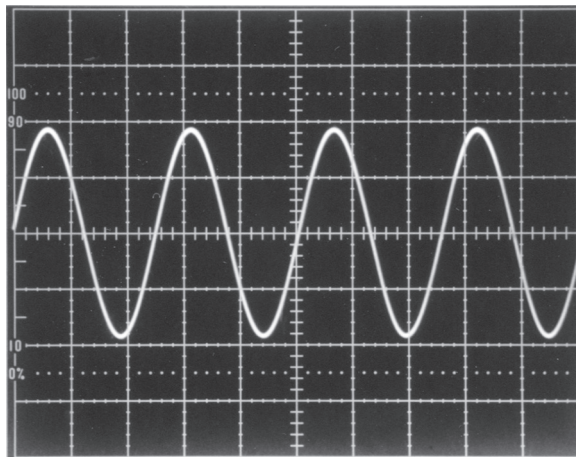
APPENDIX A**Tools for A→D Fidelity Testing**

Circuit boards for implementing the text's A→D testing are available. Table 1 lists the board functions and their part numbers. The computer software, PScope™, is also available from Linear Technology and may be downloaded at www.linear.com.

Table 1

BOARD FUNCTION	PART NUMBER
LT6350/LTC1279 Amp/A→D	DC-1783A-E
Interface	DC718
100MHz Clock*	DC1216A-A
Oscillator	To Be Released

*Any stable, low phase noise 3.3V clock capable of driving 50Ω may be used.

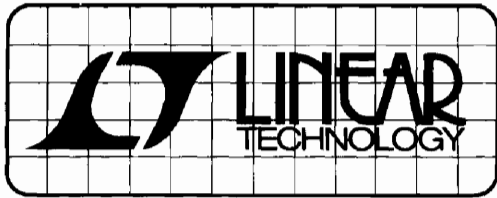


“Summon a vision and declare it pure.”

—Theodore Roethke

“Four for Sir John Davies”

1953



DESIGN NOTES

Number 8 in a series from Linear Technology Corporation

March, 1988

Inductor Selection for LT1070 Switching Regulators

Jim Williams

A common problem area in switching regulator design is the inductor, and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to approach inductor selection. It permits real time analysis under actual circuit operating conditions using the ultimate simulator—a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure 1 shows a typical flyback regulator utilizing the LT1070 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit* shown in Figure 2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure 1.

* Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, 619-268-2400

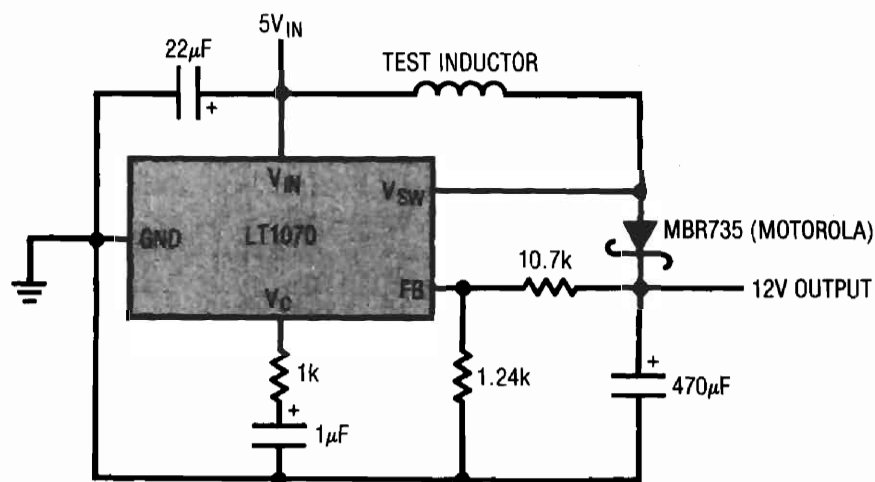


Figure 1. Basic LT1070 Flyback Regulator Test Circuit

Figure 3 was taken with a $450\mu\text{H}$ value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1070's V_{SWITCH} pin voltage while trace B shows its current. When V_{SWITCH} pin voltage is low, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure 4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure 5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure 6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

References

- AN-25 "Switching Regulators for Poets", Jim Williams, Linear Technology Corporation
- AN-19 "LT1070 Design Manual", Carl Nelson, Linear Technology Corporation

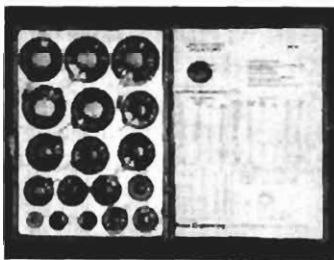


Figure 2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. (includes 18 fully specified devices)

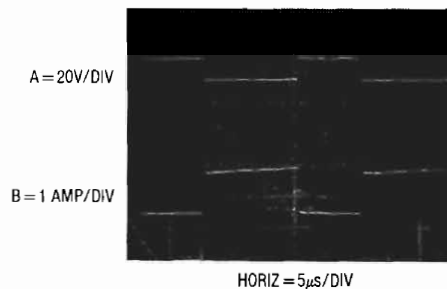


Figure 3. Waveforms for $450\mu\text{H}$, High Core Capacity Unit

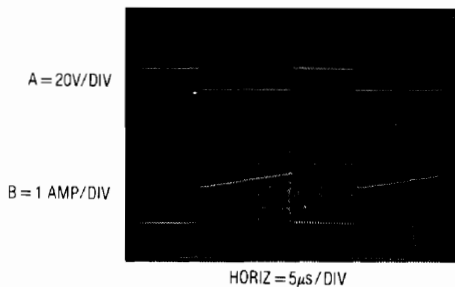


Figure 4. Waveforms for $170\mu\text{H}$, High Capacity Core Unit

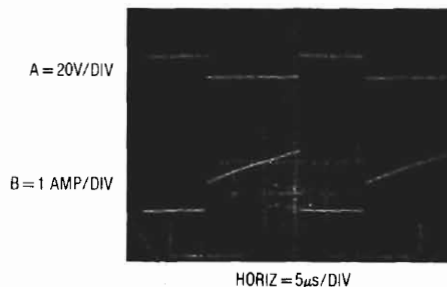


Figure 5. Waveforms for $55\mu\text{H}$, High Capacity Core Unit

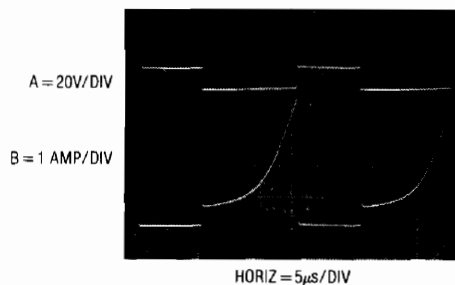
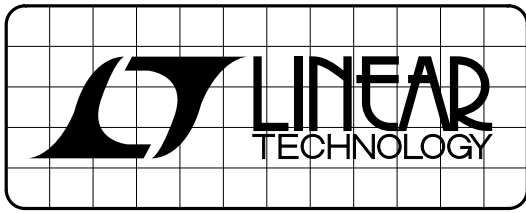


Figure 6. Waveforms for $500\mu\text{H}$, Low Capacity Core Inductor (note saturation effects)

For Switching Regulator literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.



DESIGN NOTES

A Precision Wideband Current Probe for LCD Backlight Measurement – Design Note 101

Jim Williams

Evaluation and optimization of Cold Cathode Fluorescent Lamp (CCFL) performance requires highly accurate AC current measurement. CCFLs, used to backlight LCD displays, typically operate at 30kHz to 70kHz with measurable harmonic content into the low MHz region¹. Accurate determination of RMS operating current is important for electrical and emissivity efficiency computations and to ensure long lamp life. Additionally, it is desirable to be able to perform current measurements in the presence of high common-mode voltage ($>1000V_{RMS}$). This capability allows investigation and quantification of display and wiring induced losses, regardless of their origins in the lamp drive circuitry.

Current Probe Circuitry

Figure 1's circuitry meets the discussed requirements. It signals conditions a commercially available "clip-on" current probe with a precision amplifier to provide 1% measurement accuracy to 10MHz. The "clip-on" probe provides convenience, even in the presence of the high

common voltages noted. The current probe biases A1, operating at a gain of about 3.75. No impedance matching is required due to the probe's low output impedance termination. Additional amplifiers provide distributed gain, maintaining wide bandwidth with an overall gain of about 200. The individual amplifiers avoid any possible crosstalk-based error that could be introduced by a monolithic quad amplifier. D1 and Rx are selected for polarity and value to trim overall amplifier offset. The 100Ω trimmer sets gain, fixing the scale factor. The output drives a thermally-based, wideband RMS voltmeter. In practice, the circuit is built into a 2.25" × 1" × 1" enclosure which is *directly* connected, via BNC hardware, to the voltmeter. No cable is used. The result is a "clip-on" current probe with 1% accuracy over a 20kHz to 10MHz bandwidth. Figure 2 shows response for the probe-amplifier as measured on a Hewlett-Packard HP-4195A network analyzer.

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¹ Williams, Jim, "Techniques for 92% Efficient LCD Illumination." Linear Technology Corporation AN55, August 1993.

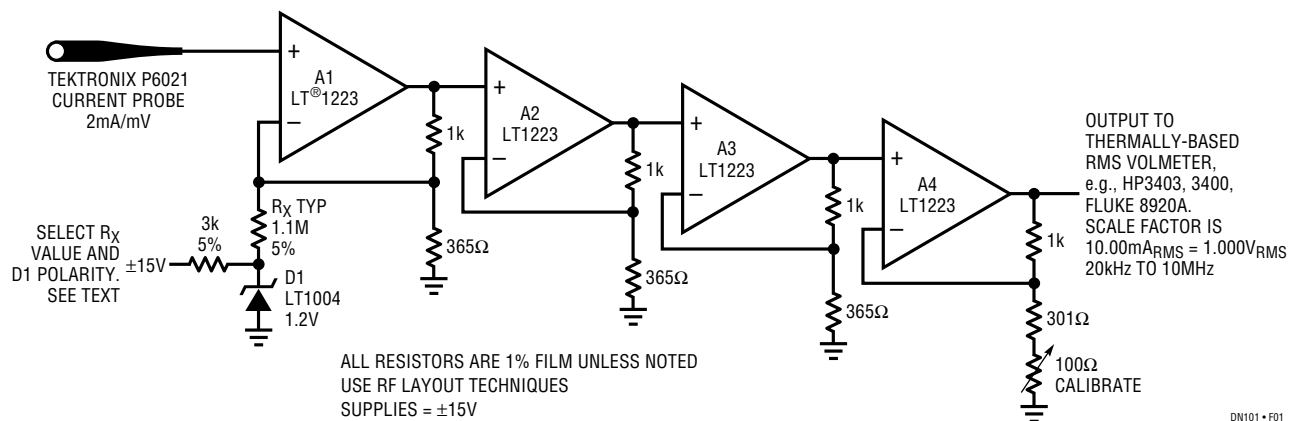


Figure 1. Precision "Clip-On" Current Probe for CCFL Measurements Maintains 1% Accuracy Over 20kHz to 10MHz Bandwidth

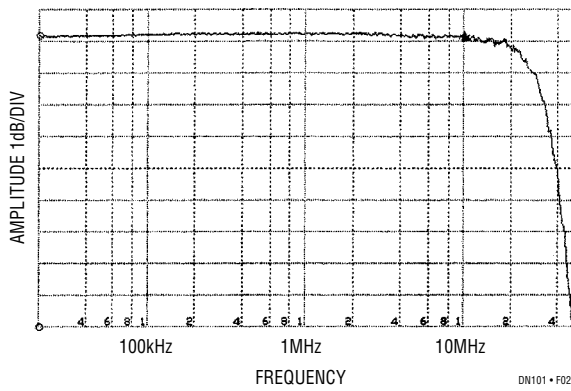


Figure 2. Amplitude vs Frequency Output of HP4195A Network Analyzer. Current Probe-Amplifier Maintains 1% (0.1dB) Error Bandwidth from 20kHz to 10MHz. Small Aberrations Between 10MHz and 20MHz Are Test Fixture Related

Current Calibrator

Figure 3's circuit, a current calibrator, permits calibration of the probe-amplifier and can be used to periodically check probe accuracy. A1 and A2 form a Wein bridge oscillator. Oscillator output is rectified by A4 and A5 and compared to a DC reference at A3. A3's output controls Q1, closing an amplitude stabilization loop. The stabilized amplitude is terminated into a 100Ω, 0.1% resistor to provide a precise 10.00mA, 60kHz current through the series current loop. Trimming is performed by altering the nominal 15k resistor for exactly 1.000V_{RMS} across the 100Ω unit.

In use, this current probe has shown 0.2% baseline stability with 1% absolute accuracy over one year's time. The sole maintenance requirement for preserving accuracy is to keep the current probe jaws clean and avoid rough or abrupt handling of the probe².

² Private Communication. Tektronix, Inc.

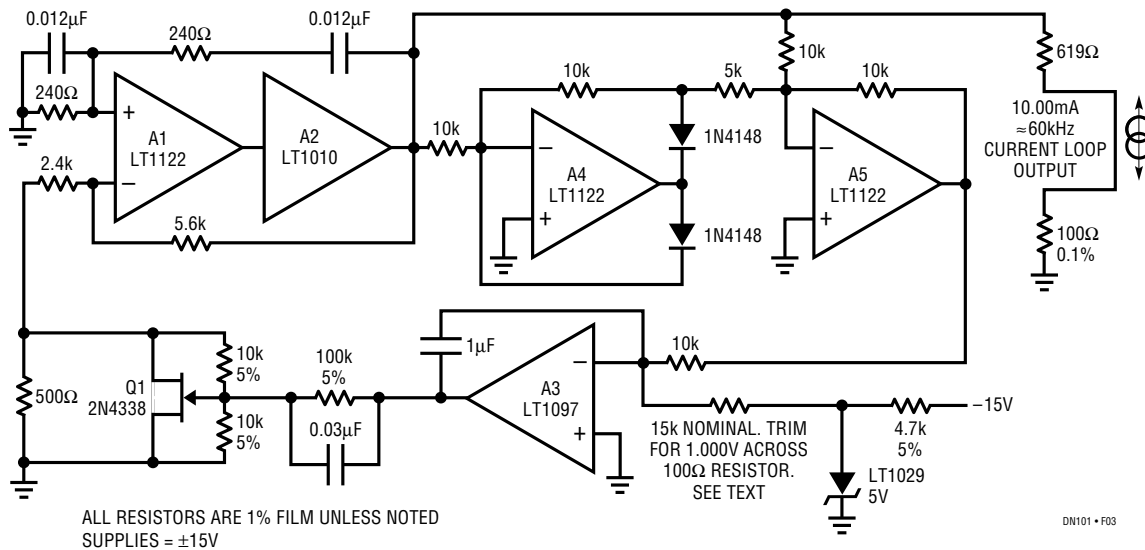
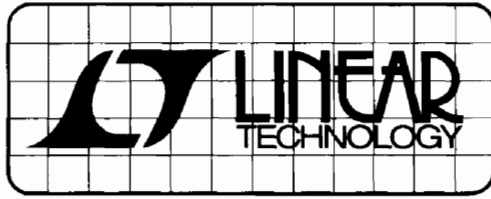


Figure 3. Current Calibrator for Probe Trimming and Accuracy Checks. Stabilized Oscillator Forces 10.00mA Through Output Current Loop at 60kHz

For literature on our High Speed Amplifiers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 456



DESIGN NOTES

Number 11 in a series from Linear Technology Corporation

June, 1988

Achieving Microamp Quiescent Current in Switching Regulators

Jim Williams

Many battery powered applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or "sleep" modes draw only microamperes. A typical lap top computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any switching regulator designed for loop stability under no-load conditions will work. In practice, a regulator's relatively large quiescent current may cause unacceptable battery drain during low output current intervals.

Figure 1 shows a typical flyback regulator. In this case the 6V battery is converted to a 12V output by the inductive flyback voltage produced each time the LT1070's V_{SW} pin is internally switched to ground. An internal 40kHz clock produces a flyback event every 25 μ s. The energy in this event is controlled by the IC's internal error amplifier, which acts to force the feedback (FB) pin to a 1.23V reference. The error amplifier's high impedance output (the V_C pin) uses an RC damper for stable loop compensation.

This circuit works well but pulls 9mA of quiescent current. If battery capacity is limited by size or weight this may be too high. How can this figure be reduced while retaining high current performance?

A solution is suggested by considering an auxiliary V_C pin function. If the V_C pin is pulled within 150mV of ground the IC shuts down, pulling only 50 microamperes. Figure 2's special loop exploits this feature, reducing quiescent current to only 150 microamperes. Here, circuitry is placed between the feedback divider and the V_C pin. The LT1070's internal feedback amplifier and reference are not used. Figure 3 shows operating waveforms under no-load conditions. The 12V output (trace A) ramps down over a period of seconds. During this time comparator A1's output (trace B) is low, as are the paralleled inverters. This pulls the V_C pin (trace C) low, putting the IC in its 50 μ A shutdown mode. The V_{SW} pin (trace D) is high, and no inductor current flows. When the 12V output drops about 20mV, A1 triggers and the inverters (74C04) go high, pulling the V_C pin up and turning on the

regulator. The V_{SW} pin pulses the inductor at the 40kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back into shutdown. This "bang-bang" control loop keeps the 12V output within the 20mV ramp hysteresis window set by R3-R4. Diode clamps prevent V_C pin overdrive. Note that the loop oscillation period of 4-5 seconds means the R6-C2 time constant at V_C is not a significant term. Because the LT1070 spends almost all of the time in shutdown, very little quiescent current (150 μ A) is drawn.

Figure 4 shows the same waveforms with the load increased to 3mA. Loop oscillation frequency increases to keep up with the load's sink current demand. Now, the V_C pin waveform (trace C) begins to take on a filtered appearance. This is due to R6-C2's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R6-C2 time constant, however, is fixed. Beyond some frequency, R6-C2 must average loop oscillations to DC.

Figure 5 plots what occurs, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 500Hz. At this point the R6-C2 time constant filters the V_C pin to DC and the LT1070 transitions into "normal" operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed loop gain set by the R1-R2 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R6-C2's break frequency. The phase error contributed by C1 (which was selected for low loop frequency at low output currents) is dominated by the R6-C2 roll off and the R7-C3 lead into A1. The loop is stable and responds linearly for all loads beyond 80mA. In this high current region the LT1070 behaves like Figure 1's circuit.

The loop described provides a controlled, conditional instability to lower regulator quiescent current by a factor of 60 without sacrificing high power performance. Although demonstrated in a boost converter, it is readily exportable to other configurations, (e.g., multi-output flyback, buck, etc.) allowing LT1070 use in low quiescent power applications.

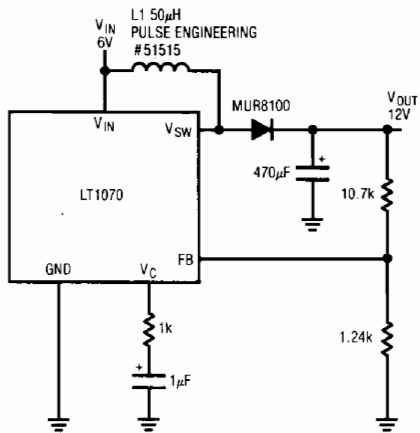


Figure 1. Typical LT1070 Flyback Regulator

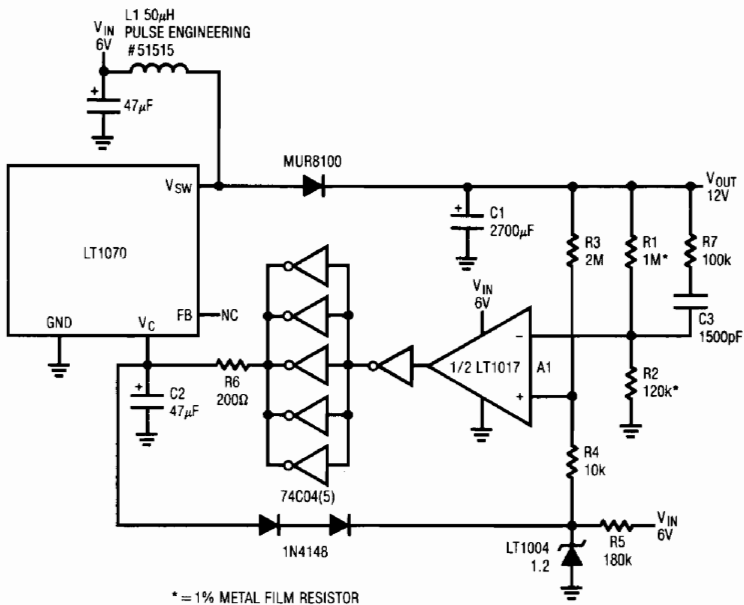


Figure 2. Low Quiescent Current Flyback Regulator

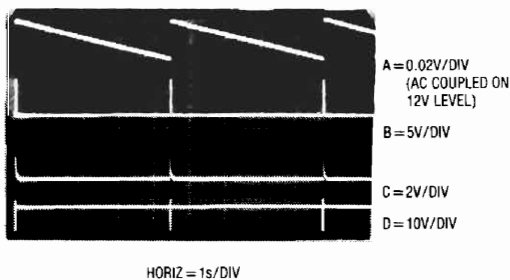


Figure 3. Waveforms at No Load for Figure 2 (Traces B and D Retouched for Clarity)

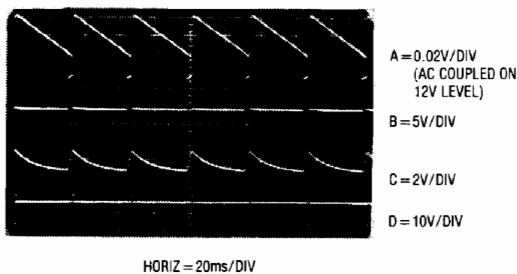


Figure 4. Waveforms at 3mA Load for Figure 2

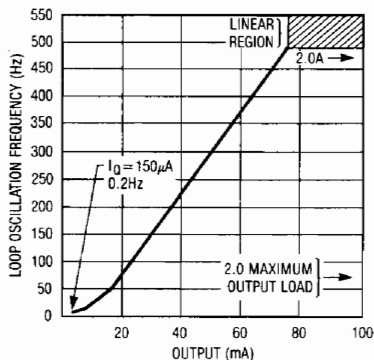
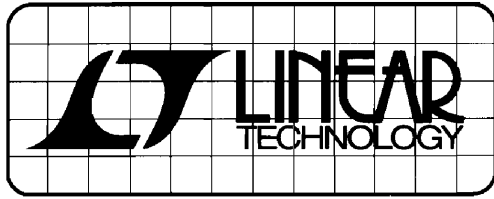


Figure 5. Output Current vs Loop Oscillation Frequency for Figure 2

For LT1070 literature call 800-637-5545. For help with an application call (408) 432-1900, Ext. 361.



DESIGN NOTES

Number 17 in a series from Linear Technology Corporation

November, 1988

Programming Pulse Generators for Flash Memories

Jim Williams

Recently introduced "flash" memories add electrical chip-erasure and reprogramming to established EPROM technology. These features make them a cost effective and reliable alternative for updatable non-volatile memory. Utilizing the electrical program-erase capability requires linear circuitry techniques. The Intel 28F256 flash memory, built on the ETOX™ process, specifies programming operation with 12V or 12.75V (faster erase/program times) amplitude pulses. These "V_{pp}" amplitudes must fall within 1.6%, and excursions beyond 14.0V will damage the device.

Providing the V_{pp} pulse requires generating and controlling high voltages within the tightly specified limits. Figure 1's circuit does this. When the V_{pp} command pulse goes low (trace A, Figure 2) the LT1072 switching regulator drives L1, producing high voltage. DC feedback occurs via R1 and R2, with AC roll-off controlled by C1 and R3-C2. The result is a smoothly rising V_{pp} pulse (trace B) which settles to the required value. The specified R1 values allow either 12V or 12.75V outputs. The 5.6V zener permits the output to return to 0V when the V_{pp} command goes high. It may be deleted in cases where a 4.5V minimum output is acceptable (see Intel 28F256 data sheet). The 0.1% resistors combine with the LT1072's tight internal reference to eliminate circuit trimming

requirements. Additionally, this circuit will not spuriously overshoot during power-up or down.

Figure 1's repetition rate is limited because the regulator must fully rise and settle for each V_{pp} command. Figure 3's circuit serves cases which require higher repetition rate V_{pp} pulses. Here, the switching regulator runs continuously, with the V_{pp} pulses generated by the A1-A2 loop. If desired, the "V_{pp} Lock" line can be driven, shutting down the regulator to preclude any possibility of inadvertent V_{pp} outputs. When V_{pp} Lock goes low (trace A, Figure 4) the LT1072 loop comes on (trace B), stabilizing at about 17V. Pulsing the V_{pp} command line low causes the 74C04 (trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V with A1 and A2 giving a scaled output (trace D). The 680pF capacitor controls loop slewing, eliminating overshoots. Figure 5 details the V_{pp} output. Trace A is the 74C04 output, with trace B showing clean V_{pp} characteristics. As in Figure 1, spurious V_{pp} outputs are suppressed during power-up or down. The diode path around A2 prevents overshoot during short circuit recovery.

A good question might be; "Why not set the switching regulator output voltage at the desired V_{pp} level and use a simple low resistance FET or bipolar switch?" Figure 6 shows that this is a potentially dangerous approach. Figure 6A shows

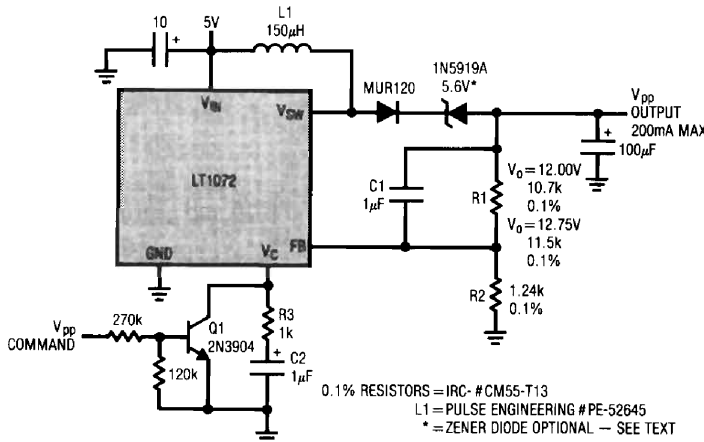


Figure 1. Basic Flash Memory V_{pp} Pulse Generator

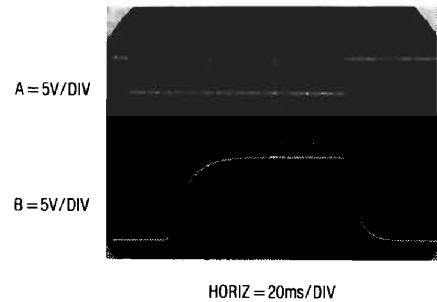


Figure 2. Waveforms for Basic Flash Memory Pulser

the clean output of a low resistance switch operating directly at the V_{pp} supply. The PC trace run to the memory chip looks like a transmission line with ill-defined termination characteristics. As such, Figure 6A's clean pulse degrades and rings badly (Figure 6B) at the memory IC's pins. Overshoot exceeds 20V, well beyond the 14V destruction level. The controlled edge times of the circuits discussed eliminate this problem. Further discussion of these and other circuits appears in LTC Application Note 31, "Linear Circuits for Digital Systems" (Available February, 1989).

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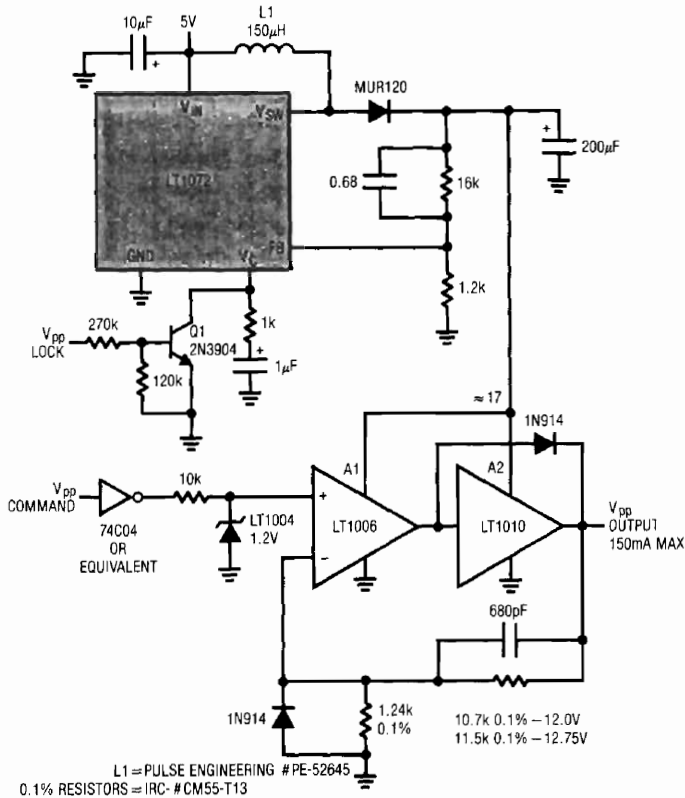


Figure 3. High Repetition Rate V_{pp} Pulse Generator

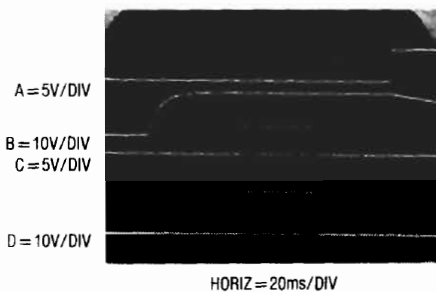


Figure 4. Operating Details of High Repetition Rate Flash Memory Pulser

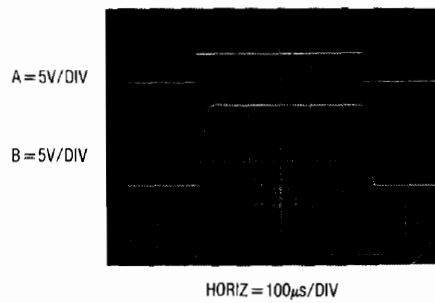


Figure 5. Expanded Scale Display of Figure 3's V_{pp} Pulse. Controlled Risetime Eliminates Overshoots.

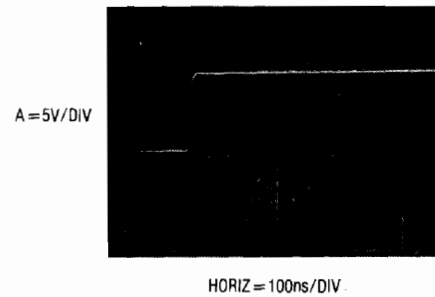
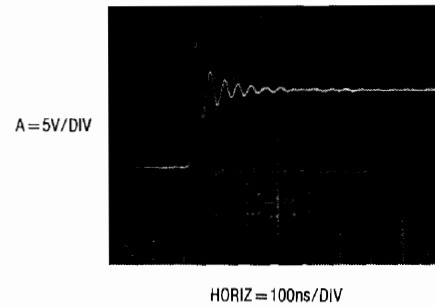


Figure 6A. An "Ideal" Flash Memory V_{pp} Pulse ...



... Figure 6B. Rings at Destructive Voltages After a PC Trace Run

For literature on LT1006, LT1010 and LT1072, call 800-637-5545. For applications help, call (408) 432-1900 Ext. 361.



DESIGN NOTES

Number 17 in a series from Linear Technology Corporation

November, 1988

Programming Pulse Generators for Flash EPROMs

Jim Williams

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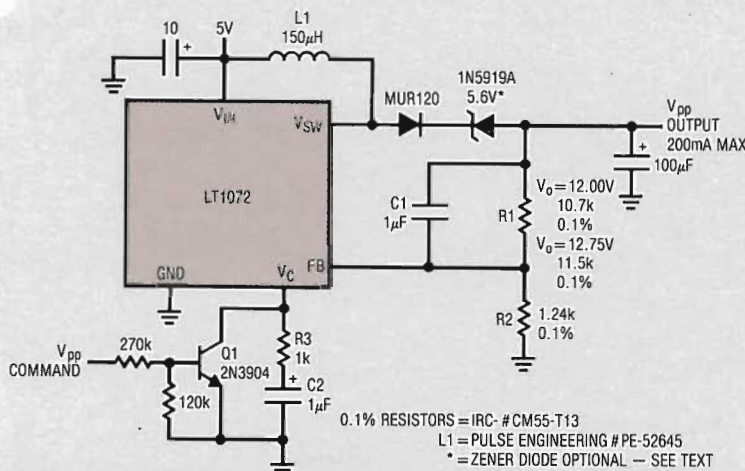


Figure 1. Basic Flash EPROM V_{pp} Pulse Generator

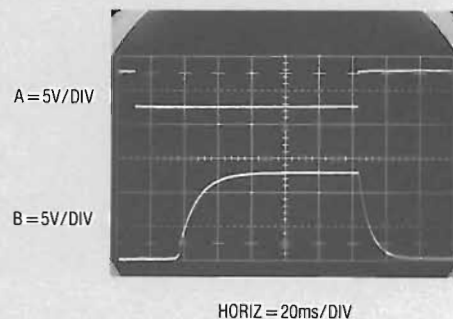


Figure 2. Waveforms for Basic Flash EPROM Pulser

the clean output of a low resistance switch operating directly at the V_{pp} supply. The PC trace run to the memory chip looks like a transmission line with ill-defined termination characteristics. As such, Figure 6A's clean pulse degrades and rings badly (Figure 6B) at the memory IC's pins. Overshoot exceeds 20V, well beyond the 14V destruction level. The controlled edge times of the circuits discussed eliminate this problem. Further discussion of these and other circuits appears in LTC Application Note 31, "Linear Circuits for Digital Systems" (Available February, 1989).

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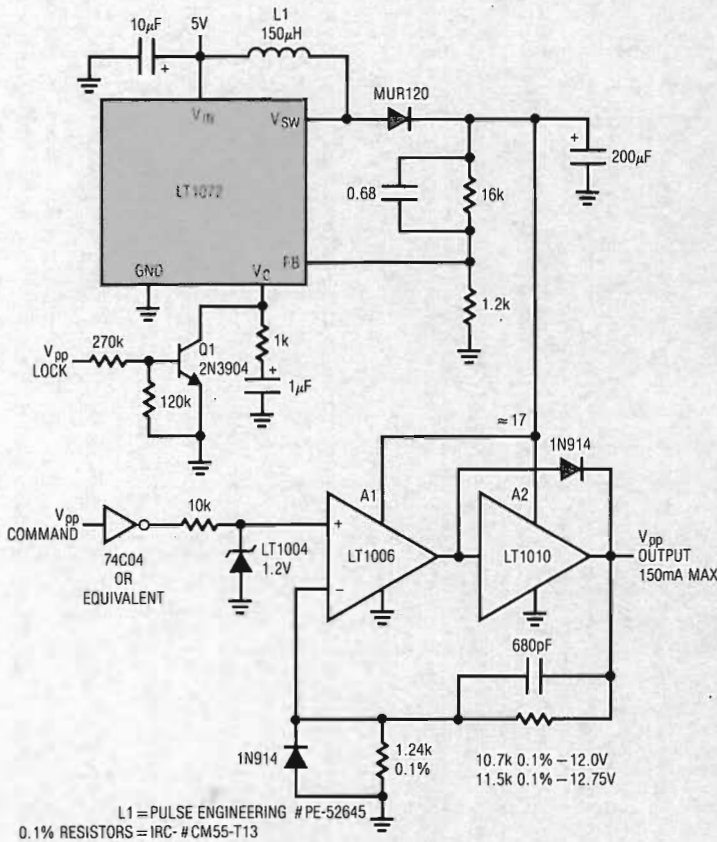


Figure 3. High Repetition Rate V_{pp} Pulse Generator

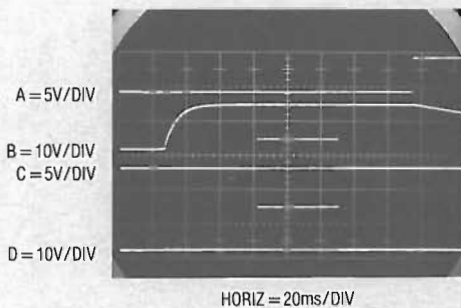
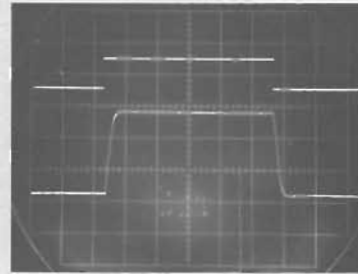


Figure 4. Operating Details of High Repetition Rate Flash EPROM Pulser

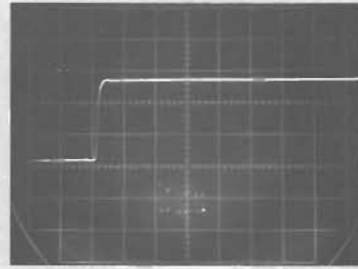
A = 5V/DIV
B = 5V/DIV



HORIZ = 100µs/DIV

Figure 5. Expanded Scale Display of Figure 3's V_{pp} Pulse. Controlled Risetime Eliminates Overshoots.

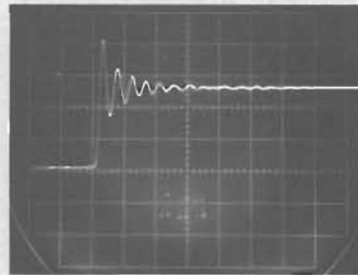
A = 5V/DIV



HORIZ = 100ns/DIV

Figure 6A. An "Ideal" Flash EPROM V_{pp} Pulse ...

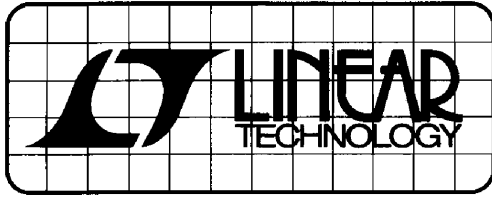
A = 5V/DIV



HORIZ = 100ns/DIV

... Figure 6B. Rings at Destructive Voltages After a PC Trace Run

For literature on LT1006, LT1010 and LT1072, call 800-637-5545. For applications help, call (408) 432-1900 Ext. 361.



DESIGN NOTES

Number 32 in a series from Linear Technology Corporation

March, 1990

A Simple Ultra-Low Dropout Regulator

Jim Williams

Linear voltage regulators with low dropout characteristics are a frequent requirement, particularly in battery powered applications. It is desirable to maintain regulation until the battery is almost entirely depleted. Regulator dropout limits significantly impact useful battery life, and as such should be minimized. Figure 1 shows dropout characteristics for a monolithic regulator, the LT1085. The $<1.5\text{V}$ dropout performance is about twice as good as standard monolithic regulators. In many cases this device will serve nicely, but applications requiring lower dropout mandate a different approach.

Figure 2's simple regulator has only 85mV dropout at 2.5A — a $13\times$ improvement. At lower currents dropout decreases to vanishingly small values. This circuit is particularly applicable in battery driven lap top computers, where multi-output

power supplies are used. In operation, the LT1431 shunt regulator adjusts its output ("collector") to whatever value is required to force circuit output to 5V . The LT1431's internal trimming eliminates the usual feedback resistors and trim-pots. Q1, the pass element, runs as a voltage overdriven source follower. This configuration offers the lowest possible dropout voltage,¹ although it does require a $+12\text{V}$ bias source for Q1's gate. This $+12\text{V}$ source is commonly present in lap top computers and similar devices because of disc drive and peripheral power requirements. Power drain on the $+12\text{V}$ supply is a few milliamperes.

*A detailed discussion of various methods for achieving low dropout appears as Appendix A ("Achieving Low Dropout") in LTC Application Note 32, "High Efficiency Linear Regulators."

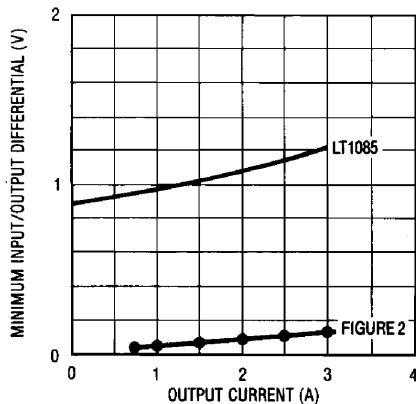


Figure 1. Dropout Performance for a Low Dropout Monolithic Regulator vs Figure 2

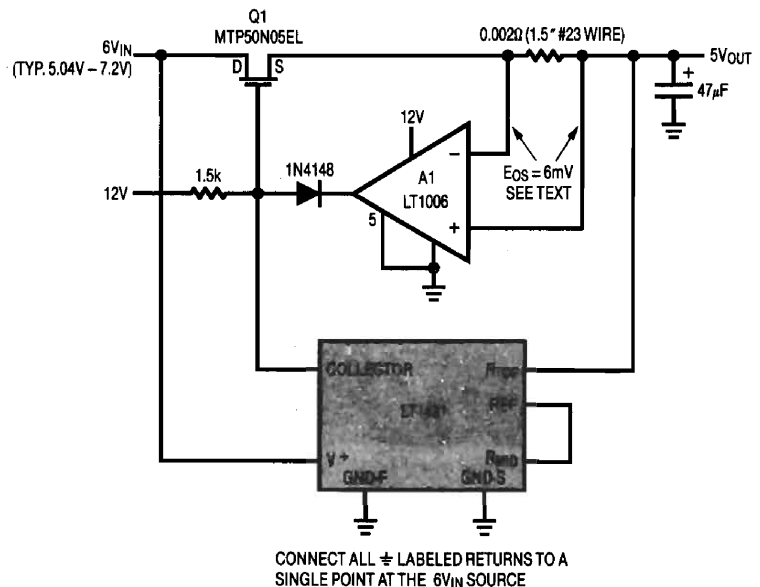


Figure 2. Ultra-Low Dropout Regulator

Providing short circuit protection without introducing significant loss requires care. A1 achieves this by sensing across a 0.002Ω shunt ($1.5''$ of #23 wire). This introduces only 6mV of drop at the circuit's 3A current limit threshold. A 6mV current limit trip point is derived by grounding A1's offset pin 5. The 6mV input offset generated at A1 by doing this is stable over time, temperature and unit-to-unit variation, and substitutions for A1 are not advisable. Currents beyond 3A cause A1 to pull low, stealing Q1's gate drive and shutting off the regulator's output. Under overload conditions A1 and Q1 form a well controlled linear current control loop with smooth limiting. Figure 3 details dropout characteristics. Results for the MTP50N05EL MOSFET specified for Q1 show only 85mV dropout, decreasing to just 8mV at 0.25A. For comparison, data for some higher resistance transistors also appears.

Q1's source follower connection makes regulator dynamics quite good compared to common source/emitter approaches. Figure 4 shows no load (Trace A low) to full load (Trace A high) response. Regulator output (Trace B) dips only 200mV and recovers quickly with clean damping. The positive slew recovery time is due to the $1.5k\Omega$ bias resistor acting against Q1's

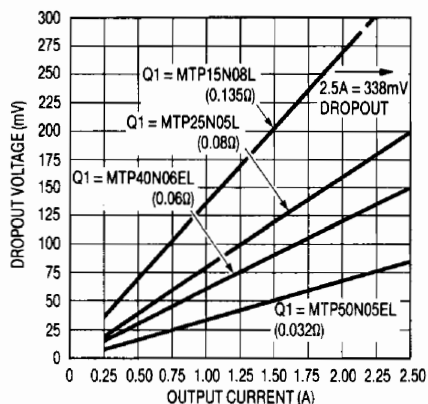


Figure 3. Dropout Characteristics for Figure 2. Q1's Saturation Directly Influences Performance.

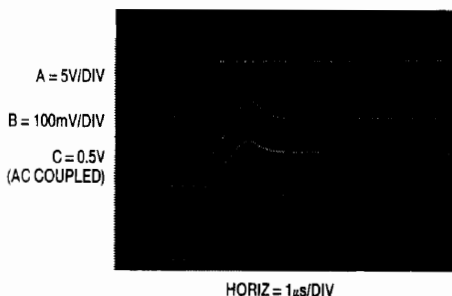


Figure 4. Transient Response for a Full Load Step. Follower Connection Provides Clean Dynamics.

input capacitance (Trace C is Q1's gate). Quicker response is possible by a reduction in this value, although current drain from the +12V supply will increase. The value used represents a good compromise. Transient recovery for load removal is also well controlled.

This regulator offers a simple solution to applications requiring extremely low dropout over a range of output currents. The performance, low parts count and lack of trimming make it an attractive alternative to other approaches. For reference, pertinent information on construction of wire shunts appears in Figures 5 and 6.

WIRE GAUGE	$\mu\Omega/\text{INCH}$
10	83
11	100
12	130
13	160
14	210
15	265
16	335
17	421
18	530
19	670
20	890
21	1000
22	1300
23	1700
24	2100
25	2700

Figure 5. Resistance vs Size for Various Copper Wire Types

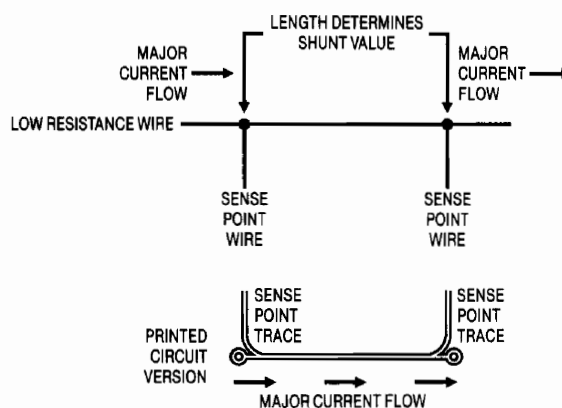


Figure 6. Detail of a Low Resistance Current Shunt

For literature on low dropout regulators, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 445.

Applications for a New Micropower, Low Charge Injection Analog Switch

Guy Hoover, William Rempfer, Jim Williams

With greater accuracy for both charge and voltage switching, the LTC201A is a superior replacement for the industry standard DG201A. In addition, the micropower LTC201A operates from a single 5V supply, and has lower on-resistance and faster switching speed. These improvements are critical to the operation of the following three circuits.

Micropower V-F Converter

Figure 1 shows a 100Hz to 1MHz voltage-to-frequency converter. This V-to-F operates from a single supply and draws only 90 μ A quiescent current, rising to 360 μ A at 1MHz. Linearity is 0.02% over a 100Hz to 1MHz range.

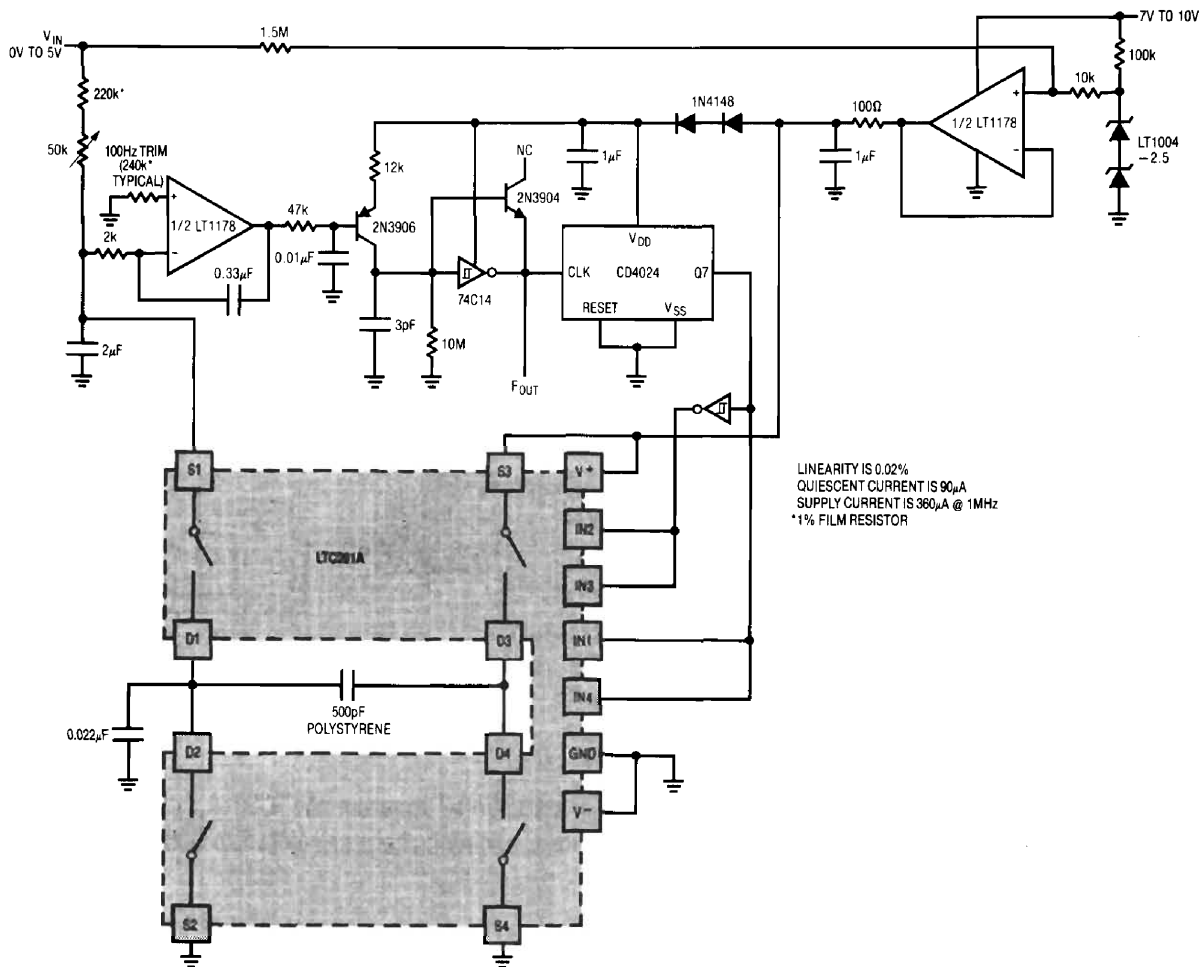


Figure 1. Micropower 100Hz to 1MHz V-to-F Converter

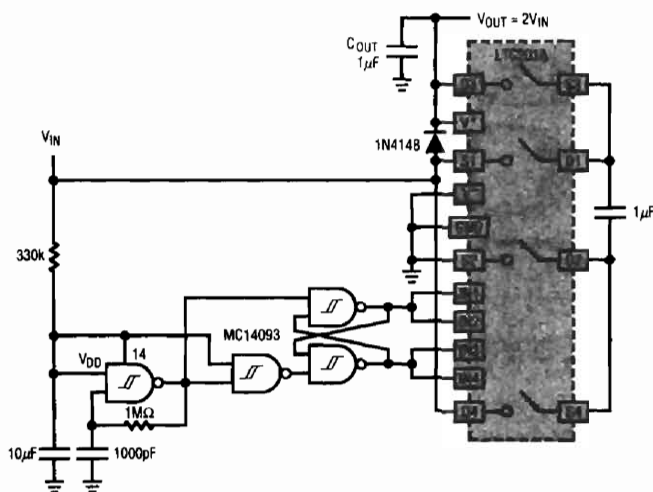


Figure 2. Micropower, 4.5V-15V Input, Voltage Doubler

The circuit consists of an oscillator, a servo amplifier and a charge pump. The oscillator's divided down output is expressed as current (charge per time) by the LTC201A-500pF combination. The input voltage is converted to current by the 220k trimmer pair. The amplifier controls the oscillator frequency to force the net value of the current into A1's summing point to zero.

The 1.5MΩ resistor between V_{IN} and the reference buffer amplifier sums a small input related voltage to the reference, improving linearity. The 0.022µF capacitor prevents excessive negative transitions at LTC201A D1-D2 pins. The series diodes in the oscillator divider supply line lower supply voltage, decreasing current consumption. The 10MΩ resistor at Q8's collector dominates node leakages ensuring low frequency operation by forcing Q8 to always source current.

Precision Voltage Doubler

The precision micropower voltage doubler of Figure 2 has an input voltage range of 4.5V to 15V. The low supply current of the LTC201A allows it to be powered directly from the input voltage. Total no load supply current of the circuit ranges from 20µA at $V_{IN}=4.5V$ to 130µA at $V_{IN}=15V$. Output impedance is only 1.2kΩ at $V_{IN}=4.5V$ and reduced to 600Ω at $V_{IN}=15V$. The accuracy of this circuit is better than 0.2% over the 4.5V to 15V input range.

The MC14093 is used to form an oscillator with complementary non-overlapping outputs. R1 and C1 determine the frequency of oscillation (roughly 1.2kHz at $V_{IN}=4.5V$). The oscillator outputs drive two sets of switches in the LTC201A and ensure that one pair of switches shuts off before the other set turns on. C_{IN} is alternately charged to V_{IN} and then stacked on top of V_{IN} to charge C_{OUT} . R2 reduces the supply voltage to the MC14093 which keeps current drain low. The diode ensures latch-free power-up for any input rise time condition.

Quad 12-Bit Sample and Hold

Figure 3's sample and hold uses the low charge injection of the LTC201A combined with the low offset voltage of the LT1014 to produce a sample to hold offset of only 0.6mV. This makes it accurate enough for 12-bit applications. Acquisition time to 0.6mV is 20µs. Aperture time is 300ns (the off time of the LTC201A). Droop rate is 2mV/ms and is limited by the I_B of the LT1014. The input range is 3.5V to -5V with ±5V supplies.

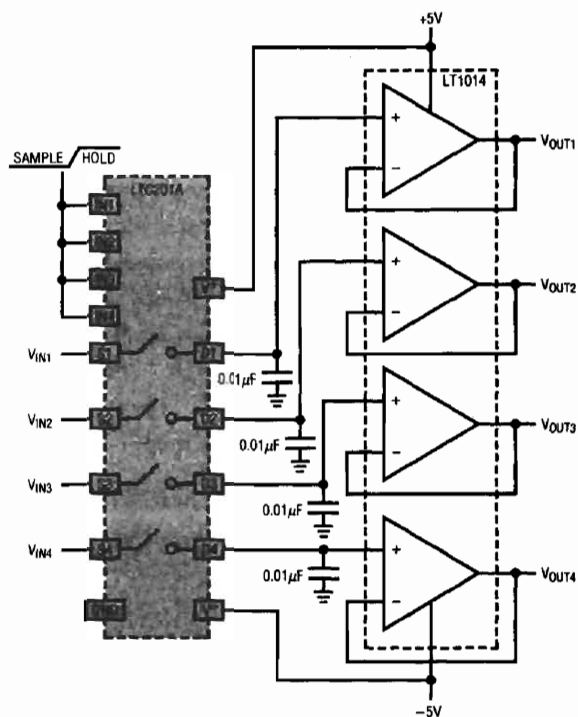


Figure 3. Quad 12-Bit Sample and Hold

For additional literature on LTC201A, call (800) 637-5545.
For applications help, call (408) 432-1900, Ext. 445.

Designing with a New Family of Instrumentation Amplifiers

Jim Williams

A new family of IC instrumentation amplifiers achieves performance and cost advantages over other alternatives. Conceptually, an instrumentation amplifier is simple. Figure 1 shows that the device has passive, fully differential inputs, a single ended output and internally set gain. Additionally, the output is delivered with respect to the reference pin, which is usually grounded. Maintaining high performance with these features is difficult, accounting for the cost-performance disadvantages previously associated with instrumentation amplifiers.

Figure 2 summarizes specifications for the amplifier family. The LTC1100 has the extremely low offset, drift, and bias current associated with chopper stabilization techniques. The LT1101 requires only 105 μ A of supply current while retaining excellent DC characteristics. The FET input

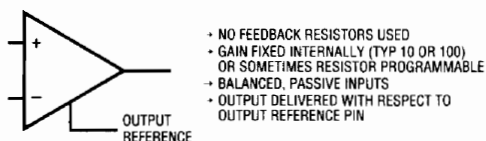


Figure 1. Conceptual Instrumentation Amplifier

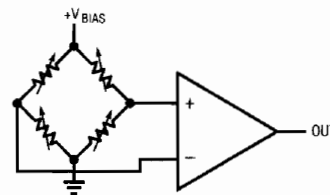
PARAMETER	CHOPPER STABILIZED LTC1100	MICROPOWER LT1101	HIGH SPEED LT1102
Offset	10 μ V	160 μ V	500 μ V
Offset Drift	100nV/ $^{\circ}$ C	2 μ V/ $^{\circ}$ C	2.5 μ V/ $^{\circ}$ C
Bias Current	50pA	8nA	50pA
Noise (0.1Hz-10Hz)	2 μ Vp-p	0.9 μ V	2.8 μ V
Gain	100	10,100	10,100
Gain Error	0.03%	0.03%	0.05%
Gain Drift	4ppm/ $^{\circ}$ C	4ppm/ $^{\circ}$ C	5ppm/ $^{\circ}$ C
Gain Non-Linearity	8ppm	8ppm	10ppm
CMRR	104dB	100dB	100dB
Power Supply	Single or Dual, 16V Max	Single or Dual, 44V Max	Dual, 44V Max
Supply Current	2.2mA	105 μ A	5mA
Slew Rate	1.5V/ μ s	0.07V/ μ s	25V/ μ s
Bandwidth	8kHz	33kHz	220kHz

Figure 2. Comparison of The New IC Instrumentation Amplifiers

LT1102 features high speed while maintaining precision. Gain error and drift are extremely low for all units, and the single supply capability of the LTC1100 and LT1101 is noteworthy.

The classic application for these devices is bridge measurement. Accuracy requires low drift, high common mode rejection and gain stability. Figure 3 shows a typical arrangement with the table listing performance features for different bridge transducers and amplifiers.

Bridge measurement is not the only use for these devices. They are also useful as general purpose circuit components, in similar fashion to the ubiquitous op amp. Figure 4 shows a voltage controlled current source with load and control voltage referred to ground. This simple, powerful circuit produces output current in strict accordance with the sign and magnitude of the control voltage. The circuit's accuracy and stability are almost entirely dependent upon resistor R. A1, biased by V_{IN} , drives current through R (in this case 10 Ω) and the load. A2, sensing differentially across R, closes a loop back to A1. The load current is constant because A1's loop forces a fixed voltage across R. The 10k-0.5 μ F combination sets rolloff, and the configuration is stable. Figure 5 shows dynamic response. Trace A is



BRIDGE TRANSDUCER	AMPLIFIER	V_{BIAS}	COMMENTS
350 Ω Strain Gage (BLH #DHF - 350)	LTC1100	10V	Highest Accuracy, 30mA Supply Current
1800 Ω Semiconductor (Motorola MPX2200AP)	LT1101	1.2V	Lower Accuracy & Cost. < 800 μ A Supply Current

Figure 3. Characteristics of Some Bridge Transducer-Amplifier Combinations

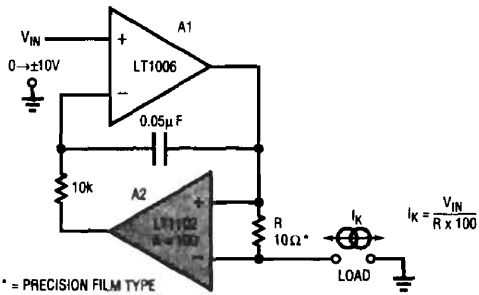


Figure 4. Voltage Programmable Current Source is Simple and Precise

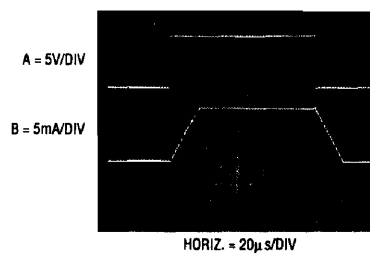


Figure 5. Dynamic Response of the Current Source

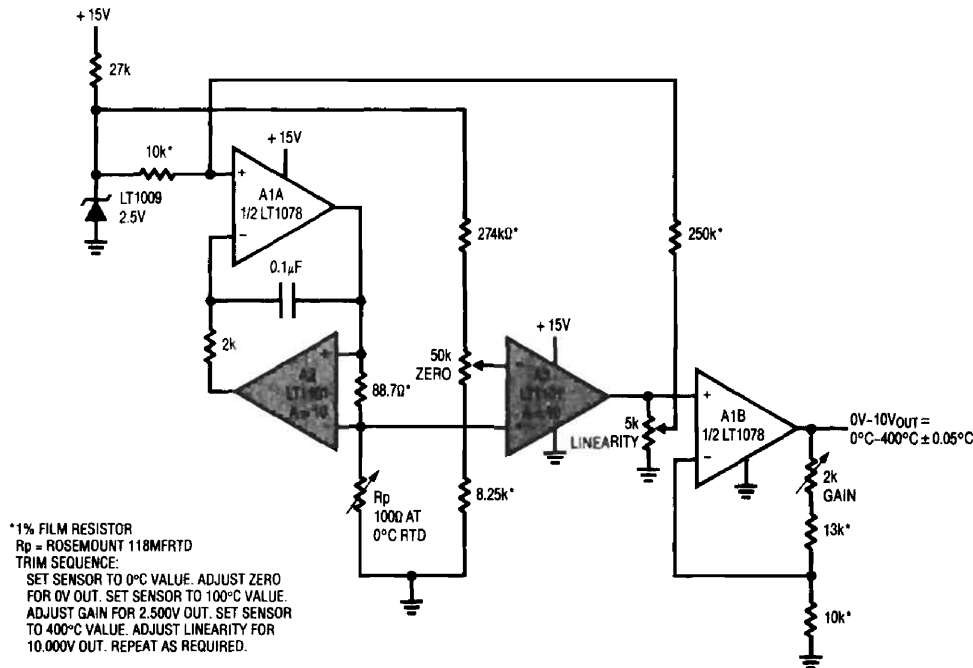


Figure 6. Linearized Platinum RTD Bridge. Feedback to Bridge from A3 Linearizes the Circuit

the voltage control input while trace B is the output current. Response is clean, with no slew residue or aberrations.

A final circuit, Figure 6, combines the current source and a platinum RTD bridge to form a complete high accuracy thermometer. A1A and A2 will be recognized as a form of Figure 4's current source. The ground referred RTD sits in a bridge composed of the current drive and the LT1009 biased resistor string. The current drive allows the voltage across the RTD to vary directly with its temperature induced resistance shift. The difference between this potential and that of the opposing bridge leg forms the bridge output. The RTD's constant current drive forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity could cause several degrees of error over the circuit's 0°C-400°C operating range. The bridge's output is fed to instru-

mentation amplifier A3, which provides differential gain while simultaneously supplying non-linearity correction. The correction is implemented by feeding a portion of A3's output back to A1's input via the 10k-250k divider. This causes the current supplied to Rp to slightly shift with its operating point, compensating sensor non-linearity to within $\pm 0.05^\circ\text{C}$. A1B, providing additional scaled gain, furnishes the circuit output. To calibrate this circuit, follow the procedure given in Figure 6.

Details of these and other instrumentation amplifier circuits may be found in LTC Application Note 43, "Bridge Circuits — Marrying Gain and Balance."

For literature on our Instrumentation Amplifiers, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 456

A Simple Ultra-Low Dropout Regulator

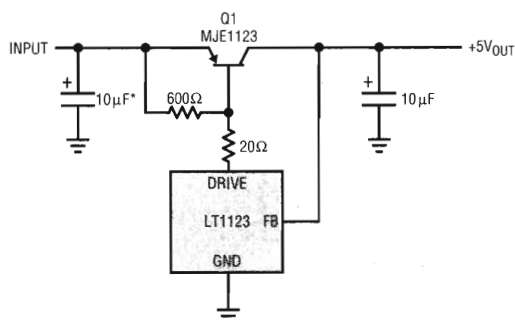
Jim Williams

Switching regulator post regulators, battery powered apparatus, and other applications frequently require low drop-out linear regulators. Often, battery life is significantly affected by the regulator's dropout performance. Figure 1's simple circuit offers lower dropout voltage than any monolithic regulator. Dropout is below 50mV at 1A, increasing to only 450mV at 5A. Line and load regulation are within 5mV, and initial output accuracy is inside 1%. Additionally, the regulator is fully short circuit protected, and has a no load quiescent current of 600 μ A.

Circuit operation is straightforward. The 3-pin LT1123 regulator (TO-92 package) servo controls Q1's base to maintain its feedback pin (FB) at 5V. The 10 μ F output capacitor provides frequency compensation. If the circuit is located more than six inches from the input

source the optional 10 μ F capacitor should bypass the input. The optional 20 Ω resistor limits LT1123 power dissipation and is selected based upon the maximum expected input voltage (see Figure 2).

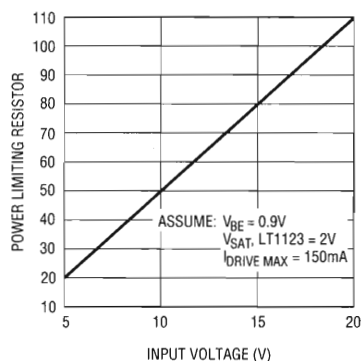
Normally, configurations of this type offer unpredictable short circuit protection. Here, the MJE1123 transistor shown has been specially designed for use with the LT1123. Because of this, beta based current limiting is practical. Excessive output current causes the LT1123 to pull down harder on Q1 until beta limiting occurs. Under these conditions the controlled pull down current combines with Q1's beta and safe operating area characteristics to provide reliable short circuit limiting. Figure 3 details current limit characteristics for 30 randomly selected transistors.



* = OPTIONAL (SEE TEXT)
MJE1123 = MOTOROLA

DN44 - TA01

Figure 1. The Ultra-Low Dropout Regulator. LT1123 Combines with Specially Designed Transistor for Lowest Dropout and Short Circuit Protection.



DN44 - TA04

Figure 2. LT1123 Power Dissipation Limiting Resistor Value vs Input Voltage

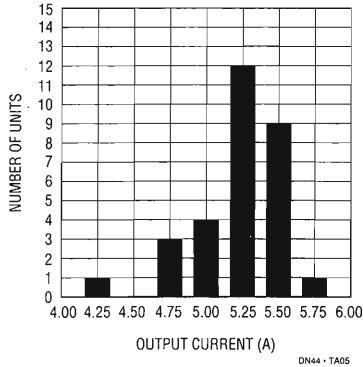


Figure 3. Short Circuit Current for 30 Randomly Selected MJE1123 Transistors at $V_{IN} = 7V$

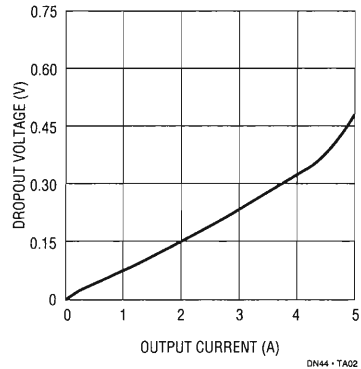


Figure 4. Dropout Voltage vs Output Current

Figure 4 shows dropout characteristics. Even at 5A, dropout is about 450mV, decreasing to only 50mV at 1A. Monolithic regulators cannot approach these figures, primarily because monolithic power transistors do not offer Q1's combination of high beta and excellent saturation. For comparison, Figure 5 compares the circuits performance against some popular monolithic regulators. Dropout is ten times better than 138 types, and significantly better than the other types shown. Because of Q1's high beta, base drive loss is only 1%-2% of output current, even at full 5A output. This maintains high efficiency under the low $V_{IN} - V_{OUT}$ conditions the circuit will typically operate at. As an exercise, the MJE1123 was replaced with a 2N4276, a Germanium device. This combination provided even lower dropout performance, although current limit characteristics cannot be guaranteed.

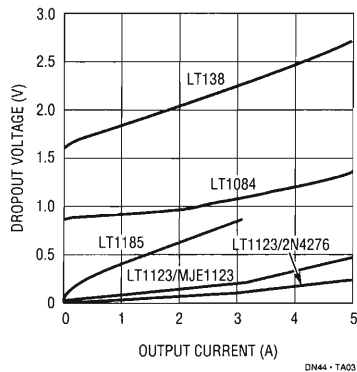


Figure 5. Dropout Voltage vs Output Current for Various Regulators

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Signal Conditioning for Platinum Temperature Transducers

Jim Williams

High accuracy, stability, and wide operating range make platinum RTDs (resistance temperature detectors) popular temperature transducers. Signal conditioning these devices requires care to utilize their desirable characteristics. Figure 1's bridge based circuit is highly accurate and features a ground referred RTD. The ground connection is often desirable for noise rejection. The bridge's RTD leg is driven by a current source while the opposing bridge branch is voltage biased. The current drive allows the voltage across the RTD to vary directly with its temperature induced resistance shift. The difference between this potential and that of the opposing bridge leg forms the bridge's output.

A1A and instrumentation amplifier A2 form a voltage controlled current source. A1A, biased by the LT1009

reference, drives current through the 88.7Ω resistor and the RTD. A2, sensing differentially across the 88.7Ω resistor, closes a loop back to A1A. The $2k-0.1\mu F$ combination sets amplifier rolloff, and the configuration is stable. Because A1A's loop forces a fixed voltage across the 88.7Ω resistor, the current through R_p is constant. A1's operating point is primarily fixed by the $2.5V$ LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity could cause several degrees of error over the circuit's $0^\circ C-400^\circ C$ operating range. The bridge's output is fed to instrumentation amplifier A3, which provides differential gain while simultaneously supplying non-linearity

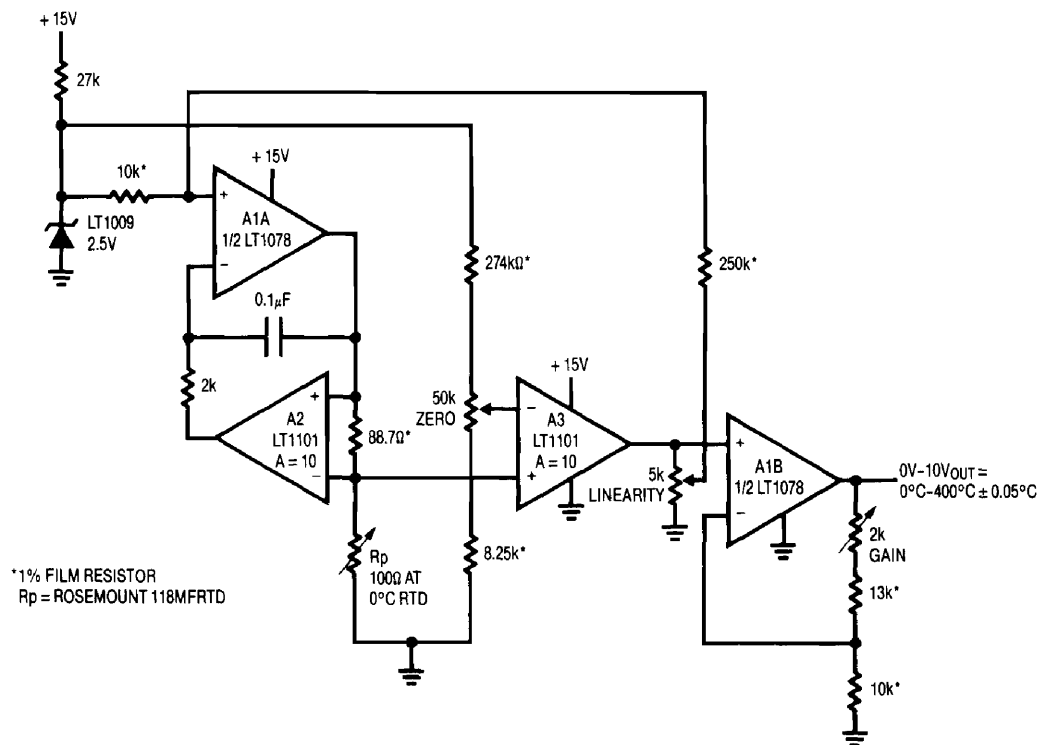


Figure 1. Linearized Platinum RTD Bridge. Feedback to Bridge from A3 Linearizes the Circuit.

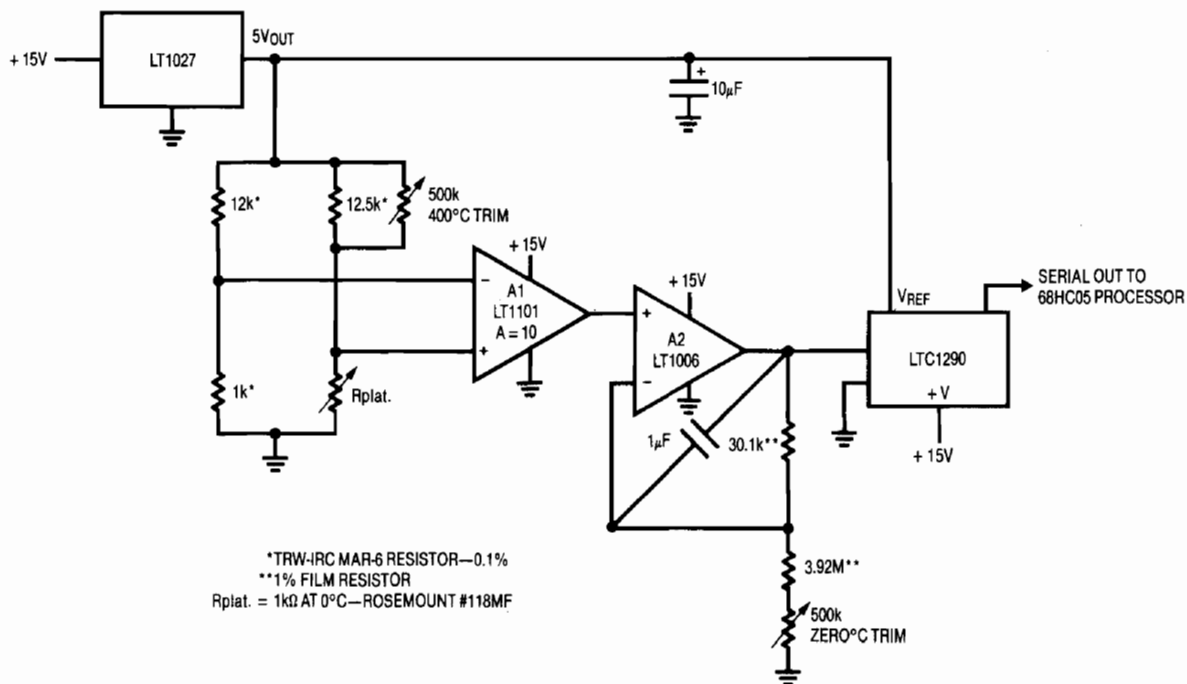


Figure 2. Digitally Linearized Platinum RTD Signal Conditioner

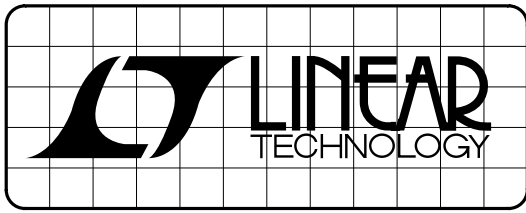
correction. The correction is implemented by feeding a portion of A3's output back to A1's input via the 10k-250k divider. This causes the current supplied to Rp to slightly shift with its operating point, compensating sensor non-linearity to within $\pm 0.05^\circ\text{C}$. A1B, providing additional scaled gain, furnishes the circuit output.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432k) for Rp. Set the box to the 0°C value (100.00Ω) and adjust the zero trim for a 0.00V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 249.0Ω (400.00°C) and trim the linearity adjustment for a 10.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within $\pm 0.05^\circ\text{C}$. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω . This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and has a very small error term.

The previous example relies on analog techniques to achieve a precise, linear output from the platinum RTD bridge. Figure 2 uses digital corrections to obtain similar results. A processor is used to correct residual RTD non-linearities. The bridges inherent non-linear output is also accommodated by the processor.

The LT1027 drives the bridge with 5V. The bridge differential output is extracted by instrumentation amplifier A1. A1's output, via gain scaling stage A2, is fed to the LTC1290 12-bit A-D. The LTC1290's raw output codes reflect the bridges non-linear output versus temperature. The processor corrects the A-D output and presents linearized, calibrated data out. RTD and resistor tolerances mandate zero and full scale trims, but no linearity correction is necessary. A2's analog output is available for feedback control applications. The complete software code for the 68HC05 processor, developed by Guy M. Hoover, appears in Application Note 43.

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DESIGN NOTES

Gain Trimming In Instrumentation Amplifier Based Systems – Design Note 51

Jim Williams

Gain trimming is almost always required in instrumentation amplifier based systems. Gain uncertainties, most notable in transducers, necessitate such a trim.

Figure 1, a conceptual system, shows several points as candidates for the trim. In practice, only one of these must actually be used. The appropriate trim location varies with the individual application.

Figure 2 approaches gain trimming by altering transducer excitation. The gain trim adjustment results in changes in the LT1010's output. The LT1027 reference

and LT1097 ensure output stability. Transducer output varies with excitation, making this a viable approach. It is important to consider that gain "lost" by reducing transducer drive translates into reduced signal-to-noise ratio. As such, gain reduction by this method is usually limited to small trims, e.g. 5-10%. Similarly, too much gain introduced by this method can cause excessive transducer drive, degrading accuracy. The transducer manufacturer's data sheet should list the maximum permissible drive for rated accuracy.

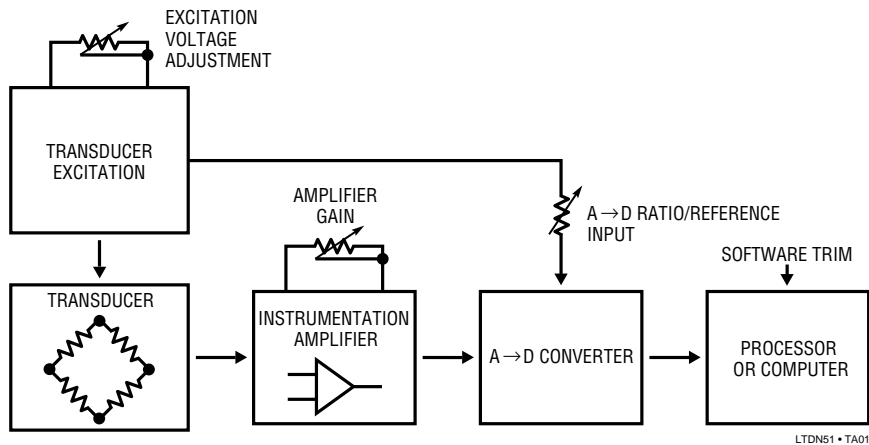


Figure 1. Conceptual Transducer Signal Conditioning Path Showing Gain Trimming Possibilities. In Practice, Only One Adjustment Is Required.

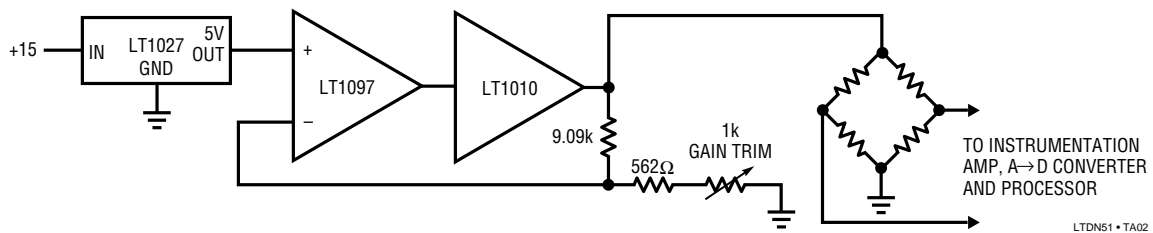


Figure 2. Gain Trimming by Adjustment of Transducer Excitation. This Method is Useable for Small (5-10%) Trims. Large Trims Will Cause Excessive Transducer Power Dissipation or "Starved" Outputs.

Figure 3 adjusts gain in the instrumentation amplifier stage. The fixed gain LT1101 instrumentation amplifier feeds a second amplifier where the trim occurs. As both cases show, the gain trim may be up or down. A secondary benefit of this trim scheme is that it permits optional offset summing and filtering. Note that either the inverter or follower may be set up for gain addition or reduction. The sole limitation is the signal polarity reversal imposed by the inverter case. This may be corrected by reversing the instrumentation amplifiers' inputs.

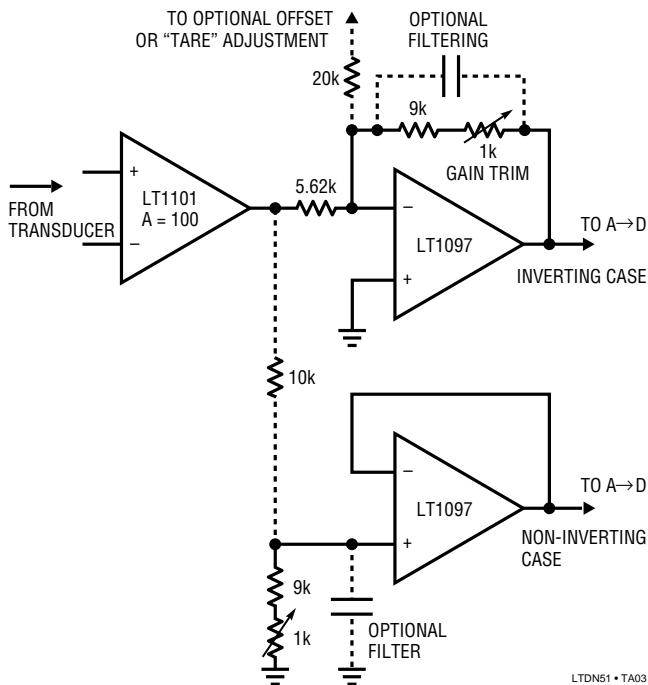


Figure 3. Gain Trimming at the Instrumentation Amplifier. A Second Stage Permits Trimming Gain Up or Down, and Allows Filtering and Offsets to Be Summed In.

A final hardware based gain trim is shown in Figure 4. Here, the A→D reference input is scaled to the appropriate voltage by the op amp and associated components. The op amp input is usually the transducer excitation voltage or, in cases where this is not possible, a reference.

One final way to trim gain is in software. If a processor is involved in the system this is a viable alternative. The software trim does a simple code conversion on the A→D output. When using this approach utilize as much of the analog components' dynamic range as possible to avoid signal-to-noise degradation.

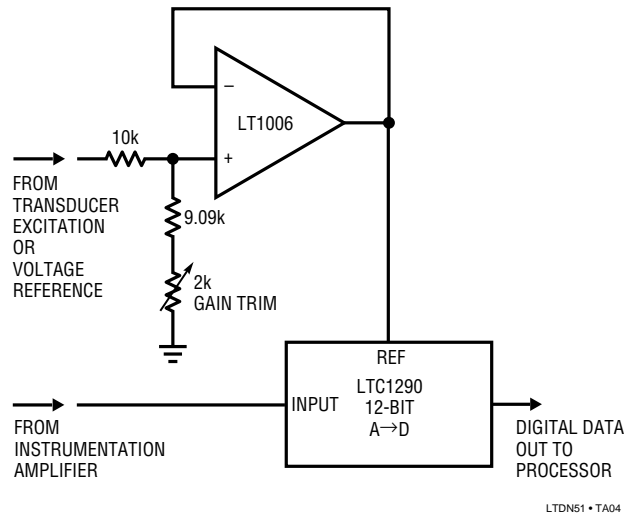


Figure 4. Gain Trimming By Adjustment of the A→D Reference Input Voltage

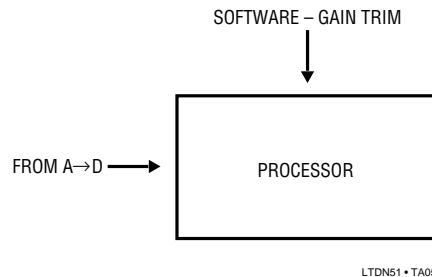
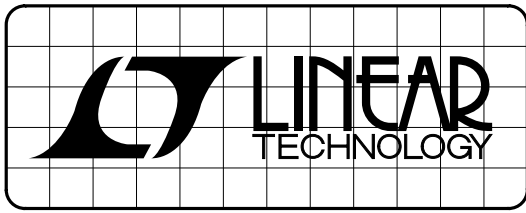


Figure 5. Software Based Trimming

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DESIGN NOTES

DC-DC Converters for Portable Computers – Design Note 52

Steve Pietkiewicz

Jim Williams

Portable computers require simple and efficient converters for +5V power and display driving. A regulated 5V supply can be generated from two “AA” cells using the circuit shown in Figure 1. U1, an LT1073-5 micropower DC-DC converter, is arranged as a step-up, or “boost” converter. The 5V output, monitored by U1’s SENSE pin, is internally divided down and compared to a 212mV reference voltage inside the device. U1’s oscillator turns on when the output drops below 5V, cycling the switch on and off at a 19kHz rate. This action alternately causes current to build up in L1, then dump into C1 through D1, increasing the output voltage. When the output reaches 5V, the oscillator turns off. The gated oscillator provides the mechanism to keep the output at a constant 5V. R1 invokes the current limit feature of the LT1073, limiting peak switch current to 1A. U1 limits switch current by turning off the switch when the current reaches the programmed limit set by R1. Switch “on” time, therefore, decreases as V_{IN} is increased. Switch “off” time is not affected. This scheme keeps peak switch current constant over the entire input voltage range, allowing maximum energy transfer to occur at

low battery voltage without exceeding L1’s maximum current rating at high battery voltage.

The circuit delivers 5V at 150mA from an input range of 3.5V to 2.0V. Efficiency measures 80% at 3.0V, decreasing to 70% at 2.0V for load currents in the 15mA to 150mA range. Output ripple measures 170mVp-p and no-load quiescent current is just 135 μ A.

A –24V LCD bias generator is shown in Figure 2. In this circuit U1 is an LT1173 micropower DC-DC converter. The 3V input is converted to +24V by U1’s switch, L1, D1, and C1. The switch pin (SW1) then drives a charge pump composed of C2, C3, D2, and D3 to generate –24V. Line regulation is less than 0.2% from 3.3V to 2.0V inputs. Load regulation, although it suffers somewhat since the –24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2.0V input at 73% efficiency.

If greater output power is required, Figure 2’s circuit can be driven from a +5V source. R1 should be changed to

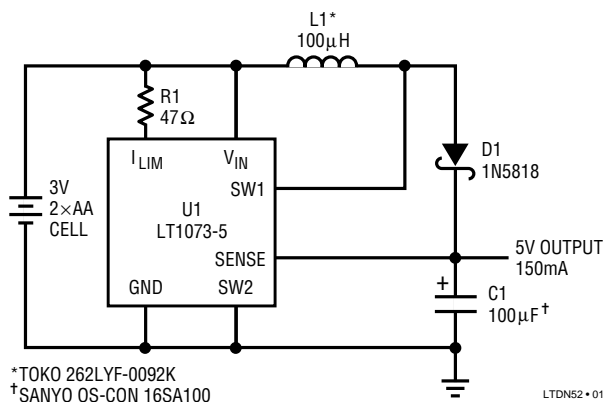


Figure 1. Two “AA” Cell to 5V Step-Up Converter Delivers 150mA

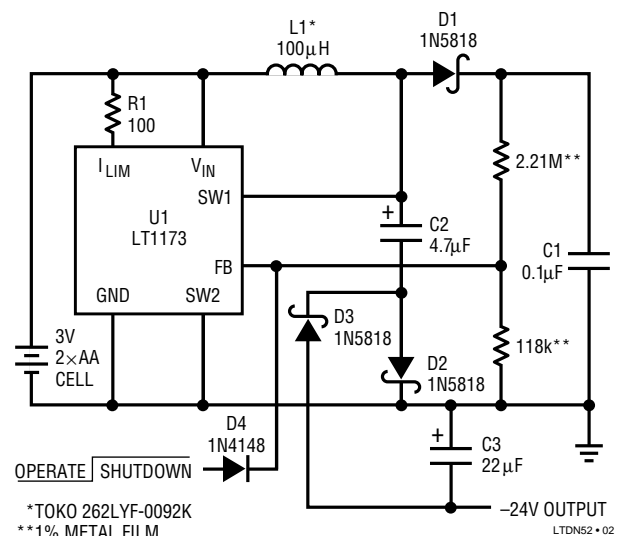


Figure 2. DC to DC Converter Generates –24V from 3V or 5V

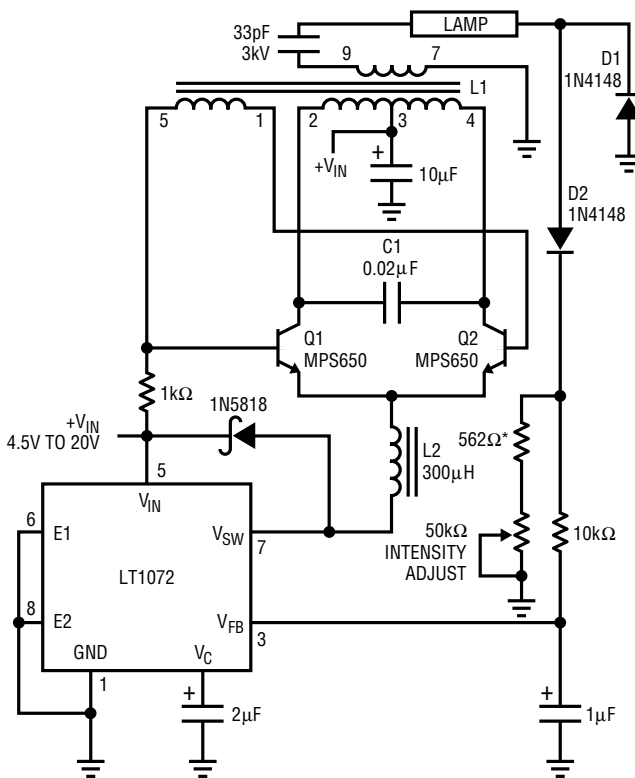
47Ω and C3 to 47μF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing the anode of D4 to a logic high, forcing the feedback pin of U1 to go above the internal reference voltage of 1.25V. Shutdown current is 110μA from the input source and 36μA from the shutdown signal.

Current generation portables require back lit LCD displays using cold cathode fluorescent lamps (CCFLs). Figure 3 provides 78% efficiency with full control over lamp brightness. 82% efficiency is possible if the LT1072 is driven from a low voltage (e.g. 3V-5V) source. Additional benefits include a 4.5V to 20V supply range and low radiated power due to sine wave based operation.

L1 and the transistors comprise a current driven Royer class converter which oscillates at a frequency primarily set by L1's characteristics and the 0.02μF capacitor. LT1072 driven L2 sets the magnitude of the Q1-Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains current flow when the LT1072 is off.

The 0.02μF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors. L1 furnishes voltage step-up, and about 1400Vp-p appears at its secondary. Current flows through the 33pF capacitor into the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across these resistors represents 1/2 the lamp current. This signal is filtered by the 10k-1μF pair and presented to the LT1072's feedback pin. This connection closes a control loop which regulates lamp current. The 2μF capacitor at the LT1072's V_C pin provides stable loop compensation. The loop forces the LT1072 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may

be varied with the potentiometer. The constant current drive allows full 0-100% intensity control with no lamp dead zones or "pop-on" at low intensities. Additionally, lamp life is enhanced because current cannot increase as the lamp ages. Detailed information on this circuit appears in LTC Application Note 45, "Measurement and Control Circuit Collection."

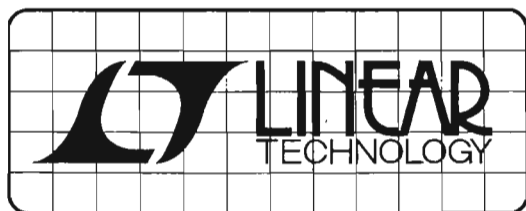


- C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FPK 2 (GERMAN) RECOMMENDED.
- L1 = SUMIDA 6345-020 OR COILTRONIX CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONIX UNIT
- L2 = COILTRONIX CTX300-4
- * = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

LTDN52 • 03

Figure 3. Cold Cathode Fluorescent Lamp Power Supply

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DESIGN NOTES

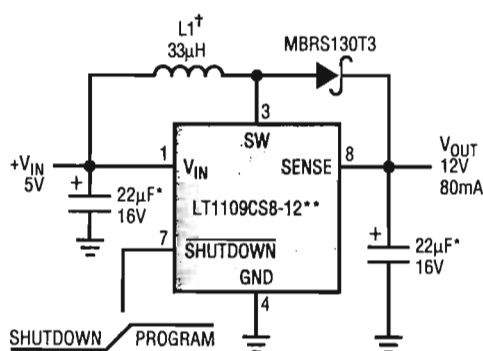
A Simple, Surface Mount Flash Memory Vpp Generator – Design Note 58

Steve Pietkiewicz
Jim Williams

“Flash” type memories add electrical chip-erase and reprogramming to established EPROM technology. These features make them a cost effective and reliable alternative for updatable non-volatile memory. Utilizing the electrical program-erase capability requires linear circuitry techniques. Intel flash memory, built on the ETOX™ process, specifies programming operation with 12V amplitude pulses. These “Vpp” amplitudes must fall within tight tolerances, and excursions beyond 14.0V will damage the device.

ETOX is a trademark of Intel Corporation.

Providing the Vpp pulse requires generating and controlling high voltages within the tightly specified limits. Figure 1’s circuit does this. When the Vpp command pulse goes high (trace A, Figure 2) the LT1109 switching regulator drives L1, producing high voltage. DC feedback occurs via the regulator’s sense pin. The result is a smoothly rising Vpp pulse (trace B) which settles to the required value. Trace C, a time and amplitude expanded version of trace B, details the desired settling to 12V. Artifacts of the switching regulator’s action are discernible, although no overshoot or poor dynamics are displayed.



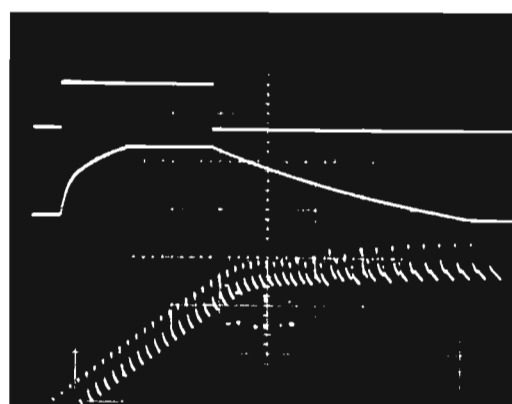
† L1 = SUMIDA CD54-330N (708-956-0666)
* HILTON CSTDD226M016TC (813-371-2600)
** USE LT1109A FOR 120mA OUTPUT (CONSULT LTC FACTORY)

DN58 - TA02

TRACE A = 5V/DIV

TRACE B = 5V/DIV

TRACE C = 0.1V/DIV
(OUTPUT)



A & B HORIZ = 1 ms/DIV
C HORIZ = 50µs/DIV

DN58 - TA03

Figure 1. All Surface Mount Flash Memory Vpp Generator

Figure 2. Waveforms for the Flash Memory Pulser Show No Overshoot

This circuit is well suited for providing V_{pp} power to flash memory. All associated components, including the inductor, are surface mount devices. As such, the complete circuit occupies very little space (see Figure 3). In the shutdown mode the circuit pulls only $300\mu A$. Output voltage goes to V_{CC} minus a diode drop when the converter is in shutdown mode. This is an acceptable and specified condition for flash memories and does not harm the memory. A 0V output is possible by placing a 5.6V Zener diode in series with the output rectifier (Figure 4A). An alternative configuration, suggested by J. Dutra of LTC, AC couples the output to achieve a 0V output (Figure 4B). Both of these methods add component count, decrease efficiency and slightly limit available output current. They are unnecessary unless the user desires a 0V output on the V_{pp} line.

A good question might be; "Why not set the switching regulator output voltage at the desired V_{pp} level and use a simple low resistance FET or bipolar switch?" This is a potentially dangerous approach. Figure 5 shows the clean output of a low resistance switch operating directly at the V_{pp} supply. The PC trace run to the memory chip looks like a transmission line with ill-defined termination characteristics. As such, Figure 5's clean pulse degrades and rings badly (Figure 6) at the memory IC's pins. Overshoot exceeds 20V, well beyond the 14V destruction level. The controlled edge times of the circuit discussed eliminate this problem. Further discussion of this and other circuits appears in LTC Application Note 31, "Linear Circuits for Digital Systems" and LTC Demo Manual DC019, "Flash Memory V_{pp} Generator."



Figure 3. Simple Flash Memory Pulser Uses All Surface Mount Components

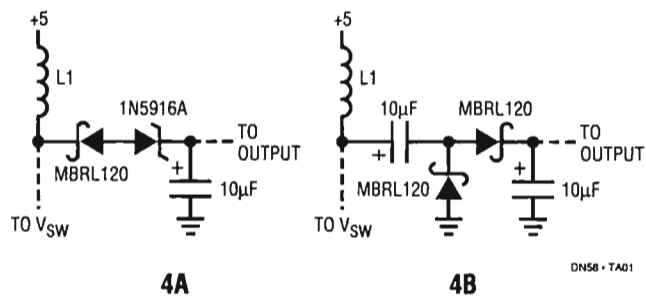


Figure 4. Two Arrangements for Obtaining a 0V Output

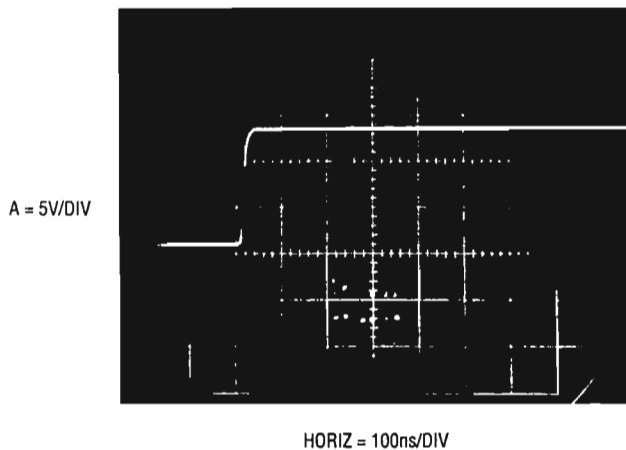


Figure 5. An "Ideal" Flash EPROM V_{pp} Pulse

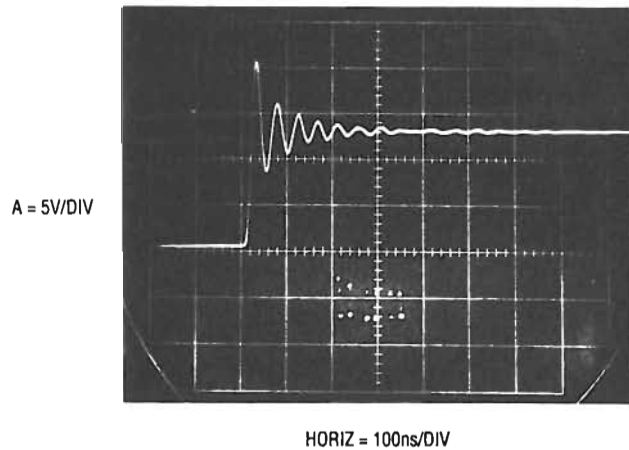
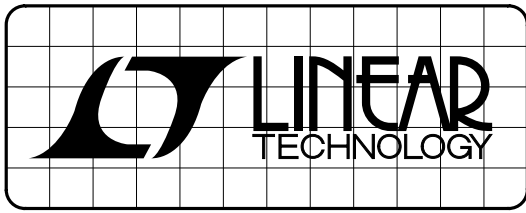


Figure 6. Rings at Destructive Voltages After a PC Trace Run

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DESIGN NOTES

A Broadband Random Noise Generator – Design Note 70

Jim Williams

Filter, audio and RF communication testing often requires a random noise source. The circuit in Figure 1 provides an RMS amplitude regulated noise source with selectable bandwidth. The RMS output is 300mV with a 1kHz to 5MHz bandwidth selected in decade ranges.

The A1 amplifier, biased from the LT1004 reference, provides optimum drive for D1, the noise source. AC coupled A2 takes a broadband gain of 100. The A2 output feeds a gain control stage via a simple selectable lowpass filter. The filter's output is applied to LT1228 A3, an operational

transconductance amplifier. A3's output feeds LT1228 A4, a current feedback amplifier. A4's output, the circuit's output, is sampled by the A5 based gain control configuration. This closes a gain control loop back at A3. A3's I_{SET} input current controls its gain, allowing overall output level control.

To adjust this circuit, place the filter in the 1kHz position and trim the 5k potentiometer for maximum negative bias at A3, pin 5.

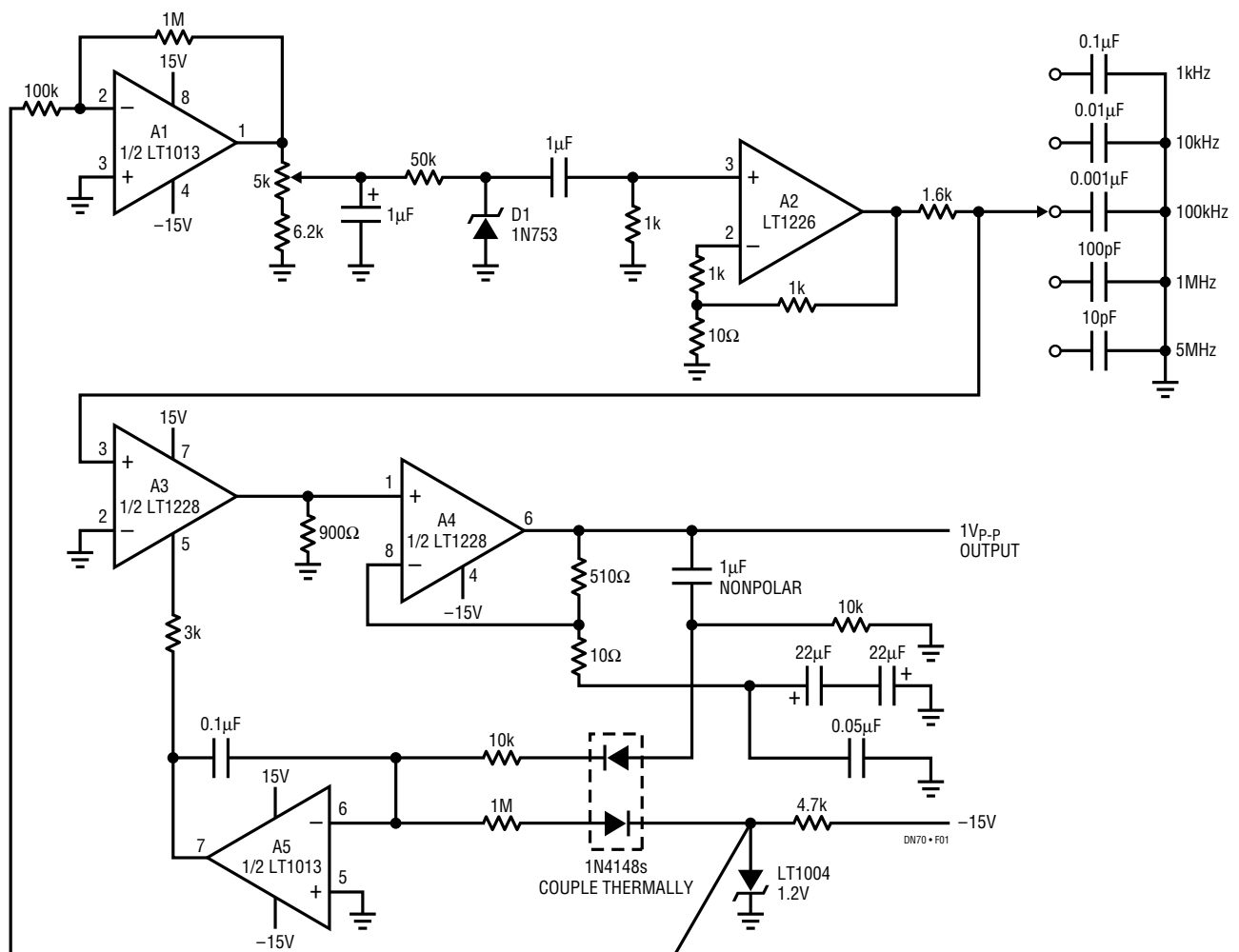


Figure 1. Random Noise Generator with Selectable Bandwidth and RMS Voltage Regulation

Figure 2 shows noise at a 1MHz bandpass while Figure 3 plots amplitude vs RMS noise in the same bandpass. Figure 4 plots similar information at full bandwidth. RMS output is essentially flat to 1.5MHz with about ± 2 dB control to 5MHz before sagging badly.

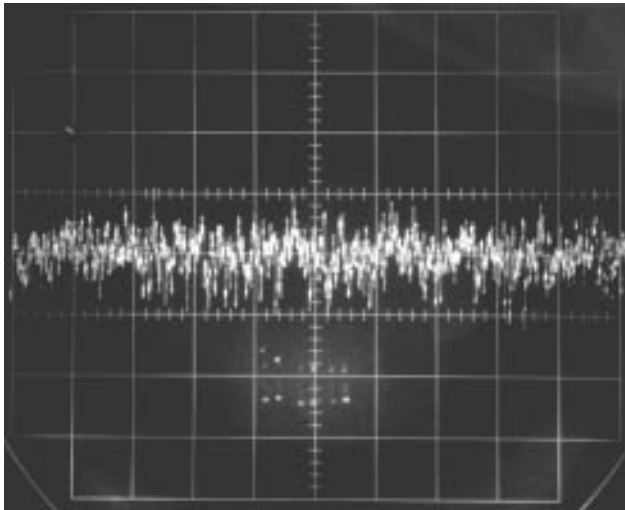
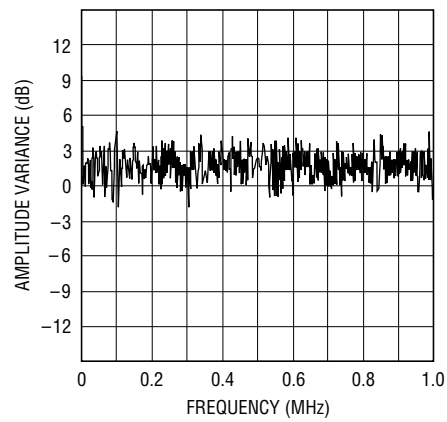
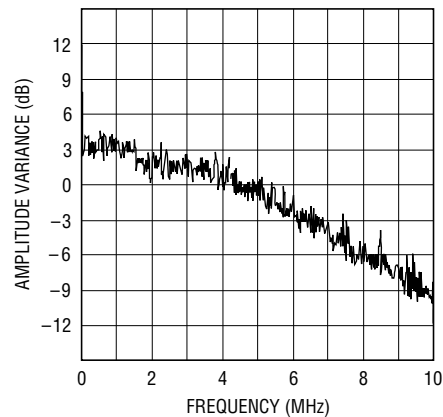


Figure 2. Figure 1's Output in the 1MHz Filter Position



DN70 • F03

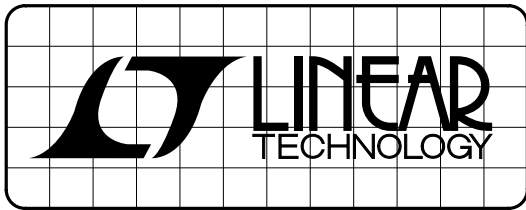
Figure 3. RMS Amplitude vs Frequency for the Random Noise Generator Is Essentially Flat to 1MHz.



DN70 • F04

Figure 4. RMS Amplitude Holds Within ± 2 dB Before Sagging Beyond 5MHz

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DESIGN NOTES

New Comparators Feature Micropower Operation Under All Conditions – Design Note 137

Jim Williams

Some micropower comparators have operating modes that allow excessive current drain. In particular, poorly designed devices can conduct large transient currents during switching. Such behavior causes dramatically increased power drain with rising frequency, or when the inputs are nearly balanced, as in battery monitoring applications.

Figure 1 shows a popular micropower comparator's current consumption during switching. Trace A is the input pulse, trace B is the output response and trace C is the supply current. The device, specified for micropower level supply drain, pulls 40mA during switching. This undesirable surprise can upset a design's power budget or interfere with associated circuitry's operation.

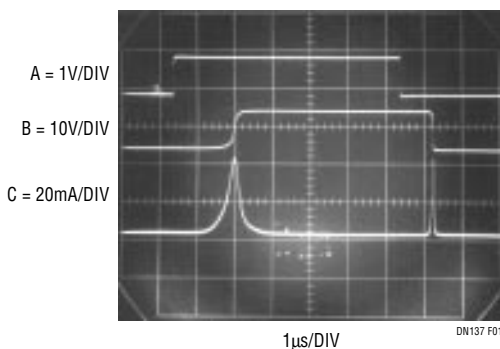


Figure 1. Poorly Designed “Micropower” Comparator Pulls Huge Currents During Transitions. Result Is Excessive Current Consumption with Frequency

The LTC[®]1440 series comparators are true micropower devices. They eliminate current peaking during switching, resulting in greatly reduced power consumption versus frequency, or when the inputs are nearly balanced. Figure 2's plot contrasts the LTC1440's power consumption versus frequency with that of another comparator specified as a micropower component. The LTC1440 has about 200 times lower current consumption at higher frequencies, while maintaining a significant advantage below 1kHz.

Table 1 shows some LTC1440 family characteristics. A voltage reference and programmable hysteresis are included in some versions, with 5µs response time for all devices.

LTC and LT are registered trademarks of Linear Technology Corporation.

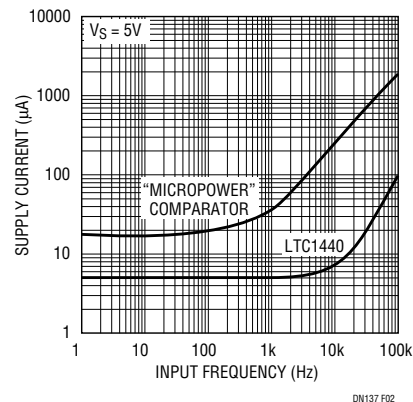


Figure 2. The LTC1440 Family Draws 200 Times Lower Current at Frequency Than Another Comparator

Table 1. Some Characteristics of the LTC1440 Family of Micropower Comparators

PART NUMBER	NUMBER OF COMPARATORS	REFERENCE	PROGRAMMABLE HYSTERESIS	PACKAGE	PROP. DELAY (100mV OVERDRIVE)	SUPPLY RANGE	SUPPLY CURRENT
LTC1440	1	1.182V	Yes	8-Lead PDIP, SO	5µs	2V to 11V	4.7µA
LTC1441	2	No	No	8-Lead PDIP, SO	5µs	2V to 11V	5.7µA
LTC1442	2	1.182V	Yes	8-Lead PDIP, SO	5µs	2V to 11V	5.7µA
LTC1443	4	1.182V	No	16-Lead PDIP, SO	5µs	2V to 11V	8.5µA
LTC1444	4	1.221V	Yes	16-Lead PDIP, SO	5µs	2V to 11V	8.5µA
LTC1445	4	1.221V	Yes	16-Lead PDIP, SO	5µs	2V to 11V	8.5µA

The new devices permit high performance circuitry with low power drain. Figure 3's quartz oscillator, using a standard 32.768kHz crystal, starts under all conditions with no spurious modes. Current drain is only 9 μ A at a 2V supply.

Figure 4's voltage-to-frequency converter takes full advantage of the LTC1441's low power consumption under dynamic conditions. A 0V to 5V input produces a 0Hz to 10kHz output, with 0.02% linearity, 60ppm/ $^{\circ}$ C drift and 40ppm/V supply rejection. Maximum current consumption

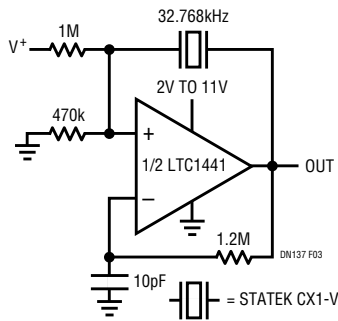


Figure 3. 32.768kHz "Watch Crystal" Oscillator Has No Spurious Modes. Circuit Pulls 9 μ A at $V_S = 2V$

tion is only 26 μ A, 100 times lower than currently available circuits. C1 switches a charge pump, comprising Q5, Q6 and the 100pF capacitor, to maintain its negative input at 0V. The LT1004s and associated components form a temperature-compensated reference for the charge pump. The 100pF capacitor charges to a fixed voltage; hence, the repetition rate is the circuit's only degree of freedom to maintain feedback. Comparator C1 pumps uniform packets of charge to its negative input at a repetition rate precisely proportional to the input voltage derived current. This action ensures that circuit output frequency is strictly and solely determined by the input voltage.

Start-up or input overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; C2, detecting this via the 2.7M/0.1 μ F lag, goes high. This lifts C1's positive input and grounds the negative input with Q7, initiating normal circuit action.

Figure 5 shows the circuit's power consumption versus frequency. Zero frequency current is just 15 μ A, increasing to only 26 μ A at 10kHz.

A detailed description of this circuit's operation appears in the August 1996 issue of *Linear Technology* magazine.

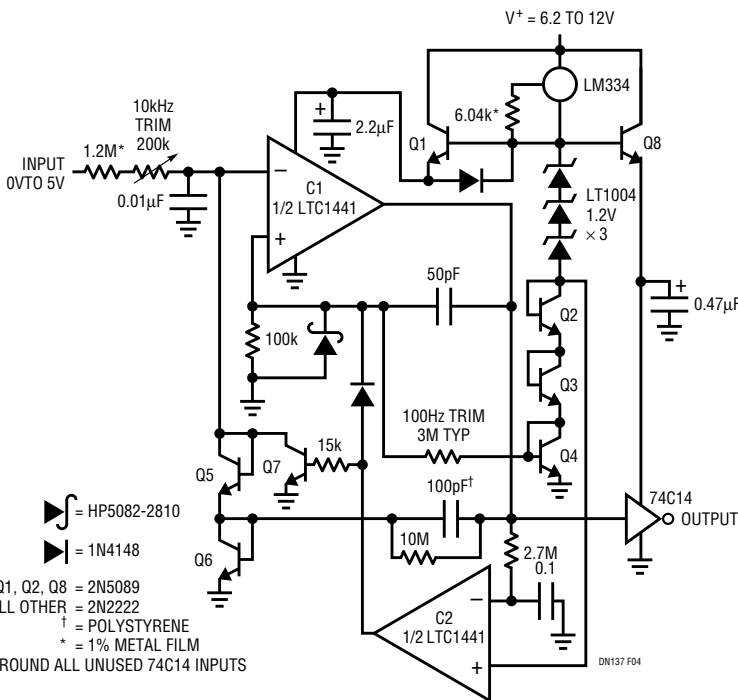


Figure 4. LTC1441-Based 0.02% V/F Converter Requires Only 26 μ A Supply Current

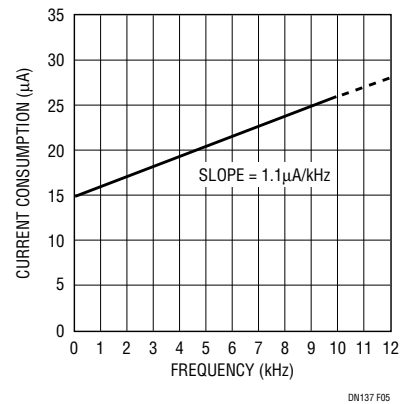
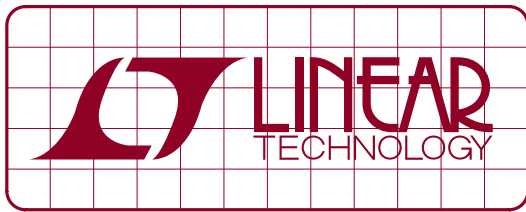


Figure 5. Current Consumption vs Frequency for the V-to-F Converter. Discharge Cycles Dominate 1.1 μ A/kHz Current Drain Increase

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DESIGN NOTES

1 μ A Op Amp Permits Precision Portable Circuitry – Design Note 163

Mitchell Lee and Jim Williams

A new dual op amp with only 1 μ A power consumption and precision DC specifications permits high performance portable applications. The LT[®]1495 has 375 μ V offset, 2 μ V/ $^{\circ}$ C drift, 1nA bias current and 100dB of open-loop gain. These attributes, combined with careful design, make portable, high performance circuitry possible.

5.5 μ A, 0.05 μ V/ $^{\circ}$ C Chopped Amplifier

Figure 1 shows a chopped amplifier requiring only 5.5 μ A supply current. Offset voltage is 5 μ V, with 0.05 μ V/ $^{\circ}$ C drift. Gain exceeding 10⁸ affords high accuracy, even at large closed-loop gains.

Micropower comparators C1A and C1B form a biphas 5Hz clock. The clock drives the input-related switches, causing an amplitude modulated version of the DC input to appear at A1A's input. AC-coupled A1A takes a gain of 1000, presenting its output to a switched demodulator similar to the aforementioned modulator.

The demodulator output, a reconstructed, DC amplified version of the circuit's input, feeds DC gain stage A1B. A1B's output is fed back, via gain setting resistors, to the input modulator, closing a feedback loop around the entire

amplifier. Amplifier gain is set by the feedback resistor's ratio, in this case 1000.

The circuit's internal AC coupling prevents A1's DC characteristics from influencing overall DC performance, accounting for the extremely low offset errors noted.

The desired micropower operation and A1's bandwidth dictate the 5Hz clock rate. As such, resultant overall bandwidth is *low*. Full power bandwidth is 0.05Hz with a slew rate of about 1V/s. Clock related noise, about 5 μ V, can be reduced by increasing C_{COMP}, with commensurate bandwidth reduction.

0.03% Linear V/F Converter with 13 μ A Power Drain

Figure 2's voltage-to-frequency converter takes full advantage of the LT1495's low power consumption. A 0V to 2.5V input produces a 0Hz to 10kHz output, with 0.03% linearity, 250ppm/ $^{\circ}$ C drift and 10ppm/V supply rejection. Maximum current consumption is only 13 μ A, 200 times lower than currently available ICs. Comparator C1 switches a charge pump comprising D1, D2 and the 100pF capacitor to maintain its negative input at 0V. A1 and associated components form a temperature compensating reference for the charge

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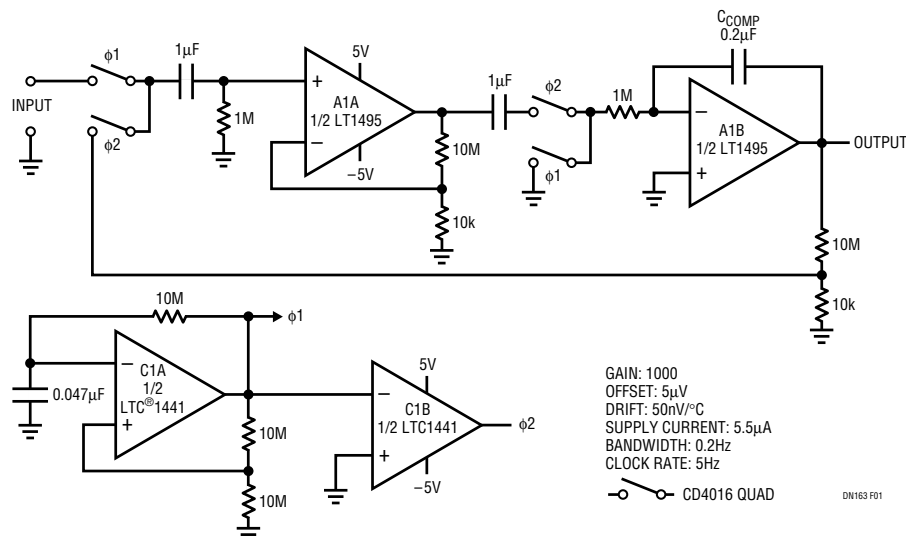


Figure 1. 0.05 μ V/ $^{\circ}$ C Chopped Amplifier Consumes 5.5 μ A Supply Current

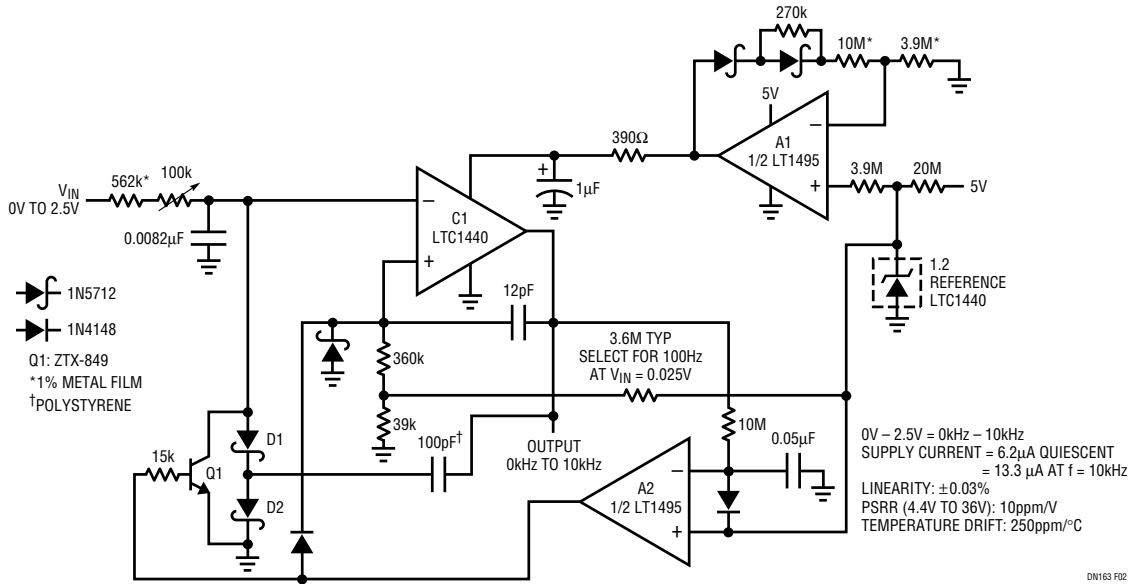


Figure 2. 0kHz to 10kHz Voltage to Frequency Converter Consumes Only 13µA

pump. The 100pF capacitor charges to a fixed voltage; hence, the switching repetition rate is the circuit's only degree of freedom to maintain feedback. Comparator C1 pumps uniform packets of charge to its negative input at a repetition rate precisely proportional to the input voltage derived current. This action ensures that circuit output frequency is strictly and solely determined by the input voltage.

Start-up or input overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; A2, detecting this via the 10M/0.05µF lag, goes high. This lifts C1's positive input and grounds the negative input with Q1, initiating normal circuit action.

Portable Reference

A final circuit is Figure 3's unique portable reference, which draws only 16µA from a pair of AAA alkaline cells. Battery life is five years—equivalent to shelf life.

Two outputs are provided: a buffered, 1.5V voltage output and a regulated 1.5µA current source. The current source compliance ranges from approximately 1V to -43V.

The LT1634A reference is self-biased, completely eliminating line regulation as a concern. Start-up is guaranteed by the LT1495 op amp, whose output initially saturates at 11mV from the negative rail. The 1µA current output is derived from a fraction of the reference voltage impressed across R3.

Note that the portable reference's current output can be pulled well below common, limited only by Q1's 45V breakdown. The 1.5V output can source or sink up to 700µA and is current limited to protect batteries in case of a short circuit.

Once it is powered, there is no reason to turn the circuit off. One AAA alkaline contains 1200mAH capacity, enough to power the circuit through the five year shelf life of the battery.

The voltage output accuracy is about 0.17% and the current output accuracy is about 1.2%. Trim R1 to calibrate voltage (0.1%/kΩ) and R3 to calibrate the output current (0.4%/kΩ).

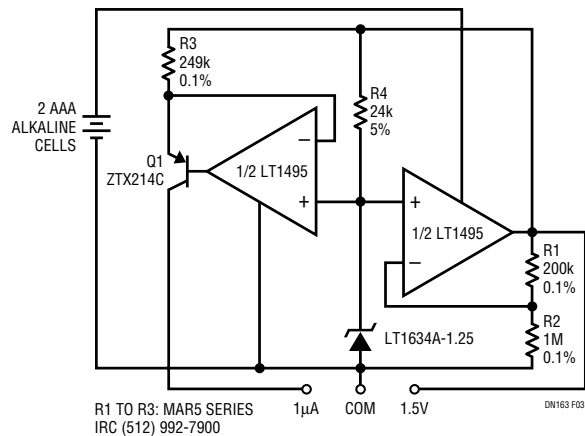
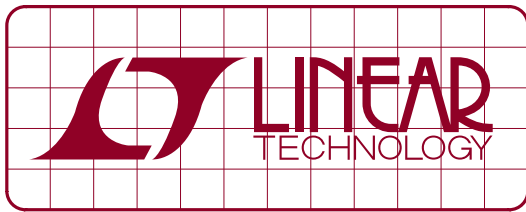


Figure 3. Portable Reference Operates Five Years on One Pair of AAA Cells

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DESIGN NOTES

High Power CCFL Backlight Inverter for Desktop LCD Displays

Design Note 164

Jim Williams

Large LCD (liquid crystal display) displays designed to replace CRTs (cathode ray tubes) in desktop computer applications are becoming available. The LCD's reduced size and power requirements allow much smaller product size, a highly desirable feature.

CRT replacement requires a 10W to 20W inverter to drive the CCFL (cold cathode fluorescent lamp) that illuminates the LCD. Additionally, the inverter must provide the wide

dimming range associated with CRTs, and it must have safety features to prevent catastrophic failures.

Figure 1's circuit meets these requirements. It is a modified, high power variant of an approach employed in laptop computer displays¹. T1, Q1, Q2 and associated components form a current fed, resonant Royer converter that produces high voltage at T1's secondary. Current flows

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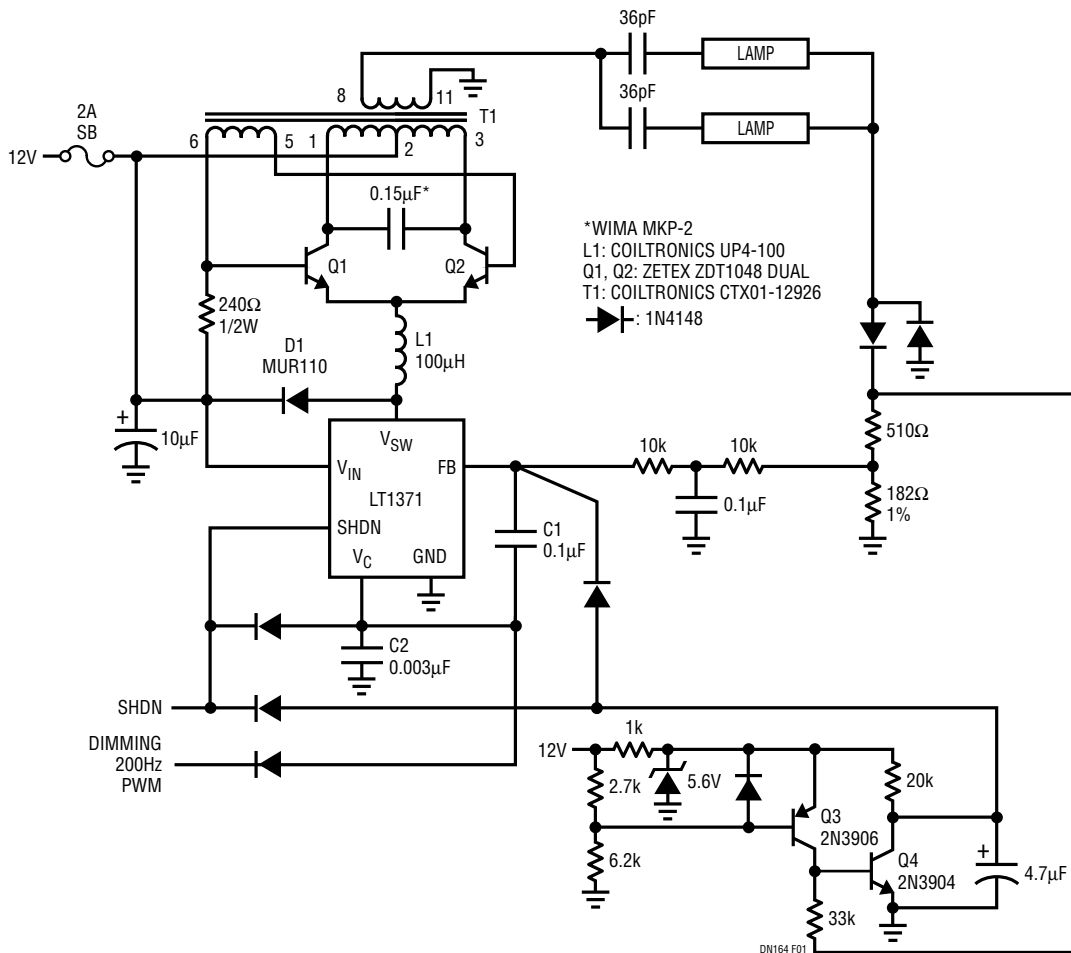


Figure 1. 12W CCFL Backlight Inverter for Desktop Displays Provides Wide Range Dimming and Safety Features

through the CCFL tubes and is summed, rectified and filtered, providing a feedback signal to the LT[®]1371 switching regulator. The LT1371 delivers switched mode power to the L1–D1 node, closing a control loop around the Royer converter. The 182Ω resistor provides current-to-voltage conversion, setting the lamp current operating point. The loop stabilizes lamp current against variations in time,

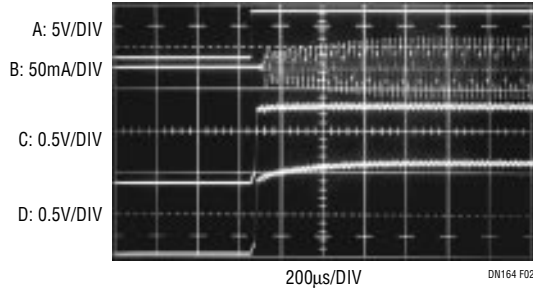


Figure 2. Fast Loop Response Maintains Regulation at 200Hz PWM Rate. Waveforms Include PWM Command (A), Lamp Current (B), LT1371 Feedback (C) and Error Amplifier V_C (D) Pins. Loop Settling Occurs in 500µs

supply, temperature and lamp characteristics. The LT1371's frequency compensation is set by C1 and C2. The compensation responds quickly enough to permit the 200Hz PWM input to control dimming over a 30:1 range with no degradation in loop regulation. Applicable waveforms appear in Figure 2.

Q3 and Q4 shut down the circuit if lamp current ceases (open or shorted lamps or leads, T1 failure or similar malfunction). Normally, Q4's collector is held near ground by the lamp-current-derived base biasing. If lamp current ceases, Q4's collector voltage increases, overdriving the feedback node and shutting down the circuit. Q3 prevents unwanted shutdown during power supply turn-on by driving Q4's base until supply voltage is above about 7V.

Figure 3 shows the shutdown circuit reacting to the loss of lamp feedback. When lamp feedback ceases, the voltage across the 182Ω current sense resistor drops to zero (visible between Figure 3's 2nd and 3rd vertical graticule lines, trace A). The LT1371 responds to this open-loop condition by driving the Royer converter to full power (Q1's collector is trace B). Simultaneously, Q4's collector (trace C) ramps up, overdriving the LT1371's feedback node in about 50ms. The LT1371 stops switching, shutting off the Royer converter drive. The circuit remains in this state until the failure has been rectified.

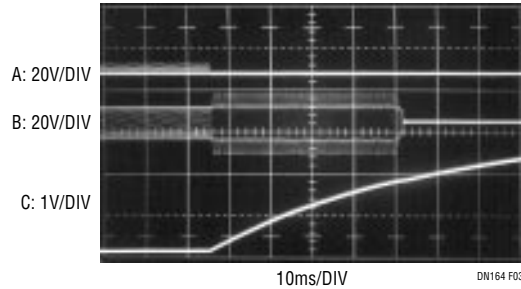
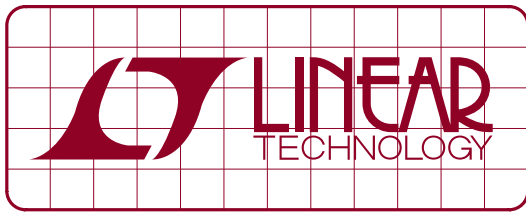


Figure 3. Safety Feature Reacts to Lamp Feedback Loss by Shutting Down Power. Lamp Current Dropout (Trace A) Allows Monitoring Circuit to Ramp Up (Trace C), Shutting Off Drive (Trace B)

This circuit's combination of features provides a safe, simple and reliable high power CCFL lamp drive. Efficiency is in the 85% to 90% range. The closed-loop operation ensures maximum lamp life while permitting extended dimming range. The safety feature prevents excessive heating in the event of malfunction and the use of off-the-shelf components allows ease of implementation.

1. See LTC Application Note 65, *A Fourth Generation of LCD Backlight Technology*.

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DESIGN NOTES

A Seven Nanosecond Comparator for Single-Supply Operation

Design Note 185

Jim Williams

The LT[®]1394—An Overview

A new ultrahigh speed, single-supply comparator, the LT1394, features TTL-compatible complementary outputs and 7ns response time. Other capabilities include a latch pin and good DC input characteristics (see Figure 1). The LT1394's outputs directly drive all 5V families, including the higher speed ASTTL, FAST and HC parts. Additionally, TTL outputs make the device easier to use in linear circuit applications where ECL output levels are often inconvenient.

A substantial amount of design effort has made the LT1394 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1394 is stable in its linear region. Additionally, output-stage switching does not appreciably change power supply current, further enhancing stability. Finally, current consumption is far lower than that of previous devices. These features make the 200GHz gain bandwidth LT1394 considerably easier to apply than other fast comparators.

This device permits fast circuit functions that are difficult or impractical using other approaches. Two applications are presented here.

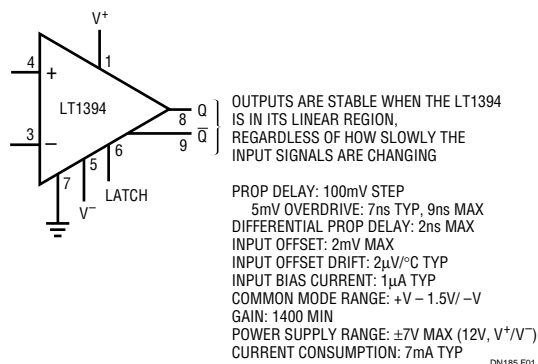


Figure 1. The LT1394 at a Glance

4× NTSC Subcarrier Tunable Crystal Oscillator

Figure 2, a variant of a basic crystal oscillator, permits voltage tuning the output frequency. Such voltage-controlled crystal oscillators (VCXO) are often employed where slight variation of a stable carrier is required. This example is specifically intended to provide a 4× NTSC subcarrier tunable oscillator suitable for phase locking.

The LT1394 is set up as a crystal oscillator. The varactor diode is biased from the tuning input. The tuning network is arranged so a 0V to 5V drive provides a reasonably symmetric, broad tuning range around the 14.31818MHz center frequency. The indicated selected capacitor sets tuning bandwidth. It should be picked to complement loop response in phase locking applications. Figure 3 is a plot of tuning input voltage frequency deviation. Tuning deviation from the 4× NTSC 14.31818MHz center frequency exceeds ±240ppm for a 0V to 5V input.

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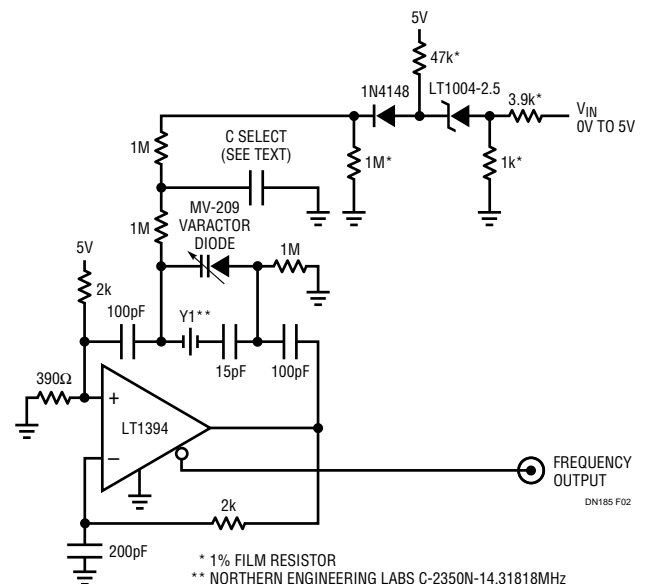


Figure 2. A 4× NTSC Subcarrier Voltage-Tunable Crystal Oscillator. Tuning Range and Bandwidth Accommodate a Variety of Phase Locked Loops

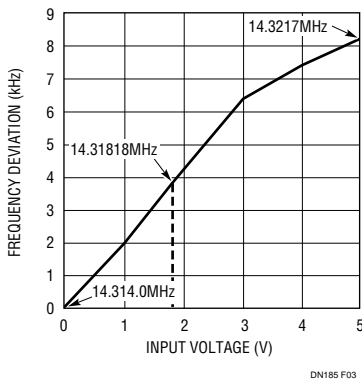


Figure 3. Control Voltage vs Output Frequency for Figure 2. Tuning Deviation from Center Frequency Exceeds ± 240 ppm

High Speed Adaptive Trigger Circuit

Line and fiber-optic receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 4 triggers on 2mV to 175mV signals from 100Hz to 45MHz while operating from a single 5V rail. A1, operating at a gain of 15, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's output signal appears at the junction of the 500pF capacitor and the 3M Ω units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive

voltage is buffered by A2 to set the trigger voltage at the LT1394's positive input. The LT1394's negative input is biased directly from A1's output. The LT1394's output, the circuit's output, is unaffected by $>85:1$ signal amplitude variations. Bandwidth limiting in A1 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

Figure 5 shows operating waveforms at 40MHz. Trace A's input produces Trace B's amplified output at A1. The comparator's output is Trace C.

Additional applications and a tutorial on high speed comparator circuitry can be found in Application Note 72, "A Seven Nanosecond Comparator for Single-Supply Operation."

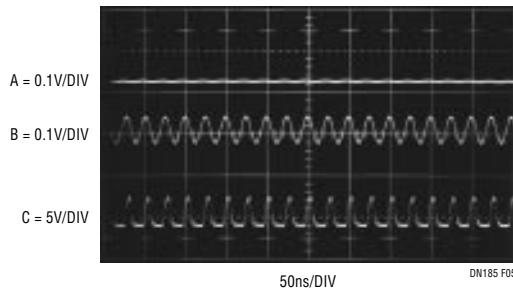


Figure 5. Adaptive Trigger Responding to a 40MHz, 5mV Input. Input Amplitude Variations from 2mV to 175mV are Accommodated

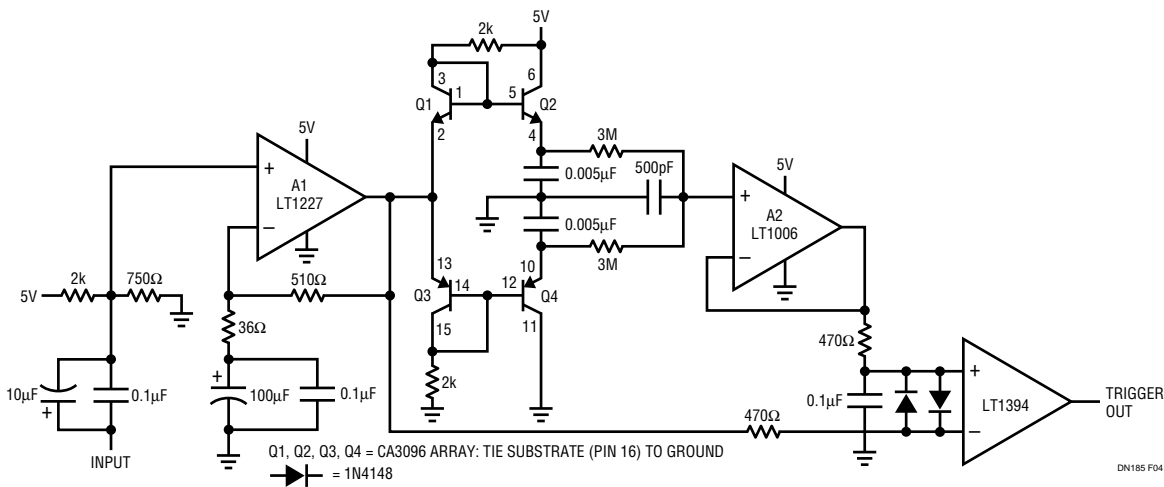
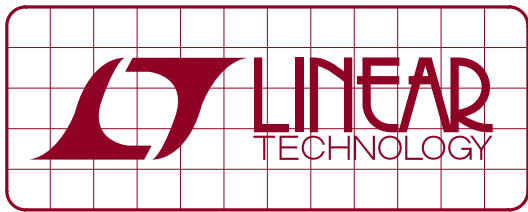


Figure 4. 45MHz Single-Supply Adaptive Trigger. Output Comparator's Threshold Varies Ratiometrically with Input Amplitude, Maintaining Data Integrity over $>85:1$ Input Amplitude Range

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DESIGN NOTES

Op Amp, Comparator and Reference IC Provides Micropower Monitoring Capability – Design Note 190

Jim Williams

Introduction

The LTC[®]1541 combines a micropower amplifier, comparator and 1.2V reference in an 8-pin package. The part operates from a single 2.5V to 12.6V supply with typical supply current of 5 μ A. Both op amp and comparator feature a common mode input voltage range that extends from the negative supply to within 1.3V of the positive supply. The op amp output stage swings from rail-to-rail. Figure 1 lists additional features along with a block diagram of the device. The part's attributes suggest low power monitoring applications and two such circuits are presented here.

Pilot Light Flame Detector with Low-Battery Lockout

Figure 2 shows a pilot light flame detector with low-battery lockout. The amplifier ("A"), running open loop, compares

a small portion of the reference with the thermocouple-generated voltage. When the thermocouple is hot, the amplifier's output swings high, biasing Q1 on. Hysteresis, provided by the 10M resistor, ensures clean transitions, while the diodes clamp static generated voltages to the rails. The 100k–2.2 μ F RC filters the signal to the amplifier.

The comparator ("C") monitors the battery voltage via the 2M–1M divider and compares it to the 1.2V reference. A battery voltage above 3.6V holds C's output high, biasing Q2 on and maintaining the small potential at A's negative input. When the battery voltage drops too low, C goes low, signaling a low-battery condition. Simultaneously, Q2 goes off, causing A's negative input to move to 1.2V. This biases A low, shutting off Q1. The low outputs alert downstream circuitry to shut down gas flow.

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SUPPLY RANGE: 2.5V TO 12.6V
 I_{QUIESCENT}: 5 μ A
 OP AMP V_{OS}: 700 μ V
 COMPARATOR V_{OS}: 1mV
 COMPARATOR HYSTERESIS: \pm 3mV
 COMMON MODE RANGE: 0V TO (V_{SUPPLY} – 1.3V)
 INPUT BIAS CURRENT: 1nA MAX, 10pA (25°C) TYP
 REFERENCE: 1.2V \pm 0.4%

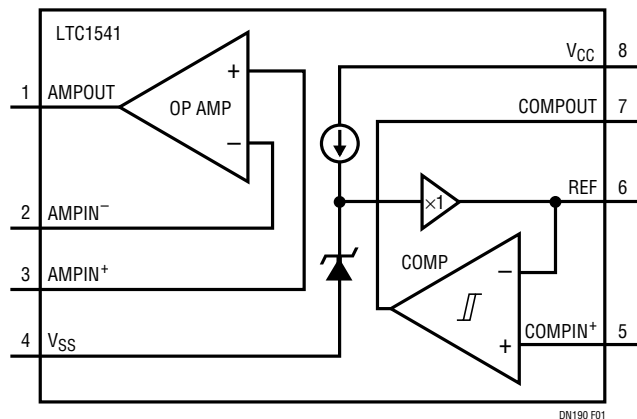


Figure 1. LTC1541 Block Diagram and Features of the Micropower Op Amp, Comparator and Reference

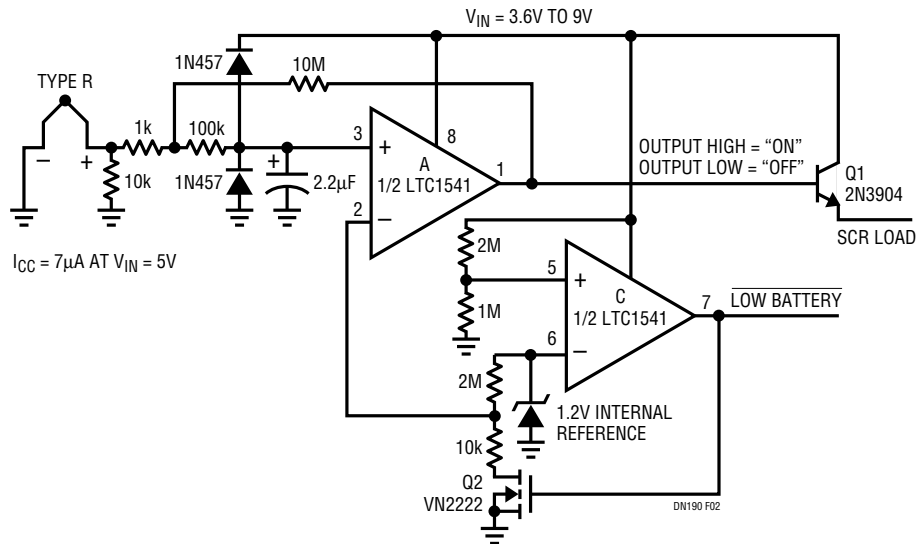


Figure 2. Pilot Light Flame Detector with Low-Battery Lockout

Tip-Acceleration Detector for Shipping Containers

Figure 3's circuit is a tip-acceleration detector for shipping containers. It detects if a shipping container has been subjected to excessive tipping or acceleration and retains the detected output. The sensitivity and frequency response are adjustable. A potentiometer with a small pendulous mass biases the amplifier ("A"), operating at a gain of 12. Normally, A's output is below C's trip point and circuit output is low. Any tip-acceleration event that causes A's

output to swing beyond 1.2V will trip C high. Positive feedback around C will latch it in this high state, alerting the receiving party that the shipped goods have been mis-handled. Sensitivity is variable with potentiometer mechanical or electrical biasing or A's gain. Bandwidth is settable by selection of the capacitor at A's input. The circuit is prepared for use by applying power and pushing the button in C's output.

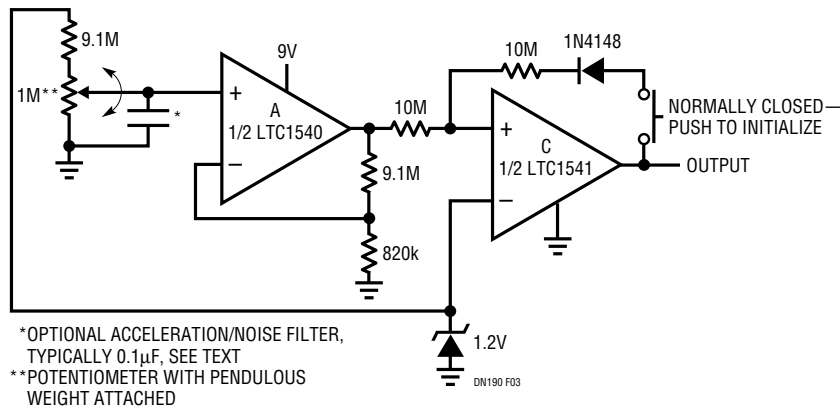
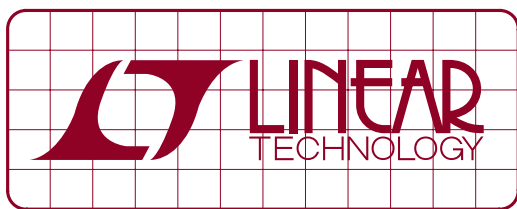


Figure 3. Tip-Acceleration Detector for Shipping Containers Retains Output if Triggered. Sensitivity is Adjustable Via Amplifier Feedback Values. Capacitor Sets Acceleraton Response Bandwidth

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DESIGN NOTES

Lowest Noise SOT-23 LDOs Have 20 μ A Quiescent Current, 20 μ V_{RMS} Noise – Design Note 220

Todd Owen and Jim Williams

Telecom and instrumentation applications often require a low noise voltage regulator. Frequently this requirement coincides with the need for low regulator dropout and small quiescent current. LTC recently introduced a family of devices to address this problem. Table 1 shows a variety of packages, power ranges and features in three basic regulator types. The SOT-23 packaged LT[®]1761 has only 20 μ V_{RMS} noise with 300mV dropout at 100mA. Quiescent current is only 20 μ A.

Applying the Regulators

Applying the regulators is simple. Figure 1 shows a minimum parts count, 3.3V output design. This circuit appears similar to conventional approaches with a no-

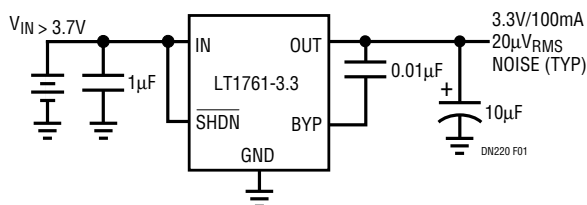


Figure 1. Applying the Low Noise, Low Dropout, Micropower Regulator. Bypass Pin and Associated Capacitor are Key to Low Noise Performance

table exception: a bypass pin (BYP) is returned to the output via a 0.01 μ F capacitor. This path filters the internal reference's output, minimizing regulator output noise. It is the key to the 20 μ V_{RMS} noise performance. A shutdown pin (SHDN), when pulled low, turns off the regulator output while keeping current drain inside 1 μ A. Dropout characteristics appear in Figure 2. Dropout scales with output current, falling to less than 100mV at low currents.

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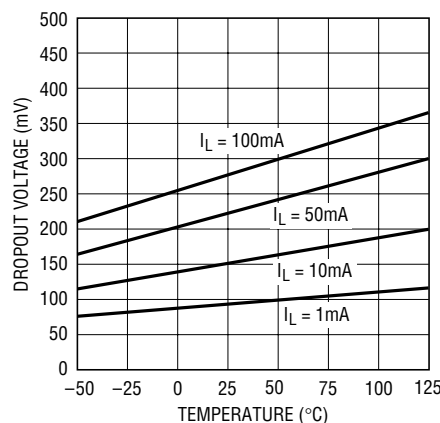


Figure 2. Figure 1's Dropout Voltage at Various Currents

Table 1. Low Noise LDO Family Short-Form Specifications. Quiescent Current Scales with Output Current Capability, Although Noise Performance Remains Constant

REGULATOR TYPE	OUTPUT CURRENT	RMS NOISE (10Hz to 100kHz) $C_{BYP} = 0.01\mu F$	PACKAGE OPTIONS	FEATURES	QUIESCENT CURRENT	SHUTDOWN CURRENT
LT1761	100mA	20 μ V	SOT-23	Shutdown, Reference Bypass, Adjustable Output. SOT-23 Package Mandates Selecting Any Two Features	20 μ A	<1 μ A
LT1762	150mA	20 μ V	MS8	Shutdown, Reference Bypass, Adjustable Output	25 μ A	<1 μ A
LT1763	500mA	20 μ V	SO-8	Shutdown, Reference Bypass, Adjustable Output	30 μ A	<1 μ A

Noise Performance

Noise performance is displayed in Figure 3. This measurement was taken in a 10Hz to 100kHz bandwidth with a “brick wall” multipole filter¹. The photo’s trace, applied to a thermally responding RMS voltmeter, contains less than $20\mu\text{V}_{\text{RMS}}$ noise. Figure 4 shows noise in the frequency domain with noise power falling with increasing frequency.

Other Advantages

The LT1761 family is stable (no output oscillation) even when used with low ESR ceramic output capacitors. This is in stark contrast to LDO regulators from other manufacturers that often oscillate with ceramic capacitors.

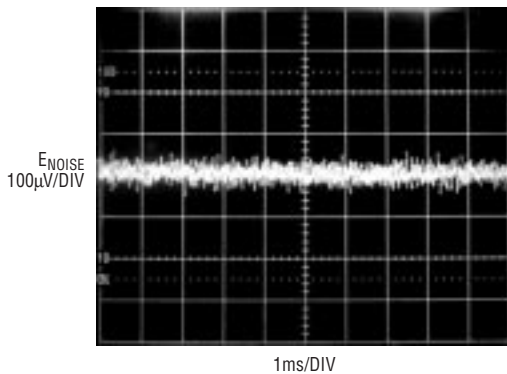


Figure 3. LT1761 Output Voltage Noise in a 10Hz to 100kHz Bandwidth. $20\mu\text{V}_{\text{RMS}}$ Noise is the Lowest Available in an LDO

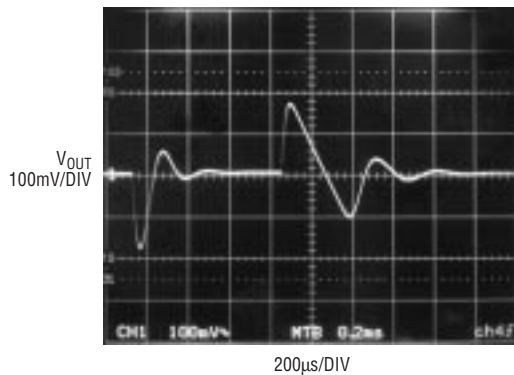


Figure 5. Transient Response with No Noise Bypass Capacitor

The unique internal architecture provides an added bonus in transient performance when adding a $0.01\mu\text{F}$ noise capacitor. Transient response for a 10mA to 100mA step with a $10\mu\text{F}$ output capacitor is shown in Figure 5. Figure 6 shows the same setup with the addition of a $0.01\mu\text{F}$ bypass capacitor. Settling time and amplitude are markedly reduced.

Conclusion

These devices provide the lowest available output noise in a low dropout regulator without compromising other parameters. Their performance, ease of use and versatility allow use in a variety of noise-sensitive applications.

¹Noise measurement and specification of regulators requires care and will be comprehensively treated in a forthcoming LTC Application Note.

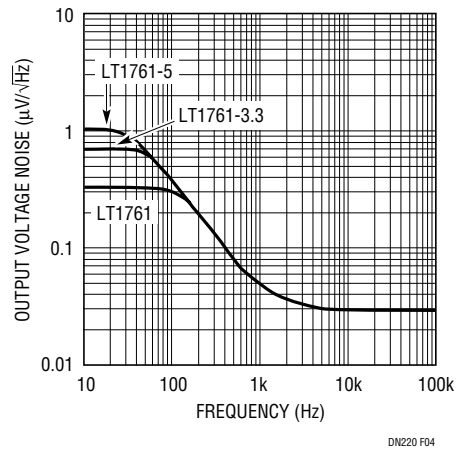


Figure 4. Output Noise Spectral Density for Figure 1’s Circuit. Curves for Three Output Versions Show Dispersion Below 200Hz

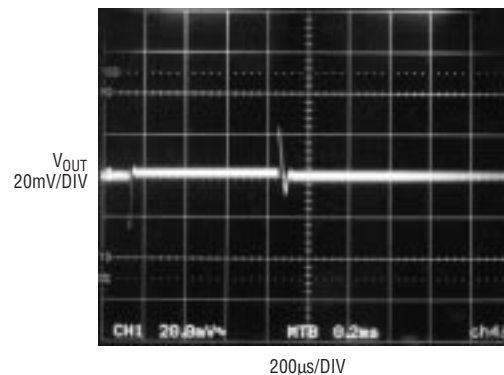
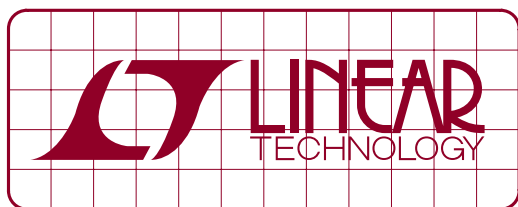


Figure 6. Noise Bypass Capacitor Improves Transient Response. Note Change in Voltage Scale

Data Sheet Download

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DESIGN NOTES

Basic Flashlamp Illumination Circuitry for Cellular Telephones/Cameras – Design Note 345

Jim Williams

Introduction

Next generation cellular telephones will include high quality photographic capability. Flashlamp-based lighting is crucial for good photographic performance. A previous full-length Linear Technology publication detailed flash illumination issues and presented flash circuitry equipped with “red-eye” reduction capability.^{1,2} Some applications do not require this feature; deleting it results in an extremely simple and compact flashlamp solution.

Flashlamp Circuitry

Figure 1’s circuit consists of a power converter, flashlamp, storage capacitor and an SCR-based trigger. In operation the LT[®]3468-1 charges C1 to a regulated 300V at about 80% efficiency. A “trigger” input turns the SCR on, depositing C2’s charge into T2, producing a high voltage trigger event at the flashlamp. This causes the lamp to conduct high current from C1, resulting in an intense flash of light. LT3468-1 associated waveforms, appearing in

Figure 2, include trace A, the “charge input,” going high. This initiates T1 switching, causing C1 to ramp up (trace B). When C1 arrives at the regulation point, switching ceases and the resistively pulled-up “DONE” line drops low (trace C), indicating C1’s charged state. The “TRIGGER” command (trace D), resulting in C1’s discharge via the lamp, may occur any time (in this case $\approx 600\text{ms}$) after “DONE” goes low. Normally, regulation feedback would be provided by resistively dividing down the output voltage. This approach is not acceptable because it would require excessive switch cycling to offset the feedback resistor’s constant power drain. While this action would maintain regulation, it would also drain excessive power from the primary source, presumably a battery. Regulation is instead obtained by monitoring T1’s flyback pulse characteristic, which reflects T1’s secondary amplitude.

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Note 1. See LTC Application Note 95, “Simple Circuitry for Cellular Telephone/Camera Flash Illuminator” by Jim Williams and Albert Wu, March 2004.

Note 2. “Red-eye” in a photograph is caused by the human retina reflecting the light flash with a distinct red color. It is eliminated by causing the eye’s iris to constrict in response to a low intensity flash immediately preceding the main flash.

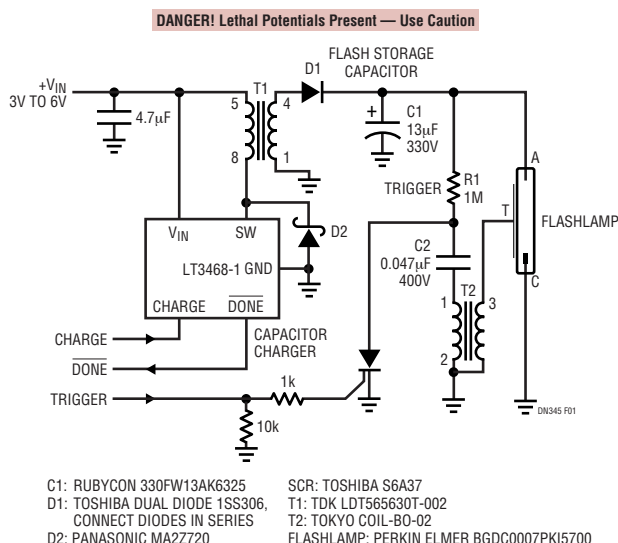
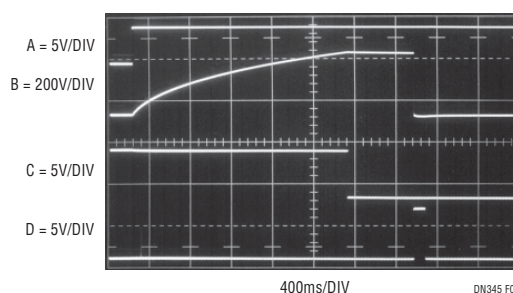


Figure 1. Complete Flashlamp Circuit Includes Capacitor Charging Components, Flash Capacitor C1, Trigger (R1, C2, T2, SCR) and Flashlamp. TRIGGER Command Biases SCR, Ionizing Lamp via T2. Resultant C1 Discharge Through Lamp Produces Light



The output voltage is set by T1's turns ratio. This feature permits tight capacitor voltage regulation, necessary to ensure consistent flash intensity without exceeding lamp energy or capacitor voltage ratings. Also, flashlamp energy is conveniently determined by the capacitor value without any other circuit dependencies.

Figure 3 shows high speed detail of the high voltage trigger pulse (trace A), the flashlamp current (trace B) and the light output (trace C). Some amount of time is required for the lamp to ionize and begin conduction after triggering. Here, $3\mu\text{s}$ after the $4\text{kV}_{\text{p-p}}$ trigger pulse, flashlamp current begins its ascent to over 100A. The current rises smoothly in $3.5\mu\text{s}$ to a well defined peak before beginning its descent. The resultant light produced rises more slowly, peaking in about $7\mu\text{s}$ before decaying. Slowing the oscilloscope sweep permits capturing the entire current and light events. Figure 4 shows that light output (trace B) follows lamp current (trace A) profile, although current peaking is more abrupt. Total event duration is $\approx 200\mu\text{s}$ with most energy expended in the first $100\mu\text{s}$.

Conclusion

The circuit presented constitutes a basic, but high performance, flash illumination solution. Its low power, small size and few components suit cellular telephone/camera applications where size and power drain are important. It provides a practical, readily adaptable path to accessing flashlamp-based illumination's photographic advantages.

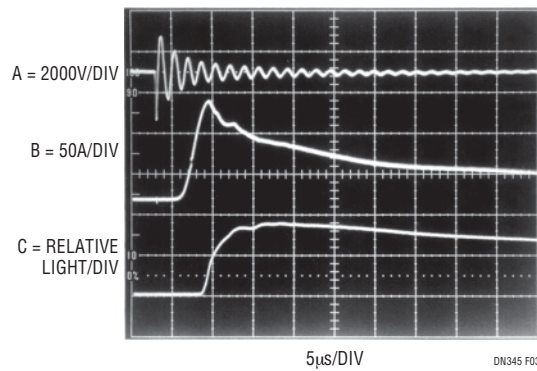


Figure 3. High Speed Detail of Trigger Pulse (Trace A), Resultant Flashlamp Current (Trace B) and Relative Light Output (Trace C). Current Exceeds 100A After Trigger Pulse Ionizes Lamp

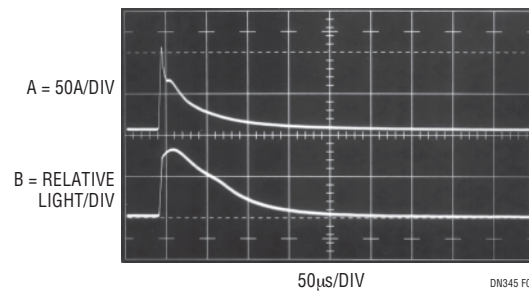


Figure 4. Photograph Captures Entire Current (Trace A) and Light (Trace B) Events. Light Output Follows Current Profile Although Peaking is Less Defined. Waveform Leading Edges Enhanced for Figure Clarity

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Testing Linearity of the LTC2400 24-Bit No Latency $\Delta\Sigma$ ™ A/D Converter

Help from the Nineteenth Century

by Jim Williams

Introduction

Verifying the linearity of the LTC2400 analog to digital converter requires special considerations. Typical nonlinearity is only 2ppm (0.0002%). Bench testing this necessitates some form of voltage source that produces equal amplitude output steps for incremental digital inputs. Additionally, for measurement confidence, it is desirable that the source be substantially more linear than the 2ppm requirement. This is, of course, a stringent demand and painfully close to the state of the art.

The most linear “D to A” converter is also one of the oldest: Lord Kelvin’s Kelvin-Varley divider (KVD), in its most developed form, is linear to 0.1ppm. This manually switched device features ten million individual dial settings arranged in seven decades. It may be thought of as a 3-terminal potentiometer with fixed “end-to-end” resistance and a 7-decade switched wiper position (Figure 1).

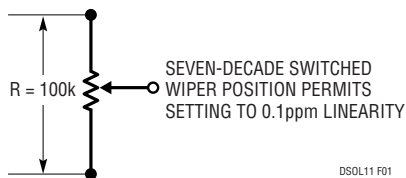


Figure 1. Conceptual Kelvin-Varley Divider

The actual construction of a 0.1ppm KVD is more artistry and witchcraft than science. The market is relatively small, the number of vendors few and resultant price high. Imagine paying \$13,000 for a bunch of switches and resistors. If this seems offensive, try building and certifying your own KVD. Figure 2 shows a detailed schematic.

The KVD shown has a 100k Ω input impedance. A consequence of this is that wiper output resistance is high and varies with setting. As such, a very high input resistance

follower is required to unload the KVD without introducing significant loading error. Now, our KVD looks like Figure 3.

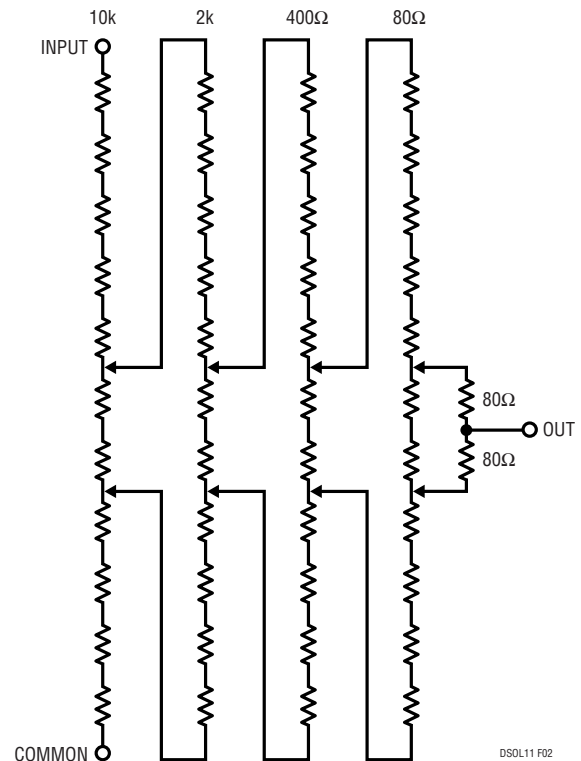
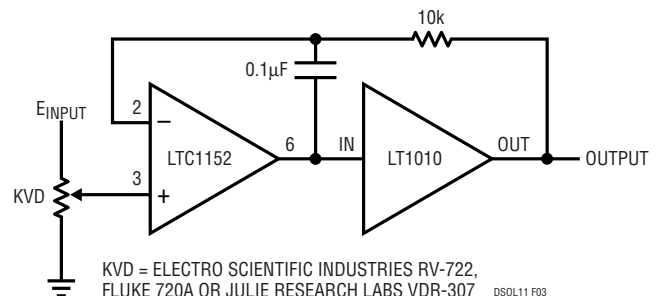


Figure 2. A 4-Decade Kelvin-Varley Divider. Additional Decades Are Implemented By Opening Last Switch, Deleting Two Associated 80 Ω Values and Continuing $\div 5$ Resistor Chains



KVD = ELECTRO SCIENTIFIC INDUSTRIES RV-722, FLUKE 720A OR JULIE RESEARCH LABS VDR-307 DSOL11 F03

Figure 3. KVD with Buffer Gives Output Drive Capability

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Design Solutions 11

This schematic is deceptively simple. In practice, construction details are crucial. Parasitic thermocouples (Seebeck effect), layout, grounding, shielding, guarding, cable choice and other issues affect achievable performance. In fact, as good as the chopper-stabilized LTC1152 is with respect to drift, offset, bias current and CMRR, selection is required if we seek sub-ppm nonlinearity performance. Figure 4, an error budget analysis, details some of the selection criteria.

In Figure 5, we can add offset trim, a second KVD and a stable voltage source to drive the main KVD. Additionally, an ensemble of three HP3458A voltmeters monitor the output.

The offset trim bleeds a small current into the main KVD ground return, producing a few microvolts of offset-trim range. This functionally trims out all sources of zero error (amplifier offsets, parasitic thermocouple mismatches and the like), permitting a true zero volt output when the main KVD is set to all zeros.

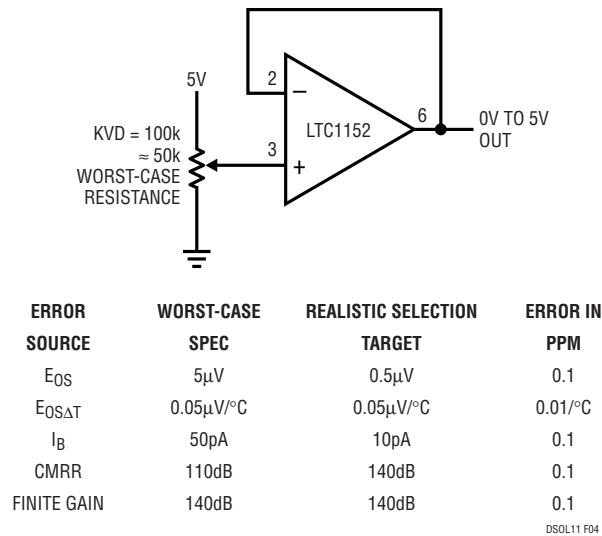


Figure 4. Error Budget Analysis for the KVD Buffer. Selection Permits \approx 0.4ppm Predicted Linearity Error

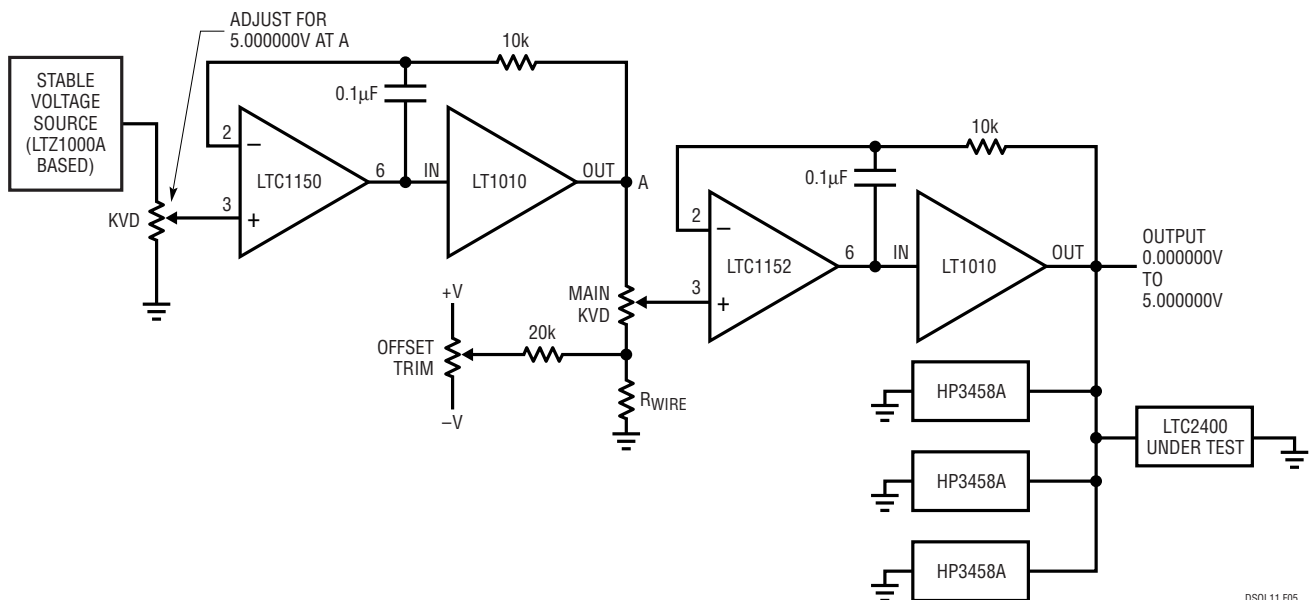


Figure 5. Simplified High Linearity Voltage Source

The voltmeters, specified for <1ppm nonlinearity on the 10V range, “vote” on the source’s output. Figure 6 is a more detailed schematic and Figure 7 highlights issues and concerns.

When studying the approach used, it is essential to differentiate between linearity and absolute accuracy. This eliminates concerns with absolute standards, permitting certain freedoms in the measurement scheme. In particular, although single-point grounding was used, remote sensing was not. This is a deliberate choice, made to minimize the number of potential error-causing parasitic thermocouples in the signal path.

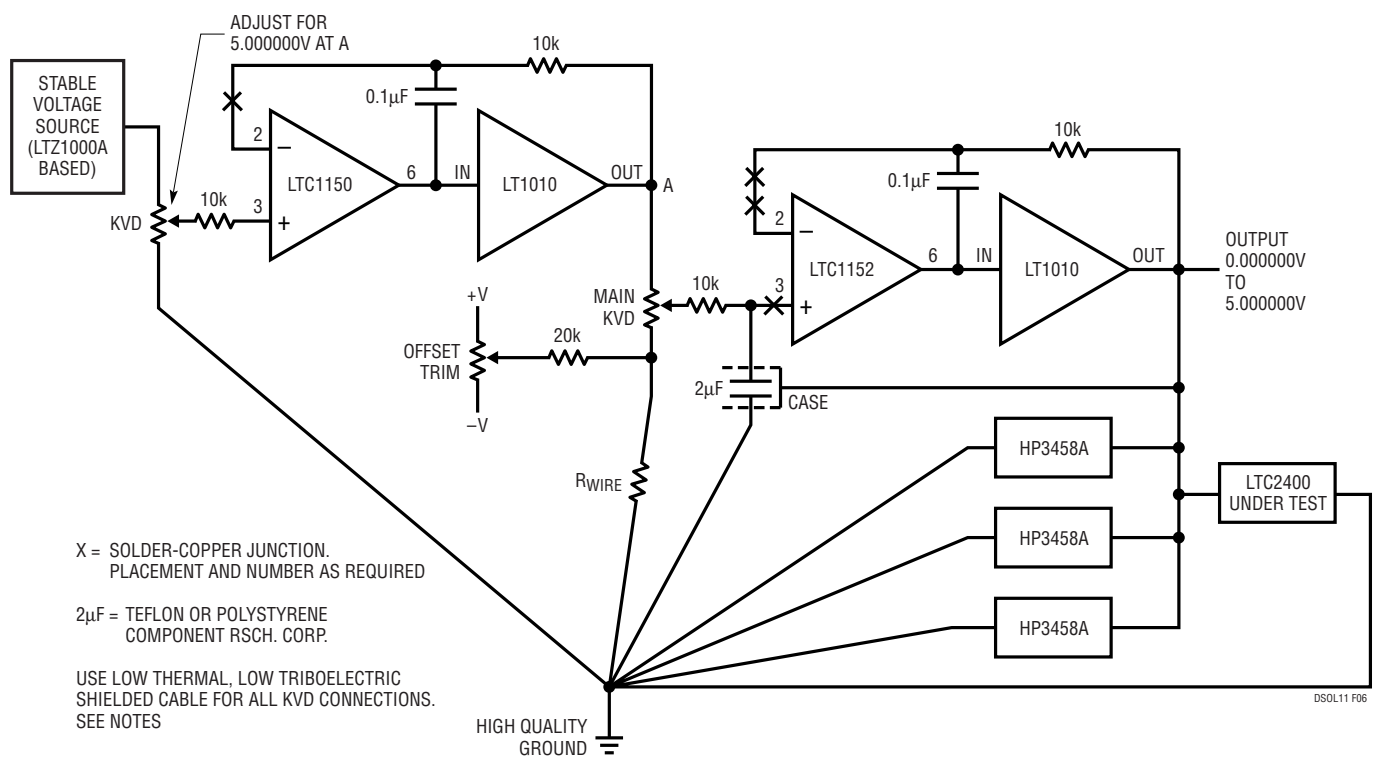


Figure 6. Complete High Linearity Voltage Source

- OFFSET TRIM VIA DRIVING KVD RETURN WIRE
- HIGH QUALITY GROUND
- CABLE CHOICE — GUILDLINE #SCW, KEITHLEY SC-93
- LOW THERMAL LUGS, BANANAS – HP11053, 8.11074
- CRUSH LUGS FOR KVD AND DVM CONNECTIONS
- DELIBERATE SOLDER-COPPER JUNCTIONS
- DRIVEN CASE GUARDS AGAINST CAPACITOR SURFACE LEAKAGE
- “MICROVOLT MAINTENANCE” (DE-OXIT, CAIG LABS)

DSOL11 F07

Figure 7. Voltage Source Notes and Special Attention Areas

Results

This KVD-based, high linearity voltage source has been in use in our lab for about a year. During this period, the total linearity uncertainty defined by the source and its monitoring voltmeters has been just 0.3ppm (see Figure 8). This is almost ten times better than the LTC2400's 2ppm specification, promoting confidence in our measurements.

Acknowledgments

The author is indebted to Lord Kelvin and to Warren Little of the C. S. Draper Laboratory (formerly the M. I. T. Instrumentation Laboratory) standards lab. Warren taught me, with great patience, the wonders of KVDs some thirty years ago and I am still trading on his efforts.

- VERIFY KVD LINEARITY BY INTERCOMPARISON AND INDEPENDENT CAL. LAB.
- TAKE WORST-CASE VOLTMETER ENSEMBLE DEVIATIONS OVER 0V TO 5V, EVERY 0.5V
- 100 RUNS (10 PER DAY, ONCE PER HOUR)
- INDICATED RESULT IS 0.3ppm NONLINEARITY

DSOL11 F08

Figure 8. Linearity Testing Using Repeated Trials with “Voting” Voltmeters